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Measures to mitigate over-frequencies at Songo Rectifier Station

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DECLARATION

I declare that this research report is my own work except as indicated in the references and acknowledgements. It is submitted in fulfilment of the requirements for the degree of Master of Science in the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination in this or any other university.

L Fanoguiço

Signed at Johannesburg

On the ……25…… day of ……July……2022……..

DEDICATION

I dedicate this research project work to my family and friends. Special mention and gratitude to my loving parents, whose words of encouragement and push for excellence and education always give me energy and strength.

ACKNOWLEDGEMENTS

It is with great gratitude that I acknowledge the tremendous support and help of my co-supervisor Professor John Van Coller, for his crucial input and insight which were invaluable for the completion of this dissertation. I would also like to thank my main supervisor Professor Chandima Gomes for his support and guidance on the research project.

LIST OF PRINCIPAL SYMBOLS

AC Alternating Current

Apollo Apollo Inverter Station

BB-I 220 kV AC Busbar I at the Songo Rectifier Station.

BB-II 220 kV AC Busbar II at the Songo Rectifier Station.

BC 220 kV AC Bus Coupler Circuit Breaker at the Songo Rectifier Station.

BESS Battery Energy Storage System

BR Braking Resistor

BSBR Breaker-Switched Braking Resistor

CB Cahora Bassa Hydroelectric power station.

DC Direct Current

EDM Electricidade de Moçambique (Mozambique electric utility).

Eskom South African Electricity Utility

GMPC Grid Master Power Controller

HCB Hidroeléctrica de Cahora Bassa, SA

HVAC High Voltage Alternating Current

HVDC High Voltage Direct Current

PCB Printed Circuit Board

SAPP Southern African Power Pool

SLG Speed Load Governor

Songo Songo Rectifier Station

SST Station Service Transformer

TL Transmission Line

TFR Transient Fault Recorder

TCBR Thyristor Phase-Controlled Braking Resistors

TSBR Thyristor-Switched Braking Resistors

VDCOL Voltage Dependent Current Order Limit

ZESA Zimbabwe Electricity Supply Authority.

Definitions

Converter Bus (BB-I) - 220 kV AC bus where the rectifier bridges are connected.

Non-Converter Bus (BB-II) - 220 kV AC bus where the HVAC transmission lines are connected. The converter bridges are not connected to this bus.

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Chapter 1. INTRODUCTION

1.1. Background

Songo Rectifier Station is located 6 km away from the Cahora Bassa hydroelectric power station in Mozambique. It was designed to transmit 1920 MW of the 2075 MW generated to Apollo Inverter Station in South Africa. Due to the large distance involved (1414 km), power transmission is by means of an HVDC scheme, consisting of two HVDC transmission lines and two converter stations (Songo and Apollo). Therefore, Songo and Apollo hold all the equipment required for power conversion from alternating current into direct current and vice-versa. The rated power transmission of the bipolar HVDC scheme is 1920 MW, consequently line-commutated converters (LCC) were employed.

The Songo Rectifier Station comprises eight three-phase converter bridges consisting of oil-filled (for cooling and insulation) thyristor valves, each rated at 240 MW, and fed by transformers from the 220 kV DC Busbar I (BB-I). Each converter bridge has an output voltage of 133 kV DC. The converter bridges are connected in parallel on the AC side and in series on the DC side. The neutral point on the DC side is connected to earth electrodes located 25 km away from the Songo Rectifier Station, making up two poles (classified as a Bipolar System). Each pole comprises four converter bridges on each side of the neutral point, see Fig. 1.1.

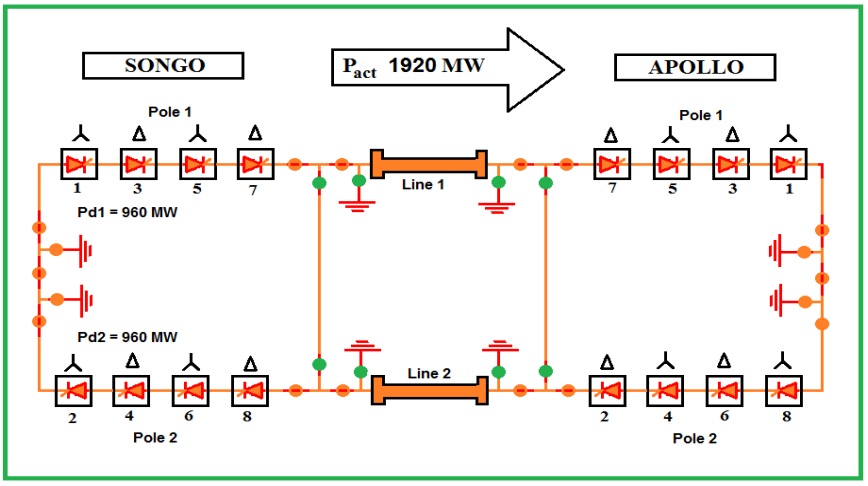


Fig. 1.1: Songo – Apollo HVDC scheme.

Cahora Bassa hydroelectric power station and Songo Rectifier Station were initially designed for islanded operation where the HVDC system was the only load on the generators. In 1993, an HVAC transmission line from Songo to Bindura in Zimbabwe was built as well as an HVAC transmission line from Insukamini to Matimba in South Africa, connecting Songo to Apollo both through HVAC and HVDC lines in parallel [1].

Following the construction of the Songo-Bindura and Matimba-Insukamini tie lines, in October 1999 a new power controller developed by Siemens, the Grid Master Power Controller (GMPC), was installed and commissioned at Songo Rectifier Station [2]. The GMPC was designed for power balance (Automatic Generation Control (AGC) functionality) as well as for dynamic

stability of the Cahora Bassa, ZESA and Eskom interconnections (Power System Stabilizer (PSS) functionality) [1].

In order to provide power supply to the north of Mozambique, there are two 220 kV AC transmission lines of 120 km length (Tete lines), connecting Songo and Matambo substations in the province of Tete, see Fig. 1.2, [3].

In Fig. 1.2 the normal system configuration of Songo Rectifier Station is shown. The three-phase AC Bus (BB-I) to which the converter bridges are connected is called the Converter Bus (BB-I) [2]. The three-phase AC Bus to which the AC transmission lines are connected is called the Non-Converter Bus (BB-II) [2]. The Converter Bus and the Non-Converter Bus are coupled through the bus coupler (BC) circuit breaker. The BC is usually closed. It is the split point for a disturbance occurring during normal operating conditions. Whenever the stability of the system is jeopardized, the BC is tripped to avoid generator pole slipping (generator G1 loaded excessively) and system instability (disturbance on Converter Bus causing a disturbance on the HVAC lines connected to the Non-Converter Bus).

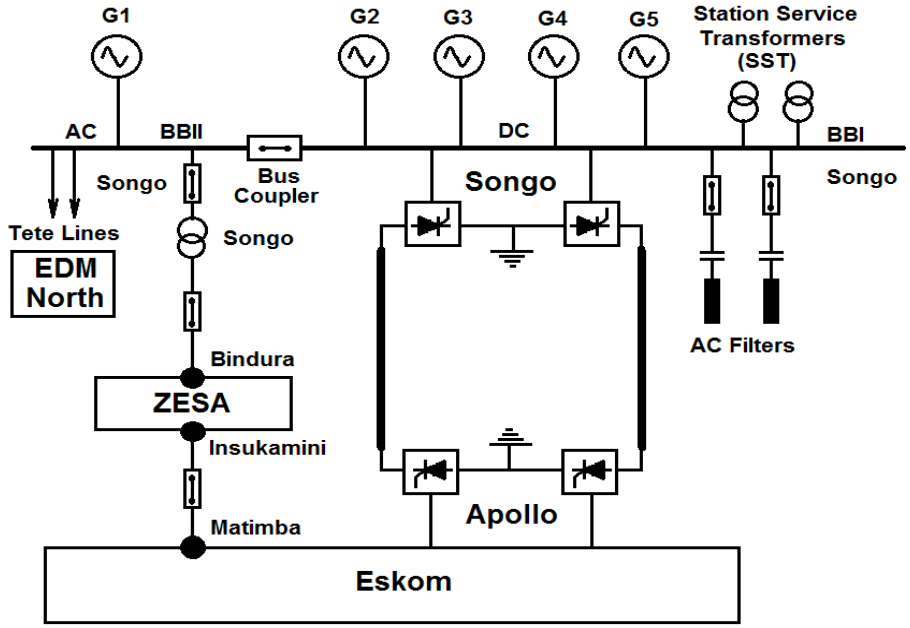


Fig. 1.2: Songo Rectifier Station and the normal system configuration, from reference [2].

At Songo Rectifier Station, the two Station Service Transformers (SSTs) supply auxiliary services critical for the converter operation. Whenever they trip, the entire Songo Rectifier Station also trips. As a result, power transmission to Apollo is halted. In theory the Converter Bus is more reliable than the Non-Converter Bus due to the number of generators connected to it. Therefore, the two SSTs are connected to the Converter Bus, as illustrated in Fig. 1.2.

Both SSTs are connected to the same bus because they could be paralleled on their secondary sides.

When the AC filters trip, the HVDC scheme and SSTs remain in service. However, the BC and the sensitive loads of the SSTs such as illumination, rectifiers and UPSs are tripped to protect the loads on Non-Converter Bus and sensitive loads from the consequent high levels of harmonics.

1.2. Frequency Fluctuation at the Converter Bus

In rectifier stations connected to remote generation, frequency fluctuation events chiefly occur on the Converter Bus. The Converter Bus is the three-phase AC bus where the converter bridges are connected. At Songo Rectifier Station in particular, this is because the BC is the default split point and always trips after an HVDC large load rejection (energy flow through the BC greater than 110 MJ) see Fig. 1.2 [2]. Following the BC trip, the Converter Bus switches to its islanded mode of operation (GMPC on Frequency Control Mode), while the frequency on Non-Converter Bus is determined by the SAPP utilities (Non-Converter Bus is directly connected to the SAPP utilities through the Songo-Bindura AC line). Maintenance of the frequency at 50 Hz at the Converter Bus is essential since this is the rated frequency in order to keep the sharply tuned AC harmonic filters in operation and also to keep the SSTs in operation, including the sensitive loads for proper operation of the HVDC scheme. Maintenance of the frequency at 50 Hz at the Converter Bus is also essential to prevent generators tripping. Although hydro generators are not sensitive for small frequency deviations, they may trip after large frequency deviation.

The control system associated with an HVDC scheme can vary the power flow over the HVDC line at very rapid rates independently of the AC system power angles [4]. For instance, following a fault on one HVDC line, HVDC power transmission on the corresponding pole can be decreased from 960 MW to zero in less than 50 ms, according to the waveforms recorded by the transient fault recorder installed at Songo. However, at the Cahora Bassa hydroelectric power station (CB) the ramp rate of the turbines is about 16 MW/s, being 40 MW/s in extreme contingencies, according to the data recorded by the TFR. This large difference in the power ramp rates between the HVDC system and the generator units may cause over or under frequency at the Converter Bus owing to excess or deficit of mechanical energy following disturbances.

Under-frequency events are neither common nor severe at rectifier stations, especially at Songo, since there are five generator units with low forced outage rates. Besides, the GMPC is designed to rapidly reduce the HVDC power order to match the remaining generation [2].

The relatively frequent tripping of converter bridges (16 bridges in total) most often during full load conditions, the two HVDC lines of 1414 km each, commutation failure events at Apollo Inverter Station caused by disturbances on the HVAC voltages make Songo Converter Bus prone to over-frequency events as a result of the load rejection. Therefore, over-frequency events are regularly observed at the Converter Bus of remote rectifier stations such as Songo, connected to remote generation, operating under full load conditions. Depending on load conditions, even a single converter bridge tripping may cause an over-frequency event on the Converter Bus.

Over-frequency has a negative impact in the interconnected system. It causes the tripping of the sharply tuned AC filters and consequent tripping of the BC, resulting in power reduction to Eskom or to ZESA. It may also cause the tripping of the entire Songo Rectifier Station due to lack of the cooling system after the tripping of the valve 380 V AC cooling pumps following thermal protection actuation. This is because the SSTs are directly connected to Converter Bus, as illustrated in Fig. 1.2. Depending on the magnitude and duration, over-frequency may also cause the tripping of generating units at the CB hydroelectric power station after the frequency of the 400 V_{AC} auxiliary supply voltage reaches 57.5 Hz for 0.3 seconds. They trip due to the loss of the generator thrust bearing oil circulating pumps. Therefore, the solution to the over-frequency

problems at the Converter Bus is crucial for the reliability of the HVDC scheme and to increase the energy supplied to Eskom and improve the reliability of supply.

1.3. Problem Statement

The reason for frequency fluctuation at remote rectifier stations is that the active power balance is easily affected after a disturbance. For instance, following a single converter bridge tripping under full load conditions, there is excess energy (accelerating power), that may cause over-frequency on the Converter Bus. In some rectifier stations connected to remote generation, the generator units and the HVDC scheme operate most of the times under full load. This is a larger problem at Songo, since the HVDC scheme and generator units operate under full load most of the times. Furthermore, the power rejected following an HVDC disturbance cannot be injected into the passive AC lines nor to ZESA, through Songo-Bindura HVAC line due to stability and limited capacity of the coupling transformer, see Fig. 1.2.

The above factors make remote rectifier stations different from normal rectifier stations. In normal rectifier stations the HVAC transmission lines usually have smaller impedance (strong AC connection). Furthermore, the transmission system does not usually operate under full load conditions and the AC system is usually not passive. Consequently, the generators connected to normal rectifier stations are less susceptible to rotor angle instability due to small accelerating power after an HVDC disturbance and smaller transmission lines reactance.

However, the solutions proposed for over-frequency problems at remote rectifier stations, described in section 2.2, are currently not applied at Songo due to the high cost involved and lack of information to justify their suitability.

It has been observed in particular at Songo Rectifier Station, that the number of station trips due to over-frequency has increased in recent years. Therefore, it is believed that the dynamic performance of the GMPC or HVDC controls is no longer the same as during initial commissioning. Furthermore, the tripping of the AC filters following an over-frequency and the impact on the Converter Bus voltage waveform, including the interaction between the HVDC controls, GMPC and generator exciters has not been fully investigated. During load rejection there is also voltage magnitude deviation on the Songo Converter Bus.

1.4. Objectives

The objectives of this research were:

1) To evaluate the actual dynamic performance of the GMPC and HVDC controls;
2) To find the causes of the tripping of the AC filters due to over-frequency and the impact on the Converter Bus voltage waveform;
3) To determine the interaction between the HVDC controls, GMPC and generator exciters for preventing over-voltages on the Converter Bus.

1.5. Research Questions

For achieving the aim of this research, which is to propose mitigating measures for preventing over-frequencies at rectifier stations, the following questions will be answered:

1) What is the actual behaviour of the GMPC and HVDC controls during and after HVDC load rejection, in particular at Songo?
2) Why is it necessary to trip the AC filters during over-frequency events and what is the impact of the tripping on the Converter Bus voltage? Can the impact of AC filters tripping on the Converter Bus voltage be demonstrated through simulations?
3) Do the GMPC, HVDC Controls, generator exciters and AVRs interact as required during over-frequencies? Can this interaction be demonstrated through simulations?

1.6. Scope of the Investigation

Frequency fluctuation events chiefly occur on the Converter Bus of HVDC rectifier stations, connected to remote generation, see Section 1.2. Therefore, the investigation was limited to over-frequency events on the Converter Bus of remote rectifier stations. HVDC and synchronous generator models were developed on PSCAD Version 5.0 to carry out the dynamic simulations of the system to investigate the necessity for tripping the AC filters and the impact on the Converter Bus voltage waveform. Data from the last 10 years recorded by the Transient Fault Recorder (TFR) installed at Songo was used for the investigation, mainly to evaluate the GMPC and HVDC control dynamic responses to faults. In particular, at Songo, the interaction between the GMPC, HVDC controls, generators exciter and AVRs was investigated through as-built drawings of the system as well as data recorded by the TFR and PSCAD simulations.

1.7. Importance of the Investigation

The largest power producer in Mozambique is HCB, which supplies 88% of all the power consumed in the country (2014) [5]. HCB also supplies power to South Africa and Zimbabwe. Therefore, the investigation will be important for the reliability of power supplied to South Africa, Mozambique and Zimbabwe. It will address the critical issues of over-frequency at Songo that leads to power reduction or trip of the entire HVDC scheme and consequently increase the reliability and availability of power to Eskom, ZESA and EDM.

In the investigation, the effectiveness of the GMPC and HVDC controls combination in mitigating over-frequencies in HVDC Rectifier Stations connected to large power systems was investigated.

The steps that will be proposed to mitigate over-frequencies at Songo in particular could be extended to other HVDC schemes.

1.8. Ethical Considerations

In order to obtain the required information, this investigation required data to be collected from the utility operating the Songo Rectifier Substation and Cahora Bassa hydroelectric power station. Request was made to HCB and accepted. Clearance from Wits University was also obtained.

Chapter 2. LITERATURE REVIEW AND THEORETICAL BACKGROUND

2.1. Negative Impacts of Load Rejections and Over-frequencies

According to the literature, load rejections and over-frequency of the supply voltage have the following negative impacts in power systems:

2.1.1. Frequency Instability

Frequency stability refers to the ability of the power system to maintain the nominal frequency following a severe system upset as result of a significant imbalance between generation and load [6]. Frequency instability can be manifested by frequency swings which may lead to tripping of generating units and/or loads and catastrophic black outs [6]. According to the literature [7], the major frequency instability events around the world in power systems are the result of a deficit of generation (under-frequency) rather than an excess of generation (over-frequency).

2.1.2. Pole Slipping

Pole Slipping may arise due to excess of prime mover input power caused by a sudden and large loss of load [8]. This condition causes high currents through the generator. Therefore, to avoid damage the generator must be immediately tripped [8].

2.1.3. Hydro Generators Lifetime Reduction

In general, a hydro generator unit is designed for a certain number of start/stop cycles, a certain number of exceptional load rejections as well as a number of extreme load rejections. Therefore, when the number of load rejections increases its remaining lifetime reduces.

2.1.4. Fatigue Damage of Hydroelectric Turbine Runners

During a load rejection event, after the tripping of the generator circuit breaker the turbine runner goes into over-speed and the protection system (SLG) closes the wicket gate at a specific rate in order to limit the water hammer overpressure build-up in the penstock and to stop the runner rotation. The strain response during this transient depends on both the geometry of the turbine runner and the protection system, which is configured during the commissioning of the turbine runner. The fatigue cycles generated by the load rejection events are significantly larger than those generated by the other operating conditions [9].

2.1.5. Overload of Induction Motors

The induction motor should deliver the required power and torque demanded by the load at the required speed. The synchronous speed is directly proportional to the frequency of the stator supply voltage, as shown in equation (2.1).

$$\omega_s = \frac{2\pi f}{p} \tag{2.1}$$

Where ω_s is the synchronous speed of the induction motor in radians per second (rad/s); f is the *frequency* of the stator supply voltage in Hertz (Hz); and p is the number of motor pole-pairs.

The actual speed of the induction motor can be found in the following equation:

$$s = \frac{\omega_s - \omega_m}{\omega_s} \tag{2.2}$$

Where *s* is the slip of the motor; and ω_m is the operating speed (mechanical speed).

If the load of the motor is a centrifugal pump, then the torque varies with the square of the mechanical speed.

$$T_m \propto \omega_m^2 \tag{2.3}$$

The mechanical power demanded by the pump is given by equation (2.4).

$$P_m = T_m \omega_m \tag{2.4}$$

From equations (2.3) and (2.4), we get the relationship (2.5).

$$P_m \propto \omega_m^3 \tag{2.5}$$

In conclusion, following an over-frequency of the supply voltage, the mechanical speed of the pumps will increase, according to equations (2.1) and (2.2). Following the increase of the speed, the mechanical power will also increase with the cube of the mechanical speed, according to equation (2.5) and consequently the electrical power *P* will also increase in the same way ($P \cong P_m$) causing overload of the induction motors and subsequent tripping.

2.2. Solutions Proposed for Over-Frequency Problems at Rectifier Stations

According to the literature, during the GMPC studies the following solutions were proposed particularly for Songo:

2.2.1. Breaker-Switched Braking Resistors (BSBRs)

Braking resistors can be installed for two main purposes at Songo: *stability control* and *prevention of generator tripping* [10].

In stability control, braking resistors are suited for keeping the voltage angle at Songo within acceptable limits. The stabilizing task during operation of the HVDC and HVAC systems in parallel requires fast reaction and better controllability than the task to control the frequency in the islanded mode of operation [10].

Braking resistors can also be used to prevent generator tripping due to over-frequency after load rejection. In CB, the generators trip when the frequency of the 400 V_{AC} auxiliary supply reaches 57.5 Hz for 0.3 seconds. They trip due to the loss of the generator thrust bearing oil circulating pumps.

The insertion of breaker-switched braking resistors (BSBR) takes time due to the breaker operating time. So BSBRs are used when fast insertion is not crucial for stability.

2.2.2. Thyristor-Switched Braking Resistors (TSBRs)

Thyristor-switched braking resistors (TSBR) have the same purpose as BSBR, the only difference being the time of insertion and the controllability of the resistance. The TSBR can be controlled in steps. For instance, 480 MW braking resistors can be controlled in steps of 70 MW [10].

2.2.3. Thyristor-Controlled Braking Resistors (TCBRs)

Thyristor-controlled braking resistors (TCBR) are controlled continuously and their insertion time is very fast. They have the same function as the BSBRs.

2.2.4. Over-frequency Generator Tripping (OFGT)

In normal operating conditions, all the generators connected to the same bus rotate at the same synchronous speed, that corresponds to the same synchronous frequency (50 Hz in SAPP). This is also valid to the entire network, such as SAPP, when it is interconnected. The single frequency of the three-phase voltage of a particular bus is determined by all the generators connected to the bus, when the bus is on island mode of operation.

When a particular generator connected to an islanded bus, tries to increase the speed, the other generators connected to the same bus will impose the synchronous frequency to the bus and the particular generator will return to the synchronous speed. If the generator continues to increase its own relative speed, different from the bus synchronous speed it will be out of step and consequently trip.

The generator synchronous speed is given by

$$n = \frac{120f}{p_f} \tag{2.6}$$

Where n is the speed in rev/min, f is the frequency in Hz, and p_f is the number of field poles.

From equation (2.6) it can be seen that the frequency is proportional to the generator speed. When there is an HVDC pole tripping, following a transmission line fault, there can be accelerating power that can cause the increase of speed of the islanded generators connected to the Converter Bus, consequently over-frequency on the Converter Bus. Since all the generators are similar and connected to the same islanded Converter Bus, the over speed will be almost the same and the frequency deviation of the Converter Bus will be the same.

When a particular full loaded generator trips (main three-phase circuit breaker open), it is common to talk about speed, not frequency, since its speed is no longer equal to the synchronous speed. From the tripped generator stand point there is an excess of mechanical power (electrical power equal to naught), consequently the generator will accelerate. The generator speed will increase, but it will not contribute to the over-frequency of the bus since it is no longer connected to it.

Over-frequency generator tripping is an emergency control measure to avoid a dramatic rise of frequency by tripping a portion of the generator units. There can be three levels of security and stability control measures, which consist of *event-based generator tripping*, *over-frequency generator tripping* and *over-speed protection generator tripping* [10]. These three levels must be well coordinated [10].

In event-based generator tripping, the disturbances leading to over-frequency are predicted. The faults with high probability are selected as priority. Power imbalance is calculated for these faults and tripping schemes are proposed. The effectiveness and validation of these schemes must be based on simulations.

Over-frequency generator tripping should be coordinate with the event-based generator tripping. The former should be a back-up of the later [11].

2.3. The Grid Master Power Controller (GMPC)

The Grid Master Power Controller (GMPC) controls the generation at the Cahora Bassa hydroelectric power station in Mozambique and its dispatch through parallel HVAC and HVDC interconnections [2]. The GMPC was installed at Songo in order to be able to ramp turbine power rapidly without disturbing the bus frequency, thus ensuring coordination between generation and load while ramping power for normal and fault conditions [2]. Maintenance of the frequency is essential in order to keep the sharply tuned AC filters in operation. So the GMPC is a form of Automatic Generation Control (AGC) designed for power balance and for dynamic stability of the Cahora Bassa, ZESA and Eskom interconnections [1].

The following three network configurations are distinguished at Songo Rectifier Station, [2]:

a) Songo–Bindura interconnection not coupled to the Converter Bus (BC open) and Songo–Apollo (Eskom) HVDC interconnection in operation;
b) Songo–Bindura interconnection coupled to the Converter Bus (BC closed) and Songo–Apollo DC interconnection in operation, but HVAC interconnection from ZESA to Eskom opened somewhere;
c) Songo–Bindura interconnection coupled to the Converter Bus (BC closed) and HVAC and HVDC interconnections from Songo to Eskom in operation (parallel operation of HVDC and HVAC interconnections from Songo to Eskom), see Fig. 1.2.

Each of the above network configurations corresponds to the following three GMPC control modes, [2]:

a) Frequency Control Mode (for Converter Bus),
b) ZESA Control Mode, and
c) Angle Control Mode.

The three control modes will be described below:

2.3.1. Frequency Control Mode

The Frequency Control Mode is meant for islanded operation of the Songo Rectifier Station, without the Songo – Bindura line coupled to the Converter Bus (BB-I) (BC open), see Fig. 1.2 [2]. The GMPC controls the turbines on the Non-Converter Bus (BB-II) to provide constant power to ZESA [2]. The frequency on the Non-Converter Bus is controlled by the SAPP utilities. For this mode of operation, the GMPC maintains exact power balance at 50 Hz on the Converter Bus by modulating the HVDC power output around its base power setting depending on the frequency error by means of proportional-integral control [2].

In this control mode, during large disturbances, such as a trip of HVDC bridges and generators that unsettle the frequency, the GMPC activates the high gain *Disturbance Controller* which takes over from the slow integral controller [2].

2.3.2. ZESA Control Mode

In the ZESA Control Mode the GMPC supplies constant power to the SAPP utilities through the Songo-Bindura interconnection [2]. The integral frequency controller is switched off while the proportional controller's gain is significantly reduced since the frequency is controlled by the SAPP utilities [2]. Due to its nonlinear gain, the latter controller has a dead-band of ±100mHz in this mode. This control configuration is necessary because the constant power requirement for the Songo-Bindura line is incompatible with any frequency control by the GMPC [2].

2.3.3. Angle Control Mode

In Angle Control Mode, the GMPC maintains the stability of the parallel HVAC and HVDC systems to Eskom through appropriate modulation of the HVDC power (faster response compared with using the turbine governors only) according to the derivative of the voltage angle between Songo and Apollo and the derivative of the Songo–Bindura power flow (equivalent to the derivative of the voltage angle between Songo and Bindura) [2]. This provides damping of any oscillation of the Songo–Bindura power flow using the derivative of voltage angle between Songo and Apollo as a reference [2]. In this control mode the GMPC does no frequency control [2]. However, the HVDC power modulation on top of this control mode provides HVAC power stabilisation [2]. In the normal system configuration, represented in Fig. 1.2, the GMPC is in the Angle Control Mode.

2.4. Battery Energy Storage System (BESS) for Grid Stability and Frequency Control

This solution for system stability and frequency control was not proposed for Songo Rectifier Station during the GMPC studies. In contrast to braking resistors, Battery Energy Storage Systems (BESSs) are used for grid-scale energy storage application. They have seen great growth recently due to their versatility, high energy density and efficiency [12]. They are able to react to grid demands nearly instantaneously, but also have the capacity to function over longer durations and have a wide range of storage and power capacities [12]. BESSs require a Battery Management System (BMS) to monitor and maintain safe, optimal operation of each battery pack and a System Supervisory Control (SSC) to monitor the whole system [12]. They may store the energy rejected after disturbances and use it to match the peak power demand, maintaining the system stability and keeping the frequency within the SAPP dead band (Secondary Control). When implemented at Songo, the BESS may avoid the frequent tripping of the BC due to excess energy after load rejection. The 960 MW rejected after an HVDC pole tripping can be stored by the BESS and used to match the demand during peak hours.

In the past, the high cost of energy storage has made it more economical to build additional generation rather than opt for energy storage [12]. But with energy storage prices continuing to fall while cycle life has increased due to new technologies, energy storage has become more viable [12].

Although the BESS can be used for grid stability and frequency control, it cannot be integrated with the GMPC in its present form.

2.5. The Southern African Power Pool (SAPP) Frequency Quality Requirements

The Songo Rectifier Station is directly connected to the Bindura Substation in Zimbabwe via an HVAC transmission line, see Fig. 1.2. Therefore, it has to comply with SAPP frequency quality requirements.

The difference between load and generation results in frequency deviations from 50 Hz and the integrated deviation appears as a departure from standard time [13]. According to the SAPP operating guidelines, the interconnection frequency shall be scheduled to 50 Hz and controlled to that value, except for those periods in which frequency deviations are scheduled to correct the time error [13].

All generating units, with nameplate ratings of 5 MVA or greater, connected to the SAPP network must be equipped with governors [13]. The frequency dead band for the governors must be set to less than ± 0.15 Hz [13]. The CB generators are rated 480 MVA and follow these rules.

The frequency of the interconnection must be maintained between 49.85 Hz and 50.15 Hz for at least 95% of the time [13]. For a credible single contingency, such as a trip of the largest generating unit or load equal to the largest generating unit in the control area, the system frequency must not deviate to outside 49.5 Hz and 50.5 Hz [13]. For credible multiple contingencies the system frequency must not deviate to outside 49.00 Hz and 51.00 Hz [13]. System operators shall start mandatory load shedding if the frequency drops to below 48.75 Hz [13].

Chapter 3. DYNAMIC PERFORMANCE OF THE GMPC AND HVDC CONTROLS - WAVEFORMS RECORDED BY THE TRANSIENT FAULT RECORDER

3.1. Introduction

The GMPC was designed for power balance (Automatic Generation Control (AGC) functionality) as well as for dynamic stability of the Cahora Bassa, ZESA and Eskom interconnections (Power System Stabilizer (PSS) functionality) [1]. It was designed for secondary frequency control at Songo. On the other hand, each generator has its own speed load governor for primary frequency control. The GMPC does not replace the generators governors. They work together. The GMPC also controls and modulates the HVDC power transmission.

To evaluate the actual performance of the GMPC and HVDC controls during over-frequencies, the waveforms recorded by the TFR in the last 10 years were analysed. For instance, after an HVDC pole trip (load rejection of 960 MW under full load), the GMPC is supposed to transiently use the overload capacity of the healthy HVDC pole and simultaneously reduce the power reference values sent to the CB turbine governors to match the remaining load on the Converter Bus. Therefore, the power reference values sent by the GMPC to the turbines are compared with the generator electrical output powers to see if they are following the GMPC reference values. The power reference values for the HVDC Pole 1 and for the HVDC Pole 2 sent by the GMPC to the HVDC controls are compared with the HVDC Pole 1 and HVDC Pole 2 actual powers. These comparisons are important due to the following: firstly, verification if the power reference values are correctly set by the GMPC; secondly, verification if the turbines governors and HVDC controls are following the reference values received from the GMPC; thirdly, to verify if Apollo takes over current control after Songo loses it during disturbances. The above principle will also be applied in the case of a bridge tripping (240 MW load rejection under full load).

In the case of a generator tripping, the power reference values sent by the GMPC to the HVDC controls for the HVDC to match the remaining generation will be verified. They are compared with the actual HVDC power to check if the HVDC controls follow the GMPC's reference power values as well as if the actual HVDC power (current) follows the HVDC controls reference power (current). In the TFR, all the variables mentioned above are available.

The behaviour of the GMPC and HVDC controls and the frequency deviation on the Converter Bus was quantified for bridge, pole and bi-pole tripping.

According to the swing equation (3.1), the frequency deviation from 50 Hz depends on the accelerating torque, after an HVDC disturbance.

$$J\frac{d\omega_m}{dt} = T_m - T_e - D_d\omega_m = T_a \qquad (3.1)$$

Where J is the combined moment of inertia of the generator and the turbine in kg·m^2; ω_m is the mechanical angular velocity of the rotor in mechanical rad/s; T_a is the accelerating torque in N·m; T_m is the mechanical torque in N·m; T_e is the electromagnetic torque in N·m and D_d is the damping torque coefficient in N·m/s.

At CB, the accelerating torque will depend on the amount of electric power rejected for an HVDC load rejection (excess energy). The amount of load rejected will depend on the number of the bridges tripped under full load. Each converter bridge is rated 240 MW.

The accelerating torque and consequently frequency deviation at the Converter Bus, are examined for the following load rejection scenarios:

A) Converter bridge tripping with sufficient reserve HVDC capacity;

B) Converter bridge tripping without sufficient reserve HVDC capacity;

C) Pole tripping with sufficient reserve HVDC capacity;

D) Pole tripping without sufficient reserve HVDC capacity;

E) Transient DC Line Faults;

F) Pole tripping without operational telecommunications;

G) HVDC station tripping.

In the Songo Rectifier Station, the normal system configuration is represented in Fig. 1.2. In this configuration, the GMPC is in Angle Control mode. So in all events below analysed, prior to the trips, the configuration is the one represented in Fig. 1.2, with all the high voltage circuit breakers closed, including the 220 kV BC. Four generators are connected to the Converter Bus and one generator is connected to the Non-Converter Bus.

3.2. Converter Bridge Tripping with Sufficient Reserve HVDC Capacity

According to the TFR, when one bridge is tripped at Songo with sufficient reserve HVDC capacity (HVDC scheme operating with less than 87.5% loading), the remaining bridges in operation can carry the HVDC power that was being transmitted before the tripping. Turbine ramping is not required, because the remaining bridges in operation carry the rejected power after the tripping. The accelerating torque is zero (no excess energy), so the closed BC remains closed. Consequently, there is no speed disturbance at CB according to the equation (3.1). As a result, no frequency deviation is observed on the Converter Bus or on the Non-Converter Bus (same bus because they are coupled). The sharply tuned AC filters do not trip due to over-frequency. When Songo has fewer bridges in operation than Apollo, the respective pole loses current control before one bridge at Apollo is inter-tripped and there is power reduction due to the current margin.

A typical example is the converter bridge 6 tripping at Songo that happened on 06/07/2017 at 01:26:25.751 (Figures 3.1 – 3.3).

Immediately before the tripping, there were seven bridges in operation at Songo (3 bridges on Pole 1 and 4 bridges on Pole 2) and six bridges in operation at Apollo (3 bridges on Pole 1 and 3 bridges on Pole 2). Power transmission was 1020 MW (510 MW for each pole), that corresponds to 70.83% loading. The BC power flow was 100 MW from the Converter Bus to the Non-Converter Bus.

During the tripping there was voltage dependent current order limit (VDCOL) actuation on Pole 2, which reduced the actual current to 40% of the nominal value (to 720 A) for 215 ms. As a result, the GMPC correctly used the transient overload capacity of the healthy pole (Pole 1), by overloading it (125%) for about 400 ms, according to Fig. 3.1. During this period, Pole 1 loses

current control (α reaches minimum value) for 175 ms. The Pole 1 HVDC control reference current follows the GMPC correctly set reference current. Consequently, the actual current on Pole 1 follows the HVDC control reference current, see Fig. 3.2.

On the other hand, the Pole 2 HVDC control reference current does not follow the GMPC reference current (power) value for 215 ms due to the VDCOL actuation on Pole 2, see Fig. 3.1 and Fig. 3.3. However, the actual current on Pole 2 correctly follows the HVDC control Pole 2 reference current, according to Fig. 3.3. Pole 2 loses current control for 489 ms when it tries to instantly increase the current to follow the GMPC reference value after the VDCOL actuation.

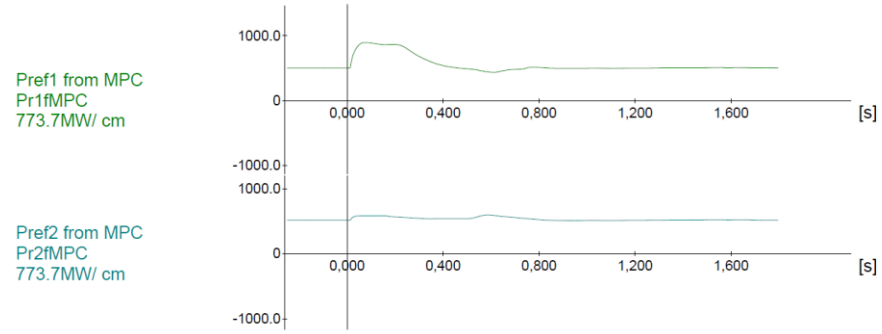


Fig. 3.1: Power reference values from the GMPC to the HVDC controls, during Bridge 6 tripping at Songo.

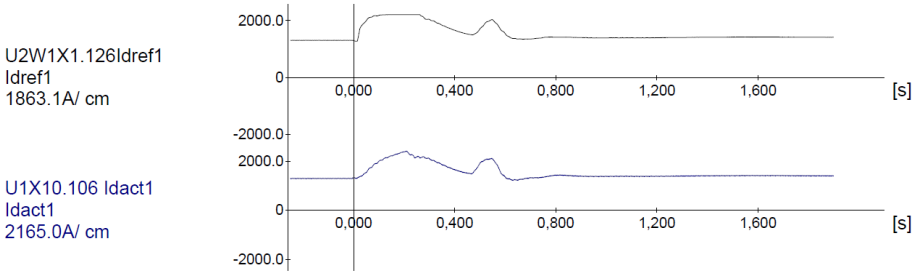


Fig. 3.2: Pole 1 actual and reference HVDC controls currents, during Bridge 6 tripping at Songo.

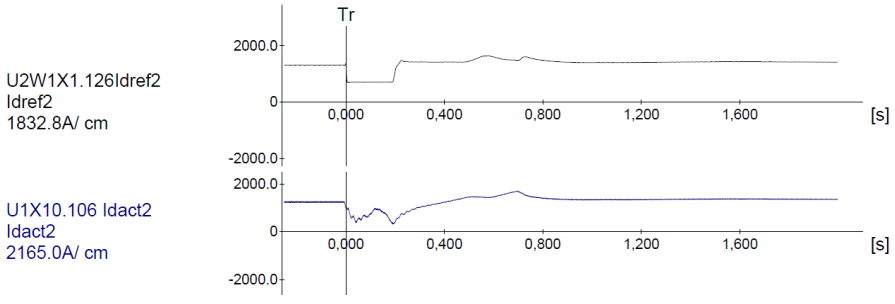


Fig. 3.3: Pole 2 actual and reference currents, during Bridge 6 tripping at Songo.

In this particular event and many other similar events, the BC did not trip and there was no frequency deviation on Songo Converter Bus. The Songo frequency was mainly determined by the SAPP utilities. There were no power oscillations at all. Songo loses current control, but Apollo takes it over. Therefore, the GMPC and HVDC controls behaved correctly.

Therefore, according to the TFR, the tripping of a single bridge with sufficient reserve HVDC capacity (HVDC scheme operating with less than 87.5% loading) does not cause frequency deviation on the Converter Bus. In these situations, the GMPC behaves correctly as designed.

3.3. Converter Bridge Tripping Without Sufficient Reserve HVDC Capacity

3.3.1. Converter Bridge Tripping during Bipolar Operation of the HVDC Scheme

According to the TFR data, in a bipolar mode operation of the HVDC scheme and normal system configuration, when a single bridge is tripped at Songo without sufficient reserve HVDC capacity (100% loading of the HVDC scheme) there is accelerating power (excess energy). The GMPC correctly uses the 125% transient overload capacity of both HVDC poles for about 2 seconds, however turbine ramping cannot be avoided. The excess energy is less than the 110 MJ BC trip threshold. Therefore, the BC does not trip, meaning the Converter Bus remains coupled to the Non-Converter Bus and the frequency of the supply voltage at Songo is determined by the SAPP utilities including CB generators.

On a bipolar and full load operation of the HVDC scheme, when a single bridge trips and simultaneously there is VDCOL actuation, the excess energy is greater than the 110 MJ BC trip setting and the BC tripping cannot be avoided. The two 220 kV busses are split and the Converter Bus switches to the Islanded Mode Operation. Over-frequency on the Converter Bus causes the tripping of the AC filters.

On full load operation of the bipolar HVDC scheme, the way a single bridge is tripped has impact on the accelerating power (or excess energy) at Songo. It is due to the ramping of power and the time the bridge takes to be switched out. While the normal switch-off sequence (NOSOF) of a bridge takes 10.699 seconds the fast action switch-off sequence (FASOF) of a bridge takes about 137 ms. During the NOSOF sequence, the turbines can be ramped down while the bridge is being taken out of operation and the bus frequency is not upset.

The following event illustrates what is explained above. On 30/06/2014 at 14:06:29.511 (Figures 3.4 – 3.7) the converter bridge 3 at Songo tripped due to a valve firing fault. There were seven bridges in operation both at Songo and Apollo (4 bridges on Pole 1 and 3 bridges on Pole 2). Before the tripping, power transmission was 1659 MW (952 MW on Pole 1 and 707 MW on Pole 2) from Songo to Apollo, that corresponds to 98.75% loading. The 220 kV BC power flow was 22 MW from the Non-Converter Bus to the Converter Bus.

During the faulty bridge 3 tripping, the GMPC correctly ramps down the CB turbines connected to the Converter Bus and uses the transient overload capacity of both poles (Pole 1 and Pole 2), by overloading them for approximately 2 seconds. The HVDC current reaches 2093.75 A on Pole 1 and 2265.82 A on Pole 2 for about 1.84 seconds. The excess energy is not enough to trip the BC at Songo. So the Converter Bus remains coupled to the Non-Converter Bus and the frequency on both busses at Songo is determined by the SAPP utilities including the CB generators. There is no frequency deviation at all and the AC filters do not trip.

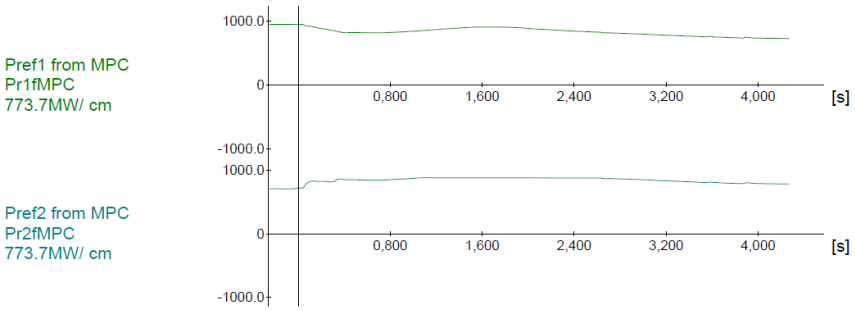


Fig. 3.4: Power reference values from the GMPC to the HVDC controls, during Bridge 3 tripping at Songo.

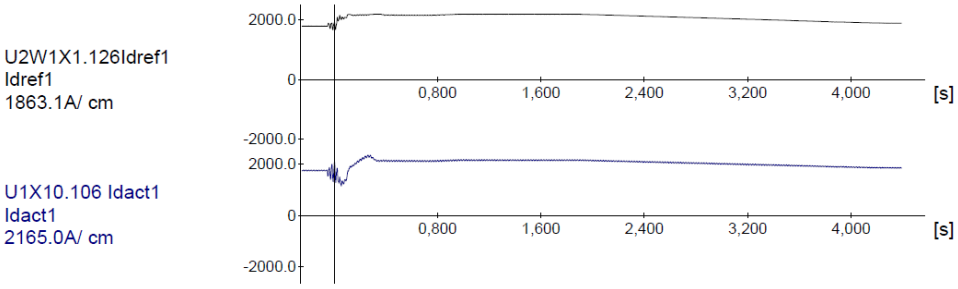


Fig. 3.5: Pole 1 reference and actual currents, during Bridge 3 tripping at Songo.

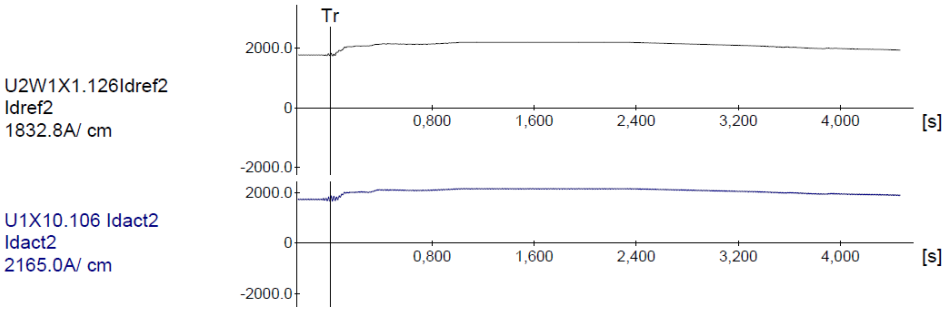


Fig. 3.6: Pole 2 reference and actual currents, during Bridge 3 tripping at Songo.

In this and many other similar events, the GMPC and HVDC controls behaved well. The BC did not trip and there was no frequency deviation at Songo after the tripping. So the AC filters did not trip by over-frequency.

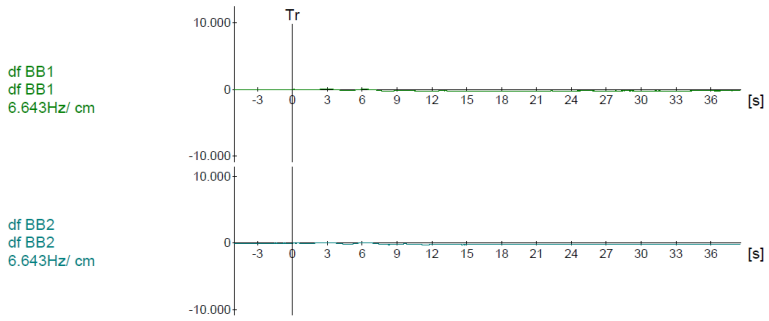


Fig. 3.7: Frequency deviation on the Converter Bus (BB-I) and the Non-Converter Bus (BB-II), after Bridge 3 tripping at Songo.

3.3.2. Converter Bridge Tripping during Monopolar Operation of the HVDC Scheme

The behaviour of the GMPC and HVDC controls was examined for the case of a single bridge tripping. Just before the tripping, it was the normal system configuration illustrated in Fig. 1.2, but the HVDC scheme was in monopolar mode operation (one pole in operation both at Songo and Apollo).

According to the data saved by the TFR, in a monopolar mode operation, when a single bridge trips at Songo, the GMPC uses the transient overload capacity of the remaining bridges in operation. It ramps down the turbines to match the remaining load. The excess energy is not enough to trip the BC. Some of the power rejected flows through the Songo-Bindura line to ZESA, however there are neither voltage dips nor power oscillation on Songo-Bindura tie-line. The frequency at Songo on the coupled busses is determined by the SAPP utilities, including the CB generators. There is no meaningful frequency deviation neither on the Converter Bus nor on the Non-Converter Bus and the AC filters do not trip by over-frequency.

The behaviour described above can be illustrated in the following event. On 02/04/2014 at 17:56:01.386 (Figures 3.8 – 3.10) the converter bridge 3 at Songo tripped due to a valve fault on the red phase. There was only Pole 1 in operation with four bridges in service on both stations. Pole 2 and Line 2 were out of service for planned maintenance. Before the tripping, power transmission was about 960 MW from Songo to Apollo, that corresponds to 100% loading. The 220 kV BC power flow was 150.93 MW from the Converter Bus to the Non-Converter Bus. Power transmission was on Tete 1 (91.6 MW), Tete 2 (147.9 MW) and Songo-Bindura (246.5 MW).

During the faulty bridge tripping, the GMPC correctly ramps down the CB turbines about 240 MW and also uses the transient overload capacity of the remaining bridges in operation for about 2 seconds. Pole 1 loses current control for 256.66 ms. However, it does not affect the overall performance of the GMPC and HVDC controls.

The BC did not trip because the energy of about 72 MJ is below the 110 MJ trip setting. Therefore, the Converter Bus and the Non-Converter Bus are not split. The Converter Bus and the Non-Converter Bus remain connected to SAPP and the frequency at Songo Rectifier Station is mainly determined by the SAPP utilities, including the CB generators.

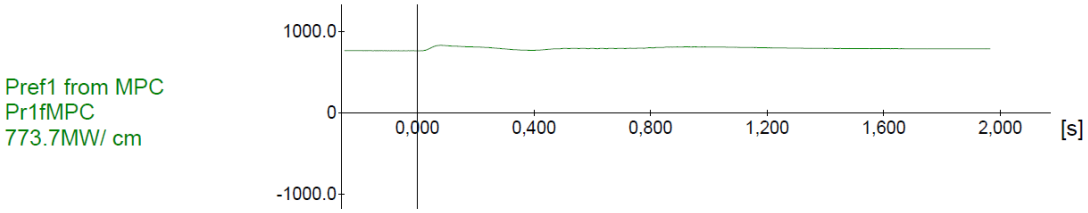


Fig. 3.8: Pole 1 power reference from the GMPC, during Bridge 3 tripping at Songo.

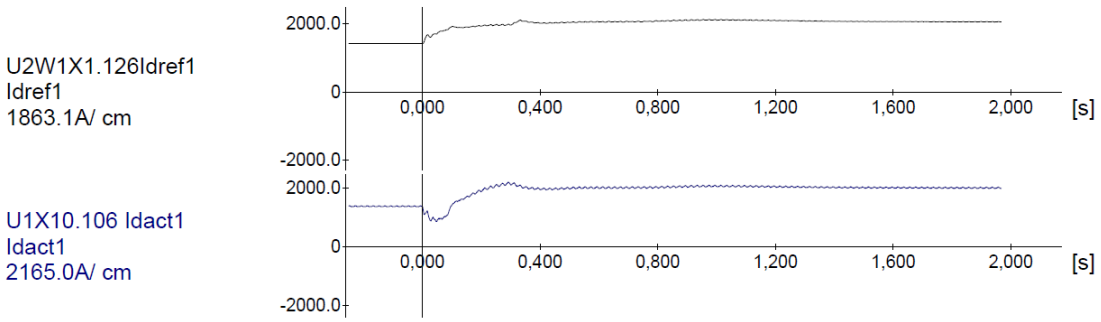


Fig. 3.9: Pole 1 reference and actual currents, during Bridge 3 tripping at Songo.

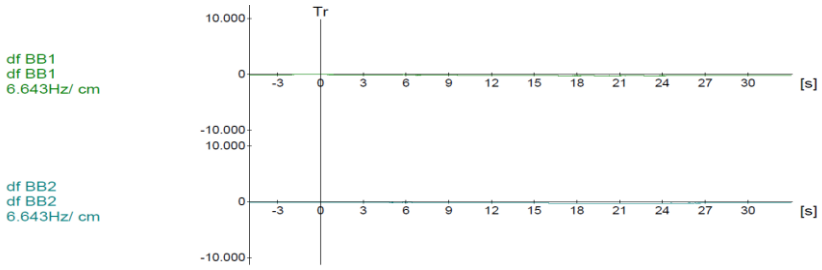


Fig. 3.10: Frequency deviation at Songo Converter Bus (BB-I) and Non-Converter Bus (BB-II), after Bridge 3 tripping at Songo.

There is no frequency deviation at all on both busses (Converter Bus and Non-Converter Bus) at Songo and there are no power oscillations. Therefore, the GMPC and HVDC controls performed well.

3.4. Pole Tripping without Sufficient Reserve HVDC Capacity

In normal system configuration and bipolar operation of the HVDC scheme, when a single HVDC pole trips at Songo, depending on the loading of the HVDC scheme prior to the tripping, the 220 kV BC may also trip. In fact, the BC tripping depends on the amount of excess energy (power imbalance or accelerating power) at Songo immediately after the pole tripping. The excess energy depends on the load rejected and the reserve HVDC capacity of the healthy pole prior to the tripping. The Songo-Apollo HVDC scheme operates most of the time under full load. This contributes to the increase of the excess energy, immediately after a pole tripping. If this energy flow is greater than the 110 MJ BC trip setting, the BC trips, splitting the Converter Bus and the Non-Converter Bus, resulting in over-frequency on the islanded Converter Bus. The frequency deviation on this bus will depend on the amount of the accelerating power (power imbalance) on the bus, immediately after the BC tripping.

Prior to a single pole trip at Songo Rectifier Station, due to a permanent fault, usually power transmission on the affected pole is more than 720 MW from Songo to Apollo. The bipolar HVDC scheme usually operates with more than 80% loading. After the tripping, the GMPC uses the reserve HVDC capacity and the 125% transient overload capacity of the healthy pole. Due to the large load rejected and only 1 second duration of the transient overload capacity, turbine ramping is required. The GMPC ramps down the CB turbines connected to the Converter Bus to

match the remaining load. However, the BC tripping cannot be avoided due to the large power imbalance (excess energy of more than 110 MJ). The two busses (the Converter Bus and the Non-Converter Bus) are split. Consequently, the Converter Bus turns into islanded mode operation. The over-frequency on this bus will mainly depend on the amount of accelerating power immediately after the BC tripping. It usually reaches 55 Hz and the frequency deviation from 50 Hz lasts about 15 seconds. The AC filters trip due to over-frequency.

The following event recorded by the TFR illustrates what is explained above. On 05/04/2009 at 18:29:32.425 (Figures 3.11 – 3.14) Pole 1 tripped at Songo, after pole differential protection operation. There were 7 bridges in operation at both stations (4 bridges on Pole 1 and 3 bridges on Pole 2). Immediately before the tripping, power transmission was 1363 MW (785 MW on Pole 1 and 578 MW on Pole 2) from Songo to Apollo, that corresponds to 81% loading. Four generators were connected to the Converter Bus (BB-I) and one generator was connected to the Non-Converter Bus (BB-II). Power transmission was on Tete 1 (8.2 MW) and Tete 2 (65.9 MW). The BC power flow just before the tripping was almost nil.

During the Pole 1 tripping there was also VDCOL operation on Pole 1. The BC tripped due to excess energy after HVDC load rejection, leaving the Converter Bus on islanded mode operation. The AC filters tripped due to over-frequency. The energy surge on the Songo-Bindura line caused oscillations, but they were damped by the CB generator connected to the Non-Converter Bus (BB-II).

During the HVDC load rejection, the GMPC used the transient overload capacity of Pole 2 (the healthy pole), by increasing its reference power to 878 MW (2250 A). Despite the Pole 2 periodic loss of current control at Songo, the actual current followed the reference current, but reduced by the current margin. However, due to the large accelerating power after load rejection and BC tripping, the frequency on the Converter Bus increased as illustrated in Fig. 3.14, while the frequency on Non-Converter Bus was determined by the SAPP utilities including the single CB generator.

During the HVDC Pole 1 tripping, the GMPC also requested turbine ramping of the CB generators connected to the Converter Bus. However, over-frequency could not be avoided due to the slow response of the turbine governors.

Figure 3.13 illustrates that there were current oscillations on Pole 2 during the disturbance. However, the GMPC performed well, because the Pole 2 reference power was correctly set and was not oscillating, while the HVDC controls response to the GMPC requested power was not that stable. Therefore, the HVDC controls did not perform well. The HVDC current oscillations on Pole 2 need to be investigated.

During the disturbance, the peak frequency on the Converter Bus (BB-I) was 57.0 Hz and the frequency deviation from 50 Hz lasted for about 17.0 seconds. On the Non-Converter Bus (BB-II) the frequency was mainly determined by the SAPP utilities and there was no frequency deviation at all.

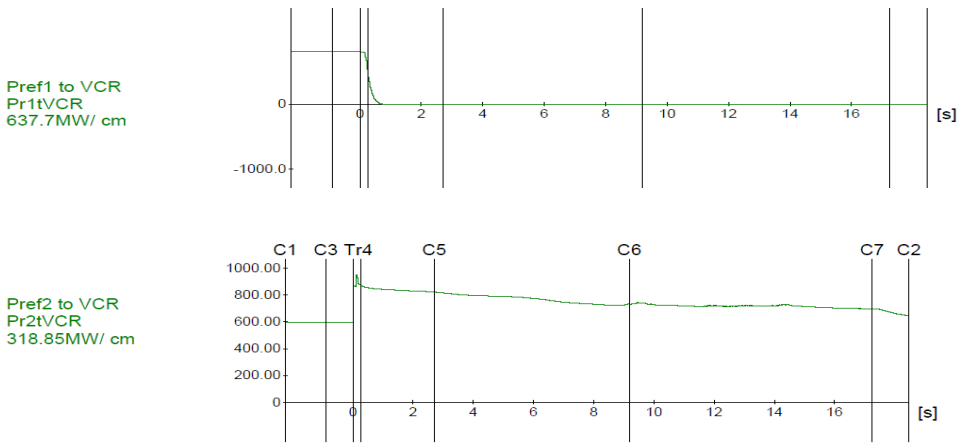


Fig. 3.11: Power reference values from the GMPC to the HVDC controls, during Pole 1 tripping at Songo.

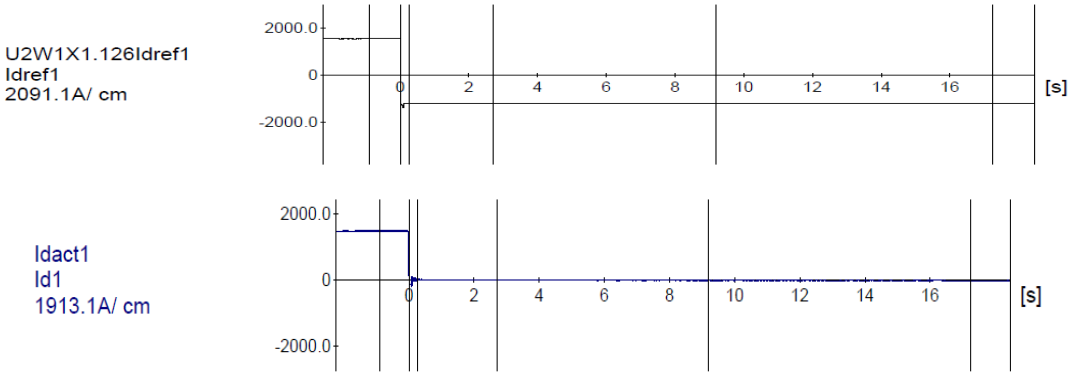


Fig. 3.12: Pole 1 reference and actual currents, during Pole 1 tripping at Songo.

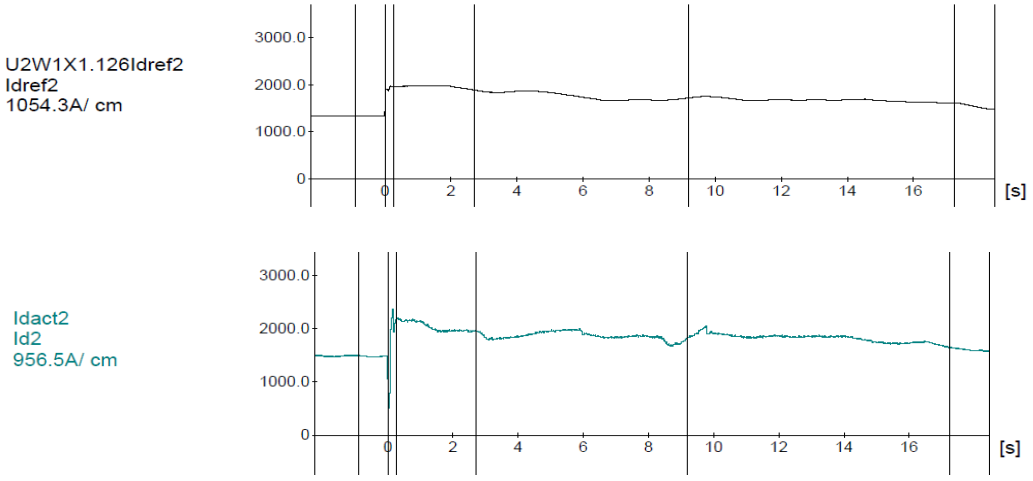


Fig. 3.13: Pole 2 reference and actual currents, during Pole 1 tripping at Songo.

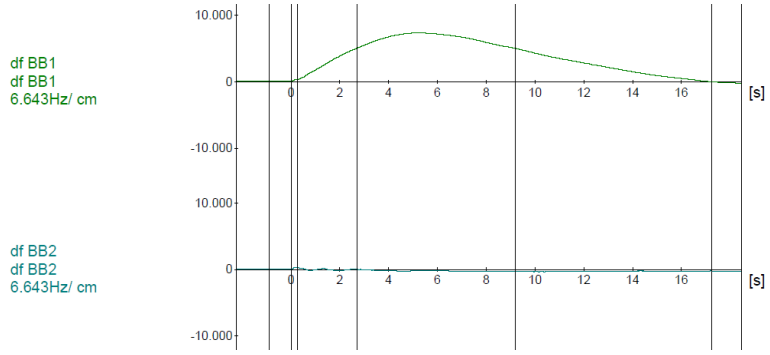


Fig. 3.14: Converter Bus (BB-I) and Non-Converter Bus (BB-II) frequency deviation, after Pole 1 tripping at Songo.

The GMPC performed well, but over-frequency could not be avoided due to the low HVDC reserve capacity on the healthy pole (about 19%) as well as the low transient overload capacity of Pole 2. The HVDC controls did not perform well. There are some oscillations in the Pole 2 DC-side current, according to Fig. 3.13.

3.5. Pole Tripping without Reserve HVDC Capacity

This situation is similar to the situation analysed in 3.4, the only difference being the insufficient HVDC reserve capacity. In normal system configuration and bipolar operation of the HVDC scheme, when one HVDC pole trips at Songo, with the HVDC scheme operating under full load (100% loading) prior to the tripping, the BC will also trip. The BC tripping depends on the amount of excess energy at Songo immediately after the pole tripping. After the BC tripping, there will be over-frequency in the islanded Converter Bus. The frequency deviation on this bus will depend on the amount of the accelerating power, immediately after the BC tripping.

The GMPC and HVDC controls behave exactly as described in 3.4. If power transmission from Songo to Apollo is greater than 1200 MW (more than five bridges in operation), after a single pole tripping, the GMPC uses the 125% transient overload capacity of the healthy pole. Due to the large load rejected and only 1 second duration of the transient overload capacity of the converters, turbine ramping is required. The GMPC ramps down all the CB turbines connected to the Converter Bus (BB-I) to match the remaining load. However, the BC tripping cannot be avoided due to the large power imbalance (excess energy of more than the 110 MJ BC trip setting). The two busses (the Converter Bus and the Non-Converter Bus) are split. Consequently, the Converter Bus switches to island mode operation. The frequency deviation (over-frequency) on this bus will mainly depend on the amount of accelerating power immediately after the BC tripping. It can reach 56 Hz and last 17 seconds. The AC filters trip due to over-frequency.

The following event illustrates the description above. On 26/12/2006 at 13:54:27.560 (Figures 3.15 – 3.17) Pole 1 tripped at Songo due to high temperature on the DC inductor. Just before the tripping, it was the normal system configuration, with the GMPC in Angle Control Mode (BC closed). The HVDC scheme was operating with three bridges on Pole 1 and two bridges on Pole 2 at both converter stations (Songo and Apollo). Just before the tripping, power transmission was on Tete 1 (12.6 MW), Tete 2 (46.3 MW) and the power through the BC was 109 MW from

the Converter Bus to the Non-Converter Bus. The HVDC scheme loading was 96.5%, power transmission was 1158 MW (693 MW on Pole 1 and 465 MW on Pole 2) from Songo to Apollo.

After the HVDC Pole 1 tripping, the BC trips due to excess energy and the Converter Bus switches to islanded mode operation. The AC filters tripped due to over-frequency. The GMPC uses the Pole 2 transient overload capacity of 2250 A. However, Pole 2 loses current control and Apollo takes it over. As a result, there is a current reduction on Pole 2 due to the current margin, according to the waveforms in Fig. 3.16. Power oscillations on the Songo-Bindura and Tete lines are well damped after the Pole 1 fault. The GMPC and the HVDC controls performed well, however over-frequency could not be avoided.

On the Converter Bus (BB-I), the peak frequency was 57.4 Hz, and the frequency deviation from 50 Hz lasted for about 18.7 seconds. On the Non-Converter Bus (BB-II) the maximum frequency deviation was 0.37 Hz, see Fig. 3.17.

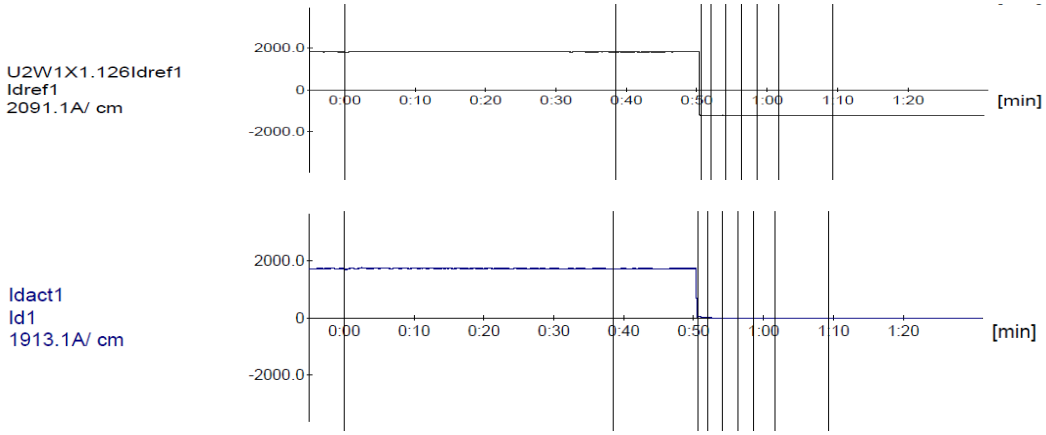


Fig. 3.15: Pole 1 reference and actual currents, during Pole 1 tripping at Songo.

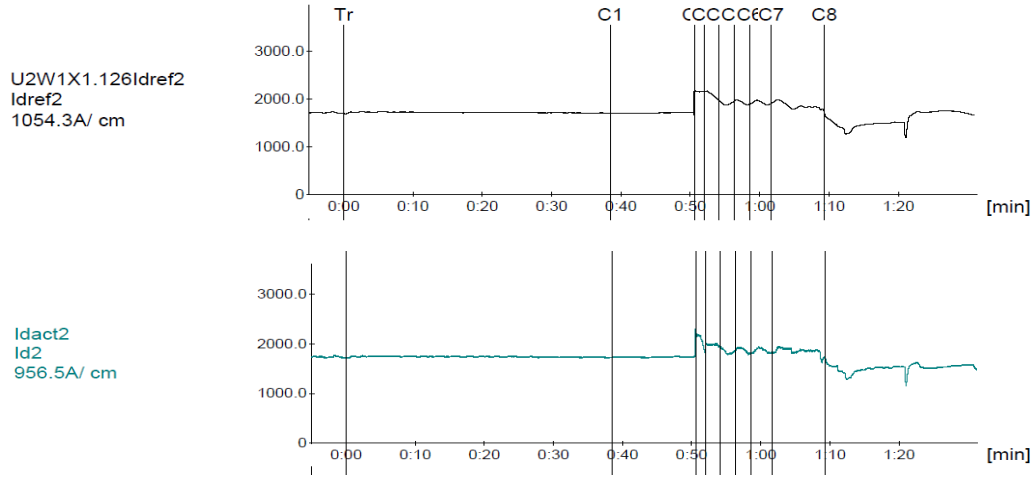


Fig. 3.16: Pole 2 reference and actual currents, during Pole 1 tripping at Songo.

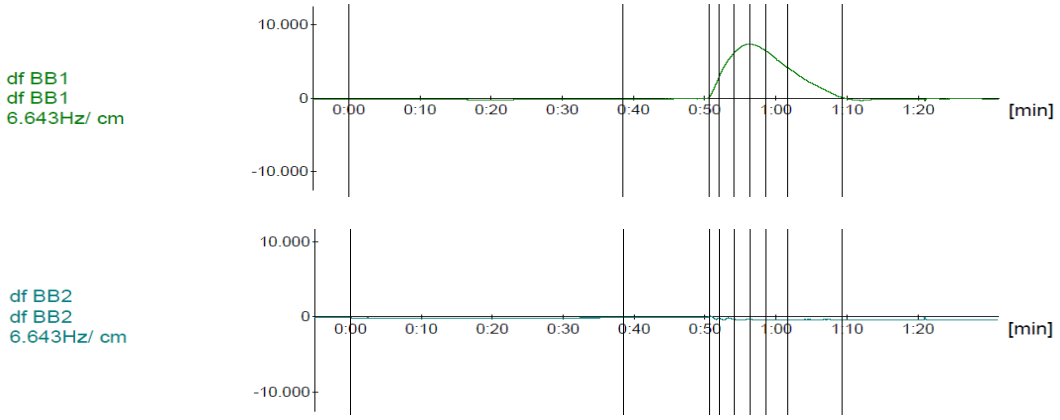


Fig. 3.17: Converter Bus (BB-I) and Non-Converter Bus (BB-II) frequency deviation, after Pole 1 tripping at Songo.

3.6. Transient (short duration) Faults on the HVDC Lines

The GMPC and HVDC controls performances during transient faults on the HVDC lines were also evaluated. For most transient faults, the GMPC and HVDC controls performed well. The GMPC does not change the reference values sent to the CB turbines during transient (short duration) faults. It only uses the transient overload capacity of the healthy pole. The HVDC controls and CB generators follow the GMPC reference values. Usually there is loss of current control on both HVDC poles, but for less than 1 second. Power oscillations on the Songo-Bindura and Tete lines are damped after the transient fault. The BC always trips by excess energy flow. However, the Converter Bus frequency deviation depends mainly on both the HVDC load and the BC power flow and direction, prior to the transient DC line fault.

The following event illustrates the behaviour of the GMPC and HVDC controls. On 22/10/2015 at 04:58:34.912 (Figures 3.18 – 3.22) there was a transient fault on HVDC Line 1, at 408 km from Songo Rectifier Station. Just before the transient fault, the system configuration was as illustrated in Fig. 1.2, with five generating units in operation and the GMPC in Angle Control Mode (BC closed). There were four bridges in operation on Pole 1 and three bridges in operation on Pole 2 in both converter stations. The HVDC scheme was nearly fully loaded (92% loading) and power transmission was 1545 MW (865 MW on Pole 1 and 680 MW on Pole 2) from Songo to Apollo. Power transmission was on Tete 1 (119 MW), Tete 2 (168 MW) and the power flow through the BC was -81 MW, flowing from the Non-Converter Bus to the Converter Bus.

From Fig. 3.18, it can be seen that there was a transient (short duration) fault on HVDC Line 1, because the current on the line goes up while the voltage goes down at the same time. It was detected by the travelling wave protection. The line was successfully reenergized after a 206.15 ms dead time.

During this transient fault, there was also VDCOL actuation on Pole 1 at Songo. In fact, in all HVDC line transient faults detected by the travelling wave protection there is also VDCOL actuation due to the instantaneous voltage reduction (earth faults with very low impedance). The VDCOL is usually the first to actuate before the travelling wave protection.

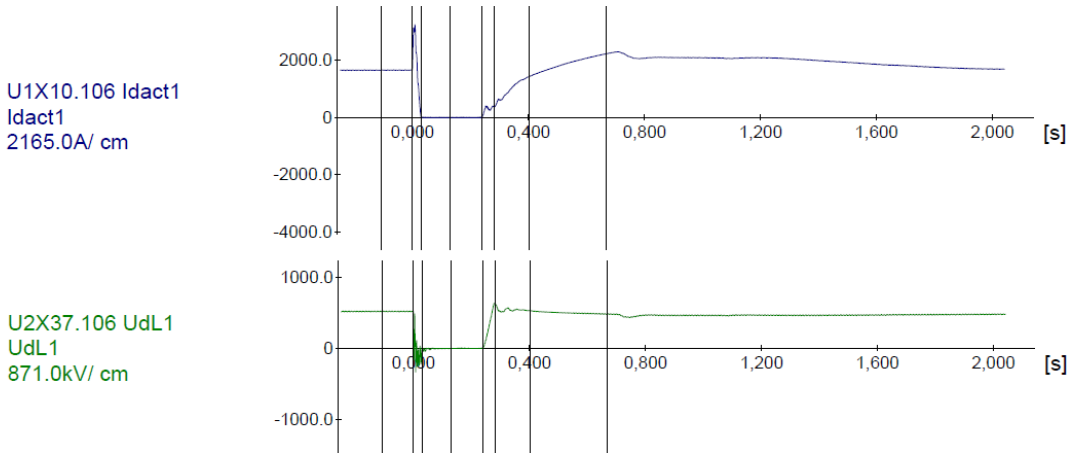


Fig. 3.18: Current and voltage on Pole 1, during the transient fault on DC Line 1.

After the fault detection, it took the HVDC controls 32.05 ms to bring the current to zero on Line 1. At Songo the fault was cleared by the force retard operation.

The GMPC correctly used the 125% transient overload capacity of the healthy HVDC Pole 2/Line 2 for 1 second, according to Fig. 3.20. The actual transient overload current was 2233 A, close to the rated overload current of 2250 A, in a system designed for steady state current of 1800 A. The GMPC also uses the transient overload capacity of the faulty DC Line 1 after the transient fault.

During the transient fault on the DC Line 1, although the transient overload capacity of Pole 2/Line 2 was used, the BC tripped due to excess energy after the energy imbalance of 194.4 MJ. The Converter Bus (BB-I) switched to the islanded (Frequency Control) mode of operation. However, the frequency deviation on the Converter Bus was less than 0.195 Hz. For the Non-Converter Bus, connected to the SAPP utilities, the maximum frequency deviation was –0.189 Hz, see Fig. 3.22.

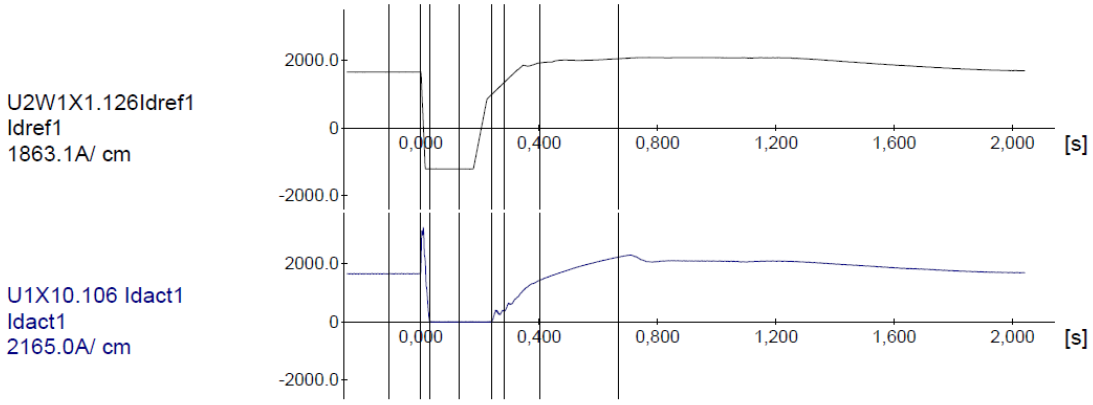


Fig. 3.19: Pole 1 reference and actual currents, during the transient fault on DC Line 1.

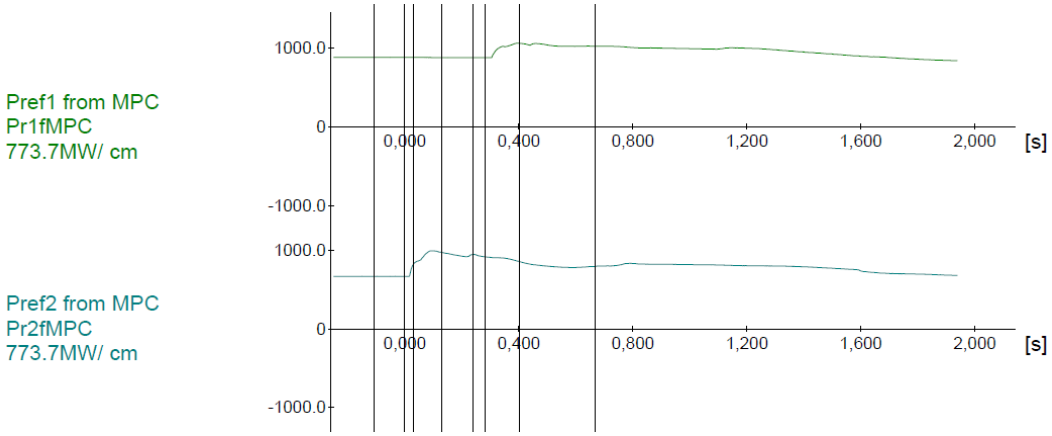


Fig. 3.20: Power reference values from the GMPC to HVDC controls, during the transient fault in DC Line 1.

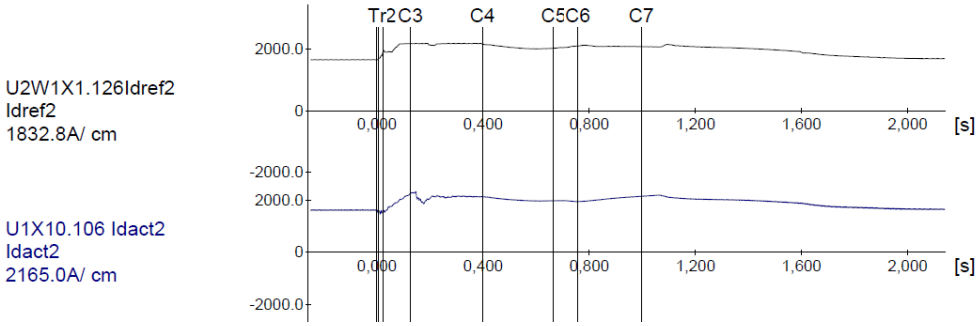


Fig. 3.21: Pole 2 reference and actual currents, during the transient fault on DC Line 1.

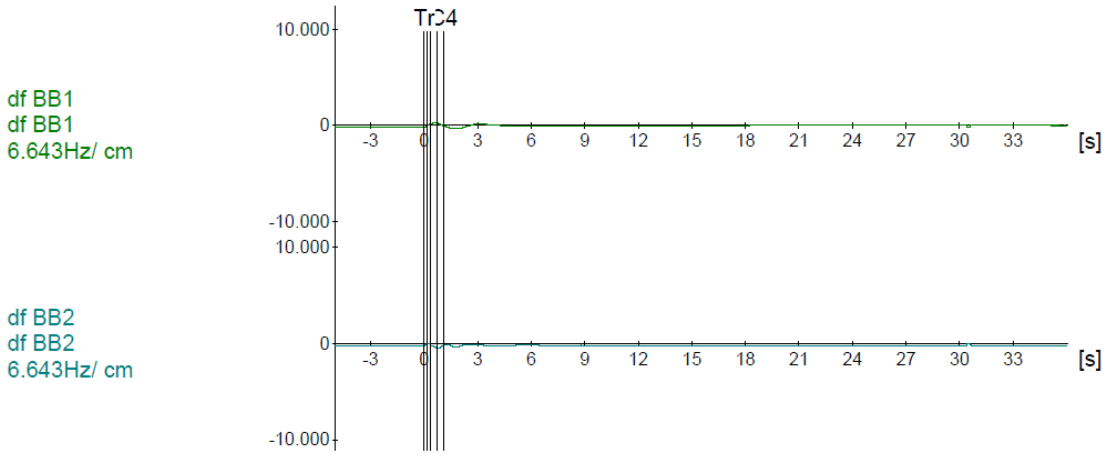


Fig. 3.22: Frequency deviation on the Converter Bus (BB-I) and the Non-Converter Bus (BB-II) during the transient fault on Line 1.

In this DC Line 1 transient (short duration) fault, the GMPC and HVDC controls performed very well. Although the BC tripped due to excess energy flow, the frequency deviation in Songo busses was less than ±0.2 Hz, for this particular event.

3.7. Pole Tripping without Telecommunications

Without operational telecommunications between the Songo Rectifier Station and the Apollo Inverter Station, neither the GMPC nor the HVDC controls performed well. Therefore, telecommunications are vital for the best performance of the GMPC and HVDC controls.

In steady state, telecommunications are crucial for the GMPC Angle Control Mode (BC closed) of operation for stabilization of the parallel operation of the HVAC and HVDC systems from Songo to Apollo. Without operational telecommunications, the BC must remain open at Songo and the GMPC must be in Frequency Control Mode. The main disadvantage of open BC operation is the under-utilization of the CB generators, since the excess power on the Converter Bus cannot flow to the Non-Converter Bus and vice-versa, see Fig. 1.2.

During transient conditions, telecommunications are crucial for the HVDC controls and consequently for full control of the HVDC power by the GMPC. So without telecommunications, after a pole trips the frequency deviation is large resulting in tripping of the AC filters, converter bridges and sometimes generating units in the power station.

A typical example of poor dynamic performance of the GMPC and HVDC controls due to lack of telecommunications is described in the following event. On 22/08/2014 at 07:35:26.834 (Figures 3.23 – 3.25) Pole 1 at Songo inter-tripped after the tripping of Pole 1 at Apollo. There were no telecommunications. Just before Pole 1 tripping, the system configuration was as illustrated in Fig. 1.2, with five generating units in operation and the GMPC in ZESA control mode. There were four bridges in operation on Pole 1 and three bridges in operation on Pole 2 in both converter stations. The HVDC scheme loading was 72.92% and power transmission was 1225 MW (621 MW on Pole 1 and 604 MW on Pole 2) from Songo to Apollo. Power transmission was on Tete 1 (119 MW), Tete 2 (168 MW), Songo-Bindura (164 MW) and the BC power flow was 81 MW flowing from BB-I to BB-II.

After Pole 1 tripping at Apollo, Pole 1 at Songo did not immediately inter-trip due to a fault on the Songo-Apollo telecommunications. Consequently, Songo did not receive the inter-tripping signal from Apollo. As a result, Pole 1 and Pole 2 at Songo lost current control and Apollo could not take it over. The GMPC lost the control of the HVDC scheme and split the Converter Bus and the Non-Converter Bus at Songo by tripping the BC. When the GMPC does not have full control of the HVDC scheme, it cannot accurately change the load reference set-point of the CB generators (secondary control). Consequently, the frequency on the Converter Bus (BB-I) reached 62.5 Hz. As a result, all the converter bridges at Songo tripped due to overload of the converter cooling pumps, see equation (2.3).

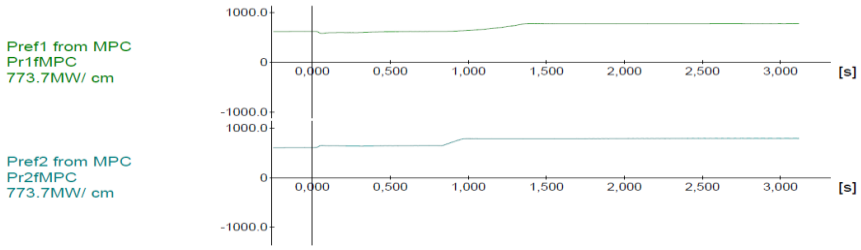


Fig. 3.23: Pole 1 and Pole 2 power reference values from the GMPC to HVDC controls, during Pole 1 tripping at Apollo.

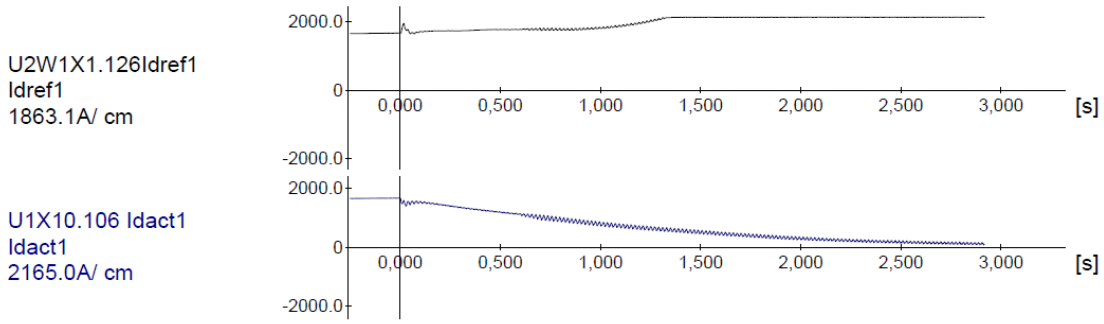


Fig. 3.24: Pole 1 reference and actual currents at Songo, during Pole 1 tripping at Apollo.

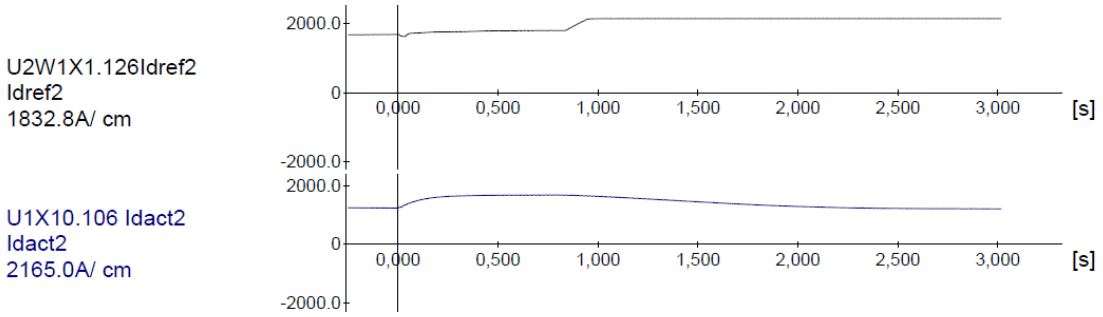


Fig. 3.25: Pole 2 reference and actual currents at Songo, during Pole 1 tripping at Apollo.

The waveforms in Fig. 3.24 and Fig. 3.25 demonstrate that without telecommunications between the Songo Rectifier Station and the Apollo Inverter Station the HVDC controls and consequently the GMPC do not perform well during disturbances. The DC Line 1 differential protection did not operate owing to lack of telecommunications between the Songo Rectifier Station and Apollo Inverter Station. For situations like this, countermeasures shall be studied and implemented at Songo. Open DC line protection or pole tripping, if the pole actual current does not follow the reference current shall be studied

3.8. HVDC Station Tripping

Station tripping is not common on the Songo-Apollo HVDC scheme since the two HVDC poles are on separate towers. The distance between the two HVDC lines is about 1 km. So faults on both poles/lines at the same time are not common. The very few of them are due to faults on the Converter Bus since both poles are connected to the same bus. When this happens, usually the Non-Converter Bus (BB-II) is also affected because the BC does not trip on phase to ground faults. Station tripping is also due to blackouts at the Cahora Bassa power station (tripping of all the generators).

When the fault affects only the Songo Rectifier Station, the BC trips due to excess energy flow and the Converter Bus switches to island operation. The Non-Converter Bus is not affected. The frequency on the Converter Bus usually reaches 60 Hz and the frequency deviation from 50 Hz lasts for about 27 seconds. It is not a critical problem since there are no loads connected to this bus, only generating units and the SST designed to operate in this harsh environment. The

sensitive loads on these two transformers are tripped before the tripping of the AC filters to avoid them being subjected to high harmonic voltage levels when the AC filters are disconnected.

3.9. Summary of the Results

In HVDC rectifier stations, it is difficult to compare two different events since two or more different events, even similar events, are never identical. This is because the operating conditions, such as loading (active and reactive power) of transmission lines and generators, busbar voltage, system configuration and other pre-fault conditions are always different for two particular events. Therefore, for the GMPC and HVDC controls performance evaluation, it was more a qualitative than a quantitative analysis of the TFR events waveforms.

A single bridge tripping, with or without HVDC reserve capacity, does not cause BC tripping nor frequency deviation at Songo. A pole tripping on full load conditions, without sufficient reserve capacity usually causes an over-frequency of about 57 Hz. While the HVDC station tripping, with more than 6 bridges in operation on full load condition, the frequency can easily reach 62 Hz on the Converter Bus.

Although the frequency on the Songo Converter Bus may reach 57.00 Hz, immediately after an HVDC load rejection, HCB always complies with the SAPP frequency quality requirement. Since the Non-Converter Bus is linked to the SAPP, this value is never reached, see Fig. 1.2. This is because following large HVDC load rejection, the BC trips due to excess energy flow (energy greater than the 110 MJ BC trip setting), leaving the Converter Bus on island operation. On the other hand, the BC also trips without delay when the frequency deviation exceeds ±850 mHz and also trips when ±450 mHz is exceeded for 18 seconds. These settings are for the BC opening before the AC filters in order to protect the Non-Converter Bus against high levels of voltage harmonics.

In summary, the GMPC and HVDC controls performance were analysed using the data recorded by the TFR installed at Songo. The waveforms prove that the GMPC performance is good, although the performance of the HVDC controls in very few cases is questionable and still rely on telecommunications between the rectifier and inverter stations.

Chapter 4. SONGO-APOLLO HVDC SCHEME MODEL DEVELOPMENT

4.1. Introduction

The aim of this chapter is to develop the Songo-Apollo HVDC scheme and Cahora Bassa generator models to study over-frequencies at rectifier stations Converter Bus and propose mitigating measures. To accomplish this, the system illustrated in Fig. 1.2 was modelled in PSCAD/EMTDC, Version 5.0. The Cahora Bassa generators and Songo converter bridges were also modelled in PSCAD/EMTDC V5. At the Apollo Inverter Station, the HVDC controls and the eight converter bridges connected to one three-phase 275 kV AC Bus were modelled. The Eskom network connected to the Apollo Inverter Station was modelled using the CIGRE benchmark model. Since the aim of the study was transient over-frequencies on the Songo Converter Bus, the GMPC angle control mode was not considered in the simulations. This mode is crucial for HVDC power modulation during parallel operation of the HVDC and HVAC systems. The modulation is based on the derivative of the voltage angle difference between Songo and Apollo and the derivative of the Songo-Bindura power. During over-frequencies on the Converter Bus, the HVAC and HVDC systems are not coupled, in other words, the BC is open. Therefore, the parallel operation of the HVDC scheme and the HVAC system from Songo to Apollo, as illustrated in Fig. 1.2, was not simulated. In fact, the GMPC was not modelled. However, the use of transient overload capacity of the healthy pole during load rejections was also considered in the simulations. This is done by the GMPC. The generators governors were modelled, with a frequency dead band of zero. Although the GMPC was not modelled, the system (model) behaviour was similar to the actual system during HVDC load rejections.

Since the over-frequency events on the Converter Bus are electromechanical transients that usually last for some seconds, the duration of the simulations was 40 to 60 seconds. Due to this large duration and complexity of the simulated system, the PSCAD snapshot feature was applied.

4.2. System Model Components

4.2.1. Songo-Apollo HVDC Scheme

a) Rectifier – Current Control

In an HVDC scheme, for monopolar operation, the DC current Id can be expressed using the rectifier and inverter voltages as:

$$I_d = \frac{V_{dcr} - V_{dci}}{R_{dc}} \quad (4.1)$$

Where V_{dcr} is the rectifier side DC voltage; V_{dci} is the inverter side DC voltage; and R_{dc} is the total DC side resistance.

According to equation (4.1), the DC current Id can be controlled either by using rectifier or inverter DC voltage, but commonly controlled on the rectifier side during normal operation.

So the direct voltage at the stations and the current (or power) can be controlled by controlling the voltages Vdcr and Vdci. This is accomplished by the control of the valve ignition angles α at

both stations or by control of the AC voltage Vl through tap changing of the converter transformers. This is done by the HVDC controls at the pole level. The ignition angle control, which is rapid (1 to 10 ms), and tap changing, which is slow (5 to 6 seconds per step), are used in a complementary manner. Ignition angle control is used initially for rapid action, followed by tap changing to restore the converter firing angles to their normal range.

The main thyristor converter control equation is given by equation (4.2). This equation demonstrates that the DC voltage can be manipulated by varying the firing angle α.

$$V_{dr} = \frac{3\sqrt{2}}{\pi} V_l cos\alpha - \frac{3}{\pi} X_c I_d \qquad (4.2)$$

Where V_{dr} is the rectifier side DC voltage; V_l is the converter transformer secondary line voltage; α is the ignition delay angle; X_c is the commutating reactance; and Id is the direct current.

At the Songo-Apollo HVDC scheme, the rectifier station (Songo) controls the current and the inverter controls the extinction advance angle ɣ in normal operating conditions.

At the rectifier station (current control), at the pole control unit, the converter firing angle is controlled with a feedback control system similar to the one shown in Fig. 4.1. The rectifier DC voltage increases or decreases according to equation (4.2). This voltage is used to adjust the DC current set point. For example, if the DC current is larger, the current error is positive, consequently the firing angle α_0 is increased in order to reduce the DC current. Current control can only be established for an angle α_0 greater than αmin.

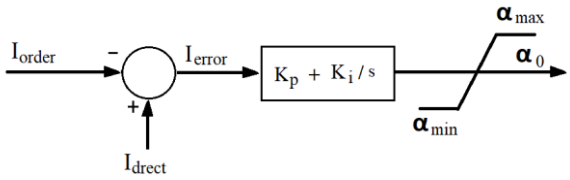


Fig. 4.1: Simplified current controller.

In Fig. 4.3 are represented the rectifier and inverter voltage-current control characteristics A and B respectively for a monopolar HVDC transmission scheme. Assuming line resistance to be negligible, the pole voltage at the rectifier station will be equal to the pole voltage at the inverter station (Vdcr = Vdci = Vd). Similarly, the DC current will be equal (Idcr = Idci = Id) for both stations. As a result, the operating points for the rectifier and inverter stations are the intersection points of the voltage-current characteristics of both stations.

The rectifier control characteristic A in Fig. 4.3 has two main regions. One for constant current control mode (CC) and other for minimum firing angle (α_0= αmin), represented as constant ignition angle (CIA). In many rectifier stations αmin= 5°.

b) Inverter – Constant Extinction Angle Control

At the inverter station, it is important to keep a safe extinction angle (ɣ) to prevent commutation failure. The minimum ɣ required for safe commutation with high-power thyristors is usually

around 10° – 15°. Therefore, ɣ reference is typically set to around 15° – 20°. The minimum extinction angle control mode is also called the constant extinction angle control mode.

The constant extinction angle (CEA) control mode is usually applied at inverter stations. In fact, the inverter station has three control systems – voltage control, extinction angle control and current control – which compete through the minimum element and the one that gives minimum angle defines the operating mode, which is usually the extinction angle (ɣ) controller for most inverter stations, including Apollo.

Some inverter stations normally use DC voltage control mode which is more stable than the CEA mode. To achieve this, in normal operating conditions, the α defined by the CEA controller αɣ will be only a few degrees larger than the α defined by the constant voltage controller αV, allowing some margin for the regulation of the DC voltage without switching to CEA. However, during disturbances, the inverter station may change to CEA or to CC mode.

Equation (4.3) demonstrates that the power factor is best for a value of extinction angle ɣ that is as small as possible. However, the probability of commutation failure increases as ɣ decreases.

$$\cos\phi \approx \frac{1}{2}[cos\gamma + \cos(\gamma + \mu)] \tag{4.3}$$

Where ϕ is the power factor angle; ɣ is the extinction advance angle; and μ is the overlap angle.

Therefore, a compromise is chosen for γ_{min} typically in the range of 15° to 18°. In Fig. 4.2 it is represented a simplified extinction angle controller.

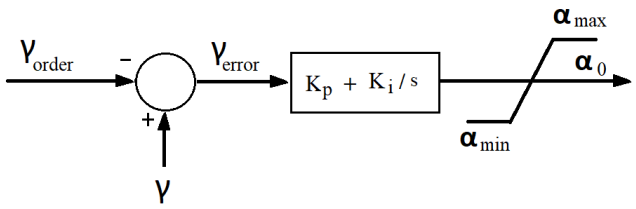


Fig. 4.2: Simplified extinction angle controller.

At the inverter station the pole DC voltage is given by the following equation:

$$V_{di} = \frac{3\sqrt{2}}{\pi} V_l cos\gamma - \frac{3}{\pi} X_c I_d \tag{4.4}$$

Where V_{di} is the inverter side DC voltage; V_l is the converter transformer secondary line voltage; ɣ is the extinction advance angle; X_c is the commutating reactance; and I_d is the direct current.

From equation (4.4), the inverter voltage - current characteristic B, is represented in Fig. 4.3. However, an additional constant current (CC) part is added to the characteristic (vertical line). This part is to ensure successful operation of the scheme in case a reduction on rectifier side AC voltage V_l resulting in downward drop of the uncontrolled part of the rectifier characteristic. If the constant current part at the inverter were absent, there would no longer be an intersection point and the system would run down to zero current. So the constant current (CC) part at the inverter allows for a degraded mode of operation.

At the inverter terminal, the transition from CEA to CC modes can be smoothly done by the insertion of current error control (CEC) in the control system. The CEC improves the dynamic performance of the HVDC scheme, when the inverter changes from CEA to CC mode, see Fig. 4.3. In the PSCAD model used for simulations, the CEC mode was included, see Fig. 4.6.

In Fig. 4.3, I_m is called the current margin and it is typically 10% of the current order.

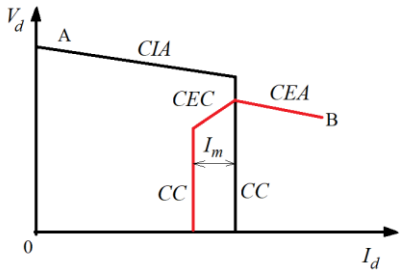


Fig. 4.3: Converter characteristics.

In Fig. 4.4 are represented the rectifier and inverter characteristics, including the voltage dependent current order limit (VDCOL). The VDCOL function is included in the converter characteristics to prevent voltage instability or HVDC system collapse. When the bus voltage decreases, the reactive power supplied to the converters by the AC filters or shunt capacitors also decrease. So to prevent voltage instability or system collapse, the DC current is also reduced by the VDCOL function.

At reduced voltages there is also risk of commutation failures, what make the valves conduct beyond the 120° conduction interval. Since the valves are designed to carry rated current for only 120°, they risk damage from overheating. Hence VDCOL is required to protect the valves during voltage reduction. So, after voltage reduction for more than 10%, the current is also reduced, usually to 30% or 40% of the rated value.

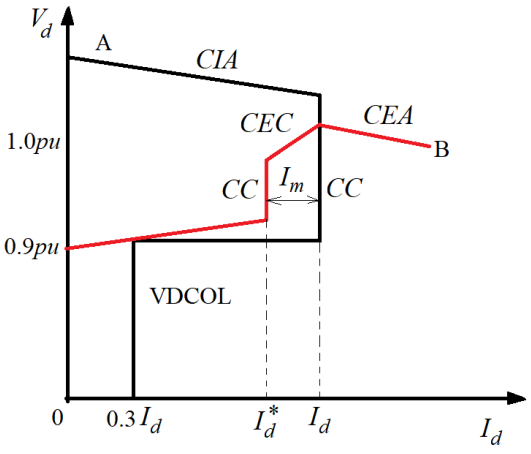


Fig. 4.4: Converter characteristics, including VDCOL.

The Songo-Apollo HVDC scheme represented in Fig. 1.1 was modelled in PSCAD, based on the CIGRE benchmark model and generic HVDC models. The HVDC controls models were also developed for both converter stations (Songo and Apollo) based on tuned generic controls. The parameters used for the HVDC control circuits were the default PSCAD generic controls

parameters, but tuned to reflect the actual system behaviour. The power circuit parameters used on the model were the actual Songo-Apollo HVDC scheme parameters.

The actual parameters of the following equipment were used for Songo Rectifier Station: AC filters (inductance, capacitance and resistance); DC filters (inductance, capacitance and resistance); smoothing reactor (inductance and resistance); surge capacitor bank (capacitance); converter transformers (MVA, frequency, leakage reactance, voltages, etc.); converter valves (thyristor on resistance, thyristor off resistance, thyristor forward voltage drop, thyristor forward breakover voltage, snubber resistance, snubber capacitance, inductance, etc.); power station to converter station AC transmission lines (impedances, frequency, etc.); and Songo-Apollo transmission line (resistance, capacitance and inductance). The DC line configuration was based on CIGRE benchmark model.

The Songo DC filters and AC filters parameters and configuration were also used for Apollo inverter station.

The Songo rectifier station control system used in PSCAD consists of a current controller, designed to maintain the HVDC system current constant. The measured DC current at Songo is compared with the reference current (desired current) to produce the current error. The current error produced is given to conventional proportional integral controller to produce the advance angle (β), which is subtracted from π to obtain the converters firing angle (α), see Fig. 4.5.

In the Fig. 4.5, it is also represented the force retard function, which is mainly designed to immediately clear DC line faults. It is applied when valve overcurrent is detected (current greater than 1.2 pu).

For the force retard operation, the valve current measured is compared with 1.2 pu reference current, using a comparator. When the valve measured current is greater than 1.2 pu, the output of the comparator is 1. Consequently, the force retard selector moves to position 1, that corresponds to 163°. The output of the force retard selector is connected to the input of the rate output limiter.

The rate output limiter, which the unit is 1/s, was inserted to limit the maximum increase rate and the maximum decrease rate of the input. The input of this block is the force retard firing angle, which immediately changes from zero to 163°.

After the output limiter, the angle is multiplied by the constant gain 0.017453 to convert it from degrees to radians since the angle defined by the current error and proportional integral controller is in radians.

The maximum firing angle is selected between the angle defined by the current error and the angle defined by force retard operation. The selection is done by maximum component.

Although, the inverter station has three control systems – voltage control, extinction angle control and current control – which compete through the minimum element and the one that gives minimum angle defines the operating mode, for simulations there were only considered the constant extinction angle (γ) and the current control modes. The constant extinction angle

(ɣ) controller was considered because it is the controller that is usually in operation at the inverter station, during steady state operation.

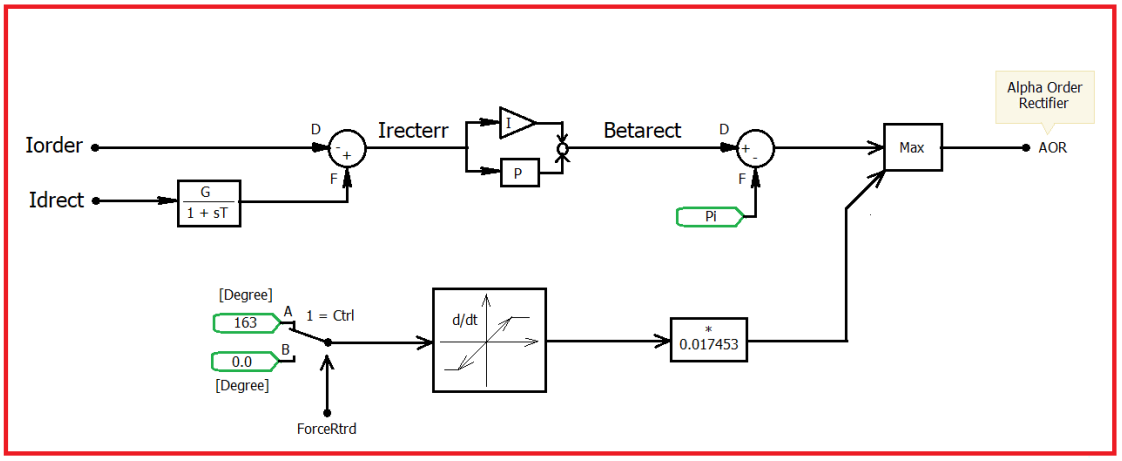


Fig. 4.5: Modelled rectifier station control system.

The current controller was used because it is important during disturbances to prevent the HVDC system collapse. The Apollo inverter control system used for simulations consists of a current controller to maintain the HVDC system current constant and extinction angle controller for maintaining the constant extinction angle (ɣ). The inverter current controller receives current reference from the rectifier station, which is reduced by a current margin Im of 10%. During normal operation of the HVDC scheme, the inverter current controller is on saturation, demanding firing angle (α) which is much larger than the inverter α demanded by the gamma controller. The inverter current controller enters into operation when the rectifier loses current control and the current error is greater than 10%. Actually, it usually happens during HVDC disturbances. The inverter station control system is represented in Fig. 4.6.

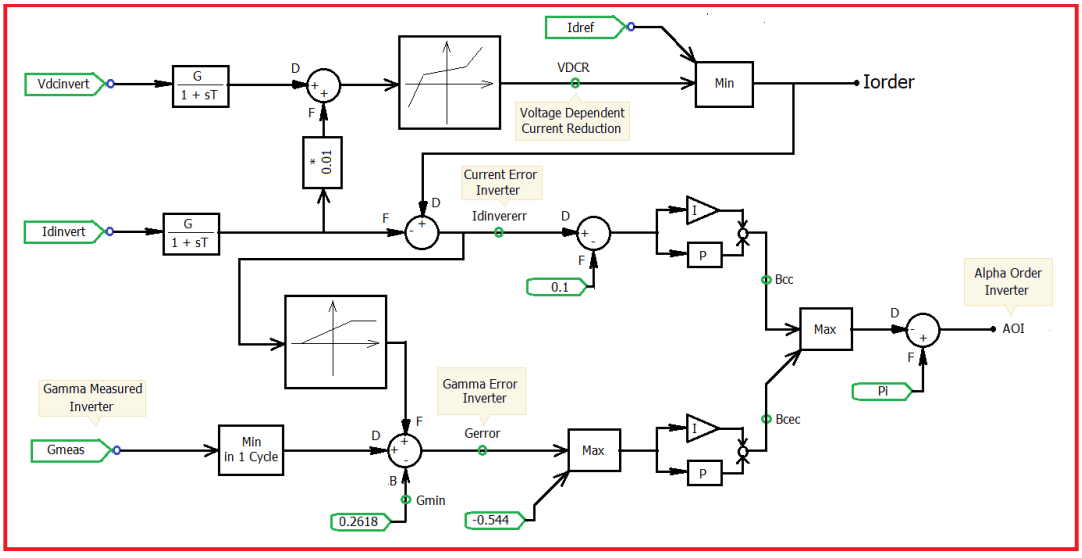


Fig. 4.6: Modelled inverter station control system.

In Fig. 4.6, cc is current control, while cec is constant extinction angle control and B is the advance angle. The current error control described above is represented between the current error and the gamma summing point.

In the designed HVDC scheme PSCAD model, for overcurrent protection, the force retard function was included in the rectifier control system. So, the current on the valves at Songo were measured, being the setting for force retard activation 1.2 pu and for force retard deactivation 1.0 pu. On force retard operation, the firing angle considered in the simulations was 163°. It means, when the valve DC current reaches 1.2 pu, the firing angle at the rectifier station is increased to 163° after an ON delay time of 20 ms, in order to immediately reduce the DC current to naught. This was the only HVDC protection considered in the simulations. The bridge AC breakers are tripped when the current reaches 3.2 pu. A 100 ms time delay for breaker opening was included in the simulations.

Since the aim of the study was over-frequencies on the Songo Converter Bus, in the simulations almost all the measurements were done at Songo.

4.2.2. Control Parameter Estimation of Regulators in Songo-Apollo HVDC Scheme

For the control of the HVDC scheme, proportional integral (PI) controllers are used as the basic regulators of the control systems [14]. They are used due to their simplicity, but robust for complex nonlinear dynamic systems [14]. Therefore, for the simulation of the Songo-Apollo HVDC scheme on PSCAD/EMTDC Version 5.0, PI controllers were used on the constant current regulators both on the rectifier and inverter stations and they were also used on the constant extinction-angle regulator at the inverter station. Since the aim of the study is over-frequency issues at the rectifier station, the constant voltage regulator was not included in the inverter controls.

4.2.2.1. Rectifier Constant Current Regulator

For the rectifier constant current regulator, the following proportional integral controller is used:

$$G_c(s) = K_p\left(1 + \frac{1}{T_i s}\right) \tag{4.5}$$

Where Gc(s) is the controller transfer function; Kp is the proportional gain; and Ti is the integrator time. Various methods are proposed by literature to calculate the parameters of the controller Gc(s). In this project, MATLAB and PSCAD/EMTDC software packages are used to find Kp and Ti.

Nevertheless, to find the initial parameters of Kp and Ki of the control transfer function Gc(s), the mathematical model of the plant (converter stations and transmission lines) are required. In other words, the transfer function of the converter station and HVDC transmission lines are necessary, in order to obtain the closed-loop transfer function of the HVDC scheme, including the current regulator. After finding the plant transfer function, calculate the PI parameters of the controller Gc(s).

Expressing the converter voltage V_{dr} as a function of the firing delay angle α, and multiplying V_{dr} by the transmission line admittance, the actual current I_{drect} can be obtained. I_{drect} is

indispensable to calculate the current error, required by the current regulator to calculate the firing delay angle α. The closed loop control system is represented in Fig. 4.7.

In Fig. 4.7 it is represented the rectifier current control system. Gc(s) is the current regulator transfer function, consisting of a PI controller, represented by equation (4.5).

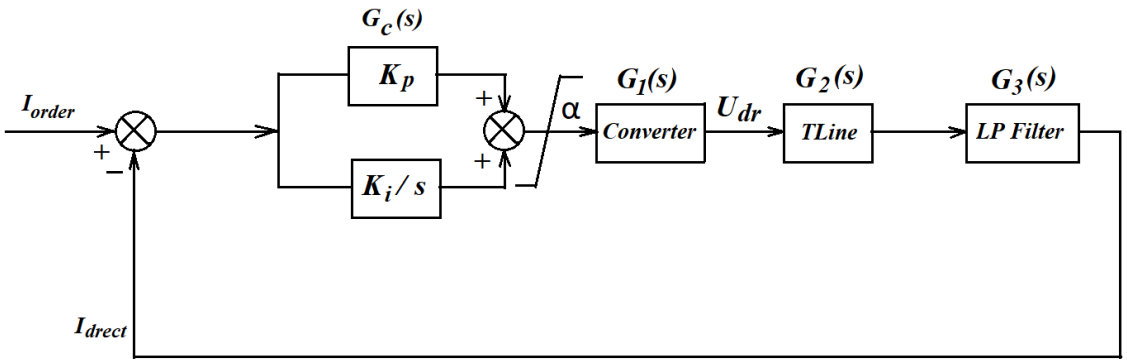


Fig. 4.7: Rectifier current controller system.

The open-loop transfer function of the HVDC scheme, represented in Fig. 4.7, is

$$G(s) = G_c(s) \times G_1(s) \times G_2(s) \times G_3(s) \tag{4.6}$$

In the following paragraphs, we will determine the transfer functions of converter bridges G1(s), transmission line G2(s), low-pass (LP) filter G3(s) and constant current regulator parameters.

a) Converter Station Transfer Function $G_1(s)$

The Songo-Apollo HVDC scheme is a bipolar system, consisting of four bridges in series per pole. However, only monopolar configuration with 4 bridges in operation is considered to represent the HVDC scheme transfer function.

The converter bridges transfer function G1(s) can be represented as a first order circuit, with the following transfer function [14]:

$$G_1(s) = \frac{G_{10}}{1+sT_1} \tag{4.7}$$

Where G10 is the open loop gain; and T1 is the time constant.

Since there are four converter bridges in operation, two delta bridges and two star bridges, it is 12-pulse operation. The SAPP network frequency is 50 Hz. So the time constant T1 is:

$$T_1 = \frac{1}{12f} = \frac{1}{12 \times 50} = 1.6667\ ms$$

The open loop gain G_{10} can be found from the following equation [14]:

$$G_{10} = -U_{dio} sin\alpha_0 = -\frac{3\sqrt{2}}{\pi} \times U_l \times B \times T \times \sin(\alpha_0) \tag{4.8}$$

Where U_{dio} is the ideal no load direct voltage; U_l is the AC system side line-to-line voltage; B is number of bridges in series per pole; T is the transformer turns ratio; and α_0 is the ignition angle (α) operating point, which is α reference of the rectifier station.

For Songo rectifier station, U_l = 220 kV; B = 4; T = 0.52 and α_0 = 15.66°. So

$$G_{10} = -\frac{3\sqrt{2}}{\pi} \times 220 \times 4 \times 0.52 \sin(15.66^{o}) = -166.81\ kV \quad (4.9)$$

So Songo converter station transfer function is:

$$G_1(s) = -\frac{166.81\times10^3}{1+1.6667\times10^{-3}s} \quad (4.10)$$

It is the open loop gain of the converter.

b) Transmission Line Transfer Function *$G_2(s)$*

To find the transmission line transfer function G2(s), the CIGRE benchmark HVDC transmission line model, represented in Fig. 4.8 will be used. It was also used for PSCAD/EMTDC Version 5.0 simulations.

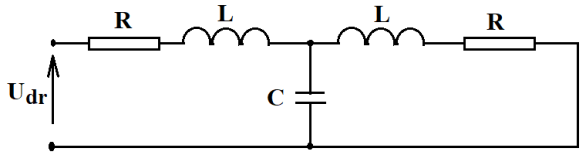


Fig. 4.8: CIGRE HVDC transmission line *T* model.

The equivalent impedance Z(s) of the model represented in Fig. 4.8, seen from the rectifier station is:

$$Z(s) = R + Ls + \frac{(Ls+R)\times\frac{1}{Cs}}{Ls+R+\frac{1}{Cs}} = R + Ls + \frac{\frac{Ls+R}{Cs}}{\frac{LCs^2+RCs+1}{Cs}} = R + Ls + \frac{Ls+R}{LCs^2+RCs+1}$$

$$Z(s) = \frac{RLCs^2+R^2Cs+R+L^2Cs^3+LRCs^2+Ls+Ls+R}{LCs^2+RCs+1}$$

The equivalent admittance Y(s) is:

$$Y(s) = \frac{1}{Z(s)} = \frac{s^2LC+sRC+1}{s^3L^2C+2s^2RLC+s(R^2C+2L)+2R} \quad (4.11)$$

For Songo-Apollo HVDC scheme, the following parameters were considered for PSCAD simulations and also for transmission line transfer function G2(s):

$$R = 7.0\ \Omega; \quad L = 0.5968\ H; \quad C = 26\ \mu F$$

Substituting in equation (4.11), the Songo-Apollo TL admittance equation is obtained:

$$Y(s) = \frac{15.5168\times10^{-6}s^2+182\times10^{-6}s+1}{9.26\times10^{-6}s^3+217.24\times10^{-6}s^2+1.195s+14} \quad (4.12)$$

Equation (4.12) is in fact Songo-Apollo TL transfer function G2(s).

$$G_2(s) = \frac{15.5168\times10^{-6}s^2+182\times10^{-6}s+1}{9.26\times10^{-6}s^3+217.24\times10^{-6}s^2+1.195s+14} \quad (4.13)$$

c) Low-Pass Filter Transfer Function $G_3(s)$

The low-pass (LP) filter G3(s) is used in the measurement circuit (feedback loop) to filter high frequency harmonic currents. The low pass filter can be represented by a first-order circuit, with the time constant τ of 0.0012 s [14].

$$G_3(s) = \frac{G_{30}}{1+s\tau} \quad (4.14)$$

Since in the control circuit the quantities are expressed in per unit (pu) values, the proportional constant G30 of the LP filter will be the reciprocal of the base dc nominal current (1800 A).

$$G_3(s) = \frac{\frac{1}{1800}}{1+0.0012s} = \frac{5.5556\times10^{-4}}{1+0.0012s} \quad (4.15)$$

It is the transfer function of the low-pass filter, including the per unit conversion.

d) Plant Transfer Function

The plant open-loop transfer function is:

$$g(s) = G_1(s) \times G_2(s) \times G_3(s) \quad (4.16)$$

$$g(s) = \frac{(-166.81\times10^{3})(15.5168\times10^{-6}s^2+182\times10^{-6}s+1)\times5.5556\times10^{-4}}{(1+1.6667\times10^{-3}s)(9.26\times10^{-6}s^3+217.24\times10^{-6}s^2+1.195s+14)(1+0.0012s)}$$

$$g(s) = -\frac{(92.67)(15.5168\times10^{-6}s^2+182\times10^{-6}s+1)}{(1.6667\times10^{-3}s+1)(9.26\times10^{-6}s^3+217.24\times10^{-6}s^2+1.195s+14)(1+0.0012s)} \quad (4.17)$$

In Fig. 4.9, it is represented the unit-step response of the plant transfer function, obtained on MATLAB simulation. The minus signal on *g(s)* function was ignored. In fact, the minus signal will only have an impact on the sign of the amplitude axis, which will be below zero. To take into account the minus signal, the signals of the reference current (ordered current) and measured current will be interchanged on the control loop.

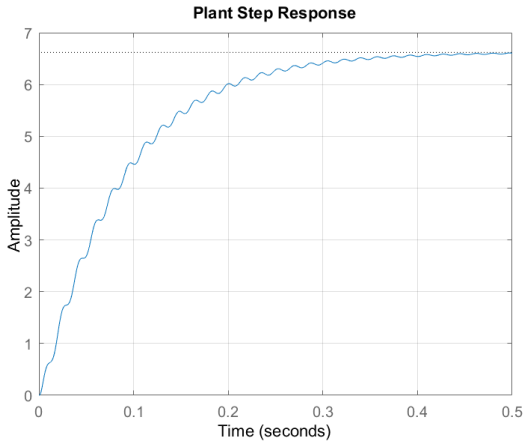


Fig. 4.9: Unit-Step response of the HVDC plant.

In Fig. 4.10, it is represented the body diagram of the plant transfer function, obtained on MATLAB.

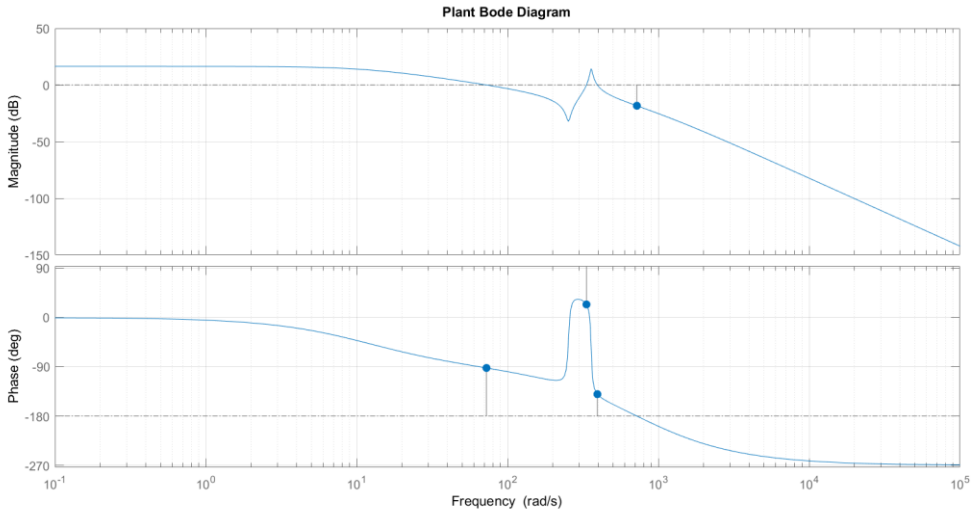


Fig. 4.10: Plant Bode Diagram.

e) Tuning of the Constant Current Regulator $G_c(s)$

The tuning HVDC PI controllers is a challenging task. The MATLAB software package was used to find the initial parameters of the PI current regulator Gc(s). The following criteria was defined to tune Gc(s):

1. HVDC system stead-state and transient stability;
2. Maximum overshoot of 20%; and
3. Maximum rise time of 40 ms.

Based on this three criteria, the MATLAB software package was used to tune the Gc(s), described by equation (4.5). The following parameters were found:

K_p = 0.39587 Overshoot = 18 %

K_i = 13.0094 Gain margin = 25.4 dB @ 688 rad/s

Rise time = 34.1 ms Phase margin = 55.1 deg @ 371 rad/s

Settling time = 160 ms Stability = stable

The closed-loop step response of the system for the controller Gc(s) with the parameters above is illustrated in Fig. 4.10.

To find the suitable parameters of the GC(s), different parameters shall be simulated on PSCAD and the results compared. It will allow the tuning of Gc(s), starting from the initial parameters found on MATLAB.

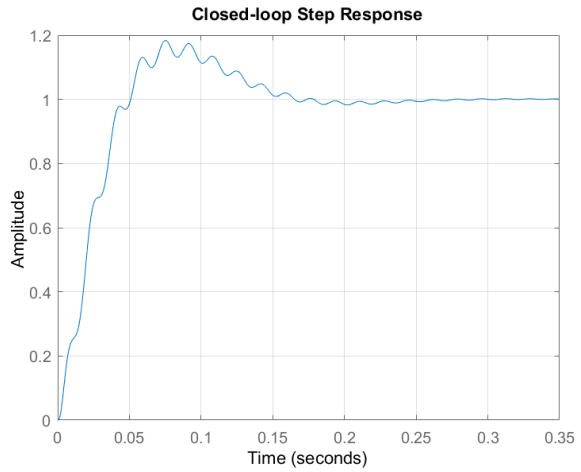


Fig. 4.11: Closed-loop step response of the HVDC scheme.

The following parameters of Gc(s) were found after PSCAD/EMTDC Version 5.0 simulations: Kp = 0.7 and Ti = 10 ms.

4.2.2.2. Inverter Constant Current and Minimum Gama Regulators

The method applied to tune the rectifier Gc(s) was also applied to tune the inverter constant current and minimum gamma regulators. The same performance criteria defined for tuning the rectifier Gc(s) was also applied for the inverter regulators.

The initial parameters considered were: Kp = 0.7 and Ti = 10 ms.

After PSCAD simulations the following parameters were found:

a) Constant Current Regulator
   K_p = 0.63 T_i = 15 ms

b) Constant Gamma Regulator
   K_p = 0.75 T_i = 54 ms

These parameters were used for the over-frequency study at the Songo Converter Bus.

4.2.3. Cahora Bassa Generators

The Cahora Bassa hydro generator models were developed in PSCAD, based on PSCAD models. The hydro turbines and governors were also modelled. The PSCAD pre-existing salient pole synchronous generator model was used for simulations. The synchronous generator was connected to an exciter, a hydro governor and hydro turbine models, as illustrated in Fig. 4.12. However, on the settings windows of these machine components actual Cahora Bassa Generators' parameters were introduced to reflect the real system behaviour. The Cahora Bassa generator parameters, such as inertia constant, permanent droop, transient droop, turbine ramp rates, transient reactance, rated power, rated voltages, rated currents, and step-up transformers parameters were used.

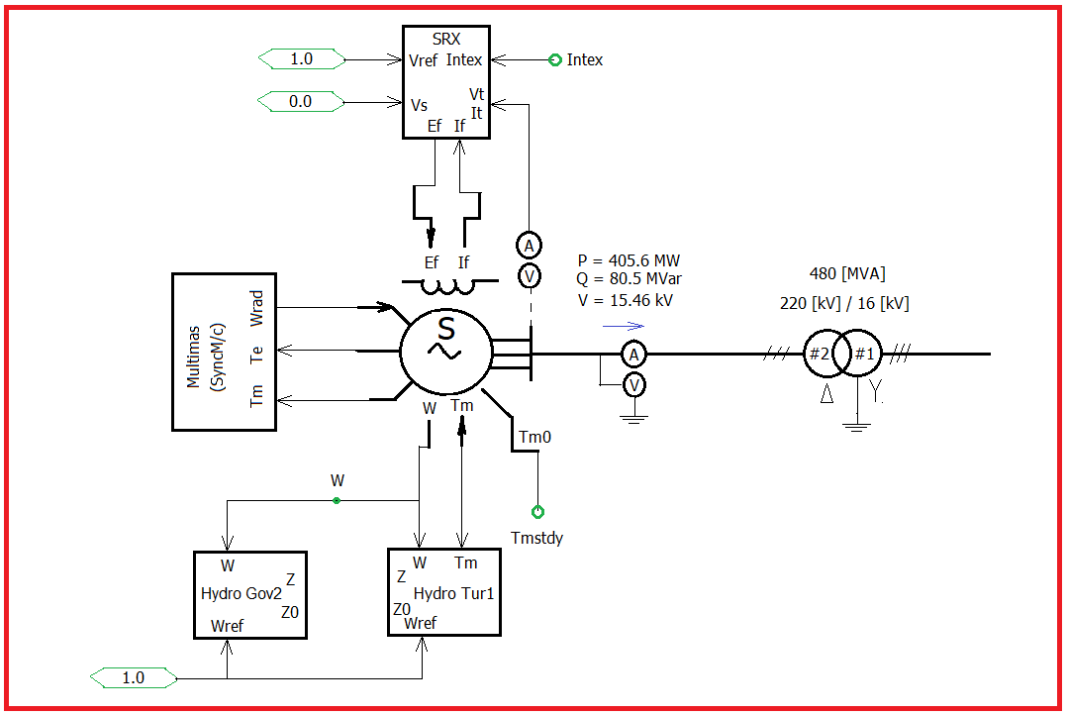


Fig. 4.12: Modelled salient pole synchronous generator and the connected 480 MVA, 16 kV / 220 kV step-up transformer.

Although the automatic voltage regulator (AVR) and excitation models are not so crucial since it is an electromechanical transient study, they were also modelled. Fig. 4.13 illustrates the AVR controls and excitation. So electromechanical simulations were carried out with a time step of 200 µs.

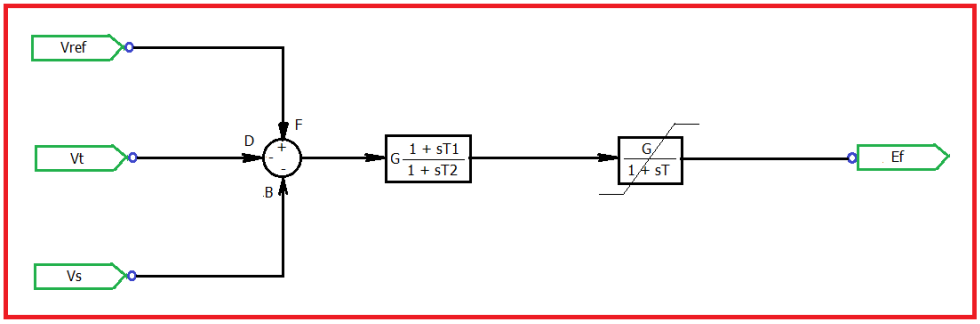


Fig. 4.13: Modelled AVR control system used for simulations.

Although the GMPC was not modelled, the frequency control mode was considered in the simulations, since the aim of the study was over-frequencies on the Converter Bus. To simulate the frequency control mode, the reference frequency of all the Cahora Bassa hydro generators was set to 50 Hz, with the dead band of zero (primary frequency control). In this way, after an HVDC load rejection (excess of mechanical power), the governor responds by immediately closing the wicket gates to reduce the mechanical power in the turbines. However, due to the high time constant of the wicket gates, the mismatch between mechanical and electrical power will cause acceleration of the generators' rotors.

Since all five Cahora Bassa generators have the same parameter values (permanent and transient droops, ramp rates, etc.), for the generators connected to same bus, their response was expected to be approximately the same.

The BC tripping was also considered in the simulations. Depending on the HVDC load rejected, it trips after 110 MJ HVDC load rejected. It corresponds to an energy of 220 MW during 500 ms.

In the simulations, the solution time step and the channel plot step was 200 μs.

4.3. System Model Validation

4.3.1. Introduction

The Cahora Bassa hydro generators and Songo-Apollo HVDC scheme models were tested and validated. The validation process consisted of comparing the actual Transient Fault Recorder (TFR) waveforms and the PSCAD/EMTDC simulation waveforms.

4.3.2. Songo-Apollo HVDC Scheme Model

For the detailed bipolar HVDC scheme model validation, two typical system contingencies (bridge tripping at Songo and transient DC line fault) were chosen for comparison.

The emergency switch off (ESOF) sequence of converter Bridge 6 at Songo was one of the contingencies considered for Songo-Apollo HVDC scheme model validation. It is not a common switch off sequence. On the ESOF operation of a single converter bridge at Songo, the secondary side of the converter transformers are short-circuited by overcurrent diverters in order to instantaneously switch off the bridge to protect the converter valves against excessive over-currents (DC current greater than 3.2 pu). It takes 60 ms, from which 4 ms for over-current diverters closing. It is followed by the bridge 220 kV AC breaker tripping and bridge thyristor blocking. At Apollo inverter station this switch off sequence was deactivated in April 2001, because it was invented for rectifier protection, but installed at Apollo for possible power reversal.

Fig. 4.14 shows the field measurements of currents on the secondary side of converter transformers, during an ESOF sequence of bridge 6 at Songo. This event took place on 25th October 2016 at 23:24:36.180.

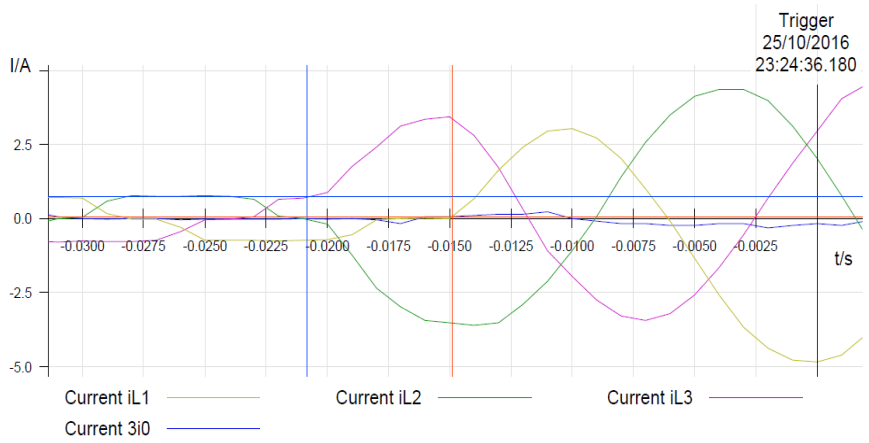


Fig. 4.14: Field measurement of Bridge 6 transformer currents (in kA) on the secondary side, during an emergency switch off sequence.

Fig. 4.15 shows the currents measured on the secondary side of converter transformers of bridge 6 at Songo, during Bridge 6 ESOF simulation.

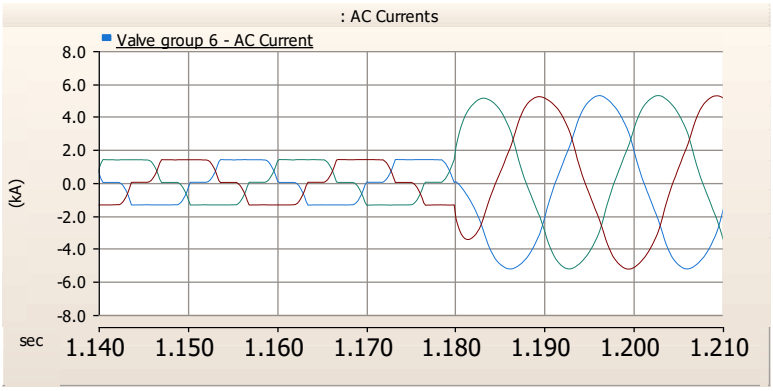


Fig. 4.15: Bridge 6 transformer currents on the secondary side, during an emergency switch off sequence simulation.

Comparing figures 4.14 and 4.15 it can be seen that the waveforms are almost the same.

During the bridge 6 tripping event described above, the BC did not trip at Songo. Fig. 4.16 illustrates the field frequency deviation from 50 Hz measured on the Converter Bus. It can be seen that the Converter Bus frequency deviation is almost naught, because of the fact that the frequency was determined by the SAPP.

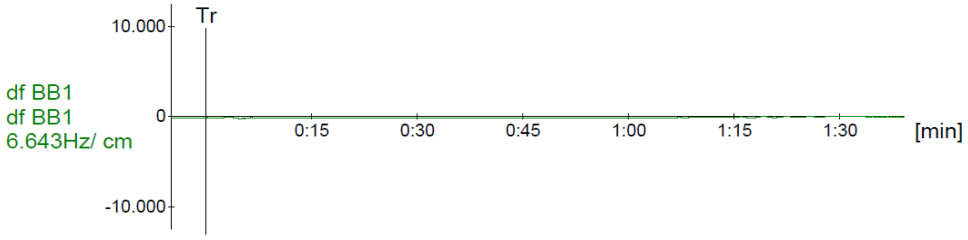


Fig. 4.16: Converter Bus frequency deviation (Hz) measurement during an emergency switch off sequence of bridge 6 at Songo.

During the simulation of Bridge 6 ESOF sequence at Songo, the frequency deviation from 50 Hz on the Converter Bus, which was coupled to the Non-Converter Bus, was as shown in Fig. 4.17. In simulation the SAPP was not modelled and hence the effect of the SAPP on the frequency deviation was not modelled.

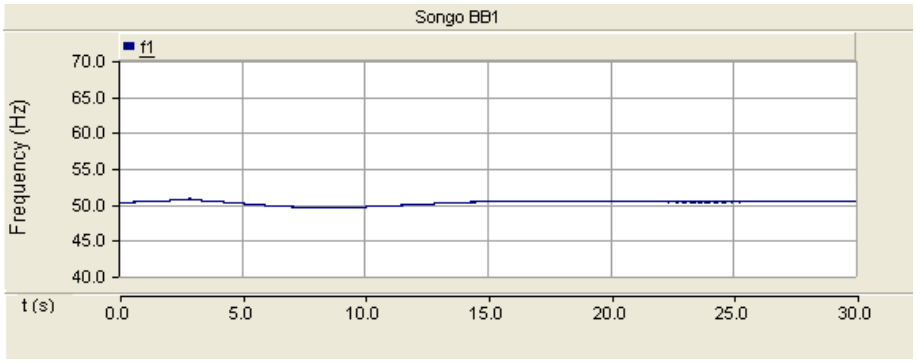


Fig. 4.17: Converter Bus frequency deviation during an emergency switch off sequence simulation of Bridge 6 at Songo.

Fig. 4.18 shows an example of a transient DC line fault, close to the Songo Rectifier Station. By tuning the PSCAD generic controls the magnitude and duration of the DC current overshoot and the delay of the DC voltage could reasonable be adapted to the given TFR waveforms.

In Fig. 4.18 are represented the Pole 1 and Bridge 7 voltages, following the transient fault on the HVDC Line 1.

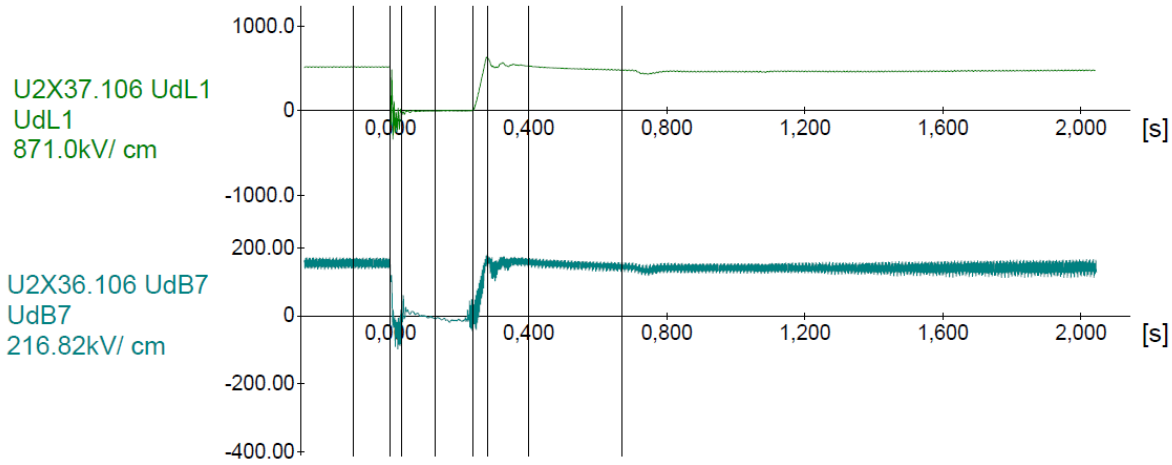


Fig. 4.18: Pole 1 and Bridge 7 voltages at Songo recorded by the TFR, during the transient fault on DC Line 1.

Fig. 4.19 shows the pole and the DC line voltages at Songo, following a simulation of a transient fault on DC Line 1. The pole voltage (VdcP) is measured after bridge 7, before the smoothing reactor, while the DC line voltage is measured at the beginning of the DC line. During transient DC line faults, the pole voltage can be negative, due to force retard operation, while the DC line voltage is nil.

On the Fig. 4.18 and Fig. 4.19, comparing the voltage waveforms of field measurements and PSCAD simulation, it can be seen that they are similar.

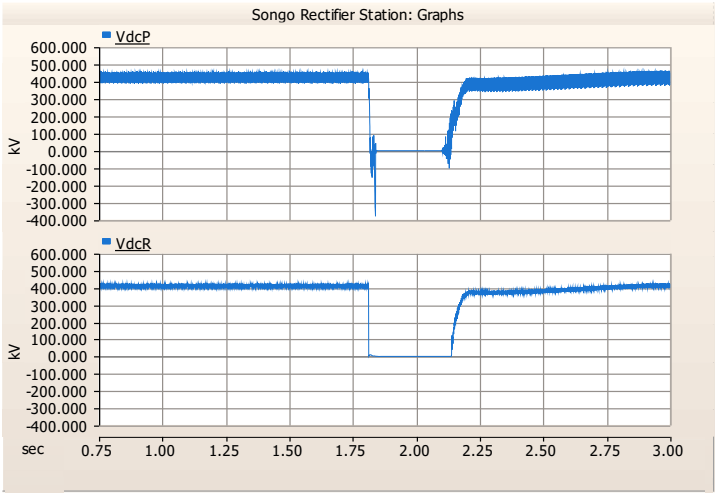


Fig. 4.19: Pole and DC line voltages at Songo rectifier station, during the transient fault simulation on DC Line 1.

Fig. 4.20 shows the DC current, for the transient event illustrated in Fig. 4.19. It was recorded by the TFR installed at Songo on the line side, after the smoothing reactor. This event is also described in section 3.6 of this report.

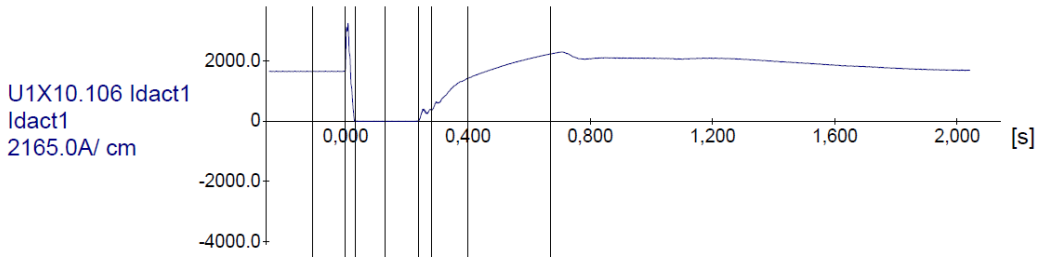


Fig. 4.20: DC current (in kA) measured at Songo by the TFR, during the transient DC Line 1 fault.

Fig. 4.21 illustrates the DC current measured at Songo, after a simulation of a transient fault on the DC Line 1 with a successful restart.

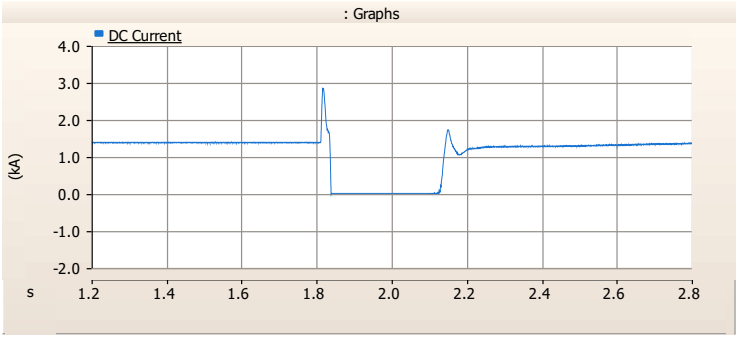


Fig. 4.21: Simulated DC current at Songo rectifier station, during the transient DC Line 1 fault.

Comparing the current waveforms of Fig. 4.20 and Fig. 4.21 it can be seen that they are almost similar.

For the same transient event on DC line 1, the actual frequency was compared with the frequency waveform obtained from PSCAD simulation. As can be seen in Fig. 4.22 and Fig. 4.23, the frequency deviation on both events is almost naught.

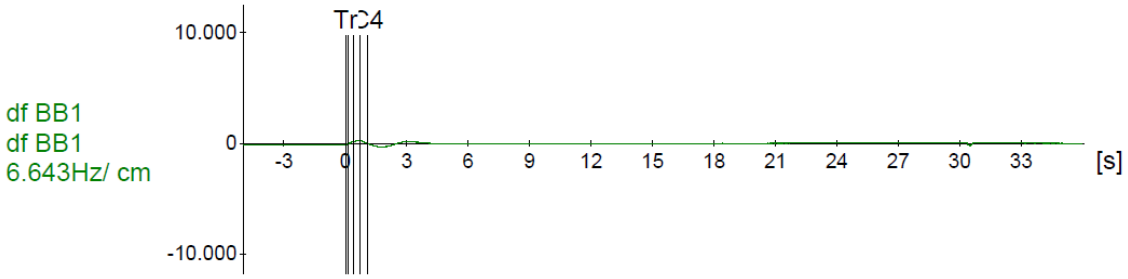


Fig. 4.22: Converter Bus frequency from field measurement

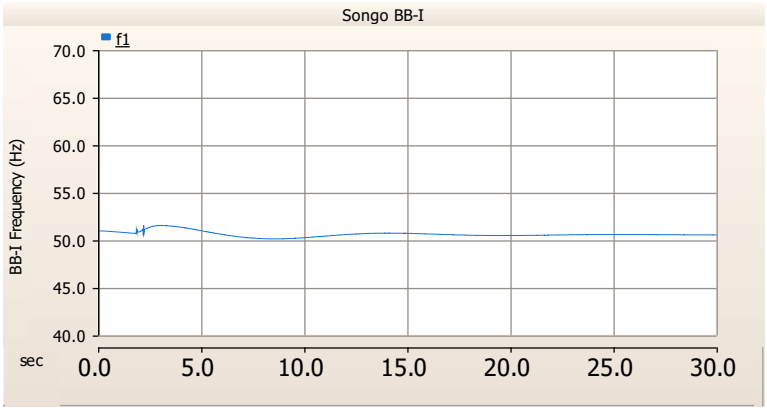


Fig. 4.23: PSCAD Converter Bus frequency simulation for the transient fault on DC Line 1.

The difference between the two waveforms is because the SAPP, which was not represented and not included in the simulations, has an impact on the Converter Bus frequency, when the BC does not trip. In this particular case, the Converter Bus frequency was only determined by Cahora Bassa Generators. However, this HVDC scheme PSCAD model can be validated.

4.3.3. Cahora-Bassa Hydro Generators Model

For the power station generators, by tuning the PSCAD generic controls and introduction of the actual generators parameters, the frequency deviation waveforms and duration were the same as the ones recorded by the TFR for the same events.

In Fig. 4.24, the actual frequency deviation recorded by the TFR, after the actual Pole 1 tripping without HVDC reserve capacity, following a permanent fault on DC Line 1 is shown. This event is described in section 3.5.

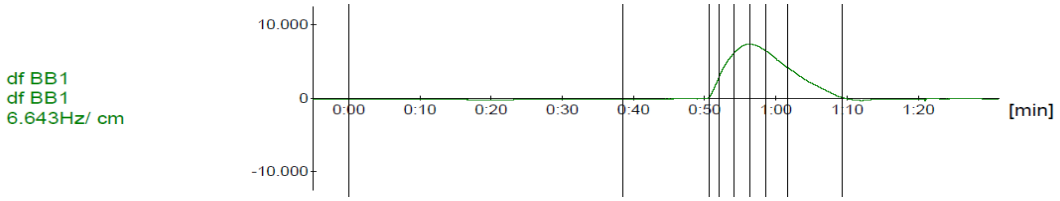


Fig. 4.24: Converter Bus frequency from field measurements, after HVDC Pole 1 tripping without reserve capacity.

In Fig. 4.25, the frequency at Songo BB-I, after a simulation of Pole 1 tripping. Prior to Pole 1 tripping, the system configuration and loading of the converter bridges and generators were almost the same as in the actual system described in Section 3.5.

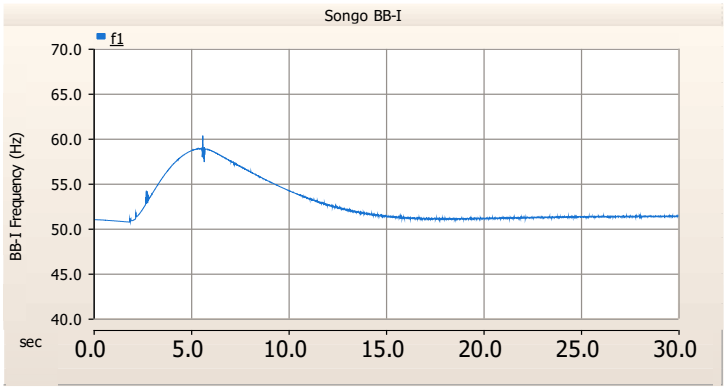


Fig. 4.25: Frequency at Songo BB-I, after Pole 1 tripping simulation without HVDC reserve capacity.

Comparing the frequency waveforms on BB-I represented in Fig. 4.24 and Fig. 4.25, it can be seen that they are similar for both the actual and simulated Pole 1 tripping.

4.4. Difference Between the PSCAD/EMTDC HVDC Controls Model and the Actual HVDC Controls

4.4.1. Introduction

The PSCAD/EMTDC Version 5.0 HVDC controls model used for simulations was compared with the actual HVDC controls, installed at Songo rectifier station. The main circuits of the HVDC controls, installed at Songo, are described on the sections below. The difference between these circuits and PSCAD/EMTDC Version 5.0 model are underlined on the respective sections. The Songo main HVDC controls printed circuit boards (PCBs) were simulated on LTSpice XVII software package to see their function and impact on the overall pole controls. Some PCBs were also simulated on PSCAD/EMTDC Version 5.0 to verify the results found on LTSpice XVII simulations and also to find their importance on the entire HVDC scheme. On the sections below are described the controls of an LCC HVDC rectifier station and compared with PSCAD/EMTDC version 5.0 HVDC controls model. It is assumed that Songo is the rectifier station and Apollo is the inverter station. The focus is on Songo rectifier station since the over-frequency study was conducted at Songo.

4.4.2. Reference Current Setting (I_{dref} *Setting*)

The main function of the reference current setting circuit, or reference current setting PCBs installed at Songo, is to generate the pole reference current required by the pole current regulator of the HVDC scheme. In normal operating conditions, the pole reference current (I_{dref}) is calculated by dividing the pole reference power, requested by the GMPC, by the actual pole voltage. Besides the function of generating the I_{dref}, the I_{dref} setting circuit also calculates the HVDC pole possible power required by the GMPC to generate the pole reference power. Furthermore, the I_{dref} setting circuit also limits the pole transient overload current during HVDC disturbances.

The main input variables of the I_{dref} setting circuit are:

- Pole reference power defined by the GMPC;
- Pole actual DC voltage;
- Reference current defined by the operator on the DC desk;
- Bus commutating voltage, measured on the three-phase Converter Bus;
- Pole actual DC current;
- Pole reference current to zero (I_{dref} = 0), from pole and HVDC transmission line protections.

The I_{dref} setting circuit also limits the rate of rise and rate of decrease of the reference current, I_{dref}. In Fig. 4.26, it is represented the circuit that limits the rate of rise and rate of decrease of the I_{dref}. This circuit was simulated on LTSpice XVII software to verify its function.

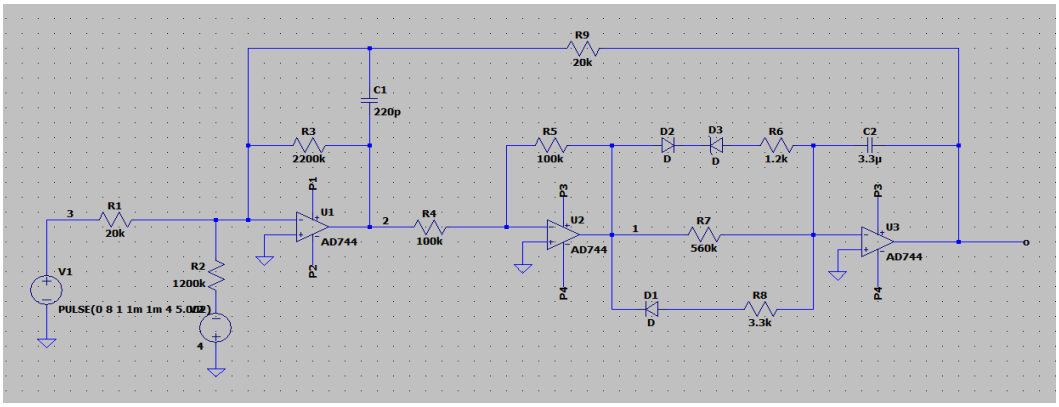


Fig. 4.26: Rate of rise limiter simulated on LTSpice XVII software.

In Fig. 4.27 are illustrated the input and output variables of the rate of rise limiter, represented in Fig. 4.26. The input variable is the green curve V(3), while the output variable is the blue curve V(0). These waveforms were obtained from LTSpice XVII simulation.

From Fig. 4.27, it can be seen that the rate of rise limiter, decreases the rate of rise of the input variable, which is a step input, although the input and output variables have different polarities. The rate of decrease of the output variable, cannot be easily seen, since it is very small, due to the scale used.

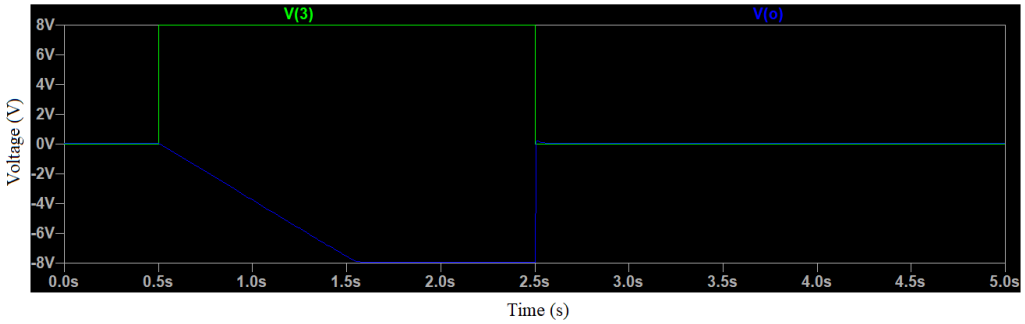


Fig. 4.27: Input and output variables of the rate of rise limiter, represented in Fig. 4.26.

While the actual I_{dref} setting circuit has six main input variables mentioned above, the PSCAD/EMTDC model only has the following inputs:

- Pole reference current;
- Pole actual DC voltage; and
- Pole actual DC current

Furthermore, the PSCAD/EMTDC Version 5.0 model does not have the rate of rise limiter, on the I_{dref} setting circuit.

Therefore, from what was exposed above, it can be seen that while the actual I_{dref} setting circuit is more complex, the I_{dref} setting circuit represented on PSCAD/EMTDC is much simpler. It has only three input and one output variables.

4.4.3. DC Current Regulator

The rectifier pole current regulator circuit is also the DC line voltage regulator, since the pole current is controlled based on the DC line voltage. The main function of the pole current regulator circuit is to generate the firing delay angle (α) based on the current error. The current error is the difference between the reference current I_{dref} and the actual measured current I_d. To achieve this, a proportional integral controller is normally used at the HVDC stations.

The following are usually the main input variables of the actual pole current regulator circuit:

- I_{dref} defined by I_{dref} *setting* circuit of the respective pole;
- I_{dref} defined by the I_{dref} *setting* circuit of the other pole;
- Pole actual DC current;
- I_{dref} from line and pole protections. This variable has only two states (0 or 1);
- Pole actual DC voltage;

On the actual controls, the pole current error enters the proportional integral controller. After the proportional integral controller, the “current error” passes through a band elimination filter. The band elimination filter is designed to eliminate 50 Hz noise.

The transfer function of the band elimination filter was determined based on the actual circuit. Equation (4.18) was found.

$$H(s) = \frac{2.251s^2+95.8s+213640}{s^2+943.9s+213640} \quad (4.18)$$

The bode diagram of equation (4.18) was obtained on MATLAB and it is shown in Fig. 4.28.

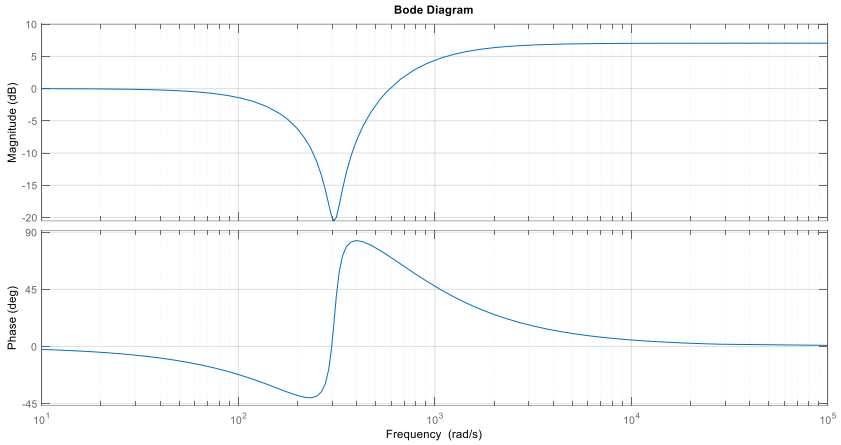


Fig. 4.28: Bode diagram of the transfer function (4.18).

From the bode diagram represented in Fig. 4.28, it can be concluded that the equation (4.18) represents a transfer function of a band elimination filter of 50 Hz (314.16 rad/s).

After the band elimination filter, the current error variable enters a linearized circuit to perform the arcsine function. From the actual arcsine function circuit, the following waveform was built using MS Excel.

The arcsine function circuit generates the firing delay angle (α) for the converter bridges.

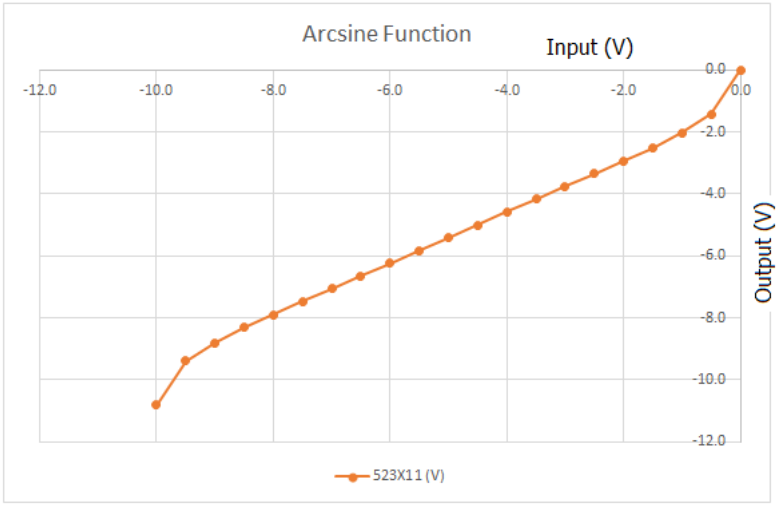


Fig. 4.29: Arcsine function.

The main differences between the pole DC current regulator of the PSCAD/EMTDC model and the actual pole DC current regulator are:

a) The PSCAD/EMTDC model does not have the maximum voltage limit, while the actual controls usually do have;
b) The PSCAD/EMTDC model does not contain the 50 Hz band elimination filter;

c) The PSCAD/EMTDC model does not have the linearization function, whereas the actual controls do have.

4.4.4. Converter Transformer Tap-changer Controller

On LCC rectifier stations, it is desirable to have a lower firing delay angle (α) to minimize reactive power consumption and also reduce the harmonics generated by the converter bridges. However, it is also important to ensure a sufficient safety margin of α to compensate for disturbances on DC and AC sides. Therefore, the firing delay angle (α) is usually set on the range from 16° to 20°. For Songo rectifier station, the reference firing delay angle (α_{ref}) is 15.66°. The converter transformers tap-changer controller circuit makes adjustments to the tap-changer position, increasing or decreasing the transformer ration, in order to maintain α at 15.66°. The tap-changer adjustments are also based on the no-load ideal direct voltage (U_{dio}) and tap-changer actual position.

The main input variables of the actual tap-changer controller circuit are:

- Actual value of the firing delay angle (α);
- Pole actual DC current;
- Actual commutating voltage;
- Converter transformer actual tap-changer position;
- Status of the AC filters (*on* or *off*);

The main output variables of the actual controllers are orders to increase or decrease the converter transformers tap-changer position.

The HVDC PSCAD/EMTDC Version 5.0 model used for simulations does not contain tap-changer controller circuit. The converter transformers tap-changer positions of the model are adjusted manually. This is the main difference between the PSCAD/EMTDC model and the actual HVDC controls.

4.4.5. HVDC Line Protections

On LCC HVDC schemes, the best way to bring the line current and voltage to zero rapidly, after a line fault, is to establish both stations as inverters. In this way, both stations drain the line energy stored in the electric and the magnetic fields. Therefore, both the actual HVDC controls and PSCAD models have the force retard operation.

The actual HVDC controls have the following HVDC line protections:

- Travelling wave protection;
- Current differential protection; and
- Open line protection;

However, on the PSCAD model used for simulations there is only overcurrent protection.

Immediately after a line fault, the actual line protections, besides blocking the HVDC current regulator, setting the firing angle to 180°, they also limit the reference current to zero, at almost the same time. This does not happen with the PSCAD model.

4.5. Conclusions

The step response of the HVDC scheme on PSCAD/EMTDC Version 5.0 is better than the step response of the HVDC plant on MATLAB. This is because the HVDC plant on MATLAB is not represented in detail. Furthermore, some rectifier and inverter parameters were not considered on the MATLAB representation. However, the MATLAB HVDC plant representation was useful to determine the initial PI controller parameters used for fine tuning of the PSCAD/EMTDC HVDC model.

At Songo Converter Station, the converter valves, converter transformers, AC filters, DC filters and smoothing reactors actual parameters were used for the PSCAD HVDC scheme model. At the Cahora Bassa Hydropower Station, the generators and the step-up transformers actual parameters were also used for the PSCAD generators models. The models PI controllers were tuned to reflect the actual Songo-Apollo HVDC scheme and the actual Cahora Bassa generators dynamic behaviour. Consequently, the Converter Bus frequency and voltage deviation during DC lines transient and permanent faults are similar for simulated and actual cases. The DC current during the same faults are also similar. Therefore, it can be concluded the PSCAD/EMTDC Version 5.0 models used for simulations -represent the actual Songo-Apollo HVDC scheme and the Cahora Bassa hydro generators models.

There are many differences between the HVDC PSCAD/EMTDC Version 5.0 model and the actual HVDC controls. The actual HVDC controls are far more complex than the PSCAD/EMTDC Version 5.0 models. However, the philosophy of the model and the actual controls are the same. So the model can be used for Songo Converter Bus over-frequency study.

After an HVDC load rejection, when the BC does not trip at Songo, the SAPP has an impact on frequency deviation on the Converter Bus. In the simulations above, the SAPP was not modelled in PSCAD hence the frequency deviation was only determined by the Cahora Bassa Generators. However, since the aim of the study is over-frequency on the DC Bus, modelling of the SAPP is not critical. This is because the BC usually trips after an HVDC load rejection, consequently the Converter Bus switches into the island mode of operation.

Chapter 5. DYNAMIC PERFORMANCE OF THE GMPC

5.1. Introduction

The evaluation of the actual dynamic performance of the GMPC and HVDC controls was done in Chapter 3. The results found in Chapter 3, are verified in this chapter through PSCAD simulations. For the simulations, the power system model illustrated in Fig. 1.2, developed in PSCAD Version 5.0 on section 4, was applied. On the Songo-Apollo HVDC scheme, one of the major contingencies are line faults. However, for the GMPC and HVDC controls performance evaluation, the difference between line faults and pole faults is insignificant. So in this section the HVDC line faults are looked at to evaluate the performance of the GMPC and propose mitigating measures.

The BC is the default split point at Songo and it plays a vital role in rotor angle stability and BB-I frequency control. Its role will be analysed in the following sections.

5.2. Permanent Faults on the HVDC Lines

In Fig. 5.1, the three-phase AC Songo BB-I voltages and rectifier Pole 1 DC voltage after a permanent fault on HVDC Line 1 are shown.

Immediately after Pole 1 tripping, the BC also trips due to excess energy flow owing to load rejection, following power imbalance on the Songo busses.

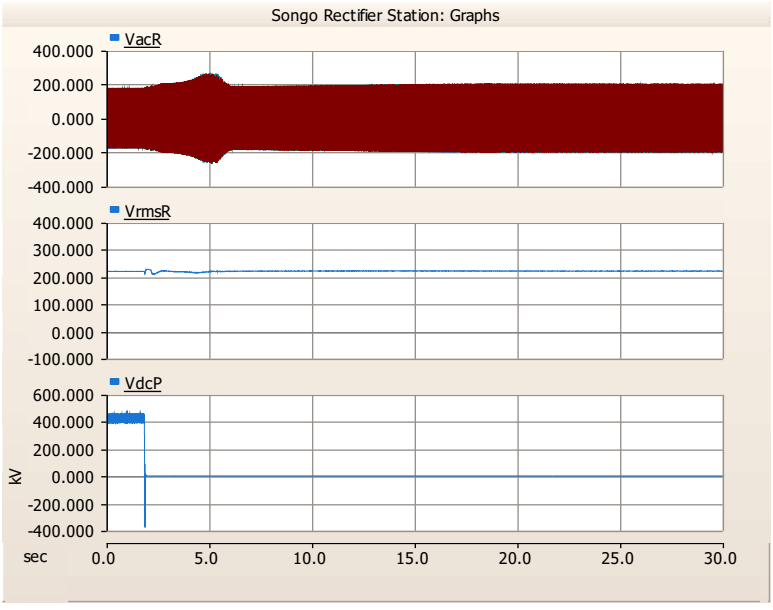


Fig. 5.1: Songo Converter Bus (BB-I) red phase voltage, Converter Bus RMS voltage and Pole 1 DC voltage, after Pole1 tripping simulation.

In Fig. 5.2, the BC active and reactive power flow, current and RMS voltage during the disturbance are shown. Prior to the disturbance, the active and reactive powers were flowing through the BC from BB-I to BB-II, i.e. in the positive direction. Immediately after Pole 1 tripping,

there is power surge flowing from the Converter Bus to the Non-Converter Bus. As a result, the power flow through the BC, immediately before the tripping, almost doubles, as illustrated in Fig. 5.2. This excess power flows to Songo-Bindura line since it is an active load, see Fig. 1.2.

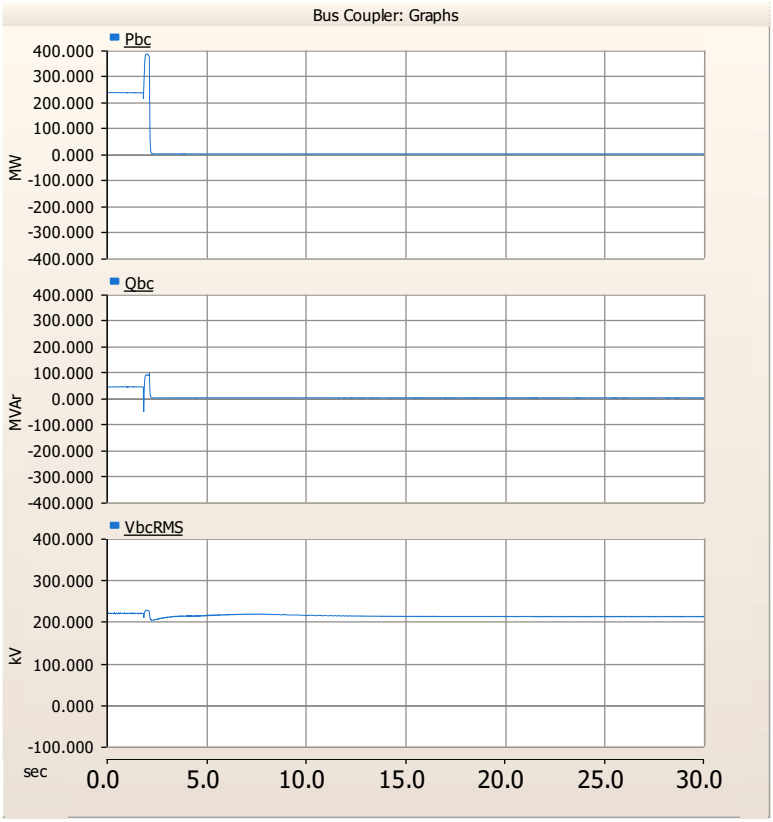


Fig. 5.2: BC active and reactive power and BC RMS voltage, after Pole 1 and the Bus Coupler tripping simulation.

The simulation results of a permanent fault on DC Line 1 are almost the same as the actual result for the same system configuration and loading prior to the fault. It reveals that the over-frequencies on Songo BB-I are normal and they cannot be avoided, but can be mitigated.

5.3. Transient (short duration) Faults on the HVDC Lines

a) Negative Power Flow through the BC (Two Generators on the Non-Converter Bus)

When the power flows through the BC from the Converter Bus (BB-I) to the Non-Converter Bus (BB-II), it is regarded as positive, and when it flows in the opposite direction, it is regarded as negative. In Fig. 5.3 the BC power flow, the BC reactive power and the BC rms voltage magnitude, during a transient fault in DC Line 1 are shown. Just before the transient fault, the active power flowing through the BC is from BB-II to BB-I, so it is negative (– 125 MW). The reactive power flow through the BC is positive (30 MVar) because it is flowing from BB-I to BB-II.

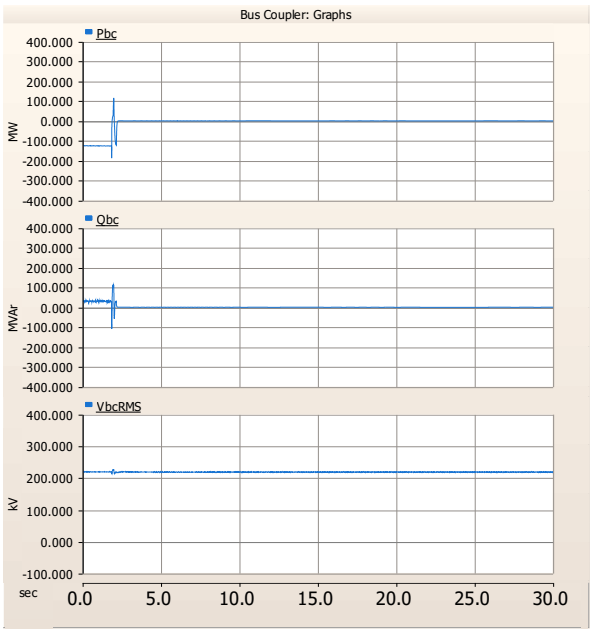


Fig. 5.3: BC active and reactive power and BC RMS voltage, after DC Line 1 transient fault simulation and the BC opens.

In Fig. 5.4 the active power of Pole 1, Pole 2 at Songo Rectifier Station after Line 1 transient fault that lasted for 95.24 ms are shown. The Pole 2 transient overload capacity was used, immediately after the fault.

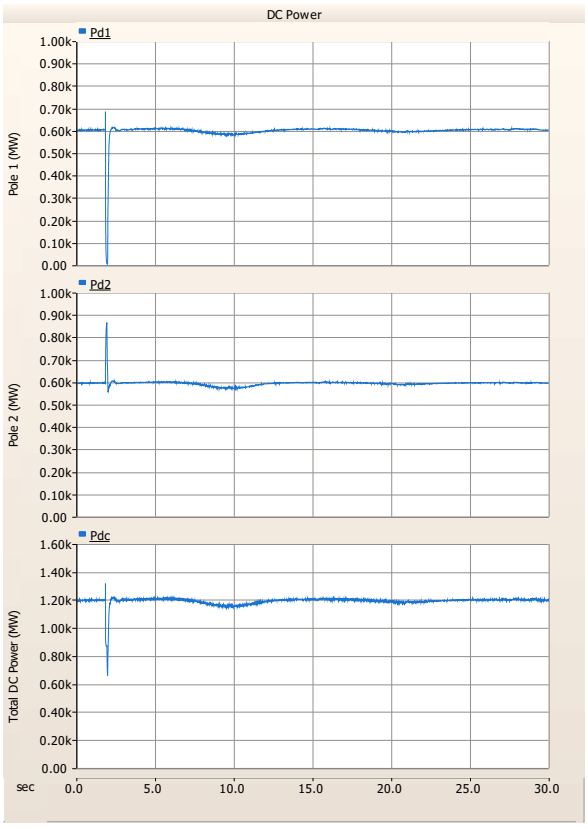


Fig. 5.4: Pole 1, Pole 2 and HVDC total active power, after DC Line 1 transient fault simulation.

This case of a transient fault on HVDC Line 1 is similar to the event described in Section 3.6. The pre-fault conditions were almost the same. The simulation result gives nearly the same frequency deviation on Songo BB-I as illustrated in Fig. 5.5.

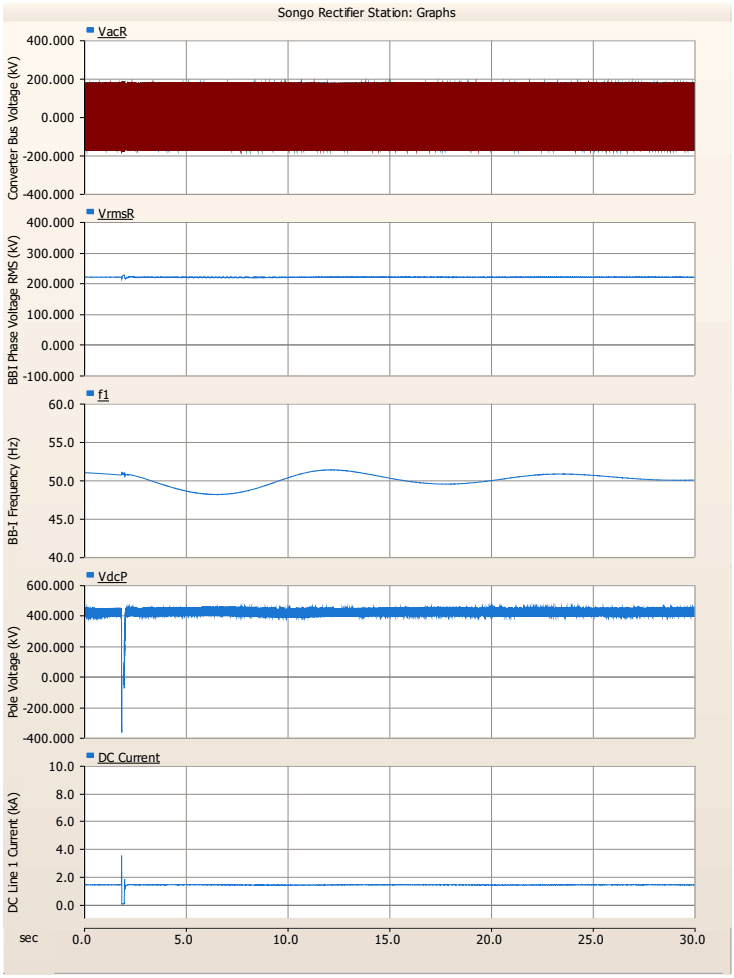


Fig. 5.5: Frequency deviation at BB-I, during transient fault simulation on DC Line 1.

The simulation results show that the GMPC/governor and HVDC controls perform well after transient faults in the DC Line 1. The frequency deviation in BB-I after the transient fault and BC tripping is not significant. However, the rotor angle stability study for this new configuration must be carried out.

b) Positive Power Flow through the BC

In this section, a typical transient fault on DC Line 1 is considered. The system configuration is the one represented in Fig. 1.2, where the BC power flow is positive. Four generators are connected to the Converter Bus and one generator is connected to the Non-Converter Bus. Power transmission from Songo to Apollo is 1200 MW, 600 MW in each pole.

In Fig. 5.6, the BC power flow, current and voltage prior to the transient fault in DC Line 1 and BC tripping are shown. Prior to the fault, the active power flowing through the BC is 235.5 MW and the reactive power flow is 42.5 MVar.

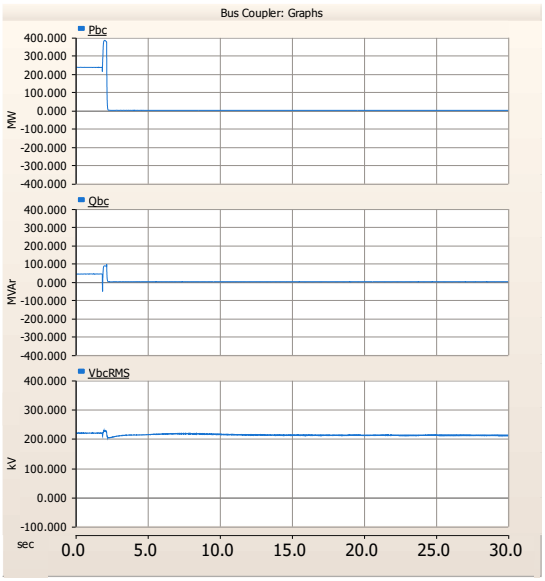


Fig. 5.6: BC active and reactive power and BC RMS voltage, after DC Line 1 transient fault simulation.

During the transient fault on HVDC Line 1, the Pole 2 transient overload capacity is used. But since it is limited to 125% it cannot take all load rejected, as illustrated in Fig. 5.7.

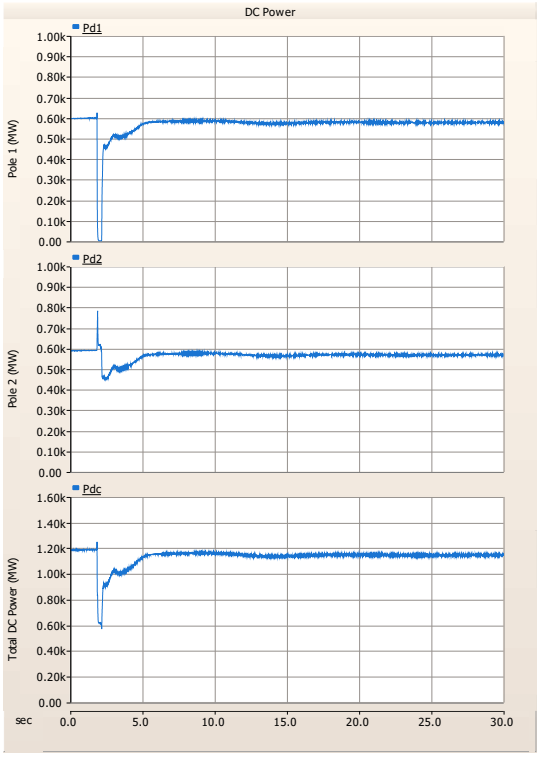


Fig. 5.7: Pole 1, Pole 2 and HVDC total active power during the transient fault simulation in DC Line 1.

At Songo Rectifier Station, the two busses are split after the BC tripping. In this case the BB-I changes to island operation (Frequency Control Mode) and the AC filters also trip due to over-frequency on BB-I. In Fig. 5.8, the frequency deviation on BB-I after the transient fault on DC Line 1 is shown.

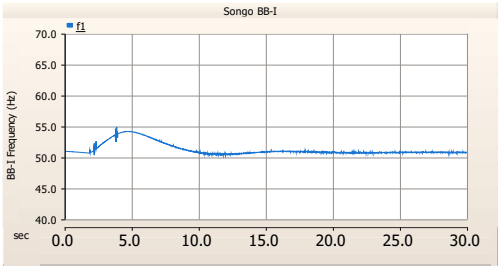


Fig. 5.8: Frequency at BB-I, during the transient fault simulation in DC Line 1.

After the transient fault on DC Line 1 and BC tripping, the frequency on BB-I reaches 54.145 Hz. The frequency on BB-I is high due to the HVDC load rejected during the transient fault and BC power rejected.

Comparing the cases in section 5.3 a) and section 5.3 b), it can be concluded that the BC power flow prior to the fault has a significant impact on the BB-I frequency deviation. The BB-I frequency deviation does not depend only on the amount of HVDC load rejected after the fault. It also depends on the amount and direction of active power flow through the BC. When the active power is flowing from BB-I to BB-II (positive power), the BC tripping increases the amount of accelerating power in BB-I. In this way, the accelerating power increases after an HVDC load rejection, exacerbating over-frequency in BB-I. Therefore, to reduce frequency deviation in BB-I following HVDC load rejection, negative BC power flow operation is recommended. However, rotor angle stability studies for two generator operation on the Non-Converter Bus (BB-II) must be conducted and overloading of Songo-Bindura transmission line coupling transformer, must be looked at.

5.4. Summary of the PSCAD Simulation Results

Although the GMPC was not modelled, on frequency control mode, its aim is to bring the frequency back to 50 Hz on Converter Bus after an HVDC disturbance. In the simulated cases, the aim of the governors is the same, since the frequency dead band is zero. On full load conditions of the HVDC scheme, the 125% transient overload capacity of the healthy pole only lasts for 3 seconds, including ramping. This has a minor impact on frequency deviation for permanent line faults.

The results found in this section are not different from the results found on section 3. In fact, this section was also used to verify the results found in section 3. According to the simulations results, the over-frequencies on BB-I, in addition to many other factors, also significantly depend on the magnitude and direction of the BC power flow. The loads in the centre and in the north of Mozambique have significantly increased in recent years. As a result, the BC power flow from the Converter Bus to the Non-Converter Bus, has also increased. This exacerbates over-frequency on the Converter Bus, after BC tripping following an HVDC disturbance. Therefore, operation of the system with two generators on the Non-Converter Bus will significantly reduce frequency deviation on the Converter Bus (BB-I) after an HVDC disturbance. This configuration must be studied due to stability and overload of Songo-Bindura Line coupling transformer concerns.

Chapter 6. INTERACTION BETWEEN HVDC CONTROLS, GMPC AND GENERATOR EXCITERS

6.1. Introduction

The system model developed in Chapter 4 was used to investigate the interaction between HVDC controls, GMPC/governor, generator exciters and AVRs during over-frequency events. A transient fault on HVDC Line 1 was simulated to see the impact of over-frequency on the Converter Bus voltage with and without the AC filters tripping. The Automatic Voltage Regulator (AVR) and excitation response were analysed for over-frequency events with and without the AC filters tripping and the results are illustrated and explained below.

6.2. Over-frequency Event Without AC Filters Tripping

In Fig. 6.1, the Converter Bus voltage waveform, during an over-frequency event, without the AC filters tripping is shown, following a transient fault on HVDC Line 1. In this PSCAD case, the over-frequency trip signal was deactivated. So there was over-frequency on the Converter Bus (BB-I), but the AC filters did not trip.

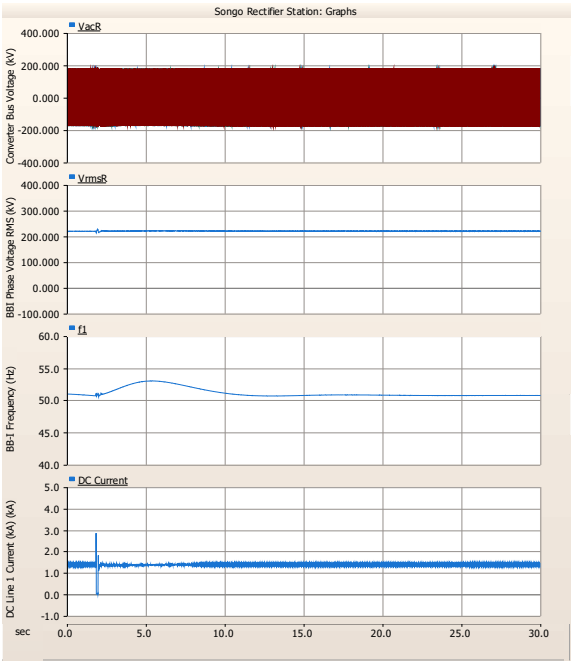


Fig. 6.1: Voltage on the Converter Bus, DC current and frequency without the AC filters tripping, during the over-frequency event following a transient fault on HVDC Line 1.

According to the simulation results, represented in Fig. 6.1, there is no overvoltage on the Converter Bus during the over-frequency event, when the AC filters remain in operation. Although the frequency changes, the Converter Bus voltage amplitude remains almost constant.

In Fig. 6.2, the AVR and excitation response of the generator connected to the Converter Bus, in the PSCAD case described above, is shown. The AVR and excitation system react to the generator speed disturbance and manage to keep the generator RMS voltage magnitude almost constant.

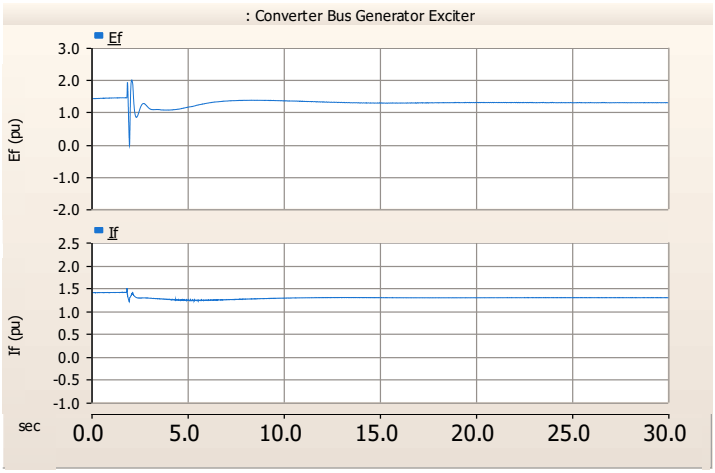


Fig. 6.2: Generator AVR and excitation response during the over-frequency event, following a transient fault on DC Line 1.

Although the generator speed increases, the RMS voltage magnitude is nearly constant and equal to the rated value of 16 kV. This voltage is measured at the generator terminals, before the step-up transformer. Consequently, the Converter Bus voltage amplitude also remains constant during the disturbance.

6.3. AC Filters Tripping Following an Over-Frequency Event

This PSCAD case is similar to the case of Section 6.2, the only difference being the AC filters tripping. In the Fig. 6.3, the Converter Bus voltage following a transient fault on HVDC Line 1 is shown, with the AC filters tripping due to over-frequency. In this figure, it can also be seen the impact of the AC filters tripping on the Converter Bus and Pole 1 voltages.

After the AC filters tripping, the Converter Bus voltage amplitude increases permanently and does not reduce. This voltage contains harmonics and it only reduces after the reconnection of the AC filters.

While in Fig. 6.1 the Converter Bus voltage amplitude did not increase during the transient fault on the DC Line 1, in Fig. 6.3, the Converter Bus voltage magnitude increases immediately after the AC filters trip. This Converter Bus voltage amplitude increase is due to harmonic peaks as illustrated in Fig. 6.3. The sudden reduction of 420 MVar in the system that were being supplied by the AC filters is compensated by an increase on the reactive power generated by the generators.

Fig. 6.4 represents one Converter Bus generator response to the same simulated transient fault on the DC Line 1, for the same PSCAD case. The AC filters trip due to over-frequency after the load rejection. The RMS generator voltage is measured before the step-up transformer.

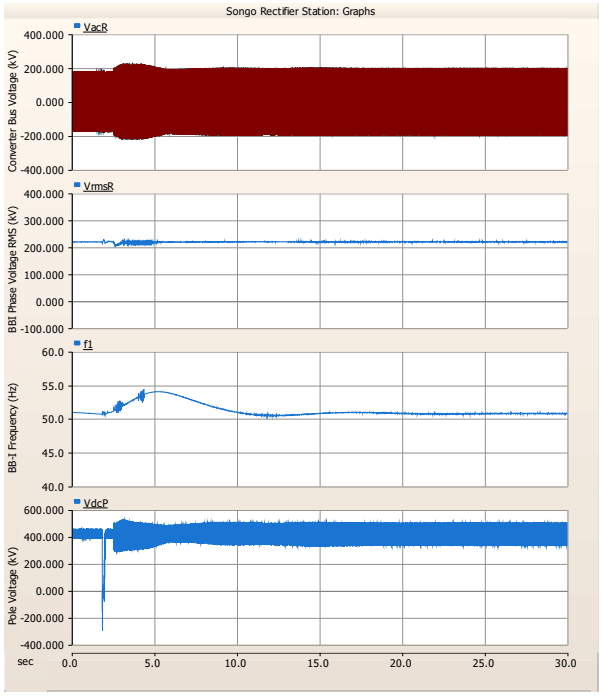


Fig. 6.3: Converter Bus voltage, DC voltage and Converter Bus frequency during an over-frequency event simulation.

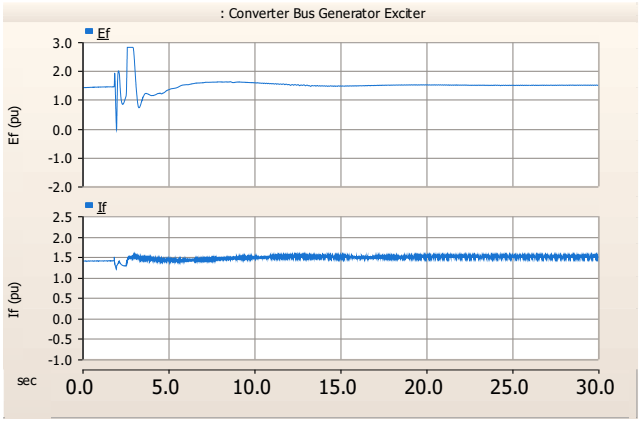


Fig. 6.4: AVR and excitation response during the transient DC Line 1 fault simulation.

Although the amplitude of the voltage in the Converter Bus increases due to harmonic peaks, the RMS voltage magnitude at the generators terminals remains constant. Therefore, after the AC filters trip, the generators exciters must reduce the reference voltage to avoid over-voltages in the Converter Bus. This is done by the GMPC.

According to the simulations, transient and permanent faults on the HVDC lines do not cause over-voltages on the Converter Bus. What causes peak voltages in the Converter Bus are the AC filters tripping due to the harmonic voltage peaks.

Fig. 6.5 shows the impact of the AC filters tripping on the Converter Bus voltage waveform and Songo-Bindura Line voltage waveform. The waveforms were recorded by the TFR installed at Songo. The AC filters tripped due to over-frequency on the Converter Bus.

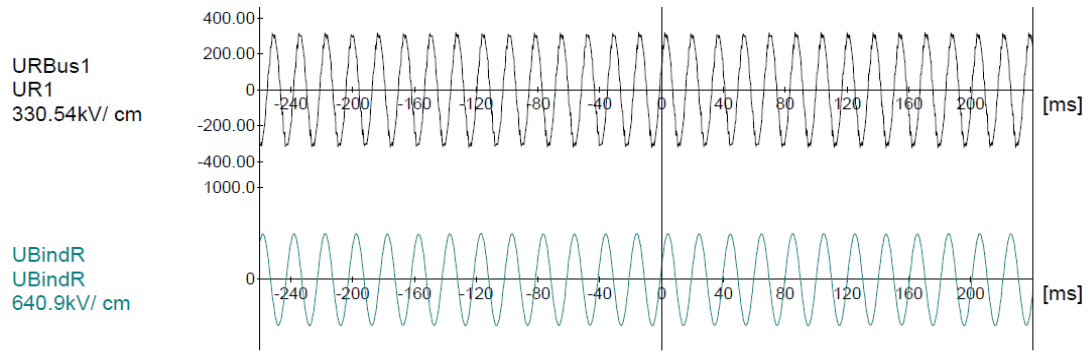


Fig. 6.5: Converter Bus (Bus1) and Songo-Bindura Line red phase voltage at Songo after the tripping of the AC filters.

In Fig. 6.5, it can be seen that the voltage at R phase in the Converter Bus is not purely sinusoidal, it contains harmonics. While the voltage on the same phase in the Songo-Bindura Line at Songo side is purely sinusoidal, it does not contain harmonics. It can also be seen that the 220 kV BC is open once the two waveforms are not in phase. Therefore, the AC filters tripping does not affect the Non-Converter Bus.

6.4. Impact of the AC Filters Tripping on the Converter Bus Voltage Waveform

6.4.1. Introduction

At Songo Rectifier Station, the AC filter circuits shunt the AC harmonic currents generated by the converter bridges. The first task of the AC filters is to prevent the distortion of the fundamental voltage waveform of the AC system. Therefore, they are connected to the bus where the converter bridges are connected. The AC filters are usually designed for minimum residual RMS values of the harmonics.

The AC filters at Songo are tuned for 50 Hz fundamental frequency operation because it is the operating frequency on the Converter Bus and SAPP in general.

Since the AC filter circuits are tuned just at the harmonic frequencies, at the fundamental frequency (50Hz) the AC filters generate capacitive reactive power. So their second function is to supply the inductive reactive power needed by the bridges during conversion (reactive power balance).

The AC filters installed at Songo have frequency protection. During frequency disturbances, they are instantaneously tripped when the frequency deviation is ±1.1 Hz (all the filter branches in service) or when the frequency deviation is ± 0.8 Hz (at least one filter branch out of service). They are also tripped when the frequency deviation is ± 0.5 Hz after a time delay of 20 s (all the filter branches in service) or when the frequency deviation is ± 0.3 Hz after a time delay of 20 s (at least one filter branch out of service). The impact of the AC filters tripping on the Converter Bus voltage profile will be analysed in section 6.4.3.

6.4.2. Single Tuned Harmonic Filters and Reactive Power Supply

There are two AC filter banks at Songo. Each AC filter bank consists of single tuned filter branches for the 5th, 7th, 11th, 13th harmonic currents and one damped filter branch for higher order harmonic currents. For instance, the 5th harmonic filter branch is a series LRC filter tuned at f0 = 250 Hz (resonance frequency) for a power system with a fundamental frequency of 50 Hz. At the resonance frequency (fo), the 5th harmonic voltage across the capacitor bank and 5th harmonic voltage across the inductor are equal and opposite polarity. So the tuned filter branch presents its lowest impedance equal to resistance R for the harmonic current, when accurately tuned (series resonance). The lower the value of R (higher quality factor Q) the better. In practical single tuned filters, RLC elements in series, the resistance cannot be seen since it is typically just the resistance of the inductor. The resistance can only be seen on the damped filters (high-pass filters) which bypasses the inductor at high frequencies.

The PSCAD model used for all simulations was developed based on the Songo actual parameters. The 5th harmonic series capacitance is 3.4 µF while the series inductance is 119 mH and the series resistance is zero. Fig. 6.6 shows the 5th harmonic filter branch, including the harmonic current. The 5th harmonic resistance is not represented because it is almost zero. For these parameter values, the 5th harmonic inductive reactance $X_{L(5)}$ is:

$$X_{L(5)} = \omega_{(5)}L = 5 \times 2\pi f_{(1)}L = 5 \times 2\pi \times 50 \times 119 \times 10^{-3} = 187\ \Omega \qquad (6.1)$$

The 5th harmonic capacitive reactance $X_{C(5)}$ is:

$$X_{C(5)} = \frac{1}{\omega_{(5)}C} = \frac{1}{5\times 2\pi f_{(1)}C} = \frac{1}{5\times 2\pi\times 50\times 3.4\times 10^{-6}} = 187\ \Omega \qquad (6.2)$$

As can be seen, from equations (6.1) and (6.2), for the 5th harmonic frequency there is *series resonance*.

$$X_{L(5)} = X_{C(5)} = 187\Omega \qquad (6.3)$$

The converter bridges are harmonic current source on the AC side. It means their internal impedance is infinite and the harmonic currents they generate are independent of the AC-side impedance. For the 5th harmonic filter branch, passing, for example, 100 A (250 Hz) (RMS) (current source), as illustrated in Fig. 6.6., the voltage across the capacitor bank is

$$V_{C(5)} = I_{(5)} \times \left(-jX_{C(5)}\right) = 100 \times (-j187) = -j18.7\ kV \qquad (6.4)$$

While the 5th harmonic voltage across the inductor is

$$V_{L(5)} = I_{(5)} \times jX_{L(5)} = 100 \times j187 = j18.7\ kV \qquad (6.5)$$

From equations (6.4) and (6.5), it can be seen that the 250 Hz harmonic voltages across the capacitor bank and across the inductor, have the same magnitude, but opposite polarity.

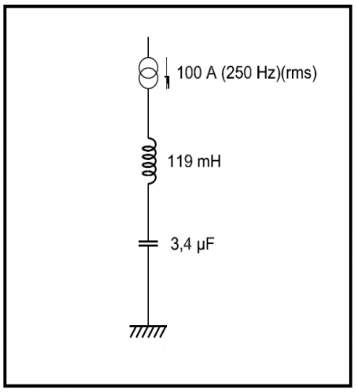


Fig. 6.6: The 5th harmonic single tuned filter branch, including the 5th harmonic current.

The 5th harmonic branch impedance at 50 Hz (fundamental impedance), Z(1) can be calculated from the circuit represented in Fig. 6.7.

$$Z_{(1)} = J\left[X_{L(1)} - X_{C(1)}\right] = j\left[2\pi f_{(1)}L - \frac{1}{2\pi f_{(1)}C}\right]$$

$$Z_{(1)} = j\left[2\pi \times 50 \times 119 \times 10^{-3} - \frac{1}{2\pi \times 50 \times 3.4 \times 10^{-6}}\right] = -j898.821\ \Omega \qquad (6.6)$$

From equation (6.6), it can be seen that the 50 Hz impedance is capacitive.

The 50 Hz current $I_{(1)}$ (fundamental current) for the 5th harmonic filter branch can also be calculated from the circuit represented in Fig. 6.7.

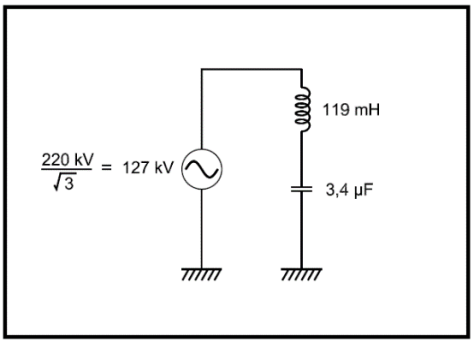


Fig. 6.7: 50 Hz current through the 5th harmonic filter branch.

$$I_{(1)} = \frac{V_{(1)}}{Z_{(1)}} = \frac{127 \times 10^3}{-j898.821} = j141.296\ A \qquad (6.7)$$

The 5th harmonic branch fundamental current leads the 5th harmonic branch fundamental voltage by 90°, because the fundamental impedance is purely capacitive.

The 50 Hz voltage across the capacitor bank is

$$V_{C(1)} = I_{(1)} \times \left[-JX_{C(1)}\right] = I_{(1)} \times \left[-J\frac{1}{2\pi \times f_{(1)} \times C}\right]$$

$$V_{C(1)} = j141.296 \times \left[-j\frac{1}{2\pi \times 50 \times 3.4 \times 10^{-6}}\right] = 132.282\ kV \qquad (6.8)$$

The 50 Hz voltage across the inductor is

$$V_{L(1)} = I_{(1)} \times JX_{L(1)} = I_{(1)} \times J2 \times \pi \times f_{(1)} \times L$$

$$V_{L(1)} = j141.296 \times j2 \times \pi \times 50 \times 119 \times 10^{-3} = -5.282\ kV \quad (6.9)$$

In Fig. 6.8, PSCAD simulated R phase voltages and current for the 5th harmonic filter branch are represented for steady-state operation. The Converter Bus frequency is almost constant and equal to 50 Hz. As can be seen, the voltages and current waveforms are periodic, but not sinusoidal. Therefore, they contain harmonics. Fourier Analysis of these waveforms can give their harmonic components. The predominant harmonics are the fundamental component (or 1st harmonic) and the 5th harmonic. In practice, for the 5th harmonic filter, besides the 1st and the 5th harmonics there are also other harmonic voltages, but their magnitudes are small, almost zero.

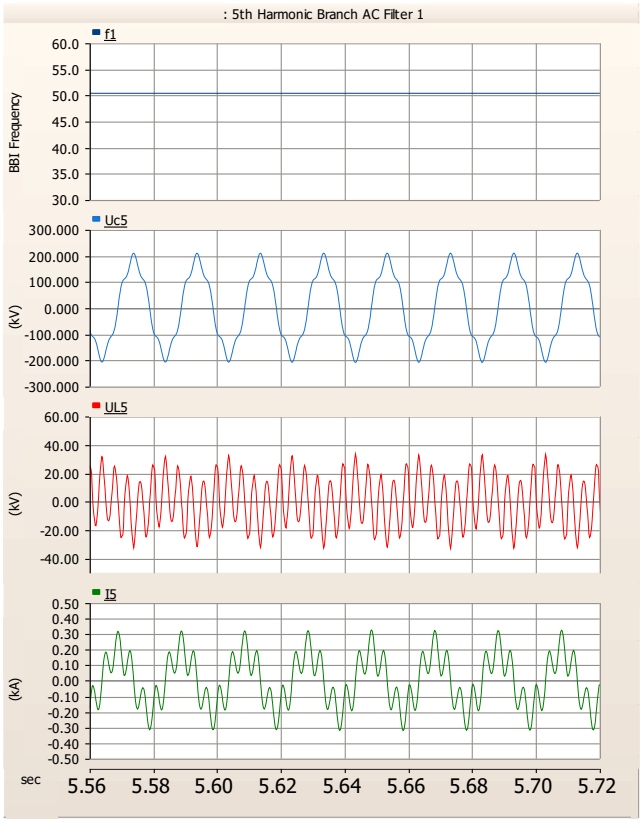


Fig. 6.8: AC Filter 1, 5th harmonic branch – Frequency in the Converter Bus (f1), R phase voltage across the capacitor (Uc5), R phase voltage across the reactor (UL5) and the R phase current (I5) for steady-state operation.

According to Fig. 6.8, the voltage across the capacitor terminals is much larger than the voltage across the reactor terminals. This is because the voltage across the capacitor terminals has two main components, the fundamental component and the 5th harmonic component, as illustrated in Fig. 6.9. The fundamental component of the capacitor voltage is much larger than the 5th harmonic component. This is also demonstrated through calculations, by equation (6.4) and equation (6.8). It can also be easily seen by Fourier analysis in Fig. 6.9. In the figure is represented harmonic order versus harmonic voltage in kV, peak values.

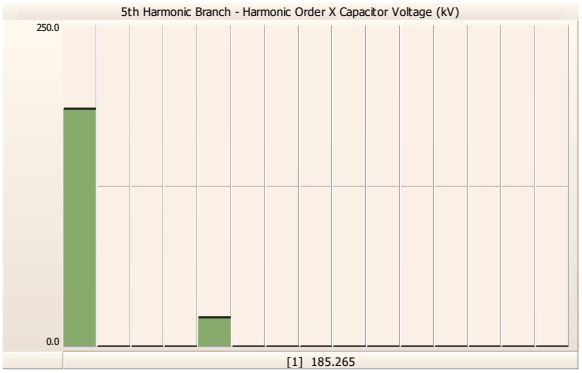


Fig. 6.9: Fourier analysis of the voltage across the 5th harmonic filter capacitor bank, for steady-state operation.

Therefore, it can be concluded that for a single tuned filter branch, the capacitor bank is subjected to voltage components of mainly two frequencies: the fundamental frequency and the harmonic frequency for which the filter is tuned. The fundamental voltage harmonic component is much greater than the harmonic frequency component for which the filter is tuned.

The voltage magnitude across the reactor terminals has mainly the 5th harmonic component, according to Fig. 6.10, since the fundamental component is small. This is also demonstrated through calculations, by equation (6.5) and equation (6.9). In equation (6.5), the 5th harmonic inductor voltage is 18.7 kV, while the 50 Hz inductor voltage is 5.282 kV.

Comparing Fig. 6.9 and Fig. 6.10, it can be seen that the 5th harmonic voltage across the capacitor bank and the 5th harmonic voltage across the inductor are almost the same, although they have opposite polarity. Equation (6.4) and Equation (6.5) demonstrate this statement. The AC filters are capacitive for the fundamental frequency and generate the reactive power needed by the converter bridges. This is demonstrated by equation (6.6) and Fig. 6.8 and Fig. 6.9. The same conclusion can be extended to other harmonic filter branches. In the Fig. 6.10 is represented the harmonic order versus harmonic voltage in kV, peak values, across the 5th harmonic branch inductor.

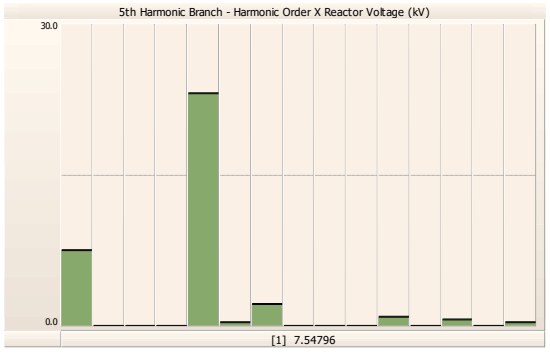


Fig. 6.10: Fourier analysis of the voltage applied to the reactor of the 5th harmonic branch, for steady-state operation.

The inductive reactance and capacitive reactance depend on the frequency. For instance, the 5th harmonic frequency ($f_{(5)}$) of the 5th harmonic current generated by the converter bridges also

depends on the actual value of the fundamental frequency ($f_{(1)}$) on the Converter Bus, as shown by equation (6.10).

$$f_{(5)} = 5f_{(1)} \tag{6.10}$$

However, the 5th harmonic filter is sharply tuned for 250 Hz.

Therefore, in the 5th harmonic filter branch, when the fundamental frequency on the Converter Bus increases the inductive reactance increases both for the fundamental and 5th harmonic frequencies, because it is directly proportional to the frequency. The capacitive reactance decreases both for the fundamental and the 5th harmonic frequencies, because it is inversely proportional to the frequency.

In contrast, in the 5th harmonic filter branch, when the fundamental frequency on Converter Bus decreases, the inductive reactance also decreases both for the fundamental and 5th harmonic frequencies, because it is directly proportional to the frequency. The capacitive reactance increases both for the fundamental and the 5th harmonic frequencies, because it is inversely proportional to the frequency.

The analysis above for the 5th harmonic filter can be extended to the other single tuned filter branches and it is for steady-state operation of the tuned filters.

According to the explanation above, the harmonic filters are sharply tuned for the resonant frequency and when there is significant fundamental frequency deviation on the Converter Bus, they are de-tuned. When they are detuned, the Converter Bus voltage waveform gets distorted.

As a result, during over-frequencies, the AC filters are tripped because they are sharply tuned, no longer provide significant harmonic filtering but they provide unwanted fundamental frequency capacitive reactive power.

6.4.3. AC Filters Tripping and the Converter Bus Voltage Waveform

The system model developed in Chapter 4 was used to investigate the impact of AC filters tripping on the 220 kV Converter Bus voltage waveform.

An HVDC disturbance may cause load rejection on the Converter Bus. When the excess energy threshold is reached, the BC trips before the tripping of the AC filters. In this way, the hazardous harmonic currents are shunted before they reach the Non-Converter Bus, where the AC loads are connected. Therefore, the tripping of the AC filters has no impact on the Non-Converter Bus voltage waveform.

In Fig. 6.11, the Converter Bus voltage and Pole 1 DC voltage before (during the fault the DC voltage is zero) and after the AC filters tripping are shown (the over-frequency and AC filter tripping occurs during the fault and hence the harmonics on the Converter Bus voltage waveform appear after 3.03 s).

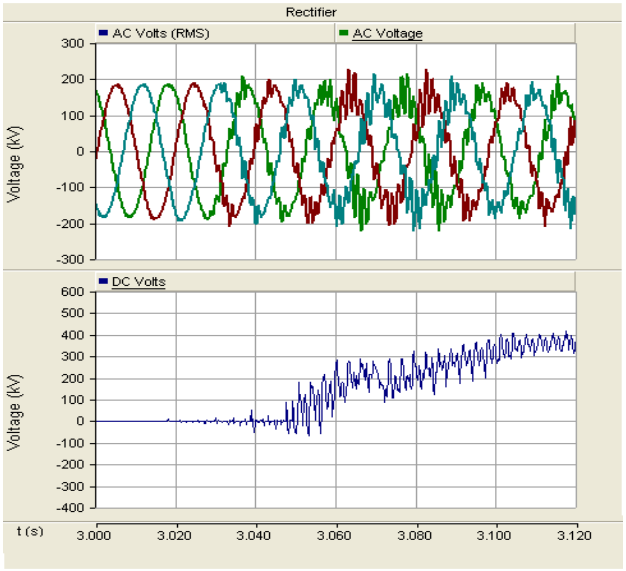


Fig. 6.11: Converter Bus voltage and Pole 1 DC voltage before and after the AC Filters tripping, during a transient fault in DC Line1.

As illustrated in 6.11, the Converter Bus voltage waveform before and after the AC filters trip is different. The current harmonics generated by the bridges have a negative impact on the Converter Bus voltage waveform. It can also be seen that, after the AC filters tripping, the 220 kV three-phase AC voltage waveform contains harmonics. The PSCAD Fast Fourier Transform (FFT) block illustrates that the predominant harmonics of this distorted voltage waveform are the fundamental component, 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} as shown on Fig. 6.12. So the main role of the AC filters for the bus voltage is to eliminate these harmonics on the Converter Bus voltage waveform during the operation of the HVDC bridges.

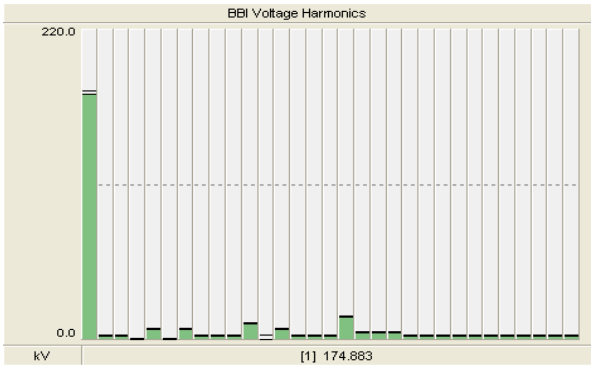


Fig. 6.12: Harmonic order versus R-Phase Converter Bus voltage (kV), peak values, after the AC filters tripping.

The AC filters tripping has a negative impact only on the Converter Bus voltage waveform. Therefore, all the AC transmission lines are connected to the Non-Converter Bus. See the system configuration in Fig. 1.2.

Fig. 6.13 shows the negative impact of the AC filters tripping on the Pole 1 DC voltage waveform, after a transient fault on Line 1. The DC voltage waveform represented is measured on the pole side of the fault. The DC voltage ripple after the AC filters trip is higher. The same also happens to the Pole 2 DC voltage waveform.

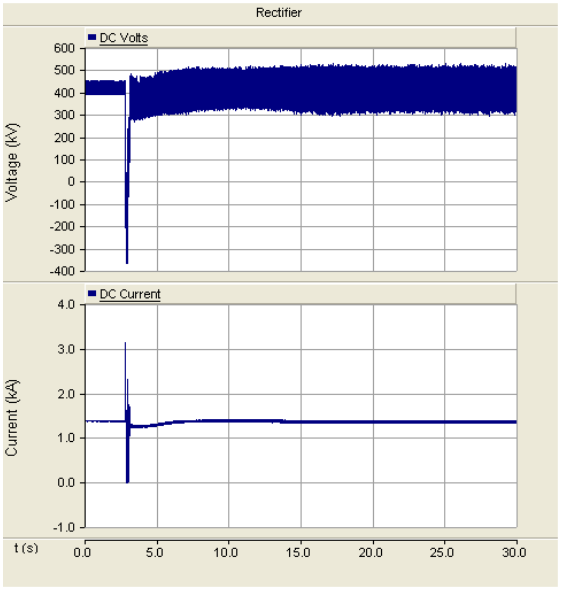


Fig. 6.13: Pole 1 DC voltage and DC current before and after the AC filters tripping.

The AC-side voltage peaks due to harmonics may cause conduction of the valve surge arresters and consequent tripping of the converter bridges by the differential protection. Therefore, counter-measures such as lowering converter transformers tap-changers are taken by the valve controls immediately after the tripping of the AC filters.

The tripping of the AC filters has also a negative impact on the currents of the generators connected to the Converter Bus, as illustrated in Fig. 6.14. The generator currents contain harmonics. The generators connected to the Non-Converter Bus (BB-II) are not affected by the AC filters tripping, because the BC trips before the AC filters are tripped.

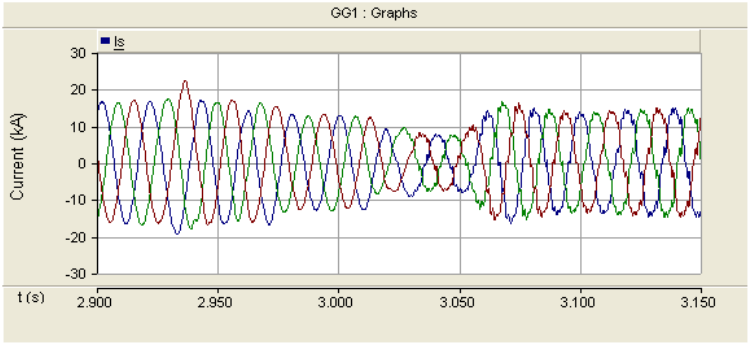


Fig. 6.14: Converter Bus Generators current, after the AC filters trip.

The tripping of the AC filters at Songo has no impact on the Apollo DC voltage, according to the PSCAD simulations.

Although the generators were designed to withstand the current harmonics generated by the Songo Rectifier Station, the harmonic currents may reduce the stator winding insulation lifetime. So the tripping of the AC filters must be avoided.

Chapter 7. MEASURES TO MITIGATE OVERFREQUENCIES ON THE CONVERTER BUS

7.1. Insertion of Braking Resistors

It has been seen that over-frequencies on the Converter Bus are mainly caused by the accelerating power following an HVDC load rejection. If there is a way of replacing this HVDC load rejected, the accelerating power can be considerably reduced and there can no longer be BC tripping nor over-frequency on the Converter Bus. One way of replacing this rejected load is through the installation of braking resistors (BRs) at Songo. Whenever HVDC load is rejected, the BRs can be immediately connected to replace this rejected HVDC load. In addition to this measure, the control of voltage angle difference between Songo and Apollo, by BR and DC power modulation is crucial for rotor angle stability.

In the power system shown in Fig. 1.2, the BRs can be connected to the Converter Bus to replace the rejected HVDC load. In the Songo-Apollo HVDC scheme, the worst load rejection scenario considered is a single pole tripping. HVDC station tripping was not considered since it is not a common event at Songo. Although the rated pole power is 960 MW, literature [10] proposes the installation of 720 MW BRs due to the 1 second 125% transient overload capacity of the healthy pole and the generators ramp rate. However, 720 MW BRs for only 1 second transient overload capacity may not be enough to prevent BC tripping due to excess energy flow through the BC due to the power imbalance. The rapid insertion of the BRs is critical to prevent both over-frequency on the Converter Bus and the first swing instability, caused by insufficient synchronizing torque.

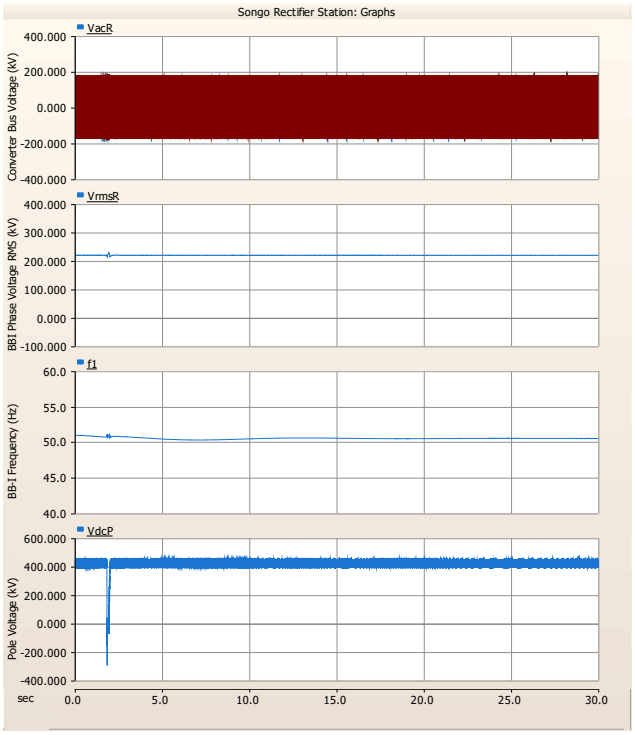


Fig. 7.1: Converter Bus phase voltage, Converter Bus RMS line voltage, Converter Bus frequency deviation and Pole 1 DC voltage, after a transient fault simulation in DC Line 1 and insertion of BRs.

Fig. 7.1 illustrates the frequency deviation on the Converter Bus, after the simulation of a transient fault on DC Line 1.

The transient fault on DC Line 1 lasted for 158.73 ms. The BRs were immediately inserted after the inception of the fault. The resistance of the BRs inserted was equal to the rejected HVDC load rejected 600 MW. The frequency deviation on the Converter Bus was insignificant so that the sharply tuned AC filters did not trip.

In Fig. 7.2 is represented the harmonic order versus the harmonic components of the DC Line 1 voltage. The DC component is 400 kV (DC) and the harmonic voltage components are less than 10 kV.

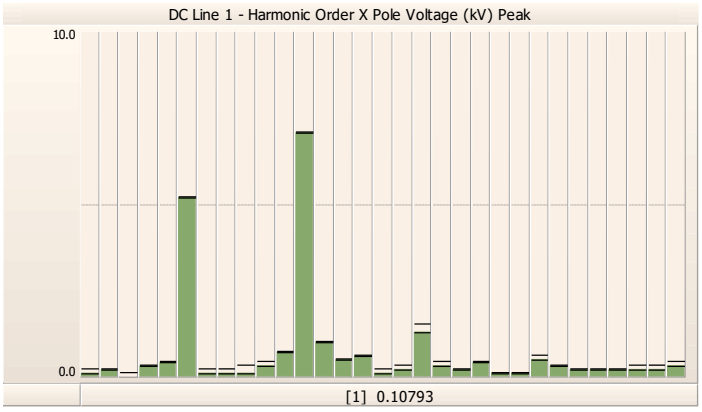


Fig. 7.2: Line 1 DC voltage harmonic components, after a transient fault simulation in DC Line 1 and insertion of BRs.

According to Fig. 7.2, the DC line voltage contains mostly the 6^{th} and 12^{th} harmonics, besides the DC voltage component, which is about 400 kV. The 6^{th} harmonic component is 5.16 kV (peak), the 12^{th} harmonic component is 7.15 kV (peak), the 18^{th} harmonic component is 1.2 kV (peak) and the rest of harmonic components are less than 1.0 kV. These values were obtained during the DC filters operation and converter bridges configuration of 6 and 12 pulses.

Fig. 7.3 shows the frequency deviation on the Converter Bus, after a simulation of a permanent fault on Pole 1, just before the smoothing inductor. In this case, the BRs were not inserted.

As can be seen in this case, the BC trips due to an excessive energy flow through it (energy imbalance greater than 110 MJ). The Converter Bus changes into island operation mode and the over-frequency reaches 59 Hz on the Converter Bus.

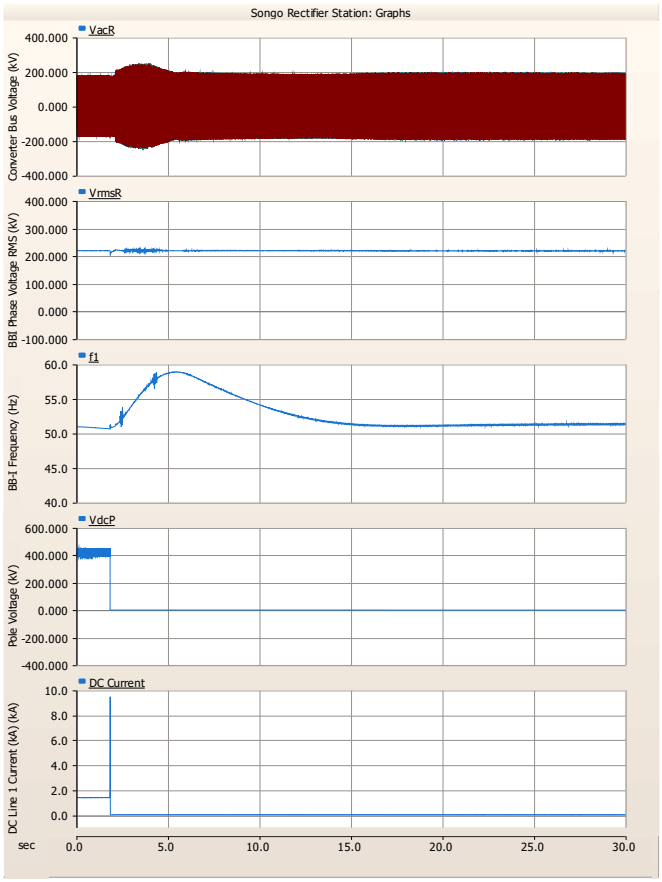


Fig. 7.3: Frequency deviation in the Converter Bus, after a permanent fault simulation in Pole 1, without insertion of BRs.

Fig. 7.4 illustrates the same case, as the case in Fig. 7.3, the only difference being the insertion of the BRs. In this case, the insertion of the BRs prevents the BC and the AC filters tripping. As can be seen, there is almost no frequency deviation at all. The frequency deviation on the Converter Bus is significantly reduced by the insertion of the BRs. They were inserted immediately after the inception of the fault. The active power of the BRs inserted is equal to the HVDC power rejected which is, in this case 600 MW.

From the PSCAD cases described above, it can be seen that the BRs can be effective in preventing over-frequencies on the Converter Bus and rotor angle instability. The BRs may also prevent the BC tripping, if the telecommunications between the Songo Rectifier Station and Apollo Inverter station are operating. The rapid insertion of the BRs is also crucial for over-frequency prevention. They cannot be inserted using circuit breakers since the operating time of the circuit breakers is too slow (more than 40 ms). Thyristor controlled BRs can be effective due to their rapid insertion.

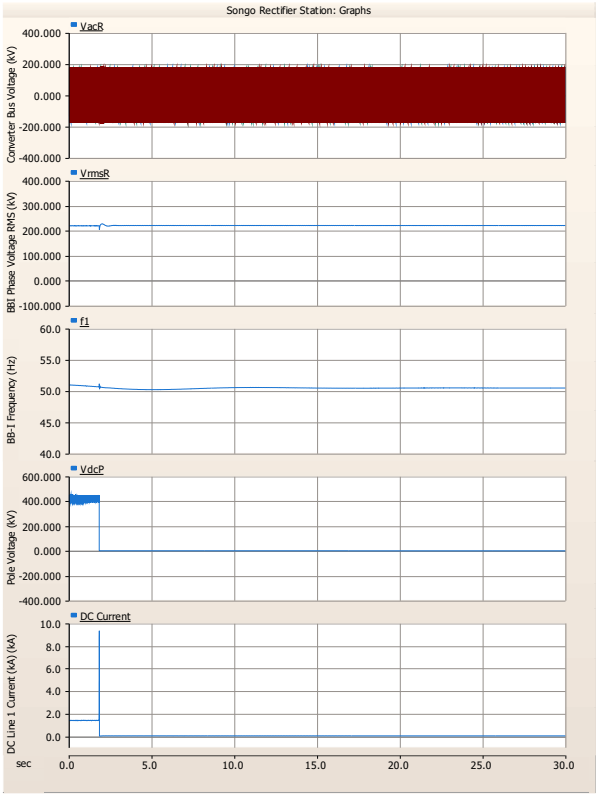


Fig. 7.4: Frequency deviation in the Converter Bus, after a permanent fault in Pole 1 and immediate insertion of BRs.

The simulation results show that the installation of braking resistors (BRs) can significantly reduce frequency fluctuations on the Converter Bus and improve rotor angle stability at Songo. The rapid insertion of the BRs and telecommunications between the Songo Rectifier Station and Apollo Inverter Stations are important for frequency control and split point tripping prevention respectively.

7.2. Two Generators Connected to the Non-Converter Bus (BC Negative Power Flow)

As seen in Section 5.3, the amount and direction of active power flow through the BC prior to the HVDC line fault has a significant impact on the Converter Bus frequency deviation. So to reduce over-frequencies in the Converter Bus, two generators connected to the Non-Converter Bus should be studied to see its impact on the system stability. With two generators connected to the Non-Converter Bus, the BC power flow is negative and over-frequencies in the Converter Bus are mitigated. This is because the BC tripping causes a power deficit in the Converter Bus, that minimizes the frequency deviation after excess energy caused by HVDC load rejection. In the opposite situation, when the BC power flow is positive, the BC tripping is load rejection on the Converter Bus. This exacerbates over-frequency in the Converter Bus after an HVDC load rejection.

Although two generators connected to the Non-Converter Bus minimizes over-frequencies on the Converter Bus after an HVDC load rejection, it may cause instability in the interconnected

system and overload of Songo-Bindura coupling transformer, after the BC tripping. So this configuration is not at all recommended before extensive and detailed studies.

With one generator in operation in the Non-Converter Bus, it is also possible to have negative power flow through the BC, and mitigate over-frequencies in the Converter Bus caused by HVDC load rejection. To realize this, the load on the Non-Converter Bus must be reduced in order to have the remaining power from the generator connected to the Non-Converter Bus to flow from the Non-Converter Bus to the Converter Bus. Whenever possible, BC power flow from the Converter Bus to the Non-Converter Bus must be minimized.

7.3. Use of Transient Overload Capacity of the Faulty HVDC Line

In the Songo-Apollo HVDC scheme, most of the DC transmission line faults are transient. After a transient fault on one DC line, its overload capacity can be used to mitigate over-frequencies in the Converter Bus at Songo. The transient overload capacity corresponds to a DC current of 2250 A, while the DC voltage remains constant. Therefore, after a transient DC line fault, even when the restart occurs at a lower voltage level, the transient overload capacity of the line can be used. In this way, the accelerating power on the Converter Bus can be significantly reduced and frequency deviation from 50 Hz mitigated.

7.4. Increase of Transient and Steady State Overload Capacity of the HVDC Scheme

Another way of preventing over-frequencies on the Converter Bus caused by HVDC load rejections is to increase both the transient and the steady-state overload capacity of the HVDC scheme. In this way, power imbalance after contingencies can be significantly reduced, and consequently over-frequencies on the Converter Bus. The implementation of this mitigating measure on the existing HVDC scheme can be challenging and costly. However, it can be easily implemented during the upgrade of the rectifier station.

The 1 second transient overload capacity of 125% is not enough to prevent over-frequencies caused by transient or permanent line faults. A study must be carried out to increase the actual transient overload capacity and duration since the Songo Rectifier Station will be refurbished. The HVDC transmission lines were initially designed for 3300 A steady-state operation. So the actual rating and the transient overload capacity of the DC lines, including the earth electrode must be accessed. The actual ratings of the smoothing reactors, DC filters, converter transformers, converter valves, AC filters, breakers, disconnects must also be assessed in the detailed study. The assessment of all this equipment must be carried out at Apollo Converter Station as well.

Chapter 8. CONCLUSIONS

8.1. Introduction

This section of the report presents the conclusions drawn from the study and discusses how the research questions were answered.

8.2. Conclusions from the Study

In recent years, the increased magnitude of frequency deviation from 50 Hz on the Converter Bus at Songo, is mainly due to the increase of power flow from the Converter Bus to the Non-Converter Bus. This increase is owing to the load increase on centre and north of Mozambique in recent years, see Fig. 1.2. Therefore, it was believed that the dynamic performance of the GMPC and HVDC controls had deteriorated in recent years.

However, the evaluation of the GMPC and HVDC controls through TFR data and PSCAD simulations shows that the performance of the GMPC and HVDC controls remain the same, since the GMPC commissioning in October 1999. What increased in recent years was the accelerating power on the Converter Bus, after an HVDC load rejection.

An alternative explanation for the need to trip the harmonic filters during over-frequency events is that because the filters are sharply tuned they no longer provide significant harmonic filtering but they provide unwanted capacitive reactive power at fundamental frequency.

The TFR data and PSCAD simulations illustrate that the GMPC, HVDC controls and generator exciters and AVRs interact as required during over-frequency events. It was demonstrated by over-frequency simulations on PSCAD/EMTDC Version 5.0.

8.3. Research Questions

The research questions proposed at the commencement of the study were addressed during the course of the study through TFR data analysis, AC filters harmonic impedance calculation and PSCAD simulations.

8.3.1. What is the Actual Behaviour of the GMPC and HVDC Controls During and After HVDC Load Rejection?

To address this question, the LCC HVDC system, the HVDC controls, the hydro generators speed load governor and the GMPC was studied. Generator rotational response following a small disturbance and generator loss of synchronism following large disturbance were also studied. On generator rotational response, the swing equation was studied to understand the relationship between load rejected and over-frequency.

The TFR data was analysed for bridge tripping, pole tripping, transient and permanent DC lines faults and station tripping to verify if the GMPC and HVDC controls behaviour was satisfactory. The analysis revealed that it was satisfactory, however in few cases the HVDC controls did not

perform that well. The TFR data also revealed that telecommunications play an important role on the system stability and frequency control.

8.3.2. Why is it Necessary to Trip the AC Filters During Over-Frequency Events and What is the Impact of the Trip on the Converter Bus Voltage?

During over-frequency events, the AC filters are tripped because they are sharply tuned, they no longer provide significant harmonic filtering but they provide unwanted capacitive reactive power at fundamental frequency.

The impact of AC filters tripping on the Converter Bus voltage waveform was clearly shown by PSCAD simulations. It can be seen on Fig. 6.3 and on Fig. 6.11. The AC filters tripping has also a negative impact on the DC voltage as illustrated on Fig. 6.3 and 6.13. There is a significant difference between the Converter Bus voltage waveform before and after the AC filters tripping. Before the AC filters tripping, the 220 kV three-phase Converter Bus voltage wave was sinusoidal, without visible distortions (meaningful harmonics). After the AC filters tripping, the Converter Bus three-phase voltage is distorted and no longer sinusoidal, but remains periodic. It means that the Converter Bus three-phase voltage contains harmonics. The most predominant harmonics on the Converter Bus voltage waveform are the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} according to PSCAD Fourier analysis of the three-phase distorted voltage. The Fourier analysis is shown on Fig. 6.12.

8.3.3. Do the GMPC, HVDC Controls, Generator Exciters and AVR Interact as Required During Over-Frequency Events?

To answer to this research question, the data recorded by the TFR installed at Songo and PSCAD simulations were carried out. According to the results, it can be concluded that the GMPC, HVDC controls and generator exciters and AVRs interact as required during over-frequency events. However, the AVRs voltage must be reduced during over-frequency events, after the AC filters tripping to avoid harmonic voltage peaks on the Converter Bus, as illustrated on Fig. 6.3 and Fig. 6.11.

8.4. Recommendations

To mitigate over-frequencies on the Converter Bus, the following recommendations were made:

1. Installation of braking resistors at Songo to absorb excess energy, after an HVDC load rejection.
2. Connection of two generators to the Non-Converter Bus, to minimize the BC power flow.
3. Use of the transient overload capacity of the faulty HVDC line, after a transient fault.
4. Increase of transient and steady state overload capacity of the entire HVDC scheme.

Section 7 of the report explains all the recommendations above. To implement each of the measures proposed above, further detailed studies are required.

There is an opportunity for Songo Rectifier Station in particular to implement some of the recommendations proposed, since there will be a refurbishment of the substation. An invitation for initial selection document submission, was issued by HCB on 18th August 2020 [15]. However, the last recommendation, must be implemented both at rectifier and inverter

stations. The HVDC transmission lines, must also be looked at to realize the last recommendation.

8.5. Suggestions for Further Research

Possible further research is:

1. Develop a detailed PSCAD model for parallel operation of the HVAC and HVDC scheme to study the GMPC Angle Control and possible operation without telecommunications.

2. Develop voltage phase angle control mode for parallel operation of the HVDC and HVAC systems between the rectifier and inverter stations in an environment with low reliable telecommunications between the stations. Most of the times, the rectifier station connected to remote generation cannot afford to keep the BC open when there are no telecommunications between the stations, because it leads to underutilization of some generating units.

3. Develop a control system at an LCC HVDC scheme, for current control at the Inverter Station during disturbances, when there are no telecommunications between the rectifier and inverter stations. It is assumed the rectifier controls the current on normal operating conditions.

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