Shunt Capacitor Bank Fundamentals and the Application of Differential Voltage Protection of Fuseless Single Star Earthed Shunt Capacitor Banks

Phillip William Baker-Duly

A research report submitted to the Faculty of Engineering and the Built Environment, of the University of the Witwatersrand, in partial fulfilment of the requirements for the degree of Master of Science in Engineering.

Johannesburg 2008

Abstract

The research investigates reactive power compensation and protection of shunt capacitor banks. The characteristics of capacitors including, formulae, design, manufacturing, and testing is presented. Capacitor units using extended foil solder type elements have losses as low as 0.1 watt/kVAr. Failure of capacitors generally occurs due to overvoltage stress. The type and aging properties of the dielectric determines the lifespan of the capacitor. Polypropylene film is commonly used as the dielectric. Basic capacitor bank design calculations are presented. A detailed discussion on the configurations and protection philosophies is described for single star earthed, single star H-bridge, double star, and C-type filter H-bridge capacitor banks. A novel approach to unbalance voltage detection and the protection of fuseless single star earthed shunt capacitor banks is investigated, engineered and tested. This methodology explores the potential evolution towards distributed protection. This involves two programmed multifunction protection relays communicating via the IEC 61850 Ethernet protocol. One relay receives voltage measurements from the high voltage busbar. The other relay receives voltage measurements from the low voltage capacitor tap point. The two relays share their measurements via the Ethernet link. The difference in measurements is used to initiate alarm and trip operations. The relay protection function satisfies criterion for reset-ability, selectivity, stability, accuracy, and loss of potential blocking. Spurious operation occurs when the Total Harmonic Distortion level is above 8%. The major short coming is the cyclic processing of the logic function. The algorithm processing duration is 396ms as opposed to an anticipated time of 60ms. This application has a competitive overall cost advantage. This is based on the number of components required, manufacturing and testing times, and onsite installation and commissioning works. It is recommended to further investigate the cyclic processing of the logic functions, as well as, to test the protection function on a power system simulator. Future prospects involve using the programmability and flexibility of the onboard relay PLC to count capacitor element failure, on a discrete basis, instead of detection and protection based on analogue threshold settings. This will mitigate ambiguous measurements and spurious operation.

Acknowledgements

I would like to thank Brendan Young for the origin of the research topic and his guidance. At the time he was the Manager of the Power Quality and Protection Department of Siemens Ltd. South Africa. Mr Vic Franzsen, Managing Director of the Westingcorp Power Capacitor factory in Centurion, South Africa, provided me with an informative factory tour on the design, manufacture and testing of power capacitors which contributed to the literature survey. During the laboratory phase of the project, Mr. Gary Oosthuizen, a Power Automation Specialist for Siemens Ltd. South Africa, gave invaluable technical support on the programming of the relay devices. And finally, Dr van Coller of the School of Electrical and Electronic Engineering, of The University of the Witwatersrand, who supervised and offered guidance to the conclusion of the project. Their contributions are gratefully acknowledged.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

ANSI	American National Standards Institute
CFC	Continuous Flow Chart
GOOSE	Generic Object Oriented Substation Event
IDMT	Inverse Definite Minimum Time
IEC	International Electrotechnical Commission
IED	Intelligent Electronic Device
IP	Internet Protocol
LCD	Liquid Crystal Display
LED	Light Emitting Diode
PCB	Polychlorinated Biphenyl
PLC	Programmable Logic Controller
THD	Total Harmonic Distortion
THDV	Total Harmonic Distortion Voltage
VT	Voltage Transformer

1 Introduction

This research paper explores the principles of reactive power compensation, particularly on the technology of shunt capacitor bank protection. The application of shunt capacitor banks from both a primary (main equipment and system layout) and secondary (control and protection) engineering perspective is investigated. The focus or the project problem of this research and laboratory work is to investigate and implement a novel approach to unbalance voltage protection of fuseless single star earthed shunt capacitor banks.

The behaviour of inductor and capacitor quantities and their typical applications within this context is demonstrated. A detailed analysis of the design, construction and testing of power capacitor units is described. This includes a discussion on their failure modes. Different bank configurations and the related protection methodologies are presented. The background literature survey defines the scope of work and provides the necessary general background to the research. The particular background information is used to facilitate the approach to solving the project problem. The researched material applies to compensation systems in general. Attention is focused on 88kV to 400kV, 36 to 150 MVAr shunt capacitor banks implemented in the Eskom Transmission System, South Africa.

Historically, protection functions have been implemented on and dedicated to a single device. Protection devices have evolved into Intelligent Electronic Devices (IED), and comprise of high-speed on-board computers. Today's relays have the functionality available for the user to implement customized Programmable Logic Control (PLC) for interlocking, measurement and protection applications. The research emphasises distributed protection. This implies a move from box-based to platform-based protection systems. An IED sends and receives information to and from other IED's, for example, voltage and current measurements. With this shared information, notification, control and protection operations can be carried out. An advantage of a platform-based system over a box-based system is that information can be shared between any IED thereby rendering the input and output ports of the device flexible. For example, instead of one relay device having all eight required voltage inputs, the voltage inputs on other devices can be used and the measurements received made available on the Ethernet bus.

A novel method of unbalance voltage protection of a fuseless single star shunt capacitor bank is demonstrated. Consider two multifunction protection relays linked by a 100 Mbit/s Ethernet bus (using the IEC 61850 protocol). Voltage is measured at two points across a capacitor bank with instrument transformers. The measurements are sent to each relay respectively. The measurements received by each device are then shared between the two devices via the communication link. The programmed algorithm in each relay compares the two measured values taken across the bank to determine if a differential voltage exits. A differential voltage implies that the capacitor bank is unbalanced. An unbalance may be due to capacitor element failure or internal bank faults. If necessary, alarm notifications and trip operations can be initiated. Differential- and unbalance voltage in terms of bank unbalance protection are synonymous and are used interchangeably throughout the text.

The research aims to:

1. Provide an introduction to the application of shunt capacitor banks.
2. Perform a study on power capacitor unit design, manufacture and test in accordance to IEC standards.
3. Investigate capacitor fusing technology and discuss advantages and disadvantages.

4. Investigate different shunt capacitor bank configurations from a primary plant perspective.
5. Investigate the protection philosophies applied to the different shunt capacitor bank configurations.
6. Engineer and test a novel approach to a differential voltage protection function specifically for fuseless single star earthed shunt capacitor banks:
    a. Provide a methodology statement.
    b. Engineer the logic necessary to perform the protection function.
    c. Implement the logic into the protection relay's programmable memory.
    d. Prepare a set of tests and prove the protection function operation using an injection test set.
    e. Critically evaluate the results on the premises of availability, reliability, selectivity, and sensitivity.
    f. Prepare a protection setting calculation tool.
    g. Provide an economic analysis of the implementation in contrast to other current applications.
7. Make recommendations on further research and development work, and future trends in protection and power automation applications.

2 Application of Shunt Capacitor Banks

2.1 A Need for Reactive Power Compensation

Shunt capacitor banks are a source of reactive power and are essential for economic operation of electrical systems. By virtue of the components that make up the electrical system, the system is inherently resistive-inductive. Capacitance (C) and inductance (L) are reactive power components. Capacitive reactive power input is equivalent to inductive reactive power output and vice-versa. Inductive reactance can be calculated by: [1]

$$X_L = 2\pi fL \quad \text{..... (1)}$$

And capacitive reactance by:

$$X_C = \frac{1}{2\pi fC} \quad \text{..... (2)}$$

It can be seen in the above two equations that capacitive reactance is inversely proportional to frequency (f), while inductive reactance is directly proportional to frequency. An LC circuit whether it is in series (termed an acceptor) or parallel (termed a rejecter) oscillates when the respective reactance values are equal at a frequency called the resonant frequency. This oscillating frequency (f_o) can be calculated by: [1]

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{..... (3)}$$

Therefore, reactive power is an oscillation of energy. The sinusoidal voltage and current waveforms have the same shape except, the waveforms displace each other by a phase shift. For a capacitor, current leads the voltage or is driven by the voltage, while current lags the applied voltage for an inductor. Essentially, for a capacitor, the current is proportional to the time rate of change of instantaneous voltage. While for an inductor, the voltage is proportional to the time rate of change of current. The sinusoidal 90° phase shift between voltage and current can be expressed as follows: [1]

$$\sin^2(\omega t) + \cos^2(\omega t) = 1 \quad \text{..... (4)}$$

The 90° phase shift presents a sine and cosine curve where their polarities are opposite through half a period resulting in negative power. This negative power is not consumed by the load but is fed back into the network; hence, an oscillation of energy occurs. However, due to the inherent inductive network, this oscillation results in additional current flow causing an increase in load (i.e. consuming the capacity) as well as additional ohmic losses. The inductive component can be offset and therefore the overall current can be reduced by adding an appropriately sized shunt capacitor. The principle of shunt compensation contributes to improving the transmission capacity, and reducing losses in the network. Therefore further volt drops are

reduced. Shunt compensation also has the capability to lower the resonant frequency and provide damping of harmonic components. Consequently, the power factor is corrected towards unity. [1]

2.2 Location Considerations

A network study is performed in order to determine the most economical and technically viable solution. The results of the study aid with selecting the type, size and location of the compensation system. The objectives are; to maintain a desired voltage profile, to improve the power factor and to reduce the losses along feeder circuits. The process to optimise a large electrical system is complex and requires iterative simulations. Voltage operational limits on existing equipment and feeder loadings also need to be assessed within the solution. One of two locations of implementation can be considered; at a) the supply point or b) the load point. However, a mix of the two is the ideal situation.

A large compensator can be positioned at the supply point of common coupling to the network. This will improve the overall power factor, voltage support and transmission capability. However, large quantities of reactive current will flow between inductive loads and the central compensator. This results in losses within the loads. Compensation positioned at the load has the advantage of offsetting inductance directly at the load thereby reducing losses in the load. It depends upon which side of the point of switching at the load the compensation device is installed. There can be adverse effects when the load is open circuit, such as over-compensation looking into the network or providing over-excitation to loads like synchronous machines. In addition, the location of transformers with respect to shunt capacitors and the inductive loads they are to off set, can result in over voltage being experienced by the transformer. Extra losses will also be experienced should reactive current be transformed twice between the load and compensator. Distributed compensation is advantageous at asynchronous generators. For example, wind turbines and cogeneration plants directly connected to the supply system without an inverter can be excited under no voltage conditions. [1]

3 Power Capacitors

3.1 Introducing the Capacitor

Once called a “condenser” but nothing was actually condensed, the capacitor is a device for storing electric charge. It comprises of two electrodes separated by an insulation medium called the dielectric. It is quantified by capacitance which is the ratio of the charge (Q) to the potential difference (V) between the conductors, having the unit farad (F) (coulomb/volt). [2]

$$C = \frac{Q}{V} \quad \text{..... (5)}$$

C is a constant for a given capacitor, and depends on the size, shape, relative position of the two conductors, and the material separating them [2]. Therefore for manufacturing purposes, known quantities can be used to produce the desired capacitor by considering:

$$C = K\varepsilon_0 \frac{A}{d} \quad \text{..... (6)}$$

K is the dielectric constant and ε_0 is the permittivity of free space. The constant is determined by the relation in equation 7 [2], where ε is the permittivity of the dielectric material. Therefore, a certain capacitance can be made by specifying the length, width and distance of separation for a known dielectric [3].

$$K = \frac{\varepsilon}{\varepsilon_0} \quad \text{..... (7)}$$

Note that in equation 5, C is not dependent on Q and V although it is proportional to Q. It is dependent on geometric and material properties of the capacitor. A potential applied to the electrodes sets up an electric field with equal but opposite charge on each electrode. Hence the net charge on a capacitor is zero. The relationship of electric field (E) to the charge per unit area σ is described in equation 8 [2]. Further to this, the relationship between V and E is governed by the distance of separation and is described in equation 9 [2]. Finally, the process of charging a capacitor consists of transferring charge from the plate at lower potential to the plate at higher potential. This requires the expenditure of work.

$$E = \frac{\sigma}{\varepsilon} \quad \text{..... (8)}$$

$$V = E.d \quad \text{..... (9)}$$

It must be noted that the discussion above together with formulae concerns parallel plate capacitors. For other geometries, for example, cylindrical capacitors, Gauss’s Law by definition would need to be applied. This determines the precise relationship between the electric flux through a closed surface and the net charge within that surface in order to establish the correct geometric quantities. The Gaussian Surface can be described by [2]:

$$\oint \overline{E} \cdot d\overline{A} = \frac{Q}{\varepsilon_0} \quad \text{..... (10)}$$

3.2 Manufacturing and Testing

Manufacturing Process

The plates of a power capacitor are made of aluminium foil separated by several layers of polypropylene dielectric film. Several layers of film are used so that a small imperfection in any one layer will not result in a defective capacitor. The foil and dielectric are wound on a mandrel into a capacitor element or 'section'. Older designs used metal tabs in contact with the foil to bring out the electrical connections. This resulted in higher losses due to the length of the current path. Currently, designs typically extend the foil beyond opposite ends of the section. [4]

Generally, standard element sizes are used, typically 314mm x 508mm [3]. The distance (d) of separation between the foil plates is determined by the dielectric stress. The norm for dielectric stress ranges between 66kV/mm and 70kV/mm [3]. The required voltage capability of an element is approximately 1kV to 2.5kV. When the section voltage is too low the individual thickness of the dielectric film required will be too thin to practically handle in the manufacturing process. When the section voltage is too high, a thicker 'sandwich' of dielectric film is required and will result in an increase in voltage stress concentration at the edge of the foil plates. This will have the effect of increasing the corona activity at the foil edge, consequently, reducing the over-voltage capability. Therefore the selection of the section voltage is an optimisation technique for the reliable operation of the element. [4]

According to equation 6, a suitable section can be designed to meet the appropriate voltage capability and capacitance of a section. In turn, the capacitor unit can be electrically sized by arranging the sections in a series-parallel combination. The series-parallel element combination is wrapped in electrical wrapping paper and inserted into a metal case. A carbon film resistor is connected across the connecting leads. This has the affect of reducing the voltage on the capacitor from rated voltage down to 50 volts in 300 seconds [5]. A cover with connecting bushings is assembled to the metal case. The unit is then hermetically sealed except for a hole used for oil impregnation [4].

The unit is dried on a time-temperature vacuum cycle for 3 days at a temperature not greater than 70 °C to remove moisture [3] and volatile materials. This improves the impregnation process. Under vacuum, the unit is then filled with dielectric fluid, filling voids, improving voltage distribution, inhibiting corona discharge and improving the thermal performance [4]. Figure 1 below shows an assembled capacitor unit as described.

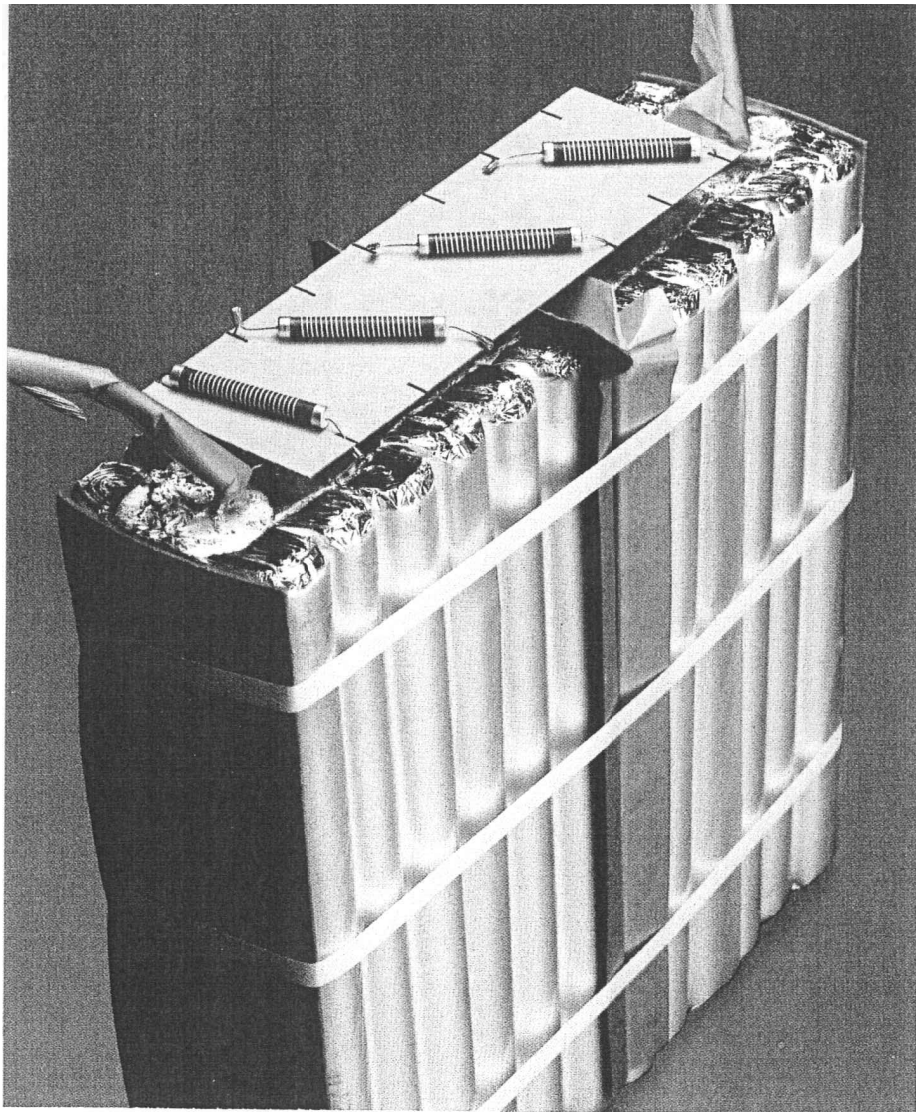


Figure 1, an assembly of a power capacitor showing the internal components [5].

Capacitor Unit Losses

The losses of a capacitor are a function of temperature and voltage. There are three areas of concern. Discharge resistor losses (i.e. the resistor ohmic value); dielectric losses (solids and liquids); and conductor losses (namely, current paths in foils, leads and connections). International Standards require resistors to reduce the voltage to 50 volts in 300 seconds. Therefore the standards dictate the resistor losses. Typically, 0.05 watts/kVAr resistor losses are expected. For dielectric losses, manufacturers using polypropylene film and non-polar insulating fluids could have losses as low as 0.03 watts/kVAr. With respect to conductor losses, it depends on the type of construction. This is generally broken down into three types of construction techniques; tab connections, extended foil crimp and extended foil solder. [5]

For tab connections, the tabs are inserted into the sections. The location and number of tabs determine the current path in the foil. The more tabs in the design, the shorter the current path thus the lower the conductor losses. The conductor losses can be calculated using the following expression taking note that the losses are a function of the square of the number of tabs. [5]:

$$Watts / kVAr = \frac{\pi PfLC}{3WN^2} x10^{-3} \quad \text{..... (11)}$$

Where,

P = foil resistivity (ohms/square)
f = frequency (hertz)
L = length of each foil (inches)
C = capacitance/winding (mF)
W = foil width (inches)
N = number of tabs/foil

For extended foil crimp designs, mechanical crimps are connected to each foil turn. Although reliable, this technique could produce a relatively high resistance connection. [5]

The extended solder design involves parallel rows of solder mats making an electrical contact (metallurgical) to each foil turn. Similar to the crimp design, the current path is reduced to the length of the extended foil. Expected losses range from 0.05 watts/kVAr for the tab design to 0.00005 watts/kVAr for the extended foil solder design. [5]

The expected overall losses for power capacitor units at 25 °C are [5]:

- Tab designs: 0.12 – 0.15 watts/kVAr
- Extended foil crimp connection designs: 0.09 – 1.2 watts/kVAr
- Extended foil solder mat design: 0.08 – 1.0 watts/kVAr

Testing Requirements

Capacitor units are tested before dispatch from the manufacturing facility. A set of mandatory tests (factory routine tests) are required as per IEC 60871-1. The following is a list of tests undertaken [6]:

- Capacitance measurement test.

The capacitance is measured at 0.9 to 1.1 times the rated voltage using a method that excludes errors due to harmonics. The allowable tolerances on units are -5% to +10%, and for banks above 3 MVAr 0% to +5%.

- Tan δ test.

A capacitor loss measurement performed at 0.9 to 1.1 times the rated voltage using a method that excludes errors due to harmonics. Generally the loss value is agreed to by the purchaser prior to manufacturing however a value of 0.1 W/kVar is expected [3].

- Voltage test between terminals.

An a.c. test is performed at twice the rated voltage for 10 seconds or a d.c. test is performed at four times the rated voltage for 10 seconds. A second test would be performed at 75% of the first test. No puncturing or flashover must occur.

- A.C. voltage test between terminals and container.

A 10 second test voltage is applied between the terminals and the container. No puncturing or flashover must occur.

- Test of the internal discharge device.

This test is done to measure the resistance of the discharge device.

- Sealing test.

A test is performed on a non-painted tank to determine any container or bushing leaks.

3.3 Performance of Different Fusing Technologies

As a series-parallel combination of elements make up a unit, so a series-parallel combination of units makes a bank. Three different fusing technologies are in use for the protection and prevention of unit case rupturing and catastrophic damage to the capacitor bank. These are internally fused elements, externally fused units and fuseless capacitor units.

An element normally fails at a point on wave [7] where voltage exceeds the design and manufactured rating of the capacitor. For internally fused elements, fuses are in series with the capacitor element. When an internally fused element fails, the system and parallel elements deliver energy to the fuse. The result is an instantaneous melting and open circuiting of the failed element. For externally fused units, capacitor units are in series with fuses. Under element or unit failure conditions, the whole capacitor unit is isolated from the bank. Banks with fused elements or units require capacitors to be connected in parallel. For fuseless capacitors, the electrodes of failed elements weld together maintaining circuit continuity. Therefore, capacitors are connected in series strings. The risk of case rupturing due to parallel capacitors delivering energy under fault conditions is minimized. [7]

Figures 2 and 3 below [adapted from 8] depict the different fusing technologies. The externally fused unit is similar to a fuseless unit except it has an external fuse and more parallel elements. The fuseless unit has more series elements compared to the externally fused type. When elements fail within an externally fused unit the voltage increases across the remaining elements in service, as does the unit current. Successive failures within externally fused units will result in the fuse operating. Fuseless units require more than ten elements in series. For example, when one element fails, 10/9 times the voltage is distributed across the remaining elements in series. This equates to more than 1.1 per unit voltage thus tripping the bank. Advantages with fuseless elements are that the protection does not have to be coordinated with fuses, and the discharge energy is lower due to few or no parallel

capacitors. In internally fused units, element failure results in fuses removing the affected element only. Therefore fewer parallel units and more series units can be employed in internally fused banks compared to externally fused banks.

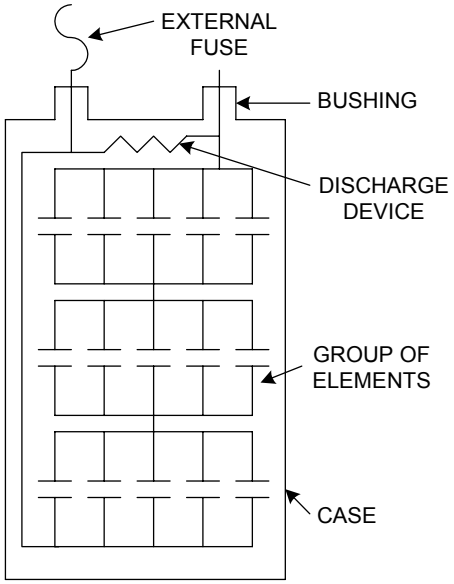


Figure 2, externally fused capacitor unit

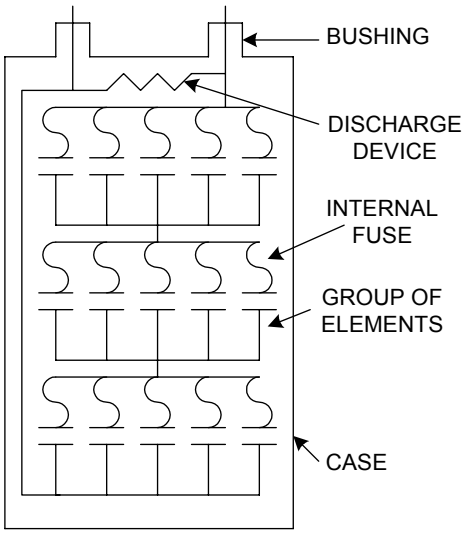


Figure 3, internally fused capacitor unit

3.4 Failure of Capacitors

The manufacturing of capacitor elements has evolved. Formerly, refined kraft paper and a Polychlorinated Biphenyl (PCB) impregnant were used as dielectric and insulating materials. Currently, thinner, uniform and lower loss Polypropylene film and non-PCB hydro-carbon dielectric fluid is used instead. Capacitor elements fail from deterioration of the dielectric due to voltage stress. This failing of the dielectric can be attributed to hot spots and imperfections. Dielectric losses cause hot spots resulting in high temperatures weakening the dielectric strength. The presence of voids or imperfections also results in a weak dielectric and therefore a shorter life span. [9]

Figure 4 below graphically illustrates the evolution of power capacitor dielectrics. This depicts the change from lossy non-environmental friendly PCB impregnated kraft paper of 3.0 to 3.5 W/kVar to the current polypropylene film of 0.1 to 0.2 W/kVar. It is interesting to note the steady response of polypropylene over the temperature range. Also, figure 4 below illustrates the relationship between different dielectrics. Actual loss values may differ from supplier to supplier depending on the grade of material used.

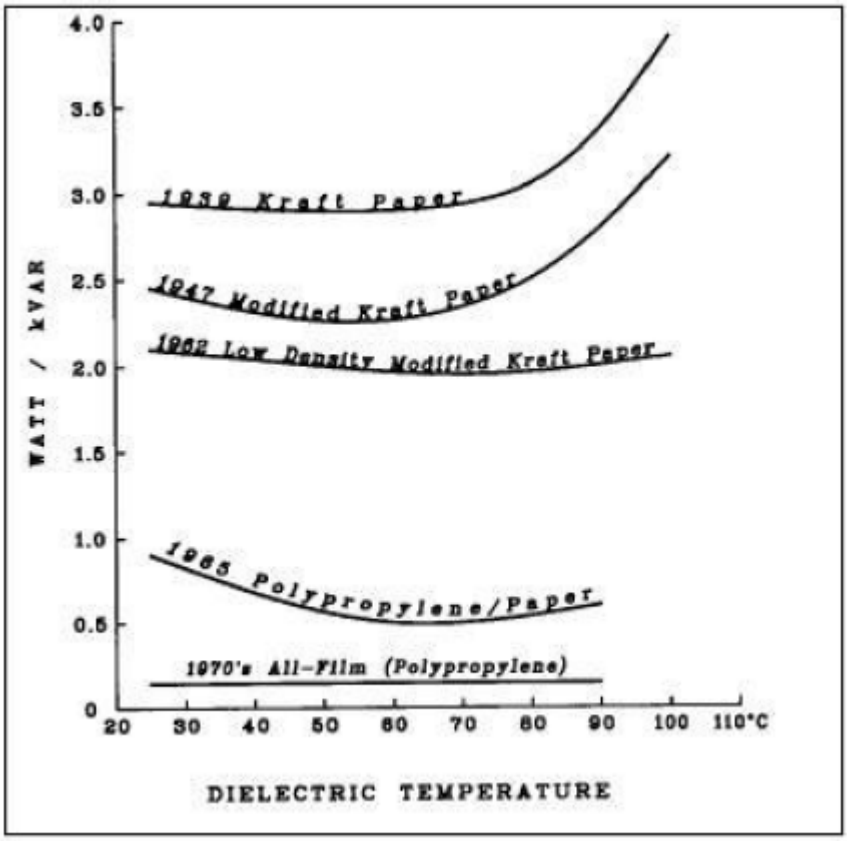


Figure 4, Variation of dielectric losses for different dielectrics [11].

Capacitor element failure modes generally follow a ‘bath tub’ curve [10]. Early failure predominately occurs in the first year of energising due to inherent defects from poor materials, workmanship and manufacturing processes. Random failure occurs between 1 and 20 years and is mainly due to system operating conditions. And finally, the wear-out failure period is predominant after 20 years and is a result of dielectric wear or aging.

4 Shunt Capacitor Bank Configurations

A shunt bank is a matrix of capacitor elements and units per phase. A capacitor is rated to withstand 1.1 per unit continuous overvoltage taking into account the affects of voltage increase due to its capacitance and the ambient temperature variations [6]. A discussion follows on general calculations, bank configurations and protection philosophy.

4.1 Basic Calculations for Capacitor Banks

The following equations are useful to determine voltage and current quantities of capacitor banks.

The line current supplied to a bank can be expressed by [12]:

$$I_{line} = \frac{Q}{\sqrt{3}.V} \quad \text{..... (12)}$$

Where,
Q = reactive power of the bank.
V = the phase-phase voltage supply to the bank.

The system voltage increase due to connection of a capacitor bank to the system can be expressed by [13]:

$$\frac{\delta U}{U} \approx \frac{Q}{S} \quad \text{..... (13)}$$

Where,
δU = voltage increase.
U = voltage before connection of the capacitor bank.
S = short-circuit power (MVA) at the point where the capacitor is to be connected.
Q = reactive power of the bank (MVAr)

Switching in a single bank will cause a transient inrush current of the following magnitude [13]:

$$\hat{I}_s = I_N \sqrt{\frac{2S}{Q}} \quad \text{..... (14)}$$

Where,
$\hat{I}_s$ = crest of inrush current in amps.
I_N = rated capacitor bank r.m.s. current in amps.
S = short-circuit power (MVA) at the point where the capacitor is to be connected.
Q = reactive power of the bank (MVAr)

4.2 Introduction to Bank Configurations

High voltage shunt power capacitor banks are generally star-connected. In the Eskom Transmission System, the banks are arranged in four configurations. The four configurations are; Single Star Earthed, Single Star H, Double Star (earthed or unearthed), and C-Filter H (harmonic current filtering) Configurations. The latter three configurations split the bank to form H-bridge configurations or a neutral bridge for double star banks. This allows an economic method of detection of unbalance current and the location of unbalance within the bank. The Single Star Earthed Capacitor Bank employs unbalance voltage detection. Figures 5, 6, 7 and 8 illustrate the circuits of the different bank configurations.

All banks are generally fed from a double busbar system. The switching bay comprises busbar disconnectors and a circuit breaker with earth-switches either side to facilitate safe maintenance of the circuit elements. The reactors in the circuits are used to limit the inrush current on energizing the bank. Reactors also detune the bank to filter out specific resonant frequencies using resistive damping. The C-Filter type bank has a flat response over a wide range of frequencies and therefore does not cause a resonance condition when connected to the power system [14]. Most large banks are connected in star configuration which provides an option of earthing. Earthed banks provide a low impedance path to ground. They are able to filter out high frequency currents. They also provide self protection to lightning surge currents and voltages. Here, capacitors can use their capability of absorbing the surge, thereby removing the need for arresters [8]. However, earthed banks can allow circulation of harmonic and inrush currents. This may result in mal-operation of fuses and protection relays due to less sensitivity. In large banks the tendency is to introduce an H-bridge per phase (for single star H and C-Filter H configurations), or a neutral bridge between two star points (for double star configuration). This enables the detection of bank unbalance through sensitive current measurement.

Both double star and single star banks use a low voltage earthing capacitor. These have a capacitance in the order of 60 to 80 times the bank capacitance. This means the capacitors shall provide low impedance to earth under unbalanced conditions. This prevents the main capacitor bank from being severely stressed by over voltages when a fault occurs in the bank. [13]

The following sections describe four typical shunt capacitor bank configurations and their protection philosophies. Table 1 below references the protection function according to the American National Standards Institute (ANSI) designation system. The single line diagrams illustrated use the ANSI codes to identify the main protection functions employed.

Table 1, ANSI protection function descriptions.

ANSI code	Function Description
27	Under voltage
49	Thermal overload
50	Over current – definite time
50N	Earth fault – definite time
51	Over current – IDMT
51N	Earth fault – IDMT
59	Over voltage
50BF	Breaker fail
67N	Directional earth fault
87N	Restricted earth fault
87V	Differential / unbalance voltage
50 U/B	Unbalance current

To ensure reliable protection of a capacitor bank, dual redundant protection devices are employed. With reference to table 1, the protection blocks illustrated in figure 5, 6, 7 and 8 show a “main protection” block and a “back up protection” block. The same functions as identified in “main” are replicated in “back up” except for restricted earth fault (87N).

The protection functions can be categorised into four areas:

- General protection
- Breaker failure protection
- Restricted earth fault (unit) protection
- Capacitor bank unbalance protection

General Protection

General protection involves the following functions:

- Over-current-definite-time and inverse-time (IDMT),
- Earth-fault-definite-time and inverse-time (IDMT),
- Directional-earth-fault protection,
- Thermal overload protection, and
- Under- and over-voltage protection.

These functions are applicable to the whole bay.

A definite time characteristic allows over current to be exceeded for up to a defined delay. The inverse time characteristic allows exponentially less over current with time according to predefined International Electrotechnical Commission (IEC) or ANSI curves. Directional protection takes into consideration the direction of energy flow to the fault.

The thermal overload protection is designed to prevent thermal overloads from damaging the protected equipment. The protection function models a thermal profile of the object being protected (overload protection with memory capability). Both the history of an overload and the heat loss to the environment are taken into account [15].

The over voltage function protects against often occurring abnormally high voltages. Some examples of over voltages occurring are:

- lightly loaded long distance transmission lines,
- islanded systems when generator voltage regulation fails, and
- after full load shutdown of a generator from the system.

The under-voltage protection function detects voltage collapses on transmission lines and electrical machines. It also prevents inadmissible operating and a possible loss of stability [15]. Both over- and under voltage protection functions are set on a definite time basis.

Breaker Failure Protection

The breaker failure protection function monitors the reaction of a circuit breaker to a trip signal. If after a programmable time delay, the circuit breaker has not opened, breaker failure protection issues a trip signal. There are two criteria for breaker failure detection:

- Checking whether the actual current flow effectively disappeared after a tripping command had been issued,
- Evaluate the circuit breaker auxiliary contact status.

The breaker failure protection function can be initiated by two different sources:

- Trip signals of internal protective functions,
- External trip signals via binary inputs.

For each of the two sources, a unique pickup message is generated, a unique time delay is initiated, and a unique trip signal is generated. The setting values of current threshold and delay time apply to both sources. [15]

Restricted Earth Fault Protection

This form of protection is designed for fast and selective differential protection based on the high impedance circulating current principle [15]. The zone of protection is between the current transformers situated before the damping circuit and the neutral point. Therefore unit protection is applied across the entire bank to the neutral point.

Unbalance protection shall be discussed under each section relating to the respective configuration.

4.3 Single Star Earthed

Figure 5 illustrates the single star earthed bank in a single line diagram form. The capacitor bank itself indicates the star connection on a per phase basis. As previously described, the outdoor bay comprises of the following switching devices; busbar disconnectors (off load switching), a circuit breaker for on-load switching and for the isolation of faults, and earth switches for safety and maintenance purposes.

The resistor is used for damping harmonic current detuned by the reactor. The purpose of the reactor is to detune the dominant harmonic current. This includes presenting the shunt compensation as an inductive quantity to the network in order to mitigate resonance between the capacitor bank and the inductive overhead line. Instead the series reactor resonates with the capacitor with the affect that their resonant magnitudes cancel each other out.

Unbalance Protection of Single Star Earthed

Figure 5 illustrates two voltage transformers measuring phase to earth voltages. One is positioned at the busbar supplying the bay, while the other is positioned at the low voltage capacitor. This form of protection may only be used on solidly earthed banks [13]. The principle of the unbalance protection is to measure the change in voltage between the busbar and the low voltage tap point. The protection is insensitive to system fluctuations as the ratio of the busbar voltage and tap voltage remain constant. Also, the protection needs to be insensitive to harmonics as this can cause bank unbalance. Therefore, insensitivity to harmonics will avoid spurious trips.

More details shall be discussed in the sections relating to the novel approach to differential protection of fuseless single star earthed capacitor banks.

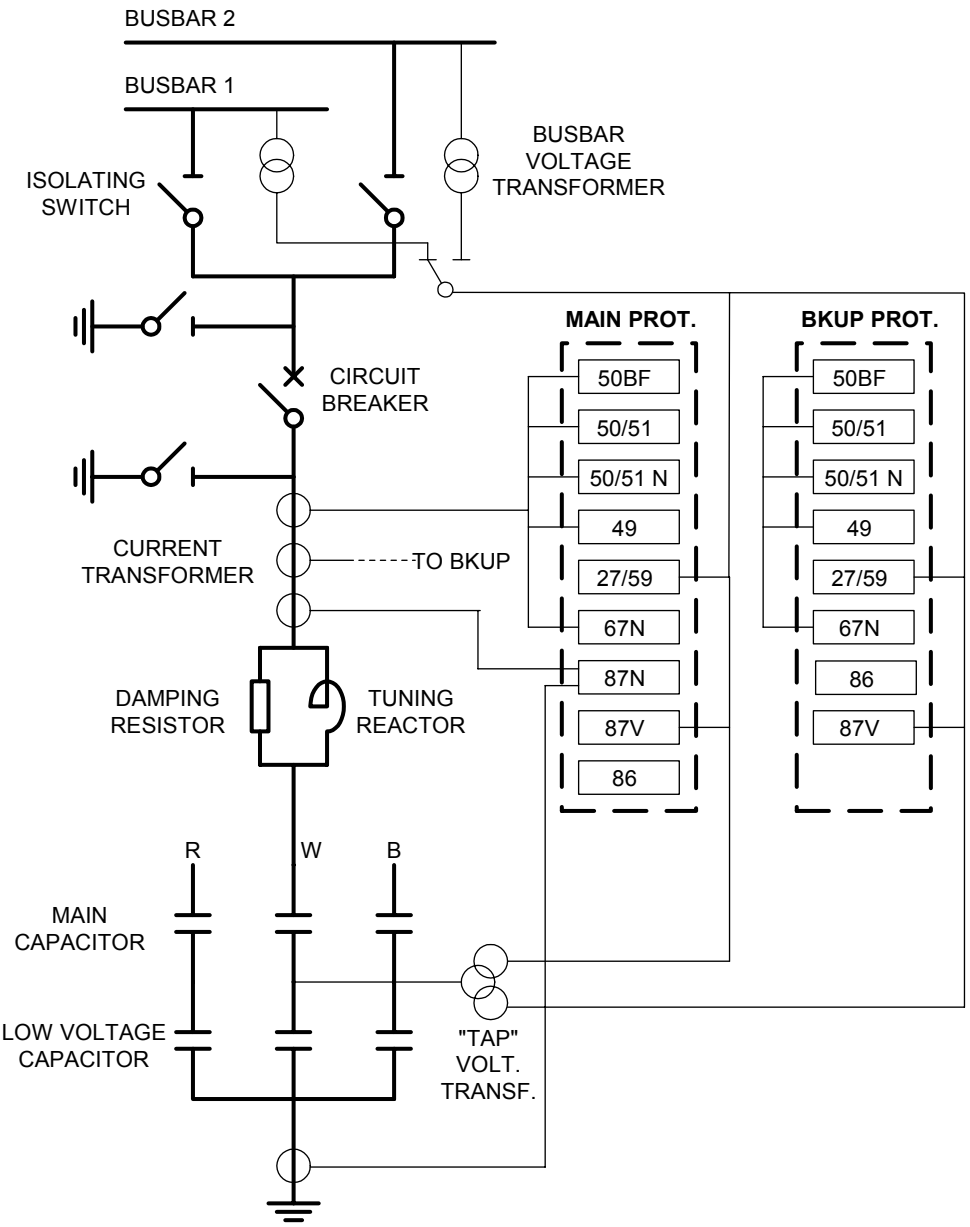


Figure 5, single star earthed configuration, adapted from [16].

4.4 Single Star H-Configuration

Figure 6 illustrates the single star H-configuration bank in a single line diagram form. As previously described, the outdoor bay comprises of the same switching devices as with the single star bank. Similar to the single star earthed configuration, the single star H-configuration has a main bank and a low voltage earthing capacitor. However, with the H-configuration, the overall bank is split on a per phase basis into four capacitor branches. A bridge links the four branches into an H-configuration. The bridge provides the means to measure current flowing, as a result of capacitor element failure.

Unbalance Protection of Single Star H-Configuration

From figure 6, it shows three current transformers located in the H-bridge. In particular, the currents measured are tested against the protection elements situated in the main (main prot.) and back-up (bkup prot.) blocks. Depending on the bank

design and construction, the measured currents are tested against preset current thresholds. Main and back-up overcurrent elements are used to detect the smallest step changes in unbalance current. The step change can be recorded as a change in the amplitude or angle of the unbalance current vector [12]. For fuseless banks, there is a step current change in the range for a single element fault. This fault occurs in the row of series connected capacitor elements of a string. For fused banks, it is the change in the range for a fault due to a fuse operation either internally or externally [12]. The back-up block has a Hi-set (or instantaneous) over current protection element. The Hi-set protection function trips the bank should there be an earth fault within the bank, an inter-rack fault or a phase to phase fault.

It is possible to determine which branch in the bank is causing unbalance. Should there be a capacitor element failure in either the top left or bottom right branch, a current in the bridge will flow from left to right. Similarly, should a current flow from right to left, the polarity in the measuring angle will change. This will indicate that either the top right or bottom left branch is faulty. [12]

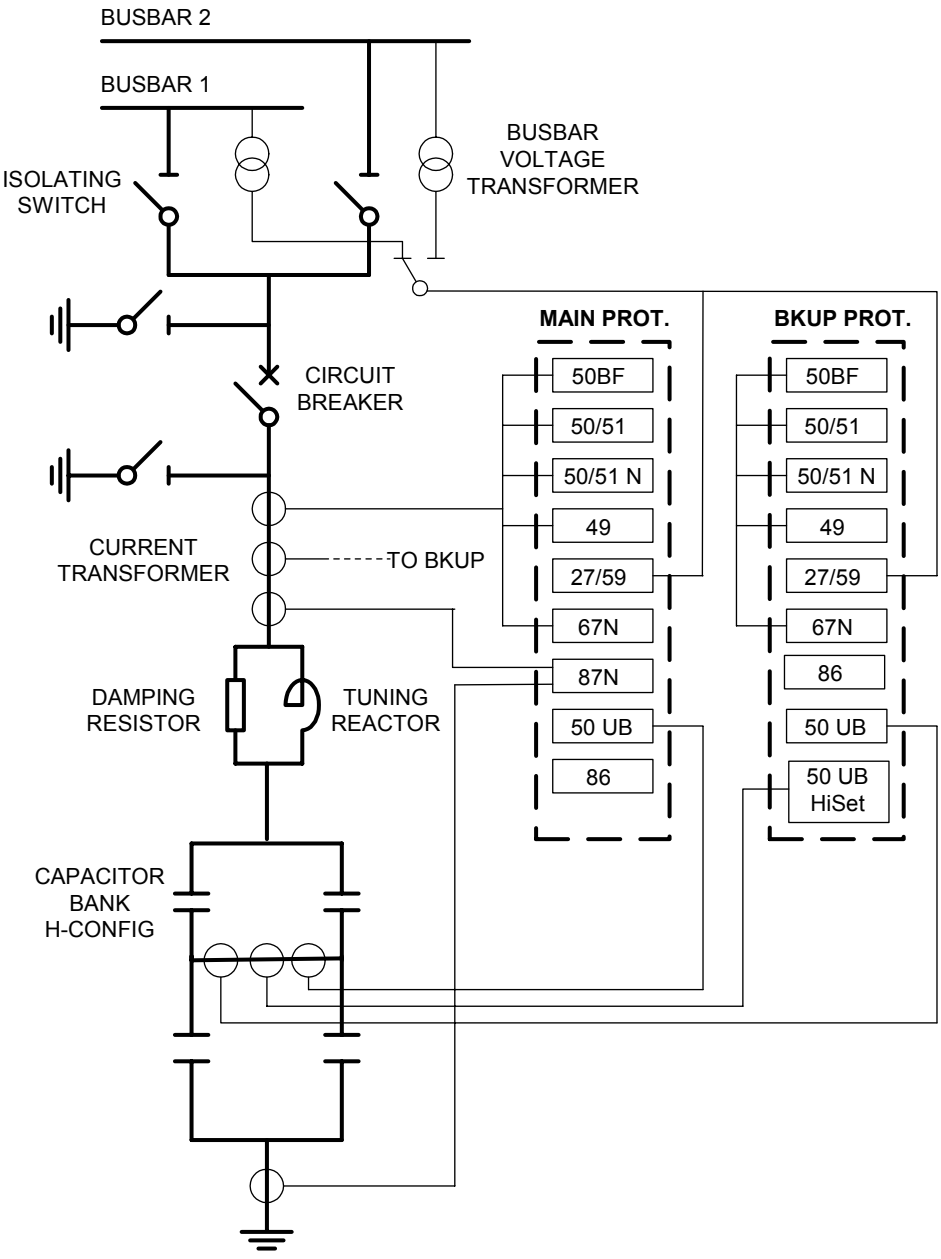


Figure 6, single Star H configuration, adapted from [17].

However, simultaneous failure of the top left and right branches or the bottom left and right branches would cancel out the current through the H-bridge. The remaining elements in the bank experience an over voltage stress but this stress is not picked up by the current transformers or at least does not exceed their preset threshold setting values. A disturbance recorder or “measurement rack” may need to be installed to trigger any change in unbalance current or angle.

4.5 Double Star

Figure 7 illustrates the double star configuration bank in a single line diagram form. The two star points are drawn to show the three phases. As previously described, the outdoor bay comprises of the same switching devices as with the single star bank. In the double star configuration, the phases are split to form two star connections each with a main capacitor bank and low voltage earthing capacitor. Splitting the bank provides the means to determine unbalance by measuring current flow in the neutral bridge.

Unbalance Protection of Double Star Configuration

From figure 7, it shows three current transformers located in the neutral bridge. As with the single star H-configuration, the currents measured are tested against the protection elements situated in the main and back-up blocks.

The capacitor bank angle is defined as the angle between the unbalance current and the red phase voltage vector. In figure 7, consider the left star point as star point 1 and the right star point as star point 2. If the fault is in the red phase of star point 1, the unbalance current will flow from left to right in the neutral bridge. This current will lead the red phase voltage by 90°. For a fault in the white phase of star point 1, the current will lead the white phase voltage by 90° but will lag the red phase voltage by 30°. Similarly, for a fault on the blue phase, the current will lead the blue phase voltage by 90° and lag the red phase voltage by 150°. [12] This method of analysis can provide the capability to determine the location of element failure.

Faults in star point 2 can be evaluated in the same way except that the current will flow from right to left in the neutral bridge. This will change the polarity of the current angle by 180°. Therefore, instead of the current leading by 90° it will lag its respective voltage by 90°. Faults in both star points could create ambiguity in the angle between the current in the bridge and the referenced red phase voltage. To solve this situation, it is recommended that a disturbance recorder or measurement rack is installed to trigger any change in unbalance current or angle. [12]

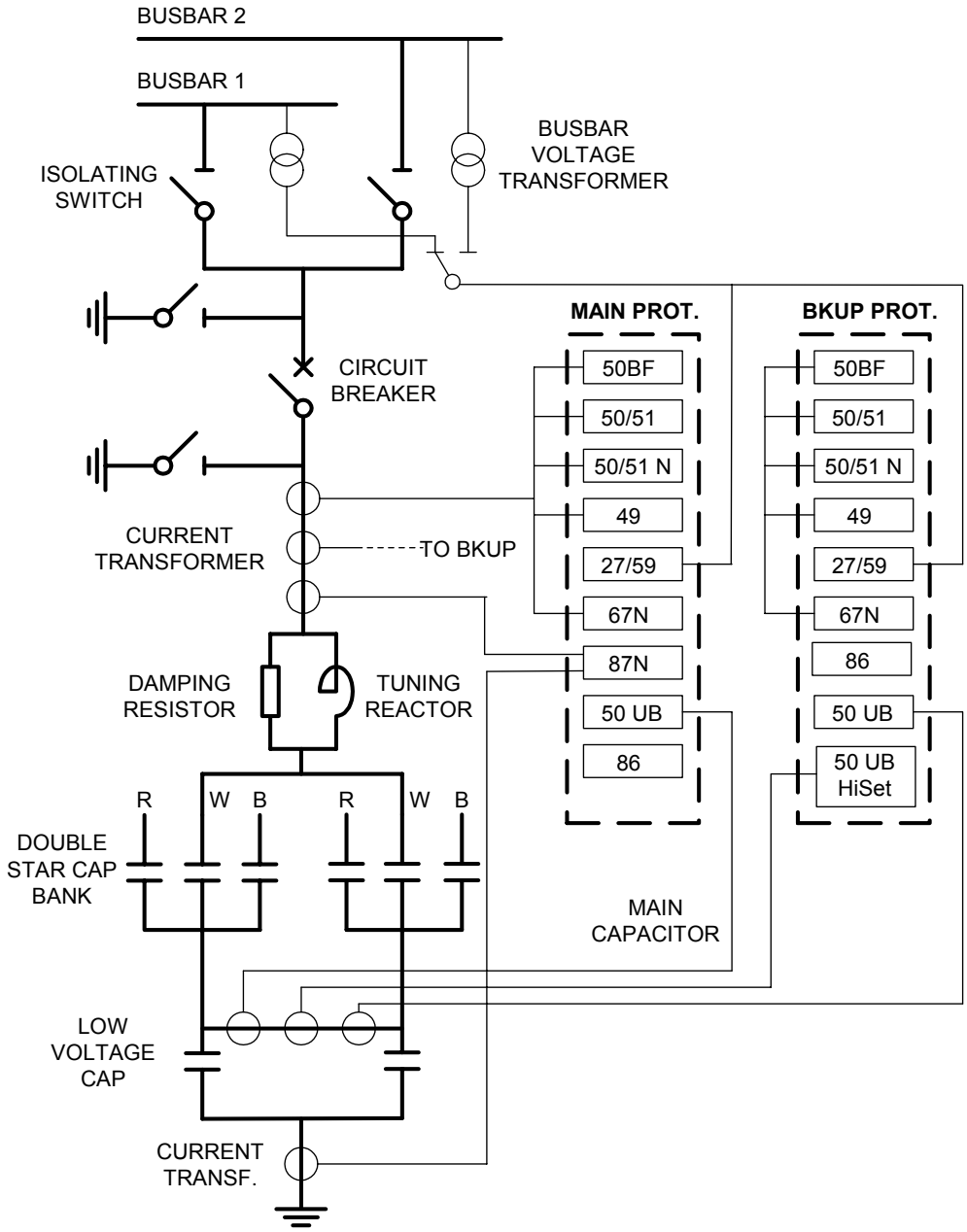


Figure 7, double star earthed (or unearthed) configuration, adapted from [18].

4.6 C-Filter H-Configuration

Figure 8 illustrates the C-Filter H-configuration bank in a single line diagram form. The overall bank is connected in star. The main capacitor bank is connected in H-configuration similar to the single star H. In addition, there is a tuning bank which is also connected in H-configuration in series with a reactor and in parallel with a resistor. For the reason previously discussed, H-configurations allow economic detection of unbalance current.

A filter circuit provides a low impedance path at a desired harmonic frequency, and therefore most of the harmonic current flows into the filter and not the network. For example, a single tuned filter may provide a peak at an undesirable parallel-resonance. Changes in the electrical system can shift the resonant frequency. This shift may be problematic as harmonic current is not being damped. This can occur at

a lower frequency or a non-offensive frequency where there is little harmonic impact. [14]

The C-type filter has a flat frequency response over the frequency range of interest, at least covering the lower order harmonics. The filter relies upon resistive damping. This yields the favourable scan characteristics of essentially no problematic resonance across the frequencies of interest. The reactance of the tuning capacitor will cancel the inductive reactance of the tuning reactor. The net impedance of the resonant combination is zero ohms. Under normal power frequency (fundamental) operation the damping resistor is effectively shunted and thus prevents costly losses. The only element left in service is the main capacitor bank. When the bank is subjected to harmonics, the filter circuit no longer presents a zero impedance path in the network. The harmonic currents are therefore dissipated into the resistor. [14]

Unbalance Protection of C-Filter H-Configuration

From figure 8, it shows three current transformers located in the H-bridge of the main capacitor bank section. As with the single star H-configuration, over current main and backup protection and backup Hi-Set protection functions are employed in the main bank. Similarly with the filter bank, main and backup over-current protection is applied. Considering the intensive dissipation of harmonics undertaken by the resistor, the resistor branch uses thermal overload protection.

As discussed with the single star H-configuration, it is possible to determine which branch in the main capacitor bank and in the filter bank, cause the unbalance. Likewise, simultaneous failures in opposite branches will cancel the current through the bridge. It is recommended that a disturbance recorder is installed to trigger any change in unbalance current or angle.

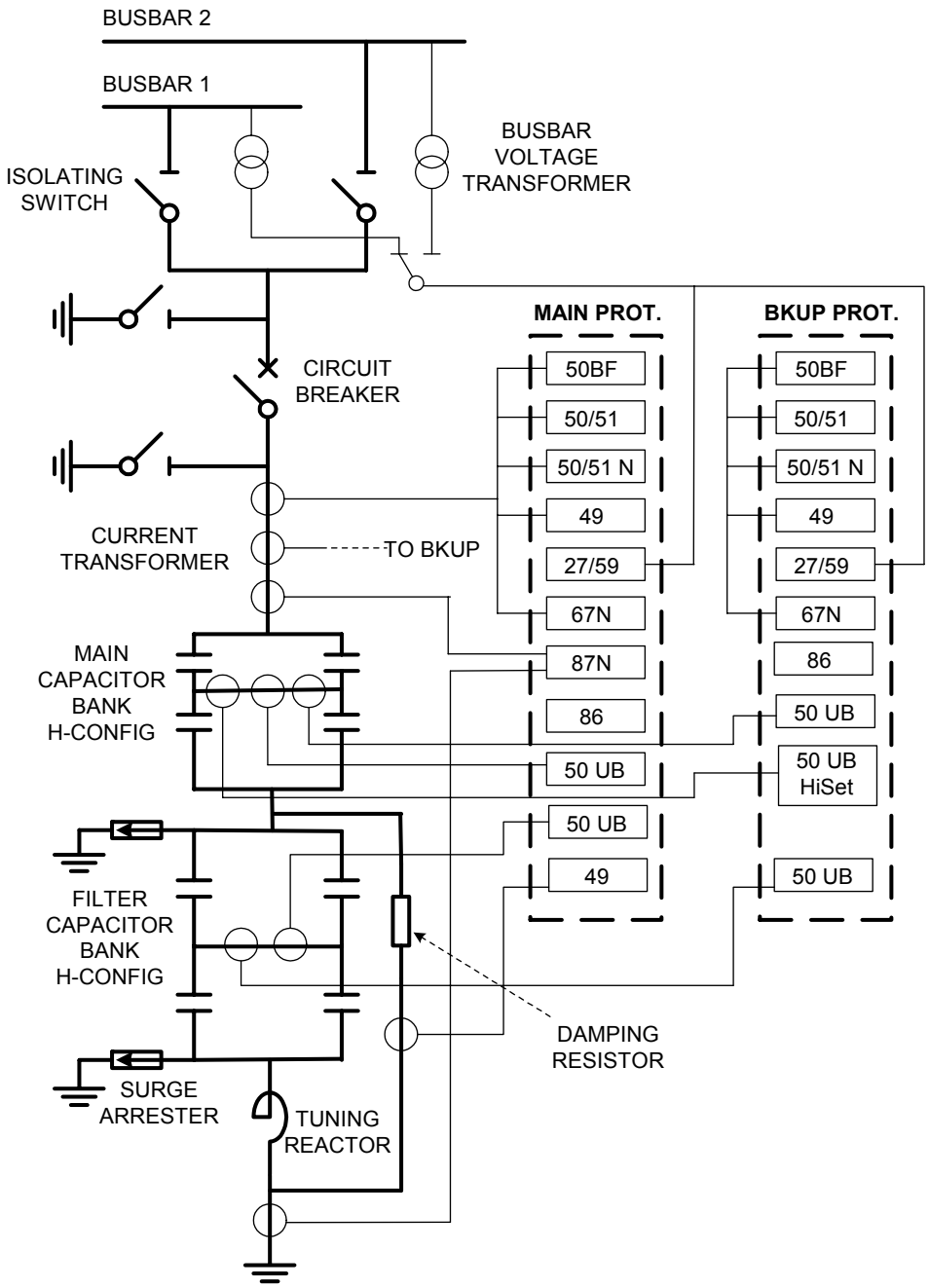


Figure 8, C-Filter H configuration, adapted from [19].

5 Novel Approach to Differential Voltage Protection of Single Star Earthed Banks

5.1 Methodology

This section focuses on the development, implementation and testing of a voltage differential protection function. This is achieved by using two multifunction relays which communicate with each other using the IEC 61850 protocol (refer to Appendix B). This is a novel approach involving "distributed" protection which is a departure from box-based protection to platform-based protection. The one relay obtains voltage measurements from the busbar supplying the capacitor bank. The other relay obtains voltage measurements from a "tap" voltage transformer within the capacitor bank. The two relays compare readings communicating via an Ethernet communication link. In accordance to programmed logic, the relay functions initiate alarm and trip signals in the event of unbalance detection in the capacitor bank. This is based on the number of failed capacitor elements. The number of failed capacitor elements per phase necessary to initiate the protection commands is determined. The application of this protection function is implemented on Siemens Siprotec range of relays. Namely their 7SJ6 type multifunction over current protection relays (refer to Appendix C).

Knowledge of capacitor bank primary plant equipment, bank configuration, and protection principals are necessary to effectively engineer the protection methodology. Figure 9 illustrates the circuit diagram of a single star earthed capacitor bank. The protection methodology is implemented for this type of configuration. The diagram shows a busbar voltage transformer supplying system voltage measurements to "relay (busbar)". A "tap" voltage transformer supplies voltage measurements from a tap point at the low voltage capacitor to "relay (tap)". If capacitor elements fail, there will be a voltage shift at the tap voltage relative to the bus voltage. This relationship can be described with the following formula:

$$\Delta V = V_S - K_r \cdot V_T \quad \text{.....} \quad \textbf{(15)}$$

Where:

ΔV = differential/unbalance voltage,
V_S = system voltage from the busbar,
V_T = tap voltage at the low voltage capacitor,
K_r = relay compensation factor.

For "healthy" bank conditions, that is, under balanced conditions, ΔV will equal zero. A finite (ΔV) will result from tolerances in the capacitors and from the windings of the voltage transformers. A finite voltage will also be established if the ratios of the measurement transformers are not designed the same. A relay compensation factor (K_r) is used to null out the ΔV such that under healthy bank conditions, ΔV equals zero.

The two relays communicate using GOOSE (Generic Object Oriented Substation Event) messaging, which is a fast inter-device communication service. GOOSE messages receive prioritization over "normal telegrams". They are sent via multicast on a publisher/subscriber architecture basis as opposed to the classic master/slave

configuration. Messages from both voltage transformers are compared via a set of engineered and programmed logic functions on the relays. The function logic determines definite step changes in voltage caused by capacitor element failure on a per phase basis.

Depending upon the quantity and arrangement of elements, an alarm signal at 1.05 per unit system overvoltage shall be initiated when a certain number of elements fail. This allows time to plan an outage and repair the bank before further damage occurs. If unattended, or due to external influences, the bank will trip at 1.1 per unit system overvoltage. The plant will then be instantaneously unavailable to the network. This may cause system disturbances and load rejection.

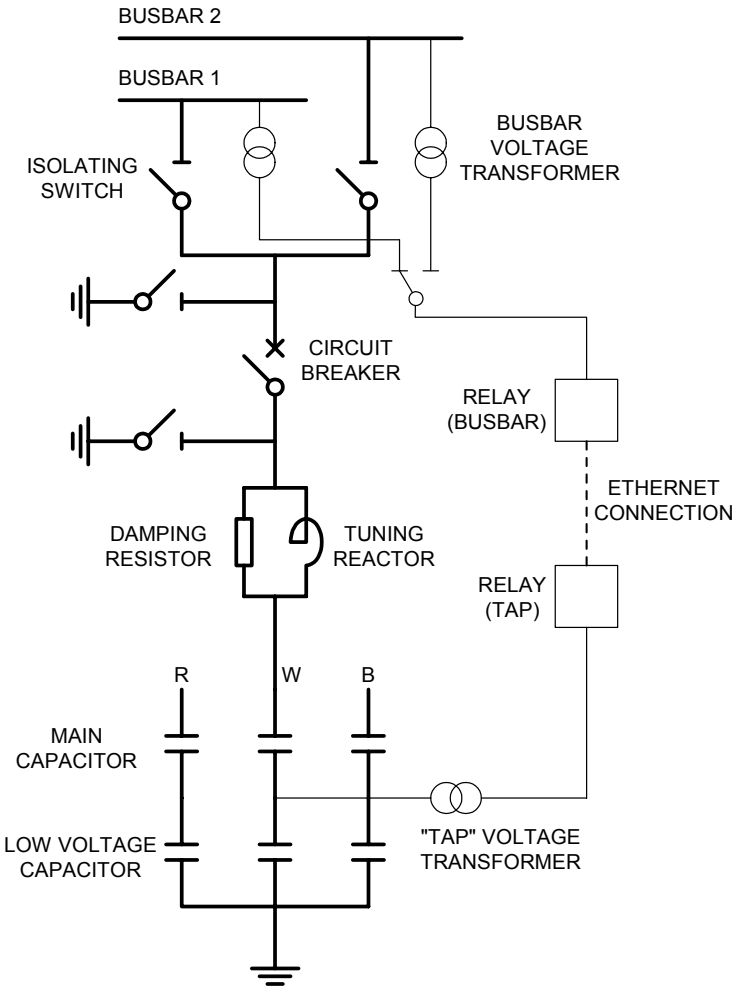


Figure 9, diagram of a single star earthed capacitor bank scheme with differential voltage protection application.

The protection function shall be tested against the parameters, ratings and recommended settings of an existing shunt compensator. The compensator is a fuseless single star earthed, 400kV 100MVAr shunt capacitor bank at Beta Substation, South Africa.

Points of consideration are relay element stability (minimum element stability), independence of phase angle of the two (bus and tap) voltage inputs, and rejection of harmonic voltages to prevent mal-operation.

Figure 10 shows the set up of the differential voltage protection application. The set up shows:

- internet Protocol (IP) address allocations,
- the Ethernet switch for network extendibility,
- the configuration tool (software on a computer),
- the voltage signal inputs from the busbar and tap points respectively.

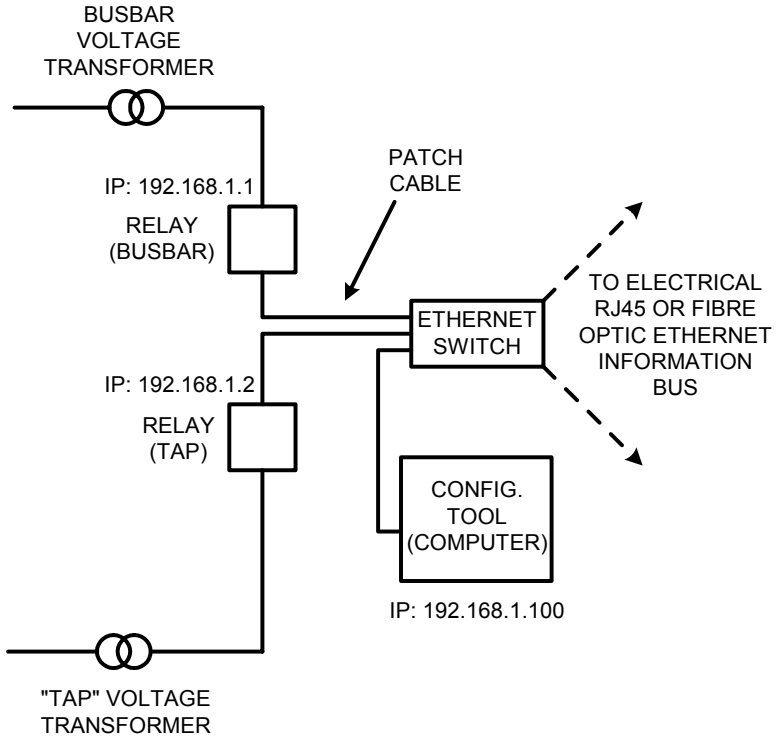


Figure 10, differential voltage protection setup (for an extendible system).

5.2 Operational Considerations

The unbalance function is specifically dedicated to monitoring and protecting the bank. Other protection functions such as over- and under voltage, over current, and earth fault protection are performed independently. The operation of the unbalance function needs to take the following into consideration:

1. The intention is to apply this protection function to the class of standard multifunction protection relays. The principles remain the same irrespective of the 'brand' of relay, however the following constraints and minimum requirements are pointed out:

    a. An IEC 61850 compliant relay and Ethernet card is required.
    b. Four voltage inputs for per-phase measurement.
    c. User programmable logic capability.

d. Inherent under- and over voltage protection elements (would therefore be able to provide a complete set of voltage protection functions).
e. Fundamental voltage measurement only.

2. Three functions of differential voltage protection are considered. Firstly, an alarm pick-up which is usually at 1.05 per unit of the capacitor element rating [20]. This function is performed on a per phase basis. Secondly, a trip pick-up which is set to 1.1 per unit of the capacitor element rating [20]. The bank should trip when experiencing this step change. The trip prevents further over voltage stress on the remaining healthy series capacitor elements. Thirdly, an instantaneous high-set trip which usually is set to 1.5 per unit [20]. Typically, the high-set trip will operate due to catastrophic failure or from inter-rack flashovers within the bank. All functions signal operation via an LED on the relay panel display (refer to Appendix D).

3. Alarm, trip and high-set functions need to be output to a re-triggerable monoflop timer. This will ensure that protection does not operate on energising or from temporary system disturbances. Essentially the re-triggerable monoflop timer provides a delay. This delay is a settling time used to mitigate false operation.

4. The protection functions must be insensitive to harmonics in order to avoid spurious alarms and trips. The filtering of the fundamental voltage is performed by the inherent filtering algorithm of the relay.

5. Magnitudes of the measured input voltages must be used to exclude the possibility of phase error between the busbar and tap points. This may occur due to the windings of the voltage transformers. A change in phase would alter the voltage vector thereby establishing a differential between the two measured points. When capacitor elements fail and therefore fuse, the impact is on the magnitude and not the phase [7].

6. A loss of potential on any of the phases will result in a differential voltage between the high-voltage bus and tap point. A loss of potential may result from clearing an external line fault or from manually energizing or de-energising the bank. Loss of potential seen by the differential protection function must be ignored. Instead, the dedicated under voltage protection element must see to this event.

7. High voltage capacitor banks are normally supplied by a double busbar system. Switching between busbars is a system operation function. Each busbar has its own voltage transformer. A voltage transformer selector is used to select the voltage transformer on the active busbar. Although the two voltage transformers are of the same design, they could introduce an error in measuring due to their inherent tolerances. This means it is probable that switching from one busbar voltage transformer to the other may yield different measurement values. To correct this, two protection setting groups for the differential function are required in the relay. That means, a unique relay compensation factor (Kr) for each voltage transformer is required.

5.3 Logic Application

The implementation of the logic can be broken down into three areas (refer to Appendix E):

1. Calculating the differential voltage as per equation 15;
2. Creating logic for the comparison of differential voltage and the alarm, trip and hi-set trip thresholds;
3. Creating logic to block the function operating when there is a loss of potential.

User defined information items are created for each function block in the 'device matrix' of the relay. Here the items are allocated to sources and destinations. Essentially the device matrix is where measurements, set points, commands and indications are masked to inputs and outputs. Such inputs and outputs are the:

- System interface, i.e. sending and receiving information is presented to the system port of the relay,
- Sources and destinations of the PLC function blocks (the Continuous Flow Charts – CFC),
- Liquid Crystal Display (LCD) of the relay if applicable,
- LED's on the front panel of the relay,
- Relay binary input and output contacts.

Information sent and received on the Ethernet bus is masked to the system interface in the device matrix. Information required for the building of logic functions in the CFC is masked to the source or destination of the CFC in the device matrix. The source and destination of the CFC in the device matrix defines whether the information item is to be used as an input or output to the PLC function blocks.

Consider the logic implemented on one relay, say the 'tap' relay. The voltage measurements from the 'busbar' relay are sent to the 'tap' relay system port for further processing. On this basis consider the logic diagrams in figures 11 to 16.

Figure 11 shows the logic as per equation 15 implemented on a per phase basis. Where the Vt measurement value (tap point) is multiplied by Kr set point value and then subtracted from Vs (busbar) measurement value. The result is processed through an absolute block to ensure a positive value for dV, the differential voltage. As capacitor elements fail so the impedance on the faulty string becomes less resulting in a tap point voltage increase. Therefore at the secondary voltage level (outputs of the VT's), Vt shall become greater than Vs resulting in a negative value for dV. Any changes in dV can be tested against positive value set points entered in the device matrix. Set points are the relay setting values. These are calculated uniquely for each application.

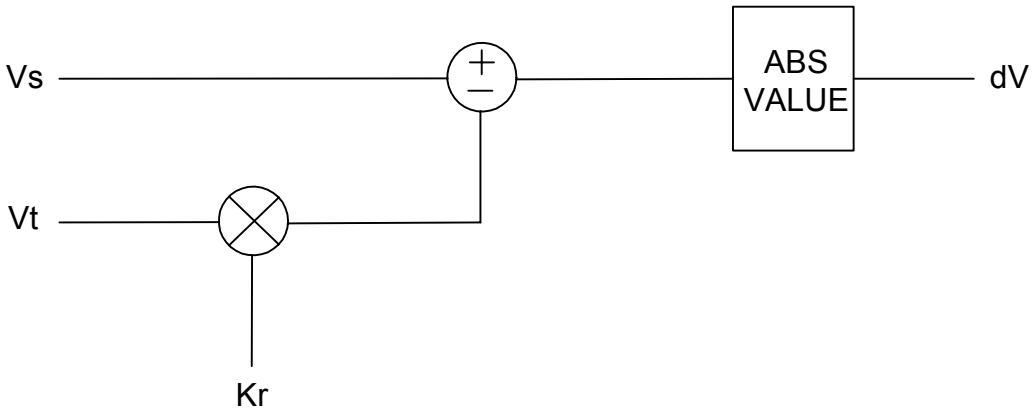


Figure 11, logic diagram showing the voltage differential calculation implemented on a per phase basis.

The output calculated dV value is then ready for processing against the set point threshold for an alarm level, trip level and hi-set trip level as indicated in figures 12, 13 and 14. Each respective set point function is processed on a per phase basis.

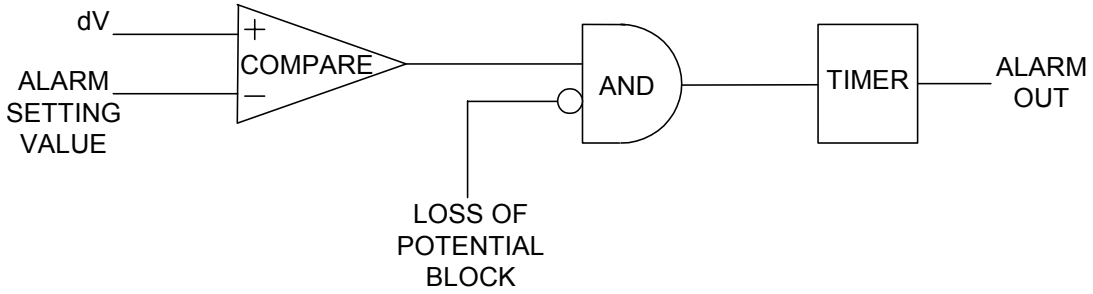


Figure 12, logic diagram showing the alarm function on a per phase basis, adapted from [9].

Figure 12 shows the comparison of the dV value and a pre-defined alarm settable value in millivolts. The comparison block used, generates a Boolean zero should the alarm setting value be greater than the dV value. A Boolean one will result should the dV value be greater than the alarm setting value. In order to ensure that the alarm output is not triggered due to a loss of potential, the loss of potential output from diagram 16 is checked against the output of the comparison logic block.

For no-loss of potential, the AND gate maintains a Boolean one. Therefore if the output of the comparison block is a Boolean one, i.e. dV exceeds the setting threshold, the output of the AND gate issues a Boolean one and starts the mono-flop re-triggerable timer. The timer is run over a user defined delay to ensure that the set change in dV is permanent. A permanent step change will result in the Alarm Out command being initiated. The alarm signal is issued on a per phase basis. Therefore one can distinguish which phase of the capacitor bank requires on-site investigating and maintenance.

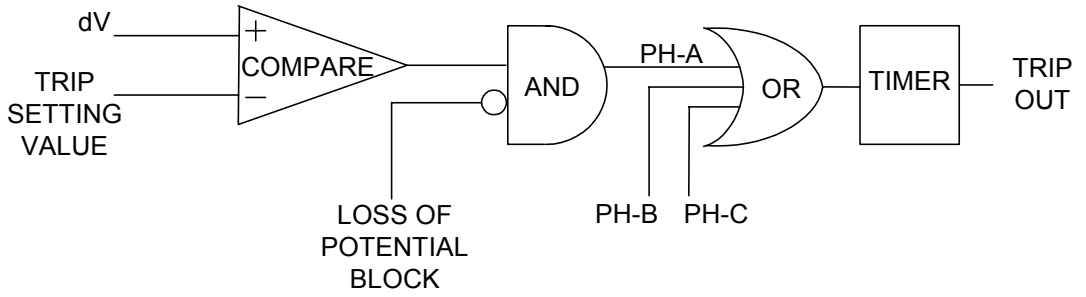


Figure 13, logic diagram showing the trip function, adapted from [9].

Figure 13 shows the logic diagram for the trip function and is applied in the same way for each phase up to the OR gate. The logic for this normal trip function is performed in a similar way as with the alarm function. The dV value is compared to the user defined trip setting value, and checked against the loss of potential function. An OR gate is inserted between the AND block and TIMER block unlike with the Alarm logic. The reason is that if dV exceeds the trip setting on any of the phases, the TRIP OUT command must be initiated immediately. This speeds up the processing time and is priority driven.

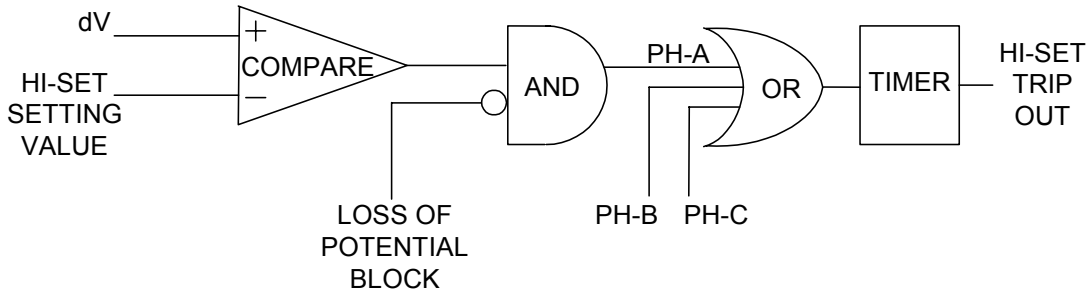


Figure 14, logic diagram showing the Hi-Set trip function, adapted from [9].

Figure 14 shows the logic diagram for the Hi-Set trip function. The processing is done in exactly the same way as done for the normal trip function illustrated in figure 13. Practically the differences would be in the user defined set points as applied to the Hi-Set setting value and the delay TIMER.

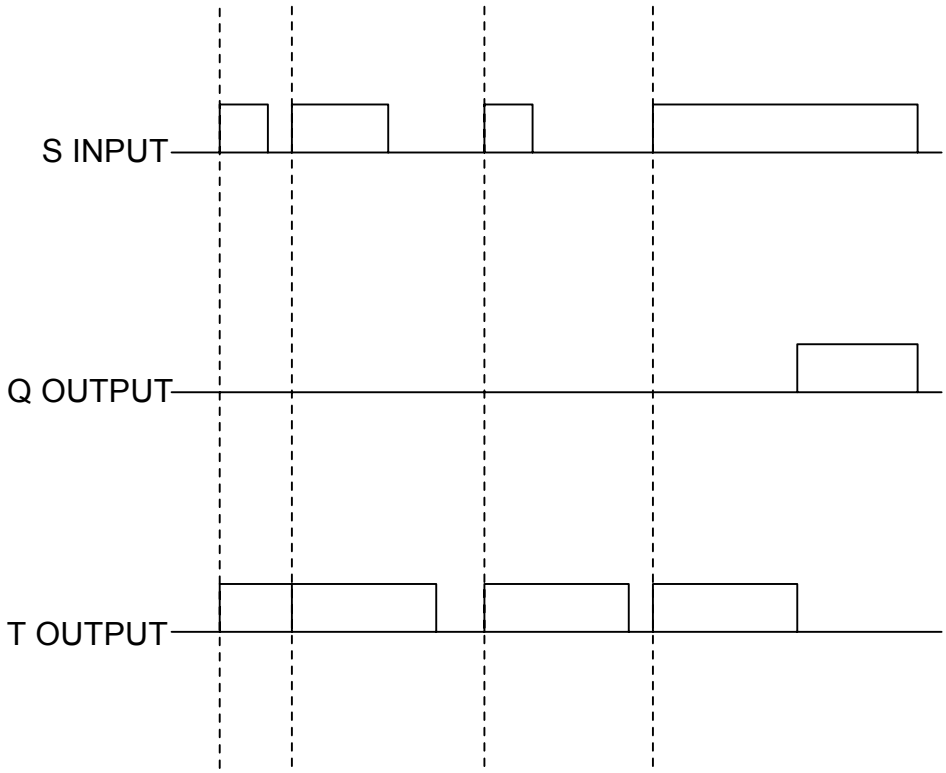


Figure 15, timing diagram for a mono-flop re-triggerable timer. [15]

Figure 12, 13 and 14 illustrate the logic for the alarm, trip and Hi-Set trip protection functions. Figure 15 shows the timing diagram of the mono-flop re-triggerable timer. The S INPUT is received from the preceding logic block. From the AND gate in the alarm logic and from the OR gate in the trip logics. The T OUTPUT is the user defined settable time delay to the timer block. The signal Q OUTPUT is the output initiating the protection command for each of the three protection functions.

When S INPUT goes high (Boolean one), the T OUTPUT timer starts. If S INPUT changes between states, the timer re-triggers. When the timer has timed out, Q OUTPUT goes high, but only if S INPUT is still high, else the process starts again. Q OUTPUT remains high as long as S INPUT is high. The timer function ensures that the step change experienced is permanent. Therefore the timer prevents spurious alarms and trips resulting from capacitor bank inrush currents, system transients or fluctuations and temperature changes across the capacitor bank.

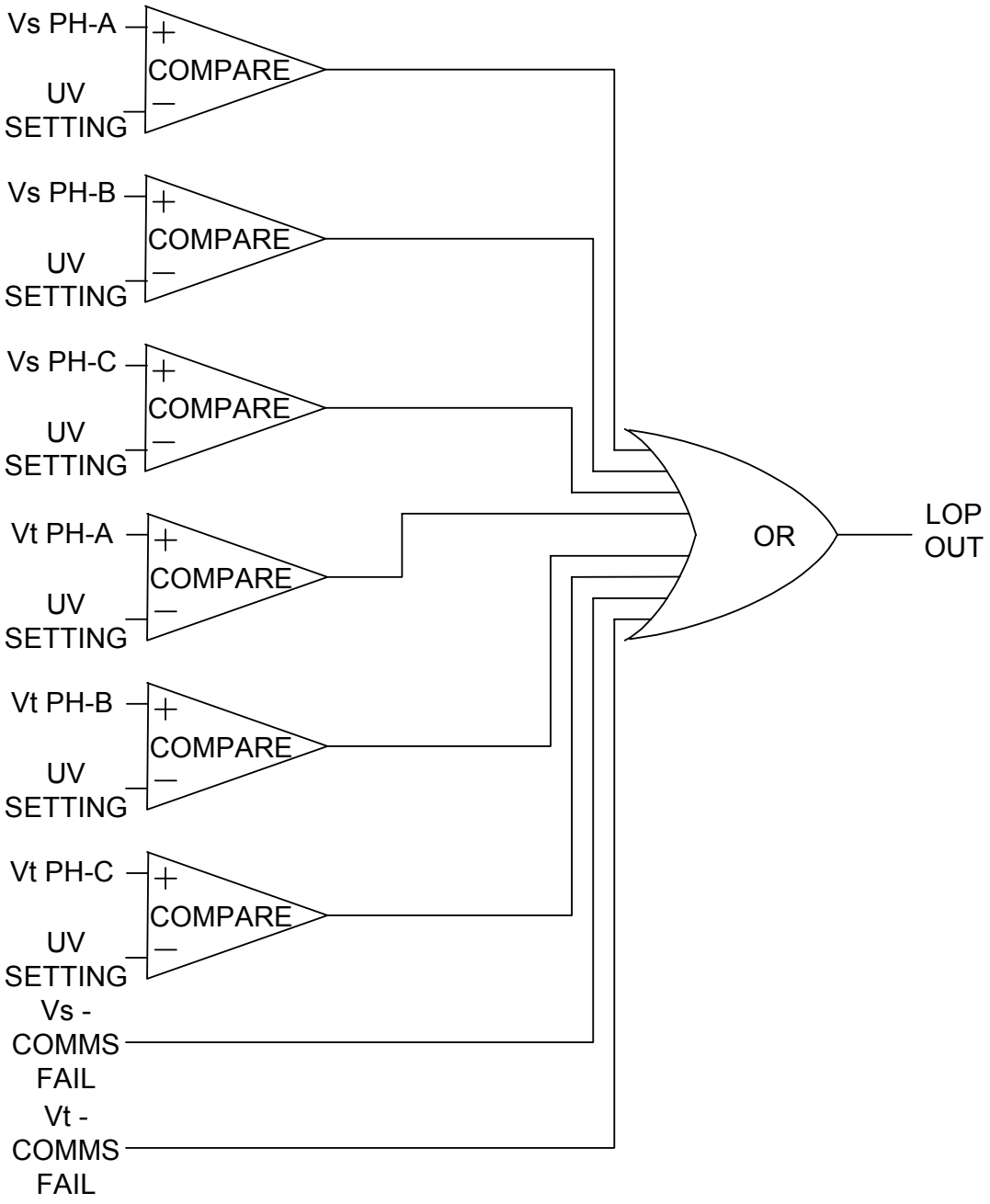


Figure 16, logic diagram showing the loss of potential block function.

Figure 16 shows the logic diagram for the loss of potential function. This function supervises the potential on all six voltage inputs including the Ethernet communication link. Here the six voltage measured values are compared against user defined under-voltage settings. Should the voltage collapse to below the threshold settings, a Boolean one result will be presented on the output of the respective comparison block. The OR gate then provides each of the negated inputs on the AND gates in the alarm, trip and hi-set trip logic functions with a Boolean one (see figures 12, 13, 14). The result is a Boolean zero thereby making the AND gate false. Note that this function is merely to block the differential function from initiating a trip command. Instead, the dedicated under voltage protection elements, as identified in section 5.2 (Operational Considerations), would execute under-voltage protection.

For research and test purposes, the protection function logic is programmed on one relay only, viz. the relay receiving the ‘tap’ voltage measurement. The relay receiving the busbar voltage transformer measurements is programmed to send the measured values to relay ‘tap’ using GOOSE messaging. If the logic is implemented on both relays, an additional ‘check’ is created over and above the essential backup protection typically employed. Here the dV protection outputs could be AND-ed or OR-ed for more reliability.

From another perspective, this also provides the opportunity that ‘actual distributed’ protection is being employed as the voltage measurements received could be sent from any IEC 61850 compliant IED device with voltage measuring elements. Hence platform-based protection is conceptualised.

5.4 Protection Settings

The differential voltage function shall be tested against the parameters of a fuseless single star earthed capacitor bank at Beta substation, South Africa. Therefore, similar setting values are used as applied [20] to the Beta Bank. This demonstrates an actual scenario.

Figure 17 and 18 respectively depict the capacitor unit and per phase bank configuration at Beta substation. The capacitor unit in figure 17 has three parallel elements and nine series elements. The bank (per phase) in figure 18 has six strings of sixteen series capacitor units. This is 144 elements in series per string and 864 elements per phase.

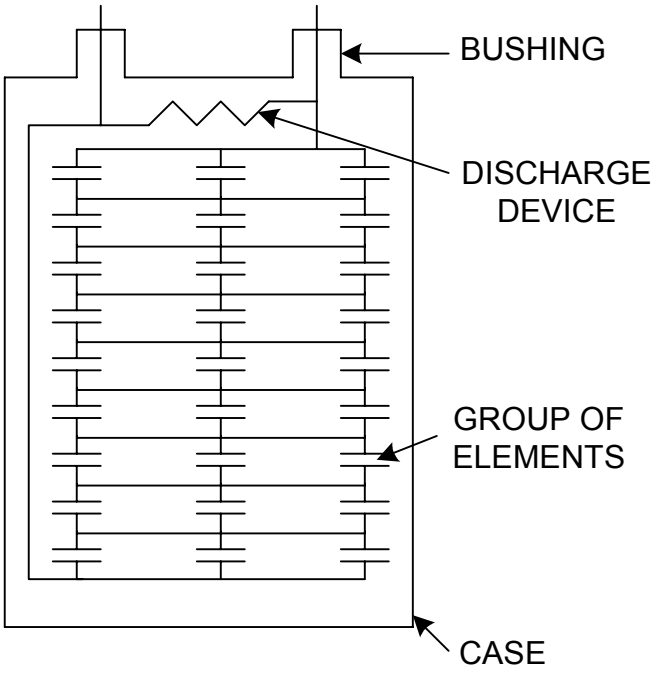


Figure 17, capacitor unit at Beta substation having a 9 by 3 series-parallel set of elements.

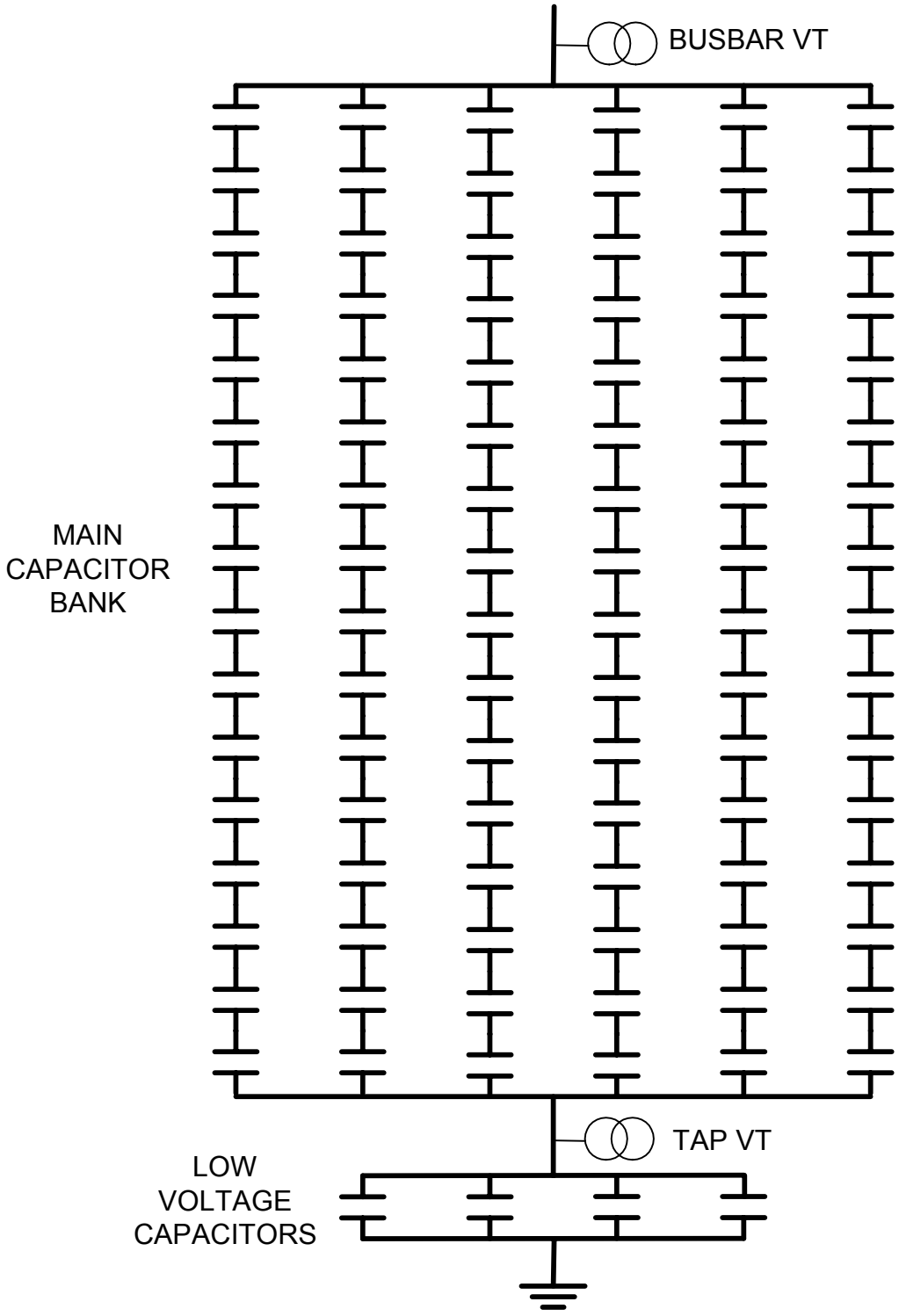


Figure 18, one phase of a capacitor bank at Beta substation having 16 series units and 6 strings.

The settings sheet comprises three main parts:

1. To determine and calculate bank design quantities,
2. To prepare a calculation table that determines the differential voltage (dV) values needed for alarm, trip and Hi-Set thresholds. This shall be in line with capacitor element over voltages of 1.05pu, 1.1pu and ~1.5pu respectively;
3. To specify the limits for voltage and time.

Part 1 – Bank Design Details

Table 2, capacitor bank design rating of Beta substation.

CAPACITOR BANK DETAILS

LOCATION	
Station:	Beta
Circuit:	Bank 1
CAPACITOR BANK (MAIN) CONSTRUCTION DETAILS	
Configuration:	Single star earthed
Fusing method:	Fuseless
Nominal system voltage (kV):	400
MVAr rating:	100
Nominal current (A):	144.34
Number of cap units in series per phase:	16
Number of strings per phase:	6
Number of cap. units per phase:	96
Total cap. units for bank	288
Number of cap. elements in parallel per can:	3
Number of cap. elements in series per can:	9
Number of cap. elements in series per phase	144
CAPACITOR UNIT RATING	
Unit KVAr rating:	451
Unit voltage rating (V):	16448
Unit current rating (A):	27.420
Unit capacitance (μF):	5.306
Unit reactance (Ω):	599.906
Capacitance of the main cap. string (μF):	0.33163
Reactance of a healthy string (Ω):	9598.489
Capacitance per phase of the main cap. (μF):	1.98975
Reactance of a phase of the main cap. (Ω):	1599.748
EARTHING (LV) CAPACITOR RATING	
KVAr rating:	167
Voltage rating (V):	825
Unit capacitance (μF):	781.012
Unit reactance (Ω):	4.076
Number of earthing capacitors in parallel:	4
Total earthing capacitance (μF):	3124.048
Total reactance (Ω):	1.019
FILTER	
Inductance (μH):	1200
Impedance at 50Hz (Ω):	0.377
Resistor (Ω):	no parallel resistor
BANK DESIGN RATINGS	
Design voltage (kV):	455.82
Design factor (p.u.):	1.1396
Design current (A):	164.52
Reactive power at design voltage (MVAr):	129.89
Capacitance of a phase - main & earthing (μF):	1.98848
Reactance of a phase - main & earthing (Ω):	1600.767

The rating values in table 2 can be found by using formulae already presented (refer to Appendix A). Capacitor element and unit quantities can be determined by using figures 17 and 18. Table 2 provides an overview of the capacitor bank electrical and physical quantities. From this, a calculation tool is developed in order to determine the dV setting thresholds. The calculation tool is depicted in table 3.

Part 2 - Determination of dV Setting Thresholds

Table 3, calculation of dV in relation to capacitor element over voltage, adapted [20].

Table used to Determine dV								
No. of failed series elements (n)	**Element OV (p.u.)**	**Over voltage across bank (p.u.)**	**Reactance of healthy string (Ω)**	**Reactance of faulty string (Ω)**	**Total effective reactance per phase (Ω)**	**Dec. in imp. factor**	**Tap VT Sec. (V)**	**dV voltage (V)**
0	1.000	1.050	9598.489	9598.489	1600.125	1.000	66.684	0.000
1	1.007	1.057	9598.489	9531.833	1598.263	1.001	66.762	0.078
2	1.014	1.065	9598.489	9465.176	1596.379	1.002	66.840	0.156
3	1.021	1.072	9598.489	9398.520	1594.472	1.004	66.920	0.236
4	1.029	1.080	9598.489	9331.864	1592.543	1.005	67.001	0.317
5	1.036	1.088	9598.489	9265.208	1590.591	1.006	67.084	0.400
6	1.043	1.096	9598.489	9198.552	1588.616	1.007	67.167	0.483
7	1.051	1.104	9598.489	9131.896	1586.617	1.009	67.252	0.568
8	1.059	1.112	9598.489	9065.239	1584.594	1.010	67.338	0.654
9	1.067	1.120	9598.489	8998.583	1582.545	1.011	67.425	0.741
10	1.075	1.128	9598.489	8931.927	1580.472	1.012	67.513	0.829
11	1.083	1.137	9598.489	8865.271	1578.373	1.014	67.603	0.919
12	1.091	1.145	9598.489	8798.615	1576.248	1.015	67.694	1.010
13	1.099	1.154	9598.489	8731.959	1574.097	1.017	67.787	1.103
14	1.108	1.163	9598.489	8665.302	1571.918	1.018	67.881	1.197
15	1.116	1.172	9598.489	8598.646	1569.712	1.019	67.976	1.292
16	1.125	1.181	9598.489	8531.990	1567.477	1.021	68.073	1.389
17	1.134	1.191	9598.489	8465.334	1565.214	1.022	68.171	1.487
18	1.143	1.200	9598.489	8398.678	1562.922	1.024	68.271	1.587
19	1.152	1.210	9598.489	8332.022	1560.599	1.025	68.373	1.689
20	1.161	1.219	9598.489	8265.365	1558.247	1.027	68.476	1.792
21	1.171	1.229	9598.489	8198.709	1555.863	1.028	68.581	1.897
22	1.180	1.239	9598.489	8132.053	1553.448	1.030	68.688	2.004
23	1.190	1.250	9598.489	8065.397	1551.001	1.032	68.796	2.112
24	1.200	1.260	9598.489	7998.741	1548.520	1.033	68.906	2.222
25	1.210	1.271	9598.489	7932.085	1546.006	1.035	69.018	2.334
26	1.220	1.281	9598.489	7865.428	1543.458	1.037	69.132	2.448
27	1.231	1.292	9598.489	7798.772	1540.875	1.038	69.248	2.564
28	1.241	1.303	9598.489	7732.116	1538.256	1.040	69.366	2.682
29	1.252	1.315	9598.489	7665.460	1535.601	1.042	69.486	2.802
30	1.263	1.326	9598.489	7598.804	1532.909	1.044	69.608	2.924
31	1.274	1.338	9598.489	7532.147	1530.178	1.046	69.732	3.048
32	1.286	1.350	9598.489	7465.491	1527.409	1.048	69.859	3.175
33	1.297	1.362	9598.489	7398.835	1524.601	1.050	69.987	3.303
34	1.309	1.375	9598.489	7332.179	1521.751	1.052	70.118	3.434
35	1.321	1.387	9598.489	7265.523	1518.861	1.054	70.252	3.568
36	1.333	1.400	9598.489	7198.867	1515.928	1.056	70.388	3.704
37	1.346	1.413	9598.489	7132.210	1512.952	1.058	70.526	3.842

Table 3 was created as a design calculation tool. This tool can be applied to other banks to determine the differential voltage resulting from capacitor element failure.

With reference to table 3, the limits for alarm, trip and Hi-Set are calculated as 0.483 mV, 1.103 mV and 3.842 mV respectively are highlighted in yellow. These values relate to ~1.05 pu for six failed series elements, ~1.1 pu for 13 failed series elements, and ~1.35 pu for 37 failed series elements.

The values in each column in table 3 are interpreted in the following way:

"The number of failed series elements" is simply that, the number of failed series elements. Zero failed elements give 1.0 p.u. voltage distributed equally across all elements.

"Element OV (p.u.)" is the voltage across one element. As elements fail, the voltage across the remaining healthy elements re-distributes. This results in a voltage increase per element. These values are calculated by establishing the voltage across one element in a unit according to the rated unit voltage, divided by the number of series elements. Therefore, for one element failure, the new element voltage is calculated for one less element.

"The overvoltage across bank (p.u.)" is the system voltage applied to the bank. 400kV would be 1 p.u. while 420kV would relate to 1.05 p.u. The banks nominal operating voltage is 420kV [20]. As capacitor elements fail, the distributed voltage across the remaining elements increase. The "element OV (p.u.)" for a specific number of failed elements is multiplied with the nominal "overvoltage across bank (p.u.)". This will determine the "overvoltage across bank" at a particular number of failed elements.

"Reactance of healthy string (Ω)" is obtained from table 2.

"Reactance of faulty string (Ω)" is calculated each time for one less element in series.

"Total effective reactance per phase (Ω)" is the overall reactance of the main capacitor bank plus the reactance of the series inductor (no resistor is in parallel). This overall reactance is calculated each time for one less element only.

"Dec. in imp. factor" is a decrease in impedance factor. This is a ratio between the total effective reactance per phase for a healthy phase and the total effective reactance per phase for a particular number of failed elements. This factor is used to determine the voltage rise at the tap point due to element failure.

"Tap VT sec. (V)" is the output secondary voltage measured across the low voltage capacitor. This would normally be $110\sqrt{3}$ volts (~63.5V). However, as the voltage supplied to the bank is 1.05 p.u., the base value for zero failures is 66.68V. The voltage rise at the tap point is calculated by multiplying the "dec. in imp. factor" for a particular number of element failures by the VT tap point base value for zero failures.

"dV voltage (V)" is the differential voltage developed between the busbar VT and the tap point VT as capacitor elements fail. This is determined by subtracting the "tap VT sec." at a particular number of element failures from the base VT tap value for zero failures. Note that the absolute value must be taken as the secondary values for VT tap increases above VT busbar.

Part 3 – Relay Setting Values

Table 4, relay setting sheet for the differential voltage protection function, adapted [20].

Relay Setting Sheet				
Function	**Description**	**Voltage Setting**	**Time Setting**	**Comments**
Kr-A	relay compensation factor for phase A	1.00164	n/a	To be adjusted against site measurement to null measured imbalances. (Kr=Vs/Vt)
Kr-B	relay compensation factor for phase B	1.00164	n/a	
Kr-C	relay compensation factor for phase C	1.00164	n/a	
Alarm A	setting value for alarm on phase A	0.483mV	2 s	Voltage value from table 3, time value ensures actual alarm persists.
Alarm B	setting value for alarm on phase B	0.483mV	2 s	
Alarm C	setting value for alarm on phase C	0.483mV	2 s	
Trip A	setting value for trip on phase A	1.103mV	200 ms	Voltage value from table 3, time value set to cater for harmonic phenomena during switch in.
Trip B	setting value for trip on phase B	1.103mV	200 ms	
Trip C	setting value for trip on phase C	1.103mV	200 ms	
Hi-Set A	setting value for Hi-Set on phase A	3.842mV	100 ms	Voltage value from table 3, time value set to block loss of potential when circuit breaker is manually opened.
Hi-Set B	setting value for Hi-Set on phase B	3.842mV	100 ms	
Hi-Set C	setting value for Hi-Set on phase C	3.842mV	100 ms	
Vs UV A	setting value for loss of potential on Vs phase A	12.7V	n/a	This setting is used to block the differential function due to external line faults. Set to 20% of nominal secondary voltage.
Vs UV B	setting value for loss of potential on Vs phase B	12.7V	n/a	
Vs UV C	setting value for loss of potential on Vs phase C	12.7V	n/a	
Vt UV A	setting value for loss of potential on Vt phase A	27V	n/a	This setting is used to inhibit the differential function when the breaker is open.
Vt UV B	setting value for loss of potential on Vt phase B	27V	n/a	
Vt UV C	setting value for loss of potential on Vt phase C	27V	n/a	

Table 4 concisely illustrates the elements of the differential voltage protection function. The setting values are obtained from table 3. Additional comments are made for each setting. It is important to note the time settings selected. The duration indicates the urgency of the notification or command. The time delays need to be

long enough to ignore system disturbances but fast enough to limit damage to the equipment. Up to 2 seconds is acceptable for alarm notifications while 100 milliseconds are necessary for instantaneous trips.

5.5 Function Testing and Results

The relay setup as per figure 10 (and pictured in Appendix C) is tested with an injection test set, type Omicron 2.56. The following tests were performed:

1. Measuring stability test

This test is performed to determine the lowest stable setting threshold of each of the six voltage input measuring elements for the differential function. The test is performed on one element, say Vt (tap point) phase A, independently with delay timers and hysteresis[1] set to zero. Nominal secondary voltage of 63.5 volts is applied, and the relay compensation factor Kr is set to 1.00164 to balance the dV calculation to zero volts. The compensation factor set shows a 0.164% error generated by the relays, omicron and interconnecting cables.

An iterative method is followed for determining the lowest stable measured value: The alarm setting field is incremented in intervals of 0.01 volts until no pickup is experienced. The tap voltage input (Vt) on phase A is then incremented in steps of 0.01 volts until pickup.

The minimum stable voltage is measured at 0.125 volts. Intermittent pickup results between 0.12 and 0.13 volts. Hysteresis is then applied to obtain a consistent stable pickup. Iteratively, the hysteresis value is worked out to 0.025.

2. Accuracy

This test is performed to determine the accuracy of the relay measuring elements. Setting values calculated for Beta substation are used.

The dV threshold pickup is set to 0.483 volts for the alarm function. The tap voltage input is increased from 0 volts through the range until the function picks up. It was found that the pickup accuracy was consistently between 0.490 volts and 0.520 volts giving an accuracy of ±0.03 volts. The relay display resolution on the relay interface increments in steps of 0.125 volts. Therefore the processing accuracy has better resolution that the display accuracy.

The alarm and trip thresholds are tested to ascertain that the output command is initiated near or before the next expected element failure. The alarm function consistently operated between 0.49 and 0.52 volts. This is below the 7^{th} (next) element failure for dV = 0.57. The trip function consistently operated at 1.11 volts. This is slightly above the 1.103 volt threshold but below the 14^{th} (next) element failure for dV = 1.197 volts.

3. Loss of Potential Block

Loss of potential to any of the voltage inputs must block the dV function from operating. A collapse of the voltage on any of the inputs results in a magnitude

[1] The comparison logic block has a hysteresis setting.

change of dV. This can be simulated by applying zero volts to the relay inputs. The test was performed 10 consecutive times without the relay tripping, however, a failed test occurred randomly when more than 10 tests were done. The reason for this spurious trip is attributed to the definite time required to process the logic. The logic is processed cyclically without interruption. A shorter processing time would aid in mitigating the trip, including giving the Loss of Potential Block command immediate priority. This is addressed under test 8.

4. Phase Error Test

The measured values from the Vs and Vt voltage transformers could introduce a phase error between each other due to their windings. Capacitor element failure results in magnitude change and not a phase angle change on the same phase. A phase error between the two voltage transformer measured values must not cause a trip. Absolute logic blocks are implemented in the dV logic calculation as per figure 11. Therefore the differential protection function is insensitive to phase error. This was also practically proved by introducing a voltage phase shift between the two relays applied on the same phase. For example, Vs phase A = 63.5V, 0° and Vt phase A = 63.5V, 60°.

5. Harmonic Voltage Block

Higher order harmonic voltage magnitudes can be large compared to the magnitude of the fundamental frequency voltage. Second order harmonic occurs upon energising as it is the dominant harmonic on inrush. During system operation, odd harmonics particularly up to the 13^{th} order are problematic, especially the so called 'triple-N' harmonics. These are an odd multiple of three times the fundamental and add in the neutral. The interest here is to block harmonic voltages as they tend to cause spurious trips.

Protection relays generally filter out harmonics in their measuring process. They also can provide 2^{nd} order harmonic inrush restraint. It was found that the relay attenuates the harmonics. If harmonics are present but at the below acceptable limits of ~8% total harmonic distortion for voltage (THDV), the attenuation is sufficient to prevent spurious trips.

However, higher THDV applied could still result in tripping. Harmonic quantities associated with a 6 pulse bridge are injected simultaneously into phase A of relay Vs and Vt to determine the response of dV. Following is a sample characteristic of these harmonics [1]:

- 5^{th} = 22%
- 7^{th} = 10%
- 11^{th} = 8%
- 13^{th} = 6%
- THD = 25.3%

This resulted in the differential function operating and tripping. The Vs measured 63.462 volts and Vt measured 64.002 volts (within 0.125 volts display accuracy). This gave a dV value of 0.54 volts (0.85% increase) which marginally exceeds the trip threshold of 0.483 volts. The interesting result is that the GOOSE message still sent a value of the fundamental frequency to Vt. This can be attributable to a lower sampling frequency of the measured value sent via GOOSE messaging. Additional

filtering techniques may need to be considered to further improve the attenuation on the Vt relay.

It is concluded that provided harmonics are maintained within acceptable limits, the protection function remains stable.

6. Selectivity

This test is performed to ascertain that the three protection functions operate independently. Output commands for each function were masked to LED's. An instantaneous dV = 4 volts test voltage was applied which is above the Hi-Set threshold of 3.84 volts. The sequence of operation was that the Hi-Set operated first, then the normal trip, followed by the alarm initiate command. This proved the selectivity of the function.

7. Reset-ability of the Alarm Function

This test is performed to check that the function resets when a dV value is picked-up. This would occur when the pickup period is shorter than the timer delay setting. The test was done by applying an inclining and declining ramp test voltage above the alarm setting threshold of 0.483 volts, with a width less than the time delay.

This test is performed by allocating an unlatched LED to illuminate when the setting threshold is exceeded. Another LED, but latch configured, is allocated should the alarm-out command be initiated thus indicating a definite step change after 2 seconds. A nominal 1 second ramp width was applied and the test passed.

8. Logic Processing Duration

The processing time of the implemented logic was measured to be of the order 396ms and the time to initiate a trip to the circuit breaker contact was measured to be 15ms.

Dedicated protection functions initiate commands from the time of pickup in 50-60ms. Therefore in comparison, 396ms can be considered too long. This processing time is dependant on the speed of the PLC class. The relay used for this investigation has four PLC classes: Interlocking (cyclic processing), measurement (cyclic processing), slow PLC (priority driven) and fast PLC (priority driven). Due to memory constraints, not all the logic blocks can be allocated to the fast PLC. This would be the ideal situation as the fast PLC has a processing time of 10ms. Also it was established that some logic blocks operate only in the fast PLC (e.g. timers) and some prefer to be processed in the measuring PLC (e.g. measured values and set point blocks).

It can be argued that the alarm function may only need to operate after a 2-10 second delay thereby eliminating the need for faster processing. However, the trip and Hi-Set commands should operate in a time closer to 60ms, or at least below 100ms which is the delay time applied to the Hi-Set function. Delay times are specified independently of the processing times for relay applications. In addition, it could be argued that capacitors have a design rating of 1.5 p.u. for 8 seconds, and therefore 396ms could be considered acceptable [6].

Ultimately the need for fast tripping is required in order to limit damage to the primary plant equipment. Therefore it is proposed that an iterative process of re-evaluating, further optimising and re-organising the logic function, so to improve the processing

time. However, this may not be enough. The memory size allocation for each PLC class and the logic block exclusivity may need to be reviewed by the manufacturer. It must be noted that different suppliers will have different methods of programming logic functions and masking their inputs and outputs. This would need to be assessed before implementation.

5.6 Discussion of Outcomes

The following recommendations are made based on the results of this protection function application:

The tests show that the function is stable. The lowest stable measured value is 0.125 volts which is 3.8 times lower than the tested alarm setting for Beta Substation shunt capacitor bank. The relay function is accurate to within 0.03 volts. The setting values for alarm, trip and Hi-set were picked-up before the next element failure. Therefore the function is accurate within one element failure.

The differential relay function did not operate for 10 consecutive tests when a Loss of Potential is experienced on any of the phases. However, spurious trips did occur. A priority driven PLC class would render the Loss of Potential block function reliable. The differential protection function is immune to phase error by virtue of taking the absolute value of dV. Therefore the voltage phase angle is not considered in the alarm and trip algorithms.

A simple test was performed to check reset-ability. The delay timer used in the logic proved to function as expected. Should the alarm or protection pickup not remain high (Boolean one) until after the timer has timed-out, the protection function resets the timer.

The harmonic block is sufficient for acceptable levels of total harmonic distortion. However, further analysis on the inherent filtering of the relay not excluding programmable measures, in order to further attenuate the measured harmonics. Albeit, a 0.8% voltage change in dV, over a 25.3% THDV is near negligible. This short coming is attributed to the sensitivity requirement of the protection function. Also, the virtually created voltage differential protection element created in the PLC logic does not have a selectable fundamental frequency filtering option as do the pre-defined built-in protection functions like over-current etc. It is recommended that this filter feature be further investigated.

The availability of the function has proved itself as the function is always ready to operate, although over-operatability or at least spurious tripping has occurred. This is attributed to the processing time and the cyclic (non-priority) driven PLC class where the bulk of the logic functions reside. Therefore, further investigation is required to optimise the processing time of the logic functions, such that the speed of processing can be reduced to below 100ms. Also, a priority driven PLC class should be preferred.

The function has proved to be selective with each operation (alarm, trip, Hi-Set) operating independently of each other. The function as yet has not proved to be reliable. Improvement in processing time to under 100ms, utilisation of a priority driven PLC class, and the improvement of harmonic attenuation to below 8% in 12 pulse applications would render the function reliable. Full network testing on a power simulator and type testing according to IEC standards would move this protection application into commercial operation.

5.7 Future Recommendations

Looking at future prospects, the distributed intelligence and the power of customisable Programmable Logic Control could be further exploited. For instance, with regards to capacitor bank protection, moving away from voltage or current threshold limits to counting the number of element failures. With reference to the unbalance protection discussion in sections 4.4, 4.5, and 4.6, by explicitly counting the element failures due to step changes in current, one is able to determine exactly the total number of failed elements. The protection would move away from a voltage threshold setting to a discrete setting defined by the number of actual element failures. This would prevent ambiguous measurements when lower than expected current flows through the H-bridge configuration. Another prospect is to use the logic to calculate unmeasured values. For example, when voltage transformers are not available or not installed, the voltage can be determined by calculation from the measured line current. That is:

$$V = \frac{1}{C}\int Idt \quad \text{..... (16)}$$

Where,
V = the capacitor voltage
C = bank or branch capacitance
I = the measured line current

The calculated voltage value can be used for monitoring over voltage stress of the capacitors across a string, branch or the entire bank. This is possible if a current measurement is available at the location of interest.

It is recommended that the function be tested on a power simulator. Details on the operating characteristics, and further areas for optimisation could be determined. Ultimately, the function would need to be independently tested according to the relevant international standards.

Finally, this implementation would be more cost affective than current supplied applications. The two multifunction relays used would be able to perform the other general protection, restricted earth fault and breaker failure protection functions with its dedicated protection elements. This would result in fewer relays than normally used in shunt capacitor bank scheme. There will also be a direct impact on factory assembly and testing costs, and the onsite commissioning costs. Fewer hours would be needed to perform these tasks compared to currently supplied capacitor bank schemes.

6 Conclusion

This research paper has explored the principles of reactive power compensation and the protection methodology of shunt capacitor banks. A discussion on the application of shunt capacitor banks and their location showed that an installed mix of supply side and load side is preferred. The basics of capacitors were presented together with relevant formulae. Design, manufacturing, losses and testing of power capacitors were investigated in detail. The application and performance of internally and externally fused capacitors; and fuseless capacitor technology was discussed.

Capacitor bank configurations of Single Star, Single Star H-Configuration, Double-Star and C-Filter Configuration were presented. A detailed analysis of the protection philosophies was demonstrated. In particularly, general protection functions, restricted earth fault, breaker failure and unbalance protection was explained.

A novel approach to a differential voltage protection function specifically for fuseless single star earthed shunt capacitor banks was presented. This function approaches protection from a different perspective. Distributed protection or platform-based protection is explored.

Two multifunction protection relays communicated via a 100 Mbit/s Ethernet bus (IEC 61850 protocol). Voltages measured at two points across a capacitor bank were sent to each relay respectively. The measurements received by each device were then shared between each other via the communication link. The programmed algorithm in each relay compared the two measured values taken across the bank to determine bank unbalance. The unbalance would be due to capacitor element failure or internal bank faults. The logic that was implemented in the relay satisfied the differential relationship between the two voltage measurements, including logic to initiate an alarm, trip and Hi-Set trip. The alarm notifications and trip commands were initiated via the relay system port and the LED's on the front panel.

A setting sheet calculation tool was developed. The setting sheet provides information on the overall capacitor bank design, a calculation tool for determining the differential voltage due to capacitor element failures, and a relay setting sheet used to set the voltage and time delay thresholds.

A set of tests was undertaken to establish the:

- Stability of the protection elements.
- Accuracy of the measuring elements.
- Selectivity of the function. The alarm, trip and Hi-Set were found to operate independently of each other.
- Loss of potential blocking. The relay function is insensitive to manual switching and system voltage collapse. Response to Loss of Potential is undertaken by dedicated/built-in under-voltage protection elements.
- Harmonic voltage attenuation. Attenuated when THDV is below 8%.
- Processing time of the logic functions is approximately 396ms. This requires further investigation and optimisation.
- Function proved to be reset-able.

This application would provide a simpler and more cost affective solution as it reduces the number of required IED's and the number of expected hours to assemble, test and commission. It is recommended that the processing time be further investigated and optimised. It is also recommended that a priority driven PLC class is used. Implementation is dependent on each supplier's device. It would be beneficial to test the function on a power simulator.

References

[1] Power Quality Application Guide, Copper Development Association, United Kingdom, http://www.cda.org.uk, last accessed October 2008.

[2] D.C. Giancoli, Physics for scientists and engineers, 2nd edition, Prentice-Hall, 1988.

[3] Westing Corp. Power Capacitor Factory, Centurion, South Africa, Factory visit 2 July 2008.

[4] J.E. Harder, Power capacitor construction capability and protection, Westing House Electric Corporation, Indiana, Presented at the Northern California Municipal Electrical Association, March 5 1981, revised 1985.

[5] The plain facts about capacitor losses, Westinghouse Electric Corporation, Transmission & distribution components division, Bloomington, Indiana, USA (an information brochure).

[6] IEC 60871-1, Shunt capacitors for a.c. power systems having a rated voltage above 1000V – part 1: General, Third edition, July 2005.

[7] E. Schweitzer, J. Schafman, Unified shunt capacitor bank control and protection, 45th annual Georgia Tech protective relaying conference, Atlanta, George, May 1-3, 1991.

[8] G. Brunello, B. Kasztenny, C. Wester, Shunt capacitor bank fundamentals and protection, Conference for protective relay engineers, Texas A&M University, April 8-10, 2003.

[9] M.S. Dhillon, D.A. Tzouvaras, Protection of fuseless capacitor banks using digital relays, SEL, USA, Technical Report, 1998.

[10] J.A. Zulaski, Shunt capacitor Bank protection methods, IEEE transactions on power apparatus and systems, Vol. PAS-101, p. 1305-1312, June 1982.

[11] S.W. Chichanowski, G.R. Newcomb, Power capacitors, Electrical electronics insulation conference, 1991, p. 162-165.

[12] Technical Instruction – Monitoring of unbalance current condition in high voltage capacitor banks, Revision 0, Eskom Transmission, South Africa, 1 August 2006.

[13] Protection philosophy: Shunt capacitor banks, Eskom distribution standard SCSASABA5 Revision 0, South Africa, February 2001.

[14] R. Horton, T. Warren (Alabama Power Company), T. Day, J. McCall, A. Chaudhary (Cooper Power Systems), Relaying 230kV 100MVAR C-Filter Capacitor Banks, Cooper Power Systems Inc, Wyoming, USA, Builletin 03019, June 2003.

[15] Multifunction protection 7SJ62 relay manual, Version 4.1, Siemens AG.

[16] Master trace file 0.52/30061 panel type 4CB2300, Revision 14 June 2007, Eskom Transmission, Simmerpan, South Africa.

[17] Master trace file 0.52/30062 panel type 4CB2400, Revision 7 June 2007, Eskom Transmission, Simmerpan, South Africa.

[18] Master trace file 0.52/30060 panel type 4CB2600, Revision 7 June 2007, Eskom Transmission, Simmerpan, South Africa.

[19] Master trace file 0.52/30063 panel type C-Filter H-Configuration, Revision 7 June 2007, Eskom Transmission, Simmerpan, South Africa.

[20] Protection settings, Beta substation shunt capacitor bank 1, Revision 1, Eskom Transmission, South Africa, 22 February 2008.

Bibliography

- Power Quality Application Guide, Copper Development Association, United Kingdom, http://www.cda.org.uk, last accessed October 2008.

- D.C. Giancoli, Physics for scientists and engineers, 2nd edition, Prentice-Hall, 1988.

- Richards, Sears, Wehr, Zemansky, Modern university physics, Addison-Wesley Publishing Co. Inc., March 1964.

Appendix

A. List of Formulae

$X_L = 2\pi fL$ ……. (1) 3

$X_C = \frac{1}{2\pi fC}$ ……. (2) 3

$f_0 = \frac{1}{2\pi\sqrt{LC}}$ ……. (3) 3

$\sin^2(\omega t) + \cos^2(\omega t) = 1$ ……. (4) 3

$C = \frac{Q}{V}$ ……. (5) 5

$C = K\varepsilon_0 \frac{A}{d}$ ……. (6) 5

$K = \frac{\varepsilon}{\varepsilon_0}$ ……. (7) 5

$E = \frac{\sigma}{\varepsilon}$ ……. (8) 5

$V = E.d$ ……. (9) 5

$\oint \overline{E} \cdot d\overline{A} = \frac{Q}{\varepsilon_0}$ ……. (10) 6

$Watts/kVAr = \frac{\pi PfLC}{3WN^2} x10^{-3}$ ……. (11) 8

$I_{line} = \frac{Q}{\sqrt{3}.V}$ ……. (12) 12

$\frac{\delta U}{U} \approx \frac{Q}{S}$ ……. (13) 12

$\hat{I}_s = I_N \sqrt{\frac{2S}{Q}}$ ……. (14) 12

$\Delta V = V_S - K_r \cdot V_T$ ……. (15) 23

$V = \frac{1}{C}\int Idt$ ……. (16) 42

B. Moving Towards Distributed Protection (Overview of IEC 61850)

This application of protection provides the following advantages:

- The two relays can also be used for other protection functions for the bank as a whole, including high-set instantaneous and definite time overvoltage, over current and earth fault protection, thermal overload, and breaker-failure protection – thereby reducing the number of required Intelligent Electronic Devices (IED's); easier engineering, production and commissioning; as well as all the associated cost.
- The implementation of Ethernet communications with IEC 61850 lends itself to all the advantages of this protocol such as:
    - Distributed intelligence i.e. no classic mater/slave configuration which result in "bottle necks".
    - Support for all substation automation functions (control, protection, monitoring).
    - Interoperability (different vendor IED's are compatible and can exchange information).
    - Interchangeability (replace one vendor IED with another vendor IED). Because functions, e.g. protection and measurement, remain vendor specific while the data exchange is standardized.
    - Future-proof architecture for easy extendibility.
    - Optimization of system architecture is possible (scalable).
    - Use of a 100 Mbits/s Ethernet bus with either electrical RJ45 or Fibre Optic interface medium.
    - Engineering and maintenance done by a standardized System Configuration Language (SCL).

C. Relay and Test Equipment Setup

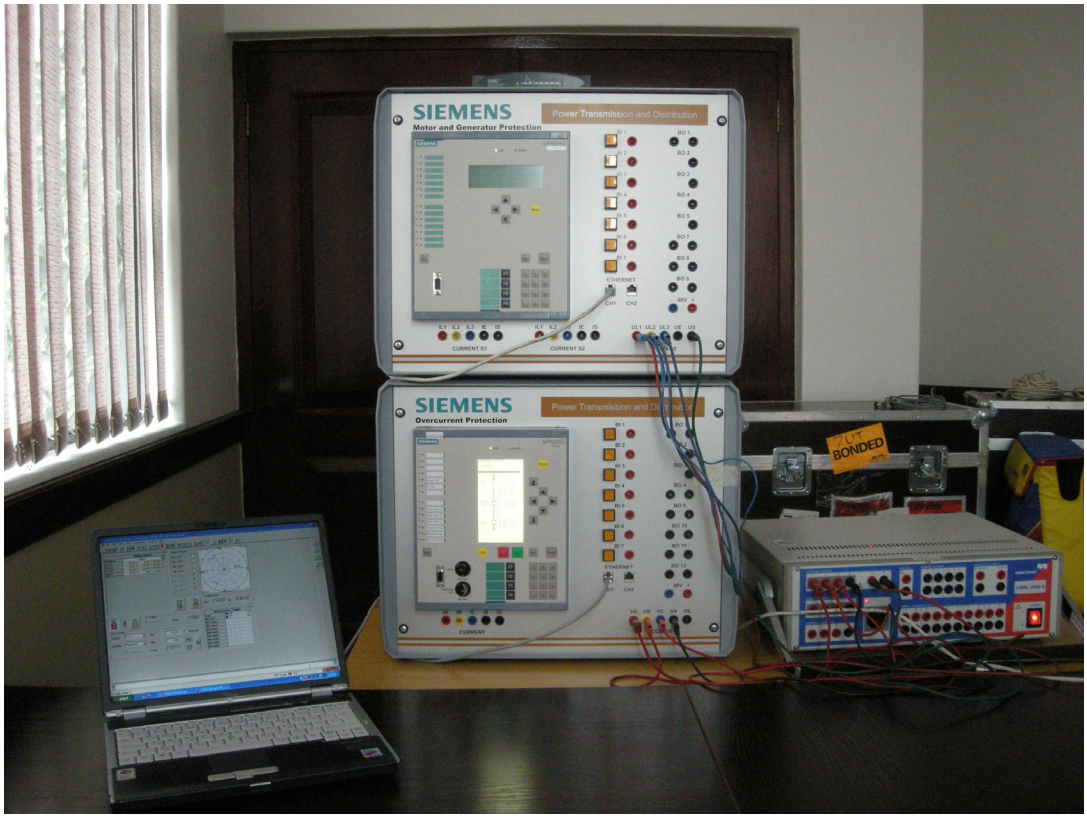


Figure 19, Photo of the relay and test equipment setup.

The above photo shows the two multifunction protection relays (Siemens type) used to implement and test the function. The top relay measures voltage from the busbar, and the bottom relay measures voltages at the low voltage capacitor point. To the right is injection test set (Omicron 256-6) used to test the differential voltage protection function. To the left is the computer used to program the logic on the relay and control the test set. All four components are connected and communicate through the Ethernet switch which is located on top of the relay boxes.

D. Relay mimic and annunciation panel

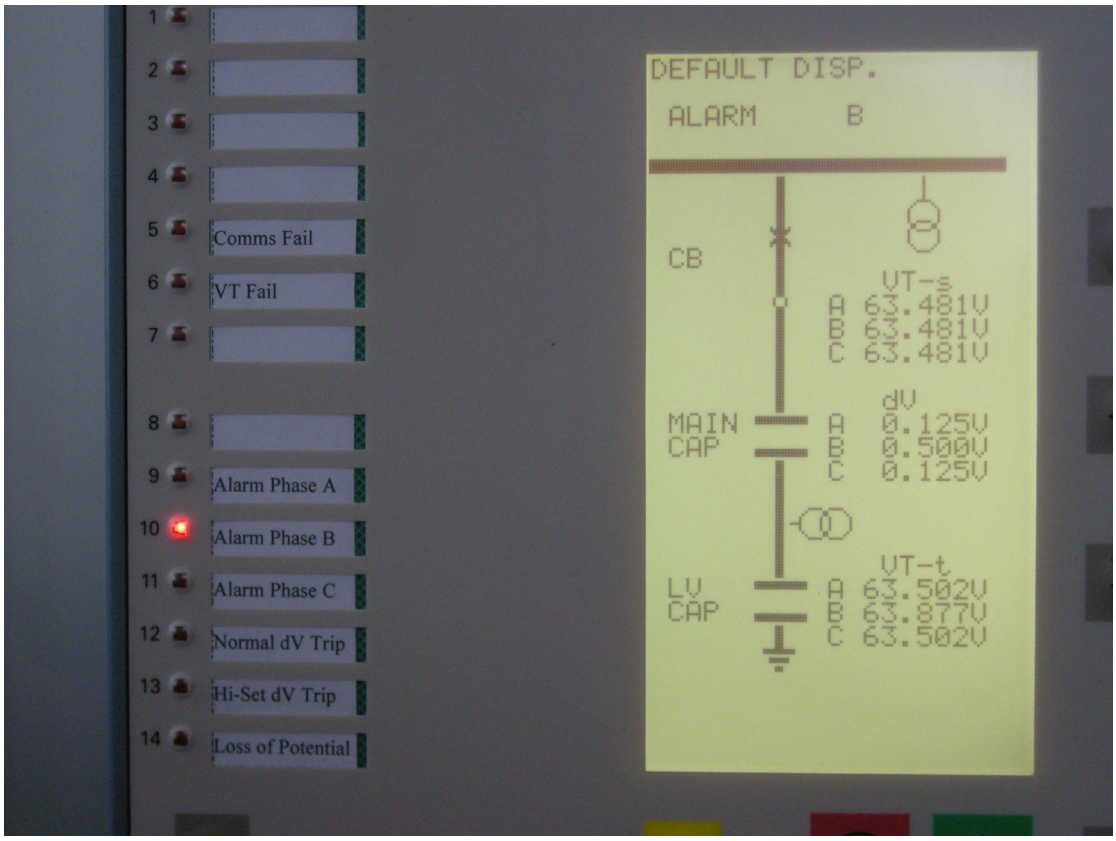
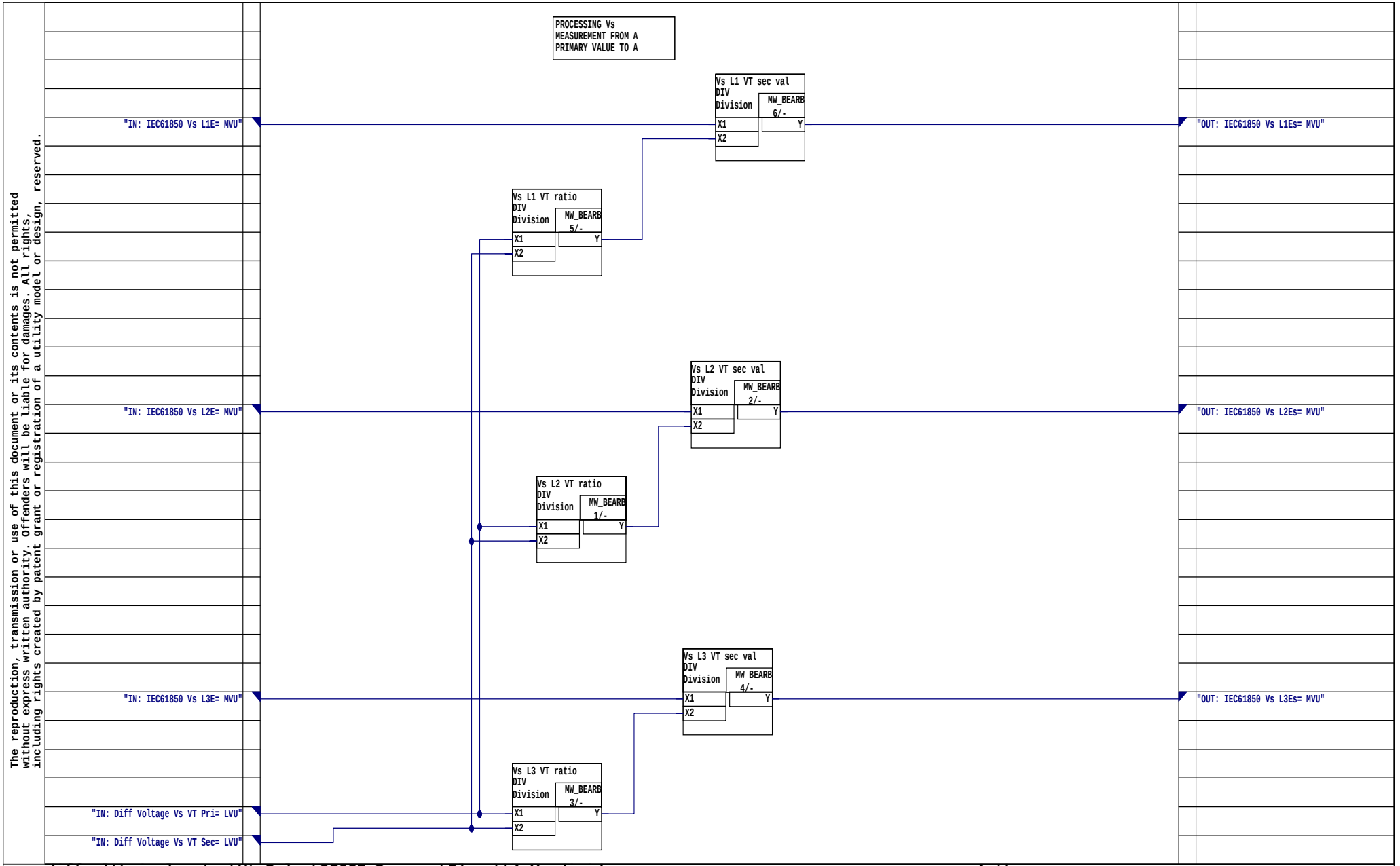


Figure 20, Close up photo of the relay mimic display and annunciation panel.

The relay mimic is programmed to illustrate a single star earthed capacitor bank. The two voltage transformers, busbar and circuit breaker are also shown. The circuit breaker on the mimic is also masked to the binary inputs and outputs to function under real application.

The mimic displays the measurements received via GOOSE messaging from the busbar VT relay (Vs), the measurements obtained from the tap voltage transformer (Vt), as well as the differential voltage (dV). Should an alarm command be initiated, this is also mapped to the display and would be located at the top in line with the word “alarm”. To the left are the LED’s. All the functions are also masked to the LED’s as depicted by their labels.

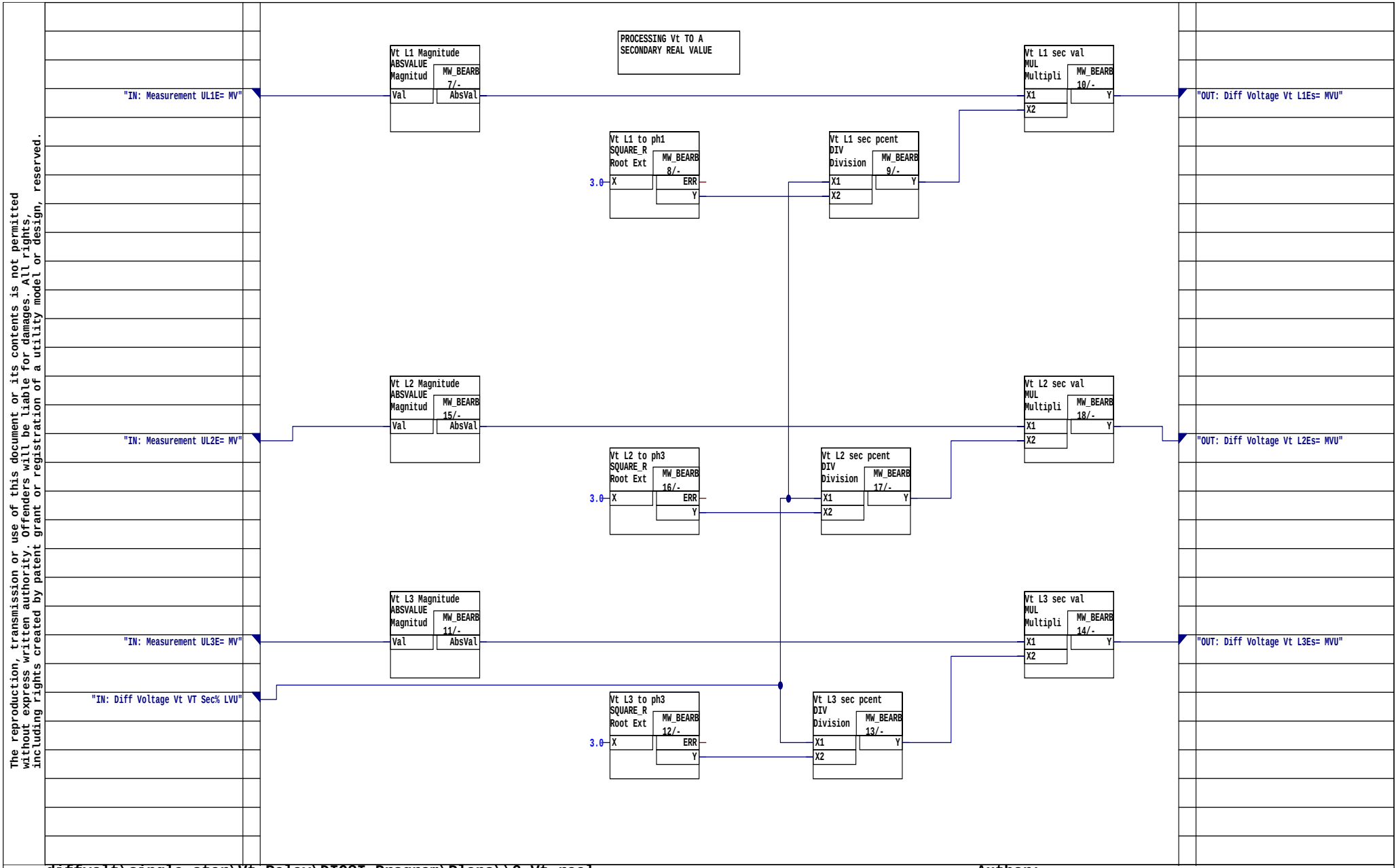
E. Continuous Flow Charts as Implemented on the Relay



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\1_Vs divide

Partit.: A Sh.: 1

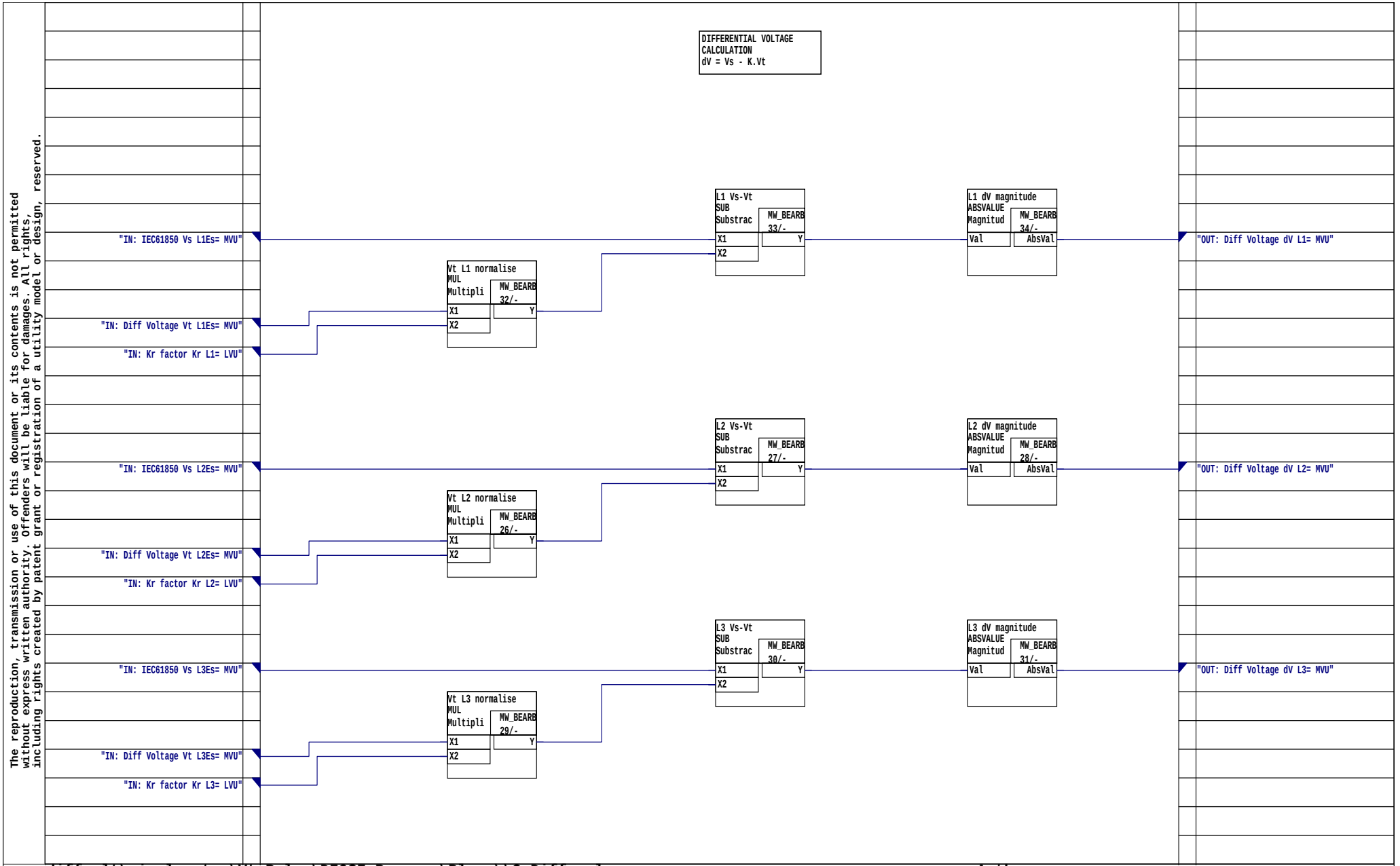
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\2_Vt real

Partit.: A Sh.: 1

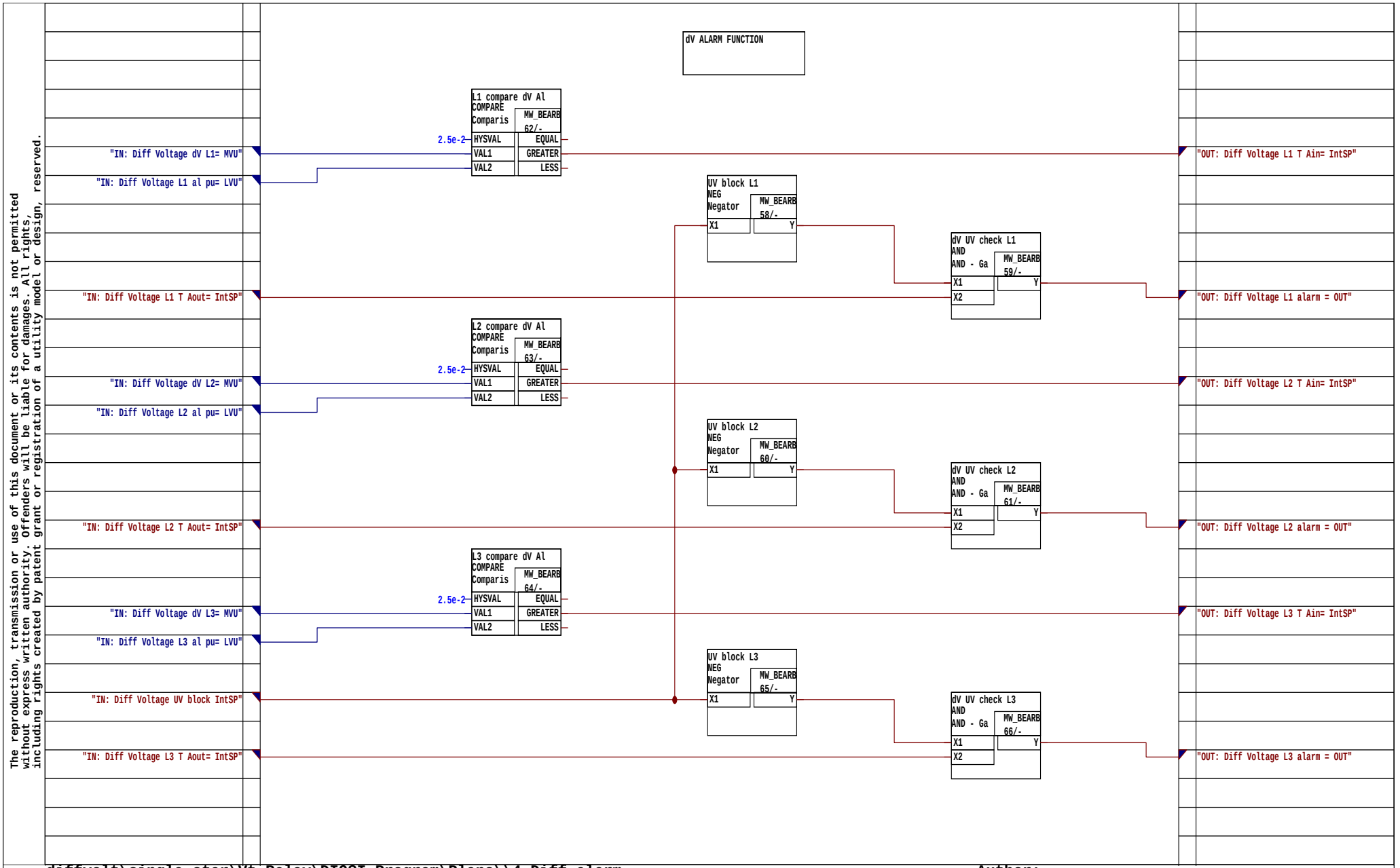
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\3_Diff calc

Partit.: A Sh.: 1

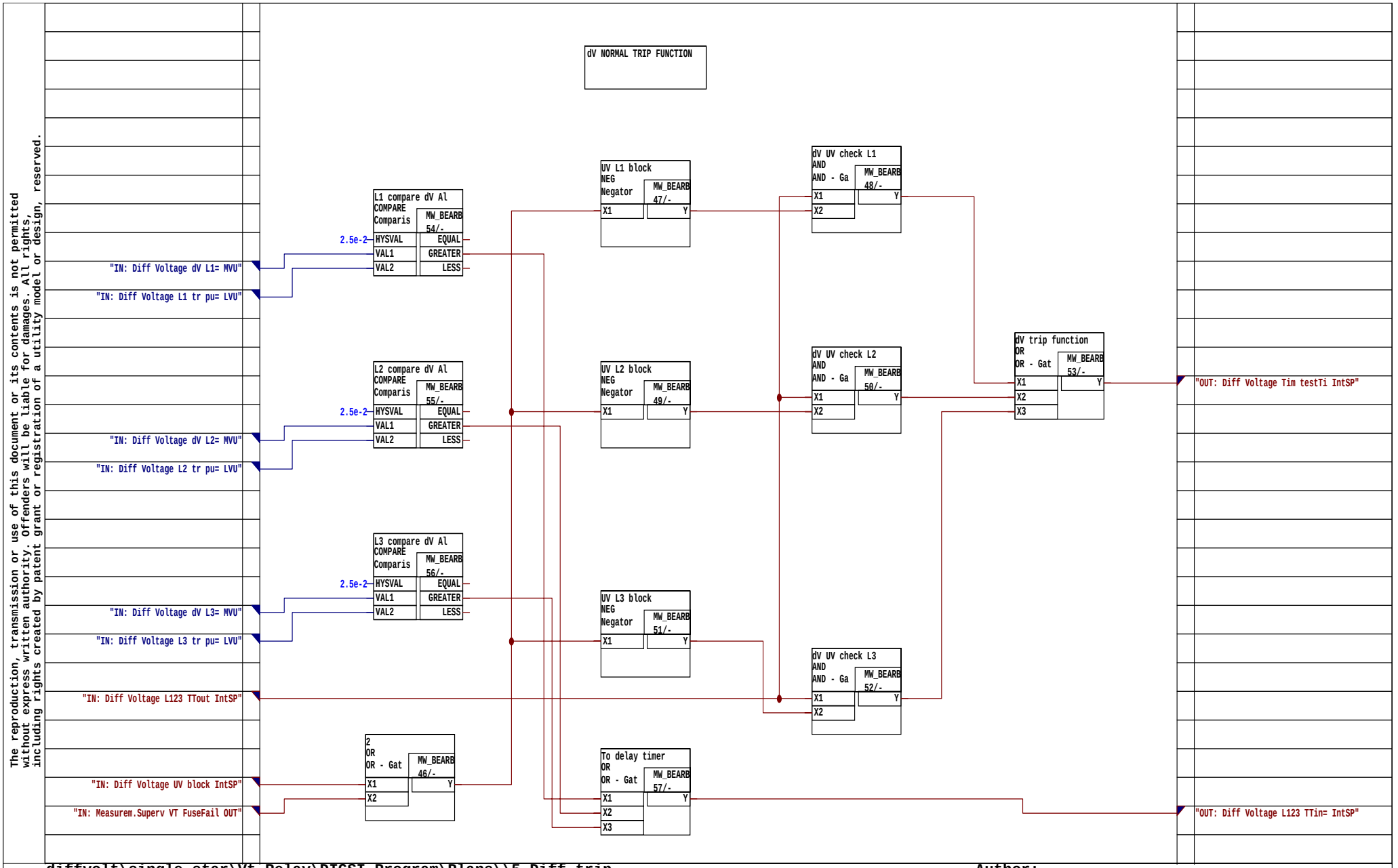
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\4_Diff alarm

Partit.: A Sh.: 1

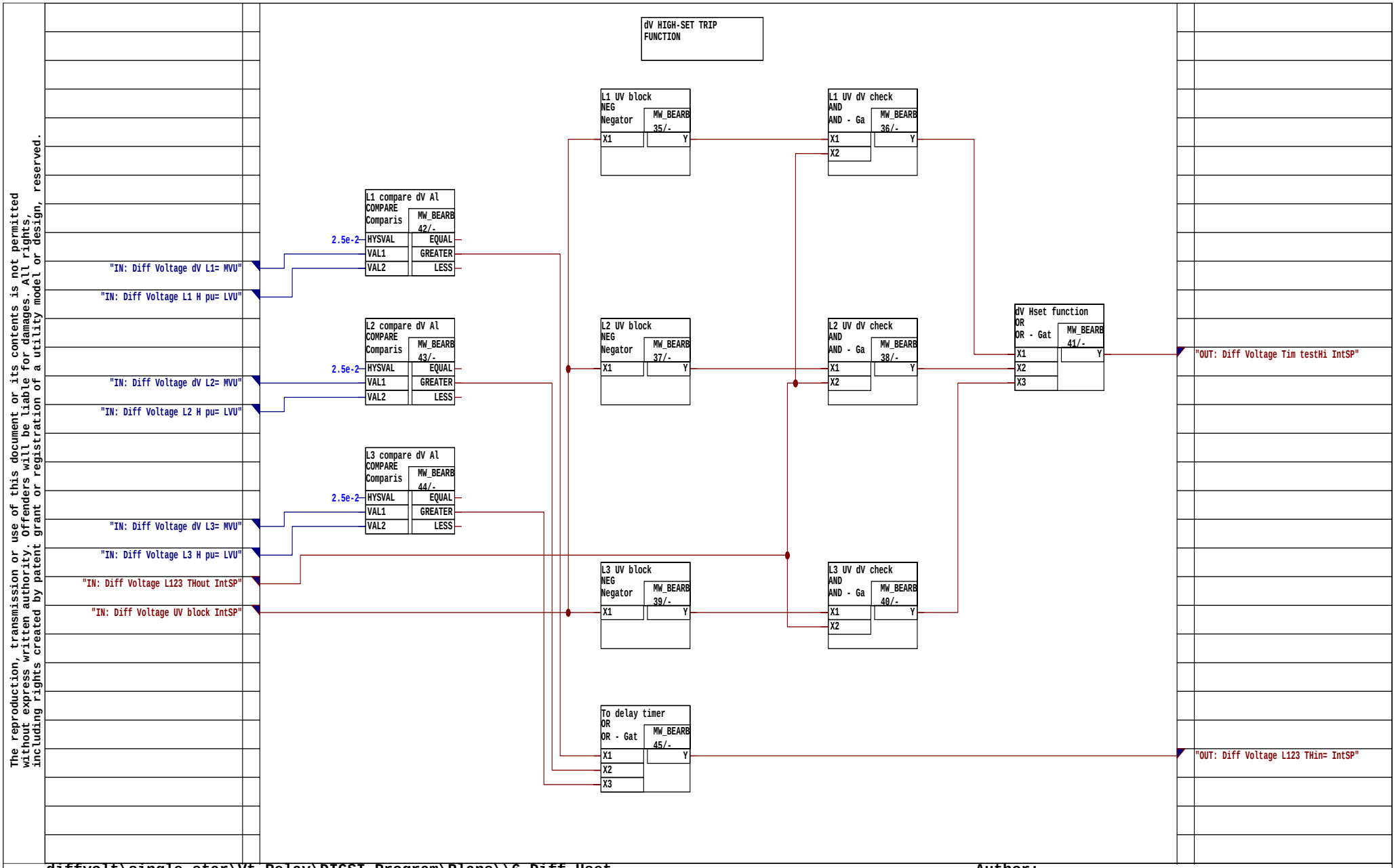
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\5_Diff trip

Partit.: A Sh.: 1

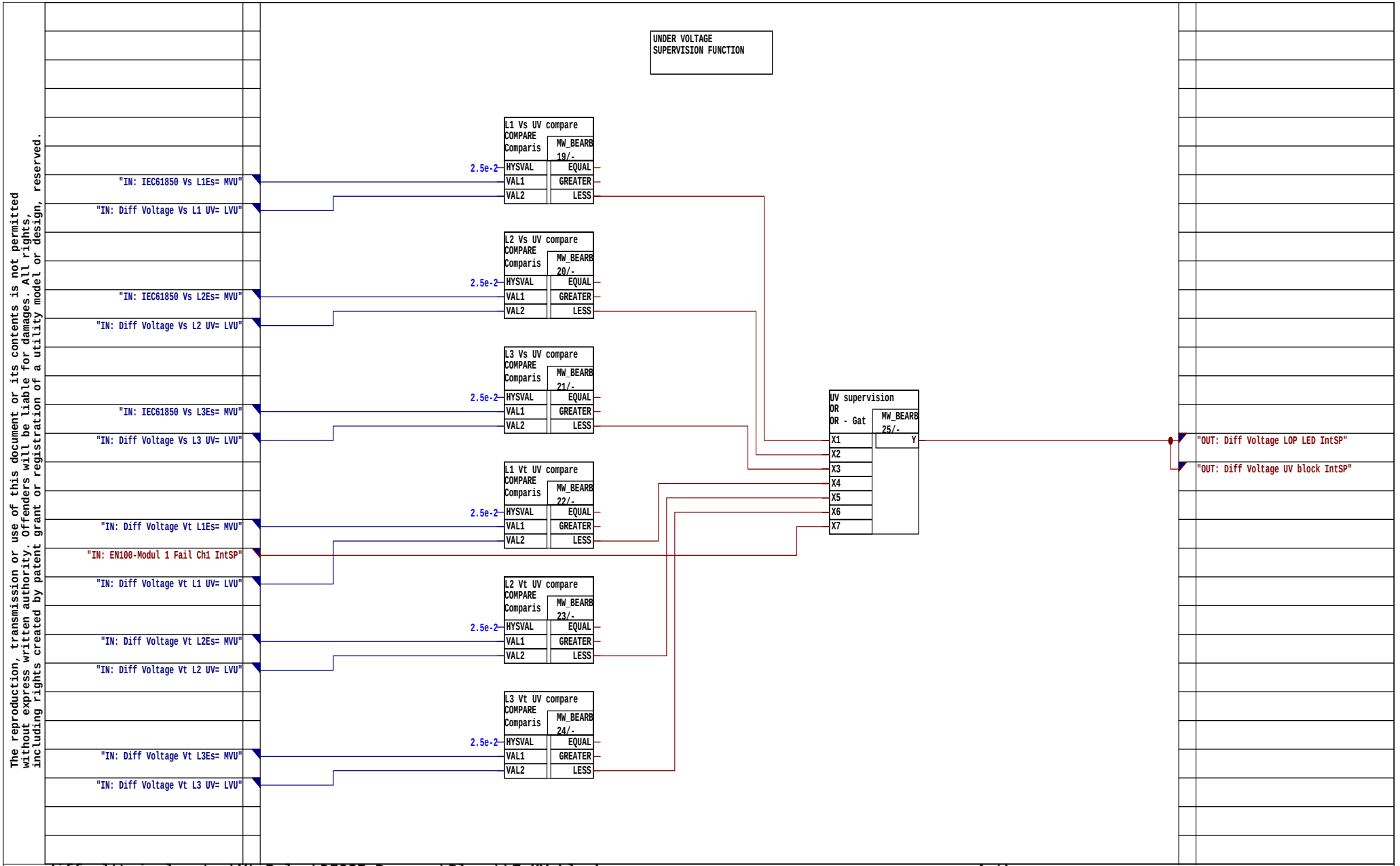
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\6_Diff Hset

Partit.: A Sh.: 1

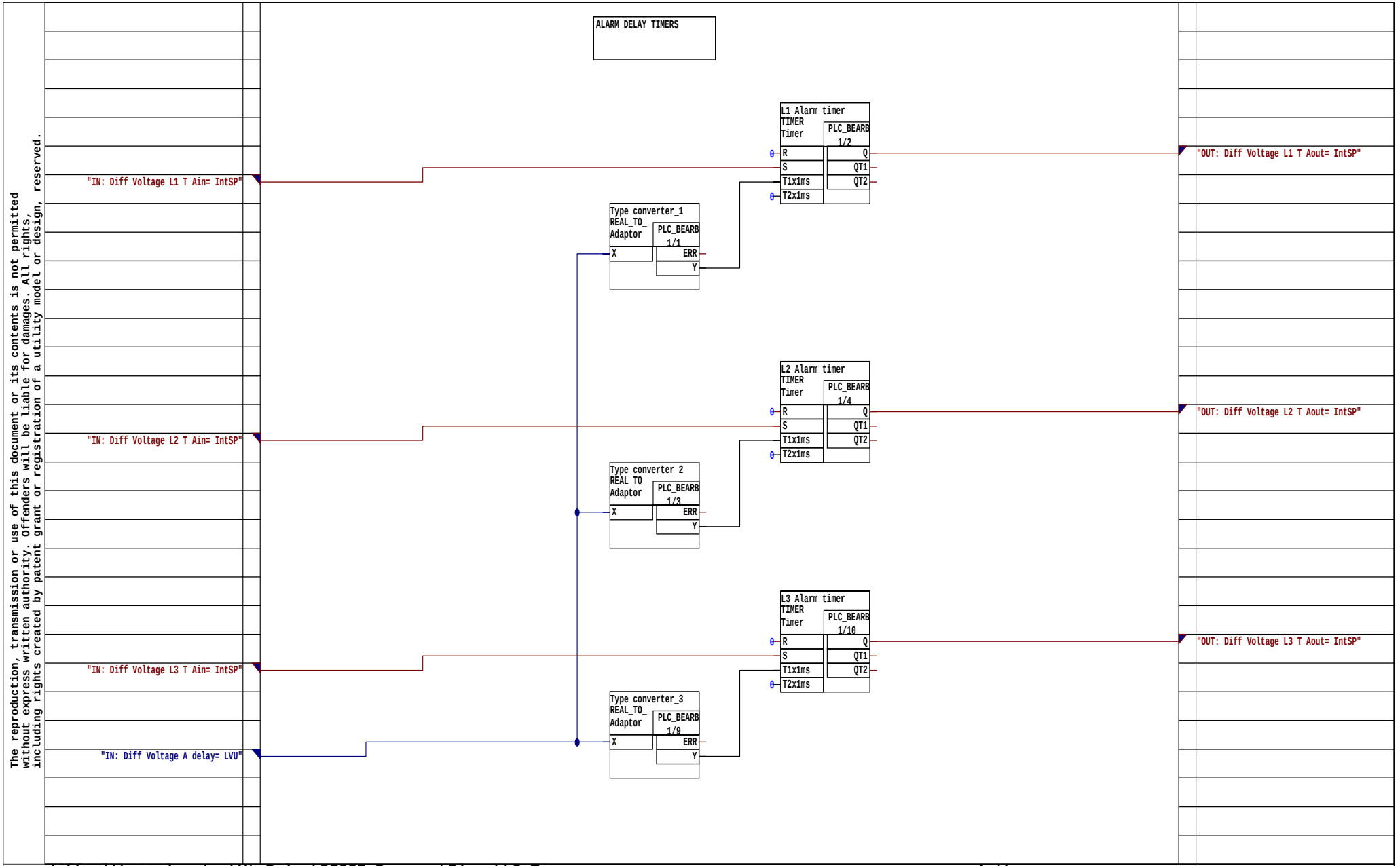
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 15:04
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\7_UV block

Partit.: A Sh.: 1

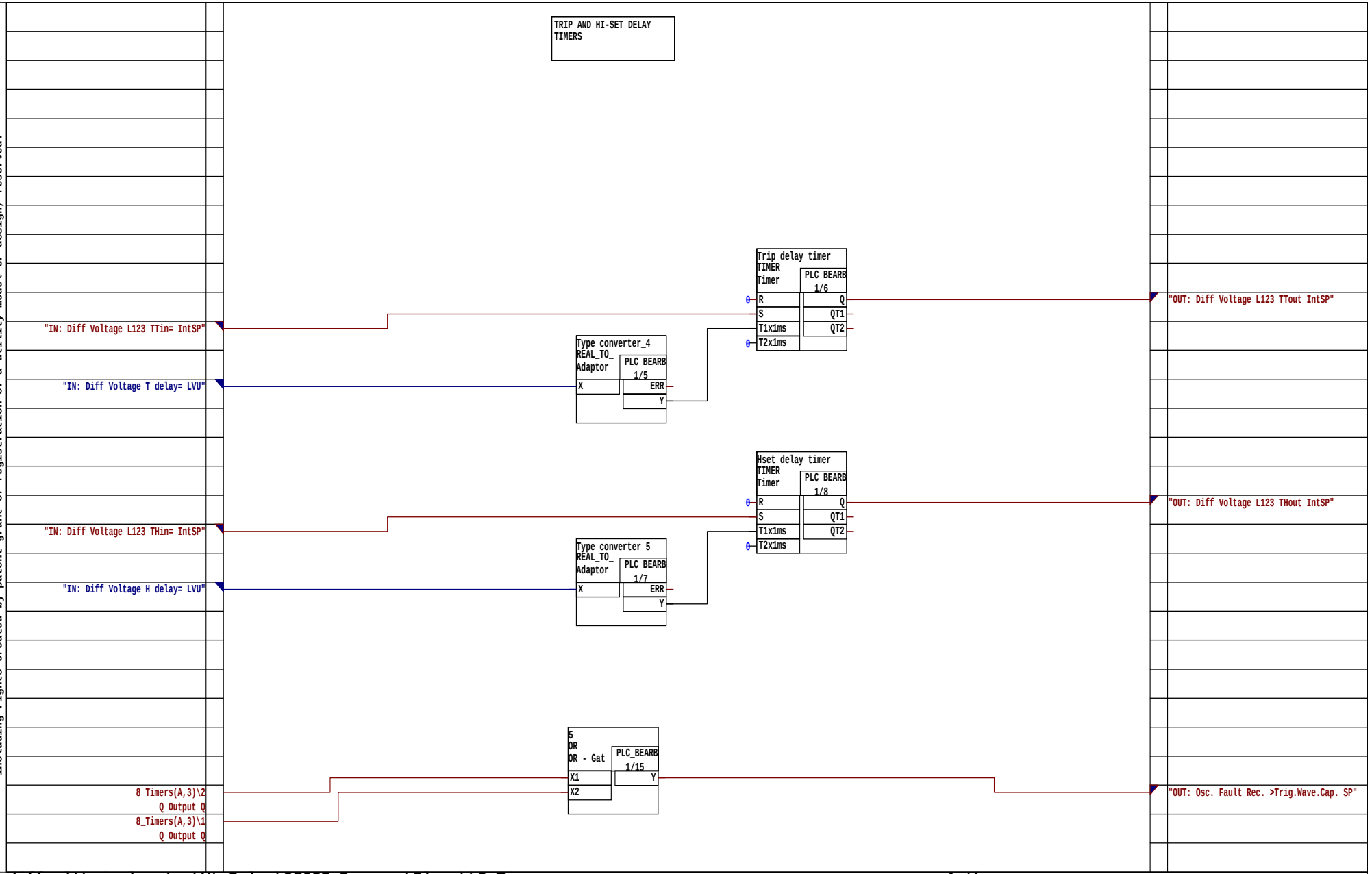
Author:
Created on:: 12/10/2008 18:33
Last change: 20/10/2008 11:34
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\8_Timers

Partit.: A Sh.: 1

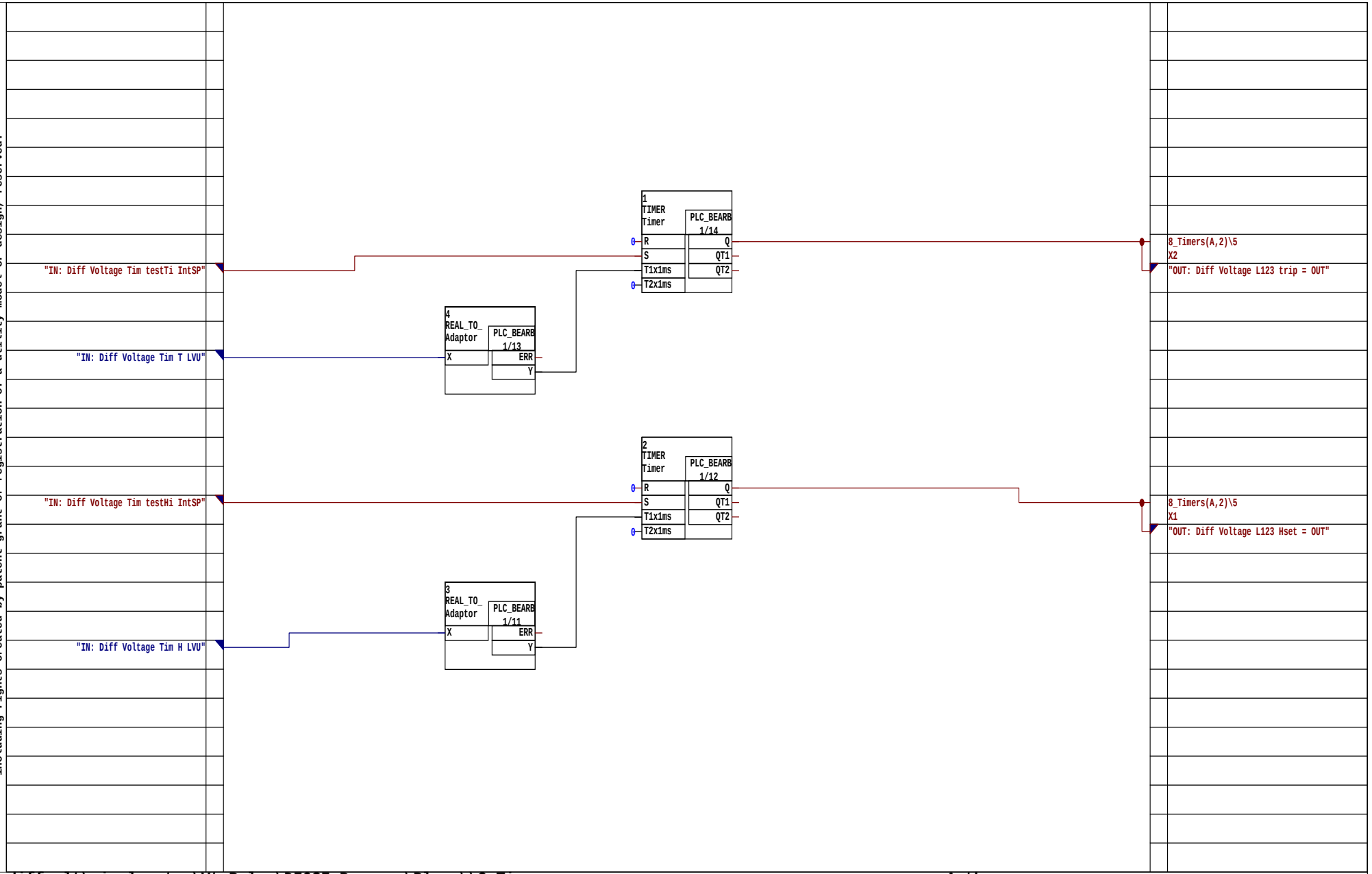
Author:
Created on:: 12/10/2008 19:34
Last change: 20/10/2008 15:04
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\8_Timers

Partit.: A Sh.: 2

Author:
Created on:: 12/10/2008 19:34
Last change: 20/10/2008 15:04
Number of pages: 1



diffvolt\single star\Vt Relay\DIGSI Program\Plans\\8_Timers

Partit.: A Sh.: 3

Author:
Created on:: 12/10/2008 19:34
Last change: 20/10/2008 15:04
Number of pages: 1