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# Power quality analysis of variable speed drives

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University of the Witwatersrand

Masters Dissertation

# Power Quality Analysis of Variable Speed Drives

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*A dissertation submitted in fulfilment of the requirements for the degree of Masters in Electrical Engineering*

*in the*

School of Electrical and Information Engineering

June 2014

# Declaration of Authorship

I, Amit Abraham, declare that this dissertation titled, 'Power Quality Analysis of Variable Speed Drives' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this dissertation has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this dissertation is entirely my own work.
- I have acknowledged all main sources of help.
- Where the dissertation is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

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*"Little by little, a little becomes a lot."*

Tanzanian Proverb

UNIVERSITY OF THE WITWATERSRAND

# *Abstract*

School of Electrical and Information Engineering

Masters in Electrical Engineering

**Power Quality Analysis of Variable Speed Drives**

by Amit Abraham

A study was conducted to evaluate the effects of harmonics generated by Variable Speed Drives (VSDs). A VSD with a technology known as Reduced Harmonics Technology (RHT) was considered and benchmarked against existing solutions in industry in terms of cost and effectiveness. The RHT VSD, like the standard VSD, uses a three phase rectifier but with significantly lower DC bus capacitor banks and an advanced motor control processor. Simulation results reveal that the RHT VSD model produced current harmonics of approximately 30% when compared to a standard VSD, without any additional mitigation solutions, produced current harmonics above 100%.

The RHT VSD was also found to be less expensive than the equivalent rated standard VSD. Laboratory experiments reveal that the input current of the RHT VSD and the standard VSD are similar to the input current waveforms from the simulation of the RHT VSD and the standard VSD respectively. Simulation of the DC bus capacitance and the source impedance reveal that in a lower range of DC capacitance values (below $C1 = 600\mu$F), the size of the DC bus capacitance has more effect on the input harmonics than the source impedance. An increase in source impedance does not reduce input harmonics. In the above mentioned range of capacitance values, it was noted that, the DC bus capacitance dominate the source impedance in its ability to reduce input harmonics. When the DC capacitance was increased above $C1 = 600\mu$F, the source impedance has more effect on the input harmonics than the size of the DC bus capacitance.

The simulation and experimental results show that there are higher order (above 13th order) harmonic frequency components appearing at the input of the RHT VSD when compared to a standard VSD. It is clear that there is a trade off, due to the effect of the motor control processor, between there being reduced harmonics at the lower orders (below 13th order) and there being an increase in harmonics at higher orders (above 13th order). It was also noted from the experiment that there is no notable difference in the harmonic content at the outputs of the two VSDs.

# *Acknowledgements*

I would like to thank my supervisor, Prof W. A. Cronje for his advice and guidance. For opening my mind to the variety of questions and fuelling my curiosity. Furthermore, I would like to thank Mr Robert P. Townsend and Mr Helgard Honiball for sharing their deep understanding and decades of industry experience.

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# Abbreviations

| | |
|---|---|
| **VSD** | **V**ariable **S**peed **D**rive |
| **FVC** | **F**lux **V**ector **C**ontrol |
| **THD** | **T**otal **H**armonic **D**istortion |
| **PQ** | **P**ower **Q**uality |
| **PWM** | **P**ulse **W**idth **M**odulation |
| **RHT** | **R**educed **H**armonic **T**echnology |
| **PCC** | **P**oint of **C**ommon **C**oupling |
| **UPS** | **U**ninterruptible **P**ower **S**upply |
| **RMS** | **R**oot **M**ean **S**quare |
| **FFT** | **F**ast **F**ourier **T**ransform |
| **PF** | **P**ower **F**actor |
| **IEEE** | **I**nstitute of **E**lectrical and **E**lectronic **E**ngineers |
| **IEC** | **I**nternational **E**lectrotechnical **C**ommission |
| **IGBT** | **I**nsulated of **G**ate and **B**ipolar **T**ransistor |
| **AC** | **A**lternating **C**urrent |
| **DC** | **D**irect **C**urrent |
| **LV** | **L**ow **V**oltage |
| **MV** | **M**edium **V**oltage |
| **CT** | **C**urrent **T**ransformer |
| **VT** | **V**oltage **T**ransformer |

*Dedicated to my parents and to my beautiful Aiba. This gruelling journey was softened by your love and support, and for that, I am truly grateful.*

# Chapter 1

# Introduction

Power quality is a topic of major interest in industry today, from the energy supplier to the consumer. Power quality is defined in this study and the main emphasis of this investigation will be harmonics. Harmonics in a Variable Speed Drive (VSD) originate from its rectifier bridge circuit; it is a result of abrupt pulse currents that are drawn by the rectifer bridge circuit [1].

## 1.1 Introduction to Variable Speed Drives

A VSD is used to control the flow of energy from the mains to the motor shaft. Energy is supplied to a process through the motor shaft. There are two physical quantities used to describe the state of the shaft: torque and speed. To control the flow of energy from the mains to the process, control of torque and speed is necessary [2]. VSDs are configured as illustrated by Figure 1.1.

In industrial applications, either one of these quantities are controlled. Either in torque control or speed control modes. When the VSD is operated in torque control mode, the speed of the VSD is determined by the load at the motor shaft. When the VSD is operated in speed control mode, the torque is determined by the load at the motor shaft [2].

VSDs are used to control AC induction motors that may be driving loads such as fans, pumps, conveyors, to operate in a wide range of speeds as opposed to a direct on-line (DOL) method that is limited to a fixed speed. VSDs are frequently referred to as variable frequency drives, adjustable speed drives, frequency inverters, or frequency converters [1]. Installation of a VSD can increase energy efficiency and energy savings can exceed 50% when compared to a DOL installation [3].

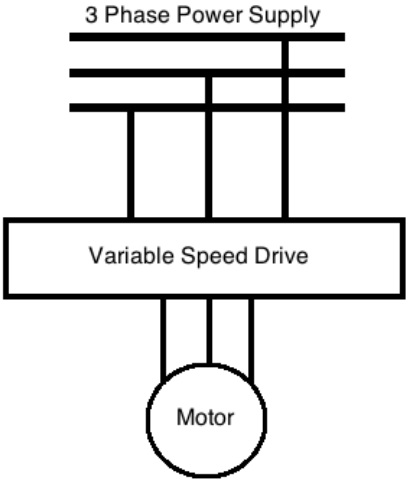



FIGURE 1.1: The basic configuration of a VSD.

VSDs can improve the power factor of motor installation, provide accurate speed control of an AC motor in applications such as, Heating, Ventilation and Airconditioning (HVAC) systems eliminating the need for expensive mechanical systems such as control valves and outlet dampers, pressure control within a water supply pump station, material handling using converyor belts and hoists. VSDs also have other benefits such as soft starting and over-speed capability [1].

### 1.1.1 Control Loop of a VSD

#### 1.1.1.1 Frequency Control of a VSD

The VSD frequency control technique uses voltage and frequency to control the motor. Furthermore, the voltage and frequency is generated outside of the motor. Both voltage and frequency reference are fed into the pulse width modulation (PWM) inverter of the VSD which simulates an AC sinusoidal current waveform and feeds this output to the motors stator windings [2].

The frequency control method does not make use of a feedback from the motor shaft. Because there is no feedback device, the frequency control philosophy is an economically viable option and a simple solution to control AC induction motors. This type of VSD is used in applications, such as pumps and fans, where high levels of accuracy and torque isn't a requirement. [2]. The frequency control loop of a VSD is illustrated in Figure 1.2.

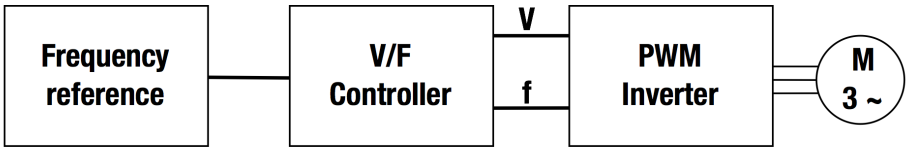



FIGURE 1.2: Control loop of a VSD with frequency control using PWM, as adapted from [2].

#### 1.1.1.2 Flux Vector Control (FVC) of a VSD

Flux Vector Control based VSDs uses a closed loop control philosophy as it obtains information about the rotor status (rotor speed and angular position) by means of a pulse encoder. The motor electrical characteristics are mathematically modelled within the VSD control circuitry. The control processor of of a FVC VSD calculates the voltage, current and frequency, which are the controlling variables, and are fed via a PWM inverter to the AC induction motor. Torque, therefore, is controlled indirectly via the speed controller of the FVC VSD [2]. The torque controller gets its reference via the speed controller. Refer to Figure 1.3 for the control loop of the FVC VSD.

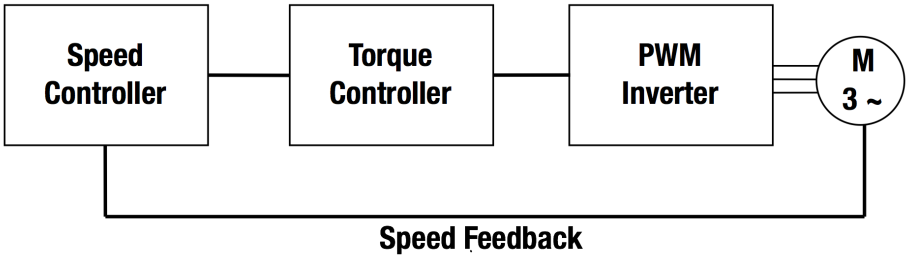



FIGURE 1.3: Control loop of a VSD with flux vector control using PWM, as adapted from [2].

## 1.2 Introduction to Power Quality

Power Quality is defined as "a term that refers to maintaining the near sinusoidal waveform of power distribution bus voltages and currents at rated magnitude and frequency" [4]. The study of power quality is to establish the parameters and the degree of variation with respect to their rated magnitude. The study of power quality can be further expanded into the following topics [4]. These topics refer to events that cause disturbances in the electric power system.

1. Interruption

   Interruption is a type of disturbance that occurs when the voltage magnitude is zero [4].

2. Under voltage

   Under voltage is a type of disturbance that occurs when the voltage magnitude is lower than the nominal value [4].

3. Over voltage.

   Over voltage is a type of disturbance that occurs when the voltage magnitude is higher than the nominal value [4].

4. Voltage/Current unbalance

   Voltage/Current unbalance is a type of disturbance that occurs when there is a deviation in the magnitude of voltage/current in one or more of the three phases [4].

5. Harmonics

   Harmonics is a non-sinusoidal waveforms resulting from non-linear loads drawing currents from a sinusoidal supply [4].

6. Transients

   Transient is a type of disturbance that occurs when there is a sudden rise in the magnitude of the signal [4].

7. Voltage sag

   A voltage sag is a type of distubance that occurs when there is a reduction in RMS voltage over a range of 0.1 to 0.9 pu for durations greater than 10 ms but no more than 1s [4].

8. Voltage swell

   A voltage swell is a type of distubance that occurs when there is an increase in RMS voltage over a range of 1.1 to 1.8 pu for durations greater than 10 ms but no more than 1s [4].

9. Flicker

   Flicker is a type of visual disturbance that occurs when there is a frequency variation of voltage in a system [4].

10. Ringing waves

    Ringing waves is a type of disturbance that occurs when there are transient waves that decay gradually [4].

11. Outages

    Outages are a type of disturbance that occurs when there is a interruption not exceeding 60s as a result of faults or tripping of switchgear [4].

## 1.3 Introduction to Harmonics

The electric power system is expected to have pure sinusoidal alternating current and voltage waveforms of single frequency. The reality is that these waveforms aren't so pure. These voltage and current waveforms are distorted and are called non-sinusoidal waveforms [4].

Harmonics can be defined as, "A sinusiodal component of a periodic wave or quantity having a frequency that is an integer multiple of the fundamental frequency" [5]. The integer multiple is referred to as the order of the harmonic. The parameter that is used to express the extent of the harmonic content of the waveform is referred as Total Harmonic Distortion (THD). The THD is defined as the ratio of the sum of all harmonic power to the power of the fundamental frequency and is expressed as a percentage of the amplitude of the fundamental component [6]. The harmonic distortion affects both the voltage (THDu) and the current (THDi) waveforms [6].

The following equation is generally accepted in industry for calculation of THD [7], where n is the harmonic order.

Equation for THD:

$$THD(\%) = \sqrt{\sum_{n=2}^{\infty}(\frac{P_n}{P_1})^2} \times 100 \tag{1.1}$$

The equations for calculating THDi and THDu are as follows.

Equation for THDi:

$$THDi(\%) = \sqrt{\sum_{n=2}^{\infty}(\frac{I_n}{I_1})^2} \times 100 \tag{1.2}$$

Equation for THDu:

$$THDu(\%) = \sqrt{\sum_{n=2}^{\infty}(\frac{V_n}{V_1})^2} \times 100 \tag{1.3}$$

Harmonics have been a problem for power systems engineers for many decades; from the very beginning since electric power industry became popular [8], the problems caused

by harmonics were noted by engineers but with no proven remedies [8]. However research conducted by Charles Proteus Steinmetz and others soon brought more insight on harmonics and its effects [8] [9]. Harmonic analysis became popular soon after French mathematician Jean Fourier developed the well known method called, "Fourier Analysis" [8]. The method for analyzing a sinusoidal current waveform to reveal the component frequencies was termed, "Harmonic Analysis" [8].

In recent years, there has been an increased number of power electronics introduced into products and equipment for everyday use and as a result, increasing the addition of harmonics into the electric power system [1] [10].

Harmonics are generally produced by personal computers (single phase loads), uninterruptible power supplies (UPSs), VSDs or any electronic device with switching supplies to convert incoming AC to DC [11]. Harmonics result from non-linear loads that draw current in abrupt pulses, instead of a smooth sinusoidal wave [11] [12].

The harmonics order found in three-phase distribution networks are generally odd numbered [13] [10]. The higher order harmonics are normally lower in magnitude. Harmonics above the order of 50 are negligible and measurements are no longer meaningful [10] [1]. Sufficiently accurate measurements are obtained by measuring harmonics up to order 30 as further measurements above the order of 30 will not be of significant magnitude [10]. Most industries and utilities monitor harmonic orders 3, 5, 7, 11 and 13 as measurements up-to this order are known to be more than sufficient [1] [10] [12].

More comprehensive conditioning takes into account harmonic orders up to 25 [1] [10] [12]. It is known that the 3rd order harmonic contributes to currents flowing through the neutral conductor, in single phase instances, and the 5th and 7th order harmonic contributes to heat losses such as those on transformer windings and conductors [1] [12].

Earlier the terms linear and non-linear were mentioned; these terms represent the relationship between the current waveform to the voltage waveform against time and are illustrated in Figure 1.4. A linear relationship exists between the voltage and current, which is typical of an across-the-line load and therefore the voltage and the current waveform have the same shape. Non-linear loads create harmonics by drawing current in abrupt short pulses, as illustrated in Figure 1.5, rather than in a smooth sinusoidal manner therefore the voltage and the current waveform do not have the same shape [11].

If a fourier analysis is performed on the current waveform of a non-linear load, one can decompose that non-sinusoidal waveform into a sum of sinusoidal waveforms and can be thought of as harmonics [12]. Even though the waveform is non-sinusoidal, because it is periodic, one can think of it as a summation of sinusoidal waveforms of varying amplitudes and frequencies [14].

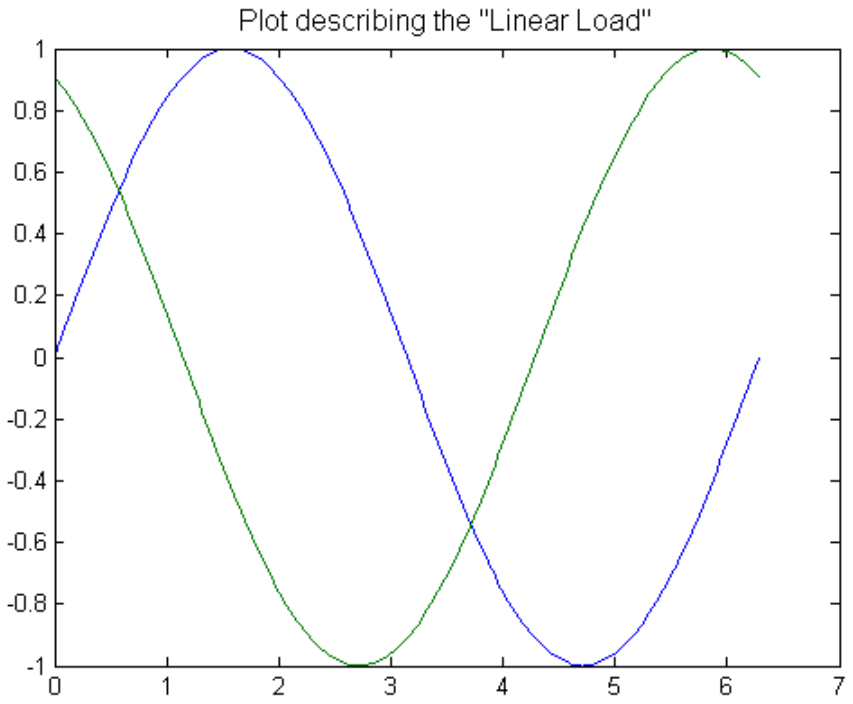



FIGURE 1.4: The representation above illustrates an example of the voltage and current relationship of a linear load, as adapted from [11].

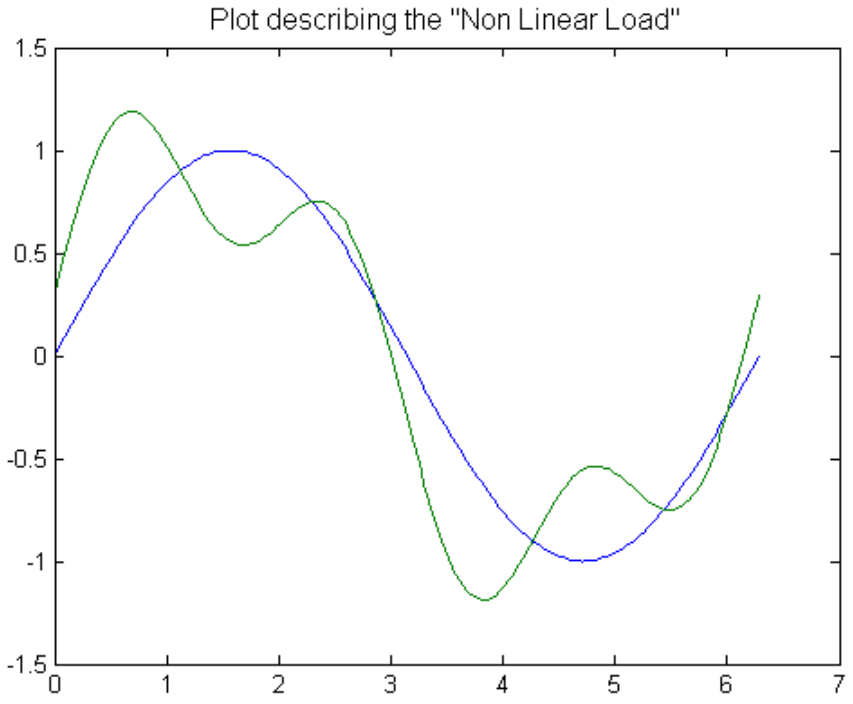



FIGURE 1.5: The representation above illustrates an example of the voltage and current relationship of a non-linear load, as adapted from [11].

The front end of a standard VSD, as illustrated in Figure 1.6, makes harmonics an inevitable phenomenon, because of the way the current is conducted through the diodes in short abrupt pulses. This is the standard power circuit elementary configuration for most pulse width modulated VSDs with diode-bridge rectifiers sold in the marketplace today. The size of the capacitor banks determines how quickly the capacitors discharge [11].

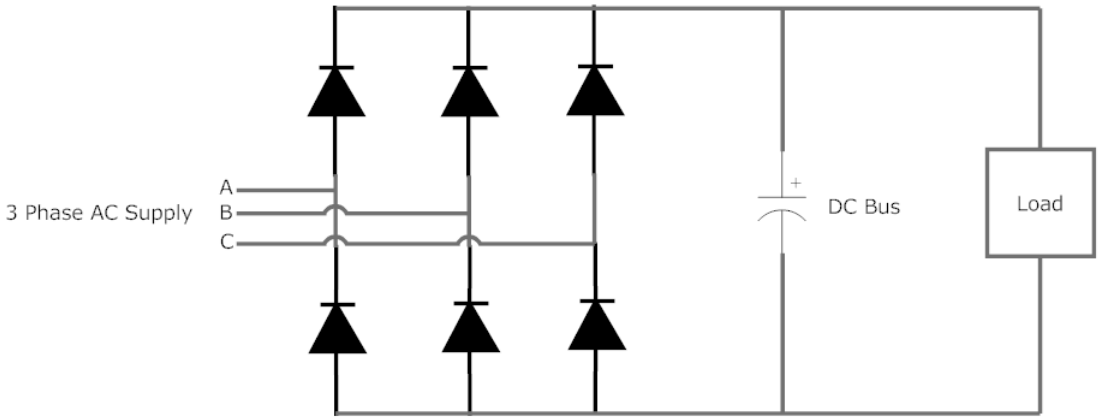



FIGURE 1.6: The representation above illustrates the typical 6-pulse rectifier circuit diagram adapted from [11].

A three-phase input rectifier with a capacitor bank draws current in abrupt pulses; this is due to the fundamental operation principle of a diode [15]. For example when the input voltage across any pair of diodes is greater than the DC link voltage, dropped across the capacitor, then current flows and charges the capacitor (Charging stage of the cycle). When the input voltage is less than the DC link voltage, the diodes no longer conducts the input current and the capacitor bank supplies the DC current which give rise to the characteristic abrupt pulsed current waveform (Discharge stage of the cycle).

The harmonic current generated by non-linear loads, delivered at non-fundamental frequencies, deliver no real power to the load [16]. Figure 1.7 illustrates how harmonic currents cause distortion to the overall current (blue curve) that is drawn. The waveform shown in blue illustrates the distorted current. The double humped shape of this waveform can be seen clearly; the positive gradient of the humps represents the charging phase of the capacitor banks; whereas the negative gradient of the humps represents discharge phase of the capacitor banks.

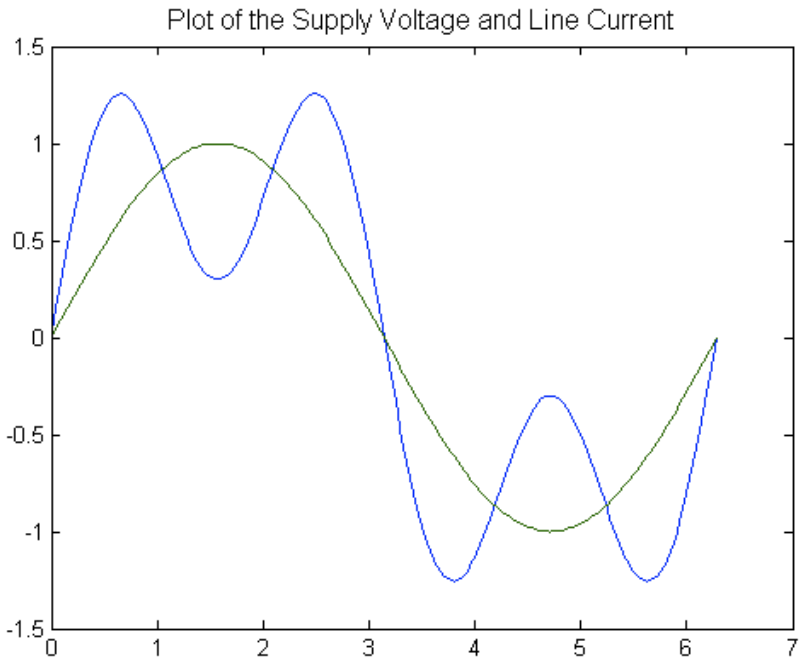



FIGURE 1.7: Harmonic Current Distortion illustrated adapted from [16].

## 1.4 Introduction to Harmonic Standards

A fair way to benchmark the mitigation solutions and understand what sets each apart would be to look at what the international standards stipulate and to what limits these standards apply.

The IEEE 519-1992, "Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems" was reviewed, it revealed that this standard was established to deal with harmonic disturbances in electrical transmission lines, power grids and entire systems [17].

Most engineers resort to applying the standard on an individual product level and by ensuring that the harmonics produced by these individual products are within the set limits, the compliance on a system level was also achieved [17].

The international standard IEC 61000-3-12, Electromagnetic Compatibility (EMC) Part 3-12 Limits is also very often used as a benchmark for harmonic mitigation on individual products. IEC 61000-3-12 stipulates harmonic current limits produced by equipment connected to public low voltage systems [18]. For compliance to IEC 61000-3-12, the THDI must be less than 48% [18].

Harmonic mitigation can become very expensive if the emissions limits are extremely strict. The harmonics standards should be carefully analyzed and applied to minimize the cost of the mitigation solution. Figure 1.8 and Figure 1.9 can clarify which standards will apply to the different consumers [6] [12].

The harmonics emission of the public network (LV or MV), from which the different customers are supplied by the utility is measured at the Point of Common Coupling (PCC) with respect to the limits of THDu. Limits are applied at the PCC are such that the utility supplies the consumers with consistent and high quality power supply [6].

IEC 61000-3-2 and IEC61000-3-12 are harmonic standards that are used to limit the emissions of LV consumers at equipment level. All equipment up to 75A require individual THDi limits. Agreements between the suppiler and the consumer is generally required for equipment above 75A with respect to local regulations [6].

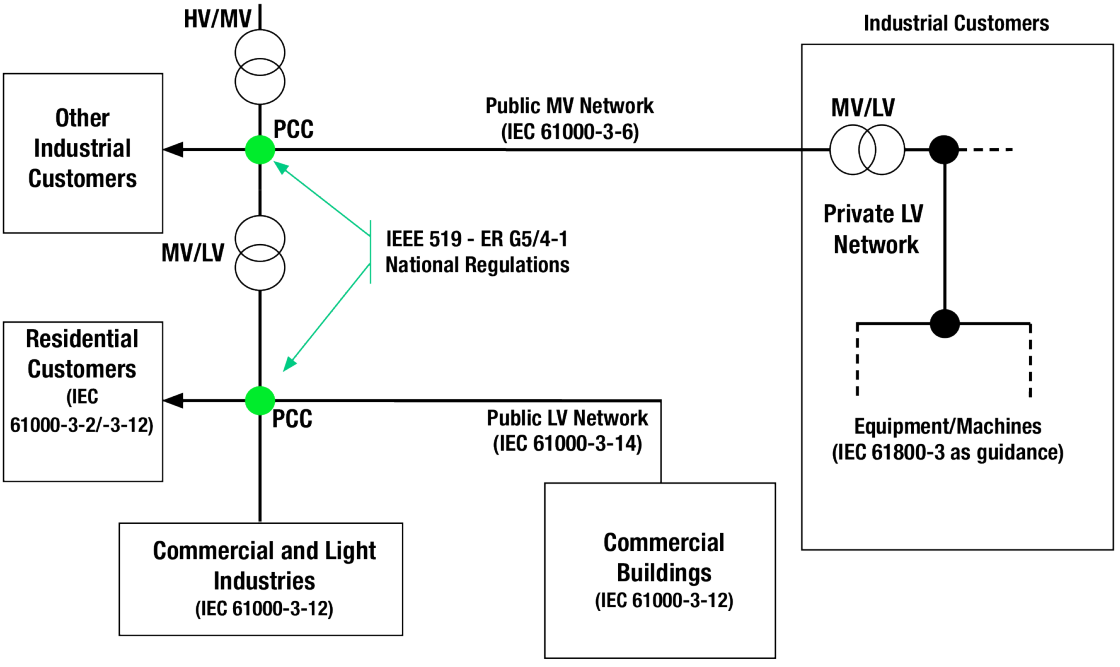



FIGURE 1.8: Illustration of the point of common coupling within the public network. Adapted from [6].

## 1.5 Aim of the Study

The aim of the study is to evaluate various effects resulting from the presence of harmonics in a VSD installation. The study will also aim to highlight existing harmonic

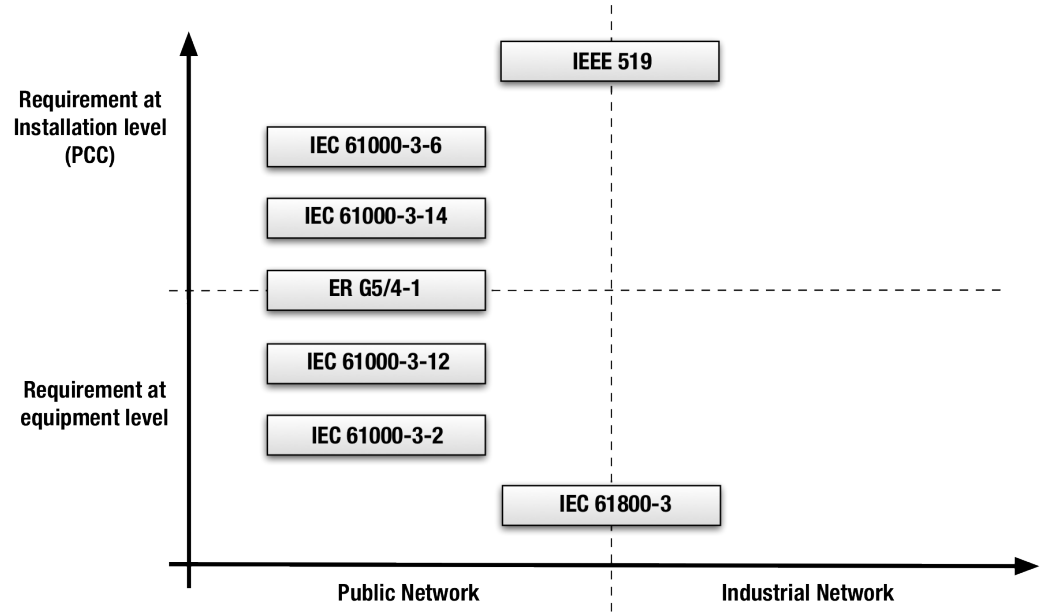



FIGURE 1.9: Standards and recommendations with harmonics. Adapted from [6]

mitigation solutions in the market and will be benchmarked with respect to its compactness, complexity, harmonic mitigation, efficiency and cost effectiveness. Furthermore, once a possible solution has been identified with respect to the above mentioned criteria, the study also aims to further quantify the effectiveness of the new solution, that is, to calculate the degree to which the solution can mitigate harmonics both at the input and at the output of the VSD.

The methods used to evaluate the harmonic mitigation solution includes a SPICE software simulation using a basic VSD model and then followed by a laboratory experiment. Majority of the mitigation solutions to be discussed are already commonly available in the market and the literature on these solutions serve as a foundation to critically analyze possible new harmonic mitigation solutions in the market. The aim of this document is not to compare all the various well known solutions, but rather to test the suitability and effectiveness of new solutions, if any.

## 1.6 Overview of Document

In Chapter 2, a literature review on the various effects of harmonics on the power system and also on the power factor of a VSD installation are discussed. Furthermore, misinterpretations of the measurement of harmonics at partial loads are discussed.

In Chapter 3, a study is done to review the commonly available harmonics mitigation solutions in the market and thereafter, the existing literature on new technology called Reduced Harmonics Technology (RHT) was reviewed. All of the harmonic mitigation solutions are reviewed under various criteria to evaluate its effectiveness.

In Chapter 4, Spice circuit simulation software was used to model the input section of a three phase rectifier circuit with consideration given to source impedance. The purpose of the simulation was to build a simplified circuit representation of a VSD. Furthermore, to reproduce the commonly known behaviour of a standard VSD and then further progress to reproduce the behaviour of the RHT VSD. The focus of the simulation model was at the input of the three phase rectifer and not the output. Lastly, after both the standard VSD as well as the RHT VSD are simulated, results will be compared to draw closer to reaching conclusions on the effectiveness and make recommendation on the viability of using the RHT VSD in the market.

In Chapter 5, an experiment was conducted to analyze the input current and the output current waveforms of the RHT VSD and the standard VSD. Consideration was given to the output to determine if the quality of the RHT VSD was compromised resulting from any improvements at the input current of the RHT VSD. Finally the document concludes in chapter 6.

# Chapter 2

# Literature Review

## 2.1 Introduction

The following chapter will focus on the consequence of the presence of harmonics on the installation of a VSD and the power system. Furthermore, the effect of harmonics on the overall power factor of the VSD installation will be discussed. Lastly, focus will be given to the misinterpretation of harmonic current measurement at partial loads.

## 2.2 Effects of Harmonics

The magnitude and frequency of the harmonics generated by a VSD are typically unique type of a distorting load and enables it to be identified with the use of fourier analysis on the overall waveform. Metering systems of various accuracies are available to measure the level of harmonic content in a waveform [19]. The distorting harmonic components propagate through the electrical/power system and causes high frequency voltage drops across the components in the power system. These voltage drops translates to distortions in voltage waveforms of neighboring customers [19].

Every electrical power system has a thevenin equivalent impedance that restricts the flow of current [20]. This impedance arises from magnetic flux effects in substation transformers and transmission lines [19].

The electrical network is a linear load [20]. Widespread power electronics usage has introduced non-linear loads into the network and the result being electrical losses and distortion of the supply in the power system [20].

Not all equipment in the market are affected by harmonics the same way; for instance, electric heaters and incandescent light bulbs are totally unaffected by harmonics [19]. AC induction motor windings are affected through the overheating caused by harmonics. The overheating accelerates the degradation of winding and thus reducing the life of the motor. Another effect of harmonics in motors includes the harmonic voltages, which results in higher currents drawn by the motor as opposed to current at 50Hz [19].

Equipment such as dimmers containing thyristors can depend on steady voltage wave shape and can thus be affected when operated under the presence of harmonics [19]. Under single-phase loads, harmonics are spread over to three phase loads; this is very common in commercial buildings. This results in higher neutral currents and often times exceeding that of the active line current [19].

Resonance is also a major concern in large plants where harmonics are prevalent [21] [10]. Resonance can for instance occur when there are power factor correction capacitors installed. The harmonics generated by VSDs can contain components of the same frequency as that of the resonant frequency of the capacitor banks [16] [10]. Some indication of resonance includes overheating, frequent circuit breaker tripping, irregular fuse operation, capacitor failure, electronic equipment malfunction, flickering lights and telephone interference [16] [10].

## 2.3 Effects of Harmonics on Power Factor

Distortion Power Factor describes how the average power transferred to the load is affected due to harmonics. A complete description can be found in IEEE 1549-2010 [22].

Where THDi is definied in Equation 1.2, the equation for Distortion PF is defined as:

$$DistortionPF = \frac{1}{\sqrt{1 + THDi^2}} \tag{2.1}$$

Where $\theta$ is the phase angle between the current and the voltage waveform, the equation for Displacement PF is defined as follows:

$$DisplacementPF = \cos(\theta) \tag{2.2}$$

Equation for overall PF:

$$TotalPF = DistortionPF \times DisplacementPF \tag{2.3}$$

Refer to Figure 2.1 for the graphical illustration of total power factor and the effect of harmonics on the total power factor [22]. This illustration is a simple way to elaborate the extent to which harmonic distortion decreases the average power transferred to the load [22].

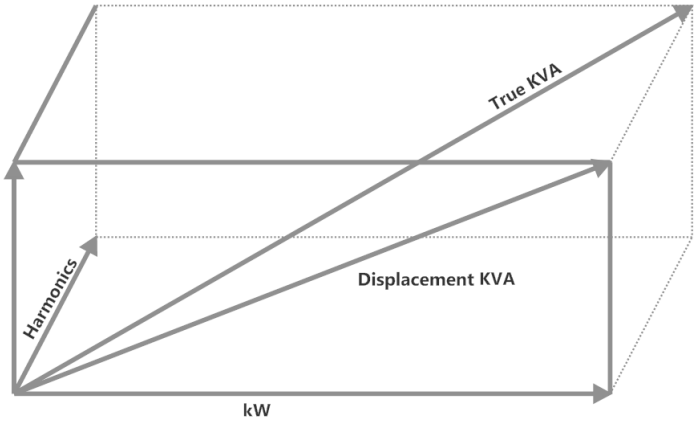



FIGURE 2.1: Graphical representation of the total power factor. Adapted from [22].

Data provided by the manufacturer of a VSD, which evaluated the effect of harmonics on the total power factor of a VSD installation, with and without the use of harmonic mitigation are recorded in Table 2.1 and Table 2.2 and illustrated in Figure 2.2; The results reveal that the power factor has almost doubled when harmonic mitigation is employed. This illustrates the extent to which harmonics influences the true power factor of a VSD installation [23].

| Load (%) | Overall Power Factor | THDi (%) |
|---|---|---|
| 10 | 0.385 | 238 |
| 20 | 0.415 | 217 |
| 30 | 0.434 | 206 |
| 40 | 0.447 | 198 |
| 50 | 0.458 | 192 |
| 60 | 0.467 | 187 |
| 70 | 0.474 | 182 |
| 80 | 0.482 | 178 |
| 90 | 0.488 | 173 |
| 100 | 0.496 | 170 |

TABLE 2.1: The table above illustrates the overall power factor across various loads as well as the THDi, when there is no harmonic mitigation. Adapted from [23].

| Load (%) | Overall Power Factor | THDi (%) |
|---|---|---|
| 10 | 0.653 | 113 |
| 20 | 0.704 | 97 |
| 30 | 0.736 | 87 |
| 40 | 0.764 | 80 |
| 50 | 0.815 | 68 |
| 60 | 0.854 | 60 |
| 70 | 0.881 | 54 |
| 80 | 0.899 | 49 |
| 90 | 0.915 | 46 |
| 100 | 0.931 | 44 |

TABLE 2.2: The table above illustrates the overall power factor across various loads as well as the THDi, when there is harmonic mitigation. Adapted from [23].

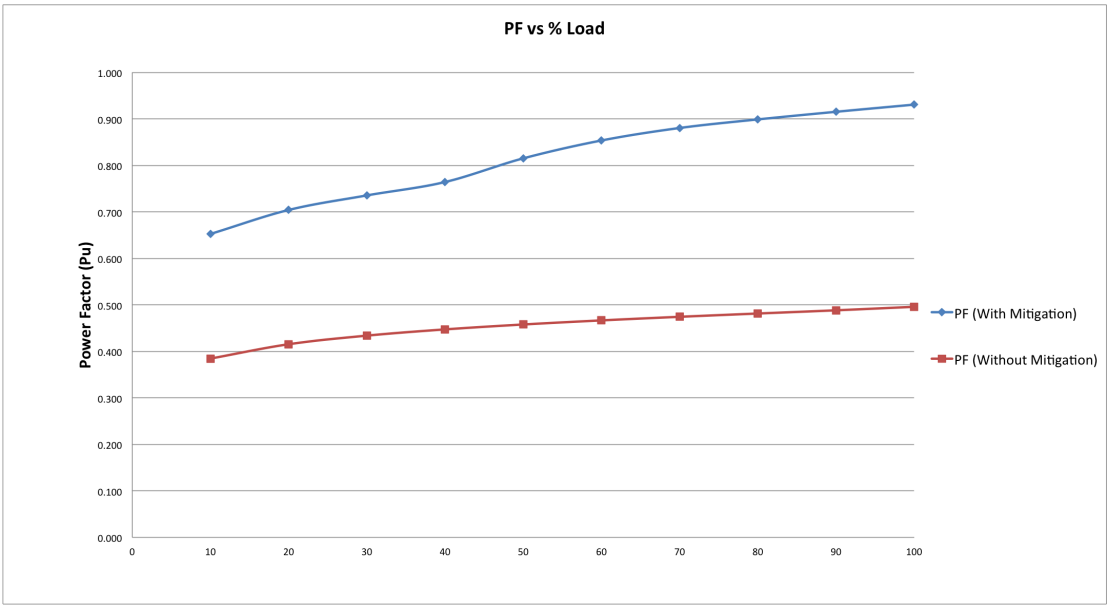



FIGURE 2.2: Illustrating the difference in power factor with and without harmonic mitigation solutions.

## 2.4 Misinterpretations of THDi measurement at partial loads

The operating speed of a VSD-driven motor is often adjusted to the requirements of a process and in such instances, the motor only draws a portion of its nominal rated current (full load current). These instances are referred to as partial load operations [6]. Harmonics measurement (THDi) of a VSD at partial load operations create mininterpretations. In the instance when the VSD is operating at full load, the fundamental current component of the non-sinusoidal input current is approximately the same value as the full load current of the VSD [6].

In the case of partial loads, the fundamental current component of the non-sinusoidal input current will be much lower than the full load current of the VSD but the sum of the harmonic currents are known to reduce but slightly when compared to the case of full load operation [6].

The above mentioned cases will have two different results when measuring the THDi. This is because of the inverse proportional relationship of the fundamental current to the THDi, as can be seen in Equation 1.2. The result, as illustrated in Figure 2.3, is an inflated THDi value at partial loads as opposed to when the VSD is operating at full load [6].

Therefore the THDi measured at partial loads are considered to be a misrepresentation and doesn't represent the actual magnitude of the harmonic distortion of the current waveform. Whereas THDi measurements at full load are considered to be a more realistic figure when describing the amount of harmonics generated.

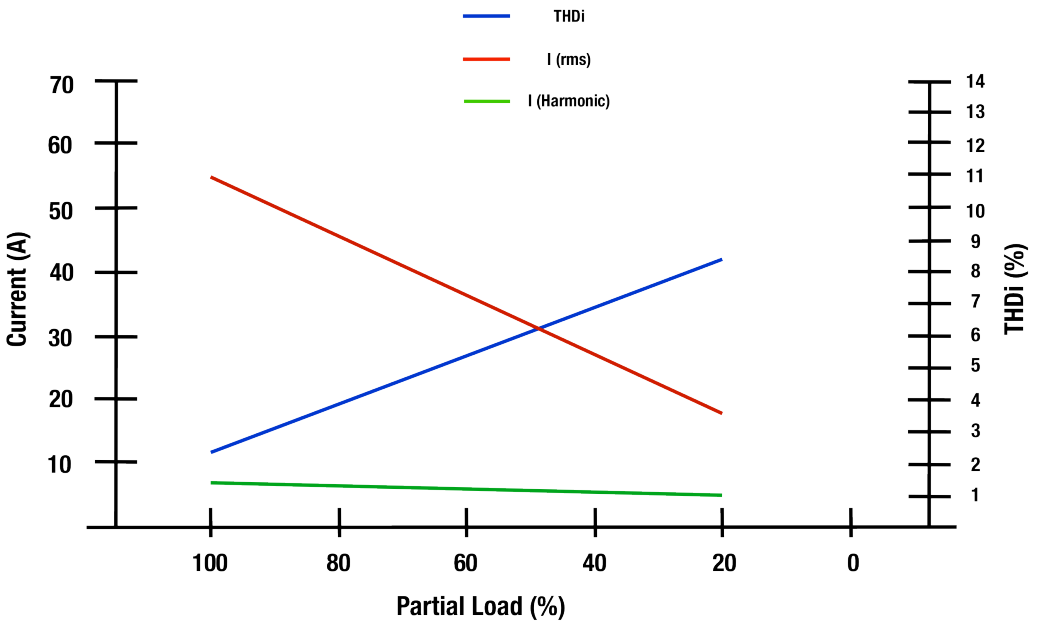



FIGURE 2.3: Misinterpretation of the THDi at partial load. Adapted from [6].

## 2.5 Conclusion

The effects of harmonics on the VSD installation was reviewed, paying careful attention to the effect on the overall power factor of the VSD installation. Results provided by a VSD manufacturer showed stark differences in the power factor on a VSD installation when tests are conducted with and without basic harmonic mitigation. When the test

was conducted without any harmonic mitigation, the overall power factor of the VSD was approximately 0.496. When the test was conducted with basic harmonic mitigation, the overall power factor of the VSD was approximately 0.931. The stark difference in the above two power factor measurements further justify the need for harmonic mitigation solutions in a VSD installation. The benefits of having effective harmonic mitigation is not just a higher power quality installation but also reduced energy costs.

# Chapter 3

# Harmonic Mitigation Solutions

## 3.1 Introduction

With regard to harmonics, the IEEE 519 standard stipulates guidelines for recommended harmonic levels in electrical distribution systems including maximum voltage and current distortion [24]. Today there are many methods of harmonic mitigation. Harmonic mitigation has an associated cost with it and at present there is a trade-off between cost and the effectiveness of the mitigation solution. A much broader criteria is often used to select a harmonic mitigation solution and are listed below [6].

1. Compactness
2. Complexity
3. Harmonic Mitigation
4. Efficiency
5. Cost Effectiveness

## 3.2 Line Reactors

The first harmonic mitigation technique is the use of Line Reactors or also known as Line Chokes. Three phase line reactors are added in series on the supply side of the VSD. This is the most common solution in the market today as it is relatively inexpensive and can lower harmonics to approximately 50%, as compared to the harmonic levels when no mitigation is added [25]. The Line Chokes are made in two variations namely the

3% and 5% impedances. The other function that the Line Chokes serve is that they provide protection against over-voltages in the supply voltage [26]. The spider diagram illustrating the various selection criterias for the line choke is illustrated in Figure 3.1.

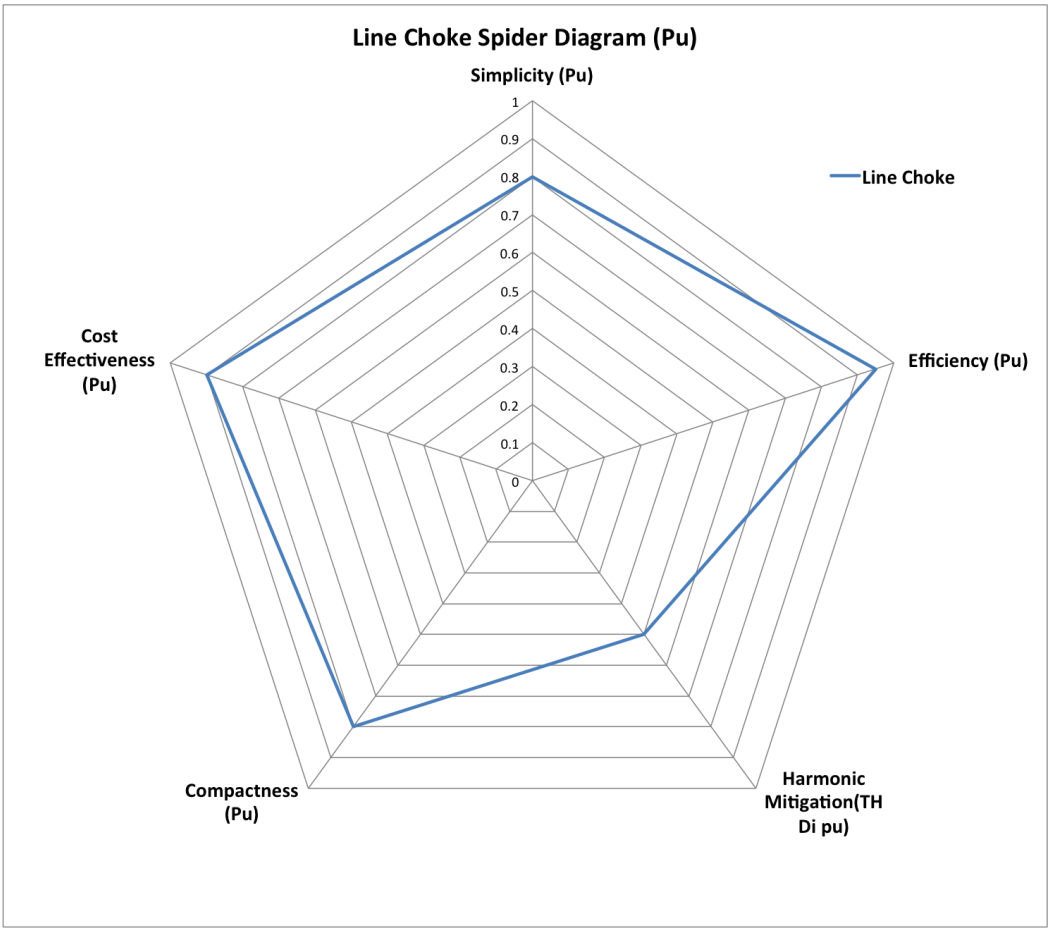



FIGURE 3.1: Line choke spider diagram. Adapted from [6].

## 3.3 DC Chokes

Another common method of harmonic mitigation in industry is the use of a DC Choke. This method involves adding an inductance to the DC bus of the VSD instead of placing line reactors in series with the VSD. The ability of the DC Choke to reduce harmonics is measurably the same as the AC Line Choke [25]. The main advantage of DC Chokes is that it is smaller in size as compared to the AC Line Choke and can in most instances be fitted into the VSD [25]. Up to a certain power rating, most VSDs have the option of a built in DC choke. The disadvantage of the DC choke is that it will not be as effective as the line choke especially against sudden spikes or over-voltages in the supply [26]. The spider diagram illustrating the various selection criteria for the DC choke is illustrated in Figure 3.2.

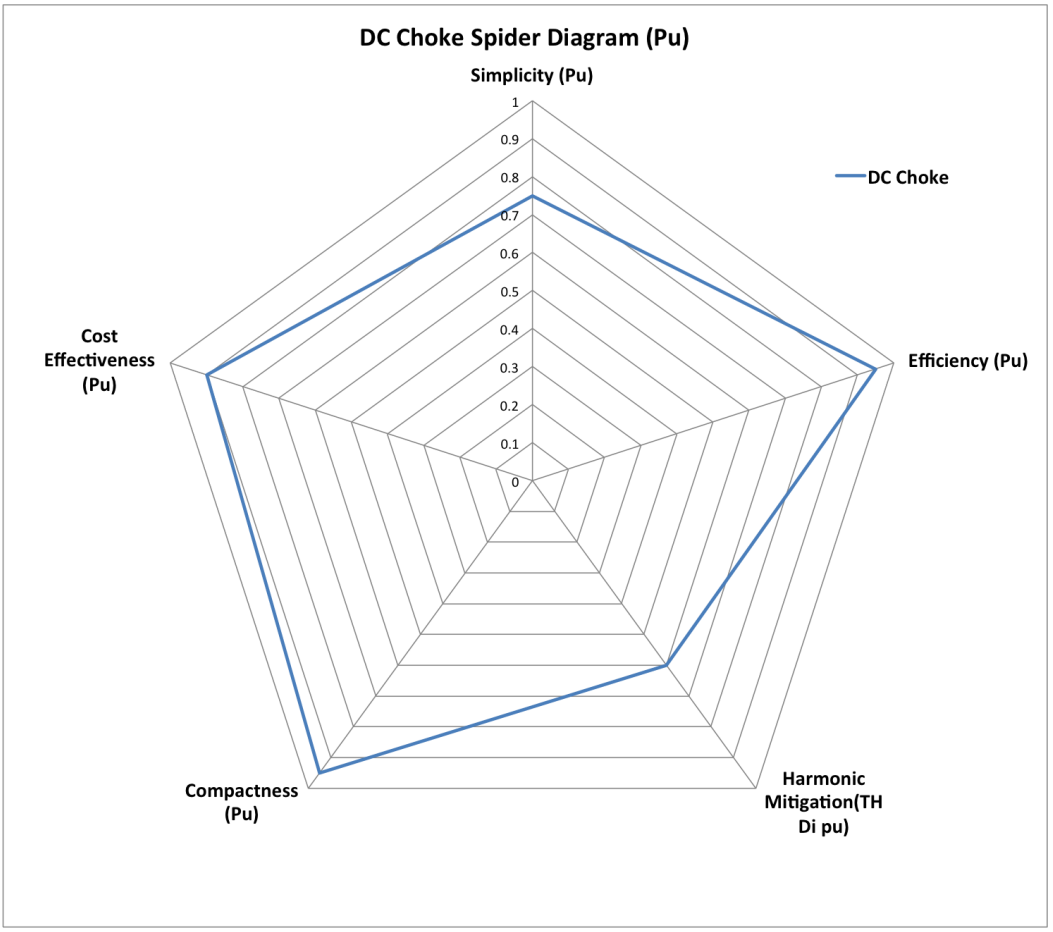



FIGURE 3.2: DC Choke spider diagram. Adapted from [6].

## 3.4 Multi Pulse Drives

In the market today, most VSD manufacturers employ a rectifier circuit in three phase to rectify the AC supply voltage to DC. The three phase rectifier bridge is also known as the six pulse diode rectifier. This form of rectification is advantageous as it is rugged and robust. A multi pulse drive employs multiple such six pulse rectifier inputs; connecting two six pulse rectifiers in parallel to feed the same DC bus forms i.e. a twelve pulse rectifier [27].

This configuration will require a phase shifting transformer and the advantage in using such a system is that it produces a smoother current waveform at the supply side than the standard six-pulse rectifier, producing a THDi lower than 10% [27]. There exists an 18 pulse as well as a 24 pulse rectifier in the market and are formed similarly by configuring three or four six pulse rectifiers in parallel. The additional transformers that are used to achieve this configuration make the multi pulse solution very expensive

and increase the overall size of the installation [28]. The spider diagram illustrating the various selection criterias for the multi pulse drive is illustrated in Figure 3.3.

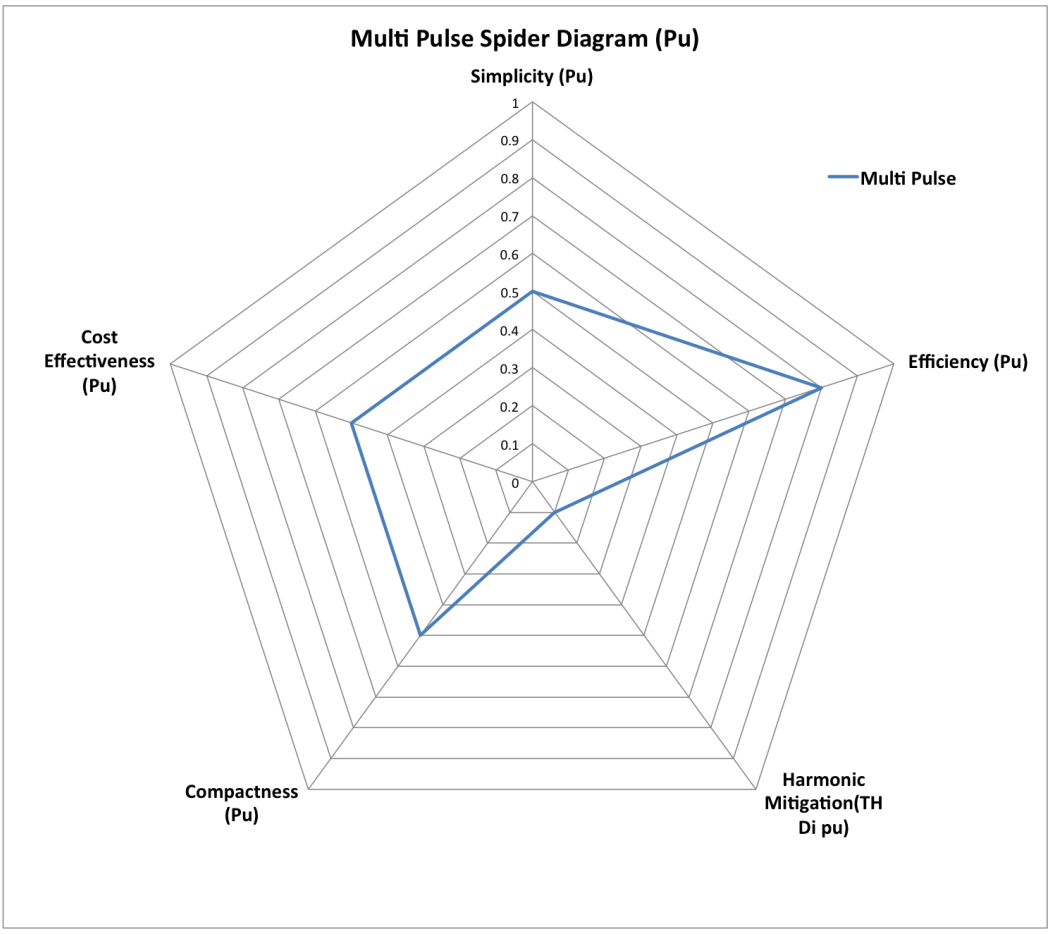



FIGURE 3.3: Multi Pulse Drive spider diagram. Adapted from [6].

## 3.5 Active IGBT Rectifiers

The active IGBT (Insulated Gate Bipolar Transistor) rectifier also known as the Active Front End is mainly used to control the power from the supply network. This form of mitigation also allows for a very low THDi of approximately 5%. The rectifier is actively controlled in the way it conducts current to produce almost sinusoidal line currents thereby reducing harmonics [29].

The main advantages are as follows:

1. Almost a perfectly sinusoidal supply current with low harmonic content
2. Almost unity power factor

3. The active front ends also have the ability to generate reactive power

The main drawback here is still the higher cost as well as the installation size when compared to the standard six-pulse diode rectifier bridge [28]. The spider diagram illustrating the various selection criteria for the multi pulse drive is illustrated in Figure 3.4.

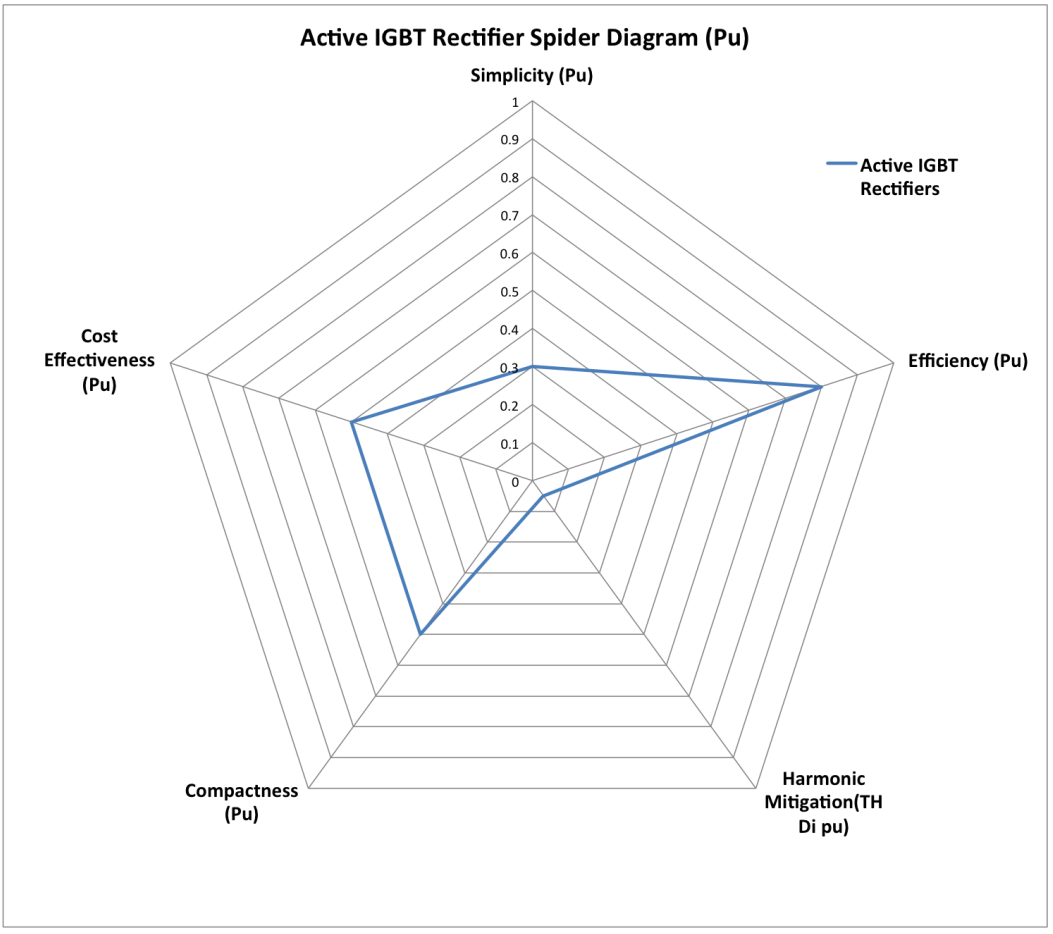



FIGURE 3.4: Active IGBT Rectifier spider diagram. Adapted from [6].

## 3.6 Passive Filters

Passive filters are also another effective method of harmonic mitigation. Such filters are often made up of resistance-inductance-capacitor combinations. Such a configuration is usually targeted at attenuating a specific range of harmonic frequencies. This is achieved by either attenuating the flow of the harmonic currents through the passive filter or as way to shunt the harmonic currents through them [26].

The disadvantage with the passive filtering techniques are that they are only partially mitigating the harmonics and dont necessarily offer a complete solution to the problem.

The size and cost of such a passive filter is also a major concern as it increases the cost of the overall installation. The spider diagram illustrating the various selection criteria for the multi pulse drive is illustrated in Figure 3.5.

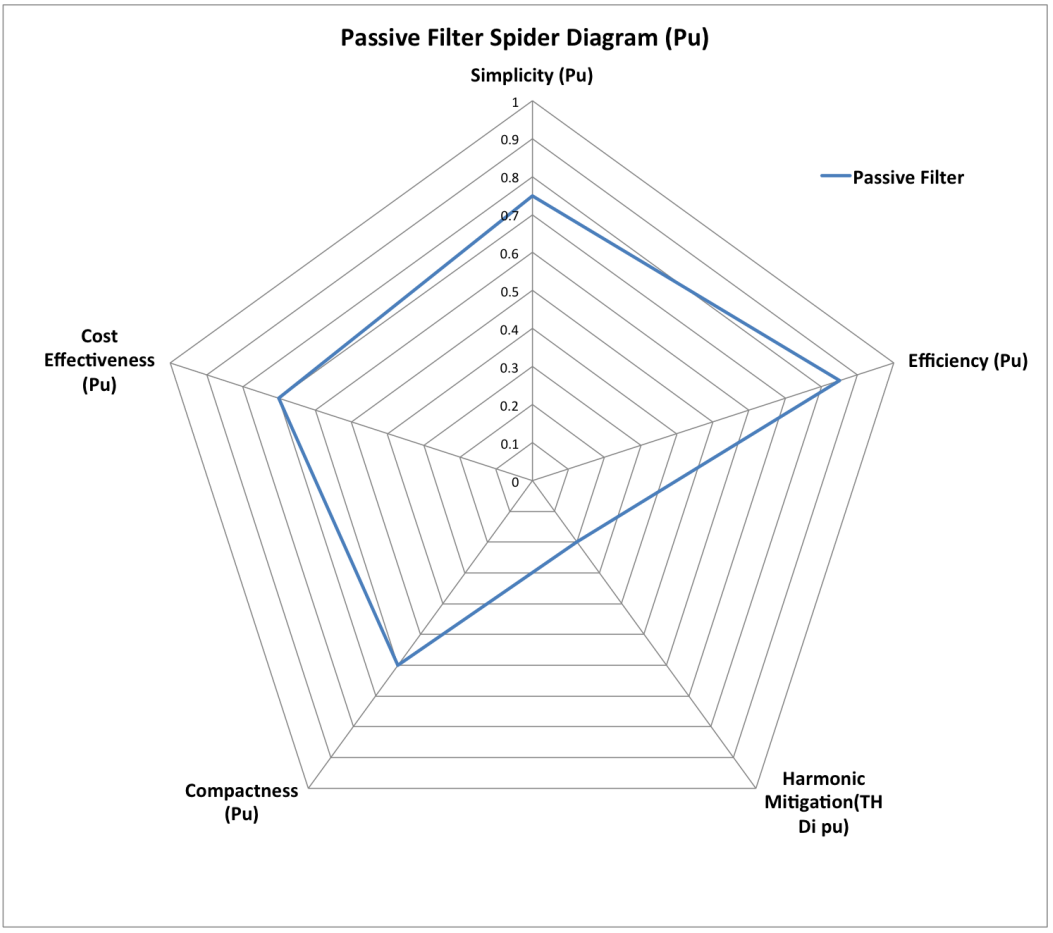



FIGURE 3.5: Passive Filter spider diagram. Adapted from [6].

## 3.7 Reduced Harmonics Technology (RHT)

The RHT solution looks directly at ways to reduce harmonics generated by VSDs. At this stage, it is understood that the cause of harmonics in VSDs are from the intermittent current drawn by the capacitors charging in the VSD. The effective mitigation of harmonics will be determined on how well the high current peak values are managed as well as the current waveform on the input side of the VSD [15].

The RHT method revolves around two principles:

1. The reduction of the capacitor sizes in the power section

2. Development of a motor control processor to manage the high ripple on the DC bus voltage

The first principle of RHT involves the optimization of the power section; this was achieved by reducing the DC bus capacitance by approximately 95% as compared to that of an equivalent standard VSD. Since the current through the capacitors are directly proportional to the capacitance, the reduction in capacitance will effectively reduce the peak values of the current spikes during the capacitor charging cycle. This result will lower the current draw of the VSD; this also improves the shape of the current waveform at the input side which reduces input current harmonics [15].

The second principle of RHT is the motor control processor. This was deemed necessary because the lower DC bus capacitance would cause increased ripple on the DC bus voltage. The ripple on the DC bus will propogate to the output of the VSD as harmonics and to the output of the motor shaft as torque ripple. The motor control algorithm serves to eliminate the DC bus ripple and motor torque ripple while delivering a sinusoidal current waveform to the motor [15].

The reduction of the DC link capacitor banks can also be justified by implementing an Active IGBT rectifier [34]. This solution also requires the input supply voltage to be balanced and the load to be linear and balanced [34]. An unbalanced AC supply at the input of a VSD can also generate voltage harmonics on the rectifier supplying the DC link and therefore VSDs encounter large DC ripple voltage, which then becomes the major contributor for harmonics on the inverter output [35].

A comprehensive and thorough analysis of the RHT motor control processor was not permitted by the manufacturer but after many discussions with the development team of the RHT VSD, the following high-level summary was permitted for academic discussion purposes.

The value of the DC capacitor voltage is measured to compensate for the ripple effect. Increasing the output torque reference to the Pulse Width Modulation (PWM) inverter eliminates the increase of the DC voltage. The higher torque reference would inherently cause a higher current to be supplied by the capacitors thereby forcing the capacitor to discharge. The inverse is also true where; decreasing the output torque reference to the inverter eliminates the reduction of the DC voltage. The lower torque reference would inherently cause a lower current to be supplied by the capacitors thereby allowing the capacitor freedom to charge and eliminate the low DC voltage. Studies have shown that to effectively reject dc-link voltage ripple, the solution will most likely form part of the PWM technique [36].

The following are results from independant tests conducted by a manufacturer with two 75kW VSDs where one VSD is a standard type, with no mitigation solution of any sort and with no reduction in DC capacitance, and the other using a RHT based VSD. Figure 3.6 illustrates the typical input voltage and current waveforms of the standard 75 kW six pulse VSD. The peak currents illustrated rise up to 300 A during the capacitors charging phase. The total harmonic current distortion measured in this experiment was approximately THDi = 80% [15].

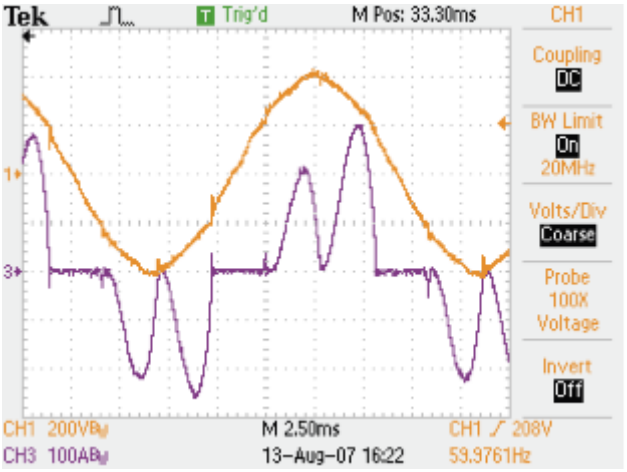



FIGURE 3.6: Typical Current and Voltage waveforms of a standard VSD without a Line Choke [15].

The previous test was repeated with a standard 75 kW VSD fitted with the addition of a line choke having 3% impedance. Figure 3.7 illustrates the input voltage and current waveforms for the configuration described. It can be clearly noted that the characteristic double-humped waveform shows a reduction in current peaks. In this case the peak current rises up to only 190 A during the capacitor charging phase. The total harmonic current distortion measured in this experiment was approximately THDi = 40% [15].

The previous two tests were based on a standard VSD; the same experiment will be performed with a RHT based VSD. Figure 3.8 illustrates the current and voltage waveforms of the RHT technology based drive. The differences in the shape of the input current waveform compared to that of the previous experiments are notably different. It can also be seen that the current peaks rise up to approximately 190 A. The reduced capacitance in the VSD has changed the shape of the input current waveform to that similar to a square-wave.

Taking a closer look at this square-wave look-alike waveform, it can be seen that the original large double-humped input current waveform is now transformed into multiple smaller, higher frequency double-humped waveforms. This is due to the lower capacitance. The lower capacitance results in more charging-discharging operations per

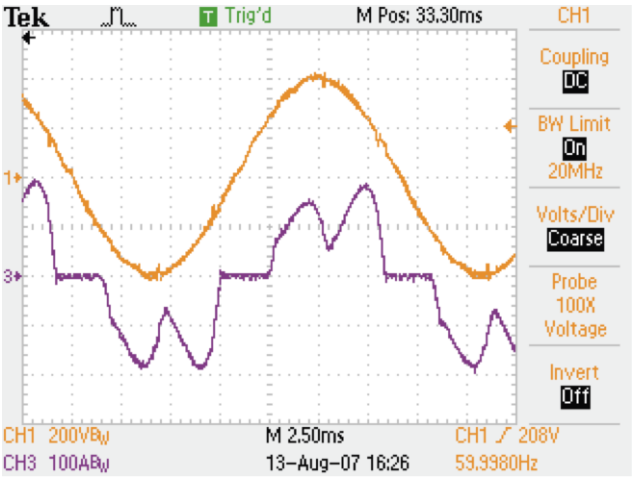



FIGURE 3.7: Typical Current and Voltage waveforms of a standard VSD with a Line Choke [15].

periodic cycle. The total harmonic current distortion measured for the square current waveform was approximately THDi = 30% [15].

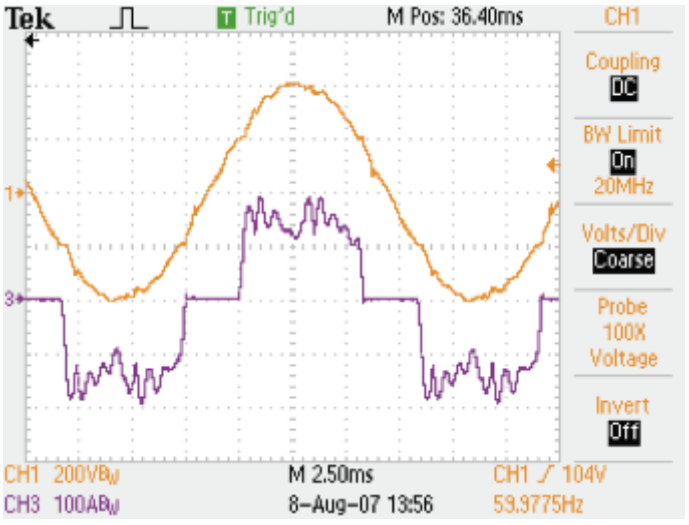



FIGURE 3.8: Typical input voltage and current waveforms of a 75kW RHT based VSD [15].

The spider diagram illustrating the various selection criterias for the multi pulse drive is illustrated in Figure 3.9.

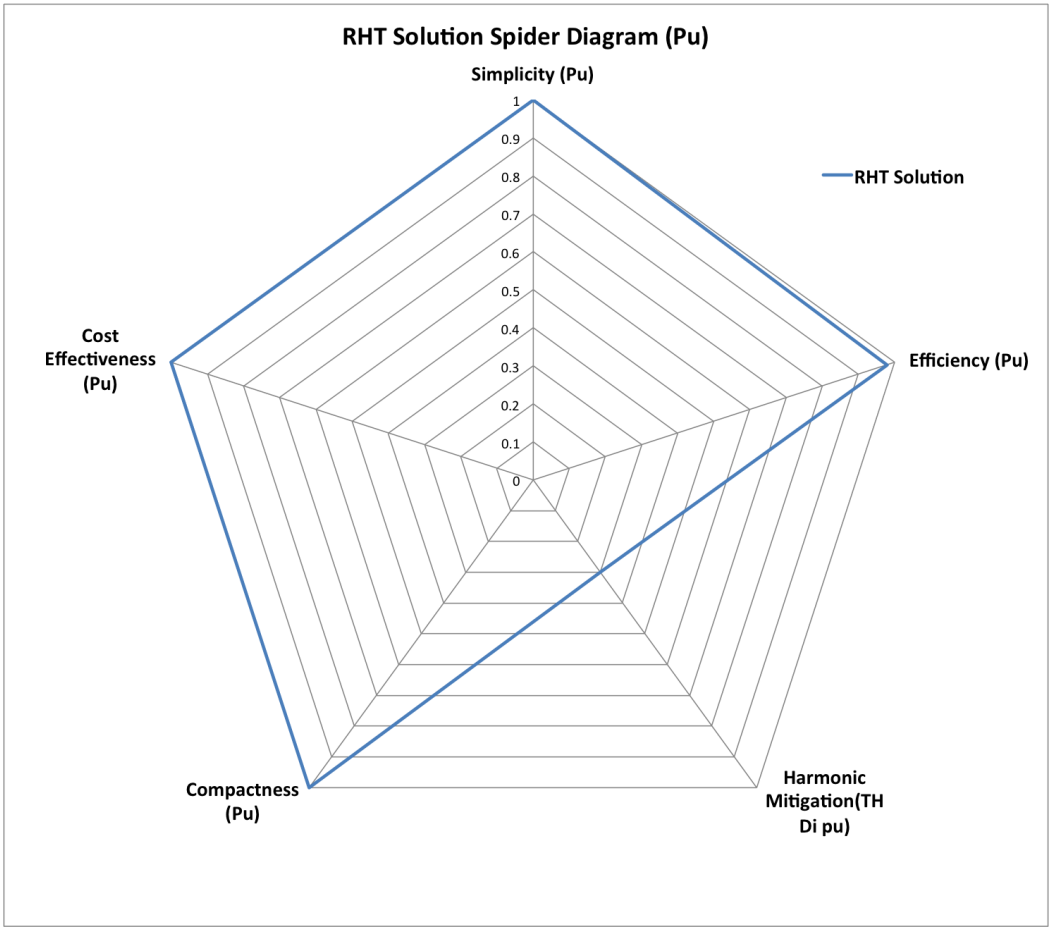



FIGURE 3.9: RHT Drive spider diagram.

## 3.8 Conclusion

The previous section looks at some of the more common harmonic mitigation solutions available for industry today. The RHT solution was then reviewed. Figure 3.10 illustrates the various harmonic mitigation solutions available with a comparison on the typical THDi (%) and typical cost ratio (%). The benchmark is against a standard 6 Pulse VSD with no additional harmonic mitigation installed. It revealed that the RHT based VSD is cheaper and also performs better than the standard six pulse VSD in terms of harmonics.

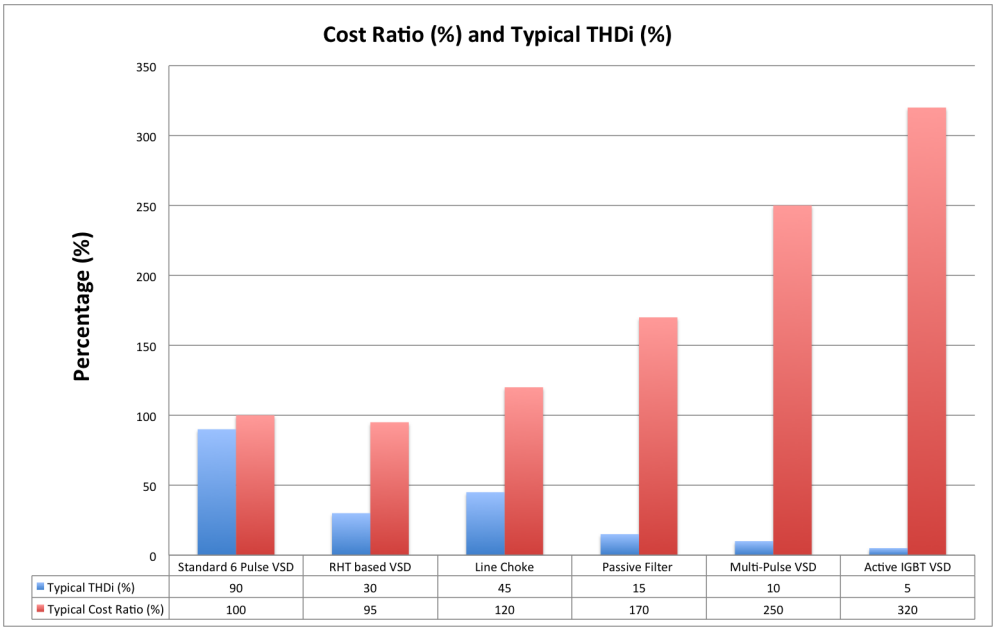



FIGURE 3.10: Overview of various harmonic mitigation solutions, illustrating the typical THDI and typical cost ratio [15].

# Chapter 4

# Simulation of a three phase rectifier circuit

## 4.1 Introduction

Spice simulation software was used to model the front end (Input section) of a three phase rectifier circuit. The purpose of the simulation was to build a simplified circuit representation of a VSD. Furthermore to reproduce the commonly known behaviour of a standard VSD and then proceed to reproduce the behaviour of the RHT VSD by reducing the size of the DC bus capacitance. The focus of the simulation model was at the input of the three phase rectifer and not the output. The primary intention of the simulation is not to calculate THDi, although THDi calculations have been done eventually, the primary intention is to observe graphically, the difference in input current waveforms of the RHT and the standard VSD model. The graphical observations are performed in both time and frequency domains.

The three phase rectifier circuit model took into account the effects of source impedance and resistance of the bridge rectifier. The impedance of any cables between the source and the rectifier input was not included in the circuit model. The parameter of interest was the input current of the rectifier when simulating the equivalent model of a standard VSD model and a RHT VSD. The input current waveform was then used to perform a Fast Fourier Transform (FFT) within the Spice simulation environment. The simulation also investigated the effect of source impedance on the harmonics generated in a three phase rectifier.

## 4.2 Circuit Modelling

### 4.2.1 Source Impedance and three phase rectifier model

The power system is considered to be a non-ideal source where its source impedance is represented in the form of a series resistance ($R_S$) and a series inductance ($L_S$). which represents the equivalent source impedance measured from the input of a VSD [30]. The source impedance could have considerable influence on the harmonics generated by the VSD and so it is included into the simulation. The inductor represents the equivalent impedance of the transformer windings and a small resistance generally represents the heat losses within the transformer [31] [10].

For the purposes of the simulation, a 3 phase, 400V, $Z_{pu} = 4\%$ Impedance, 50 kVA transformer was selected as the supply source to the three phase rectifier.

The three phase rectifier was modelled using a 6 pulse diode rectifier circuit, a resistor of 0.1 Ω to represent the arbitrary resistance of the diodes and a capacitor in parallel to the bridge rectifier to represent the DC bus capacitance of a VSD. A resistor was used to model the load. Refer to Figure 4.1 for the complete three phase rectifier representation of a VSD using Spice. The calculations for the source impedance is described in Appendix C.

## 4.3 Simulation Results

### 4.3.1 Simulation of the standard VSD model

A standard VSD model was built in Spice using the model of a three phase rectifier and some data gathered from claims made by a manufacturers datasheets. The source impedance of the earlier mentioned transformer was calculated using the derivation in Appendix C and is illustrated in Figure 4.1. A large DC bus capacitor of $C1 = 2000\mu$F is used in this simulation. The load is represented by a resistor of 20 Ω.

Using the above mentioned parameters, the model shown in Figure 4.1 was simulated for four cycles and the resulting input current is as shown in Figure 4.2. The current waveform is distorted to an extent as was seen in Figure 3.6 and Figure A.3.

The FFT of the input current waveform of the standard VSD was performed using Spice simulation software and the result is plotted in Figure 4.3.

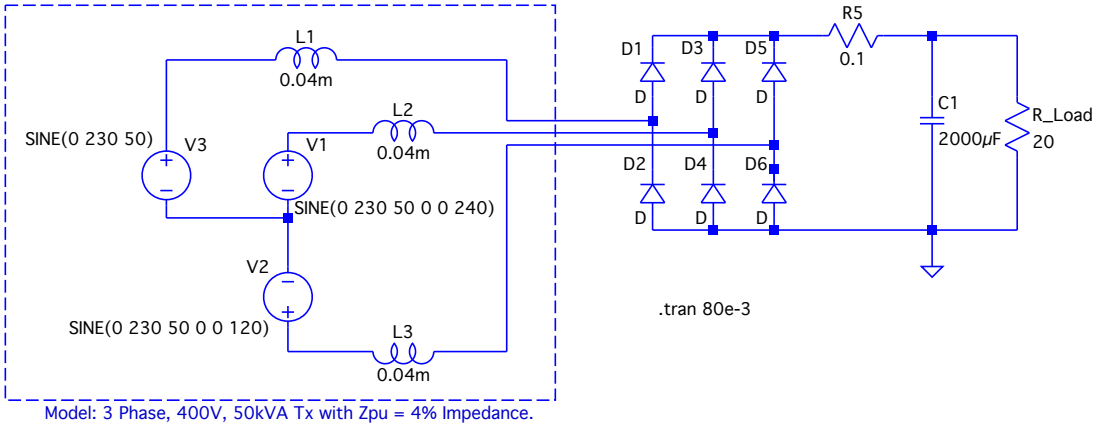



FIGURE 4.1: Circuit simulation model of a VSD with a 3 phase supply.

### 4.3.2 Simulation of the RHT VSD Model

The RHT VSD was also modelled in Spice but with a greatly reduced capacitance of 2.5% of that of a standard VSD. The source impedance was calculated in Appendix C and is illustrated in Figure 4.1. A DC bus filter capacitor of $C1 = 50\mu$F. The load is represented by a resistor of 20 Ω.

Using the above mentioned parameters, the model shown in Figure 4.1 was simulated for four cycles and the resulting input current is as shown in Figure 4.4.

The FFT of the simulated input current waveform of the RHT VSD was performed using Spice simulation software and the result is plotted in Figure 4.5.

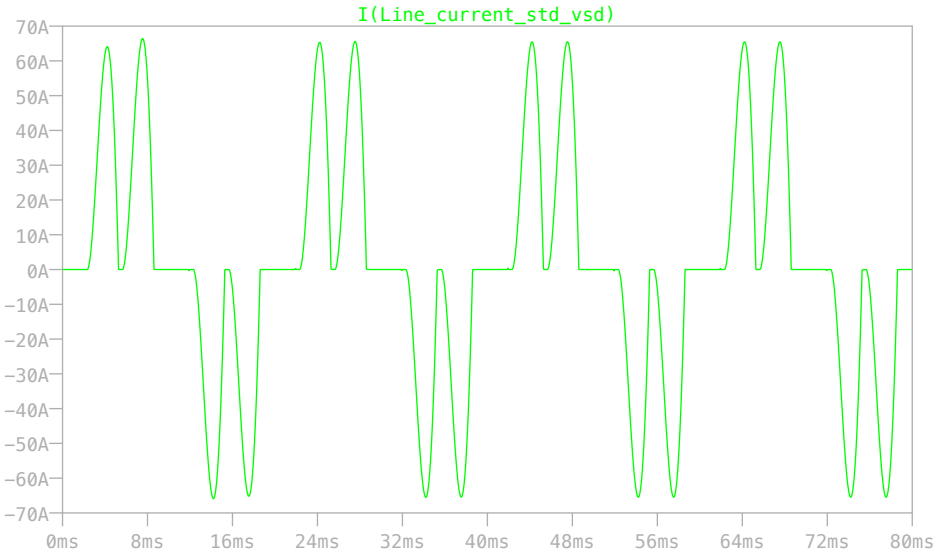



FIGURE 4.2: Simulated input current waveform of a three phase rectifier representation of a standard VSD with DC bus capacitance of, $C1 = 2000\mu$F.

### 4.3.3 Simulation of harmonics by varying DC bus capacitance and source impedance

Using the derivation from Appendix C for the source impedance measured from the input of a VSD, a further simulation was performed. The purpose of this simulation was to understand the effects of varying the DC bus filter capacitance and the source impedance. The DC bus capacitance was varied from $C1 = 50\mu F$ to $C1 = 2000\mu F$. The source impedance of the above mentioned transformer was varied from $Z_{pu} = 2\%$ to $Z_{pu} = 8\%$. The results for the simulation are tabulated in Appendix C and is illustrated Figure 4.7.

## 4.4 Conclusion

The simulated input current waveform of the standard VSD, as illustrated in Figure 4.2, is distorted to a similar extent as the claims made by the manufacturer (Figure 3.6). The simulated input current waveform of the RHT VSD, as illustrated in Figure 4.4, showed high frequency content similar to the claims made by the manufacturer (Figure 3.8).

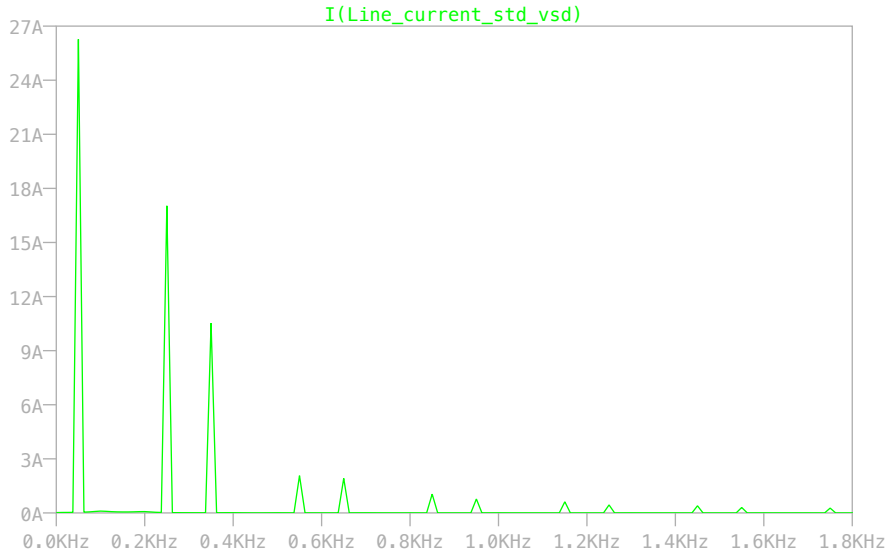



FIGURE 4.3: Simulated FFT spectrum of the input current of a three phase rectifier representation of a standard VSD with DC bus capacitance of, $C1 = 2000\mu$F.

The results were further summarized as shown by Figure 4.6. The summarized view of the FFT results confirm that the RHT VSD has a range of higher amplitude harmonics from the 13th to the 17th order. This effect is not evident in the FFT results of the standard VSD.

The RHT VSD has an advanced motor control processor that is used to reject ripple that is caused by the lower DC bus capacitance. When the DC bus ripple is at its peak, the motor control processor will increase the torque reference thereby discharging the DC bus voltage slightly. When the DC bus capacitor discharges by that slight amount, the result will be a slight reduction in the input current of the RHT VSD.

When the DC bus ripple is at its lowest, the motor control processor will decrease the torque reference thereby charging the DC bus voltage slightly. When the DC bus capacitor charges by that slight amount, the result will be a slight increase in the input current of the RHT VSD. The above mentioned increase and decrease in the input current that results from the DC ripple compensation is clearly evident in the lab experiment of the input current of the RHT VSD.

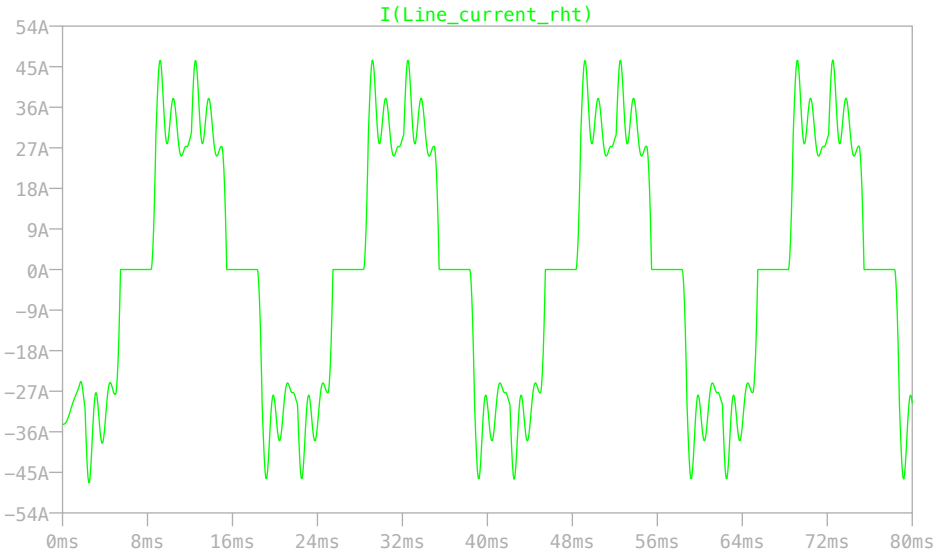



FIGURE 4.4: Simulated input current waveform of a three phase rectifier representation of a RHT VSD with DC bus capacitance of, $C1 = 50\mu$F.

The increase and decrease appears as rapid spikes on the peaks of the input current waveform, as illustrated in Figure A.2. The presence of the abovementioned phenomenon is clearly absent in the input current of the simulated model of the RHT VSD, as illustrated in Figure 4.4. This absence is due to the fact that the motor control processor was not part of the simulation model of the RHT VSD.

The simulation results of the input current harmonics as a function of DC bus capacitance and source impedance is shown in Figure 4.7 and reveal two specific phenomenon. Firstly, the reduction of DC bus filter capacitance makes a notable difference in the input current harmonics. Secondly, also according to [30] and [32], an increased source impedance results in lower input harmonics.

The results in Figure 4.7 illustrate that in a lower range of DC capacitance values (below $C1 = 600\mu$F), the size of the DC bus capacitance has more effect on the input harmonics than the source impedance. An increase in source impedance does not reduce input harmonics. Below $C1 = 600\mu$F, it can be clearly seen that, the DC bus capacitance dominate the source impedance in its ability to reduce input harmonics. When the DC capacitance was increased above $C1 = 600\mu$F, the source impedance has more effect on the input harmonics than the size of the DC bus capacitance.

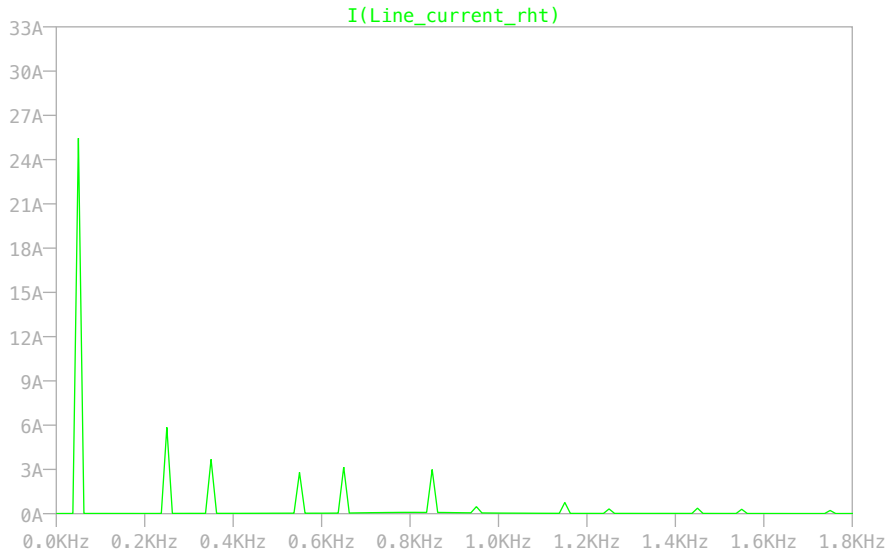



FIGURE 4.5: Simulated FFT spectrum of the input current of a three phase rectifier representation of a RHT VSD with DC bus capacitance of, $C1 = 50\mu$F.

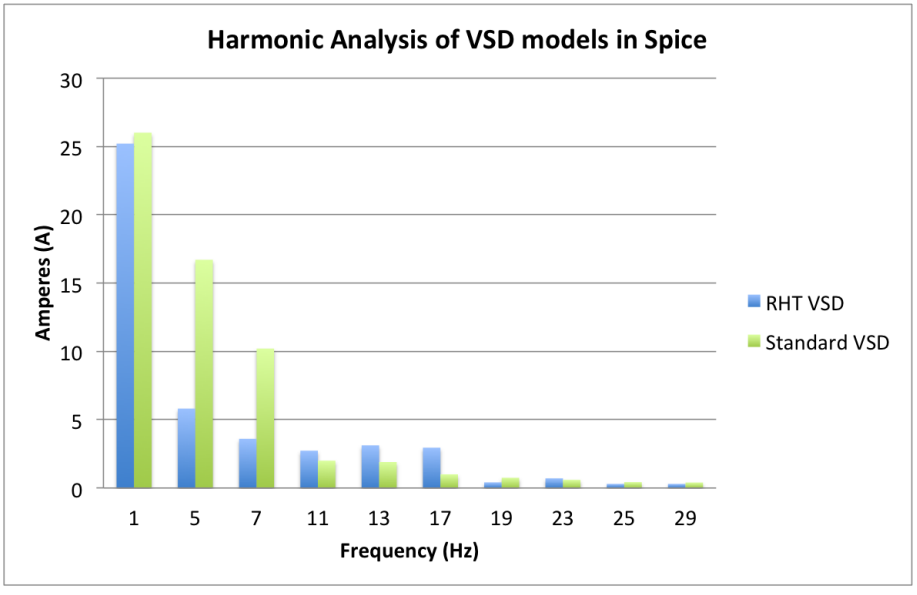



FIGURE 4.6: Summary of the simulated FFT results for a standard and RHT VSD representation using LTSpice.

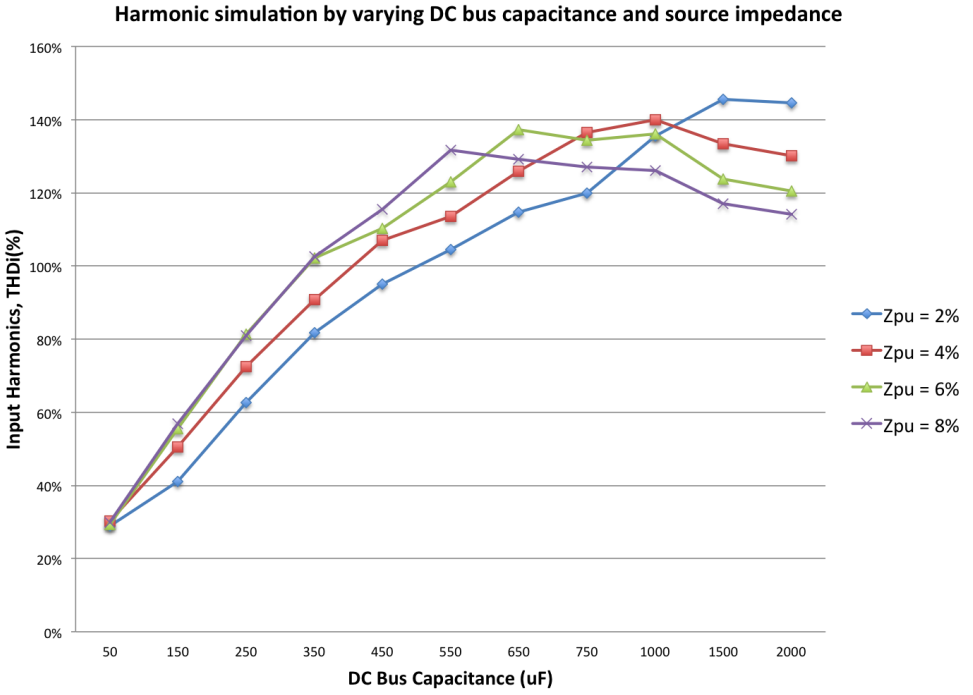



FIGURE 4.7: Simulation of input current harmonics (THDi) as the DC bus filter capacitance and source impedance are varied.

# Chapter 5

# Analysis of Experimental Results

## 5.1 Introduction

The RHT solution has illustrated its strengths in producing lower harmonic content on the line current, whilst still being affordable. This however resulted in a ripple voltage being formed on the DC bus [15]. The ripple voltage on the DC bus can produce harmonics at the output (inverter output) of the VSD [33]. As discussed earlier, the RHT VSD has an advanced motor control processor to eliminate the ripple on the DC bus. Although a comprehensive and thorough analysis of the RHT motor control processor was not permitted by the manufacturer, one could still evaluate its effectiveness by benchmarking its ability to emulate the output of a standard VSD.

A lab experiment was performed to analyze the input and output currents of the RHT based VSD and compare it to the input current of a standard VSD. The analysis done on the input section of the VSDs are described in detail in Appendix A. Furthermore, measurements were taken of the output currents of the VSDs and an analysis was done to establish if there are any differences at the output of the VSDs.

Laboratory experiments were performed under no-load condictions. As illustrated in Figure 2.3, experiments under full load would add little additional value because the harmonic currents will not increase significantly at full load. Furthermore, the purpose of the experiment was to observe the shape of the input and the output currents both in the time and frequency domain.

## 5.2 Results: Output current of the RHT VSD and the standard VSD

### 5.2.1 Time Domain analysis of the output currents of the RHT VSD and the standard VSD

Figure 5.1 and Figure 5.2 illustrate the output currents of the RHT VSD as well as the standard VSD respectively. A visual inspection of these two waveforms suggest that there are no significant variations. The frequency domain analysis of the output waveforms will be performed to further support this claim.

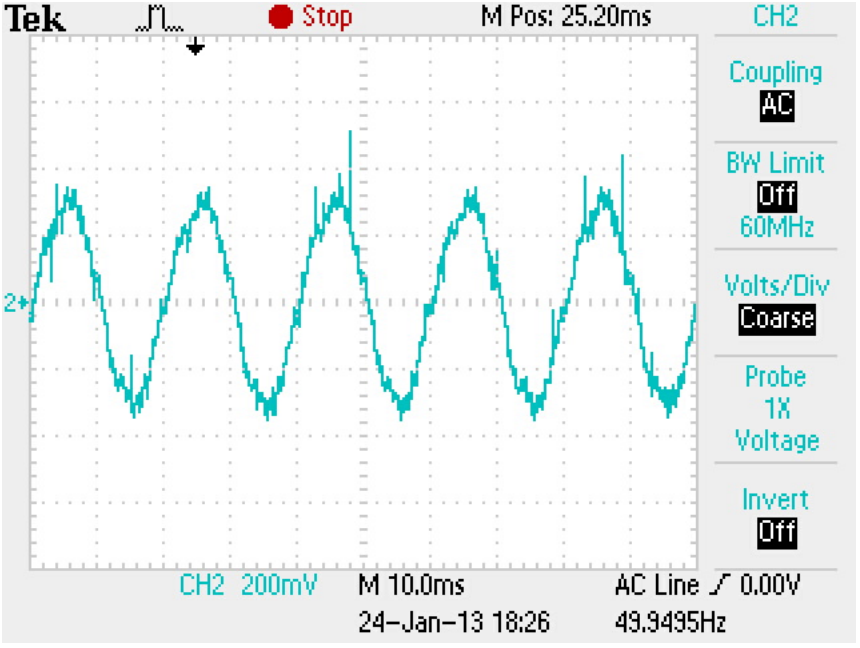



FIGURE 5.1: Output current measurement of the RHT VSD.

### 5.2.2 Frequency Domain analysis of the output currents of the RHT VSD and the standard VSD

The FFT of the output waveforms are also performed with the data that is captured on the oscilloscope. Matlab simulation software was again used to perform the FFT analysis of the output waveforms. Refer to Appendix B for the Matlab code used for the FFT analysis [37] [38]. The RHT VSD as well as the standard VSD was tested under no-load and steady state conditions using the same motor. The FFT results are plotted on a per unit basis, where both the fundamental currents were assumed to be the same and the amplitudes of the rest of the harmonic components were compared to the fundamental.

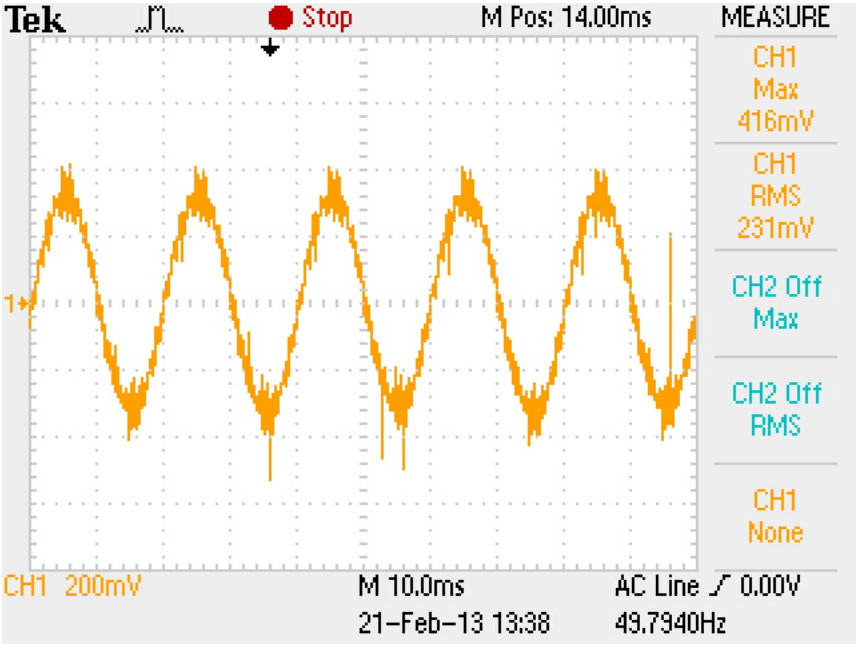



FIGURE 5.2: Output current measurement of the standard VSD.

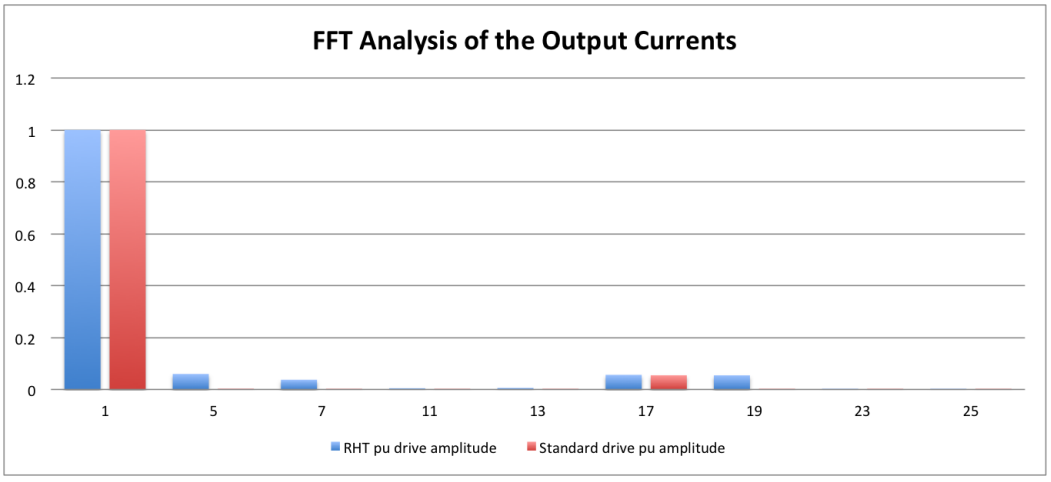



FIGURE 5.3: FFT Analysis of the output currents of the RHT VSD and the standard VSD.

## 5.3 Conclusion

Figure 5.3 is a bar graph illustration of the FFT results of the output current of the VSDs. It is clearly evident that there are no significant differences in the harmonic content of the output waveforms of both VSDs. The 5th and the 7th harmonic component of the RHT VSD show a variation when compared to the standard VSD. This deviation is not sufficient cause for concern to the performance of the motor. Similarly, the 17th and the

19th order harmonic of the output current of the RHT VSD displays some negligable variation.

Figure A.4 is a bar graph illustration of the FFT results of input currents of the VSDs. The RHT VSD shows better performance in the lower order harmonics when compared to the standard VSD. These being the 13th order harmonic and lower. However, the RHT VSD shows deteriorating harmonic performance from the 17th order onwards. This behaviour is similar to the that seen in the simulation results in Figure 4.6 . The trade-off would be to have better harmonics performance in the lower order at the cost of having slightly higher harmonics in the higher orders.

# Chapter 6

# Conclusion

The focus of this study revolved around harmonics and VSDs. These two topics were discussed into further depth including the advantages of using a VSD and the cause and effects of harmonics. It was shown that the harmonics generated by VSDs can have a significant impact on the overall power factor of the installation. Some of the well known solutions for harmonic mitigation were also discussed. Particular attention was given to a new solution called RHT. The RHT solution was benchmarked against the standard VSD technology and proved to be successful in its ability to produce lower harmonics as well as to draw less current. The RHT solution is built on the idea that the size of the DC capacitor banks are significantly reduced and it also employs the aid of a motor control processor to compensate for the additional ripple appearing on the DC bus voltage.

Software simulation of the VSD circuit and laboratory experiments support the claim of lower harmonics with lower DC bus capacitance. However, when examining the frequency spectrum of the input current of the VSD, it was noted that there were higher order harmonic content starting above the 13th order. This suggested that the RHT VSD improved the harmonic performance below the 13th order at the cost of having slightly higher harmonics content above the 13th order. These higher order harmonics are a direct result of the motor control processor that is used to mitigate the DC bus ripple. Furthermore, the effect of ripple on the DC bus raised concerns of harmonics on the output current of the RHT VSD. The laboratory experiment was conducted to evaluate the effectiveness of the motor control processor to eliminate any harmonic content on the output current of the RHT VSD.

The laboratory experiments confirm that the RHT VSD successfully maintains a sinusoidal output current waveform similar to that of the standard VSD, further emphasizing the effectiveness of the motor control processor of the RHT. In conclusion, the RHT

VSD has a higher efficiency due to the lower input current harmonics which results in a higher total power factor. Therefore the RHT VSD would be able to deliver lower reactive power than the standard VSD which would explain the lower current drawn by the RHT VSD.

# Appendix A

# Lab Experiment

## A.1 Analysis of the RHT VSD output voltage (Lab Experiment)

### A.1.1 Objective

The objective of the experiment is to investigate the difference in the output current harmonics of a RHT based VSD to that of an equivalent standard VSD. The investigation will serve to highlight whether the output power quality of the RHT based VSD was compromised due to its reduced capacitor bank sizes and the motor control processor that manages the DC ripple that results from the smaller capacitance. If differences in the outputs of the two VSDs are found, arguments will be made to conclude the overall effectiveness of the RHT solution for harmonic mitigation.

### A.1.2 Laboratory Equipment

The supply for the experiment is a 50 Hz balanced 3 phase, 4-wire system of 400 V line-to-line. A 3 phase variac is connected at the bench so that the line voltage may be kept steady at 400 V line-to-line. The laboratory equipment used to successfully complete the experiment are as follows.

#### A.1.2.1 Measurement Box

A measurement box is used to take measurement from the VSDs. The measurement box consists of six voltage transformers (VTs) to measure the phase and line voltages as well as four current transformers (CTs) to measure the line currents. All VTs have

a winding ratio of approximately 31:1 and all CTs have a winding ratio of 10:1. The impedance at the termination of each of the CT outputs is 1 OHM.

#### A.1.2.2 Schneider Electric VSD (RHT VSD)

Rated at 2.2kW, 400V, 4.5A will be used for measurements for RHT results. No line chokes or motor chokes will be installed. When measurements are taken, the RHT VSD will be running under no-load conditions at the rated speed of 50Hz.

#### A.1.2.3 Siemens Simatics VSD (Standard VSD)

Rated at 2.2kW, 400V, 4.5A will be used for measurements for standard VSD results. No line chokes or motor chokes will be installed. When measurements are taken, the standard VSD will be running under no-load conditions at the rated speed of 50Hz.

#### A.1.2.4 Tektronics Oscilloscope

An oscilloscope is to be used to measure the required voltage and current waveforms of the above mentioned VSDs. The measurement data will be captured (.csv format). The screenshot of the waveforms will also be captured.

### A.1.3 Experiment A (RHT VSD)

The experiment will be setup with the equipment illustrated in Figure A.1.

#### A.1.3.1 RHT VSD input current measurement

The RHT VSD is to be switched ON and the motor is to be ramped up to the rated speed of 50 Hz. Channel 1 of the oscilloscope will be used to measure the input current on one of the phases of the RHT VSD. It is recommended that more than one cycle of the periodic signal is captured.

The FFT analysis done on the waveform with multiple cycles was found to provide results of higher quality. This is because having more cycles of the sinusoidal waveform increased the frequency resolution of the signal. This can be seen in equation A.1, by increasing the number of samples (N) and also the sampling period (T), the frequency resolution was improved.

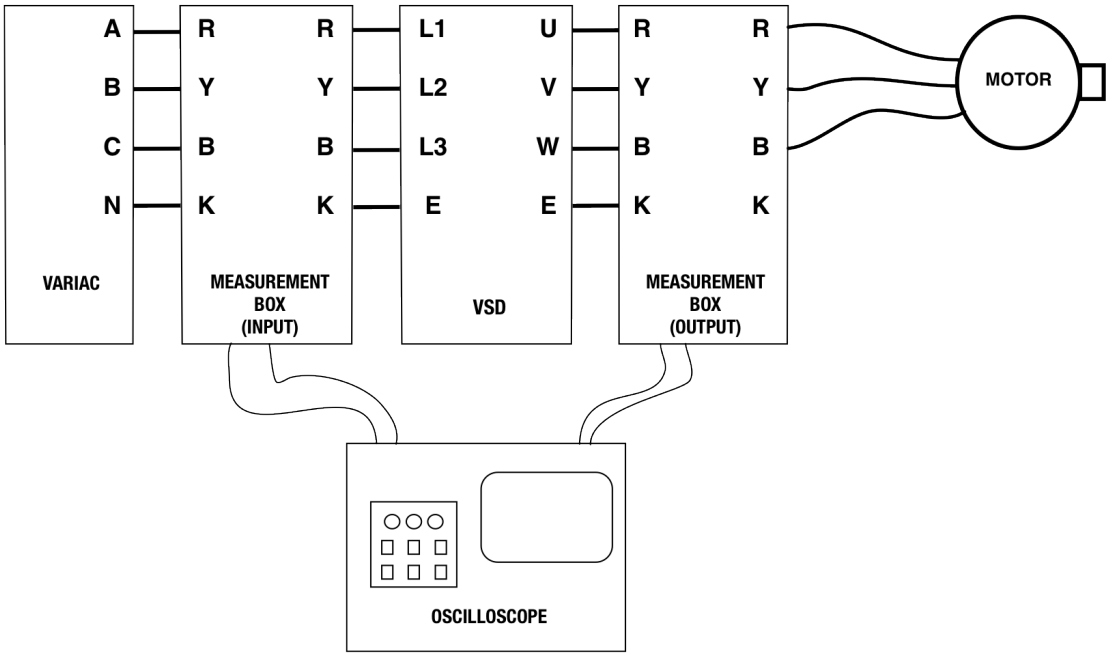



FIGURE A.1: The experiment was conducted with the VSD setup as shown in this diagram.

$$\Delta\omega = \frac{2\pi}{NT} \tag{A.1}$$

The input current is first mesured so that it can be compared to the expected waveforms shown in the section introducing the RHT technology. Once the input waveform is confirmed, one can continue to measure the output current waveform of the RHT VSD. The input current waveform as well as the waveform data are to be captured and stored as a picture format (.jpg) and as a spreadsheet (.csv) respectively.

#### A.1.3.2 RHT VSD output current measurement

Repeat the input current measurement procedure when measuring the output current of the RHT VSD on Channel 2 of the oscilloscope.

### A.1.4 Experiment B (Standard VSD)

The experiment will be setup with the equipment illustrated in Figure A.1.

#### A.1.4.1 Standard VSD input current measurement

The standard VSD is to be switched ON and the motor is to be ramped up to the rated speed of 50 Hz. Channel 1 of the oscilloscope will be used to measure the output current on one of the phases of the standard VSD. It is recommended that more than one cycle of the periodic signal is captured.

The FFT analysis done on the waveform with multiple cycles was found to provide results of higher quality. This is because having more cycles of the sinusoidal waveform increased the frequency resolution of the signal. This can be seen in equation A.1, by increasing the number of samples (N) and also the sampling period (T), the frequency resolution was improved.

The input current is first mesured so that it can be compared to the expected waveforms of that of a standard VSD. Once the input waveform is confirmed, one can continue to measure the output current waveform of the standard VSD. The input current waveform as well as the waveform data are to be captured and stored as a picture format (.jpg) and as a spreadsheet (.csv) respectively.

#### A.1.4.2 Standard VSD output current measurement

Repeat the input current measurement procedure when measuring the output current of the standard VSD on Channel 2 of the oscilloscope.

### A.1.5 Results: Input current of the RHT VSD and the standard VSD

#### A.1.5.1 Time Domain analysis of the Input currents of the RHT VSD and the standard VSD

Figure A.2 can be compared to the results illustrated in Figure 3.8. The significantly reduced distortion and the generally sinusoidal wave shape is evident as a result of the reduced capacitance of the RHT VSD.

Figure A.3 can be compared to the results illustrated in Figure 3.6. The significant distortion wave shape is evident as a result of the higher capacitance of the standard VSD.

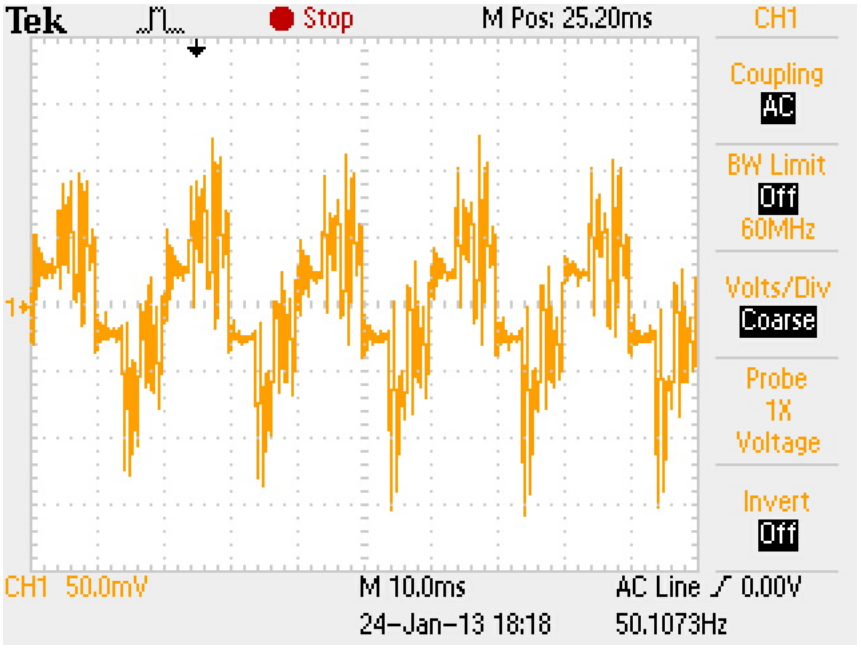



FIGURE A.2: Input current measurement of the RHT VSD.

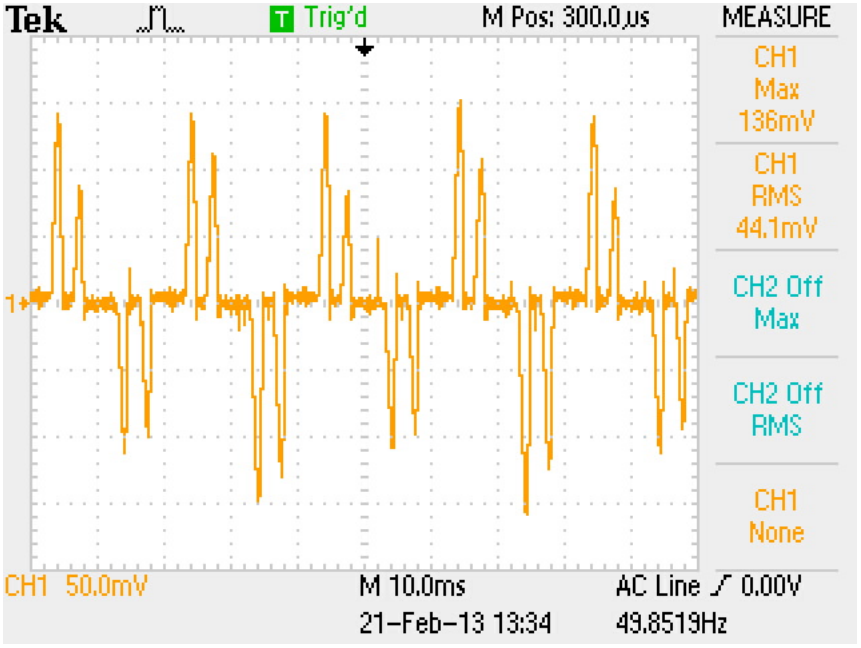



FIGURE A.3: Input current measurement of the standard VSD.

### A.1.5.2 Frequency Domain analysis of the Input currents of the RHT VSD and the standard VSD

The FFT of the input waveforms are performed with the data that is captured on the oscilloscope. Matlab simulation software was used to perform the FFT analysis of the input waveforms. Refer to Appendix A for the Matlab code used for the FFT analysis. The RHT VSD as well as the standard VSD was tested under no-load conditions using the same motor. The FFT results are plotted on a per unit basis and the harmonic components were compared to the fundamental.

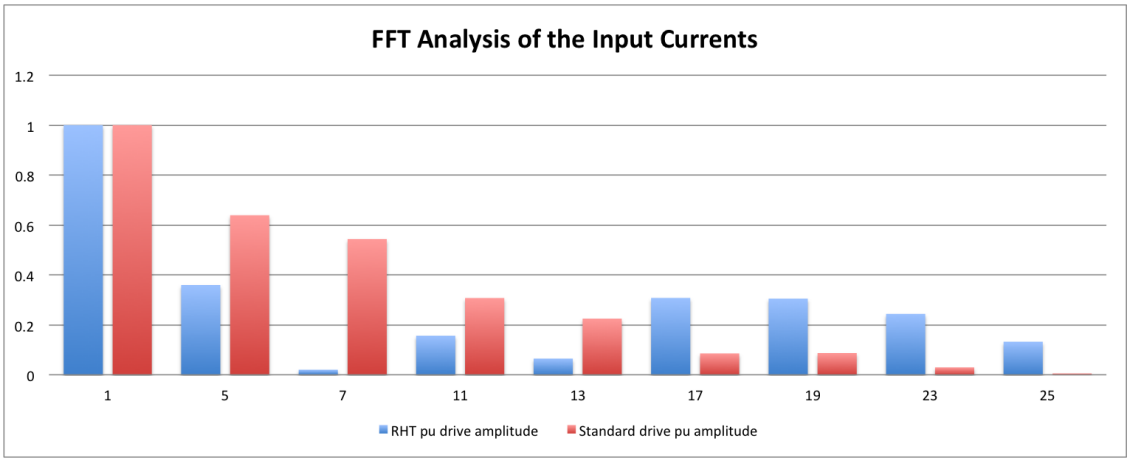



FIGURE A.4: FFT Analysis of the input currents of the RHT VSD and the standard VSD.

Figure A.4 is a bar graph illustration of the FFT results of input currents of the VSDs.

# Appendix B

# MATLAB Code

The code below represent the different attempts to read the contents of a csv file into an array. The data is the samples are stored in a csv file that is populated by the oscilloscope. The csvread command simply takes the csv file and turns it into a matrix. The data in the array is then used to perform a FFT (Fast Fourier Transform) which reveals the frequency components in the time domain signal captured by the oscilloscope. The frequency axis on the plot (x-axis) resulting from the FFT operation was then scaled until the fundamental component was correctly aligned with the frequency of 50 Hz [37] [38]. The remainder of the expected harmonic components (5th, 7th, 11th, 13th etc) were assumed to be aligned automatically their respective frequencies (250 Hz, 350 Hz, 550 Hz, 650 Hz respectively). Once the frequencies were correctly aligned to the respective harmonic components, their amplitudes were noted.

```
M=csvread('data4.csv',0,4,[0,4,2499,4]);
Gain = 2;            % The gain is there to compensate
Xscale =  25.6;    % Used to scale the x-axis  to match the frequencies
    of the x-axis to the correct harmonic components.

L=length(M);           % Length of array

%##############################################%
           %Failed Attempt #1

% fs = 100000;                          % Sample frequency (Hz)
%
% m = length(M);          % Window length or the Number of samples
```

```
% n = pow2(nextpow2(m));  % Transform length
% y = fft(M,n);           % DFT
% f = (0:n-1)*(fs/n);     % Frequency range
% power = y.*conj(y)/n;   % Power of the DFT
%
% plot(f,power)
% xlabel('Frequency (Hz)')

%##############################################%
            %Failed Attempt #2
%
% Fs = 100000;           % Set Sampling frequency
%
% n = pow2(nextpow2(L));  % Transform length of Array
% y = fft(M,L);           % DFT
% f = (0:n-1)*(Fs/n);     % Frequency range
%
% nyquist = 1/Fs;
% freq = (1:L/2)/(L/2)*nyquist;
% plot(freq,power)
% xlabel('Frequency')
%##############################################%
           %Working Attempt
NFFT = 2^nextpow2(L);      % Transform length  of Array
Y=fft(M,NFFT)/L;
f=500*Xscale*linspace(0,1,NFFT/2+1);
plot(f,Gain*abs(Y(1:NFFT/2+1)))
xlabel('Frequency (Hz)')
title('FFT')

%##############################################%
```

# Appendix C

# Source Impedance Modelling

## C.1 Basic Assumptions

The calculation of the source impedance was undertaken with certain assumptions. The six-pulse VSD is supplied by a balanced three phase power supply. The supply voltage is represented by a sinusoidal phase to neutral voltage of 230V. The impedance of the source is represented using a series inductance and a series resistance [30] [39]. Considering that the rectifier circuit forms part of the input stage of a high power load, the equivalent series resistance that forms part of the source impedance is small and is neglected or assumed to be less that 1% of the effective impedance of the series inductance (Ls) [31] [10].

For simplicity of the model, a small resistance of approximately 1mΩ is lumped into the internal model of the inductance and the model of the complete supply source is shown in Figure C.1 [40] [41]. The DC bus filter is modelled using a single capacitor and produces a DC voltage with low-frequency, low-amplitude ripple and for simplicity [42], the rectifier load is modelled using a resistor.

## C.2 Derivation of source impedance parameters

The system parameters and variables were normalized so that the results obtained in harmonic analyses are independent from voltage and current levels [42]. The source impedance, $Z$, of a transformer with impedance $Z_{pu} = 4\%$, is calculated using Equation C.1 [43] [42].

$$Z = Z_{base} \times Z_{pu} \tag{C.1}$$

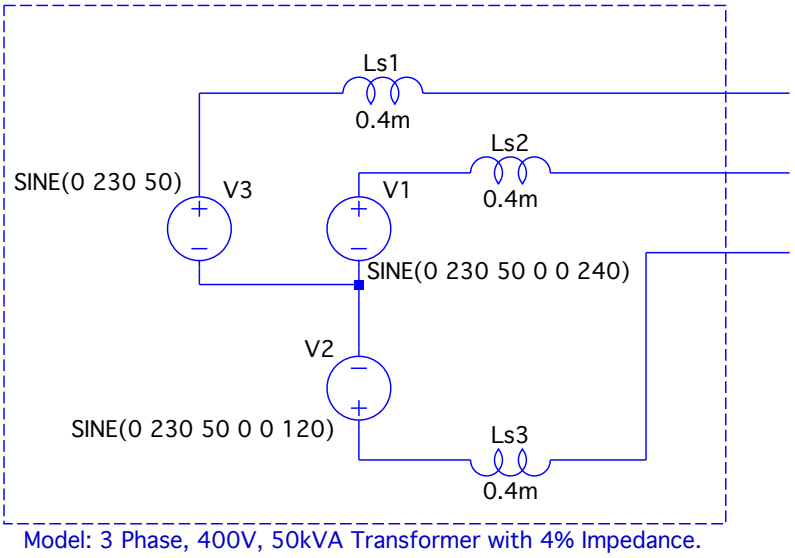



FIGURE C.1: Simulation circuit model of a 3 phase supply.

The base impedance, $Z_{base}$, is calulated from base voltage, $V_{base}$, and base current, $I_{base}$, as shown in Equation C.2 [43].

$$Z_{base} = \frac{V_{base}}{I_{base}} \tag{C.2}$$

The voltage base, $V_{base}$, is calulated from line voltage at the secondary of the transformer, $V_L$, as shown in Equation C.3 [43].

$$V_{base} = \frac{V_L}{\sqrt{3}} \tag{C.3}$$

The current base, $I_{base}$, is simply the current through each phase, $I_L$, and is as shown in Equation C.4 [43].

$$I_{base} = I_L \tag{C.4}$$

## C.3 Simulation of input harmonics by varying DC bus capacitance and source impedance

From the basic assumptions and the derivation in the previous sections, a further analysis was conducted, using the model shown in Figure 4.1, to highlight the effect of DC bus capacitance on the amount of harmonics generated by a VSD. The analysis was repeated using a source with varying source impedance.

| Zpu = 2% | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **C1 (uF)** | **H1** | **H5** | **H7** | **H11** | **H13** | **H17** | **H19** | **H23** | **H25** | **H29** | **THDi(%)** |
| **50** | 14.5 | 3.22 | 1.55 | 1.305 | 0.995 | 0.799 | 0.73 | 0.58 | 0.57 | 0.45 | **29%** |
| **150** | 14.5 | 4.34 | 2.3 | 1.8 | 1.36 | 1.22 | 1.11 | 1.06 | 1.03 | 1.13 | **41%** |
| **250** | 14.8 | 6.3 | 3.22 | 2.71 | 2.05 | 2.04 | 1.8 | 2.13 | 2.2 | 2.77 | **63%** |
| **350** | 14.8 | 8.066 | 4.4 | 3.4 | 2.84 | 2.75 | 2.84 | 3.26 | 3.44 | 2.12 | **82%** |
| **450** | 15.04 | 9.402 | 5.8 | 3.86 | 3.85 | 3.44 | 3.9 | 3.83 | 2.911 | 1.42 | **95%** |
| **550** | 15.15 | 10.43 | 7 | 4.16 | 4.31 | 4.52 | 4.442 | 3.3 | 2.31 | 0.95 | **105%** |
| **650** | 15.2 | 11.3 | 8.21 | 4.61 | 5.02 | 5.4 | 4.7 | 2.66 | 1.753 | 0.9 | **115%** |
| **750** | 15.2 | 11.5 | 8.93 | 5.49 | 5.56 | 5.5 | 4.6 | 2.25 | 1.25 | 0.95 | **120%** |
| **1000** | 15.47 | 13.08 | 11.18 | 7.7 | 6.59 | 4.83 | 3.74 | 1.65 | 0.933 | 0.66 | **136%** |
| **1500** | 15.7 | 14 | 12.75 | 9.23 | 7.4 | 3.96 | 2.49 | 0.688 | 0.53 | 0.57 | **145%** |
| **2000** | 15.7 | 14.04 | 12.77 | 9.18 | 7.28 | 3.56 | 1.96 | 0.706 | 0.5 | 0.612 | **145%** |

FIGURE C.2: Simulation results of THDi vs DC bus capacitance with source impedance, $Z_{pu} = 2\%$.

| Zpu = 4% | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **C1 (uF)** | **H1** | **H5** | **H7** | **H11** | **H13** | **H17** | **H19** | **H23** | **H25** | **H29** | **THDi(%)** |
| **50** | 14.6 | 3.39 | 1.77 | 1.305 | 1.04 | 0.771 | 0.765 | 0.55 | 0.62 | 0.45 | **30%** |
| **150** | 14.65 | 4.511 | 2.5 | 1.95 | 1.65 | 1.502 | 1.54 | 1.8 | 2.52 | 2.7 | **50%** |
| **250** | 14.7 | 6.255 | 3.4 | 2.94 | 2.65 | 3.1 | 4 | 3.85 | 2.5 | 0.6 | **72%** |
| **350** | 14.8 | 7.9 | 4.7 | 3.85 | 4.1 | 5.6 | 5.2 | 2.12 | 0.98 | 0.54 | **91%** |
| **450** | 14.9 | 9.72 | 6.15 | 5.3 | 6.5 | 5.72 | 4.1 | 1.125 | 0.56 | 0.49 | **107%** |
| **550** | 15 | 10 | 7.311 | 6.673 | 7.35 | 5.15 | 3.31 | 0.5 | 0.64 | 0.261 | **114%** |
| **650** | 15.11 | 11.13 | 9.02 | 8 | 7.6 | 4.6 | 2.5 | 2.66 | 0.446 | 0.18 | **126%** |
| **750** | 15.25 | 12.75 | 11.2 | 8.6 | 7.15 | 3.92 | 2.14 | 0.24 | 0.46 | 0.16 | **137%** |
| **1000** | 15.53 | 13.8 | 12.44 | 8.5 | 6.54 | 3.1 | 1.66 | 0.05 | 0.375 | 0.57 | **140%** |
| **1500** | 15.55 | 13.6 | 12 | 7.85 | 5.76 | 2.3 | 0.94 | 0.34 | 0.7 | 0.422 | **133%** |
| **2000** | 15.42 | 13.5 | 11.6 | 7.4 | 5.1 | 1.84 | 0.5 | 0.6 | 0.86 | 0.45 | **130%** |

FIGURE C.3: Simulation results of THDi vs DC bus capacitance with source impedance, $Z_{pu} = 4\%$.

| Zpu = 6% | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **C1 (uF)** | **H1** | **H5** | **H7** | **H11** | **H13** | **H17** | **H19** | **H23** | **H25** | **H29** | **THDi(%)** |
| **50** | 14.5 | 3.3 | 1.77 | 1.16 | 0.97 | 0.68 | 0.69 | 0.5 | 0.62 | 0.45 | **29%** |
| **150** | 14.6 | 4.48 | 2.48 | 1.95 | 1.8 | 1.9 | 2.5 | 3.886 | 2.66 | 0.75 | **56%** |
| **250** | 14.72 | 6.39 | 3.64 | 3.54 | 3.5 | 6 | 5.15 | 1.26 | 0.8 | 0.33 | **81%** |
| **350** | 14.85 | 8.8 | 4.86 | 6.05 | 7.222 | 5.4 | 3.2 | 0.443 | 0.675 | 0.22 | **102%** |
| **450** | 15 | 9.2 | 6.71 | 7.83 | 7.84 | 4.16 | 1.8 | 0.631 | 0.68 | 0.13 | **110%** |
| **550** | 15.15 | 11 | 9.5 | 8.5 | 7.2 | 3.12 | 1.24 | 0.575 | 0.3 | 0.39 | **123%** |
| **650** | 15.38 | 13.58 | 12 | 8.22 | 6.13 | 2.96 | 1.58 | 0.01 | 0.3 | 0.4 | **137%** |
| **750** | 15.6 | 13.6 | 12.12 | 7.96 | 5.99 | 2.56 | 1.25 | 0.125 | 0.4 | 0.48 | **134%** |
| **1000** | 15.66 | 13.46 | 11.9 | 8.5 | 7.45 | 1.83 | 0.583 | 0.33 | 0.483 | 0.23 | **136%** |
| **1500** | 15.58 | 13.28 | 11.31 | 6.72 | 4.45 | 1.19 | 0.38 | 0.68 | 0.723 | 0.274 | **124%** |
| **2000** | 15.4 | 13 | 10.9 | 6.3 | 3.86 | 0.85 | 0.612 | 0.812 | 0.703 | 0.3 | **121%** |

FIGURE C.4: Simulation results of THDi vs DC bus capacitance with source impedance, $Z_{pu} = 6\%$.

| Zpu = 8% | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **C1 (uF)** | **H1** | **H5** | **H7** | **H11** | **H13** | **H17** | **H19** | **H23** | **H25** | **H29** | **THDi(%)** |
| **50** | 14.55 | 3.3 | 1.74 | 1.207 | 1.1 | 0.715 | 0.75 | 0.56 | 0.74 | 0.72 | **30%** |
| **150** | 14.61 | 4.683 | 2.51 | 2.31 | 2.02 | 3.18 | 3.8 | 2.43 | 0.645 | 0.68 | **57%** |
| **250** | 14.72 | 6.42 | 4.15 | 4.05 | 5.6 | 5.2 | 2.77 | 0.77 | 0.64 | 0.26 | **81%** |
| **350** | 14.9 | 8.15 | 5.388 | 7.8 | 7.88 | 3.61 | 1.28 | 0.765 | 0.53 | 0.18 | **103%** |
| **450** | 15 | 10.01 | 8.71 | 8.42 | 6.88 | 2.2 | 0.97 | 0.443 | 0.1 | 0.49 | **116%** |
| **550** | 15.5 | 13.34 | 11.76 | 7.83 | 5.6 | 2.4 | 1.11 | 0.17 | 0.33 | 0.33 | **132%** |
| **650** | 15.65 | 13.44 | 11.83 | 7.43 | 5.31 | 2 | 0.685 | 0.383 | 0.432 | 0.36 | **129%** |
| **750** | 15.62 | 13.4 | 11.67 | 7.07 | 5 | 1.577 | 0.425 | 0.367 | 0.385 | 0.26 | **127%** |
| **1000** | 15.7 | 13.34 | 11.7 | 7 | 5 | 1.6 | 0.463 | 0.463 | 0.463 | 0.175 | **126%** |
| **1500** | 15.433 | 12.92 | 10.65 | 5.75 | 3.36 | 0.55 | 0.68 | 0.75 | 0.6 | 0.31 | **117%** |
| **2000** | 15.275 | 12.66 | 10.26 | 5.3 | 2.94 | 0.555 | 0.84 | 0.74 | 0.44 | 0.3 | **114%** |

FIGURE C.5: Simulation results of THDi vs DC bus capacitance with source impedance, $Z_{pu} = 8\%$.

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