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A proposed test system and strategy for the production testing of pulse code modulation codecs.

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3 PROPOSED TEST SYSTEM LAYOUT

In chapter 2 the the test system parameters, sample size and system frequencies, where specified. In addition, an adaptive measurement technique has been suggested in order to provide a solution to the problem of input signal resolution. All this is common to any test system layout chosen. The purpose here is to give a brief account of how the layout, proposed in the present work, was arrived at and to give a description of its operation.

3.1 Description of proposed test system

The test system proposed is similar to that given by Dell [1981]. The difference between the proposed test system and that suggested by Dell lies mainly in the test signal generation required for the encoder under test section. Dell uses a commercially available digital signal generator which produces an analcgue sinusoidal signal. In the proposed test system, presented in the present work, all test signal generation is done in software and a digital to analogue converter is used to convert the digital signal to an analogue equivalent which is then applied to the input of the encoder under test. For the decoder under test section, signal generation for the proposed system is the same as that suggested by Dell.

The block schematic of the proposed test system is given in figure 51. The system is configured in such a manner so as to perform the half channel tests required for specifying the performance of the codec under test. This is done by

configuring the encoder section of the codec under test in cascade with a software implementation of an ideal decoder. Similarly, the decoder section of the codec under test is cascaded with a software implementation of an ideal encoder.

As stated previously, a digital to analogue converter is provided in order to convert the digital test signal, generated by the test system software, into

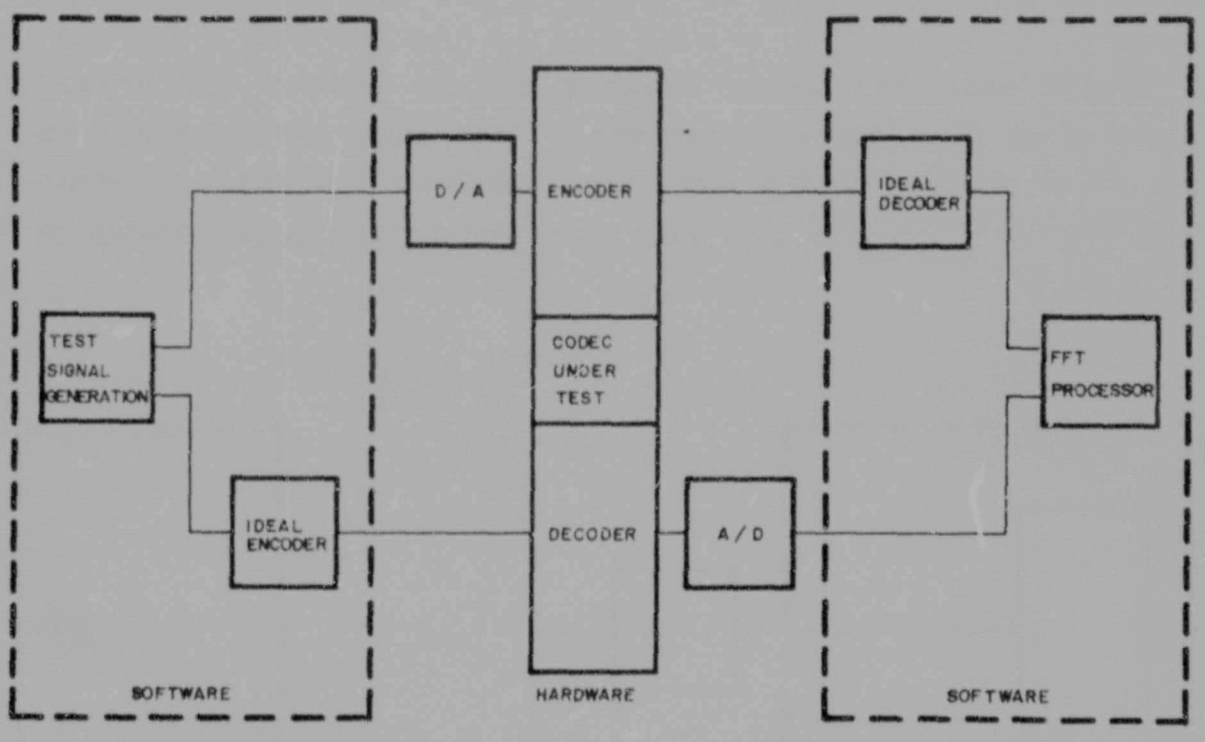

FIGURE 5! BLOCK SCHEMATIC OF PROPOSED TEST SYSTEM

an analogue equivalent so as to excite the encoder section of the codec under test. An analogue to digital converter is provided in order to convert the analogue output information from the decoder under test into a digital equivalent for processing by the test system software.

The test system software provides system control. In addition it performs the generation of the signal stimulus, required to excite the codec under test, and processing of the output information from the encoder and decoder sections of the codec under test, so as to provide quantization distortion and gain tracking values for various levels of input signal. Hence for the proposed test system all signal generation and processing is done in software. A point to note at this stage is that the encoder and decoder sections of the codec under test are configured in parallel. This can be seen from figure 51.

During the course of the present work, the possibility of configuring the sections of the codec under test in a serial configuration was investigated. The block schematic of this proposed layout is shown in figure 52.

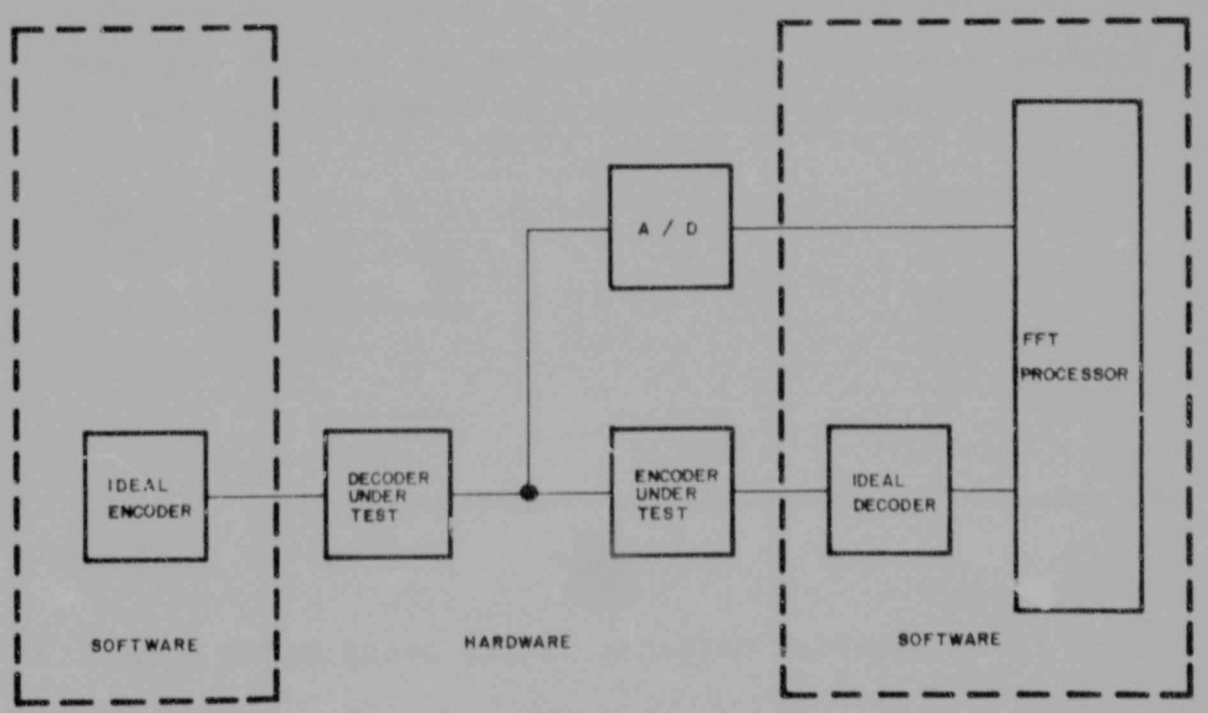

FIGURE 52 BLOCK SCHEMATIC OF SYSTEM LAYOUT WITH ENCODER AND DECODER SECTIONS OF CODEC UNDER TEST IN A SERIAL CONFIGURATION.

The signal stimulus generated in software is passed through an ideal encoder, also implemented in software, and is used to excite the decoder section of the codec under test. The output of the decoder section is converted by an A/D converter and is processed by the system software in order to obtain quantization distortion and gain tracking values pertaining to the decoder under test. At the same time the analogue output of the decoder is used to excite the encoder under test. The output of the encoder is passed through a ideal decoder, again implemented in software, before being processed by the system software to obtain performance values for the encoder under test.

This particular configuration has one advantage. From a hardware aspect, only an A/D converter is required whereas in the parallel configuration both a A/D and D/A converter are required.

The idea behind the serial configuration layout was obtained from theory proposed by Capecchiacci and Molinari [1975]. They put forward the hypothesis that the noise generated by a codec can be summed on a power basis, viz:

$$\frac{N}{S} = \frac{N_T + N_C + N_D}{S} \qquad (3.1)$$

where N_T = theoretical or reference noise power due to an ideal device

N_C = noise power due to encoding decision level errors

N_D = noise power due to decoding reconstruction level errors

N = total noise power

The half channel contributions to the total noise power are given by

N_{TC} = noise power with a imperfect encoder and a theoretical decoder

N_{TD} = noise power with a imperfect decoder and a theoretical encoder

Adding N_T/S to both sides of the above equation we obtain

$$\frac{N + N_T}{S} = \frac{N_T + N_C + N_D + N_T}{S} \qquad (3.2)$$

Now

$$N_{TC} = N_T + N_C \qquad (3.3)$$

and

$$N_{TD} = N_T + N_D \qquad (3.4)$$

which is consistent with the definition of N_T as the reference value and N_C and N_D as deviations from the reference value.

Thus

$$\frac{N + N_T}{S} = \frac{N_{TC} + N_{TD}}{S} \qquad (3.5)$$

Thus in terms of the half channel values, the full channel value is

$$\frac{N_{FC}}{S} = \frac{N_{TC}}{S} + \frac{N_{TD}}{S} - \frac{N_T}{S} \qquad (3.6)$$

When the encoder and decoder are ideal

$$N_{TC} = N_T$$

$$N_{TD} = N_T$$

and equation (3.6) reduces to

$$\frac{N_{FC}}{S} = \frac{N_T}{S} \qquad (3.7)$$

Equation (3.6) is derived on the important assumption that the errors associated with the encoding decision levels are independent of the errors associated with the decoding reconstruction levels. In order to verify this the test layout shown in figure 52 was simulated on a computer using the TESTS simulation package. The encoder and decoder were each simulated to have a 0.90 step generator gain error.

The following terms are defined as signal to noise ratios:

Q_T = theoretical quantization distortion

Q_{TC} = quantization distortion for a imperfect encoder and theoretical decoder

Q_{TD} = quantization distortion for a imperfect decoder and theoretical encoder

Q_{FC} = quantization distortion for full channel test i.e. a imperfect encoder and a imperfect decoder

The computer simulation results were used in order to try and verify the assumption on which equation (3.6) is based. This is shown below:

$$Q_T = 42.13 \text{ dB} = 10 \log [S/N_T]$$

i.e. $N_T/S = 6.12 \times 10^{-5}$

$$Q_{TC} = 37.63 \text{ dB} = 10 \log [S/N_{TC}]$$

i.e. $N_{TC}/S = 1.73 \times 10^{-4}$

$$Q_{TD} = 37.95 \text{ dB} = 10 \log [S/N_{TD}]$$

i.e. $N_{TD}/S = 1.60 \times 10^{-4}$

Now from the simulation results we obtain a full channel value for quantization distortion to be

$$Q_{FC} = 34.41 \text{ dB}$$

Using the equation for the full channel value, derived above, and the theoretical and half channel values obtained

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$$Q_{FC} = 34.41 \text{ dB}$$

Using the equation for the full channel value, derived above, and the theoretical and half channel values obtained

from the simulation we get

$$N_{FC}/S = 1.73\text{x}10^{-4} + 1.60\text{x}10^{-4} - 6.12\text{x}10^{-5} = 2.72\text{x}10^{-4}$$

Therefore $$Q_{FC} = 10 \log [S/N_{FC}] = 35.66 \text{ dB}$$

The discrepancy between the simulated full channel value and the calculated full channel value is caused by the fact that the encoder and decoder imperfections are dependent. As is seen from figure 52, the decoder output signal is used to excite the encoder. However, the decoder output has been corrupted and contains distortion components caused by the reconstruction level errors. Thus the signal used to excite the encoder is not distortion free and hence an erroneous result is obtained for the full channel quantization distortion value.

It is possible to solve this problem by subtracting the distortion components, introduced by the decoder, in the software processing, shown as the FFT processor in figure 52. However, it is felt that this technique introduces a burden on the software overhead. As a result a serial configuration layout was not acceptable. Instead the parallel configuration, as shown in figure 51, was chosen for the proposed test system layout.

3.2 Detailed design of proposed test system

Before undertaking the detailed design of the hardware and software components present in the proposed test system, the measurement accuracy required needs to be defined.

To do this the measurement accuracy of a commercially available test system, the Hewlett Packard Primary Multiplex Analyser (PMA) was studied [Hewlett Packard, 1979]. A summary of the PMA measurement accuracies for quantization

distortion and gain tracking, using a single frequency tone, are given in tables 3 and 4 respectively.

TABLE 3 Accuracy for quantization distortion measurement using single frequency tone

S/N ratio (dB)	accuracy (dB)
< 30	± 0.4
< 40	± 0.7
< 50	± 3.5

TABLE 4 Accuracy for gain tracking measurement using a single frequency tone

input level (dBm0)	accuracy (dB)
> -47	± 0.10
> -67	± 0.15
> -77	± 0.25

Waddington [1969], describes the Marconi TF2343 quantization distortion tester and gives its measurement accuracy for quantization distortion to be ± 0.5 dB at 35 dB.

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As stated in chapter 2, the measurement accuracy of a test system affect the yield of the system. In using a low accuracy the probability of calling a bad device good or a good device bad is high, especially when the measurement value obtained lies close to the CCITT mask. Looking at the gain tracking mask recommended by CCITT, for input signal levels greater than -40dBm0 we have a pass margin of + 0.5 dB. In other words, the gain tracking value measured must fall within this boundary for the device to be classified as good. For the PMA test system the accuracy that the measured value can have over this range is + 0.1 dB, i.e. 20 per cent. It is felt that an accuracy of this nature would effect the yield of the test system considerably. For quantization distortion the accuracies given by Hewlett Packard (+ 0.4 dB) and Waddington (+ 0.5 dB) are acceptable.

Hence in the present work an accuracy of + 0.01 dB has been adopted for the gain tracking measurement, preferably over the entire input level range [-55 dBm0 to + 3 dBm0] but particularly over the range -40 dBm0 to +3 dBm0 where the pass margin is + 0.5 dB. For quantization distortion an accuracy of + 0.5 dB has been adopted over the entire range [-45 dBm0 to 0 dBm0].

3.2.1 Encoder test section

The encoder test section, showing both software and hardware components, is shown in figure 53. The reference voltage (3.14V) needed for the encoder under test and power supply requirements for the D/A converter and encoder are not shown for simplicity. In the transmit software the sinusoidal generator, generates a sine wave signal at various amplitudes determined by the control software. This is sampled at a sampling frequency of 8000 hertz i.e. every 125 microseconds. Altogether 256 samples are taken for each amplitude level and stored in memory. Each sample is then

read out of memory, under program control, and passed through a software implemented A/D converter which produces a digital 12 bit number which is sent via the data bus to a hardware D/A converter. The analogue voltage developed at the output of the D/A converter, for each sample value, is applied to the input of the encoder under test. The digital output of the encoder is read into the receive software memory via the system data bus. The samples are then passed through an ideal decoder implemented in software. This produces the half channel configuration required for the encoder test as defined previously.

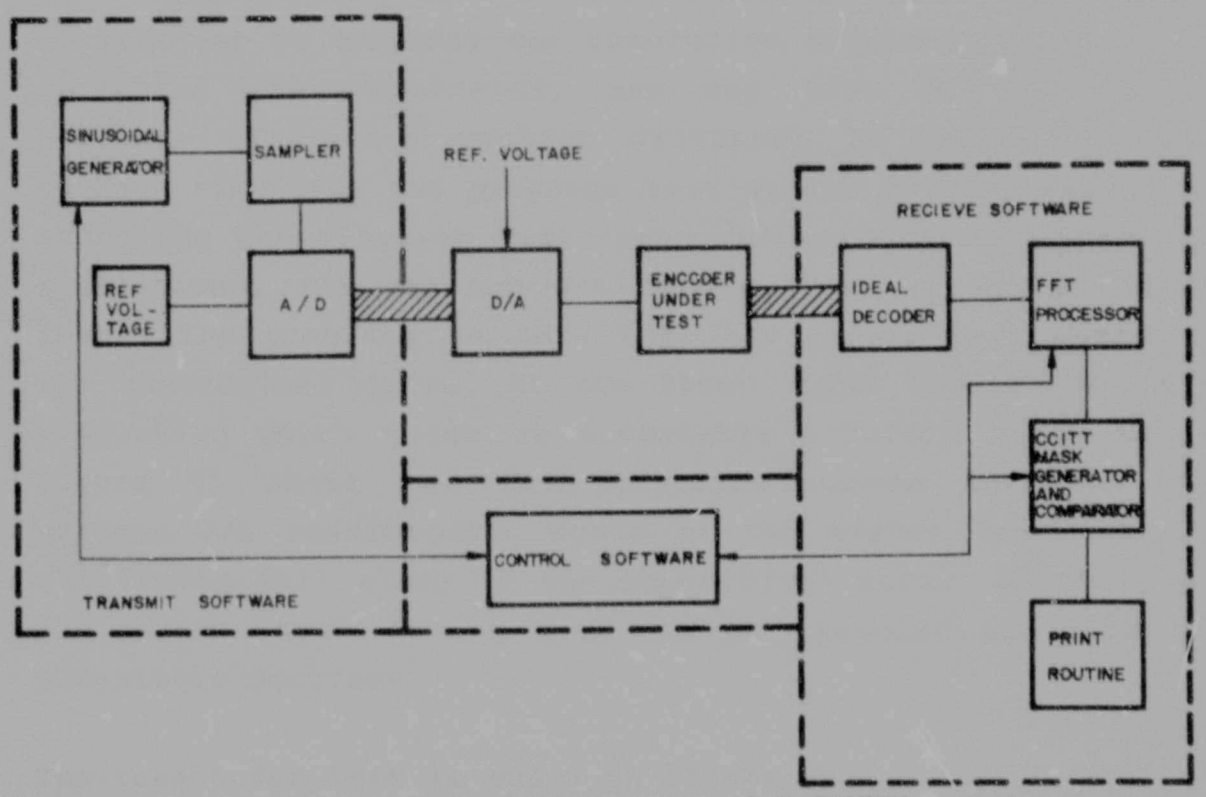


FIGURE 53 ENCODER TEST SECTION OF PROPOSED TEST SYSTEM

For each individual input signal level, the 256 samples are passed on to the FFT processing software. Here the distortion components present in the signal are identified, the input signal component is filtered out and the signal to

quantization distortion and gain tracking values are calculated. These values are compared with the quantization distortion and gain tracking masks, recommended by CCITT, generated internally by the software. The masks are generated together with appropriate guardbanding as discussed in chapter 2. Should the values obtained fall within the guardbands, the control software changes the input resolution to a much finer resolution and the test process is repeated. The operation of the control software is discussed in chapter 4. The print routine prints the results out (fail or pass) on an I/O device.

The requirements for the D/A converter are significant. Firstly let us consider the resolution required. In order to determine the resolution, use was made of the TSTRAT software simulation package discussed in chapter 4. The package simulates the proposed test system layout. Figure 54 shows the quantization distortion values obtained, from the simulations, for various D/A resolutions. At higher input levels the accuracy is such that the values fall close to the theoretical curve. At the lower input levels the only resolution which gives an acceptable accuracy is 16 bits. Figure 55 shows the gain tracking curves obtained for various D/A resolutions. Again at the higher input levels the curves fall close to the theoretical curve. However, at the lower input levels none of the resolutions give an acceptable accuracy.

The reason for this is shown in figure 56.

Here is shown a section of the piece-wise characteristic curve for a D/A converter and an encoder. At the higher input levels, a rough resolution on the D/A decision levels is sufficient to stimulate the individual decision levels of the encoder. However at lower input levels the resolution of the D/A converter is not adequate to allow each individual

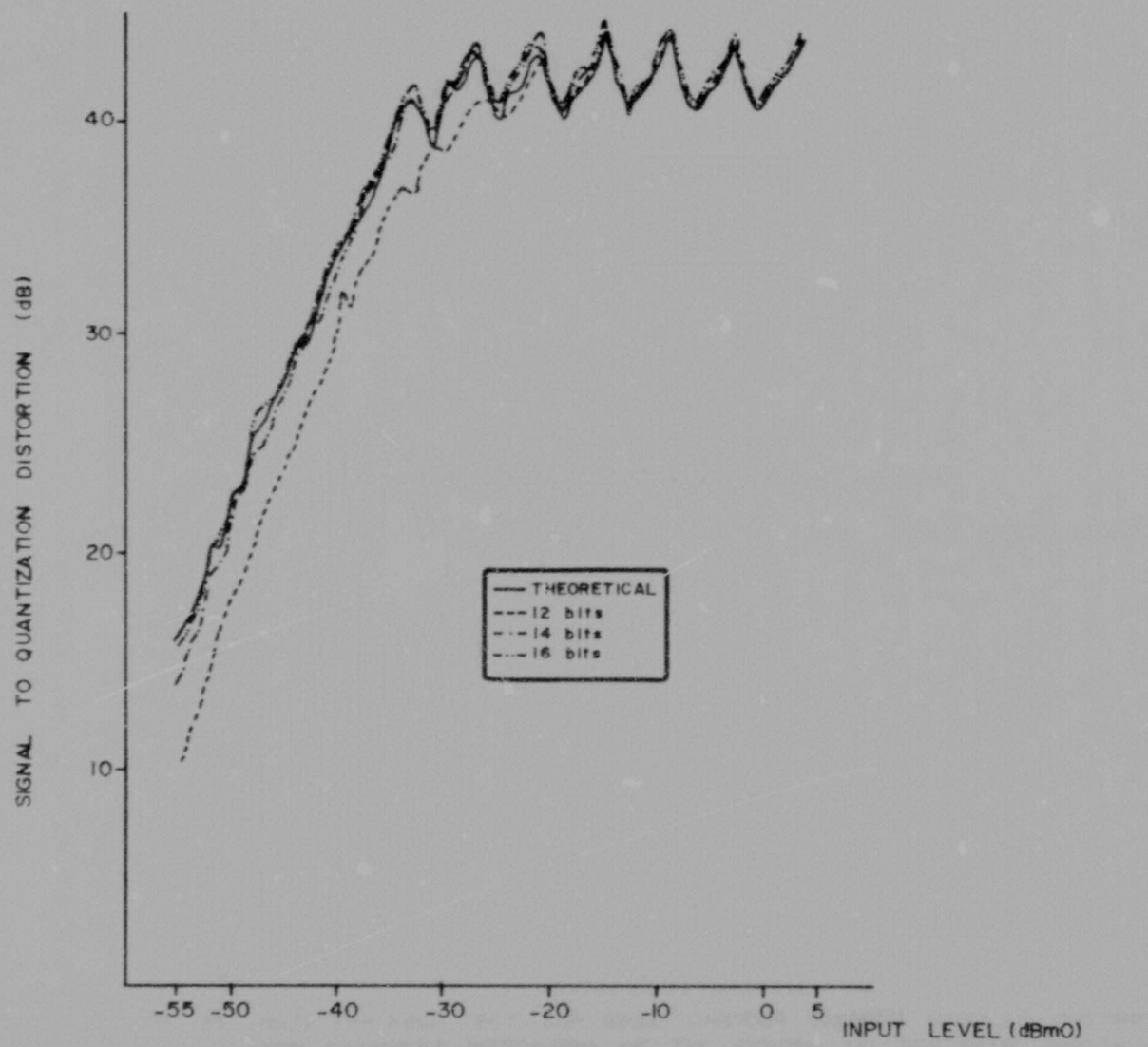
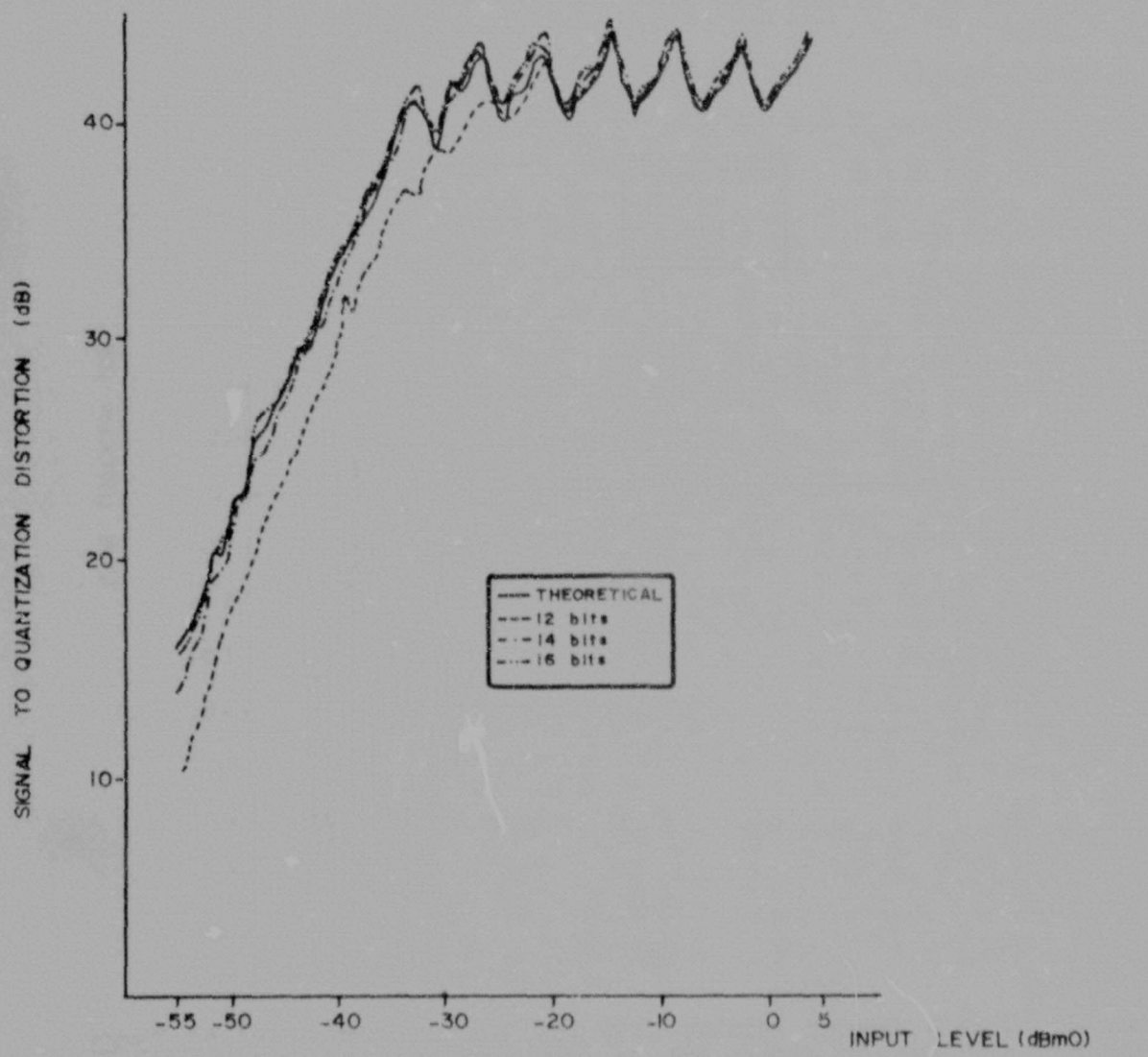


FIGURE 54 QUANTIZATION DISTORTION TEST FOR IDEAL ENCODER SHOWING RESULTS OBTAINED FOR DIFFERENT RESOLUTION OF THE DIGITAL TO ANALOGUE CONVERTER.



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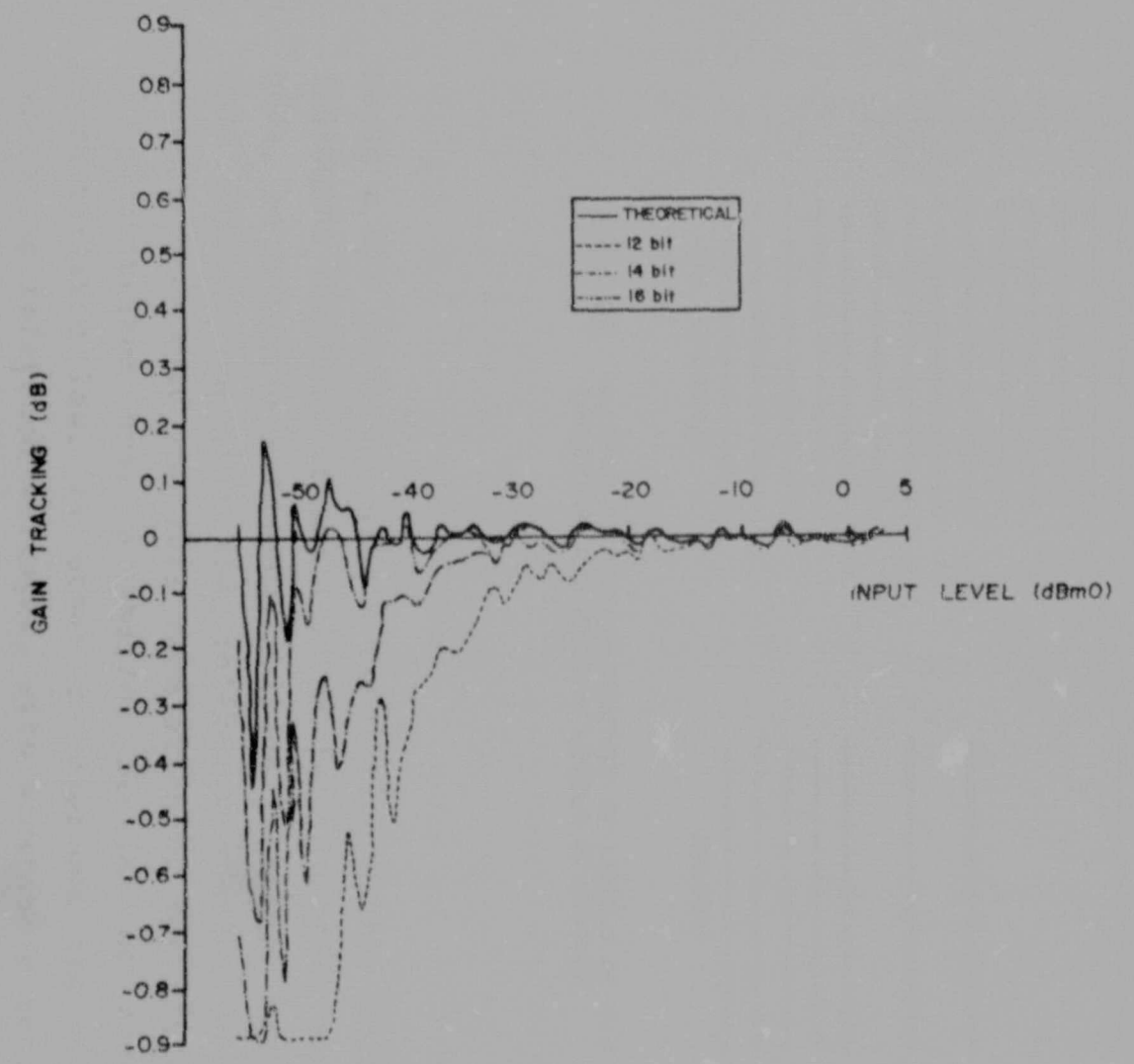

FIGURE 55 GAIN TRACKING TEST FOR IDEAL ENCODER SHOWING RESULTS OBTAINED FOR DIFFERENT RESOLUTION OF THE DIGITAL TO ANALOGUE CONVERTER.

decision level of the encoder to be excited.

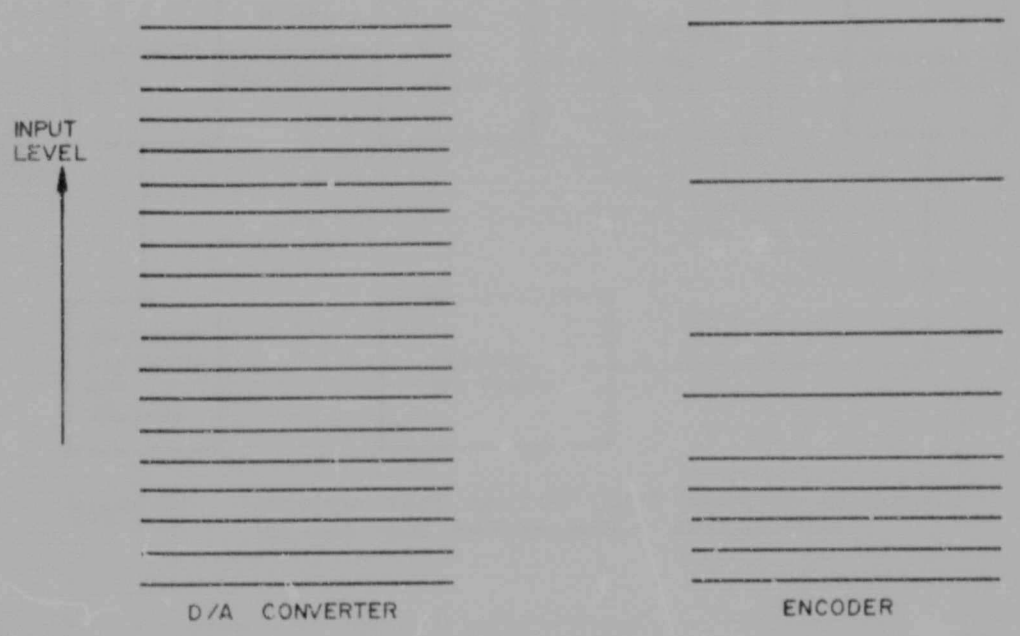

FIGURE 56 DIAGRAM SHOWING RESOLUTION OF LEVELS IN D/A CONVERTER AND DECISION LEVELS IN ENCODER.

Using a D/A converter with a resolution better than 16 bits increases the cost of the test system. In order to overcome this, an adaptive reference voltage technique was adopted. This entails changing the reference voltage of the D/A converter so that the full resolution of the D/A converter is concentrated over a smaller section of the encoder characteristic law. In order to overcome the problem of generating reference voltages, with acceptable accuracy, in the range of a few millivolts, the system shown in figure 57 was proposed.

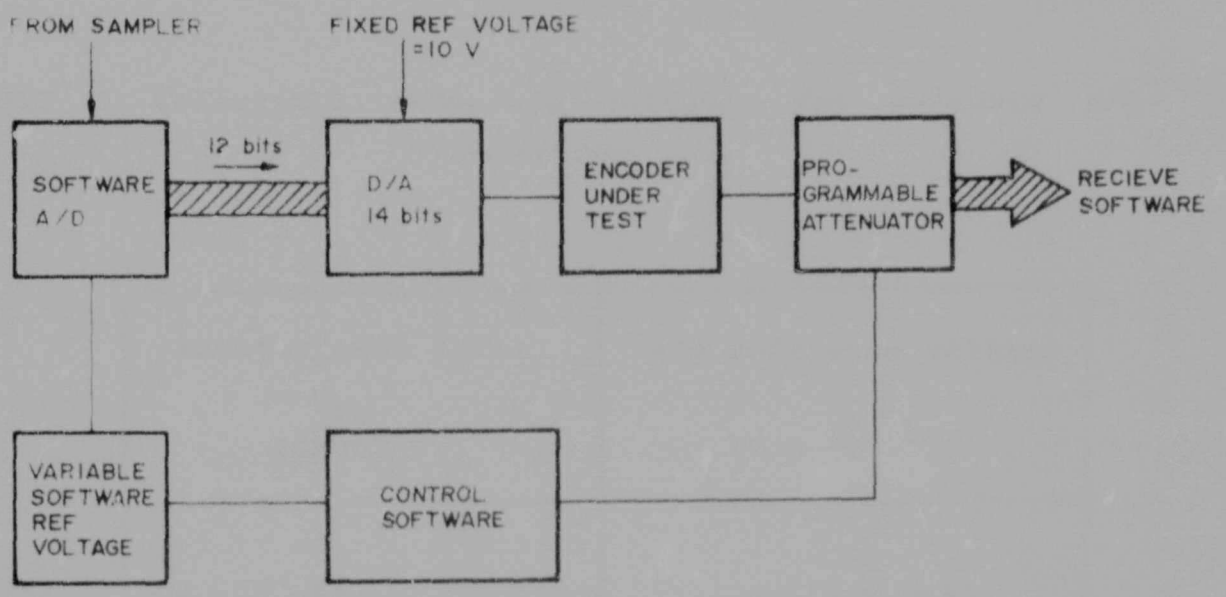

FIGURE 57 ENCODER TEST SECTION USING ADAPTIVE REFERENCE VOLTAGE AND PROGRAMMABLE ATTENUATOR

The reference voltage used for the hardware D/A converter is fixed and a value of 10 volts was chosen. The reference voltage used for the software A/D converter is derived from a base reference voltage of 4 volts and is dependent upon the input signal level range as shown in table 5.

A resolution of 12 bits was chosen for the software A/D converter. A resolution of 14 bits was chosen for the D/A converter in order to compensate for the least significant bit (LSB) error inherent in practical D/A's.

TABLE 5 Selectable reference voltages for software A/D converter

input signal level V_{IN} (dBmO)	A/D reference voltage (mV)
$V_{IN} \leqslant -49$	4/512 = 7.81
$-49 < V_{IN} \leqslant -43$	4/256 = 15.63
$-43 < V_{IN} \leqslant -37$	4/128 = 31.25
$-37 < V_{IN} \leqslant -31$	4/64 = 62.50
$-31 < V_{IN} \leqslant -25$	4/32 = 125
$-25 < V_{IN} \leqslant -19$	4/16 = 250
$-19 < V_{IN} \leqslant -13$	4/8 = 500
$-13 < V_{IN} \leqslant -7$	4/4 = 1V
$-7 < V_{IN} \leqslant -1$	4/2 = 2V
$V_{IN} > -1$	4V

A programmable attenuator is used in order to correct the analogue output voltage from the D/A converter. The attenuator is controlled by the system control software. The programmable attenuator does away with the need for separate reference voltage sources for the D/A converter.

Figures 58 and 59 show the quantization distortion and gain tracking curves obtained for an ideal encoder test using a 12 bit D/A converter and the adaptive reference voltage technique described above. An ideal 12 bit D/A converter was simulated and hence the effect of LSB error was not considered. The accuracies obtained lie well within the

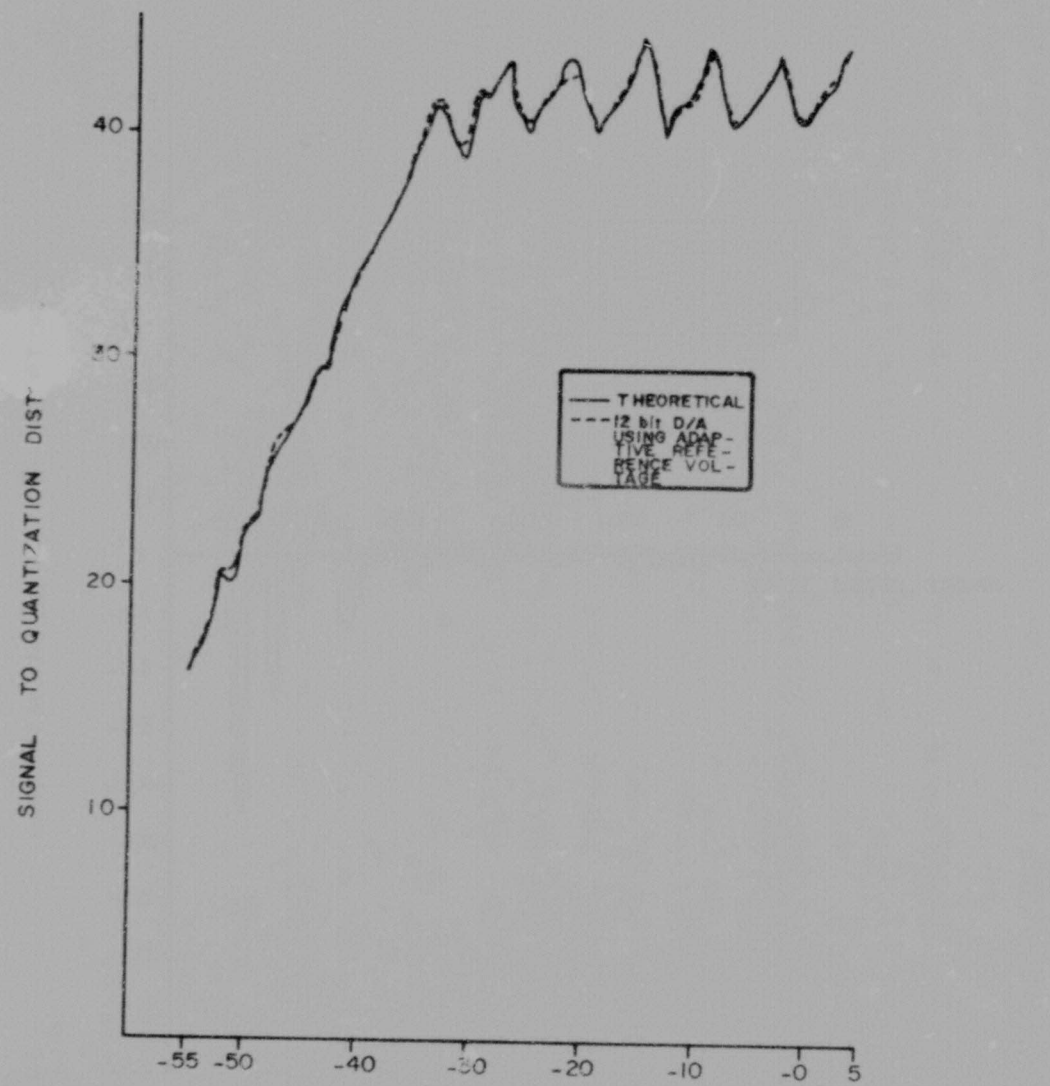

FIGURE 58 QUANTIZATION DISTORTION TEST FOR IDEAL ENCODER USING A 12 BIT DIGITAL TO ANALOGUE CONVERTER AND A ADAPTIVE REFERENCE VOLTAGE TECHNIQUE.

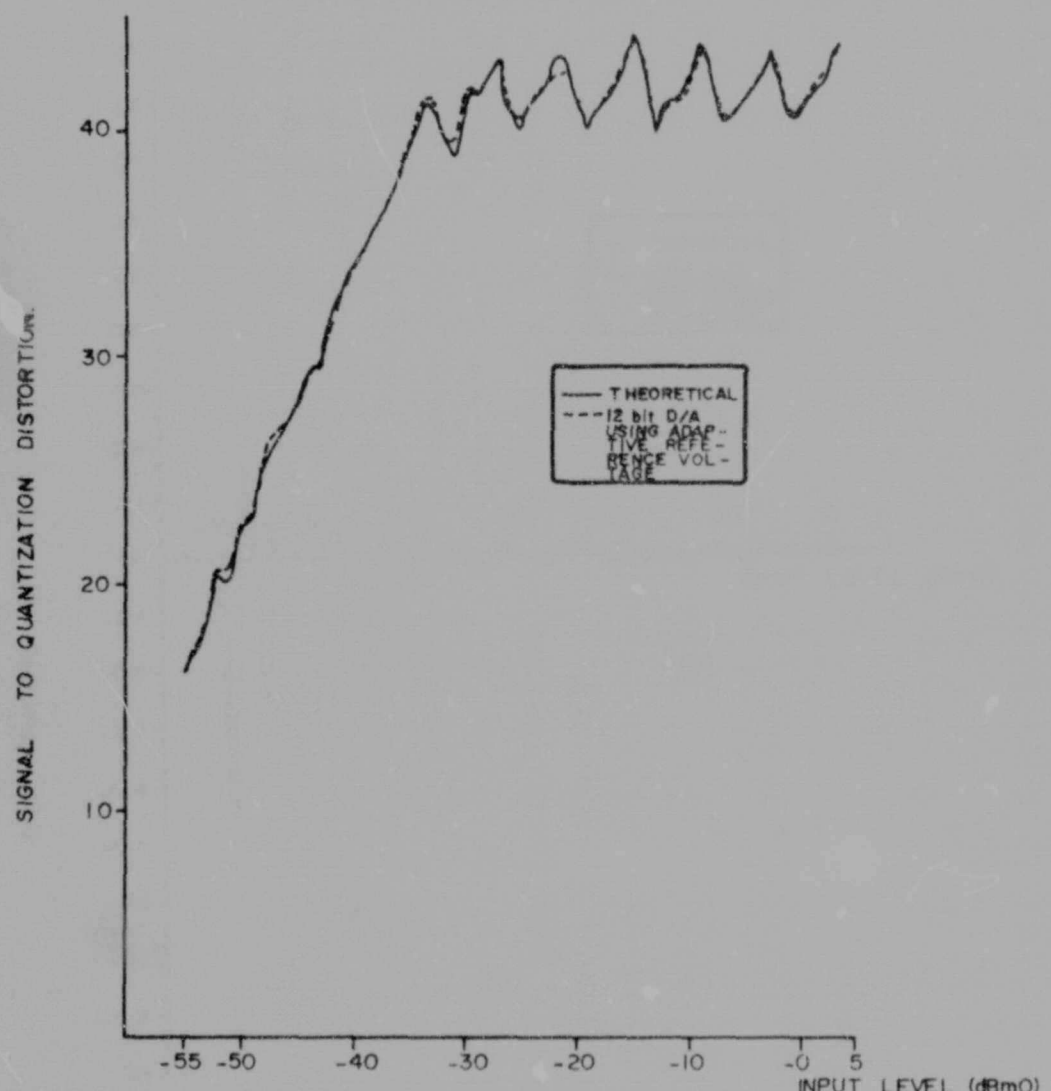

FIGURE 58 QUANTIZATION DISTORTION TEST FOR IDEAL ENCODER USING A 12 BIT DIGITAL TO ANALOGUE CONVERTER AND A ADAPTIVE REFERENCE VOLTAGE TECHNIQUE.

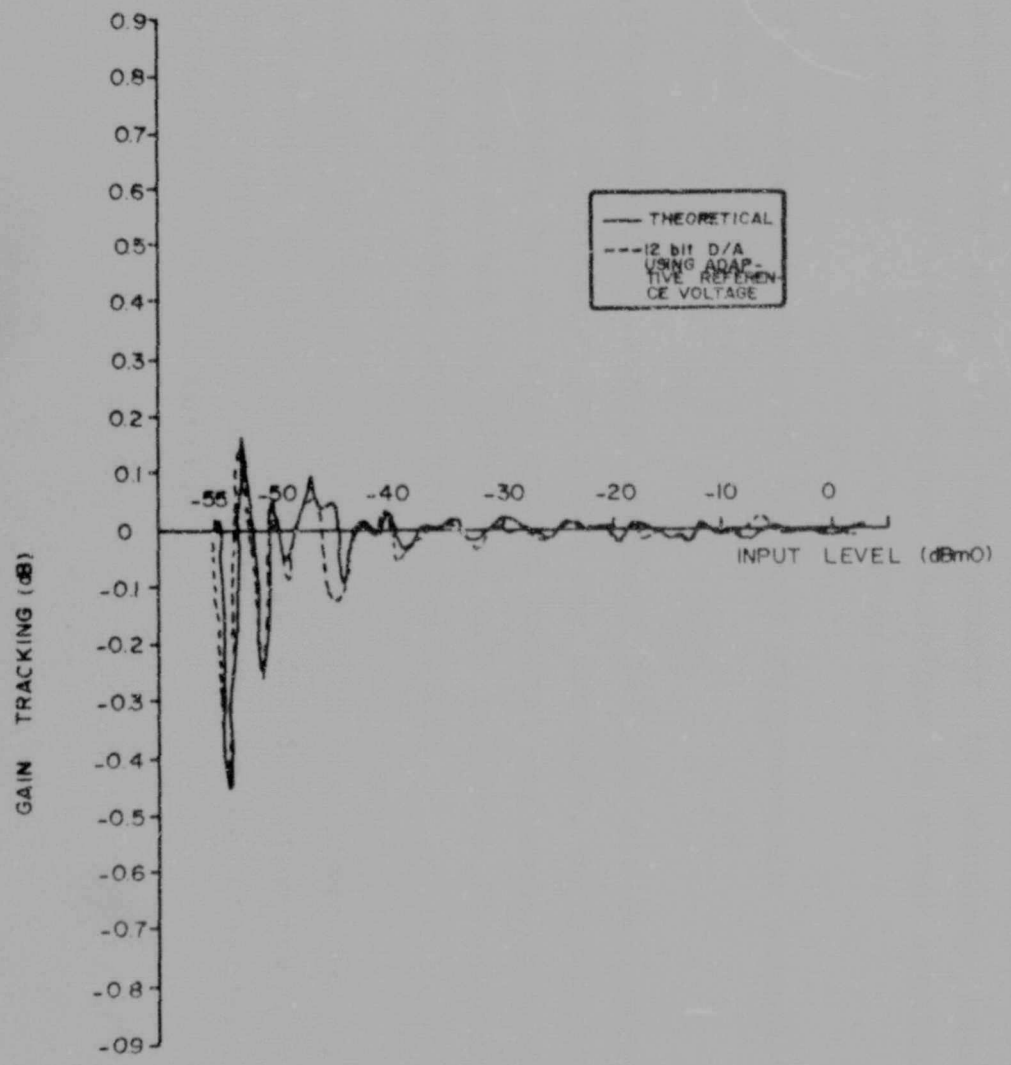

FIGURE 59 GAIN TRACKING TEST FOR IDEAL ENCODER USING A 12 bit DIGITAL TO ANALOGUE CONVERTER AND A ADAPTIVE REFERENCE VOLTAGE TECHNIQUE.

specification called for earlier, viz. ± 0.5 dB for quantization distortion and ± 0.01 dB for gain tracking.

In addition an encoder with a 1 per cent level shift error was simulated. Tests were carried out using a 16 bit D/A converter and a 12 bit D/A converter with the adaptive reference voltage technique. The theoretical results were obtained using the TESTS simulation package.

Figures 60 and 61 show the quantization distortion and gain curves obtained. The improvement in accuracy using the adaptive reference voltage technique is shown significantly in the case of the gain tracking test.

The suggested circuit for the programmable attenuator is shown in figure 62.

The attenuator uses a standard voltage divider circuit. A series of analogue switches are provided, controllable, via a decoder, by the test system control software. A particular analogue switch is addressed and switched in depending on the input signal level range selected.

One problem that is envisaged with the above programmable attenuator is that the voltage divider presents a varying output impedance. This would need to be considered when actual hardware is built.

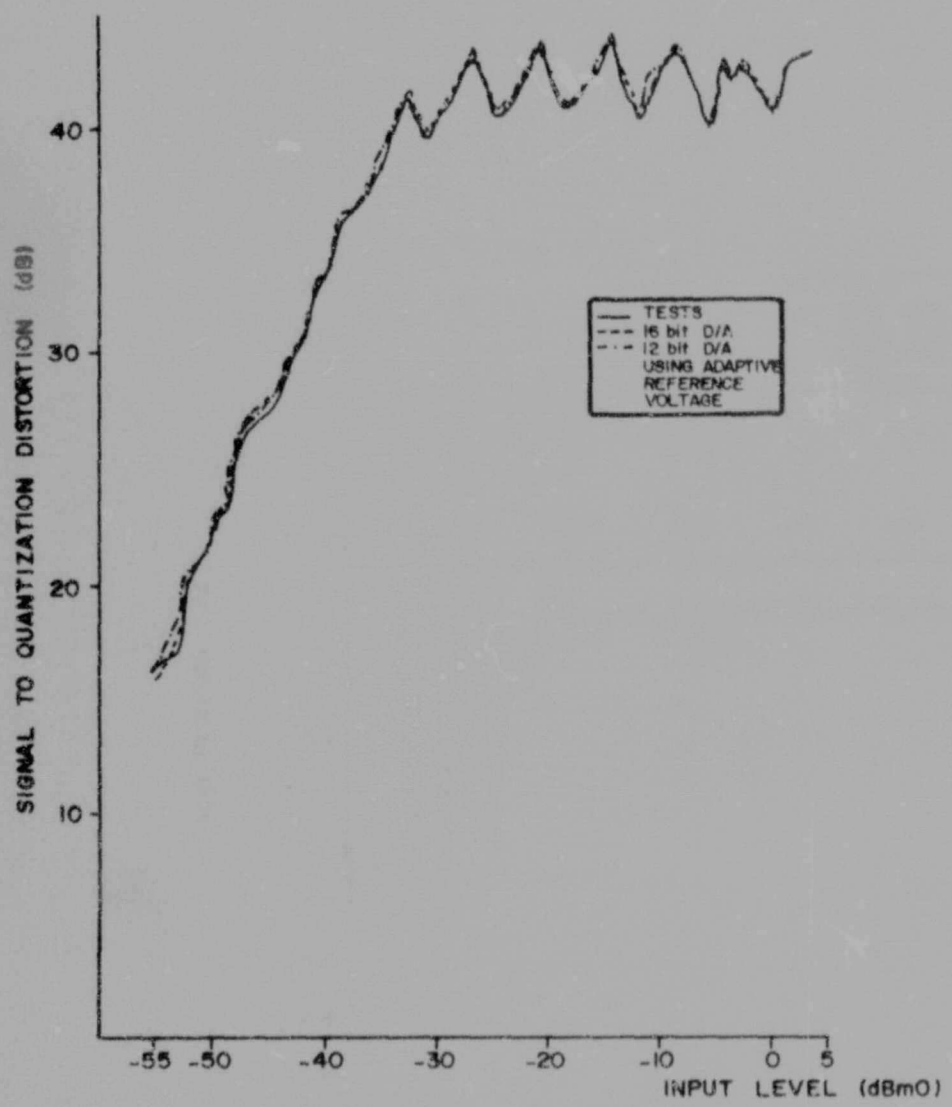

FIGURE 60 QUANTIZATION DISTORTION TEST FOR AN ENCODER HAVING A ONE PERCENT LEVEL SHIFT ERROR

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