UNIVERSITY OF THE WITWATERSRAND

Development of TileCoM firmware and software for the off-detector electronics of the ATLAS Tile Calorimeter at the HL-LHC

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Declaration of Authorship

I, Mpho Gift Doctor GOLOLO, declare that this thesis titled, "Development of TileCoM firmware and software for the off-detector electronics of the ATLAS Tile Calorimeter at the HL-LHC" and the work presented in it are my own. I confirm that:

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- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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Date: 08 / 08 / 2023

"For I know the plans I have for you," declares the LORD, "plans to prosper you and not to harm you, plans to give you hope and a future."

Jeremiah 29:11

Abstract

In 2010 the LHC started to operate as the energy frontier particle accelerator in the world, situated close to Geneva and 100 m below the French and Swiss border in a circular tunnel of 27 km. The HL-LHC which is an upgrade of the LHC is envisioned to maximize the instantaneous luminosity of $\mathcal{L} = 1 \times 10^{34}$ cm^{-2}s^{-1} by a factor of 5 to fully exploit the physics potential at the energy frontier.

During 10 years of operation, an improved TDAQ system architecture will have the capability to accommodate the trigger rates and the amount of data generated from the HL-LHC. TileCal is the ATLAS central hadronic calorimeter, a sampling calorimeter with iron as passive medium and plastic scintillator tiles as active medium. The ATLAS TileCal Phase-II upgrades will prepare the ATLAS experiment for the HL-LHC and includes new requirements in terms of radiation levels, an increase in data bandwidth, and clock distribution. To meet the requirements of the HL-LHC, a completely new readout electronics is designed to support the data acquisition system of TileCal.

As part of the new readout electronics, this thesis is focused on the design of the TileCoM and Tile GbE Switch. The Tile GbE Switch PCB is manufactured by two South African companies, Trax Interconnect and Jemstech. The PCBs are fully functional and have been integrated with new readout electronics. Three main functionalities are implemented on the TileCoM in software and firmware implementation as key elements of the TDAQ and DCS of the ATLAS TileCal at the HL-LHC. The TileCoM and Tile GbE Switch are successfully integrated with the ATLAS Phase-II TileCal upgrade electronics. This is achieved by successful remote control and monitoring of the ATLAS TileCal Phase-II upgrade electronics. This thesis shows monitoring results based on voltage, current and other parameters.

Acknowledgements

Many people contributed to the success of this thesis, as well as the financial sponsors, and I would like to thank them all. I would like to thank the South African Department of Science and Innovation and the National Research Foundation for their continued support through the SA-CERN program and other forms of support.

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I would like to extend my gratitude to my co-supervisor, Dr. Fernando Carrió Argos from the Instituto de Física Corpuscular, University of Valencia. Thank you very much for always being accessible and willing to help during work hours, evenings, weekends, and holidays. You were even available and offered to help during COVID times. The guidance and suggestions you provided during all these years at CERN have greatly impacted my career. I have never had a technical supervisor like you in my career.

I would like to thank the School of Physics at the Institute for Collider Particle Physics, University of the Witwatersrand. The great hardware team that offered inspiration and support. You are an incredible team that makes this group feel like family. To my colleagues in the hardware team, Edward Nkadimeng, Thabo Lepota, and others, your inputs in my work helped in the submission of conference proceedings and journal. The technical knowledge and guidance shared during my PhD journey played an important role in the submission of this thesis.

I would like to thank the TileCal collaboration at CERN for allowing me to be

part of the amazing team with the ATLAS experiment. To the colleagues I met at CERN, Eduardo Valdés Santurio, Filipe Martins, Alberto Valero and others, thank you very much for the support and advice. The advice I have received from Eduardo Valdés Santurio in terms of remote programming and TilePPr-DCS interface from Filipe Martins really helped me to publish my conference proceeding would not have survived the TileCal maintenance period if it was not Irakli Minashvili. He provided clear and knowledgeable maintenance procedures that we followed during maintenance. I am so grateful to be part of the TileCal team and I hope to continue to be part of this team. I learn a lot from this team.

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List of Abbreviations

ACBB	ATCA Carrier Blade Board.
ADC	Analog-to-Digital Converter.
ALICE	A Large Ion Collider Experiment.
ALTI	ATLAS Local Trigger Interface.
AMC	Advanced Mezzanine Card.
APU	Application Processing Unit.
ASIC	Application-Specific Integrated Circuit.
ATCA	Advanced Telecommunications Computing Architecture.
ATCN	ATLAS Technical and Control Network.
ATLAS	A Toroidal LHC AparatuS.
AXI	Advanced eXtensible Interface.
BIOS	Basic Input/Output System.
BSP	Board Support package.
CERN	European Organization for Nuclear Research.
CLB	Configurable Logic Block.
CLI	Command-Line Interface.
CMS	Compact Muon Solenoid.
CPM	Compact Processing Modules.
CPU	Central Processing Unit.
CTP	Central Trigger Processor.
DAC	Digital-to-Analog Converter.
DAQ	Data AcQuisition.
DB	DaughterBoard.
DCS	Detector Control System.
DDR	Double Data Rate.

DHCP	Dynamic Host Configuration Protocol.
DSP	Digital Signal Processor.
DSS	Detector Safety System.
EEPROM	Electrically Erasable Programmable Read-Only Memory.
EF	Event Filter.
ELMB	Embedded Local Monitoring Boards.
EMI	Electromagnetic Interference.
FEB	Front-End Board.
FELIX	Front-End LInk eXchange.
FET	Field Effect Transistor.
FF	Flip-Flop.
FPGA	Field Programmable Gate Array.
GPU	Graphic Processing Unit.
GBT	GigaBit Transceiver.
GCC	GNU Compiler Collection.
GCS	Global Control Station.
GPIO	General Purpose Input Output.
HAL	Hardware Access Library.
HDL	Hardware Description Language.
HTT	Hardware-based Tracking for the Trigger.
HL-LHC	High Luminosity LHC.
HLT	High-Level Trigger.
HV	High Voltage.
HVPS	High Voltage Power Supply.
ID	Inner Detector.
IPMB	Intelligent Platform Management Bus.
IPMC	Intelligent Platform Management Controller.
IPMI	Intelligent Platform Management Interface.
JTAG	Joint Test Action Group.
IIO	Linux Industrial Input Output.
LHC	Large Hadron Collider.

LHCb	Large Hadron Collider beauty.
LHCf	LHC forward.
LCS	Local Control Station.
LUT	Look-Up Tables.
LS1	First Long Shutdown.
LS2	Second Long Shutdown.
LTP	Local Trigger Processor.
LTPI	Local Trigger Processor Interface.
LVDS	Low Voltage Differential Signalling.
LVPS	Low Voltage Power Supply.
MoEDAL	Monopole and Exotics Detector at the LHC.
MB	MainBoard.
MPSoC	MultiProcessor System-on-Chip.
MS	Muon Spectrometer.
OLE	Object Linking and Embedding.
OS	Operating Systems.
OPC UA	Open Platform Communications Unified Architecture.
PS	Proton Synchrotron.
PS	Processing System.
PL	Programmable Logic.
PMT	PhotoMulTiplier.
POL	Point-of-Load.
QSFP	Quad Small Form-factor Pluggable.
RAM	Random Access Memory.
RGMII	Reduced Gigabit Media-Independent Interface.
RPU	Real-Time Processing Unit.
ROD	Read Out Driver.
RoI	Regions of Interest.
RTM	Rear Transition Module.
SCADA	Supervisory Control and Data Acquisition.
SCS	Subdetector Control Station.

SD	Super-Drawers.
SDK	Software Development Kit.
SPS	Super Proton Synchrotron.
SoC	System-on-Chip.
SODIMM	Small Outline Dual Inline Memory Module.
SPI	Serial Peripheral Interface.
TBM	Trigger and Busy Module.
TCK	Test Clock.
TDI	Test Data In.
TDO	Test Data Out.
TCP/IP	Transmission Control Protocol and the Internet Protocol.
TileDMU	Tile De-randomizer.
TileCal	Tile Calorimeter.
TileCoM	Tile Computer-On-Module.
TOTEM	TOTal Elastic and diffractive cross-section Measurement.
TDAQ	Trigger and Data AcQuisition.
TDAQi	Trigger and Data AcQuisition interface.
TDR	Technical Design Report.
TileGbE	Tile Gigabit Ethernet.
TilePPr	Tile PreProcessor.
TMS	Test Mode Select.
TRT	Transition Radiation Tracker.
TTC	Trigger, Timing, and Control.
TTCrx	Trigger, Timing, and Control receiver.
TTCex	Trigger, Timing, and Control emitter.
UART	Universal Asynchronous Receiver/Transmitter.
PCB	Printed Circuit Board.
VME	Versa Module Eurocard.
XML	Extensible Markup Language.
XSCT	Xilinx Software Command-Line Tool.
XVC	Xilinx Virtual Cable.

Dedication

To my late dad, Lesetja Andries Bambo, losing you on 29 December 2021 was a devasting experience I have ever had to go through. Having to go through your funeral on the 3rd of January 2022 was an unbelievable experience. To my late son, Leano Gololo, you will forever have a special place in my heart. It was heartbreaking to lose you on 30 September 2022. To my late granny, who raised me until 18, I still cannot believe we lost you in October 2022. May your souls rest in peace. ***This Ph.D. is dedicated to all of you! Thank you!!!****...*

Publications

1. Gololo M.G.D, on behalf of ATLAS collaboration, Performance for the ATLAS Tile Calorimeter, Journal of Instrumentation: Conference Series, Volume 15, The International Conference Instrumentation for Colliding Beam Physics (INSTR2020) held at Novosibirsk, Russia from 24 to 28 February 2020. https://iopscience.iop.org/article/10.1088/1748-0221/15/08/C08020/meta

2. Gololo M.G.D, Carrio Argos. F, Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter, Journal of Physics: Conference Series, Volume 1690, 5th International Conference on Particle Physics and Astrophysics will be held at MEPhI 5-9 October 2020, Moscow, Russian Federation. https://iopscience.iop.org/article/10.1088/1742-6596/1690/1/012054/meta

3. Gololo M.G.D, Carrio Argos. F and, Mellado B, The development of a real-time Monitoring system for the ATLAS Tile Calorimeter Phase-II Upgrades, pp. 491 - 496. ISBN: 978-0-620-97693-0. https://events.saip.org.za/event/206/page/446-the-proceedings-of-saip2021

4. Gololo M.G.D, Carrio Argos. F and, Mellado B, South African contribution towards the ATLAS Tile Calorimeter PreProcessor, pp. 91 - 95. ISBN: 978-0-620-97693-0. https://events.saip.org.za/event/206/page/446-the-proceedings-of-saip2021

5. Gololo M.G.D, Carrio Argos. F and, Mellado B, Tile Computer-on-Module for the ATLAS Tile Calorimeter Phase-II upgrades, Journal of Instrumentation, publisher: IOP Publishing, Volume 17, Pages P06020, June 2022. https://iopscience.iop.org/article/10.1088/1748-0221/17/06/P06020

Chapter 1

Introduction

The ATLAS Tile Calorimeter (TileCal) readout Phase-II Upgrades electronics are the focus of this thesis, specifically, the design of Tile Computer-On-Module (TileCoM) and Tile Gigabit Ethernet (TileGbE) Switch developments as part of the readout electronics. Three main functionalities are implemented on the TileCoM in software and firmware as key elements of the Trigger and Data AcQuisition (TDAQ) and Detector Control System (DCS) of the ATLAS TileCal at the High Luminosity-Large Hardron Collider (HL-LHC). These functionalities are part of the requirements for the ATLAS Phase-II Upgrades. Six chapters are presented in this document, and they are all summarized below.

Chapter 2 presents an introduction to the TileCal LHC, the data acquisition system of the LHC. The ATLAS experiment and TileCal are introduced in this chapter. A brief introduction of the readout electronics and the ATLAS TDAQ architecture is provided. Chapter 3 introduces the HL-LHC and the ATLAS Phase-II Upgrade electronics readout. A description of each and every module of the on- and off-detector electronics for the ATLAS TileCal Phase-II upgrades is provided.

Chapter 4 presents the design of the TileCoM and the TileGbE modules for Tile PreProcessor (TilePPr). A detailed design in terms of the components used in each module as well as their placement in the readout chain are presented. The TileGbE Switch Printed Circuit Board (PCB) is manufactured by two South African companies, Trax Interconnect and Jemstech. The PCBs are fully functional and have been integrated with new readout electronics.

Chapter 5 explains the firmware and software design of the TileCom.. These functionalities are remote programming of the TilePPr and TDAQ system interfaces,

and the TilePPr and DCS system interface. The architectures of these designs are presented and details are given on their implementation This chapter also explains how these designs are integrated with the readout electronics. Different communication protocols are introduced and explanation is given on how they are used to remotely access the TileCoM and the readout electronics.

Chapter 6 explains the testing methodologies used to test firmware and software designs. The testbench includes a network router, one TileGbE Switch, an Avnet Ultra96 version 2 Zynq UltraScale+ MultiProcessor System-on-Chip (MPSoC) TileCoM evaluation board, and a Compact Processing Modules (CPM) emulator such as Xilinx VC707 evaluation board. All testbench modules are remotely accessed through the network router. The TileCal GbE Switch is used to connect the off-detector electronics to the network. Results for each functionality test are presented in this chapter.

Chapter 7 presents the conclusions and future plans for the TileCoM in the ATLAS Phase-II Upgrade readout electronics.

Chapter 2

The Large Hadron Collider

2.1 Introduction

The LHC [1] is known to be the world's largest particle accelerator located close to Geneva and 100 m below the french and swiss border in a circular tunnel of 27 km [2]–[3]. The concept of HL-LHC prevails as a feasible solution. The HL-LHC is designed to deliver the instantaneous luminosity of $\mathcal{L} = 1 \times 10^{34}$ cm^{-2}s^{-1} which is an increase of its potential in the frontiers of high energy physics. This luminosity is achieved by enhancing the performance of the Proton Synchroton (PS) Booster and collimators [4]. These advantages make HL-LHC a better infrastructure for continuing to carry out the primary functions of LHC and contribute to the four main experiments. These include ATLAS [5], CMS (Compact Muon Solenoid) [6], ALICE (A Large Ion Collider Experiment) [7], and LHCb (Large Hadron Collider beauty) [8].

2.1.1 LHC experiments

With the various stages that comprise the accelerator complex of the European Organization for Nuclear Research (CERN), the LHC is considered to be the last stage that the series of accelerators undergoes to increase the energy of proton beams. Figure 2.1 shows the CERN accelerator complex [9] with a number of accelerators. The source of this accelerator begins at the Linear accelerator 4 (Linac4), which generates the negative hydrogen ions to 160 MeV. At this stage, these hydrogen ions still contain additional electrons that are stripped, leaving only protons. These protons

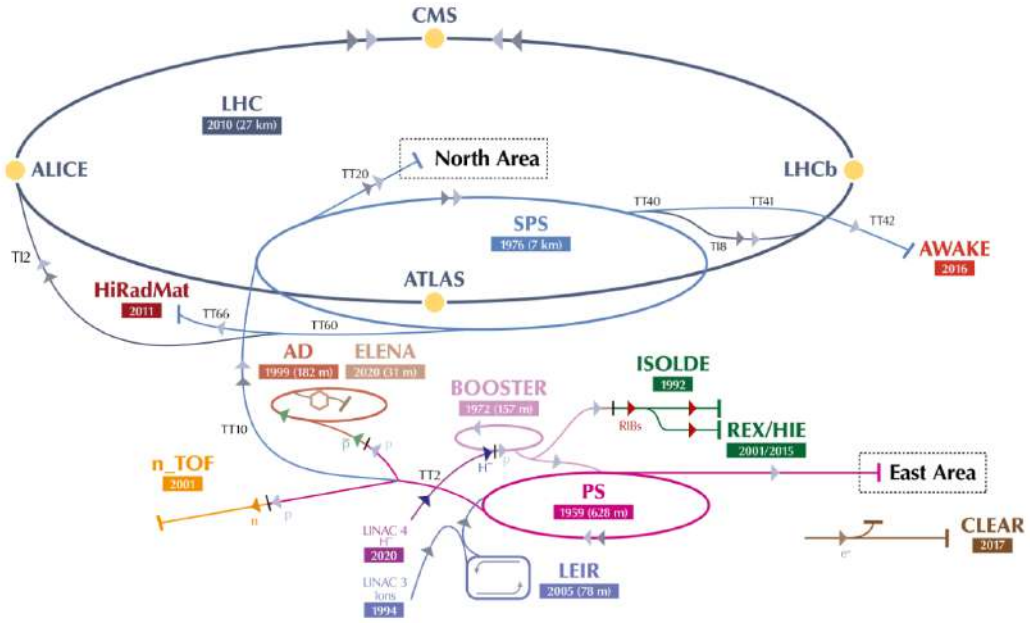


FIGURE 2.1: The CERN's accelerator complex [1].

are accelerated to 2 GeV for injection into the Proton Synchrotron (PS). The acceleration Beams are accelerated to 26 GeV for injection into the Super Proton Synchrotron (SPS). The protons are then accelerated up to 450 GeV in the SPS.

At this stage, the protons are ready to be transferred to the LHC accelerator, where one pipe of the beam circulates in one direction, while the other beam circulates in another direction. When the ring is filled, it takes 20 minutes for the protons to reach their maximum energy of 8 TeV. After many hours of beam circulation, the total energy at the collision point is equal to 13 TeV at the four collision detectors, ALICE, ATLAS, CMS, and LHCb. The maximum amount of energy of 13 TeV was achieved during Run 2. In addition to these four experiments, there are three more installed around the accelerator complex. These include TOTEM (TOTal Elastic and diffractive cross-section Measurement) [10], LHCf (LHC forward) [11], and MoEDAL (Monopole and Exotics Detector at the LHC) [12].

Fundamentally, these experiments are used to detect the particles generated during the collisions between the proton beams and the accelerator rings corresponding to the main experiments, namely ATLAS, CMS, ALICE, and LHCb. They are popularly known for their characteristic feature of being multipurpose experiments situated on opposite sides of the LHC ring. In addition, they were particularly designed and optimized to study new physics beyond the Standard Model and also measure

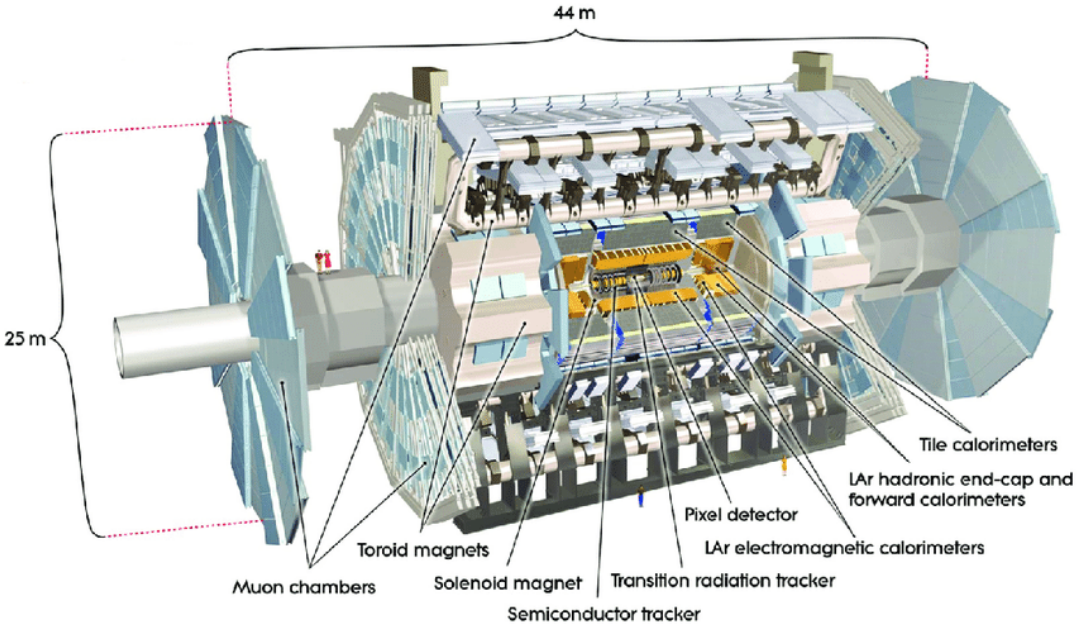


FIGURE 2.2: The ATLAS experiment [5].

the properties of the strong and electroweak forces with immense precision at the TeV scale. The ATLAS and CMS experiments announced their discovery of a Higgs boson having an estimated mass of 125 GeV [13, 14] on 4^{th} of July 2012. TOTEM is located in close proximity to the CMS detector and performs high-precision measurements of the proton size and the LHC luminosity. LHCf and MoEDAL are located near the ATLAS detector and in the walls of the LHCb cavern, respectively [12].

2.2 The ATLAS experiment at the LHC

The existence of the ATLAS experiment [5] can be traced back to 1994 when it was initially proposed as a general-purpose particle detector [15]. It was designed to study the products of p-p collisions at the LHC. The basic principle of this experiment involves the collision between two proton beams at the center of the ATLAS detector generating particles in all directions.

Compared to other experiments in the LHC, ATLAS is considered the largest, with an overall weight of approximately 7,000 tons. It is also 45 m long, with a height greater than 25 m. With the emergence of advanced technologies over the last

decade, the expected performance [16] of the ATLAS detector has rapidly improved to actual measurements on collision data [17] and cosmic rays [18].

Furthermore, to measure different particles emerging from the collisions, the ATLAS experiment utilizes three concentric subdetectors: Inner Detector (ID), electromagnetic and hadronic calorimeter systems, and Muon Spectrometer (MS). As depicted in Figure 2.2, this experiment has cylindrical symmetry. The Transition Radiation Tracker (TRT) [19] is made up of 370,000 cylindrical drift tubes or straws of 4 mm diameter. The barrel portion has about 50,000 straws, each separated at z = 0 to reduce occupancy. The ID subdetector [20], [21], [22] is situated in the inner part of the ATLAS experiment. The Pixel detector contains 80 million channels with a size of 250 x 50 μm^2 or 150 x 50 μm^2. The SCT is made out of 1 million 80 mrad long silicon microstrips. The ID is surrounded by the solenoidal magnet, where the magnetic field bends the trajectories of the charged particles. The outermost layer of the ATLAS comprises MS and a toroid magnet, where a muon tracking system measures trajectories of the muons beyond the calorimeters. These systems are used for measurements of electromagnetic and hadronic energy in the range of $|\eta| < 4.5$.

2.2.1 ATLAS readout system

Figure 2.3 shows an overview of the overall architecture of the ATLAS Trigger system for the TDAQ Phase-I upgrade. Compared to the previous architecture with three levels of event selection, only the Level-1 (L1) trigger system and High Level Trigger (HLT) are used. L1 calorimeter trigger electronics, which include on-detector electronics, are not replaced because trigger latency is a crucial variable for L1 trigger upgrades.

The event rate from the bunch crossing to the L1 trigger system is accepted at the L1 Accept. As this level is largely based on the hardware, a decision comes to the on-detector electronics. These L1 trigger system events are stored in pipeline memories that are then de-randomized and transmitted to the ReadOut Driver (ROD) [24] in off-detector electronics. They are responsible for energy and time reconstruction, generating busy data integrity checks, and lossless data compression. To readout the entire TileCal detector, 32 ROD modules are required.

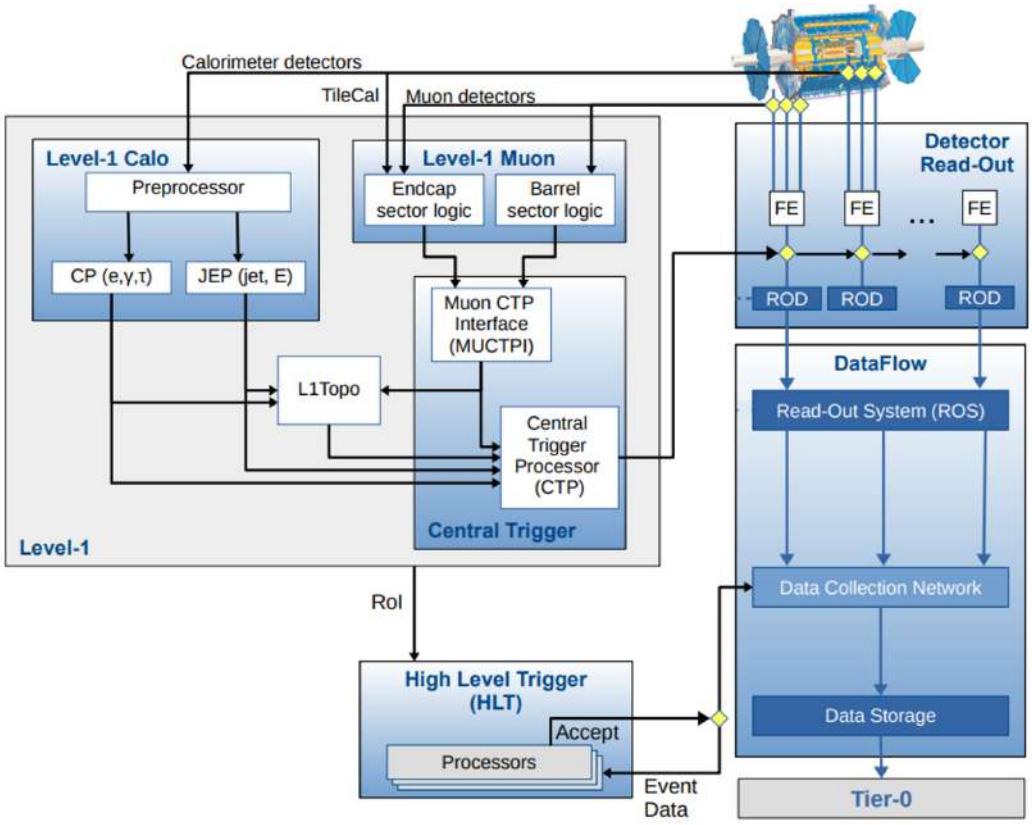


FIGURE 2.3: Block diagram of the ATLAS-Trigger-system [23].

The Regions of Interest (RoI) request data from the ROD system through the data collection network to be processed at the (HLT). The HLT processes these incoming data at approximately 550 ms after the L1A.

The HLT is the final trigger decision level where full process events and the selected events are stored in the CERN computer center for further physics analysis. This level operates at 960 MB/s in conjunction with RoI and event data. The L1 and HLT levels are DAQ for the ATLAS detector.

2.3 The Tile Calorimeter

The ATLAS central hadronic calorimeter is popularly known as TileCal, and it is depicted in Figure 2.4. The (TileCal) [25] is a sampling calorimeter with iron as passive medium and plastic scintillator tiles as active medium. It comprises an inner and outer radius of 2.28 m and 4.23 m, respectively, with a central barrel of 5.56 m long and two extended barrels of 2.91 m, at either end to cover a region within the range of $0 < |\eta| < 1.7$. Each barrel contains steel and scintillator tiles with a total weight

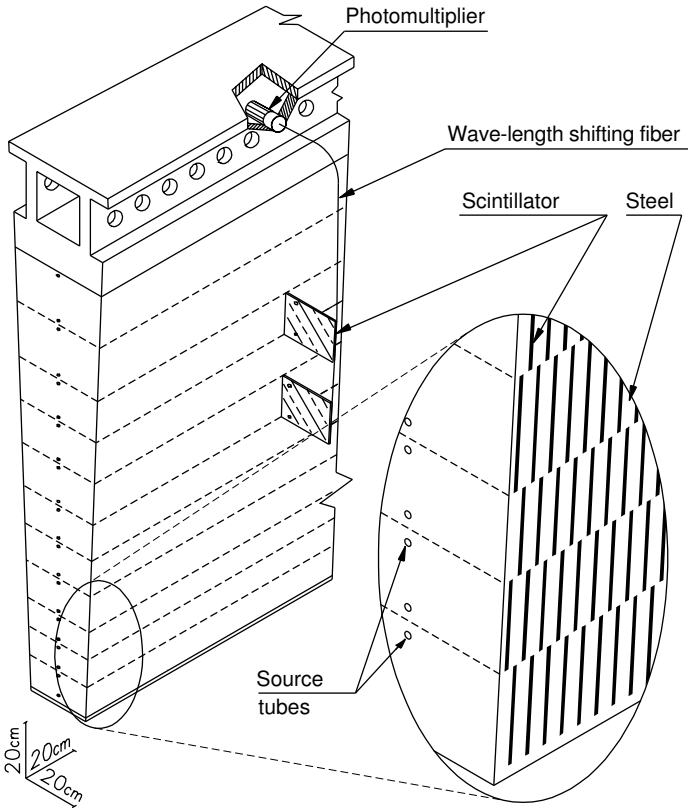


FIGURE 2.4: A schematic of a TileCal wedge-shaped module showing the plastic scintillators sandwiched between steel absorbers. The on-detector electronics drawer is located in the outer radius to read out the PhotoMultiplier Tubes (PMT) [26].

of 2,600 tons. In this instance, the steel and scintillator tiles are used as absorber and active medium, respectively.

The TileCal active medium is made up of scintillating tiles of eleven different sizes [27]. They have radial lengths ranging between 97 mm and 187 mm and are about 3 mm thick. In addition, they also consist of azimuthal lengths ranging between 200 mm and 400 mm, where different sizes of the tile consist of different corresponding depths in radius. To generate the ultraviolet scintillation light in the polystyrene base material of the tiles, the ionizing particles crossing the tiles are activated. Through the use of wavelength shift, this light is converted further to visible light. To protect the tile and improve the scintillation light yield, the tiles are housed within a plastic sleeve. The optical non-uniformity of tiles to a level below 5% for a sum of signals of both tiles is minimized by using the mask pattern contained in the plastic sleeve. The three-dimensional cell structure to form three radical sampling depths, approximately 1.5, 4.1, 1.8λ at $\eta = 0$ is defined by fiber grouping. These cells

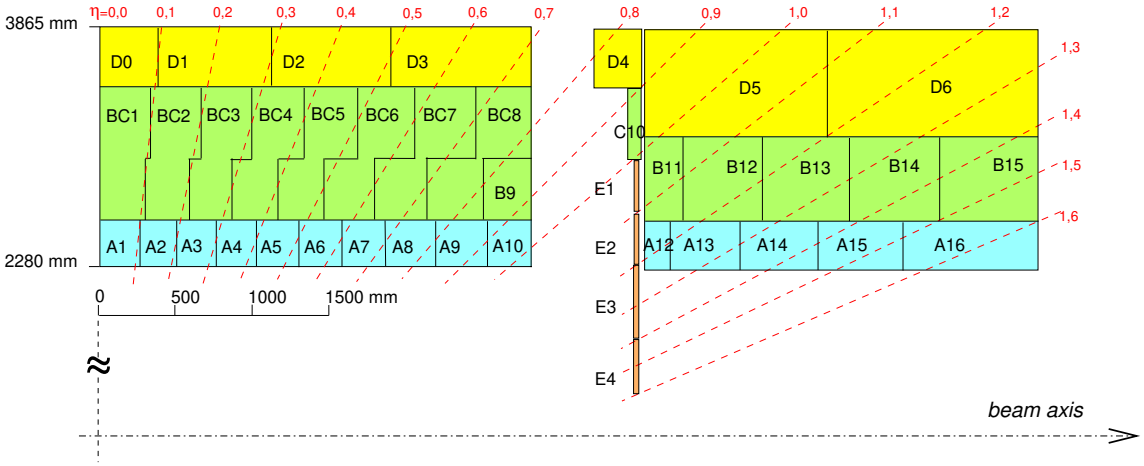


FIGURE 2.5: Segmentation in depth and η of the TileCal modules for half of the long barrel (left) and for an extended barrel (right). The distribution of tileCal cells is symmetric with respect to the interaction point at the origin [27].

consist of dimensions of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ in the first two layers and 0.2×0.1 in the last layer. In Figure 2.5, the depth and η-segmentation of the barrel and the extended barrel modules are illustrated. This figure shows the signals generated by particles crossing the calorimeter at different positions.

The light from the cells is routed to the PMTs through WLS fibers [28]. The PMTs and on-detector electronics are on the outer radius of the module in a rigid steel girder called Super-Drawers (SD). The PMTs convert light into electrical signals that are read out and processed by on-detector electronics. These PMTs, along with all of the readout electronics, are situated in SDs. In total, TileCal contains 256 SD with on-detector electronics. The SD is linked to the off-detector electronics through an optical link, which is explained in detail in Section 3.2.3. Other trigger and readout electronics are situated off-detector in the ATLAS counting rooms (USA15).

Figure 2.6 shows a cross-sectional view of the ATLAS Tile and Liquid Argon calorimeters divided into four logical subdetectors consisting of central long barrels (LBA, LBC) and extended barrels (EBA, EBC). As mentioned above, the on-detector electronics read electrical signals from the PMTs. These signals are digitized at the LHC frequency (40 MHz) with 10-bit Analog-to-Digital Converters (ADCs) and stored in pipeline memories. Additionally, PMTs transmit analog trigger sums of cells to the ATLAS L1 Calorimeter trigger system for L1A and ROI generation.

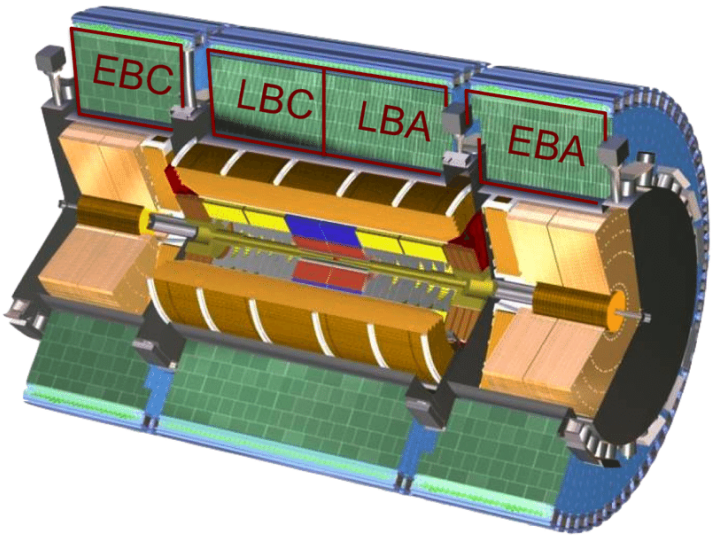


FIGURE 2.6: TileCal partitions: EBA and EBC partitions correspond to the Extended Barrels and LBA and LBC partitions correspond to the central Long Barrel [28].

2.3.1 TileCal readout chain

The complete readout chain of the TileCal front-end electronics is depicted in Figure 2.7. The 3-in-1 cards receive electrical signals from PMTs and amplify and shape them. The PMTs also distribute two copies of the analog signal with a ratio of 1:64. Upon reception of the PMT analog signals by Digitizer boards, the signals are further digitized at the LHC frequency and stored in the configurable-depth pipeline memories of the de-randomizer (TileDMU). In parallel with the readout path, trigger-tower signals are transmitted to the L1 trigger system by summing five signals from three sampling layers. Two signals are from the first layer, another two are from the second layer, and the last signal is from the third layer.

Subsection 2.3.2 to Subsection 3.2.3 detail each stage of the TileCal readout chain and how they all contribute to the data flow. The on-detector electronics include PMTs with 3-in-1 cards, a Digitizer board, an Interface, and an Adder board. The off-detector electronics include the ROD.

2.3.2 On-detector electronics

Photomultiplier block

The PMT block comprises a mechanical structure made of a steel cylinder and a

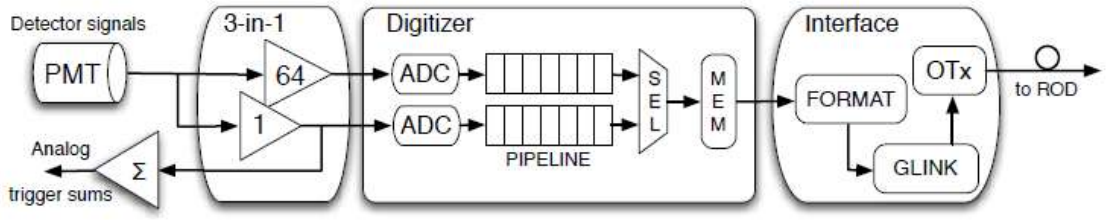


FIGURE 2.7: Block diagram of the current TileCal readout chain [29].

mu-metal shield for magnetic shielding. Each on-detector electronic SD contains 12 PMT blocks in the long barrel and 10 in the extended barrel. Each of these has a light mixer, a PMT, its active High Voltage (HV) divider base, and an amplifier card (3-in-1 card). As shown in Figure 2.8, they are interconnected with the motherboard. The motherboard receives electrical signals from the PMTs, digitizes these signals, and transmits data to the ROD. The PMT block comprises the following main components:

- Photomutlipliers: These specific PMTs consist of a compact size with a volume of $28 \times 28 \times 28$ mm^3. In addition, the PMT has a dynode structure with eight amplification stages.

- Light mixers: To avoid the correlation between the position of the fiber and the area of the photocathode receiving the light, the light mixer is used. This mixer mixes the light that emerges from all the fibers in the bundles. In addition, the PMT relies on the photocathode surface position illuminated.

- Magnetic shielding: PMT consists of mu-metal and iron magnetic shielding. To avoid the gain variations that may be caused by residual fields from the ATLAS solenoid and toroids, magnetic shielding is used. In addition, it should also provide up to 500 Gauss magnetic field shielding in any direction for protection purposes.

- HV dividers: In PMT, the dividers are used to partition the HV between the dynodes. In addition, they also serve as a socket to enable the connection between the PMT and the on-detector electronics. This design aspires to reduce the capacitance between the PMT and the electronics, leading to minimized noise and unreliable connections.

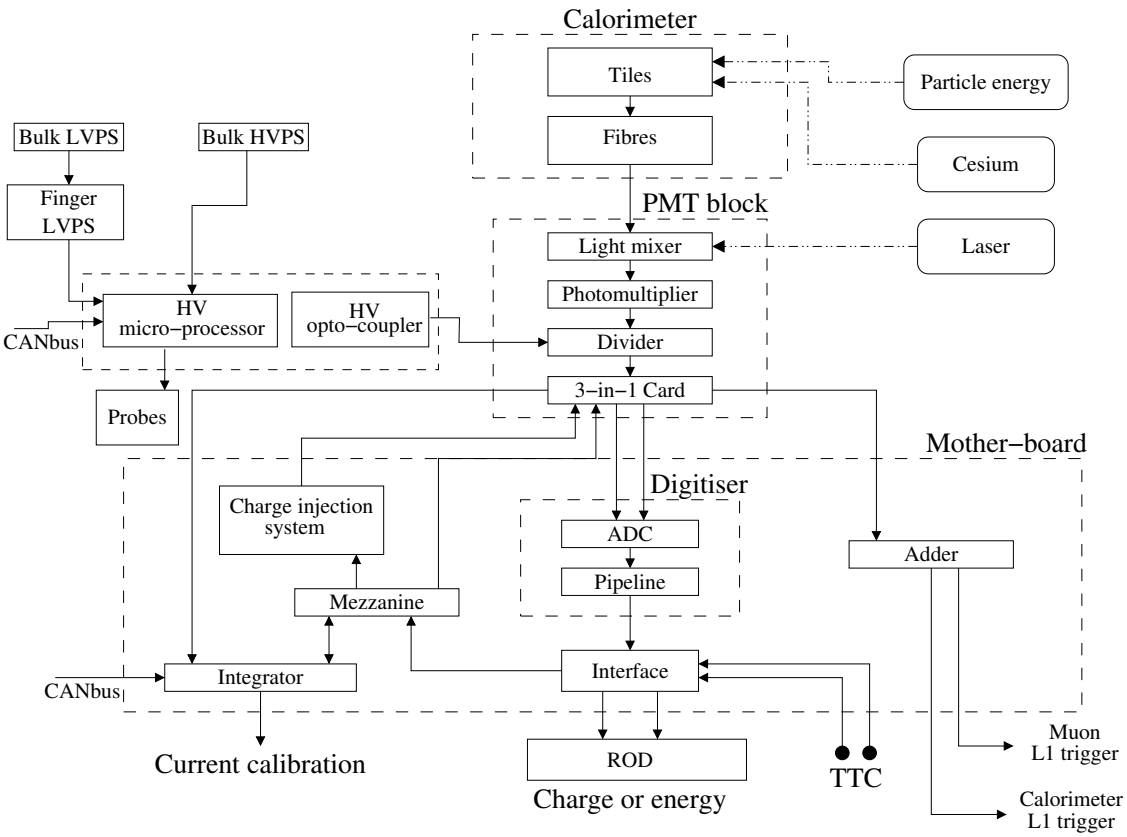


FIGURE 2.8: Block diagram of the TileCal electronics [29].

- 3-in-1 cards: These boards are crucial cards designed with discrete components as part of the on-detector electronics. The main functions of these cards in on-detector electronics are to amplify the PMT signals using the high and low gain, set gains, and also provide calibrations for charge injection. In addition, they also integrate and digitize the current from minimum-bias events. Each PMT produces raw data, which will be digitized and consequently routed to the off-detector for further processing and data acquisition. This raw data is transmitted from the on-detector electronics by an Interface Card.

Digitizer system

There are up to eight Digitizer boards for each SD of the LB and six Digitizer boards for the EB modules. The key components of the Digitizer boards include, but are not limited to, 10-bit ADC, TileDMU ASIC [30], and two 8-bit Digital-to-Analog Converters (DAC). The high and low signals generated from PMT are amplified and shaped using 3-in-1 cards, which are further transmitted to Digitizer boards for digitization every 25 ns. The PMT signals produce high and low gain with a gain

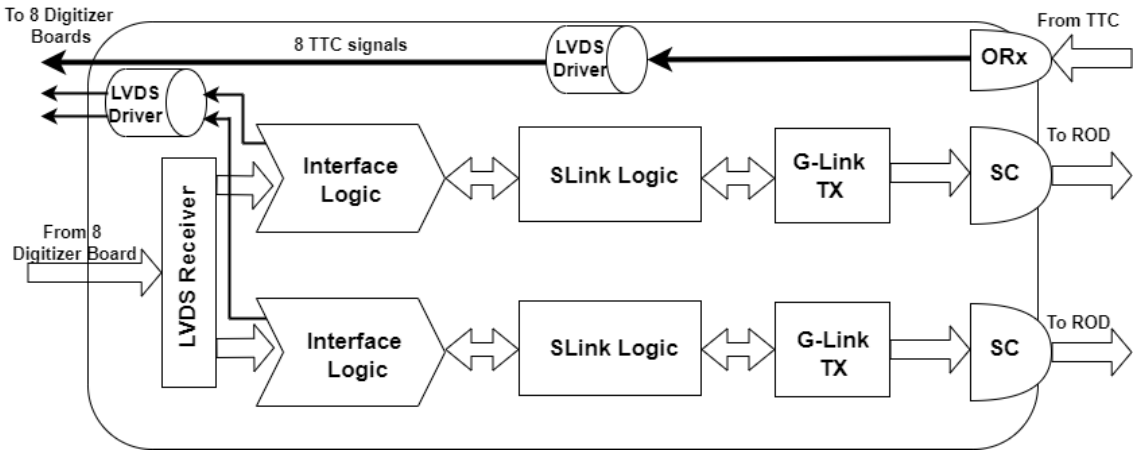


FIGURE 2.9: Block diagram of the Interface board [32].

ratio of 64. Furthermore, the digitized data is stored using the two-depth configurable pipeline memories located in the TileDMU ASIC until received by the L1A. To transmit L1A signals upon their reception to the ROD system in the off-detector electronics, the data frame containing up to 16 samples is further copied into the derandomizer buffers situated on the Interface boards. Although the data bandwidth is always the same, data may be lost if 16 samples are sent due to limited bandwidth during normal operation. Trigger, Timing, and Control receiver (TTCrx) ASIC [31] recovers and distributes the bunch crossing clock to the on-detector electronics.

The clock can collectively be adjusted for all ADCs in a Digitizer board in steps of 106 ps as performed by TTCrx. In addition, the motherboard also has an analog part that provides a voltage reference to the ADCs and two 8 bit DACs.

Interface board

The primary purpose of the Interface Board [32] is to receive and distribute Trigger, Timing, and Control (TTC) signals to the electronics. It also formats the data collected from the digitized boards and uses the optical link to transport the digitized data to the ROD system. The Interface board is considered to be the digital link composed of the off-detector electronics system. To reduce possible errors arising from a single event, the interface board utilizes the implemented redundant readout system with one output fiber, whereas the other output fiber is used as a spare.

Adder board

The analog signals collected from the 3-in-1 cards, which are also made up of the trigger tower, are received by the Adder boards. Furthermore, the boards perform

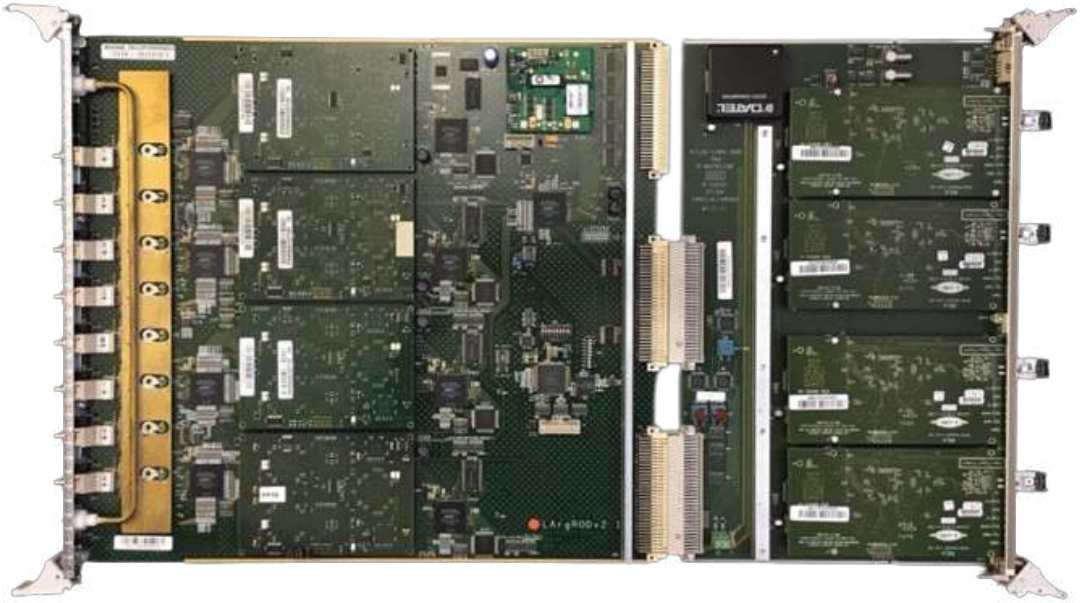


FIGURE 2.10: Block diagram of the TileCal off-detector electronics including the ROD module and Transition Modules [24].

an analog sum on the collected signals. Several sums are present that form trigger towers that are transmitted to the L1Calo and L1Muon systems. An analog sum comprises the sum of all the cells, whereas the analog sums contain the last layer cell.

2.3.3 Off-detector electronics

The off-detector electronics, also referred to as back-end electronics, are situated in the counting rooms of the cavern (USA15), separate from the detector. They are located 70 m away and are categorized into two subsystems, namely the ROD system and the TTC system. In addition, the off-detector electronics are partitioned into four and are dedicated to the readout of the long and extended barrels. These units are further categorized into different crates, namely a $6U$ Versa Module Eurocard (VME) TTC crate and a $9U$ VME ROD crate.

Readout Driver

RODs [33] are responsible for energy and time reconstruction, generating busy data integrity checks and lossless data compression. A total of 32 ROD modules are required to readout the entire TileCal detector. The ROD comprises these key components: the ROD motherboard and four Processing Units (PU). Each of these PUs has two commercial Digital Signal Processor (DSP) chips for data processing

before further transmission to the ATLAS DAQ system. The ROD plays a crucial role in the off-detector electronics by receiving data from the SD via optical links. In total, 8 RODs per partition are required for Tile-level readout. In the rack, a total of 32 RODs are partitioned into four crates, one per barrel. In addition, each ROD consists of a Trigger and Busy Module (TBM). To provide a combined busy signal to the ROD module, the TBM collects the busy signals produced by eight RODs. Additionally, TBM also receives and transmits the collected TTC signals from the local TTC system.

ATLAS Local Trigger Interface (ALTI)

ALTI [34] is a specially designed 6U VME64x module that combines the capabilities of four TTC modules currently used in the experiment. The main purpose of ALTI is to provide the interface between the L1 Central Trigger Processor (CTP) and TTC optical broadcasting network to the ATLAS subdetectors, which includes on-detector electronics. The CTP makes the initial trigger decision by selecting promising possibilities for particles coming from the L1 calorimeter and L1 muon trigger systems. The following are four existing TTC modules currently employed that are replaced by ALTI:

- Local Trigger Processor (LTP): The TTC signals produced by the CTP are received by LTP and further transmitted using the TTCvi module.
- LTP Interface (LTPI): The LTPI utilizes the CTP to exchange information with various LTP modules.
- TTC VME Bus Interface (TTCvi): The TTCVi exchange channel signals A and B with TTCex for its encoding and distribution to the on-detector electronics.
- TTC Emitter (TTCex): The TTCex allows the conversion of the commands received from the TTCvi into optical signals.

In addition to the modules above in the TTC crate, there are other modules that are specifically designed for calibration purposes and also receive, manage, and act at the reception of TTC information.

- Shaft module: This module controls the calibration trigger requests and shares the requests during physics runs.

- TTC Receiver in PCIe Mezzanine Card (TTCpr) module: For calibration runs, TTCpr is primarily used to provide information about TTC to the TDAQ software. In addition, it is also connected to the Single Board Computer (SBC) of the TTC crate.
- Laser readout Driver: This module collects and transmits the Laser Calibration system information to the TDAQ software.

2.4 Summary

Chapter 2 presents an introduction to the TileCal LHC, the data acquisition system of the LHC. The ATLAS experiment and TileCal are introduced in this chapter. A brief introduction of the readout electronics and the ATLAS TDAQ architecture is provided. Chapter 3 introduces the HL-LHC and the ATLAS Phase-II Upgrade electronics readout. A description of every module of the on- and off-detector electronics for the ATLAS TileCal Phase-II upgrades is provided. The operation of the on-detector modules, such as the PMT, Digitizer system, Interface Board, and Adder Board, is explained in detail. The operation of the off-detector electronics is explained in terms of the ROD and the ATLTI.

Chapter 3

ATLAS Upgrades for HL-LHC

The enhanced version of the LHC, popularly known as HL-LHC, is envisioned for a planned Long Shutdown 3 (LS3) period from 2026 to 2028. Compared to LHC, the HL-LHC will produce more than 250 fb^{-1} of data per year and will be capable of collecting up to 4000 fb^{-1} of integrated luminosity. The HL-LHC will also provide a nominal instantaneous luminosity of 5×10^{34} $cm^{-2}s^{-1}$, which is 5 times the initial design value. To achieve this goal in an acceptable amount of time, an average of 200 simultaneous p-p interactions per bunch crossing is required. The integration of Phase-II Upgrades will be utilized to prepare the ATLAS experiment for this tremendous improvement. The function of HL-LHC will be primarily centered around the recently discovered Higgs boson properties measurement. Specifically, this will include the studies of the Higgs coupling to the different fermions and bosons and the precise measurement of the trilinear Higgs self-coupling through monitoring of di-Higgs generation. A detailed overview that illustrates LHC to HL-LHC is shown in Figure 3.1.

Due to the continuous stress experienced by hardware in high radiation and the advancement in the technology deployed, the LHC schedule accommodates three upgrade phases with their corresponding Long Shutdown periods. The first Long Shutdown (LS1) occurred from 2013 to 2014, followed by the second Long Shutdown (LS2) from 2019 to 2021. The first stage, called Phase-0, involves collisions at an increased center of a mass of energy of 13 TeV and also the minimization in the brunch crossing time between 50 ns and 25 ns to be recorded using the required preparations. The second LS2, which started the upgrade of Phase-I, commenced in 2019 for ATLAS, CMS, ALICE, and LHCb. This period involved the installation of

FIGURE 3.1: HL-LHC plan for the next ten years, with a series of Shutdowns with dedicated upgrades and an increase in energy and luminosity [35].

prototypes in preparation for Run-3 to handle the center of a mass of energy of 13.6 TeV.

Since the luminosity is expected to have doubled during this phase, ATLAS upgraded the muon system for the change and also improves its performance. During the LS3, the replacement of hardware for both the accelerator and all detectors begins to take place. After LS3, several subdetectors will be prepared for the HL-LHC luminosity conditions by the ATLAS Phase-II Upgrade. Due to an expected increase in pile-up events per beam crossing in ATLAS of up to 200, a finer granularity is needed for the detector and also an improved TDAQ architecture with the capability to accommodate the trigger rates and amount of data generated. In addition, this luminosity value will also require improved on-detector electronics that are capable of withstanding the expected radiation levels.

Due to this radiation, some of the detectors will be affected and will require a complete upgrade of the traditional detector and electronics. These include ID, the LAr Forward Calorimeter, and the Forward Muon Wheels. However, this does not apply to calorimeters and muon chambers, which do not require improvement in

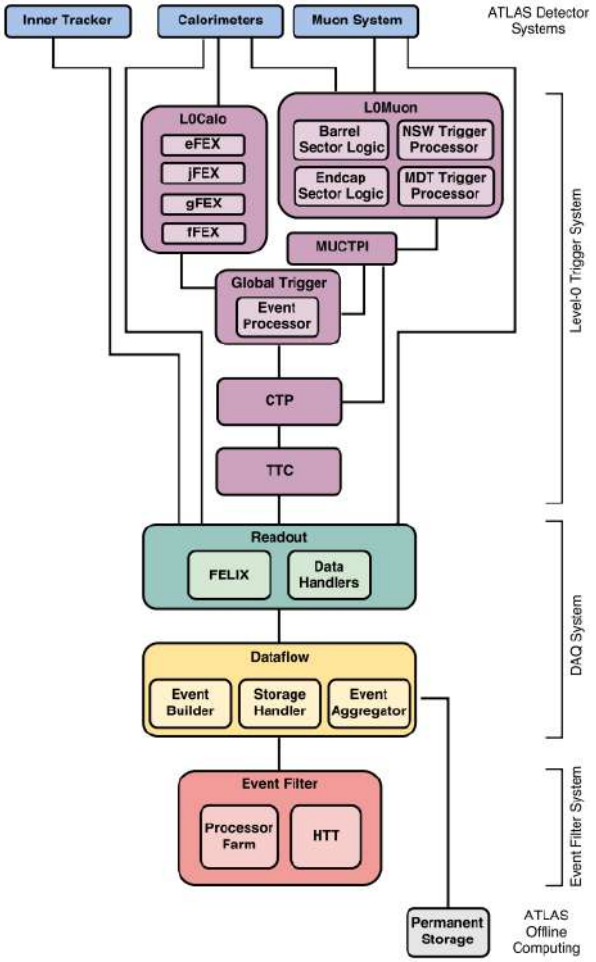


FIGURE 3.2: The TDAQ architecture for Phase-II Upgrades [36].

their structures and active materials. This is only required for an on-detector electronics system to withstand the increased radiation and data bandwidth.

3.1 TDAQ architecture

The transition from LHC to HL-LHC and the increased trigger rates and data volumes emerge along with stringent performance requirements. To meet these requirements, a complete redesign of the TDAQ architecture is required. A block diagram of the TDAQ architecture for the HL-LHC is shown in Figure 3.2 [37]. The architecture is divided into three main systems; the Level-0 (L0) Trigger System, the DAQ system, and the Event Filter (EF) System. The single-level hardware trigger stage and software system, also known as the L0 trigger system and EF, respectively, are the key elements of the proposed TDAQ designed for HL-LHC.

The L0 Trigger system includes hardware-based systems in terms of the L0 Calorimeter Trigger (L0Calo), the L0 Muon Trigger (L0Muon), the Global Trigger, and the Central Trigger subsystems. The calorimeters transmit the coarse granularity data to the L0Calo system to perform the calculations of E_T^{miss} and also identify the electron, tau, and jet candidates. The L0 Muon system reads data from both the Calorimeters and the Muon system. Global Trigger refines the trigger objects calculated by L0Calo and L0Muon, computes event-level values, and runs topological algorithms using full-granularity calorimeter information. The CTP creates triggers from the combinations of inputs or conditions received from the Global Trigger and other sources while driving the Trigger TTC network to begin the readout process of the detectors.

Furthermore, the DAQ system comprises a readout and a dataflow subsystem. The dataflow block in the architecture is responsible for the transport of data, aggregation, and compression of event data. The resulting trigger data and detector data are transmitted at 1 MHz via the readout subsystem where the Front-End LInk eXchange (FELIX) system [38] is located, as well as Data Handler elements. FELIX is used for the readout, command propagation, and transmission to the front-end electronics. The data to the trigger systems is transmitted directly from the TDAQi. In addition, the dataflow includes the components Event Builder, Storage Handler, and Event Aggregator. They are constructed using standard Personal Computers (PC), a common network infrastructure, and servers. Custom input/output cards are included in the Readout system to transform the detector front-end protocol data into common network packets.

The primary purpose of the EF system is to optimize the trigger objects to achieve the desired output rate. A CPU-based processing farm and an HTT co-processor constitute the EF system. The Hardware-based Tracking for the Trigger (HTT) has global (gHTT) and regional (rHTT) track rebuilding capabilities. The Dataflow system receives the EF trigger decision and moves approved events to permanent storage. In parallel to the buffering of the event data, the EF processes the events between fills. Using the software algorithm at a trigger rate of 10 kHz, the EF makes the final trigger decision. This occurs at the final stage of the trigger architecture.

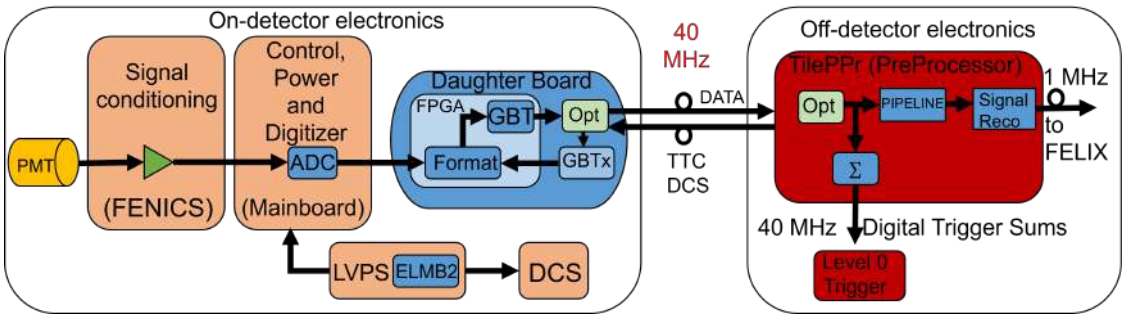


FIGURE 3.3: Block diagram of the TileCal readout architecture for the Phase-II Upgrade [39].

To meet the latency requirements of the improved TDAQ system, the detectors aim to employ a large pipeline of memories to store data generated from each level.

3.2 The Tile Calorimeter Upgrade

The motivation behind the TileCal upgrade involves the aim of meeting the requirements emerging with HL-LHC. To fulfill the increased radiation tolerance requirements, a complete reconstruction of the readout electronics for the Phase-II Upgrade is expected. In addition, this reconstruction will allow the Phase-II Upgrade to be suitable for the TDAQ architecture. This aspires to deliver more precise and higher-granularity data to trigger systems. Figure 3.3 shows a block diagram of the TileCal readout architecture for the Phase-II Upgrade. The architecture is divided into two stages, on- and off-detector electronics.

The on-detector electronics are detailed in Subsection 3.2.1 in terms of the PMTs, FENICS, MainBoard, and the Daughterboard. Each block of on-detector electronics performs a specific function on the overall performance of the ATLAS TileCal Phase-II Upgrades. FENICS are used to shape and amplify these signals in two gains. An increase in the dynamic range of digitization from 16 bits to 17 bits is introduced in the upgrade system. One MainBoard [40] is allocated to each mini-drawer, and it is used to digitize the PMT signals by 12-bit dual ADCs. A DaughterBoard [41] is used to collect digital samples from the MainBoard ADCs. The data collected is then transmitted through the high-speed link to the off-detector electronics. A Low Voltage Power Supply (LVPS) [42] is used to power four mini-drawers.

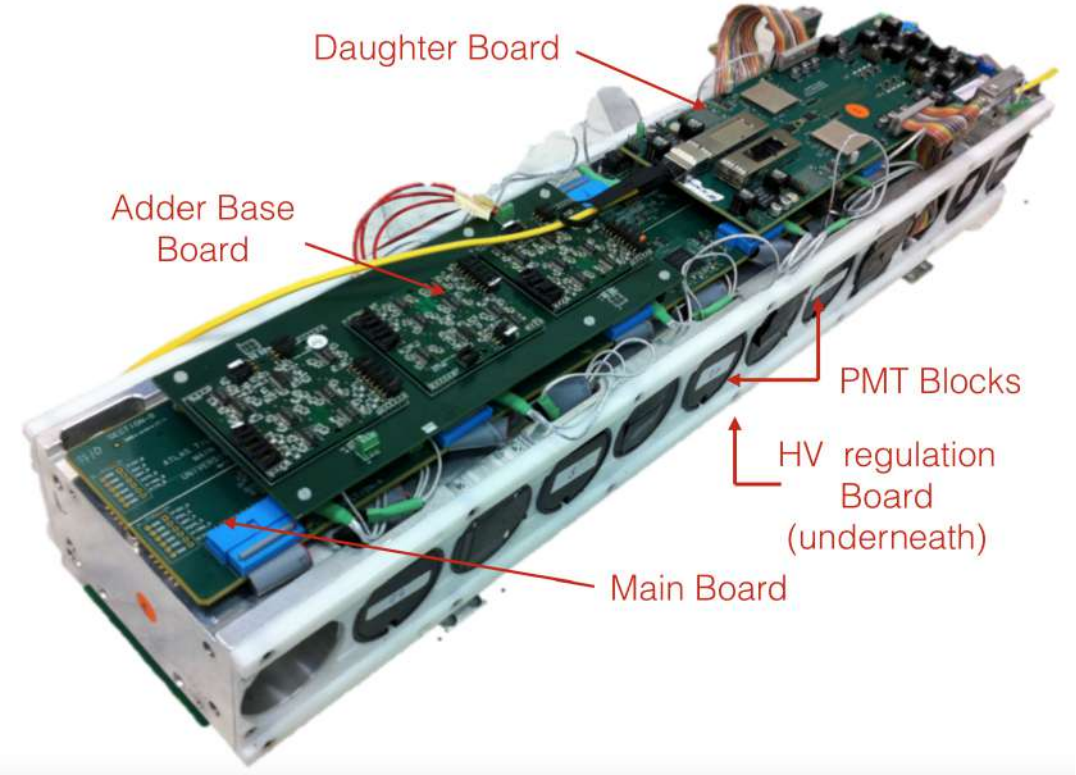


FIGURE 3.4: Picture of the TileCal modules and mini-drawers [43].

The off-detector electronics aspire to read out the detector and also to deliver the preprocessed trigger objects generated by cells to the trigger system at the LHC frequency. The off-detector is divided into a TilePPr and a Tile Trigger and Data Acquisition Interface (TDAQi). The TilePPr module is composed of an Advanced Telecommunications Computing Architecture (ATCA) carrier with four Advanced Mezzanine Card (AMC) [44] slots to host the CPM [45]. The TilePPr receives digital data from the on-detector electronics at the accelerator frequency. One TilePPr is composed of 4 CPMs. Each TilePPr reads out and operates up to eight TileCal modules, where each CPM reads out two modules. The CPMs are responsible for storing the digitized samples in pipeline memories until the reception of a trigger acceptance signal and online energy reconstruction. Then, the triggered data are transmitted from the CPMs to the FELIX after reception from the ATLAS trigger system. The TDAQi receives the reconstructed energy per cell from the CPMs and creates trigger objects [46]. These trigger objects are sent to the ATLAS trigger system for every bunch crossing 25 *ns*.

In the legacy system, 256 optical links with a bandwidth of 800 Mbps for each

FIGURE 3.5: Picture of the PMT block [47].

link is required to readout the detector. Compared to this traditional system, the upgraded architecture consists of 16 uplinks and 8 downlinks per LB module and 12 uplinks and 6 downlinks per EB module. A total of 1,792 optical links for downlinks with a bandwidth of 4.8 Gbps and a total of 3584 links with a bw of 9.6 Gbps is needed for the Phase-II. In addition to the use of high-speed links between off-detector electronics and trigger systems, a new TDAQ architecture requires a considerable amount of bandwidth and a number of links.

3.2.1 On-detector electronics

The Tile on-detector electronics are contained within a mechanical structure known as mini-drawers. To organize and divide the on-detector electronics into four independent modules as shown in Figure 3.4, the mechanical design of the SD is changed from two drawers to four drawers. Furthermore, this change allows easy access and serviceability while simultaneously minimizing the impact of single-point failures.

PMT dividers and FENICS

The operation of PMT modules for the TileCal Phase-II Upgrades [47] is similar to that of PMT in the legacy system. However, the new and old design includes active dividers which are used to stabilize the PMT gain, instead of passive resistor as in the legacy system. In the new HV dividers, the active components and transistors were originally designed to offer constant gain independently of the anode current

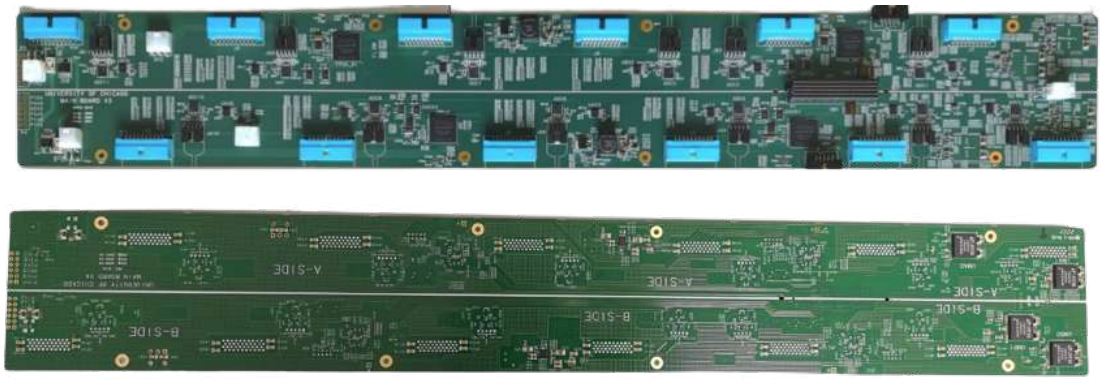


FIGURE 3.6: Picture of the MainBoard (Front and back) [40].

at the HL-LHC. In this instance, the anode currents are expected to be greater for some cells as a result of the pulse rates.

Placing FENICS [48] in close proximity to the PMT reduces the signal path, which in turn minimizes the source capacitance and noise pick-up. The FENICS receive pulses from the PMTs, shape and prepare them for the ADCs that are based on the MainBoard using two gains. Additionally, these FENICS also offer slow integrator signals that are required for luminosity monitoring and detector calibration. The gain ratio between the high and low gain of the FENICS output is 40.

MainBoard

The primary function of the MainBoard [49] shown in Figure 3.6, is to control the FENICS while providing a high-speed route to deliver the digitized PMT signals to the DaughterBoard. The main components of this board are four Altera Cyclone IV FPGAs, which are used in the configuration and control of FENICS. In addition, the MainBoard includes the circuitry to digitize the signals generated from the ADCs. The operation of converting the analog to digital signals is performed by the ADCs on the MainBoard. The MainBoard uses dual 12-bit ADCs to digitize signals from PMT blocks and 16-bit ADCs for all the slow integrator signals. These digitized data for the fast ADCs is then transmitted at 560 Mbps to the DaughterBoard.

The DC-to-DC converters installed in the MainBoard convert +10 V input to five logic voltages (±5 V, +2.5 V, +1.8 V, +1.2 V). These voltage values are transmitted to the DaughterBoard (DB) for monitoring after being buffered. Four serial configuration devices for each MainBoard are used to store parameters for FPGAs.

FIGURE 3.7: Picture of the DaughterBoard version 6 [50].

DaughterBoard

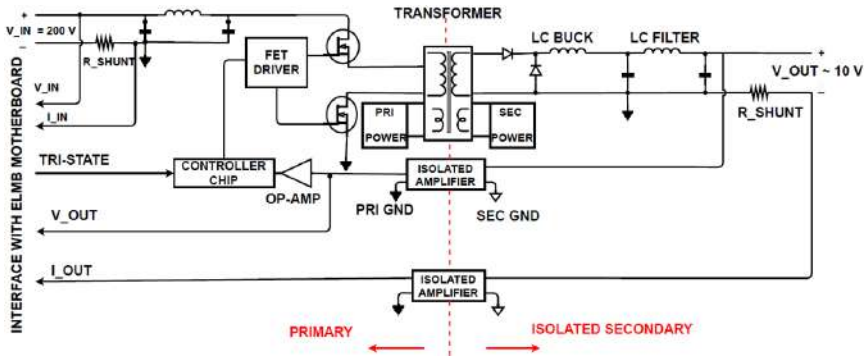
The DB [50] serves as the interface path between the Tile on-detector electronics and the off-detector electronics located in the counting rooms (USA15). This link is connected through the multi-gigabit optical links with the off-detector TilePPr. As part of the on-detector electronics, the DB receives and executes configuration commands. In addition, it will also collect the digitized signal collected from the PMT and send it to TilePPr. For the digitization of PMT signals, the DBs are also used to distribute the improved LHC clock to the FEBs. To allow additional redundancy, the DB is divided into independent halves. Each side comprises six PMTs on one side of the drawer. Figure 3.7 shows version 6 of the DaughterBoard for the ATLAS TileCal Phase-II Upgrade.

Two FPGAs (one for each side of the board) are installed on the DB for data transmission to the off-detector electronics. Split power distribution planes with independent power supplies are implemented to power the DB. Small Form-factor (SFP) connectors establish the electrical-optical interface for the fiber cables.

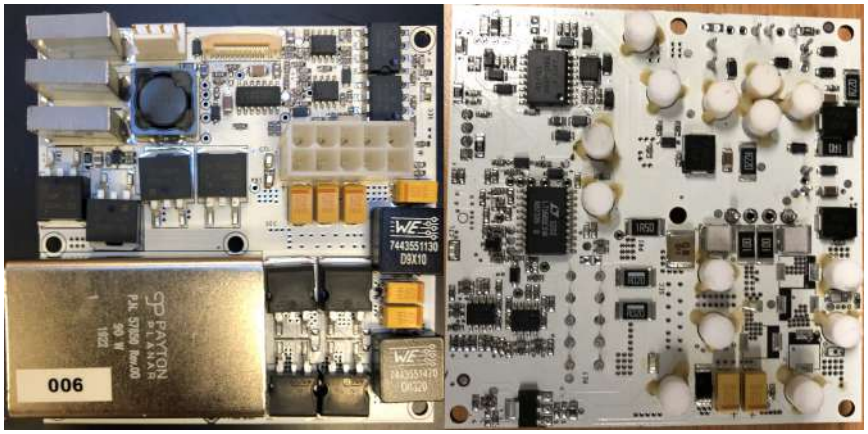
3.2.2 Power supplies

Low-Voltage Power Distribution

The low-voltage power distribution schema has undergone several versions. Figure 3.8 shows version 8.4.2 of the LVPS brick. The left figure shows the schematic, and the right figure shows the populated PCB. Using a three-stage power distribution system, the low-voltage power is distributed to the on-detector electronics. The



(A) A block diagram of the Low Voltage Power Supply brick



(B) Front (left) and back (right) of the Low Voltage Power Supply brick

FIGURE 3.8: Low Voltage Power Supply brick [42].

bulk 200V commercial power supply is responsible for the first stage of the Low Voltage (LV) distribution system [51] [52]. The second stage involves the generation of 10V by the upgrade bricks inside the finger Low Voltage Power Supplies (fLVPS). An fLVPS consists of eight bricks with the same design to power the mini-drawer modules. In the third stage, Point-of-Load (POL) converters transform the incoming 10V into the necessary voltage for the front-end electronics located on the Mainboard.

The LT1681 controller chip [53], a dual transistor synchronous forward controller with a maximum output duty factor of 45%, is the main component of the design. It produces the drive pulse at a frequency of 300 kHz. Field Effect Transistor (FET) drivers are responsible for driving the current and voltage on the primary side of the transformer. The secondary side of a transformer includes a buck converter that converts the signal to a constant voltage for the output. In addition, the DCS system is used to monitor and control the fLVPS bricks. However, a sufficient amount of effort has been made to allow the fLVPS bricks to be radiation-tolerant.

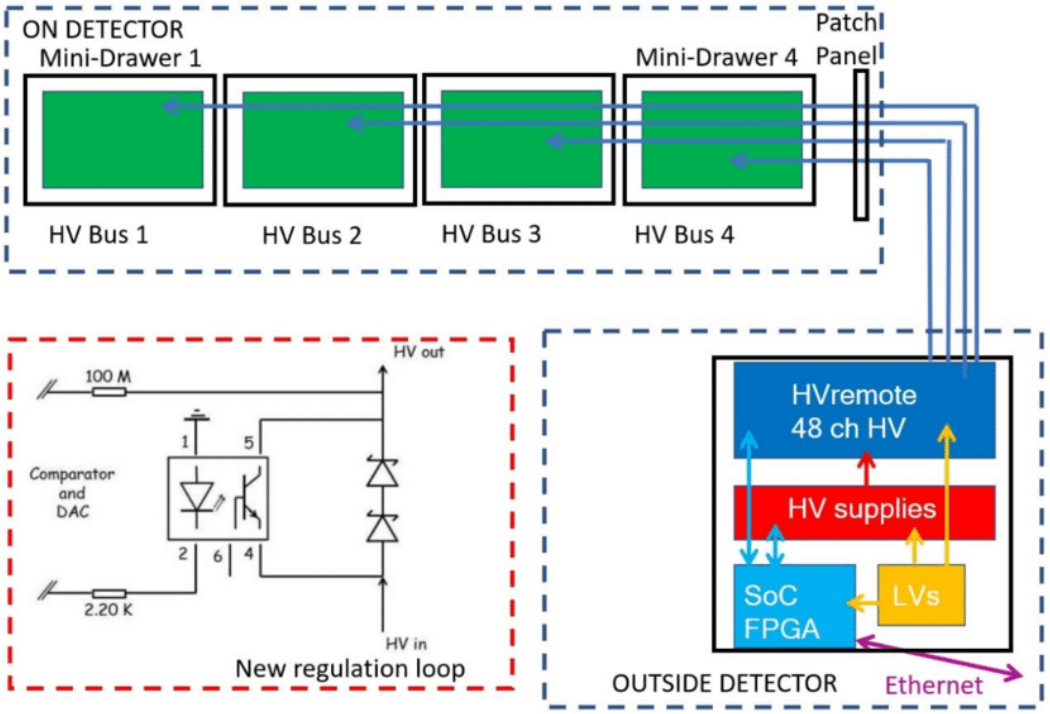


FIGURE 3.9: High-Voltage for Phase-II Upgrade [54, 55].

High-Voltage Power Distribution System

The Phase-II Upgrade will include HV remote boards and respective HV supply boards for TileCal's HV system. Figure 3.9 shows the block diagram for the TileCal readout chain. The regulation of this system is remotely located at a distance from the detector using a large number of 100 m long cables to bring the HV to the detector modules. Passive HV boards are installed in the mini-drawers to transport the HV to the PMTs. The HV remote boards are the boards that regulate the HV for each individual PMT of TileCal using the regulation loop.

A detailed implementation of the High Voltage Power Supply (HVPS) for the LBs is depicted in Figure 3.9. The HV remote includes an System-on-Chip (SoC) FPGA (Zybo Z7 Zynq) that enables the two Serial Peripheral Interface (SPI) buses to be utilized at the same time. One SPI is used for the HV remote boards, while the other SPI is used for the HV supply boards. Each PMT will receive the HV independently through individual wires.

In the HV remote system, access to HV boards for maintenance will be easy, as the electronics will be located in the USA15. Additionally, this system will also not require radiation-tolerant electronics. In contrast, the shortcomings of this system

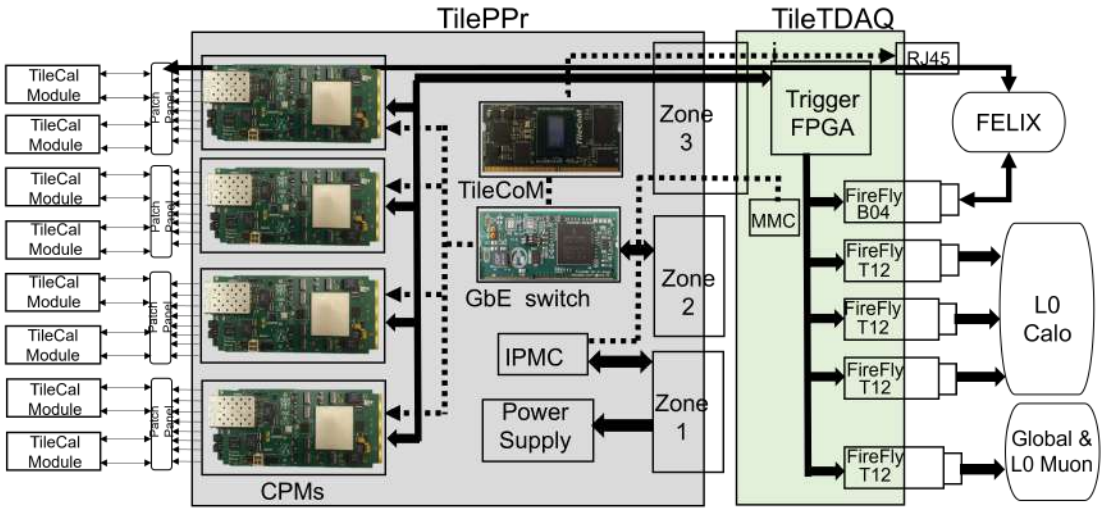


FIGURE 3.10: The TilePPr Phase-II Upgrade system [57].

are that it requires almost 10,000 of 100 m long wires. HV remote prototypes are ready and have been tested for performance. Performance results [56] show that all prototypes supply HV as required to the PMTs and the remote HV boards perform regulation according to the specification.

3.2.3 Off-detector electronics

TilePPr for the Phase-II Upgrade system

The digital samples from the Daughterboard are transmitted to the off-detector electronics. Figure 3.10 shows a block diagram of the TilePPr. The CPM is the core of the TilePPr reading out and operating the TileCal modules. It is responsible for storing the digitized samples in pipeline memories until the reception of a trigger acceptance signal. The Tile Trigger and Data Acquisition interface (TDAQi) receives the reconstructed energy per cell from the CPMs and creates trigger objects [46]. Depending on the trigger system, the reconstructed information contains calibrated energy for each cell.

The FELIX system, the central component of the ATLAS DAQ system, receives the selected data events after the trigger decision. TDAQi system constructs the trigger primitives and interfaces with the trigger and FELIX systems. Both systems use four racks (VME and ATCA) as well as 32 boards for the final design. An approximate bandwidth for each board for the upgrade system is 1.28 Tbps. The readout

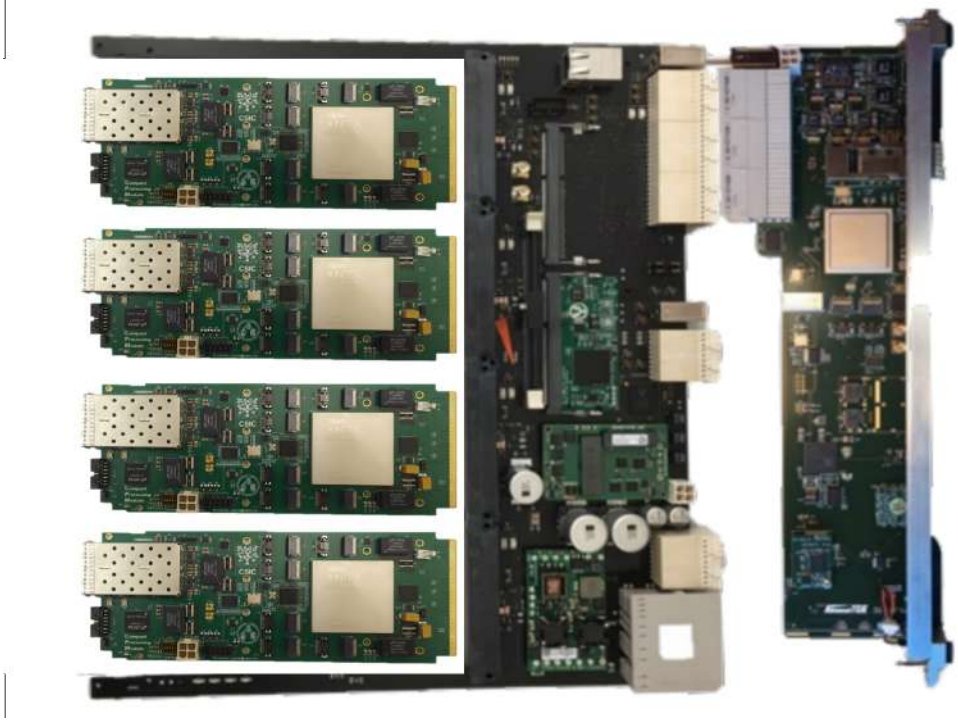


FIGURE 3.11: A picture of the ATCA carrier board with 4 CPMs and a TDAQi [58].

system will be partitioned into four shelves. Two ATCA shelves will be used for the long barrel and two to the extended barrel. One TilePPr module will be connected to eight TileCal modules from the on-detector electronics. The TDAQi is a Rear Transition Module (RTM) of the ATCA explained in detail in Subsection 3.2.3. The on-detector electronics are also redesigned to align with the upgrade system of the off-detector electronics.

As the final design of the TilePPr system will be a full-sized ATCA blade, three backplane connectors are used to connect to the shelf ATCA. Figure 3.11 shows a picture of the ATCA carrier board with 4 CPM and a TDAQi. These connectors are called zones 1 to 3 and are described as follows:

- Zone 1: This zone is used to provide slow control paths for shelf management and power connections.
- Zone 2: This zone is used for communication purposes amongst the TilePPr modules.

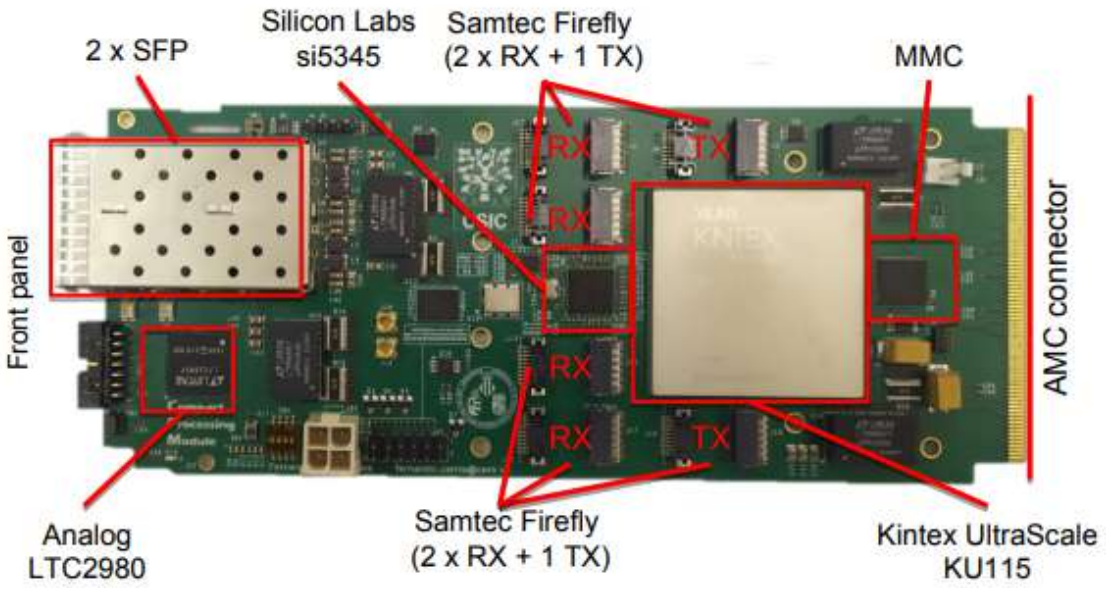


FIGURE 3.12: Version 2 of the Compact Processing Module [45].

- Zone 3: This zone is used to provide high-speed connections between CPM and TDAQi.

Compact Processing Module (CPM)

Figure 3.12 shows the second version of the CPM for TilePPr. This is a 14-layer module with six power distribution layers and eight for high-speed and control signals. The CPM is made up of several components including the Xillinx Kintex UltraScale (KU115 FPGA) [59], the Module Management Controller (MMC), Samtec Firefly optical modules, and others. The Xillinx Kintex UltraScale FPGA is responsible for data acquisition and processing.

One ATCA [60] Carrier Blade Board (ACBB) will be equipped with of 4 CPM boards. The ACBB has been designed to provide a maximum of 400 W at 12 V, as well as connectors for all TilePPr components. The final design of the TilePPr includes a total of 128 CPMs and 32 ATCA carriers required to read out the entire TileCal detector in the HL-LHC. One CPM will operate two TileCal modules where one long barrel consists of 45 PMT channels and one extended barrel with 32 PMTs. Thus, in order to communicate with the on-detector, the CPM includes four receivers and two transmitter Samtec FireFly modules to interface with the detector. These are high-speed communication modules used to transmit detector data at 9.6 Gbps (four uplinks) through 32 GBT links. The SFP modules are used for the FELIX interface.

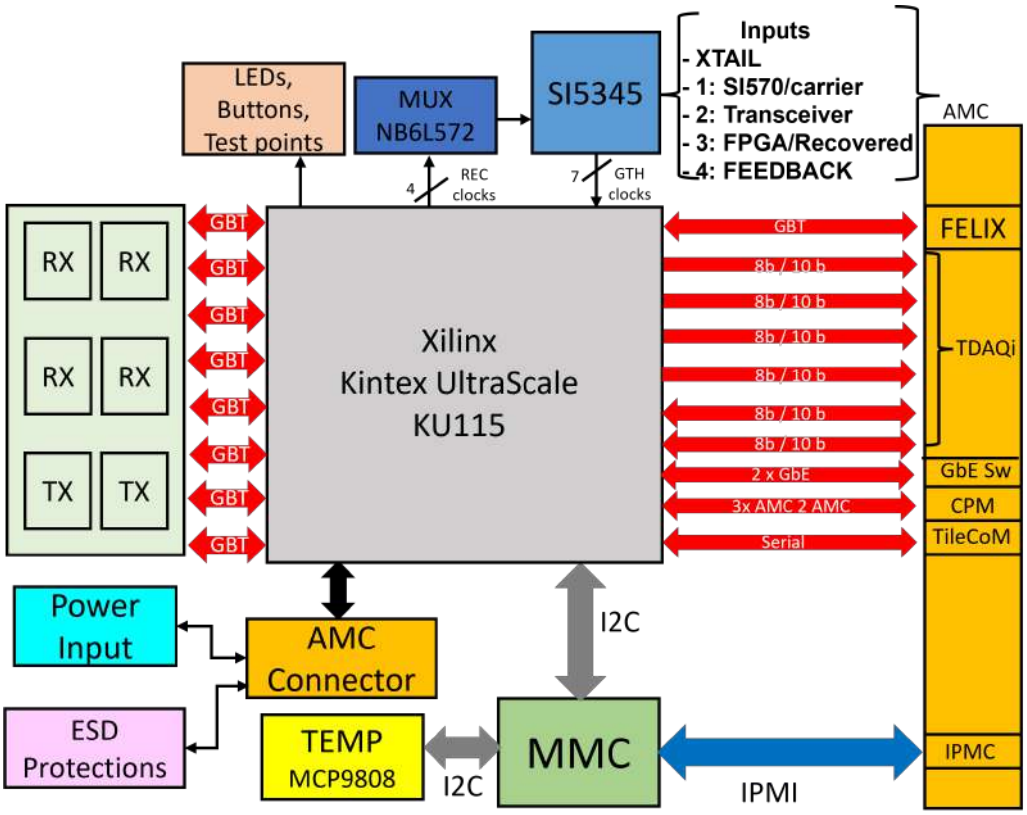


FIGURE 3.13: Compact Processing Module block diagram [45].

The LHC clocks are also transmitted at 4.8 Gbps (downlinks) and the reconstructed energy is transmitted to TDAQi via 4 FELIX FULL-mode e-links.

Figure 3.13 shows a block diagram with the main components of the CPM. The CPM receives power from the ATCA carrier through the AMC connector. Control and monitoring are performed by the MMC that is connected to the Intelligent Platform Management Controller (IPMC) through the Intelligent Platform Management Interface (IPMI). The MMC controls and acquires monitoring data from the sensors and CPM through the I^2C protocol. The CPM includes a clock circuitry architecture that is designed for several functions, such as utilizing the dedicated output clock buffers to directly extract the recovered clock from the MGT transceivers. The circuitry also utilizes the Si5345 jitter cleaner to clean the clock before returning it to the main FPGA.

Tile Computer-On-Module (TileCoM)

The TileCoM is used as an entry-point computer to remotely access the entire TileCal readout electronic system. The TileCoM is a SoC based system that is connected to the CPMs, GbE, and TDAQi board, through the ATCA carrier. As this is the

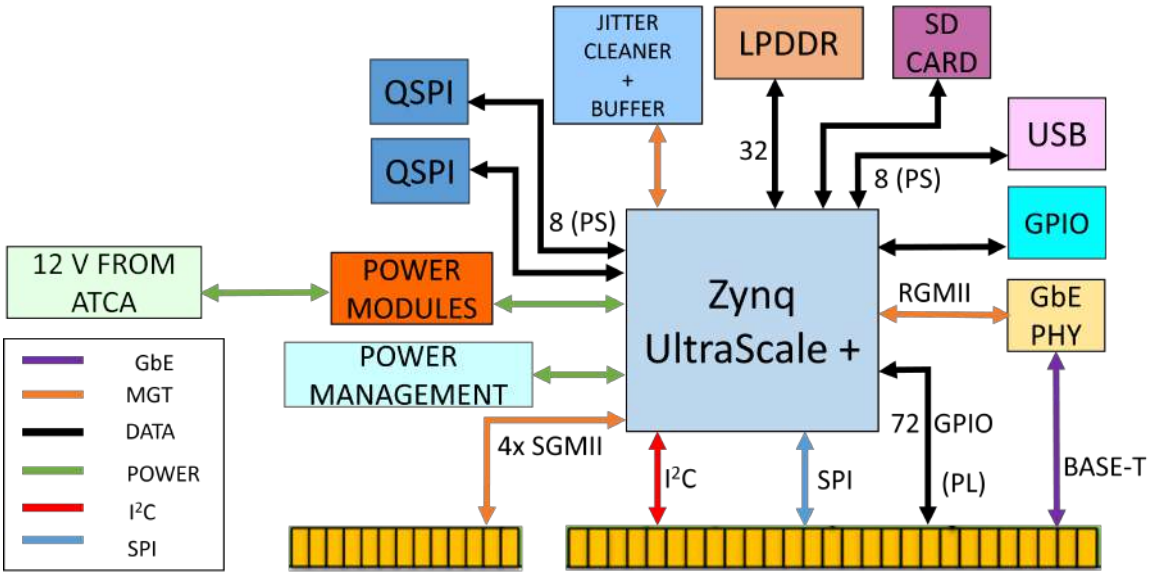


FIGURE 3.14: Block diagram of the TileCoM.

main objective of this document, a detailed design of this board is clearly detailed in Chapter 4. For the final design, this board will be connected to the ATCA carrier board through a Small Outline Dual Inline Memory Module (SODIMM) socket.

Similarly to all the modules of the TilePPr modules, the TileCoM is also designed to meet the system requirements of the TilePPr and ATLAS TileCal Phase-II Upgrade. These requirements are in terms of the size of the PCB, manufacturing materials, thickness, power, and the network specification requirements. All these specification requirements need to be met for the TileCoM to be compatible with the TilePPr. These requirements are clearly described in the Technical Design Report (TDR) [61] for ATLAS TileCal, the ATLAS SoC requirements [62] and the ATLAS Technical and Control Network (ATCN) requirements documentation.

Figure 3.14 shows the TileCoM hardware architecture with the main components used for the TileCoM functionality. Figure 3.15 shows a picture of the first TileCoM prototype. This is a 10-layer PCB with four power layers and six signal layers. The TileCoM meets the ATLAS TileCal TDR for the HL-HLC, adhering to the TDAQ architecture requirements.

To meet the HL-HLC specifications and requirements, the main objectives of the TileCoM are as follows:

- Implementation of remote programming using Xilinx Virtual Cable (XVC) IP

FIGURE 3.15: Picture of the first prototype of the TileCoM.

cores. The ATCA carrier includes one master Joint Test Action Group (JTAG) chain for the CPMs and TDAQi, and one remote JTAG chain per two Tile Modules through the CPMs.

- Interface with the DCS system through a dedicated GbE port from sensor monitoring reading from ATCA carrier, TDAQi and on-detector electronics.

- Interface to the TDAQ system for slow control and configuration of TilePPr and all on-detector electronics.

Tile GbE Switch

Figure 3.16 shows a block diagram of the Tile GbE Switch to connect the TilePPr modules to the network. The main components on the Tile GbE Switch, as shown by the block diagram, includes; power modules, an Ethernet Switch module (BCM5396-KFBG) [63], a configuration unit (ATMEGA168A) [64], and others. The design and PCB verification tests are part of the objectives of this thesis. The design is clearly described in Chapter 4 of this documentation, and Chapter 6 shows the integration of this module with the TilePPr modules.

The Tile GbE Switch is a small card with a total PCB size of 30 mm x 67.60 mm. The size of this card was a priority in the design, as this module will be part of the TilePPr modules fitted on the ATCA carrier. The Tile GbE Switch prototype used for the development of this thesis is manufactured by two South African companies,

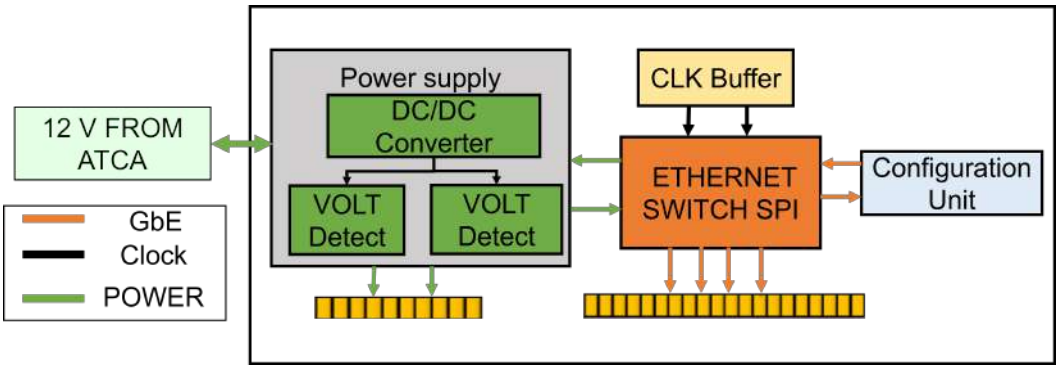


FIGURE 3.16: Block diagram of the Tile GbE Switch.

Trax Interconnect [65] and Jemstech [66]. Trax Interconnect was responsible for manufacturing the PCB and Jemstech populated the PCB with components. Similarly to all TilePPr modules, this module is powered by the ATCA with 12 V.

Figure 3.17 shows a second prototype of the Tile GbE Switch inserted on the motherboard to connect the TilePPr modules to the network. System integration tests of this module with the TilePPr modules are performed in stages. The first stage includes standalone tests where communication tests from the Tile GbE Switch to the TilePPr modules are performed. This test involves integrating the Tile GbE Switch with the TileCoM through the Tile GbE Switch motherboard. However, only the TileCoM evaluation board was used to test communication for the first stage of integration tests. Successful hardware validation and communication tests with the PCB were obtained after manufacture. The TileCoM functionalities were implemented using the Switch for the first stage. The second stage of the test involves inserting the Tile GbE Switch into the ATCA carrier and performing communication tests with the TilePPr modules.

Intelligent Platform Management Controller (IPMC)

Figure 3.18 shows the functional block diagram of the CERN IPMC mezzanine module [67]. This module is compliant with the DIMM-DDR3 VLP form factor and the connector pin-out is aligned with the ACBB carriers. The Tile IPMC is designed with an SoC FPGA where all firmware applications are implemented on the embedded ARM Cortex M3 processor. This SoC FPGA (A2F200 FPGA) is connected to external components such as Ethernet PHY, Electrically Erasable Programmable Read-Only Memory (EEPROM), flash memory, I^2C buffers, and IOs to interface with the Intelligent Platform Management Bus (IPMB).

FIGURE 3.17: The Tile GbE Switch second prototype board produced in South Africa inserted in a motherboard.

This module interconnects with the MMC on the CPM through the local Intelligent Platform Management Bus (IPMB-L). Thus, it can also be used for control and monitoring purposes of TilePPr and on-detector electronics. All ATCA modules are connected to the IPMC through the IPMB-L bus for data traversal. Components such as the fan tray and the power entry module are controlled by the shelf manager. These components can be remotely controlled through the IPMC to control the health status of TilePPr modules. The main functionality of this IPMC includes monitoring in terms of temperatures, voltages, current, and control in terms of fan speed and power management. The Shelf Managers are external interface systems that run embedded Linux to access the components of the ATCA. A maximum of 2 shelf managers can be used for a single ATCA. The first ATCA shelf manager is always active for a fully functional ATCA, and the second shelf manager is used as a backup in case of the active shelf manager malfunctions.

Figure 3.19 shows a picture of the CERN-IPMC mezzanine module. ATCA shelf managers communicate with this module through the zone 1 connector "(backplane) of the TilePPr. A connection to the TDAQi is also established through zone 3 of the ATCA, and this communication is also used to control and monitor the TDAQi module. These two communications are established through IPMB-A and IPMB-B,

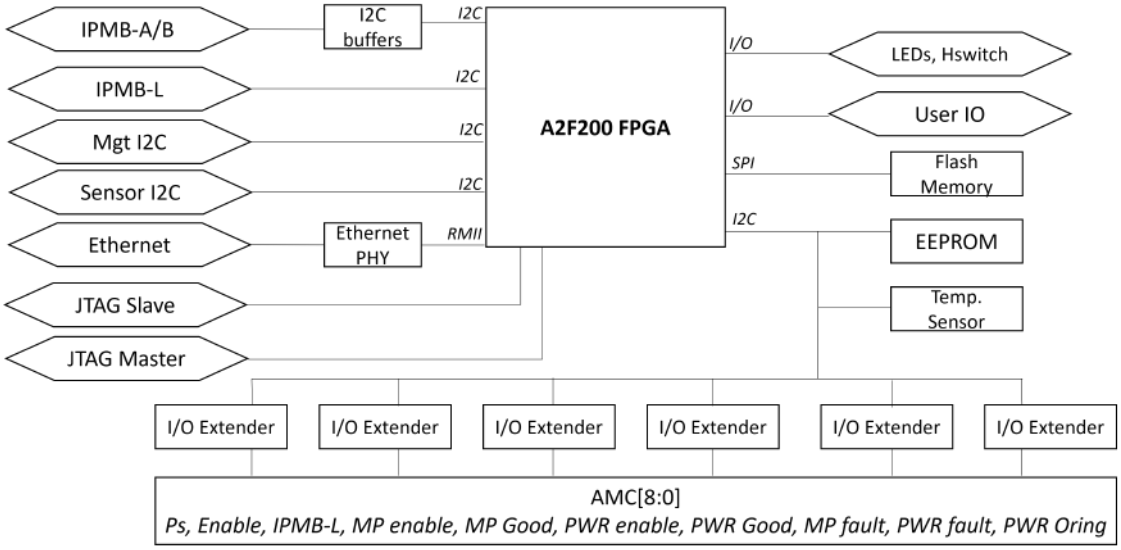


FIGURE 3.18: The CERN IPMC functional block diagram [68].

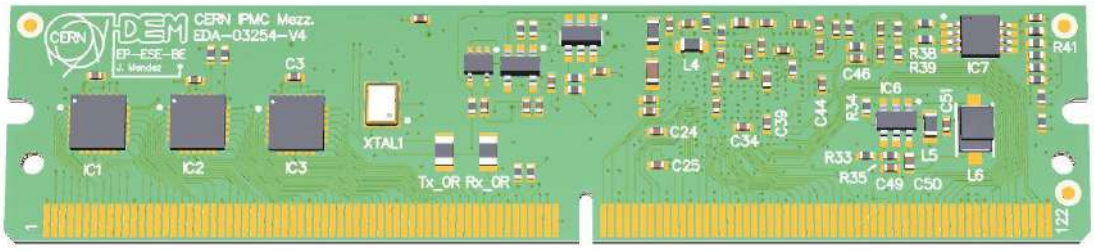


FIGURE 3.19: A picture of the CERN-IPMC mezzanine card [68].

with specific hardware addresses for each dedicated module.

The IPMC is also responsible for the power management of the ATCA, hence the connection to zone 1. The functionality is included and defined in the software design that is implemented on the SoC FPGA processor. The IPMC is dedicated to controlling the input voltage of the ATCA to 12 V, which is used to supply all TilePPr modules. The sensors included in the IPMC module, such as the temperature sensor, can be used to control the fan speed, and thus control the temperature of the TilePPr modules. This module also includes JTAG interfaces to configure the onboard FPGA.

TDAQi board for the Phase-II Upgrade system.

The TDAQi constructs several trigger primitives with variable granularity and different resolutions. The ATLAS Phase-II trigger system, which consists of the L0Calo Trigger, L0Muon Trigger, and the Global Trigger, is then supplied with the trigger

FIGURE 3.20: The TDAQi Phase-II Upgrade board [57].

primitives by the TDAQi through low- and deterministic-latency optical communications. Figure 3.20 shows the TDAQi board for the TileCal Phase-II Upgrade. The TDAQi is an ATCA-standard RTM module designed to process the cell energies received from the CPM and transmit the trigger primitives to the ATLAS Trigger System. This module uses Kintex Ultrascale+ FPGA (XCKU15P-2FFVA1760E) [69] from Xilinx. As the main core of the TDAQi module, all main functionalities and data flows are implemented in the FPGA processing FPGA. This includes the implementation of various high-speed data links with different data protocols and data processing algorithms. This FPGA involves a large number of high-speed interfaces, such as (GTY/GTH) and logic resources. Other components included on the module are optical transceivers such as four samtec firefly, which provides 12-way transmitters, and a single samtec firefly, which provides 4-way bi-directional transceiver.

The TDAQi module is also powered through the ATCA carrier through the Zone 3 connector with a 12 V power supply. This 12 V payload power is then converted to different voltages using different voltage regulators. In total, there are six power regulators in the module. The maximum allowable power of the TDAQi module according to the ATCA specification is 50 W. The TDAQi module also includes Management Power (MP) to power subsystems such as the MMC and associated circuitry. The MMC is implemented with the ATmega128L-8AU microcontroller. This mezzanine module is used for hot-swap power management, sensor reading, and communication with the IPMC. As explained in the IPMC Section, the sensor monitoring data of this MMC is transmitted to the IPMC.

The TDAQi requires a total of 6 power voltages, where three power converters,

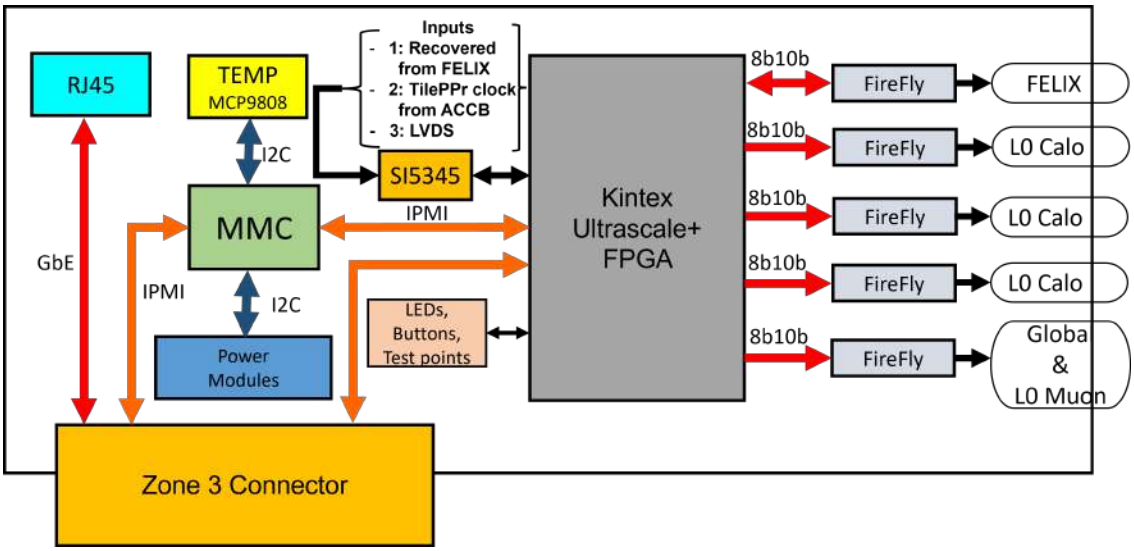


FIGURE 3.21: Block diagram of the TDAQi board [57].

LTM4647 [70], LTM4644 [71], and LTM4646 [72], are used. LTM4646 generates 1.2 V and 0.9 V for MGT transmission lines. LTM4644 generates 1.8 V and 3.3 V and MGT transmission lines. Finally, the LTM4647 generates 0.85 V for the ADC voltage levels. The Processing FPGA will periodically check and read the voltage, current, and temperature of power modules, as well as the temperature of the power converters while in use. The LTM2987 [73] is a 16-channel module (micromodule) power system manager used for fault management, telemetry, margin, supervision, fault management, and sequence. The LTM2987 will automatically shut off all voltages in the event of a malfunction or power outage to protect the onboard components. Lastly, USB-JTAG is used for the physical interface with the TDAQi module to program FPGAs with bitstreams. The final design of the off-detector electronics will consist of 32 TDAQi modules with identical hardware designs installed on four ATCA shelves.

Figure 3.21 shows a block diagram of Tile TDAQi with all the main components highlighted. The TDAQi interfaces with the TDAQ system through FireFly optical modules. There are four FireFly transmitters and one bidirectional FireFly Optical Transceiver used for integration. One 12-channel FireFly transmitter is used to interface with eFEX, one 12-channel FireFly transmitter is used to interface with jFEX, one 12-channel FireFly transmitter is used to interface with gFEX, and one 12-channel FireFly transmitter is used to interface with Global & L0Muon. The bidirectional FireFly module is used to interface with FELIX.

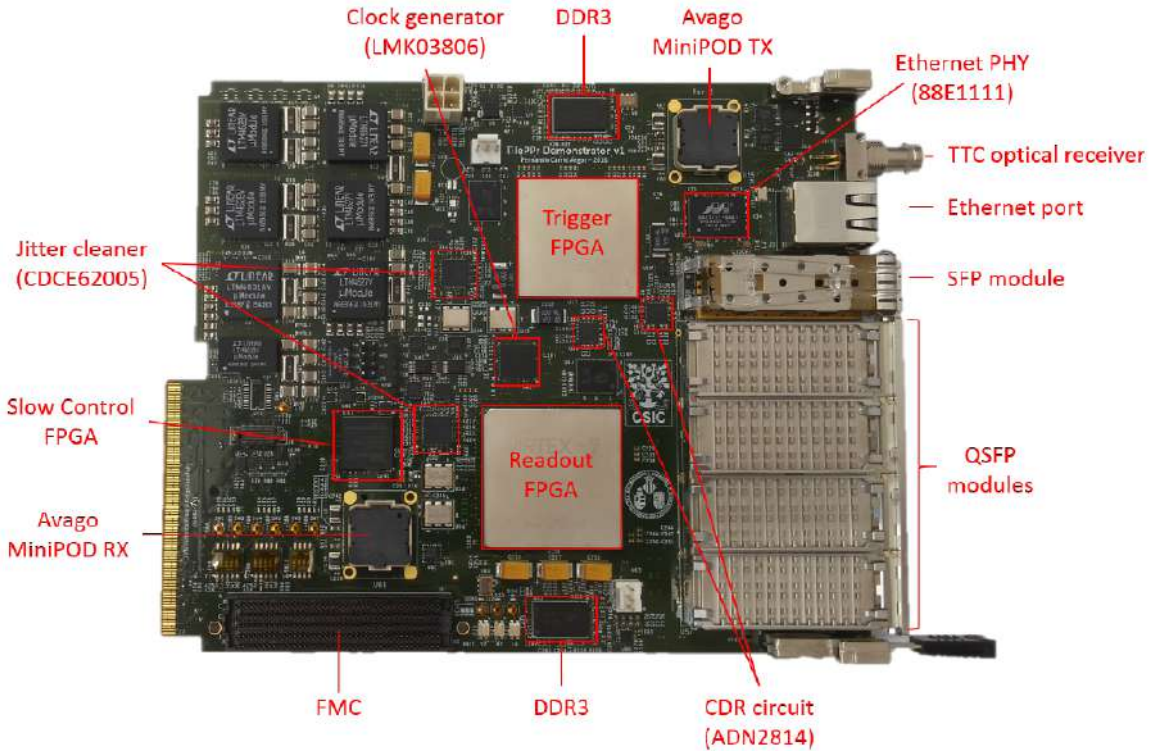


FIGURE 3.22: The TilePPr Demonstrator board [74].

3.2.4 The TilePPr Demonstrator module

Figure 3.22 shows the TilePPr Demonstrator board with labels of the components. The Demonstrator module is controlled and readout by the TilePPr Demonstrator [75], which also propagates the LHC clock in the direction of the on-detector electronics. Additionally, this is a crucial module of the Demonstrator data acquisition system, which serves as a link between the upgrade on-detector electronics and the existing ATLAS TDAQ and Trigger, Timing, and Control (TTC) systems. The TilePPr Demonstrator module is a reduced version of TilePPr and similarly resembles the CPM module of TilePPr. The PCB is made up of 16 layers, eight of which are for the power and ground planes, and the other eight layers are signal layers. The PCB has a total thickness of 1.6 mm which is compliant with the AMC standard. This module is also powered by 12V from the ATCA carrier, which powers all voltage regulators in the module.

Figure 3.23 shows a block diagram of the TilePPr Demonstrator module. A Xilinx Virtex-7 XC7VX415T (Readout FPGA) and a Xilinx Kintex-7 XC7K420T FPGA (Trigger FPGA) are installed on the double mid-size advanced mezzanine card (AMC)

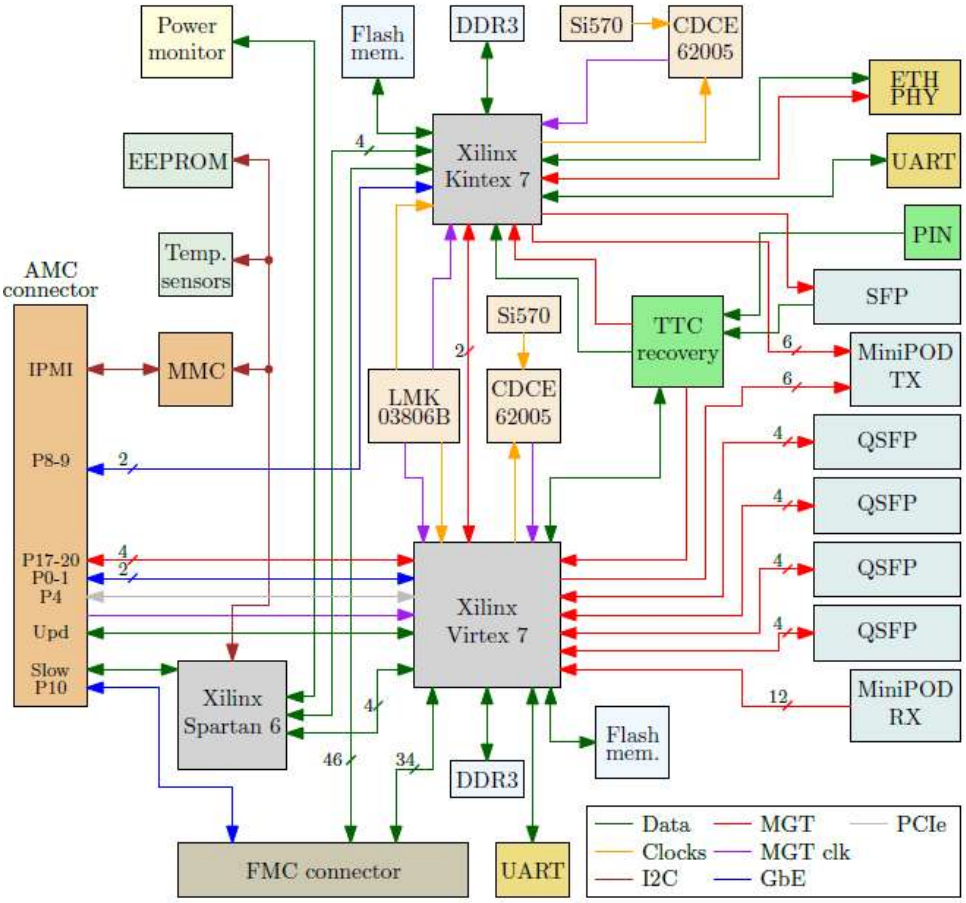


FIGURE 3.23: Block diagram of the TilePPr Demonstrator module [74].

form factor of the TilePPr Demonstrator. Through 16 high-speed lines operating at 4.8 Gbps/9.6 Gbps, the Readout FPGA interfaces with four Quad-SFP (QSFP) modules to provide high-speed communication with the on-detector electronics. Additionally, it interacts with the TTC system to retrieve the LHC clock, as well as the legacy ROD and FELIX systems to transmit the triggered data. On the other hand, the Trigger FPGA is not utilized during the normal functioning of the Demonstrator module and is instead designed for the study of sophisticated pre-processing trigger algorithms for the HL-LHC. To integrate with the on-detector electronics, the TilePPr module consists of four QSFP connectors. The off-detector electronics communicate with the on-detector electronics through the GBT links.

System integration tests have been carried out to fully test the infrastructure and operation of the TilePPr Demonstrator module in terms of power management, clock network, and slow control interface between modules. The design of the TilePPr

demonstrator module and the firmware is a product of the Instituto de Fisica Corpuscular team. However, Chapter 6 presents the control and monitoring of this module.

3.3 Comparison between the proposed and the current system

As introduced at the beginning of this document, the TileCoM and Tile GbE Switch are the main contributions of this document. This sub-section compares the proposed and current systems regarding technologies, advantages, and disadvantages. The control and monitoring methodology comparison of the current and proposed system is also presented. As stated in the objectives, the TileCoM will be used as an interface between the off-detector electronics with DCS and TDAQ systems. Thus, the focus of the comparison is based on the hardware control and monitoring of the readout systems:

3.3.1 Technology

Current system

(a) Software:

The migration of the DCS from Windows to Linux was the primary directive for the ATLAS DCS update for Run 2. The most recent version of PVSS, which was renamed to WinCC Open Architecture (OA) (more on WinCC), and CERN Scientific Linux 6 were installed on the PC hosts. The OPCs DA utilized during Run 1 were replaced by the new OPC Unified Architecture (OPC UA) due to the switch from Windows to Linux.

(b) Hardware:

This system uses PCs that supports general-purpose operating systems. Thus, a numerous applications can be installed on the PC, such as a Graphical User Interface (GUI).

Proposed system

(a) Software:

The proposed system offers a SoC-based operating system to implement the DCS monitoring software. CentOS Linux system is implemented on the TileCoM, and the OPC Unified Architecture (OPC UA) will be used as the DCS software monitoring system. DCS will communicate with the electronic chain system through this software implemented on the TileCoM.

(b) Hardware:

The TileCoM is a mezzanine board with limited hardware resources compared to a regular PC. Thus, applications designed to be installed on the TileCoM will require some optimization to achieve the desired performance.

3.3.2 TDAQ and DCS path for the readout electronics

Current system

The main objective of this thesis is control and monitoring of the readout system and the configuration of FPGAs on the readout system. Currently, the front-end and back-end electronics are monitored by DCS, and the electronics configuration via TDAQ is performed through a different path. The TileCal DCS hierarchy for the current system monitors the long and extended barrels directly. The back-end electronics are also monitored separately by the DCS system.

Proposed system

The primary distinction between the current and proposed systems is the reliance of the TDAQ and DCS routes on the TileCoM for the readout electronics. The configuration performed via TDAQ, and the control and monitoring of the readout system will be performed through the TileCoM. Thus, the same methodology in the current system of the OPC UA server will be implemented on the TileCoM to control and monitor the readout system.

3.3.3 Advantages and disadvantages

Current system

The current system DCS monitoring system and configuration paths are separate. The current DCS monitoring system is directed to specific sections of the electronics system, which is tedious for maintenance purposes and adding new functionalities. A separate OPC UA server is implemented for on-detector barrels which is a completely different server for the readout system.

Proposed system

The proposed system readouts both the on- and off-detector electronics using one server implemented on the TileCoM. It is easy to do maintenance and updates on a single server that accommodates the entire electronic system. The TileCoM and the Tile GbE Switch are small mezzanine boards that are easy to debug in case of faults and malfunctions.

Chapter 4

Design of the TileCoM and GbE Switch Prototype

As stated in Chapter 3, TilePPr is the main module of off-detector electronics. This TilePPr includes different modules to readout and process data from on-detector electronics. Some of these modules include the TileCoM and GbE Switch, which will be connected to the ATCA carrier through the SODIMM connector. The main functionalities of TileCoM are described in Chapter 5.

The TileCoM is an entry-point computer to remotely access the entire TileCal readout electronic system. This board is connected to other TilePPr modules, such as the CPM, TileCal GbE Switch, and IPMC modules. All of these modules are powered and connected to the ATCA carrier.

This chapter presents the design of TileCoM and the Tile GbE Switch in terms of specification requirements, component selection, and PCB layout design. For the TileCoM and GbE Switch, a small testbench will be used to test before insertion into the TileCal Phase-II Upgrade electronic chain.

4.1 TileCoM and Tile GbE Switch design

4.1.1 TileCoM design

The main components of the board are the Zynq UltraScale+ ZU2CG [76], the power supply, two Quad Serial Peripheral Interfaces (QSPI), GbE PHY, and Double Data

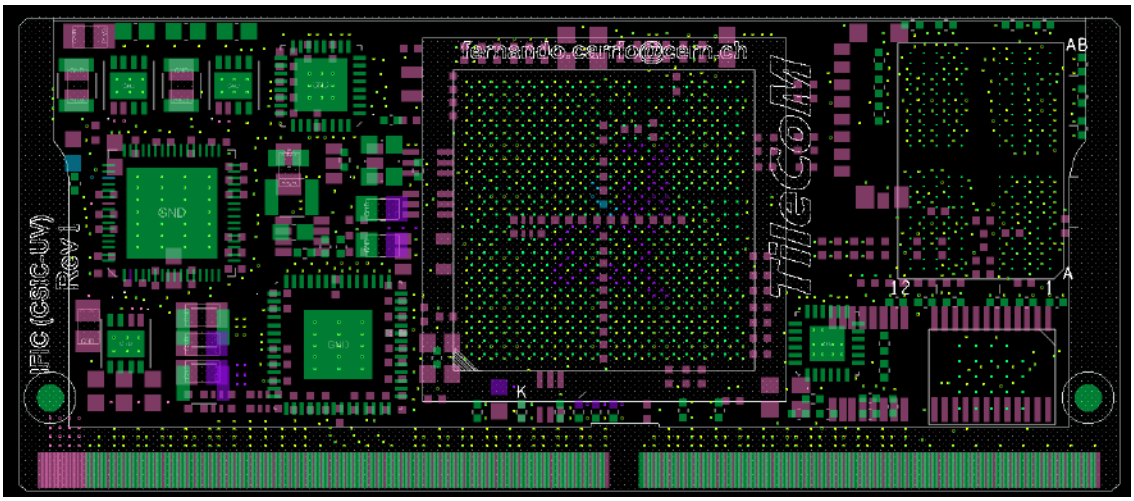


FIGURE 4.1: The TileCoM component layout.

Rate (DDR) memory. The external interfaces are the 72 General Purpose Input Output (GPIO) ports, the Serial Peripheral Interface (SPI), and I^2C. The Zynq UltraScale+ ZU2CG interfaces with GbE PHY [77] through the Reduced Gigabit Media-Independent Interface (RGMII) [78] protocol. The software developments discussed in Chapter 5 communicate through the GbE port from TileCoM to TilePPr modules. The GbE and I^2C protocols interface with the Tile GbE Switch card and the ATCA carrier, respectively. The Transmission Control Protocol and the Internet Protocol (TCP/IP) are used to access the TileCoM remotely. The remote programming functionality, as described in Chapters 5 and 6, uses the GPIO ports. The Universal Asynchronous Receiver/Transmitter (UART) is used for the terminal display of the embedded Linux.

Figure 4.2 shows a sketch of the TileCoM stack-up with 10 layers. Several iterations were performed during the routing and placement of the components to meet the minimum number of layers. The spacing of the components and the signal routes was also considered to meet the requirements of high-speed design. Thus, no congestion of components is seen in the design. The following points discuss the TileCoM stack-up layers:

- Layers 1 and 10 are the top and bottom conductors with a thickness of 35 μm.
- Layers 2 and 9 are used as ground planes with a thickness of 17 μm.

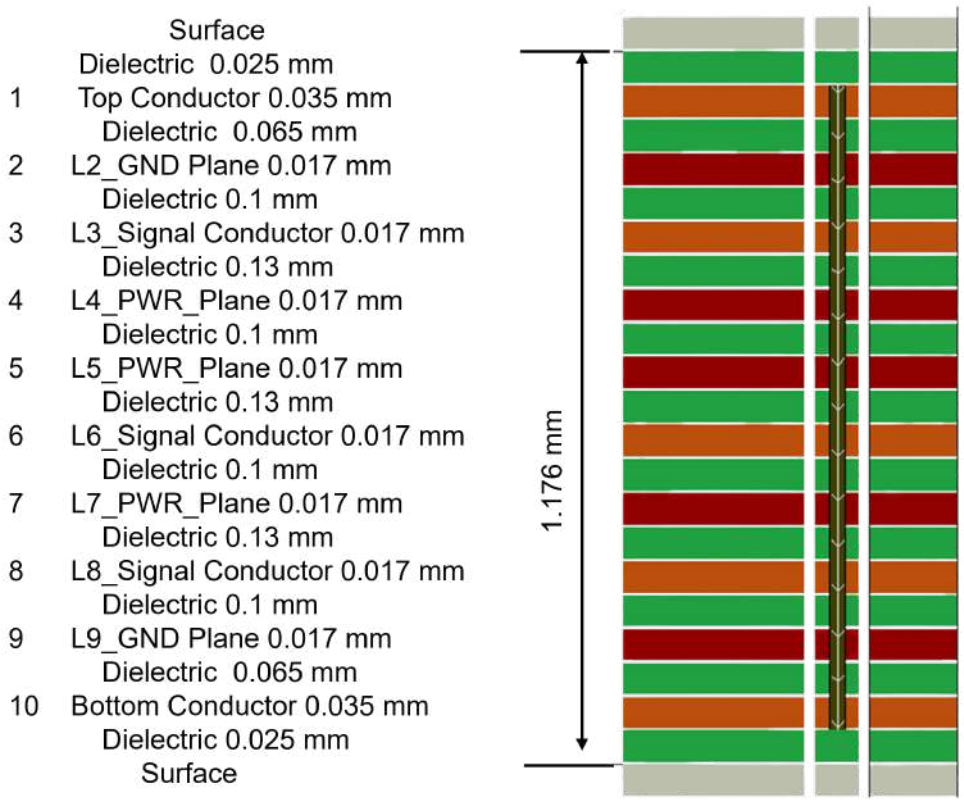


FIGURE 4.2: Sketch of the PCB 10 layers TileCoM stack-up.

- Layers 3, 6, and 8 are signal conductors used to transmit and receive signals amongst components such as the Zynq UltraScale FPGA, DDR4, etc., with a thickness of 17 μm.
- Layers 4, 5, and 7 are power plane layers for all the different power levels on the board from the input 12V down to all the voltage regulations with a thickness of 17 μm.

4.1.2 TileCoM components and their functionalities

The TileCoM prototype is designed to fulfill all the functional requirements described in Chapter 5. All components are selected according to the hardware specifications for the off-detector electronics and the overall ATLAS Trigger and DAQ systems for the HL-LHC. Some of these requirements are compliance with the ATCA

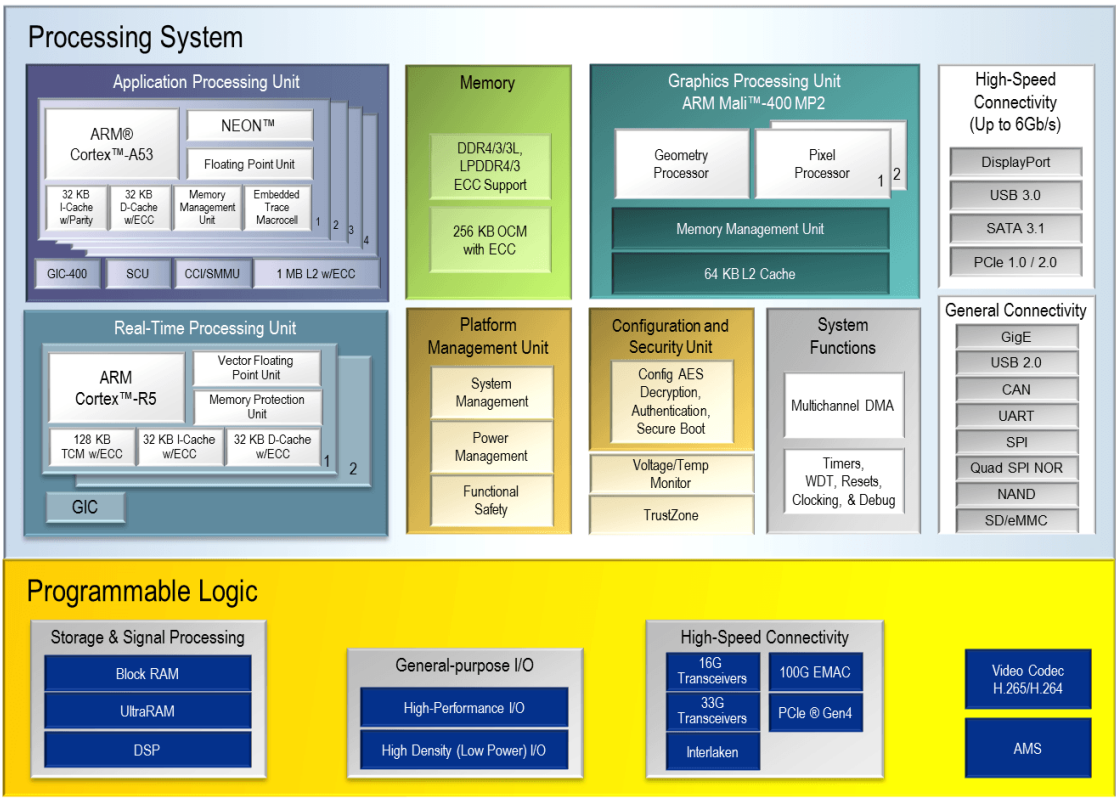


FIGURE 4.3: The Zynq UltraScale+ ZU2CG PS and PL architecture [79].

standards, remote programming of the on- and off-detector electronics, and providing monitoring data to DCS. Each component used in the TileCoM design is aligned with the requirements mentioned above.

The following Subsections represent a detailed explanation of every component used on TileCoM. This section presents the major components, such as the SoC FPGA, a memory component, a clocking unit, power modules, and connectors, such as the QSPI and SODIMM connectors. All of these modules are connected to the main component of the PCB, the SoC FPGA. Different communication protocols and interfaces are also discussed in the subsections on how data is transmitted through signals of the PCB. Protocols such as the GbE, I^2C protocols, SGMII, and the RGMII are discussed.

Field Programmable Gate Array

Figure 4.3 shows the architecture of the Xilinx Zynq UltraScale+ ZU2CG[1], which is the core of the TileCoM. The Zynq UltraScale+ ZU2CG is divided into two sections, the Processing System (PS) and the Programmable Logic (PL). The PS comprises the Application Processing Unit (APU), the Real-Time Processing Unit (RPU), the internal memory, the Graphic Processing Unit (GPU), the high-speed interface connectors, the platform management unit, the configuration and security unit, the system functions, and general interface connectors. Each of these components has internal blocks that contribute to the functionality of the Zynq UltraScale+ ZU2CG. This includes major components such as a dual core ARM Cortex-R5F-based Real-Time Processing Unit (RPU), on-chip memory, ARM Mali-400-based GPU, and interconnects with external components. Zynq UltraScale+ ZU2CG can implement high-performance applications from a single platform. The main functionalities of TileCoM are implemented in PS and PL to interact with hardware and the rest of the ATLAS TileCal Phase-II Upgrade electronic readout system. Among all these mentioned components of the Zynq UltraScale+ ZU2CG, the APU and the RPU are used primarily to implement the software functionalities of TileCoM. These software implementations interface with the memory and high-speed and general connectivity, as explained in Chapter 5.

The PL implements the firmware necessary to interface directly with the hardware. This consists of the storage and signal processor, GPIO and high-speed connectors, and Video Codec and AMS. The storage and signal processor consists of Random Access Memory Blocks (RAM), Ultra RAM, and Digital Signal Processing (DSP) [81] blocks. Some of these components are used for the firmware implementation of TileCoM functionalities. For example, the PL GPIOs and the block RAM are used for the firmware implementation of remote programming. This includes using the GPIOs as JTAG ports to send JTAG signals to program FPGAs remotely on the ATLAS TileCal electronic chain.

[1]The Xilinx Zynq UltraScale+ MPSoC FPGA used on the TileCoM [80]

TABLE 4.1: The Zynq UltraScale+ ZU2CG resource table.

Zynq UltraScale+ ZU2CG	Device Name	Type/Amount
PS	APU Processor Core	Cortex-A53 e
	RPU Processor Core	Cortex-R5 MPCore
	Memory	LPDDR4 and 2x Quad-SPI
PL	System Logic Cells	103,000
	CLB Flip-Flops	94,000
	CLB LUTs	47,000
	Block RAM	5.3 Mb
	Clock Management Tiles	3

Clocking unit

The selected clocking units are in parallel with the TilePPr cloking unit to meet the requirements mentioned in Section 4.1.2. Thus, the transceivers used in this design require a high quality and very low jitter for the clock. The SI5338C, the I^2C-programmable any-frequency, any-output quad clock generator [82] component, is a differential clock generator for the TileCoM. The SI5338 component is used in conjunction with the clock buffer on the TileCoM board. The 854S006AGILF is a Low-Skew, 1-to-6, crystal-to-LVDS Fanout Buffer [83], which is a high-performance differential-to-Low Voltage Differential Signalling (LVDS) fanout buffer with a single input and six repeated output buffers.

Power distribution

As explained in Chapter 3, similarly to all TilePPr modules, TileCoM receives an input voltage from the ATCA carrier. A 12 V voltage is supplied from the ATCA carrier to the power and management modules on the TileCoM board. These TileCoM modules include TPS6508641 which is a configurable multirail PMU for Xilinx MPSoCs and FPGAs [84], LTC2954-1 which is a pushbutton On/Off controller with μP Interrupt [85], and lastly the CSD87331Q3D, which is a 30-V, N channel synchronous buck NexFET™ power MOSFET [86]. Each of these modules works together to supply and manage the power consumption of the TileCoM board.

Therefore, it is necessary to use a voltage regulator to supply the accurate voltage level for all components of the TileCoM board. The TPS6508641 is a voltage regulator for Xilinx® MPSoCs and FPGAs that takes the 12 V input voltage from the ATCA carrier and reduces it to 1.2 V, 1.8 V, 3.3 V, and 5.0 V, respectively. This is used to

supply both the PS and the PL blocks of the Zynq UltraScale+ ZU2CG. All Zynq voltages are supplied from TileCoM power modules.

Step-down voltages, such as 1.8 V, are used to supply the GPIOs, 3.3 V supplies the LTC2954-1 power module, and 5 V is used to supply the USB port. The CSD87331-Q3D power block features high-current, high-efficiency, and high-frequency capabilities using MOSFETS. This is designed specifically for synchronous buck applications.

Memory

As explained in Section 4.1.2, the PS of the TileCoM FPGA consists of internal memory. The TileCoM uses a DDR4 as an external memory for the board. The MT53D512-M32D2DS053 AIT:D[2] from Micron Technology Inc. has been used to perform TileCoM memory operation. This memory provides 2GB (512Mbit x 32) of 533MHz (1066Mbps) LPDDR4 memory. This is sufficient for the applications developed in Chapter 4 for all the main functionalities of TileCoM.

Operating System

The selected OS for TileCoM is CentOS 7. CentOS files, as used in [88] were used for TileCoM OS. These include the boot and root files generated for CentOS 7. A micro-SD card connector is part of the TileCoM PCB components to insert the SD card with a push-push style socket. The generated CentOS 7 files are loaded and mounted on the SD card. When TileCoM is turned on, the embedded Linux OS boots from the SD card. The architecture of this Linux is fully explained in Chapter 4, including a procedure on how the files were generated and mounted on the SD card.

Interconnects

Different interconnects are used in the TileCoM design using different protocols. The TileCoM PCB uses the SODIMM connector to connect to the ATCA carrier board. This connector is used for several connections, including power, ground, and signal. For example, a 12V power supply from the ATCA carrier is received through

[2]SDRAM - Mobile LPDDR4 Memory IC 16Gbit 1.866 GHz [87]

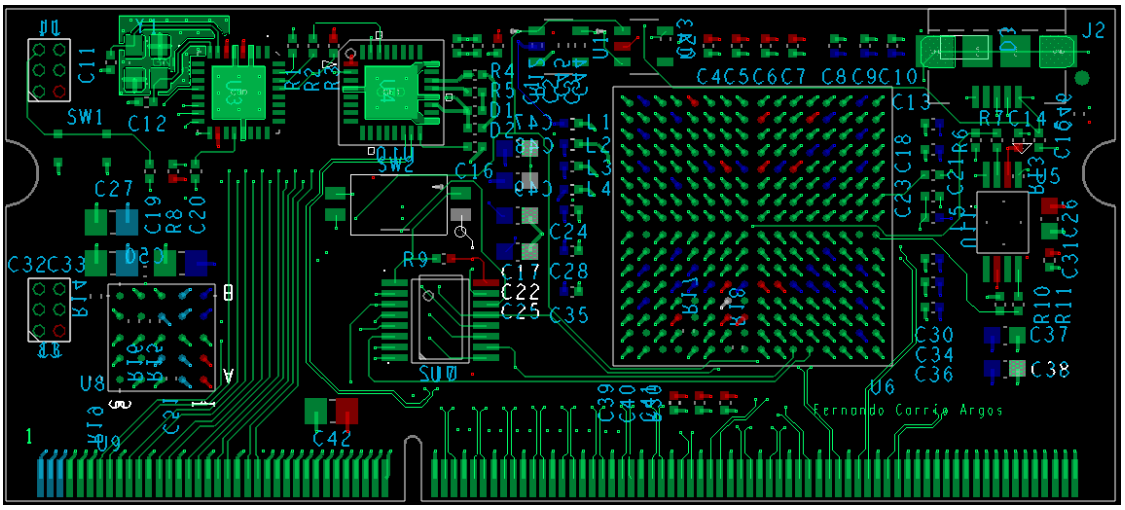


FIGURE 4.4: Tile GbE Switch component layout.

SODIMM connector to TileCoM. The GbE PHY connection to TilePPr modules is through this connector to access TilePPr modules remotely, as explained in Chapter 4.

Several GPIO ports (for PS and PL of the TileCoM) are used to access the TilePPr modules through the SODIMM connector. Some of these ports will be used as JTAG signals to remotely program the on- and off-detector FPGAs. Protocols such as I^2C will be used to control and monitor the ATCA board.

4.1.3 Tile GbE design

As is shown in Figure 4.4, the placement of the components is not congested, and this was achieved due to several iterations of the placement and routing of the components. Figure 4.5 shows the stack-up for the Tile GbE card. This card consists of a total of 6 layers for power rails and signal routing. This card was designed to meet the GbE speed design requirements. The following is a description of the six layers of the Tile GbE card and their functionalities towards the main design of the card:

- Layers 1 and 6 are the top and bottom conductors with a width of 18 μm.
- Layer 2 is the VCC power plane conductor with a width of 18 μm.
- Layers 3 and 5 are the ground power plane conductors with a width of 18 μm.

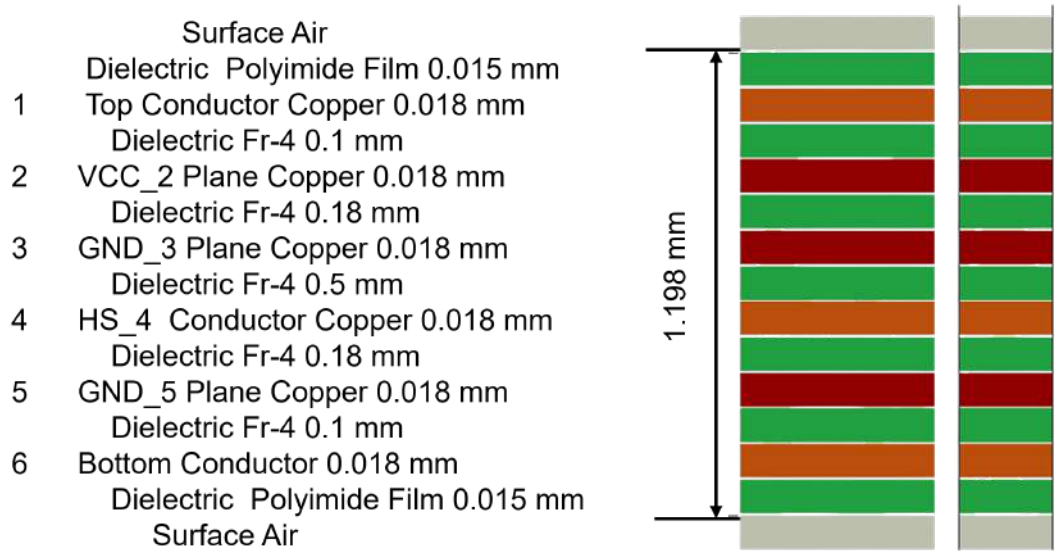


FIGURE 4.5: The Tile GbE Switch second prototype board.

4.1.4 Tile GbE Switch components and their functionalities

GbE module

The Broadcom BCM5396 chip[3] is the core of the Tile GbE Switch. The speed of this chip is in the range of 10/100/1000 Mbps for a 16-port switch via 1.25G SerDes/SGMII/fiber. These SGMIIs ensure superior Electromagnetic Interference (EMI) performance and the lowest board layers while maintaining connections to TilePPr modules. The Broadcom BCM5396 also supports integration with 4K MAC addresses and EEPROM for low-cost chip configuration. This chip has high system reliability and can reduce noise due to the elimination of components.

Configuration units

As explained above in Section 4.1.4, the BCM5396KFBG chip is the core component of the Tile GbE Switch. This chip is used together with several components for the board's functionality. ATMEGA168A[4] is a low-power 8-bit microcontroller that will possibly be used in the future to configure and manage the GbE Switch.

[3]Single-Chip 16-Port SerDes Gigabit Switch [89]
[4]The high-performance Microchip 8-bit AVR® RISC-based microcontroller [90]

Thus, if this component is used to manage the GbE Switch, the configuration files will be transmitted to the ATMEGA168A microcontroller via SN74CB3T325. The SN74CB3T3257 is a 4-BIT 1-OF-2 FET multiplexer/demultiplexer [91] and CAT93C86VI-GT3 is a 128 kb I^2C CMOS serial EEPROM [92]. The SN74CB3T3257 is a 4-bit multiplexer/demultiplexer with a single enable input and select inputs. The enable input is used to determine the direction/operation and the select inputs are used to control the data path. The CAT93C86VI-GT3 is an EEPROM to store these configuration files.

Power module

Similarly to TileCoM components, the Tile GbE Switch uses the SODIMM connector to connect to the ATCA carrier. This board is also powered with a 12V from the ATCA carrier and supplies the rest of the components with the appropriate voltage levels. A DC-DC voltage regulator, LTM4622IVis a step-down DC/DC µModule regulator [93] that is used to supply 1.2V to the board components.

4.2 Conclusion

This chapter presents the designs and PCB layout of the TileCoM and the Tile GbE Switch. A discussion of components for each module is first introduced in the early sections of this chapter regarding placement on the board and their functionalities. As discussed, the main component of TileCoM is the Zynq UltraScale FPGA, and the main component of Tile GbE Switch is the GbE module.

Chapter 5

Firmware and Software architecture on the TileCoM

The main goal of this chapter is to present the firmware and software design as well as their implementations on the TileCoM. These implementations are the main functionalities of TileCoM for the ATLAS Tile Calorimeter Phase-II Upgrade system. All the functionalities discussed in this chapter are designed and implemented in relation to the designs discussed in Chapter 4.

These designs also meet the requirements and specifications of the ATLAS TileCal Phase-II Upgrades. Some of these requirements are to implement three main functionalities of TileCoM introduced in Section 5.1. The firmware and software tools used to implement these functionalities are also explained in Section 5.1. All these functionalities are implemented using a testbench that includes the Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board, the Tile GbE Switch connected to the motherboard, and a 12 V power source. A detailed description of this testbench is discussed in Chapter 6.

Section 5.1 gives an introduction about the software tools used to implement TileCoM main functionalities. Section 5.2 presents an introduction of the DCS that is used for the control and monitoring of the ATLAS TileCal Phase-II electronic system. Section 5.3.1 and 5.3.2 presents the deployment of the embedded Linux. Section 5.3.3 and 5.3.4 presents the firmware and software implementation of the remote programming functionality. Section 5.3.5 and 5.3.6 presents the TileCoM and the TDAQ system communication. Lastly, Section 5.3.7 and 5.3.8 explains the TileCoM and DCS system interface.

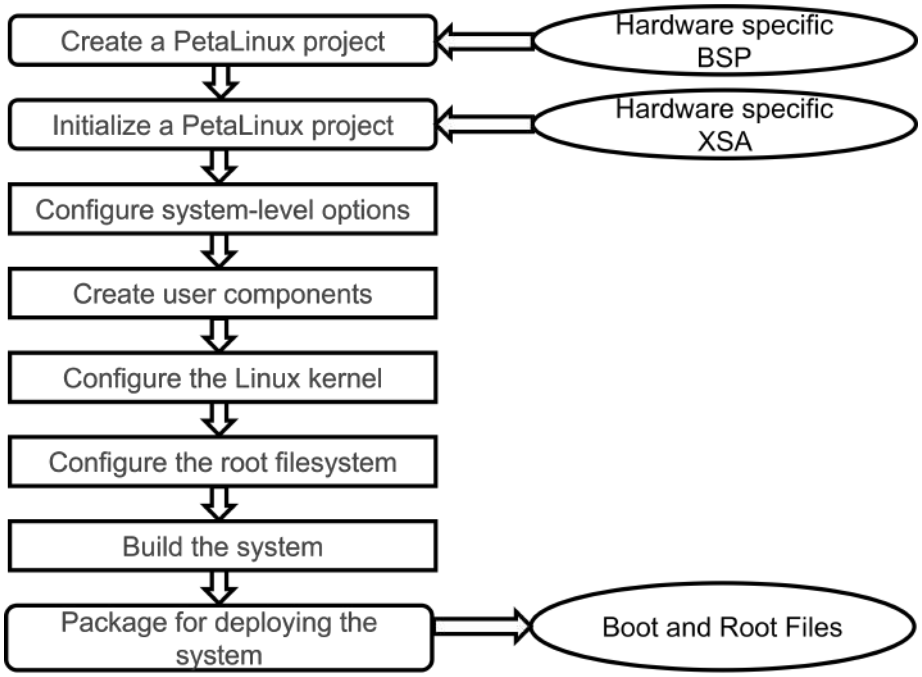


FIGURE 5.1: Overview design flow for a PetaLinux project [95].

5.1 Introduction

Section 5.3 presents a detailed description of the three main functionalities of TileCoM. The first functionality of the TileCom includes remote configuration of on-detector electronics and TilePPr FPGAs. This involves sending configuration bit-streams remotely to on- and off-detector FPGAs. The second functionality involves the interface of TilePPr with the ATLAS TDAQ system. This involves the use of Ironman software [94] with the IPbus protocol for communication purposes. The third and last functionality involves interfacing TilePPr with the ATLAS DCS by providing monitoring data. This involves implementing a DCS server on TileCoM to send monitoring data to the DCS. The following sections introduce the software tools used to implement the TileCoM functionalities:

5.1.1 PetaLinux tool-chain design flow

The PetaLinux tool-chain provides the necessary tools to customize, build and deploy Embedded Linux solutions for Xilinx MPSoCs [95]. PetaLinux tool-chain is

used in this thesis to generate boot files for the CentOS 7 embedded Linux. PetaLinux tools consist of a number of software packages for ease of development. Packages such as command-line interfaces, applications, device drivers, development templates, bootable systems, image builder, debug agents, GCC tools, etc.. Developers can modify the Linux kernel, bootloader, and applications using these tools. On a high level, the PetaLinux tool contains Yocto Extensible Software Development Kit (SDK), XSCT (Xilinx Software Command-Line Tool), and PetaLinux Command-Line Interface (CLI) tools. The PetaLinux CLI tools were used in the generation of boot files for the Operating Systems (OS) implemented on the TileCoM.

Figure 5.1 shows an overview of the design flow for a PetaLinux project. This design flow includes the steps followed in generating boot files. The first two steps include creating and initializing the PetaLinux project. An Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board support package (BSP) file was used to create a PetaLinux project. A software suite called Xilinx Vivado design suite is used in conjunction with PetaLinux tool-chain. Vivado design suite is a software suite that is used for the synthesis of Hardware Description Language (HDL) designs, implementation, and generation of bitstreams for target FPGAs. Synthesis converts HDL files into a transistor-level description on the basis of timing and I/O constraints. The Implementation step optimizes, place, and route the design to fit the target FPGA. Lastly, the bitstream required for programming the FPGA is produced by the Bitstream Generator. In this thesis, A hardware description file (.xsa) generated from Vivado version (2021.1) is imported into the PetaLinux project to initialize and configure the project specifically for the evaluation board. These files are used with the PetaLinux tool-chain command to enable the design and configure the kernel. Running the command with the HDF file generates a window to configure kernel boot arguments and generate boot arguments automatically. The window is also used to set the kernel boot arguments. Finally, the project is built, and the boot and root files are generated.

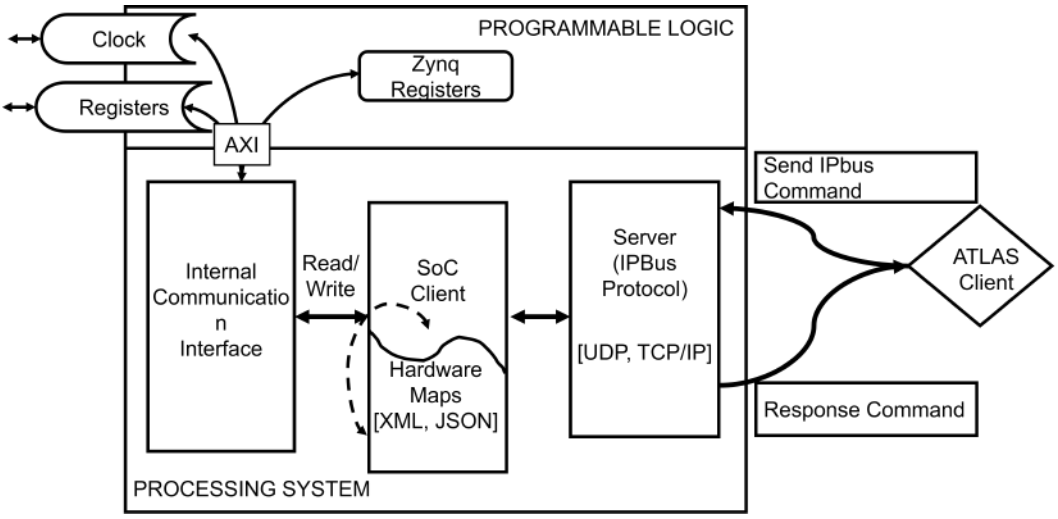


FIGURE 5.2: The Ironman software block diagram [94].

5.1.2 Ironman software

This Section introduces the software used to implement the TilePPr and TDAQ interface functionality as detailed in Section 5.3.5. The IPbus protocol [96] is a packet-based control protocol that is used to communicate with FPGA-based devices to read and modify memory-mapped resources. The implementation of control software to interface with the CPM firmware uses TCP/IP. Figure 5.2 shows the architecture of Ironman software [94]. Ironman is a Python framework that implements a single-threaded, reactor-based, event-driven callback for server and client communication. It enables the ATLAS client to communicate with the TileCal Phase-II Upgrade readout electronic chain. This framework is used to standardize communication protocols on embedded processors. As this framework is developed to allow for a wide array of standard networking protocols, this implementation focuses only on the IPbus protocol for communication purposes.

The framework is divided mainly into three software blocks on the PS and three firmware blocks on the PL of the TileCoM. The three software blocks on the PS are the server, the SoC client, and the internal communication interface. The other blocks on the PL simply establish hardware interfaces with other hardware through the clock, IPbus registers, and SoC registers. The interface between PS and PL of the ZYNQ UltraScale+ FPGA is through the Advanced eXtensible Interface (AXI) [97]. However, for this functionality, only PS blocks are implemented. The internal communication interface software block is used to interface with the hardware. This

block of Ironman software is hardware dependent. The custom code for this block is written to read and write to specific registers.

The SoC client is an interface between the server and the internal communication block. All packets received and forwarded by the server are analyzed by the SoC client. Incoming data from the server is analyzed by checking whether the packet has a valid address, valid permissions, and valid data. If all these checks are good, then the packet is forwarded to Internal Communications to build up the response. In the Python script, this is achieved by the Jarvis [98] module to handle the hardware manager.

The server block establishes the main communication between TileCoM and the ATLAS client user. The software uses applications of the standard Twisted protocol [99], such as a reactor model, which is a global loop that responds to listeners when events have been triggered in the server. This software is implemented in such a way that the server is actively communicating with both the ATLAS client and the SoC client through the reactor module. Modules such as serverfactory, IPBusPacket, history, reactor, and deferred are imported in the Python implementation of Ironman software. These IPBusPackets are used when packets of data are received, and the deferred is used for callback chains. Upon the arrival of data, sanity checks are performed and saved to the history if no request is sent to the SoC client. The history module stores data for a period of time for future data requests. The serverfactory module enables the implementation of the Twisted Internet through TCP to establish a remote connection.

The ATLAS client performs a transaction request or a status query by sending and receiving the IPbus command. The IPbus commands are sent to the hardware running the Ironman software, where the server is actively listening and sends this request to the SoC client. In this thesis, TileCoM runs Ironman software and the server continually waits for IPbus request commands. TileCoM responds to the ATLAS client by sending the IPbus response command. The server reactor, as explained in Section 5.1.2, continuously listens and communicates with the CPM through GbE. Ironman implemented on TileCoM uses the register address table to transmit and receive packets of data.

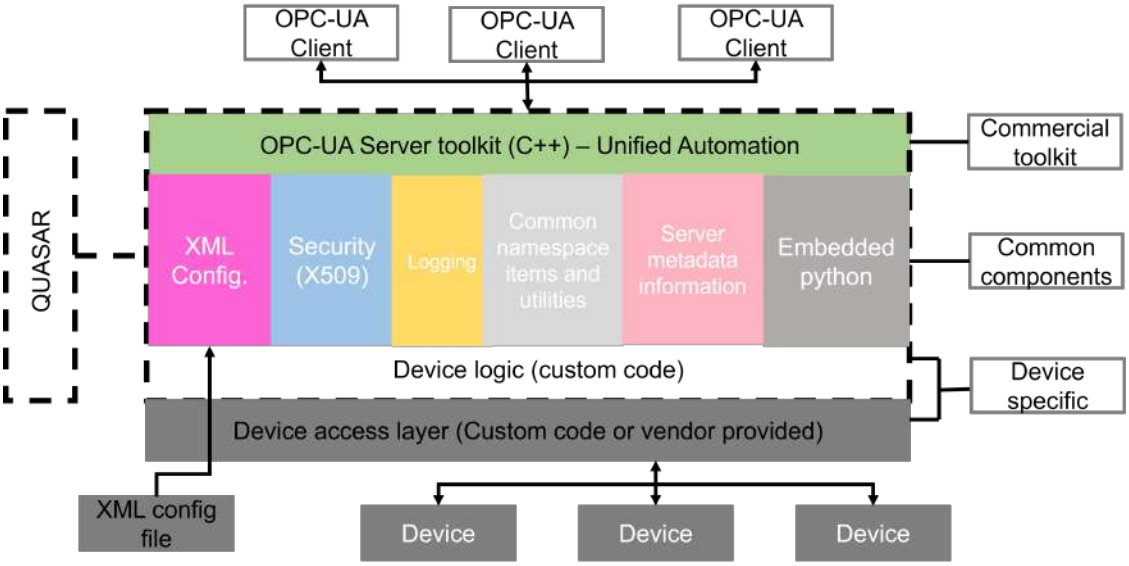


FIGURE 5.3: Block diagram of the Quasar components [100].

5.1.3 Quasar framework

The Quick Open Platform Communications Unified Architecture (OPC UA) server generation framework (Quasar) [100] framework is used to implement a server on the TileCoM to read out DCS monitoring data. This is the TilePPr and DCS interface functionality as explained in Section 5.3.7. Quasar is divided into three main components as shown in Figure 5.3. The first layer involves the hardware access layer. This layer is hardware-dependent, and Linux Industrial Input Output (IIO) is used in this thesis to access TileCoM hardware. The second layer involves the common Quasar components such as the device logic, Extensible Markup Language (XML) configuration, server metadata information, etc.. The device logic is the custom C++ code implemented in the framework to interface with the hardware access layer. For this functionality, the memory map is used to map the sensor address of the Xilinx ADC. This layer communicates with the XML design file to form a tree structure of the sensors included in the design. Authentication to the server is handled by security (X509 certificate handling) in parallel with the logging component of the Quasar. All these are major components for transferring data from the server to the DCS.

Quasar design can be developed in two ways, using C++ or Python. In this thesis, a C++ Quasar is used to implement the server on the TileCoM. The Quasar

framework adheres to all the Object Oriented Programming model (OOP) to organize software design around data and objects. All OOP concepts, such as encapsulation, polymorphism, and data abstraction, are used in the design to organize the code. Quasar produces a variety of unique components based on the server design. These elements include the creation of C++ classes for address space, the creation of XML Schema Definition (XSD) configuration schema for the information model, the creation of the configuration loader, the logic transformation of the devices and the transformation of the code for Supervisory Control and Data Acquisition (SCADA) [101] integration. To receive call service request of data from the DCS client to the server, OPC UA methods are used as nodes in the address-space to send the requested data. To be able to send these requested data to the DCS client, a configuration file is used to declare all the sensors using the XML file. This configuration file is used to exchange data between the server and the DCS client. Thus, if the design is validated without any errors, the build is configured and the server is finally compiled.

The third layer of the Quasar framework includes the OPC-UA server toolkit. This layer is used to enable communication between the server and the OPC-UA client applications. Some client applications are available to test the publication of data acquired by the OpcUAXADC server, such as SCADA. The Quasar framework is flexible to work with a number of libraries and also interconnects with other frameworks. The open62541 [102] is a free and open-source implementation library of OPC UA. UA SDK is a commercially available licensed library that can be used to build the Quasar framework modules. For this design, open62541 is used to enable the Quasar framework together with its adapter.

5.2 Detector Control System

This section introduce the DCS system used to control and monitor the TileCal Phase-II upgrade electronic system. The TileCal DCS is primarily responsible for controlling and monitoring high- and low-voltage systems. It is also responsible for safety, calibration systems, data acquisition, and detector infrastructure (cooling and racks).

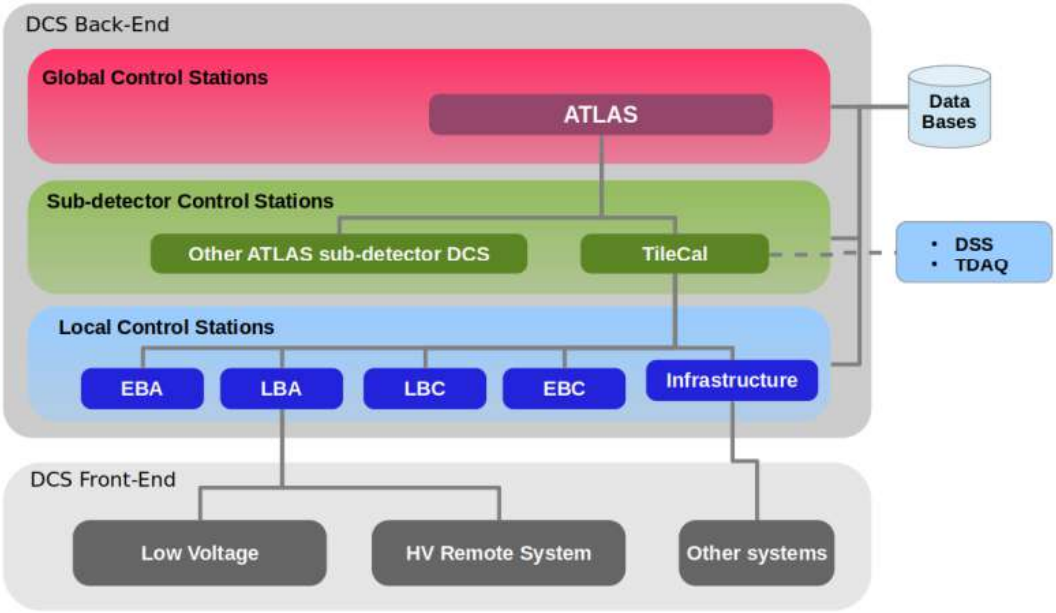


FIGURE 5.4: TileCal DCS hierarchy for Run 2 [103].

This has been successful for both Run 1 and Run 2 in terms of control and monitoring of the ATLAS detector. Figure 5.4 shows the TileCal DCS hierarchy for Run 2 in terms of the front- and back-end. The DCS front-end includes monitoring of the fLVPS and the HV distribution. Embedded Local Monitoring Boards (ELMB) [104] are responsible for the monitoring of fLVPS, which mainly uses an OPC Data Access (OPC DA). The Zybo SoC board, as part of the HV remote, connects to the DCS through the HV Remote SPI bus control and its dedicated HV supply boards [105]. To check the temperature of the board and evaluate the cooling conditions, temperature probes are used as part of the HV boards. The software running on the SoC is written in Python, implementing the required SPI instructions to operate the control chips on each board. The DCS and the controller communicate via a TCP/IP protocol, allowing the DCS to send commands or inquiries to the controller with a response from the controller.

The DCS back-end includes three layers: the Global Control Station (GSS), the Subdetector Control Station (SCS), and the Local Control Station (LCS). This hierarchy enables the experiment to be partitioned into distinct segments that can function independently or as a unit. The GSS offers high-level oversight and management of all sub-detectors, with lower levels taking care of data processing and command execution. TileCal is part of the SCS in connection with the TDAQ system and the

TABLE 5.1: Comparison of embedded Linux with general-purpose Linux.

Linux layer	Personal Computer Linux	Embedded Linux
Bootloader	BIOS	U-Boot
Kernel	CPU Architecture	PS
Root file system	Hard drive	SD card
Services	Numerous services	Limited resource
Applications	General purpose	Specific purpose

Detector Safety System (DSS) to ensure that the collection of physics data and detector operation is coordinated. The TileCal LCS manages the LV and HV systems of the sub-low detector level monitoring and control. To supervise and interact with the crates and boards, as well as to include the HV system in the DCS, a SCADA is used. When the observed values are out of range, the control system will be able to alert the operators, archive the monitored data, and take automated action if necessary. The designs and developments presented in this thesis focus solely on the ATLAS TileCal DCS.

As stated in the previous chapters, TileCoM is the entry point for controlling and monitoring the entire ATLAS TileCal Phase-II Upgrade electronic chain. The design specifications of the TileCoM and Tile GbE Switch presented in Chapter 4 adhere to the specifications and requirements of the TileCal DCS [106]. Some of these requirements are communication protocols, the type of server that can be used to control and monitor, or the type of data that can be transmitted between the TileCoM and the DCS. For example, DCS Run 1 used Object Linking and Embedding (OLE) for Process Control Data Access (OPC DA) to perform remote control and monitoring. This is replaced by the OPC-UA in Run 2. The designs in this thesis focus on the OPC UA to monitor the ATLAS TileCal Phase-II Upgrade electronic chain as discussed in Section 5.3.8.

5.3 Developments of TileCoM functionalities

5.3.1 Objective of the embedded Linux deployment

All firmware and software implementations on TileCoM for the required functionalities are developed on the recommended Operating System (OS). The CERN Computing Security rules clearly state that all computing devices in the technical network must be centrally managed, as detailed in the ATLAS System-on-Chip (SoC) requirements specification document [62]. According to the ATLAS SoC requirements, the CentOS and PetaLinux tool-chain are the two preferred Linux-based OS for the implementation of embedded solutions for the ATLAS Phase-II Upgrade.

Table 5.1 compares a general-purpose Linux on a PC and an embedded Linux. TileCoM is an SoC-embedded system that is used specifically for three main functionalities. These functionalities are implemented in the application layer of embedded Linux. A general-purpose computer uses a Basic Input/Output System (BIOS) to boot the OS immediately after the computer is turned on. However, TileCoM uses the boot loader (U-Boot) for the initial setup. This enables the binary program of the operating system to be loaded into the memory and run the operating system. All the embedded Linux stack uses similar files to boot and run the operating system. Figure 5.6 shows a block diagram used to deploy embedded Linux on TileCoM. All layers and files were generated specifically for the TileCoM. Each stack layer is used for a specific purpose in the overall functionality of the OS.

The CentOS embedded layers on the TileCoM

The selected OS for TileCoM is CentOS 7 as used in [88]. These files were loaded onto the SD card to boot the embedded Linux. The three main parts of CentOS 7 implemented on TileCoM are detailed below.

- Linux applications in the user space: This is the user interface that allows users to develop software and firmware applications. The XVC [108] server, IPbus, and OPC server are implemented in the user space.

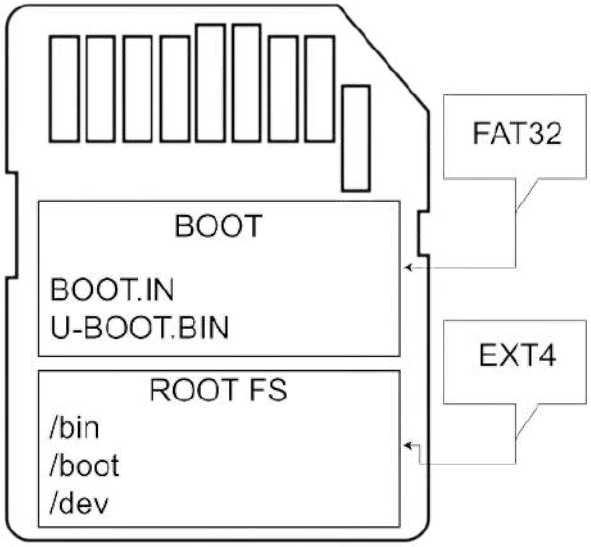


FIGURE 5.5: FAT32 and EXT4 SD card partition [107].

- Kernel version and set of common drivers: The kernel is configured specifically for TileCoM using the specific board support package from Xilinx. Configurations, such as setting kernel bootargs and user-space I/O drivers, are generated for CentOS 7.

- System tools and libraries: The user-space I/O drivers generated during kernel configuration enable communication between the TileCoM I/O and the embedded Linux. Libraries such as IIO are used for the monitoring functionality implemented in Section 5.3.8 to read from ADC sensors.

Figure 5.6 shows the architecture of the embedded Linux implemented in TileCoM. In relation to the three main parts of embedded Linux, as described above, an additional layer is the boot loader. CentOS root files provide network services such as TCP/IP and UDP. TileCoM is configured to use the Dynamic Host Configuration Protocol (DHCP) [109] to acquire an IP address when connected to the network. The boot files were generated using the PetaLinux tool-chain, and the root file system was used from CentOS 7. Section 5.3.2 explains the steps used to generate boot files and install root files.

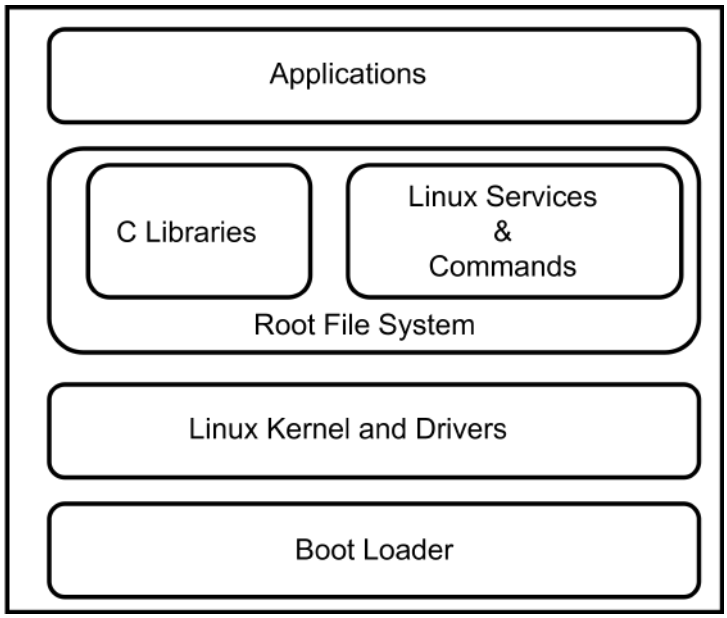


FIGURE 5.6: The embedded Linux architecture [107].

5.3.2 Implementation procedure of embedded Linux deployment

Deployment of embedded Linux procedure involves two steps: generation of the boot files using Petalinux tool-chain and installation of the root file system on the SD card.

Generation of the boot files using Petalinux tool-chain

CentOS 7 OS is used on the host machine to install and create a Petalinux tool-chain project. The design flow for a Petalinux tool-chain introduced in Section 5.1.1 was followed to generate boot files. As explained, a bitstream file is used as part of the PetaLinux tool-chain project. For the TileCoM embedded Linux implementation, a bitstream file includes Vivado IP-blocks. The same IP created for the remote programming functionality is used as part of the PetaLinux tool-chain project. The details of the design are explained in Section 5.3.4.

Specific device-tree files are modified to allow all configured peripherals to communicate with the Linux UIO space. Files such as zynqmp fsbl.elf, pmufw.elf, and design wrapper.bit are used to create BOOT.BIN and Image.ub. BOOT.BIN and Image.ub include the kernel used to boot the embedded OS. Section 5.3.2 provides an explanation of the root file system used for the CentOS implemented in TileCoM. The SD card is divided into two sections, as shown in Figure 5.5, the FAT32 format

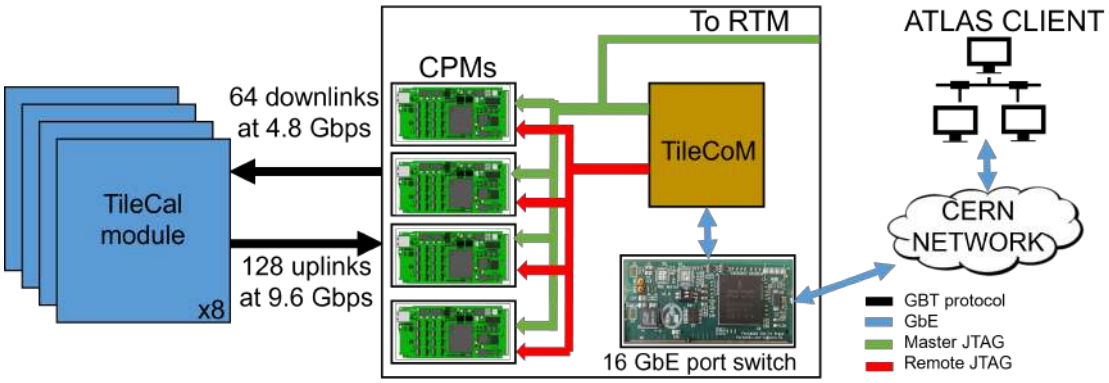


FIGURE 5.7: The ATLAS TileCal Remote programming architecture [107, 111].

section that stores BOOT.BIN and Image.ub, and the ext4 partition is used to store the root file system.

Installation of the Root File System

The root file system is installed in the SD card. The files are cloned from the CERN GIT repository [110] and installed in the ext4 section of the SD card. A CentOS 7 host system is used for the cloning and installation of these files. The extra packages used to create the project are Git 1.7.8, Tar 1.24, and Python 2.7.3. The Dandified YUM (Dnf) package is used for installation purposes compared to the traditional YUM installation package. A QEMU is used to emulate the root file system on the host machine before installation on the SD card. This is helpful for testing purposes to verify that all required files were successfully created. After verifying that all necessary directories and files are present, the root file system is copied to ext4 of the SD card. When the embedded Linux is booted, additional packages such as the NTP server, the GNU Compiler Collection (GCC), ROOT, and others are installed. These packages are essential for networking purposes, a compilation of scripts, plotting of graphs, and other functions.

5.3.3 Objective of FPGA remote programming

TileCoM will be used to remotely program the on- and off-detector FPGAs. The target FPGAs include the DaughterBoard and MainBoard FPGAs in the on-detector

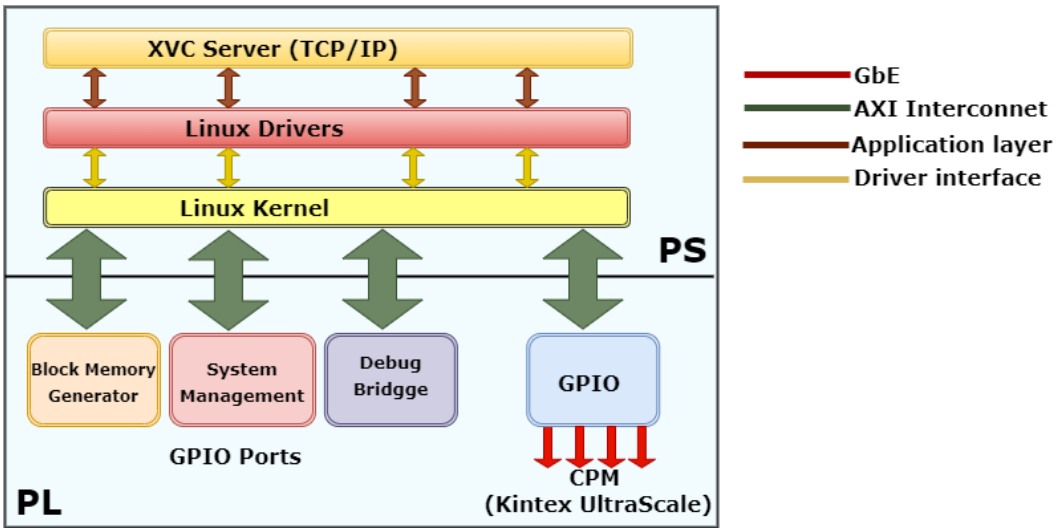


FIGURE 5.8: The remote programming PS and PL blocks of remote programming implemented in TileCoM [107, 111].

electronics and the CPM and TDAQi FPGAs in the off-detector electronics, as introduced in Chapter 3. Each TileCoM configures four CPM Kintex Ultrascale FPGAs (KU115-1A1517C), one TDAQi Kintex Ultrascale FPGA (XCKU15P-2FFVA1760E), 32 DaughterBoards (64 XCKU035-1FFVA1156C FPGAs) and 32 MainBoards (128 Cyclone IV FPGAs). FPGA configuration files, such as bitstreams and memory flash files, will be sent through TCP/IP to TileCoM from external servers. Then TileCoM configures the desired FPGA using dedicated JTAG chains implemented over the fiber for the on-detector electronics. Figure 5.7 shows a block diagram that defines the interconnection paths between TileCoM and the target FPGAs for remote programming.

5.3.4 Implementation procedure of FPGA remote programming

The remote programming functionality is implemented on the PS and PL sections of the TileCoM using the following procedure:

Remote programming software in PS part of the TileCoM

As shown in Figure 5.8, the remote programming software in the PS part of TileCoM is divided into three blocks. The Linux kernel and Linux drivers are generated from the PetaLinux tool-chain, which is part of the embedded CentOS 7 as described in

Section 5.3.2. The Linux application includes an XVC server that is compiled using the C-language source codes. The XVC server is implemented on top of the Linux kernel and driver layers. The application uses low-level libraries and drivers to communicate with the hardware through the TCP/IP protocol. The C-language source codes include functions that control the GPIO ports. These functions mainly assert the GPIO ports, set directions, transmit bitstreams and memory flash files, and finally, de-assert these GPIO ports. An executable file is created for the XVC server upon the compilation of these source codes used to run the server. The debug bridge, as explained in Section 5.3.4, works closely with the application in terms of the TCP/IP protocol and enables remote access to the IP block design. This is verified by checking if the debug bridge acquires communication via User Input Output (UIO). Upon verifying the availability of the debug bridge in the UIO, the TileCoM network connectivity is tested to enable remote connection. Thus, running the XVC application will automatically enable the detection of the server and the available device using the hardware manager of the Vivado software tool.

The TileCoM is interfaced with TilePPr modules through GbE. Upon running the server on the TileCoM, the Vivado hardware manager software tool detects the JTAG-connected FPGA devices on the network. The ATLAS client sends bitstreams to TileCoM using the Vivado hardware manager software tool. Two types of JTAG chain, Master and Remote, send configuration files to the target FPGAs on the electronic chain. The JTAG signals are sent to the on-detector electronics using the GBT protocol at 9.6 Gbps. An ATLAS client is able to remotely connect and send configuration files over the network. This will enable remote access to the XVC application and the Vivado hardware manager tool to detect the necessary FPGAs. The XVC software application is connected to the device driver to open, send directions, and close GPIO ports.

Functionality of the IP in PL part of the TileCoM

Figure C shows a block diagram with the subsystems used in the PS and PL part of TileCoM. The PL part of TileCoM consists of the IP blocks that are connected together for the IP block design of the XVC. The PL design is made up of the Block Memory Generator, System Management, Debug Bridge, and GPIO slaves. The Block

TABLE 5.2: Occupied FPGA resources by the Remote Programming IP core.

FPGA resource	Utilization (%)	Utilization	Available
Look-Up Tables (LUT)	3.17%	2238	70560
Flip Flops	1.70%	2396	141120
RAM blocks	0.35%	102	28800
Input/Output (IO)	7.32%	6	82
Global clock buffer (BUFG)	2.55%	5	196

Memory Generator creates compact, high-performance memories running up to 450 MHz. This IP block uses data widths from 1 to 4096 bits and memory depths from 2 to 128k. System Management provides a complete solution for system monitoring of the TileCoM device. It uses a standalone measurement of system functionality, including sequences and alarms. The Debug Bridge provides a mechanism to establish the communication between the debug cores and non-JTAG interfaces. Lastly, the GPIO slaves are used to create JTAG ports on the TileCoM GPIO ports to send bitstreams. These GPIO ports are changed to Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), and Test Data Out (TDO) ports to allow JTAG signals to be sent over these ports. The PS AXI bus is mainly used to connect data transferred between the PS and the PL. Table 5.2 shows the FPGA resources occupied by the Remote Programming IP core. Resources are measured in terms of the amount of Look-Up Tables (LUT), Flip Flops (FF), Global clock buffer (BUFG), Input/Output (IO), and others.

An additional slave GPIO IP block is used to connect to external blue and yellow LEDs. This extra slave GPIO IP block is used to monitor the functionality of the firmware. The blue LED flashes when the bitstream is flashed on the TileCoM. The yellow LED continually blinks at an interval of 5ms after running the XVC server. Each slave GPIO IP block receives an asynchronous clock and a reset from the PS through the peripheral. This is the same clock and resets used throughout the design as all other IP blocks used for the design. The external interfaces of the GPIO IP block are connected to the 40-pin low-speed expansion header of the evaluation board.

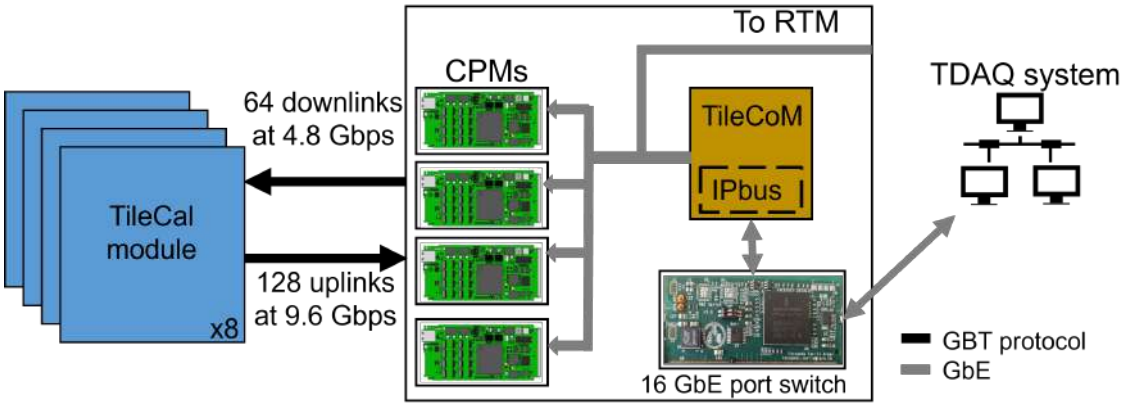


FIGURE 5.9: The ATLAS TileCal TilePPr-TDAQ interface block diagram [111, 112].

5.3.5 Objective of ATLAS TilePPr-TDAQ interface system

The TileCal off-detector electronics for the ATLAS Phase-II Upgrade are divided into two main sections: the TilePPr section and the TDAQi section. Figure 5.9 shows a block diagram of the TilePPr and TDAQ system interface. This functionality focuses mainly on the communication of TilePPr and TDAQi with the ATLAS TDAQ system. The main purpose of this communication is to slow-control and configure the on- and off-detector electronics. It also involves monitoring of on-detector electronic sensors and TilePPr sensors, which include CPM and ATCA on-board sensors. This involves the configuration of ATCA carriers and CPMs in terms of clocks, optical modules, and other peripherals. This functionality is achieved with an implementation of TileCoM via the IPBus protocol and Ironman software.

5.3.6 Implementation procedure of TilePPr-TDAQ interface system

Ironman IPbus software integration

The Ironman software introduced in Section 5.1.2 is implemented on the TileCoM to communicate with the IPbus firmware on the CPM and firmware on the TDAQi. The internal communication block of the Ironman software establishes communication with the TDAQ system through the TileCoM PL. This implementation enables the TDAQ system to access TilePPr. The ATLAS TDAQ system operates as the ATLAS client of the Ironman architecture, as explained in Section 5.1.2. The TDAQ system will transmit and receive IPbus commands as configuration signals to both on- and

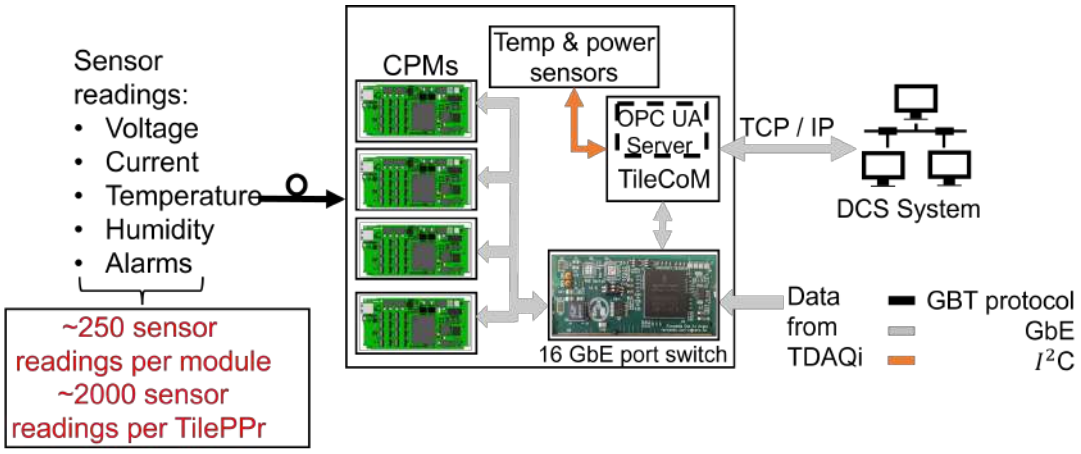


FIGURE 5.10: The ATLAS TilePPr and DCS interface functionality [111, 113].

off-detector electronics. These signals will request data packets to the GbE Switch to access the entire TileCal electronic readout chain. These requests are received by the server running on the TileCoM, transmitted to the other Ironman software blocks, and transmitted back the response to the TDAQ system. The server is continuously running on the TileCoM PS listening to requests from the TDAQ system.

For the initial test station, the TileCoM XADC is used to test the implementation. In this case, the internal communication interface transmits the packet requests to the XADC. The internal communication block requests offset, raw, and scale sensor data of the voltage and temperature sensor data from the XADC. Each temperature and voltage peripheral is assigned an identical address for IPBus read requests. A hardware definition file in a YAML Ain't Markup Language (YAML) is used to add hardware definitions for the XADC.

5.3.7 Objective of the the ATLAS TilePPr-DCS system interface

This functionality focuses on the communication, acquisition, and publication of sensor data to the DCS. This is achieved by a server on the TileCoM to control and monitor the TileCal Phase-II Upgrade electronics system. Figure 5.10 presents the general block diagram of the TilePPr and DCS interface functionality [103]. This block diagram basically shows the connection to all the components of the off-detector electronics and the external user. All TilePPr modules communicate with each other through GbE to transfer monitoring data. However, the TileCoM communicates

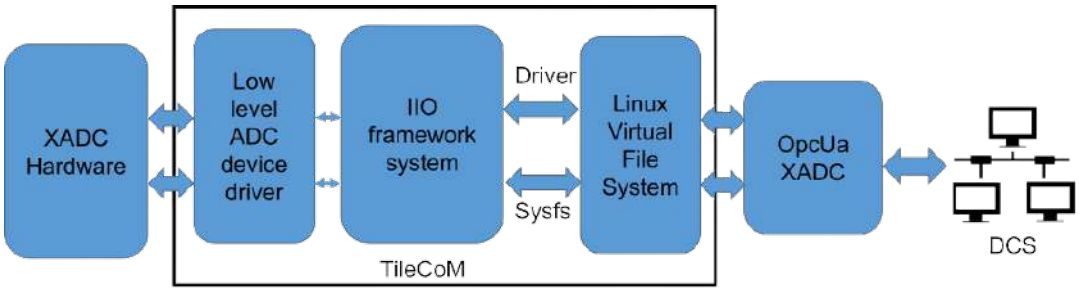


FIGURE 5.11: OPCUA server for Xilinx Analog to Digital (OpcUAX-ADC) [111, 113].

with the ATCA through the I^2C interface. The DCS communicates with the servers through the TCP/IP protocol that is accessible remotely when both the DCS and TileCoM are connected to the same ATCN network. The servers will run concurrently on the TileCoM, and these servers will read approximately 2,000 sensors per TilePPr. All the 2,000 sensors are read from the on-detector electronics. They will transmit sensor data from TilePPr to DCS at a maximum frequency of 0.1 Hz [106]. In simple terms, this functionality focuses on the sensor monitoring reading from TilePPr, TDAQi, and on-detector readout electronics. This functionality focuses on the following four factors from the readout electronics:

- Power consumption, optics diagnostics, temperature sensors, etc..
- I^2C interface for reading local ATCA carrier sensors.
- CPMs retrieve sensor data from on-detector through GBT links.
- TileCoM reads out sensor data from CPM and TDAQi through GbE (IPbus).

5.3.8 Implementation procedure of the TilePPr-DCS system interface

Quasar+XADC software integration

This server was tested with both the UA expert [114] and the SCADA for the publication of data for DCS. The test-bench used for software implementation consists of an integration of the TileCal GbE Ethernet Switch (motherboard and card), the network router, the Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board, and the CPM emulator board as the Xilinx Virtex-7 FPGA VC707 Evaluation Kit. An OpcUA server is implemented on the TileCoM to readout sensor data from

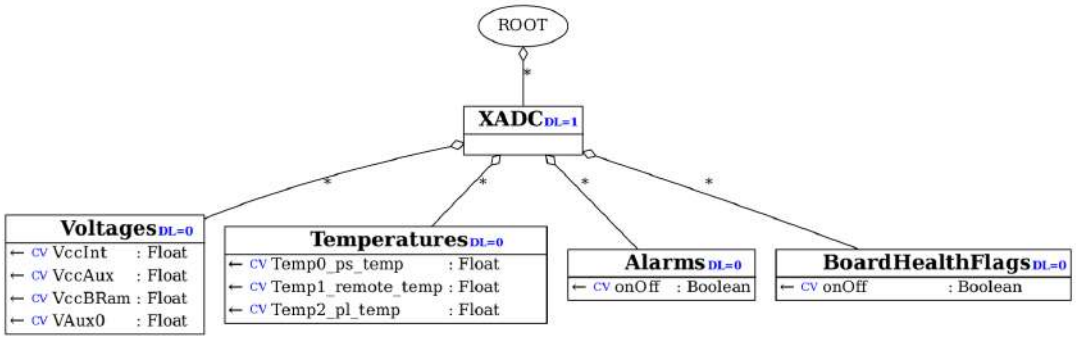


FIGURE 5.12: The Quasar block design to read the XADC sensor [111, 113].

the electronic system. These servers will run concurrently on the TileCoM and are called Tile OpcUAXADC and Tile OPCUA IPbus.

The Quasar framework introduced in Section 5.1.3 is used to design and implement this TileCoM functionality. Upon building this design, an executable is created to run a server on TileCoM. This server uses a TCP/IP protocol to communicate with DCS clients and transmit data to the client. Figure 5.11 shows a block diagram of the Tile OPC-UA server. Different blocks perform a specific function for the overall functionality of the server. These blocks are the XADC hardware, the low-level ADC device driver, the IIO library, the Linux virtual file systems and OpcUAXADC. All of these blocks are linked to a readout of sensor data.

Figure 5.12 shows a Quasar-generated design of the Tile OpcUAXADC server in a tree-format structure. Quasar enables users to design the server using XML design files. This shortens the development cycle and allows users to focus on critical parts of the design. As shown in the figure, the XADC is directly connected to *ROOT* of the design. The XADC is the parent design, and all children related to the XADC are connected to the XADC. Voltages, Temperatures, Alarms, and BoardHealthFlags are all children related to XADC. All these children are designed as device logic using the Quasar framework, as explained above. The Voltage and the Temperature include cache variables that are named specifically to the sensors on the XADC. The Alarms and BoardHealthFlags include Boolean variables to ensure the safety and health status of TileCoM.

Specific hardware addresses are included in the implementation to link to each type of sensor. As shown in the block diagram in Figure 5.11, the XADC hardware

TABLE 5.3: Subdirectories and functions of the IIO library.

Directory	Function / data type	Operation
Sys directory	IIO_chan_info in_voltage0_raw in_voltage_scale	Includes channel information calls read values. calls scale values
Device driver	Poll function Buffer functions struct	Call iio_trigger_poll and iio_trigger_poll Allocation purposes (kfifo or ring buffer) Declares all these functions
IIO subsystem	IIO ring IIO core IIO trigger	Trigger functions to capture data trigger register and unregister Trigger allocation and free function

block is the actual sensors in the readout electronics. Any type of XADC sensor in the readout electronics uses a specific address that is used in the implementation of the server to readout data. Thus, the implementation calls these specific addresses to recognize each type of sensor. Communication between the XADC sensor and the server transmits and receives signals to transfer signals from the hardware to the software on the TileCoM. The low-level ADC device driver is configured and implemented during the generation of embedded Linux files, as explained in Section 5.3.2.

Table 5.3 shows a table of different directories with related functions and data types. These functions were implemented in TileCoM as an interface between hardware and application software. Different levels of the design are shown in terms of these functions and access to the XADC. The IIO subsystem directory is directly linked to the read channel for data transfer. The device driver directory is used for the allocation and declaration of functions. The system directory is used to read raw and scale values from the ADC. In order to precisely know the type of value to request, a bitmask is used to allow for precise identification of the channel needed. For example, in the case of voltage or temperature values, a scale is used to convert the returned value to voltage and temperature. The registration of devices with functions and the declaration of channels using *struct* is sufficient for the basic design of the IIO device drivers. All the blocks of the design are linked together with a transmit and receive signal amongst each other.

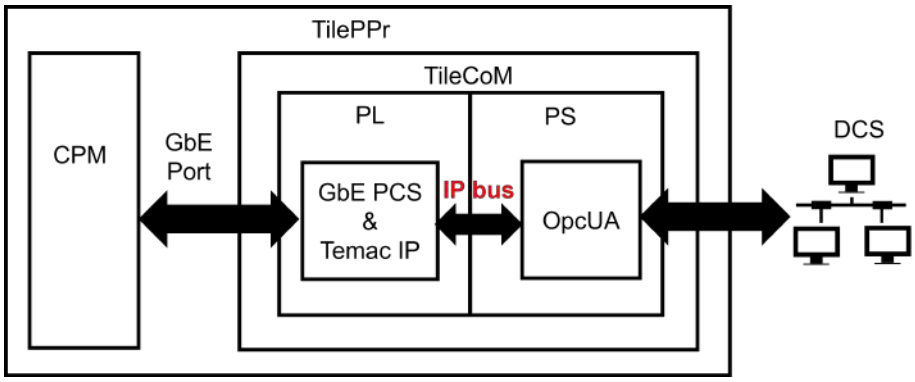


FIGURE 5.13: Tile OPCUA IPbus server for TilePPr and DCS monitoring systems [111, 113].

Quasar+IPbus software integration

Figure 5.13 shows a block diagram of the Tile OPCUA IPbus server for the TilePPr and DCS monitoring systems. This is the main OPCUA server for readout electronics and transmitting sensor data to the DCS. The block diagram shows the integration of modules for the off-detector electronics. This server also reads sensor data from the on-detector electronics through the CPM. Each block shown in Figure 5.13 performs a specific function in the overall functionality of the server. Compared to the Tile OpcUAXADC server, this server is developed on both the PL and the PS of TileCoM.

The server is integrated into the PS to run the executable file and transmit sensor data to the DCS client. Hence, the PS includes the OPCUA block with an interconnection to the PL through the AXI interconnect. However, to connect the CPM and TileCoM, a few IP blocks are used on the TileCoM PL. The main IP blocks used in the design are the GbE PCS and temac IP blocks. These two blocks enable the connection through GbE between TileCoM and CPM. Both the CPM and the TileCoM are connected to the Tile GbE Switch through their GbE ports. The IPbus is integrated with the Quasar framework to acquire data from the CPM.

Figure D shows the design generated by a Quasar framework. Compared to the OpcUaXADC server design, the tree design diagram has four levels, from *ROOT* to *leaves*. However, the generation of these two designs both uses XML files. TileCoM is the parent in this design with two children, CPM and TDAQi. As this is the main server for the TilePPr and DCS functionality, the CPM child in the design is linked to

all the on-detector electronics sensors and some of the off-detector electronics sensors. The TDAQi child is connected to the ATCA and TDAQi sensors to transmit sensor data to the DCS client. Some sensors are shown in the design for demonstration purposes. However, the actual design includes approximately 2,000 sensors for each TileCoM parent in the design.

As can be seen in the figure, all the sensors connected to the CPM and TDAQi are designed as cache variables because they continually change with time. Most of these sensors acquire data as floating variables, except for BoardHealthFlags and Functionality. These are not actual sensors but peripherals included in the design to monitor the safety and health status of the boards on the readout electronics. Each sensor in the design is regarded as a device logic to be able to recognize each sensor type.

The IPbus is integrated into the Quasar framework to enable the server to acquire data through the PL. The use of IPbus enables the design to access the Hardware Access Library (HAL) and Read-Modify-Write (RMW) transactions. This part of the OPCUAIPbus design is used as an API for transaction purposes. The addresses of each sensor are stored in the register. XML files are used as connection and address table files to initialize the addresses of each sensor and to declare the type of protocol to transfer data. For this design, only the TCP/IP protocol is used, not the UDP. Multiple register tables can be used to declare the addresses of each sensor.

In-depth details of the IPbus framework are explained in Section 5.3.5. This framework is used in conjunction with the Quasar framework to handle the request and transmit data packets through TileCoM.

Chapter 6

Integration Tests of TileCoM and TilePPr components

Chapter 5 presented the implementation of TileCoM functionalities in terms of firmware and software implementation. The remote programming functionality of TileCoM is explained in terms of the IP block firmware and software design. TilePPr and TDAQ integration is described in terms of implementing Ironman software on TileCoM. Lastly, the TilePPr and DCS integration functionality is explained in terms of implementing two OPC UA servers on the TileCoM.

This Chapter presents the results of the implementations discussed in Chapter 5. The first Section of this chapter presents the modules used for the testbench. As this contribution presents the first stage of tests for the TileCoM, all the modules are commercial boards, excluding the Tile GbE Switch with the motherboard. The second Section presents the integration results of the TileCoM, and the last Section discusses the results of the ATCA preparation for the Demonstrator project.

This Chapter also explains how the TilePPr Demonstrator board is integrated with the ATCA [60] and TilePPr modules of the ATCA. This project serves as a basis for the final design of the TilePPr module. Control and monitoring of the TilePPr Demonstrator board and the ATCA carrier are presented in the last section of this chapter. Monitoring results in terms of voltage, current, and temperature are shown with discussions related to threshold values.

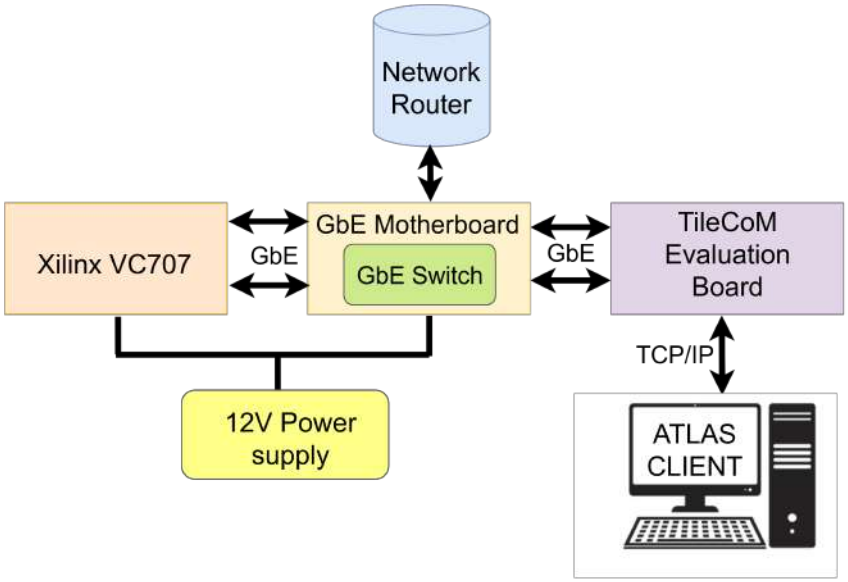


FIGURE 6.1: The integration of the first prototype TilePPr boards testbench.

6.1 Integration setup with first prototypes

Figure 6.1 shows the first TileCoM testbench with the TilePPr modules. With respect to the testbench and the final TilePPr design, it can be deduced that not all modules are on the testbench. The main objective of this testbench is to operate the TileCoM module with some TilePPr modules. As explained in the introduction of this chapter, this is the first stage of tests for the TileCoM. The TileCoM evaluation board is used to design, implement and test all of the functionalities of the TileCoM.

Figure 6.1 shows the Xilinx VC707 evaluation board, GbE Switch, GbE Switch motherboard, TileCoM evaluation board, the network router, and the ATLAS client. The Xilinx VC707 evaluation board is used as part of the TilePPr modules to communicate with the Tile GbE Switch and the TilePPr module. Using the SODIMM connector, the GbE Switch motherboard is used as a slot to insert the GbE Switch. The motherboard consists of 16 SFP modules and an SODIMM connector to interface them with a GbE Switch. The Xilinx VC707 evaluation board and GbE Switch motherboard are supplied with 12V power.

The network router is used for test purposes to connect the testbench to the network. All the TileCoM functionalities mentioned need to be accessed remotely by the ATLAS client. The router is connected in a point-to-point connection with the GbE Switch via an Ethernet port. The other Ethernet ports of the GbE Switch connect

FIGURE 6.2: Xilinx VC707 evaluation board [115].

the Xilinx VC707 evaluation board and the TileCoM evaluation board. This enables the ATLAS client to remotely access all testbench modules through the TileCoM over TCP/IP.

6.1.1 Xilinx VC707 evaluation board

Figure 6.2 shows a Xilinx VC707 evaluation board [115] used as one of the modules to test the TileCoM functionalities. The Xilinx VC707 evaluation board is a highly flexible and high-speed serial base platform used for numerous applications. The kit includes 485 760 logic cells, 56 GTX (Gigabit Transceiver) 12.5 Gb/s transceivers, and I/O pins. For this contribution, it is mainly used for processing and data storage. This is ideal for the high-performance transmission of packets of data between TileCoM and Xilinx VC707.

The Valencia team designs the firmware design for this module and is flashed on the FPGA to test communication between TileCoM and Xilinx VC707. This module is used to represent the CPM compared to the final design of the TilePPr. The Xilinx VC707 evaluation board is designed differently from the CPM board. However, the functionality tests performed on the integration with TileCoM are similar to those with the CPM. TileCoM is integrated using the GbE protocol with the Xilinx VC707 evaluation board in the same way it will be integrated with the CPM. For the TilePPr and DCS interface, the firmware acquires sensor data and transmits these data to the TileCoM through the AXI chip-to-chip implementation on the TileCoM.

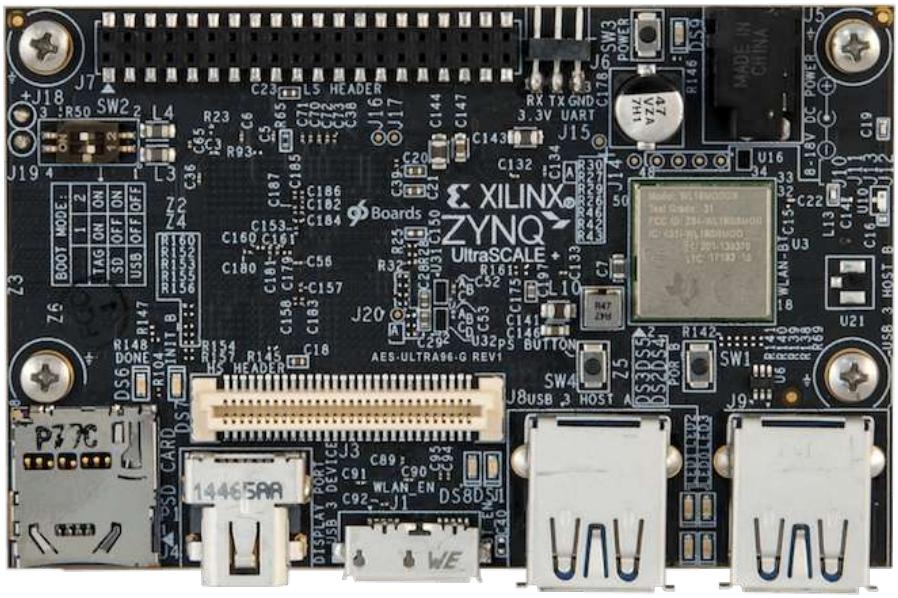


FIGURE 6.3: Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board [116].

6.1.2 Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board

Figure 6.3 shows a picture of the Avnet Ultra96 version 2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board [116]. Xilinx manufactures the FPGA chip on the evaluation board. However, the evaluation board is designed and manufactured by Avnet. This evaluation board is used for test purposes to prepare for the TileCoM-TilePPr integration tests. The evaluation board and the actual TileCoM use a similar ZYNQ UltraScale+ MPSoC FPGA chip. Thus, the firmware and software developments implemented on the evaluation board will still be able to be implemented on the actual TileCoM. The firmware and software implemented on TileCoM evaluation board, as explained in Section 6.2, communicate with the peripherals of the evaluation board such as GPIOs, USB-UART, etc. Minor changes to the firmware and software will include changing the peripherals during implementation on the actual TileCoM. For example, the remote programming functionality uses the GPIO port positions on the evaluation board. GPIO port positions will need to be modified on the firmware and software to implement this functionality on the actual TileCoM.

Apart from the Xilinx Zynq UltraScale+ MPSoC ZU3EG, the evaluation board

consists of several key features, such as the 40-pin low-speed expansion header, 60-pin high-speed expansion header, and other components. These key features were immensely used for this thesis's firmware and software development. For example, the DONE and INIT_B LEDs are used while flashing the firmware bitstream on the TileCoM PL. Thus, these two LEDs should be ON during every boot and external flashing of the bitstream. A 40-pin low-speed expansion header is used to test remote programming functionality. GPIO ports are assigned to some of these pins, and the JTAG signals of the evaluation board are connected to these GPIO ports.

Specific Board Support Package files (BSP) for the evaluation board are used during the embedded Linux and firmware design. These files were imported into the Vivado IDE to design and generate bitstreams for the evaluation board. The first design involved the transmission of packets of data through the Bluetooth / Wifi chip. An improvement in the design involves the use of USB ports to connect the evaluation board to the network. Thus, a USB-to-Ethernet adapter is used to enable this communication over a LAN cable.

To configure and program the evaluation board, a JTAG/UART Parallel Optical Device (POD) is used to connect to the JTAG terminals of the board. The POD connects to the evaluation board's TDI, TDO, TMS, and TDI terminals. The POD also connects to the UART terminals of the evaluation board. These terminals are the transceiver terminals that enable the UART terminal to be used on display. Thus, a USB cable is connected to the POD to display the terminal of the embedded Linux. The PS of the Xilinx Zynq UltraScale+ MPSoC ZU3EG is directly connected to the UART of the POD, and any operation performed on the terminal is transmitted to the PS and back to the terminal. The POD includes a reference voltage used as a voltage translating level between the 3.3V and the voltage on the evaluation board.

The terminal software used to connect and display the embedded Linux running on the evaluation board is Putty [117]. The first stage of tests using Putty involves serial communication. A point-to-point connection between the POD and the laptop display establishes this serial communication. The speed of the serial interface is set to 115,200 at data bits of 8 and stop bit of 1. The parity and flow control parameters are set to none. However, the TileCoM functionalities are intended to operate remotely. Thus, the second stage of the tests involves using ssh over Putty to *log-in*

FIGURE 6.4: The Tile GbE Switch motherboard.

to the evaluation board.

6.1.3 The Tile GbE Switch motherboard

As explained in Chapter 5, all TileCoM functionalities are implemented to operate remotely, and the use of the GbE Switch enables a connection of the TilePPr to be accessed remotely. Integration tests involve remote access to the testbench for this contribution. Figure 6.4 shows the custom GbE motherboard and the GbE Switch explicitly designed for Tile readout electronics. As shown, the GbE Switch card is connected directly to the motherboard through the SODIMM connector. The motherboard is powered by an external power supply of 12V and has 16 Ethernet ports used for test purposes. The motherboard is used to resemble the final design of the ATCA carrier. This board is designed and produced by the Valencia team. It is used in this contribution only for testing purposes.

Of all the 16 ports available on the motherboard, only three ports are used to transmit and receive data packets for this contribution. Two GbE standalone tests were performed to check the functionality of these cards. The GbE card passed the continuity tests with no components short-circuited, and all components were successfully mounted. The second test involved communication tests using the TileCoM evaluation board, the Xilinx PYNQ board, and a computer display. The GbE

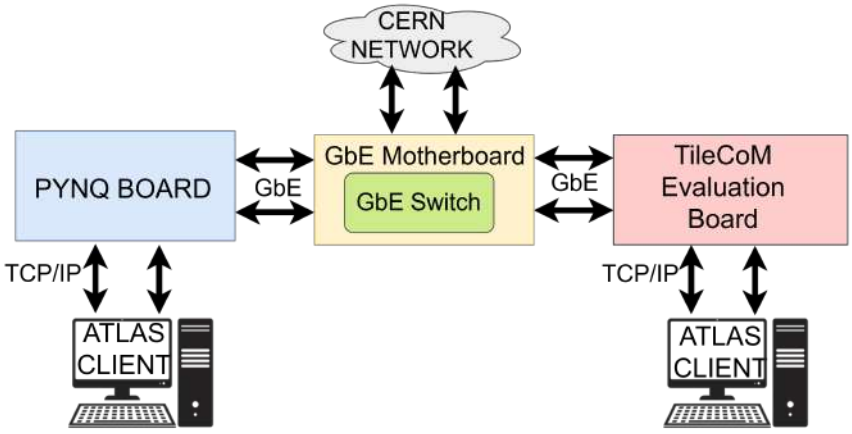


FIGURE 6.5: The TileCoM and PYNQ board test station.

was connected to the motherboard and the CERN network. The TileCoM evaluation and the Xilinx PYNQ board were connected to the motherboard to allow network access on both boards. These two boards were connected to their display and successfully pinged each other. Figure 6.5 shows a block diagram of the modules used for communication tests.

6.2 Integration tests for TileCoM main functionalities

6.2.1 FPGA remote programming

As mentioned in the previous chapters, this contribution focuses on the implementation of three main functionalities of TileCoM on the TileCal readout chain. The first functionality is remote programming of the FPGAs on the readout chain. This Section presents the first stage test results for this functionality. The same testbench presented at the beginning of the chapter is used to test this functionality. This test includes the integration of firmware and software with the TilePPr modules. The step-by-step process from synthesis to bitstream generation is detailed below. This design is interfaced with the software on the TileCoM PS through the AXI interface. The software is designed and implemented on TileCoM using the C-language. The process of compilation, running, and detecting the server in the Vivado software is also explained below.

As mentioned that the implementation of the remote programming is on the PS

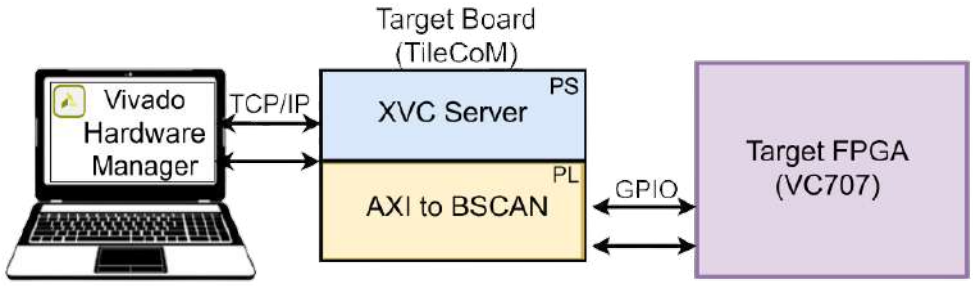


FIGURE 6.6: Hardware manager integration with with TilePPr modules.

and PL, the PS resembles Zynq UltraScale+, while PL shows a number of interconnected IP blocks. PL IP blocks are the debug bridge, five GPIO IP blocks, the reset of the processor system, and the clocking wizard. The interface between PS and PL is through the AXI peripheral. The AXI peripheral provides an interface for the master and slave connection. All GPIO IP blocks connected to the AXI interface are connected as slaves.

The main IP block used to detect TileCoM through the TCP/IP protocol is the debug bridge. It can be seen from the IP block design that there are two debug bridge IP blocks. Out of 5 modes (From AXI to BSCAN, From JTAG to BSCAN, From PCIe to BSCAN, From PCIe to JTAG, and From AXI to JTAG) provided by XVC in the debug bridge, this design uses the JTAG to BSCAN to detect the TileCoM PL. XVC commands are received via the AXI4-Lite slave interface in this mode. Since the PS transmits data packets through the network, this mode is used to gain access to the device's boundary scan. The access enables the server to detect the TileCoM PL and eventually gain access to the TileCoM GPIO pins. Tests for TileCoM to program the VC707 can also be performed using the AXI to JTAG mode. This mode is only used if the SoC is used to drive external FPGAs. However, for this contribution, the AXI to BSCAN is used to program and configure the TileCoM.

The design is synthesized and implemented before the generation of the bitstream. Constraint parameters related toTileCoM hardware are included in the constraints file prior to design implementation. The successful implementation of the design generated a bitstream that is used to program TileCoM.

Figure 6.6 shows a block diagram of integration between the Vivado hardware manager and the target FPGA. A hardware manager is a tool used to access the

TABLE 6.1: Remote programming five C-language software functions.

Function	Operation
Gpio_open	Use of open drain and open source to drive the signal levels.
Set_direction	Used to control the GPIO pin as an input or output.
Set_value	Sets the GPIO pin with a 1 or 0 to drive the signal.
Get_value	Get a signal of 1 or 0 from the user to drive the GPIO pin.
Gpio_close	Close all GPIO pins to initial signal.

XVC server remotely and send bitstreams. This is achieved through Ethernet using the TCP/IP protocol. Upon a server in TileCoM, the server connects to the debug bridge in the PL through AXI. To send a bitstream using the hardware manager, an open target tab is used to detect the localhost hardware server. Right-clicking the localhost hardware server enables the ATLAS client to add XVC. A window opens with the hostname and port input is used to input an IP address and a port number. These details are defined in the XVC software design. The target FPGA shows up in the Vivado software hardware manager under the device target. A bitstream is then sent to the target FPGA such as the VC707 in the hardware manager with its own FPGA device name.

As mentioned in Chapter 5, the target FPGA is accessed through JTAG chains. However, GPIO pins are used as JTAG chains to access and send JTAG signals from TileCoM to VC707. These pins are defined in the software part of the XVC server. The design constitutes of five C-language functions shown in Table 6.1. All these functions are used in conjunction with the network function of the software design. The network function includes the socket function to set the IP address and port number.

Figure 6.7 shows a graph of the time measurements taken during remote programming of the Virtex FPGA. Several iterations were performed during measurements of the time it takes to program the FPGA. The statistical median of the measured data is 4.939 s, the mean is 5.045 s and the standard deviation is 0.319.

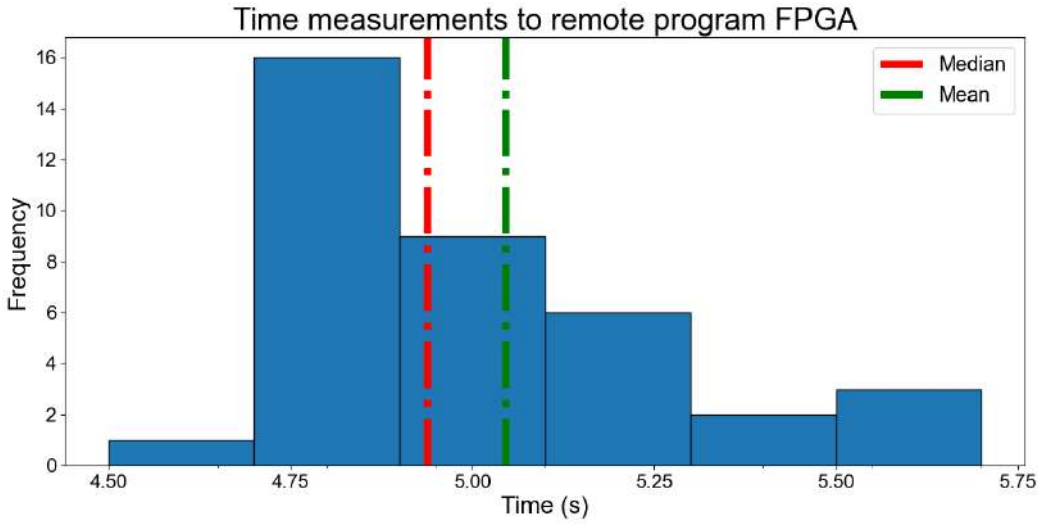


FIGURE 6.7: Time measurements to remote program FPGA.

6.2.2 Interface with the ATLAS DCS system functionality

The TileCoM implements two OPC servers for DCS monitoring. The first Xilinx Analog-to-Digital Converter (XADC) OPC server monitors power consumption, optical diagnostics, and temperature sensors. The second OPC server is implemented to interface with the ATCA carrier, TDAQi, and CPM sensors. Additionally, this second server reads out local ATCA carrier sensors through the I^2C interface and reads out sensor data from CPM and TDAQi through GbE using the IPbus software implementation.

The Quasar software development framework, as discussed in Chapter 5, is used for generic and efficient development of OPC UA servers. The Quasar designs are created in XML formats, and OPC UA executables are generated to run the servers. This framework reduces the development cycle and enables developers to integrate their devices. Configuration files are also generated in XML formats for client connectivity and server data representation. To integrate this framework with TileCoM XADC, the IIO library is added to the custom C++ code. That is, when the server is running on the TileCoM, the server reads out sensor data from the device logic and publishes these data through the configuration file to the client application.

A few client applications are available to test publication of data acquired by the OPCUA server, such as the SCADA. These servers are tested with both the UA expert and SCADA for publication of data for DCS. The testing stages with both

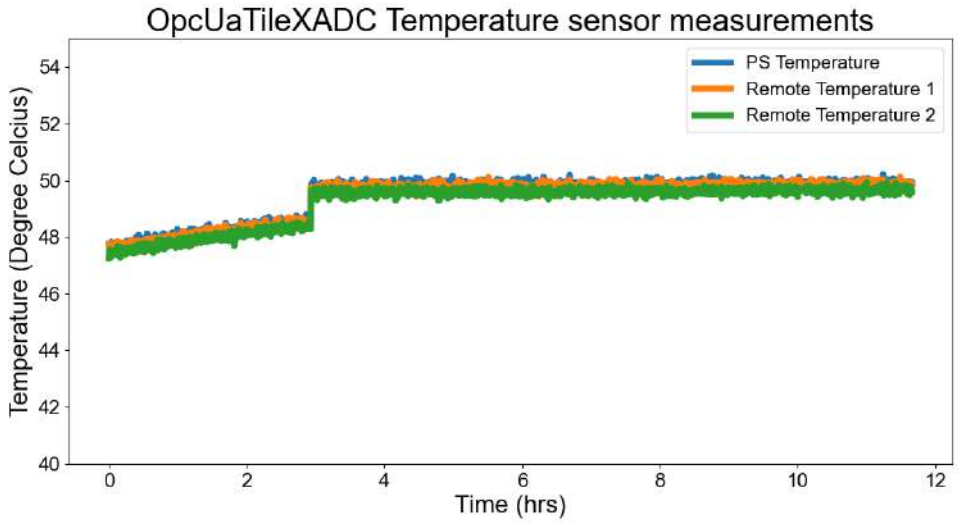


FIGURE 6.8: The OpcUATileXADC Temperature and Voltage sensor data.

client applications show that the OPC servers from the TileCoM are portable for these two client applications. This shows flexibility for ATLAS users who will be using TileCoM to integrate their system with the DCS. The sensor data are acquired and published to the client application in real-time every second. The ability of the quasar framework to acquire sensor data every second enables the server to acquire accurate sensor data. The acquired data are approximately equal to the values expected from the datasheet of the XADC sensors. DC and AC switching characteristics present the nominal and threshold values of these sensors. The voltage sensor on which this contribution is focused is the the VCC supply of the DDR module. The temperature sensors on which this contribution focuses are: PS temperature, remote temperature 1 and remote temperature 2.

The minimum threshold, and maximum values of these sensors are included in the Xilinx datasheet. A comparison of the sensor data measured and the datasheet proved the functionality of the server running on the TileCoM. A minimal difference was obtained between the measured values and the datasheet values. This is acceptable depending on the accuracy of the sensors' measurements. Figure 6.8 shows a plot of temperature sensor readings taken for a period of 24 hours running the OPCUA server on TileCoM. The temperature readings are changing in the range of 48 °C for the PS temperature sensor. The temperature of the board increased during the data acquisition period, but all temperature values remained at the threshold

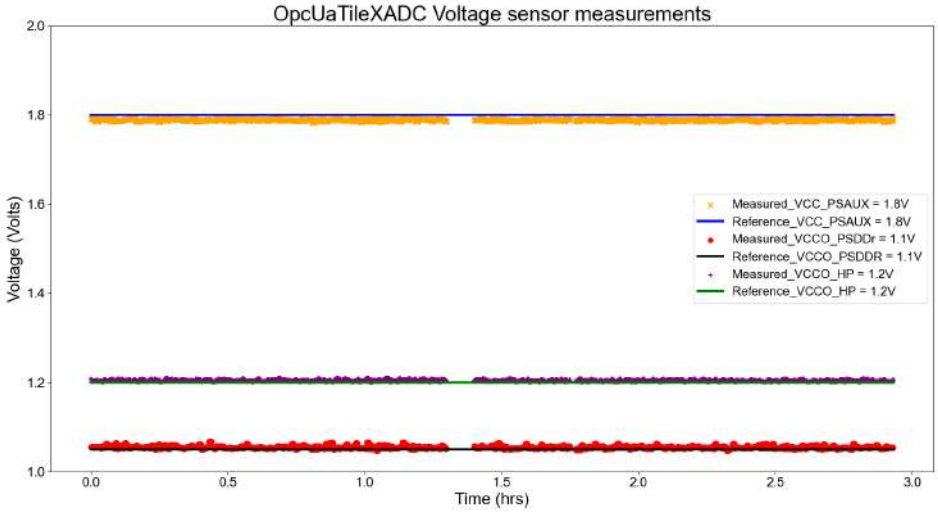


FIGURE 6.9: The OpcUATileXADC voltage sensor data.

values according to the recommended operating values from the manufacturer. The temperature range for the sensors shown in the figure is between 0 °C and 100 °C. This includes the operating range for both extended devices and industrial devices. The tests were started early in the morning until the evening. The starting temperature of the board runs at approximately 47 °C and ends at approximately 47 °C. The graphs show a linear increase in the temperature readings, and no cooling mechanism was installed during the tests. Figure 6.9 shows the voltage measurements read out by the OpcUAXADC server implemented in Chapter 5. These readings were taken for 3 hours and the measurements are within the threshold values recommended by the FPGA manufacturer.

The final design of the TilePPr and DCS interface involves the implementation of a TileCoM server to accommodate all TilePPr modules. The server will publish the sensor data to the DCS client application (SCADA and/or UA expert). A screenshot of the DCS client GUI application used to publish the sensor data is shown in the Appendix C.

6.3 ATCA and TilePPr Demonstrator board monitoring

This section presents preparation of the TilePPr modules for the Demonstrator project. Modules presented in this section are used as the first prototypes for the final design

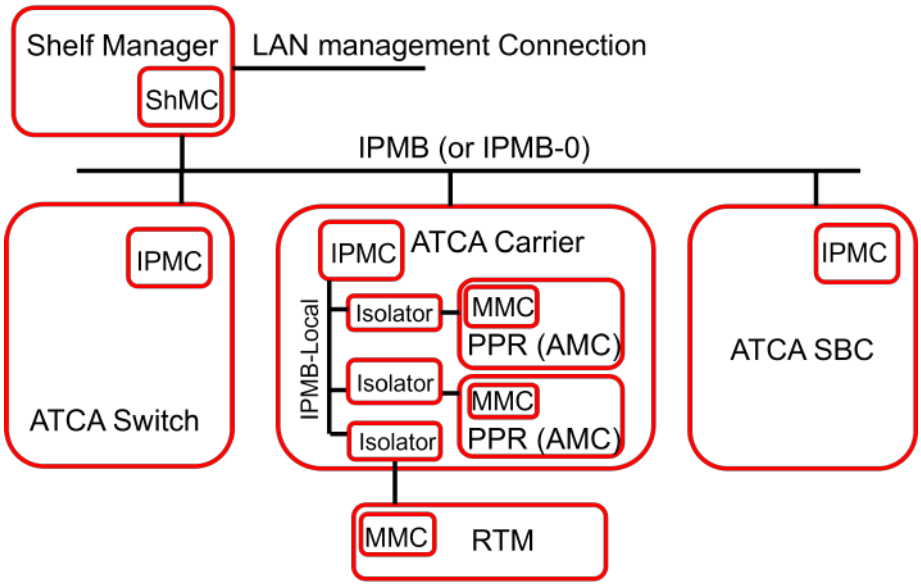


FIGURE 6.10: I^2C Communication of the ATCA shelf manager through IPMI [68].

of the TilePPr project. These include the TilePPr Demonstrator board to load the firmware developed by the Valencia team, the ATCA chassis with the carrier, and the shelf managers. These modules are integrated together in this section inside an ATCA chassis. The ATCA chassis is connected to the CERN network through the shelf manager and adheres to the CERN ATCN computer networking rules.

Several tests were carried out to connect the modules in the ATCA chassis to the network. The main purpose of connecting the ATCA chassis to the network is to allow remote access to the readout chain. The final Demonstrator is inserted in ATLAS and the entire readout electronic chain is accessed through the ATCA chassis. That is, connecting the ATCA chassis enables the entire readout electronic chain to connect to the network. The Demonstrator module has one DBv4 and TilePPr Demo with 16 uplinks and 16 downlinks.

In preparation for the final Demonstrator project, the goals for the ATCA preparation project are mentioned in Chapter 5. These goals were established to remotely control and monitor the status of TilePPr modules in an ATCA. The following Sections provide a detail procedure on how these goals are achieved and a presentation of the monitoring results.

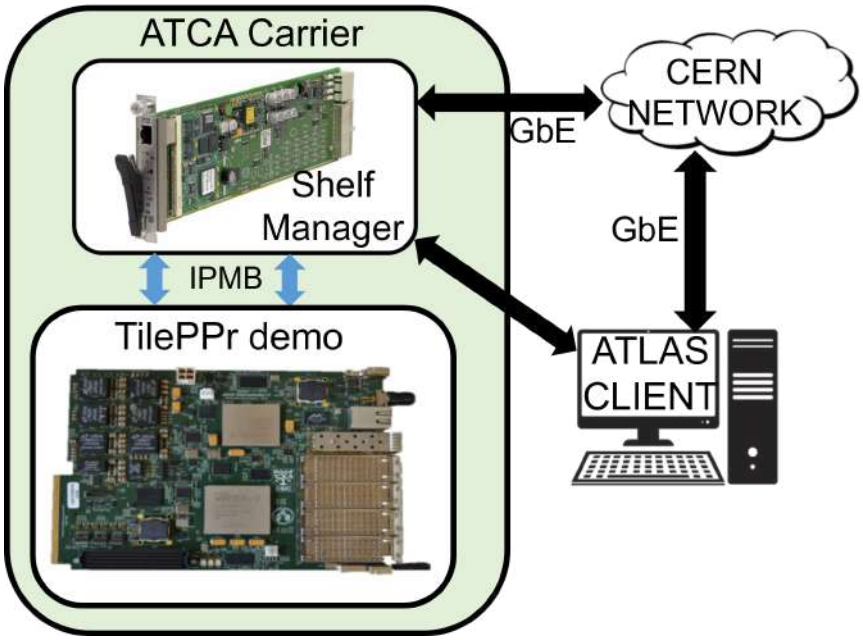


FIGURE 6.11: ATCA preparation for the Demonstrator project test-bench.

6.3.1 IPMI Communication of modules in the ATCA

Figure 6.10 shows the IPMI hardware management interface used to interface the TilePPr modules in an ATCA chassis for communication purposes. This tool is installed on the shelf manager which is responsible for all the services such as power control, fan speeds, temperature readings, and voltage readings, among others. All TilePPr modules communicate with the shelf manager via IPMB using the I^2C protocol. Three IPMCs are connected to the IPMB where one IPMC communicates with the GbE Switch and the other IPMC communicates with the SBC. The last IPMC is connected to the ATCA carrier, which includes a local IPMB. This local IPMB includes a slot for a TilePPr Demonstrator board with the MMC. The connection of this TilePPr Demonstrator board to the local IPMB is through the isolator connector. In a case where it is necessary to use one TilePPr Demonstrator board instead of two, an isolator is open to break the communication connection to the IPMB.

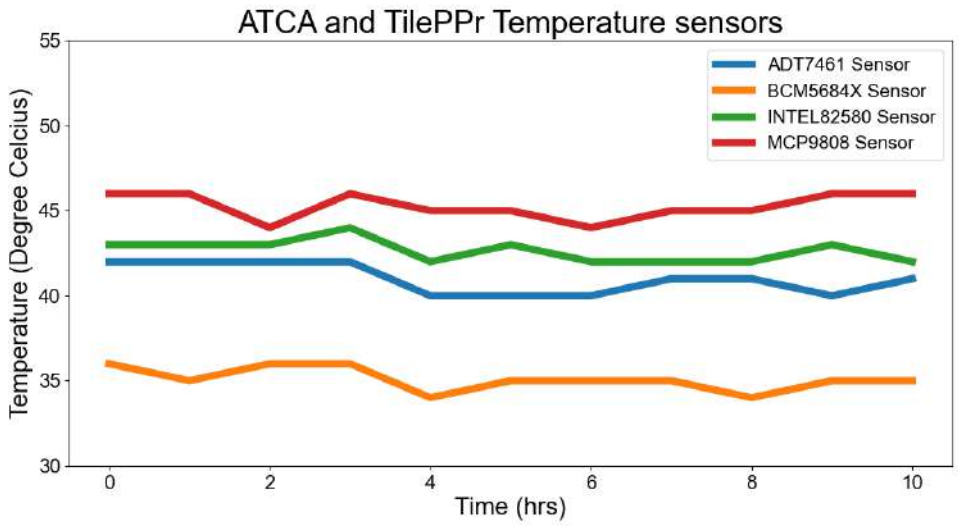


FIGURE 6.12: The ATCA carrier temperature monitoring results.

6.3.2 Testbench used for the Demonstrator project preparation

Figure 6.11 shows the testbench used to prepare the ATCA and the Tile Demonstrator board for the demonstrator project. This block diagram shows the main components that are connected to perform tests. The TilePPr Demonstrator board is inserted into the ATCA carrier in the AMC slot. The shelf manager 500 (Shm500), together with the backup shelf manager, comes with the ATCA shelf. A shelf manager, as shown in the figure, is connected to the ATCA carrier through the IPMB bus. The ATCA shelf includes numerous RJ45 connector ports where one port is directly connected to the wall (CERN network) and the other port on the shelf manager, which is connected to an external computer.

An on-the-shelf-running embedded Linux is used to configure the network and run tests on it. A CentOS 7 was running on the shelf manager, and the network was configured to use automatic DHCP protocol to connect to the network as soon as the RJ45 connector is connected to the wall socket. The first stage of the tests involved a point-to-point connection between the computer and the shelf manager. Upon connecting and configuring the ATCA to connect to the network, the two devices managed to ping each other using the Ethernet cable. As one of the main purposes of this project is remote-access to the ATCA modules, SSH is then used for the second stage of the test using PUTTY software. Remote log-in into the shelf manager enabled sensor data acquisition by running software on the terminal.

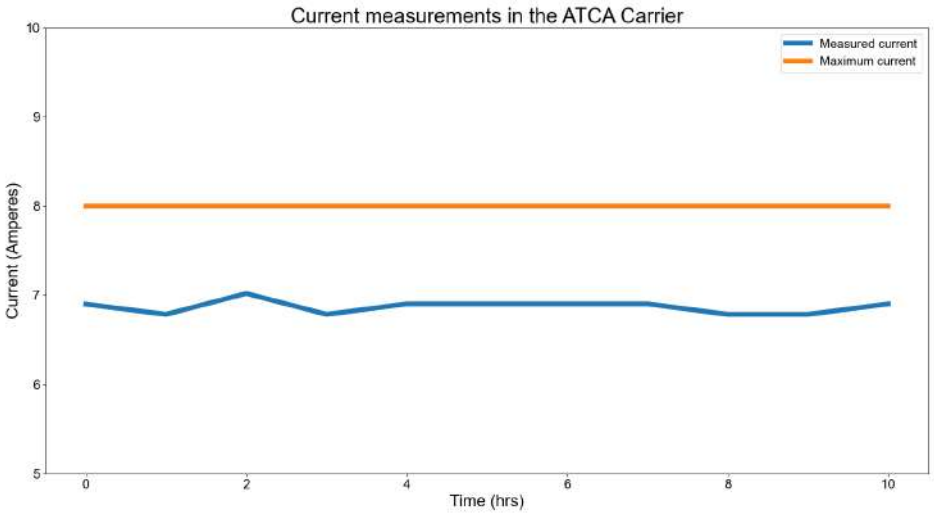


FIGURE 6.13: The ATCA carrier current monitoring results.

The software developed and used on the terminal access the IPMB bus to send requests for sensor data. As explained in Chapter 5, to access the ATCA sensors and the TilePPr Demonstrator board, the request from the shelf manager is transmitted to the IPMB and the IPMB-L to publish these data back to the shelf manager. These tools are developed in C++ and are used in conjunction with the IPMI to publish these data on the terminal. The sensor data was saved in the text files. The following sections show plots of the text files. The ROOT software tool offered by CERN is used to plot the temperature and voltage sensor data in this Section. This ROOT software tool is used in C-language to generate these plots. That is, a script written in C-language plots data from the text files and presents them as shown in the following Subsection. The test period for all sensors was 10 hours from 8:00 a.m. to 18:00 p.m.

6.3.3 ATCA carrier and TilePPr sensor monitoring results

A 2-slot ATCA Shelf [118] is used during the experimental tests with the AT8404 [119] carrier from Kontron. This Section presents the monitoring results of the sensor data acquired during the testing period. As mentioned that the tests were performed for 10 hours, Figure 6.12 shows the plots for different subsystems with sensors on the ATCA carrier. These different subsystems were measured during the testing period with temperatures ranging from 34 °C to 50 °C. These subsystems are

ADT7461 [120], BCM54680 [121] and INTEL82580 [122]. These subsystems are part of the ATCA carrier and are used to monitor the health status of the ATCA carrier. Measurements on the TilePPr Demonstrator module were also taken during the testing period. Measurements were taken from the MCP9808 [123] temperature sensor installed on the TilePPr Demonstrator module. The temperature sensor can measure from -20°C to 100°C with an accuracy of $\pm$0.5 °C. The room temperature was 23 ° C at the time of measurement. The temperature values of the MCP9808 sensor fluctuated between 40 °C to 54 °C. The ATCA carrier includes cooling fans on both sides of the ATCA shelf. These fans were off during the testing stage and no other cooling method was used during the testing period. The two fans on the ATCA shelf can also be remotely turned on and off even if the modules have not reached the threshold values. The commands were transmitted as soon as there is an increase in temperature to test the cooling of the TilePPr Demonstrator module. This can be done by using the IPMI command through the embedded Linux running on the shelf manager.

The main purpose of performing tests without cooling mechanisms is to test the threshold of all of these sensors. However, the ATCA is equipped with IPMI software that automatically switches on the cooling fans during ATCA overheating. A limited amount of processing was performed during the testing period, and the modules inside the ATCA shelf did not overheat. These were standalone tests without any integration between the on- and off-detector electronics. Figure 6.13 shows the ATCA carrier current monitoring results acquired during testing periods. The current was also measured for 10 hours of testing which ranges between 6.8 A and 7.1 A. This is the current measurement for the ATCA carrier hosting one TilePPr Demonstrator board. The TilePPr Demonstrator board consumes a maximum of 4 A and the carrier consumes a current of 4 A. Thus, the measured current is the sum of the TilePPr demonstrator module and the ATCA carrier.

Figure 6.14 shows measurements of voltages acquired from the voltage regulators on the TilePPr demonstrator module. The LTM4601A [124], LTM4618 [125], LTM4628 [126], and LTM8029 [127] voltage regulators were measured during the experiments. The LTM4601A regulates the 1.2 V, the LTM4618 regulates the 1.8 V, the LTM4628 regulates 3.3 V and the LTM8029 regulates the 5.0 V. The LT4363 [128]

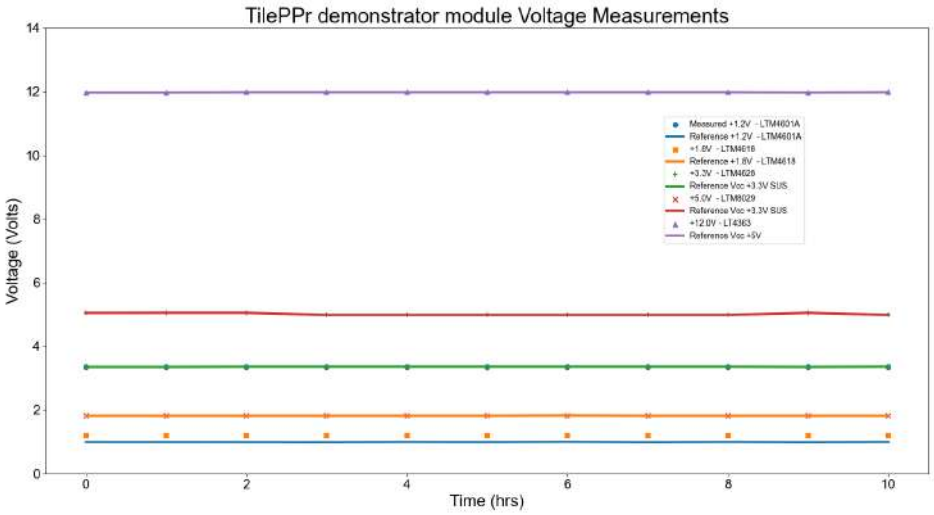


FIGURE 6.14: The TilePPr Demonstrator Voltage monitoring results.

regulates the 12 V input voltage and current consumption using the resistor connected to the LT4363 regulator.

Similarly to the ATCA carrier monitored by the ATCA Shelf Alarm Panel (SAP), the TilePPr Demonstrator module is also monitored by the SAP. If the module reaches the threshold value, the SAP LED flashes and the ATCA fans will turn on. The ATCA SAP LED monitors all modules in the ATCA shelf, including shelf managers.

Chapter 7

Conclusion

The ATLAS TileCal Phase-II Upgrade system implies the complete redesign of the on- and off-detector readout electronics in order to accommodate the current DAQ system to the new requirements for the HL-LHC. The off-detector electronics are divided into two main parts that consist of FPGA boards: TilePPr and TDAQi. As part of TilePPr, this thesis is focused on the TileCoM and Tile GbE Switch hardware, firmware, and software design. The Tile GbE Switch PCB is manufactured by two South African companies, Trax Interconnect and Jemstech. The PCBs are fully functional and have been integrated with new readout electronics. The design of the TileCoM and the Tile GbE Switch is presented in Chapter 4 of this document.

Three main functionalities are implemented in the TileCoM in software and firmware as key elements of the TDAQ and DCS of the ATLAS TileCal at the HL-LHC. The remote programming functionality is used to remotely program the MainBoard, Daughterboard, CPM, and TDAQi FPGAs. The second functionality interfaces with the on- and off-detector electronics with the TDAQ for configuration and slow control via GbE. Different calibrations runs through the TileCoM. This functionality also includes monitoring of ATCA on-board sensors, CPM sensors, and on-detector electronics, and configuration of the ATCA carrier and CPMs. Lastly, the third functionality involves an implementation of the communication between the TilePPr and the DCS. Two OPCUA servers are implemented on the TileCoM to read out sensor data from the on- and off-detector electronics. All these functionalities have been successfully implemented on the TileCoM. In the final application, approximately 2,000 sensors from the on-detector electronics are monitored by each TileCoM module.

A testbench used during the test stage includes one TileCal GbE Switch, one network router, one Avnet Ultra96-V2 Zynq UltraScale+ MPSoC TileCoM evaluation board, and one Xilinx VC707 evaluation board as a CPM emulator. The network router is used to provide external access to all the boards that integrate the testbench. The TileCal GbE Switch is used as an interface for interconnecting all TilePPr modules. The Avnet Ultra96-V2 Zynq UltraScale+ MPSoC TileCoM evaluation board is connected to the computer via UART to display the embedded Linux terminal and control different applications developed for TileCoM.

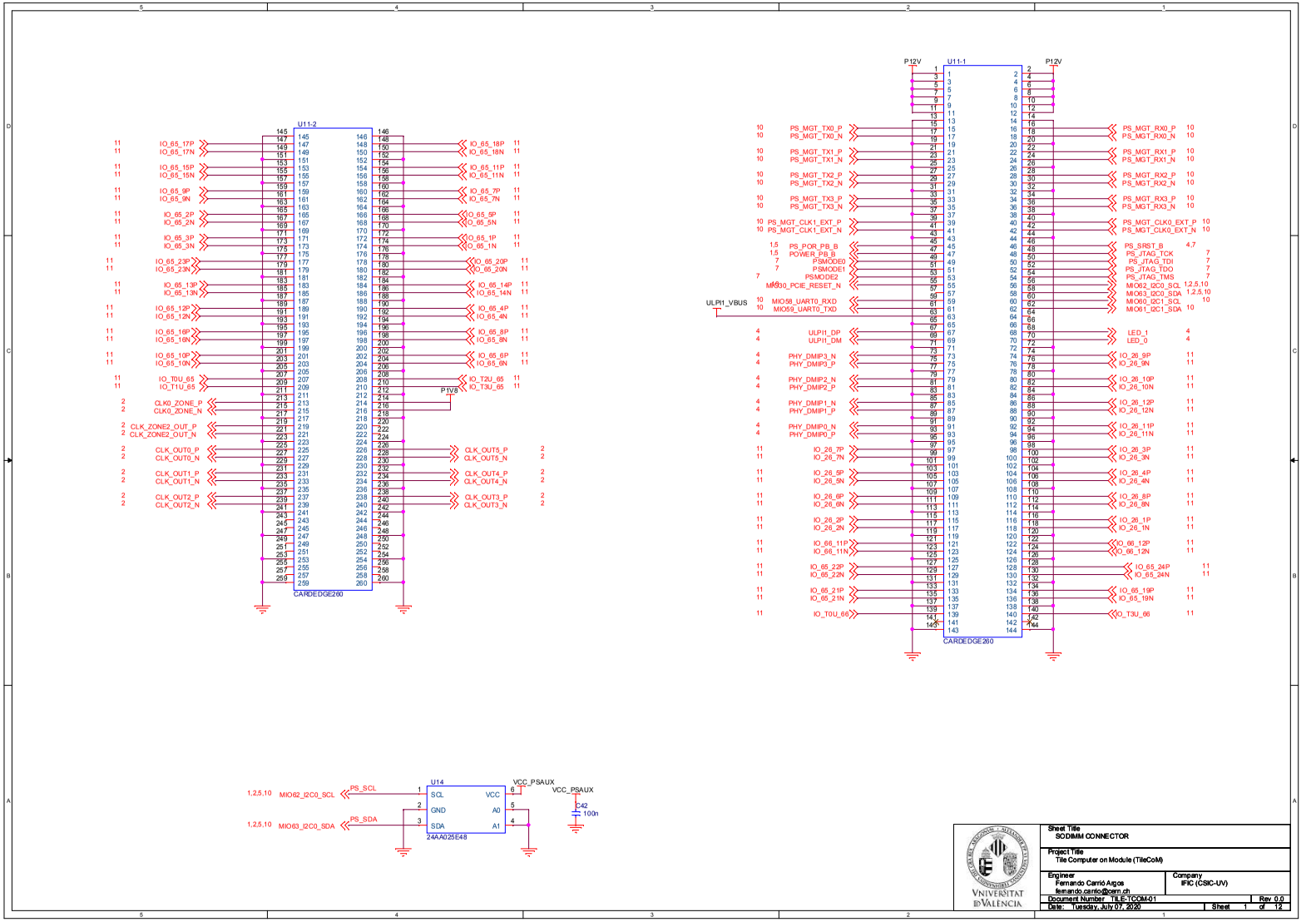
The results of the main TileCoM functionalities include plots to show the sensor data results. The TilePPr and DCS integration has been successfully tested where sensor results are acquired by the OPC UA and SCADA system. These results are presented in graphs in Chapter 6. All main functionalities are successfully implemented on the Avnet Ultra96-V2 Zynq UltraScale+ MPSoC TileCoM evaluation board. In this thesis, a project on ATCA preparation is also presented. Three main objectives were achieved on this project which are: to visualize in real-time the state of the ATCA shelf boards, sensors and alarms; to send configuration commands via the IPMI hardware management port to the TilePPr Demonstrator inserted in the carrier; and to keep historical records of the performance (power consumption, communication links failure, temperature, etc..) of different boards.

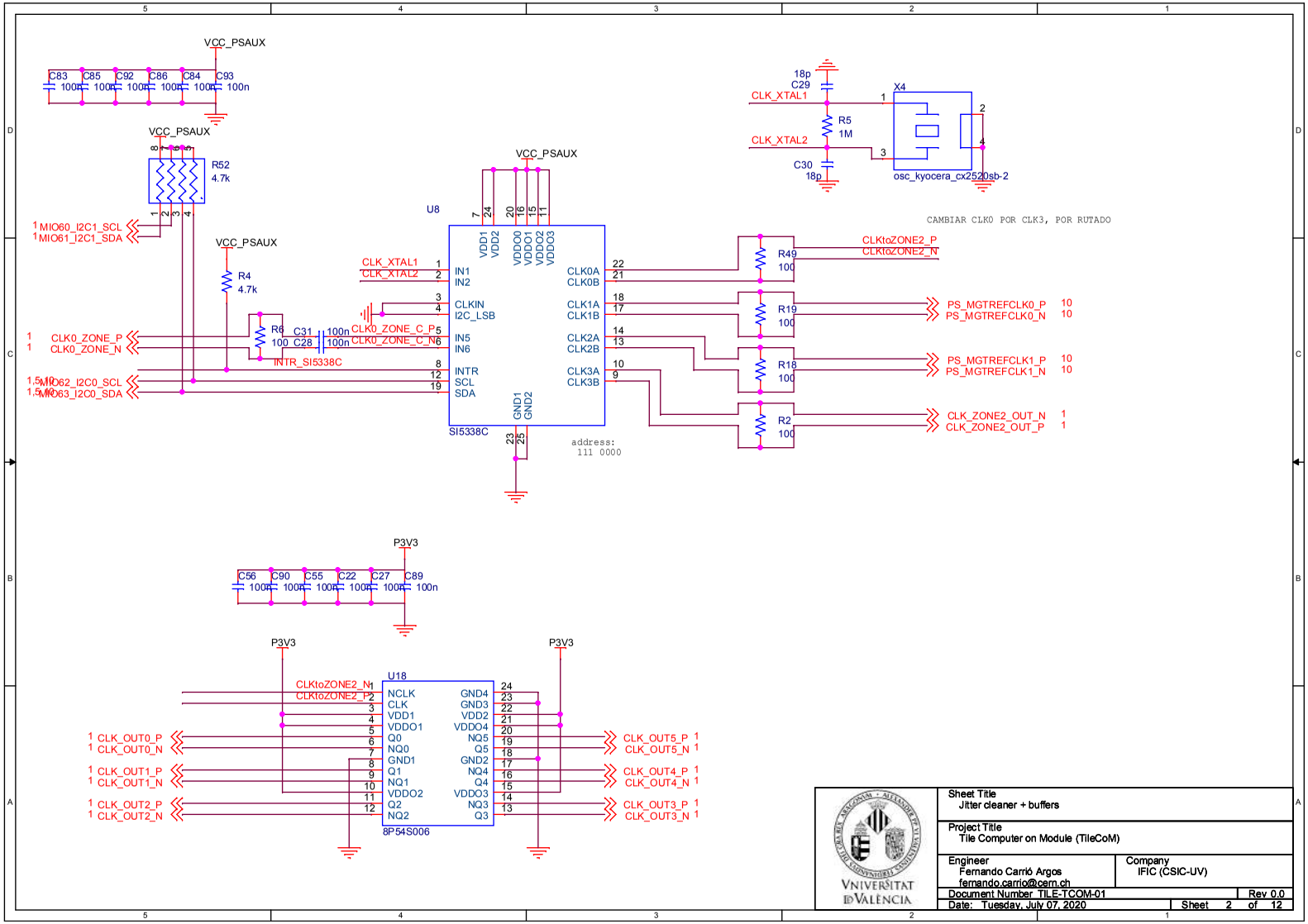
Future work involves the installation of the TileCoM in the ATCA for the demonstrator project. The plan is to remotely program the on- and off-detector electronics of the demonstrator project; integrate TilePPr with DCS and TDAQ system through version 1 of the TileCoM.

Appendix A

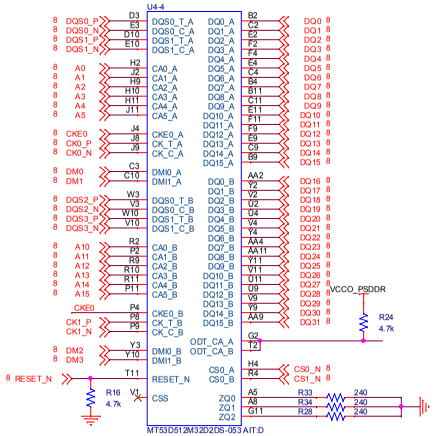
TileCoM Schematic design

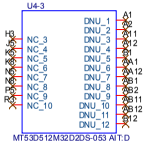
As introduced in Chapter 4, the TileCoM design is one of the main contributions of this thesis. The PCB layout presented in Chapter 4 is a result of the TileCoM schematic shown in this Appendix. This schematic shows the connection of all the components used in the design of the TileCoM.

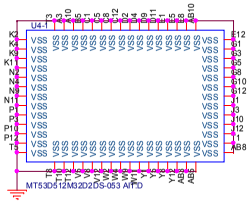

U11-2
CARDEDGE260
U11-1
CARDEDGE260
P12V
P12V
P1V8
ULPI1_VBUS
U14
24AA025E48
VCC_PSAUX
VCC_PSAUX
C42
100n
PS_SCL
PS_SDA
SCL
SDA
GND
VCC
A0
A1
Sheet Title
SODIMM CONNECTOR
Project Title
Tile Computer on Module (TileCoM)
Engineer
Fernando Carrió Argos
fernando.carrio@ific.uv.es
Company
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
Rev 0.0
Date: Tuesday, July 07, 2020
Sheet 1 of 12

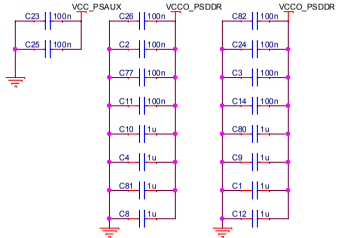


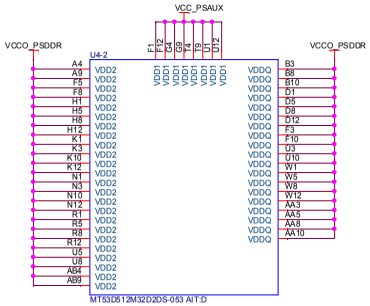
Sheet Title	Jitter cleaner + buffers
Project Title	Tile Computer on Module (TileCoM)
Engineer	Fernando Carrió Argos fernando.carrio@cern.ch
Company	IFIC (CSIC-UV)
Document Number	TILE-TCOM-01
Rev	0.0
Date:	Tuesday, July 07, 2020
Sheet	2 of 12



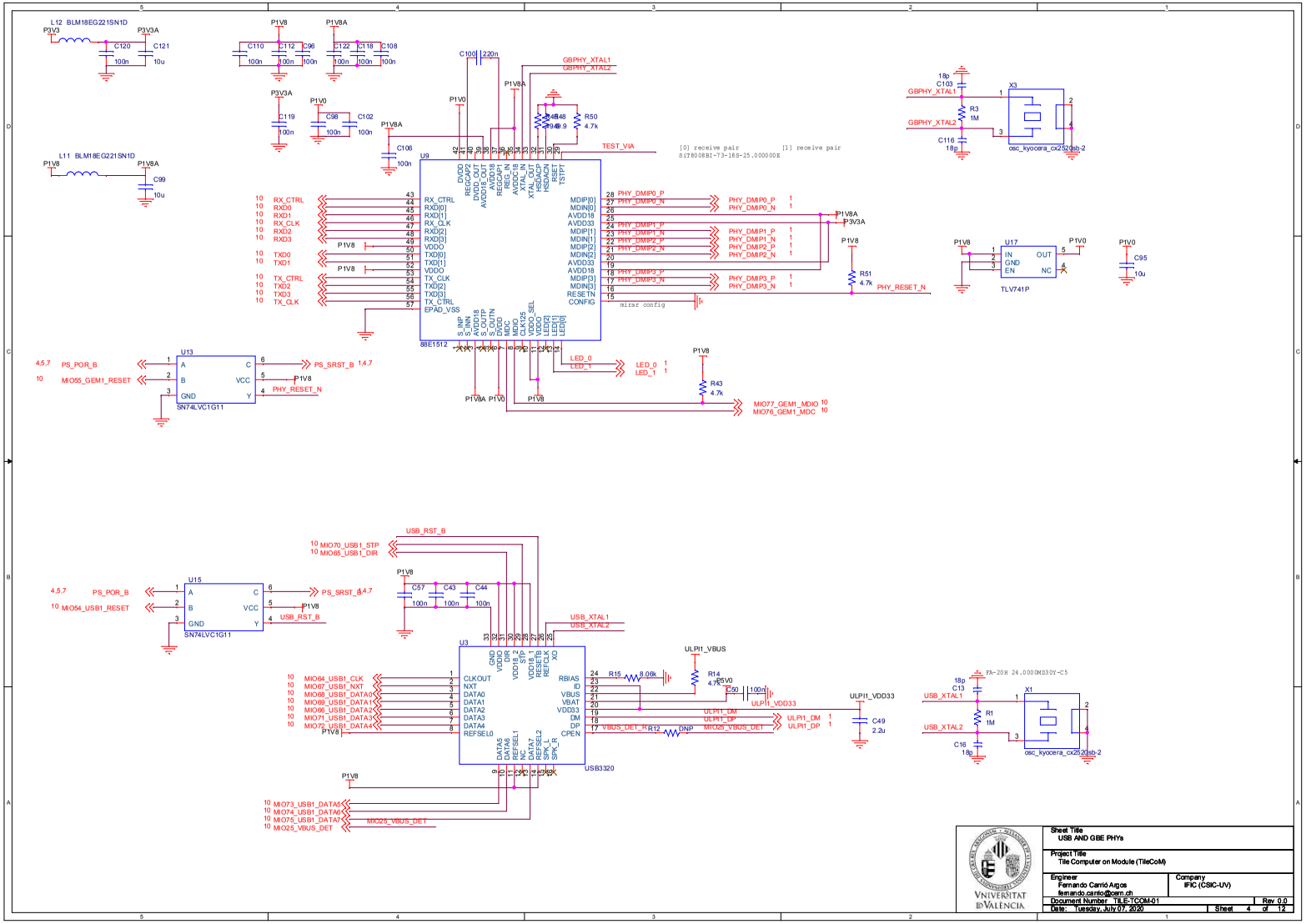








Sheet Title: DDR4 MEMORY	
Project Title: Tile Computer on Module (TileCoM)	
Engineer: Fernando Carrió Argos fernando.carrio@cern.ch	Company: IFIC (CSIC-UV)
Document Number: TILE-TCOM-01	Rev: 0.0
Date: Tuesday, July 07, 2020	Sheet 3 of 12


L12 BLM18EG221SN1D
L11 BLM18EG221SN1D
U9
88E1512
U13
SN74LVC1G11
U15
SN74LVC1G11
U3
USB3320
U17
TLV741P
X3
osc_kyocera_cx2520sb-2
X1
osc_kyocera_cx2520sb-2
TEST_VIA
PS_POR_B
PS_SRST_B
PHY_RESET_N
MIO55_GEM1_RESET
MIO54_USB1_RESET
USB_RST_B
GBPHY_XTAL1
GBPHY_XTAL2
USB_XTAL1
USB_XTAL2
ULPI1_VBUS
ULPI1_VDD33
MIO77_GEM1_MDIO
MIO76_GEM1_MDC
MIO25_VBUS_DET
Sheet Title
USB AND GBE PHYs
Project Title
Tile Computer on Module (TileCoM)
Engineer
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Company
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
Rev 0.0
Date: Tuesday, July 07, 2020
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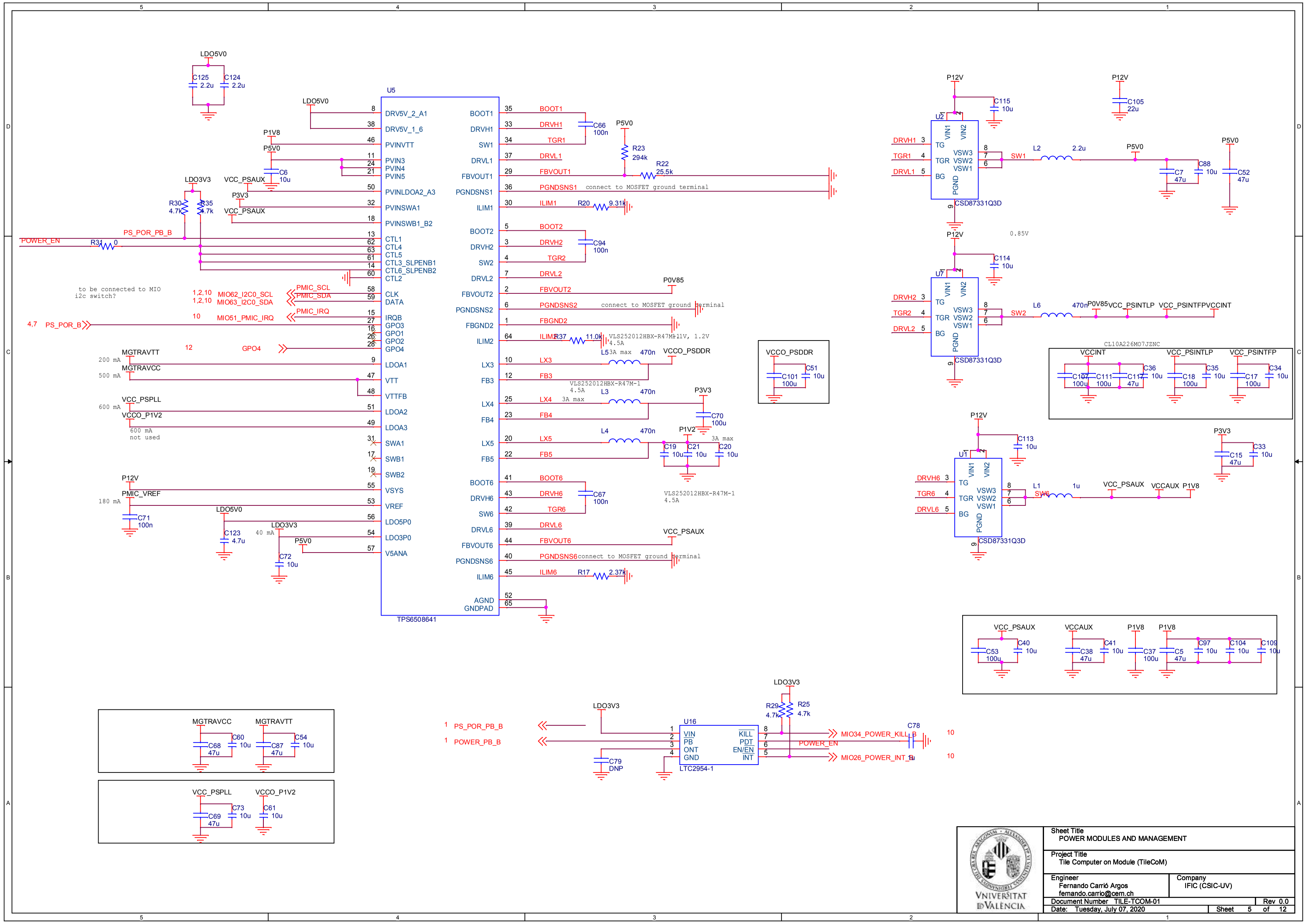
Sheet Title
POWER MODULES AND MANAGEMENT
Project Title
Tile Computer on Module (TileCoM)
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Company
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
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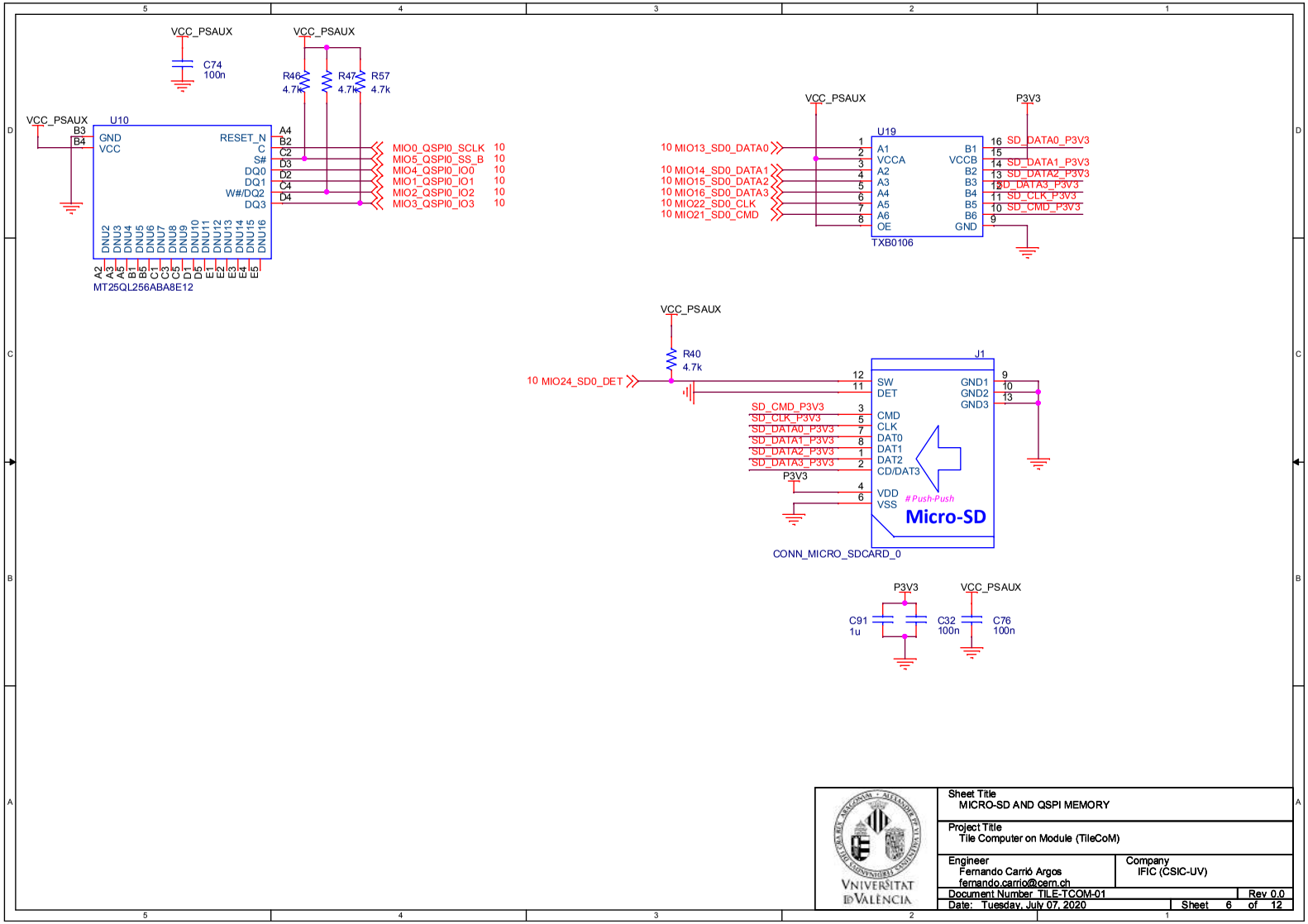
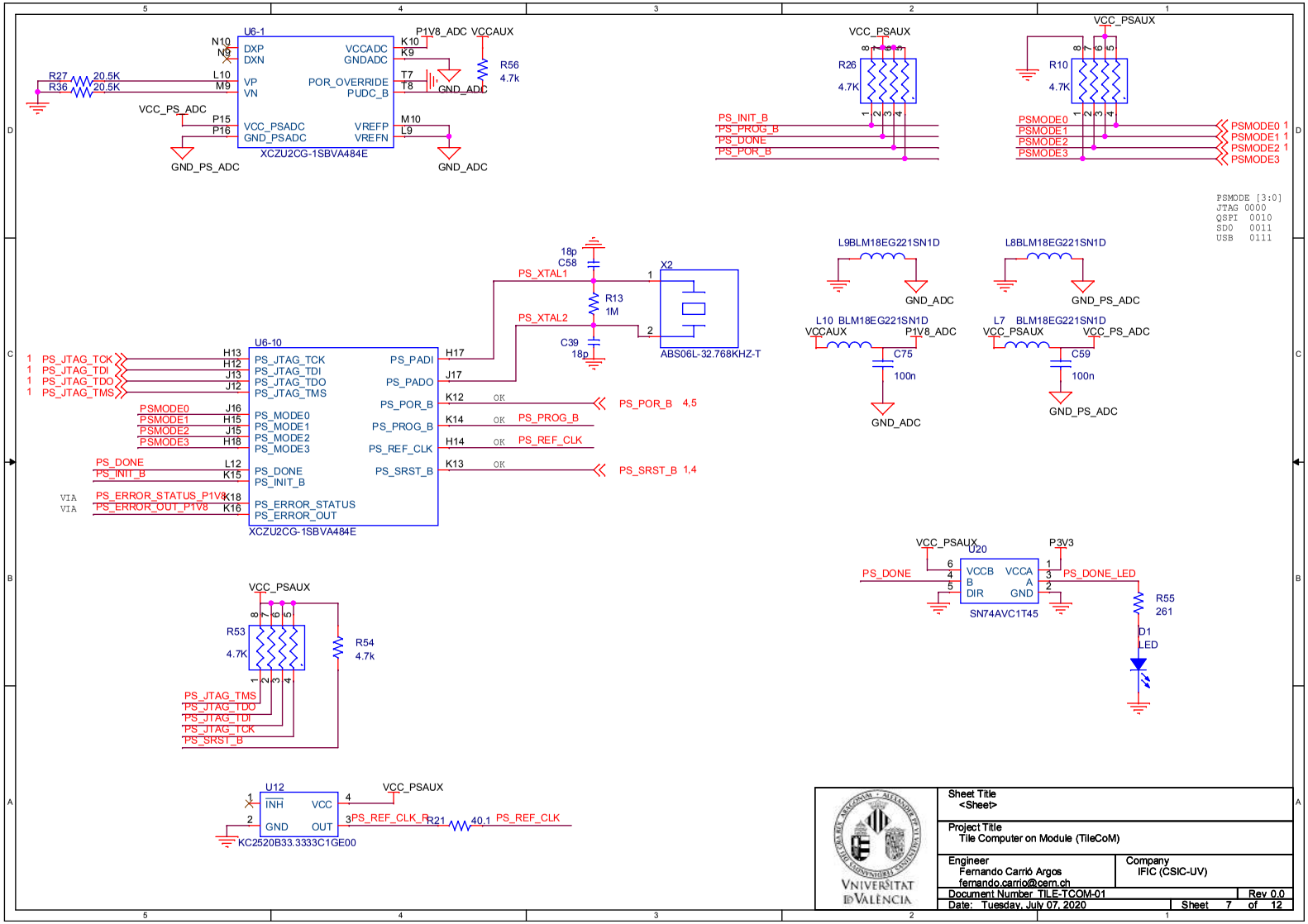
Date: Tuesday, July 07, 2020
Sheet 5 of 12
VNIVERSITAT DE VALÈNCIA
U5
TPS6508641
U2
U7
U1
CSD87331Q3D
U16
LTC2954-1
VCCO_PSDDR
VCC_PSAUX
VCCAUX
P1V8
MGTRAVCC
MGTRAVTT
VCC_PSPLL
VCCO_P1V2
VCCINT
VCC_PSINTLP
VCC_PSINTFP
POWER_EN
PS_POR_PB_B
POWER_PB_B
MIO34_POWER_KILL_B
MIO26_POWER_INT_B
MIO62_I2C0_SCL
MIO63_I2C0_SDA
MIO51_PMIC_IRQ
PS_POR_B
GPO4
to be connected to MIO
i2c switch?
connect to MOSFET ground terminal



Sheet Title	MICRO-SD AND QSPI MEMORY
Project Title	Tile Computer on Module (TileCoM)
Engineer	Fernando Carrió Argos fernando.carrio@cern.ch
Company	IFIC (CSIC-UV)
Document Number	TILE-TCOM-01
Rev	0.0
Date:	Tuesday, July 07, 2020
Sheet	6 of 12


U6-1
XCZU2CG-1SBVA484E
P1V8_ADC
VCCAUX
R56
4.7k
R27
R36
20.5K
20.5K
VCC_PS_ADC
GND_PS_ADC
GND_ADC
VCC_PSAUX
R26
4.7K
PS_INIT_B
PS_PROG_B
PS_DONE
PS_POR_B
R10
PSMODE0
PSMODE1
PSMODE2
PSMODE3
PSMODE [3:0]
JTAG 0000
QSPI 0010
SD0 0011
USB 0111
U6-10
XCZU2CG-1SBVA484E
PS_JTAG_TCK
PS_JTAG_TDI
PS_JTAG_TDO
PS_JTAG_TMS
PS_MODE0
PS_MODE1
PS_MODE2
PS_MODE3
PS_DONE
PS_INIT_B
PS_ERROR_STATUS
PS_ERROR_OUT
PS_PADI
PS_PADO
PS_POR_B
PS_PROG_B
PS_REF_CLK
PS_SRST_B
18p
C58
C39
18p
PS_XTAL1
PS_XTAL2
R13
1M
X2
ABS06L-32.768KHZ-T
L9BLM18EG221SN1D
L8BLM18EG221SN1D
L10 BLM18EG221SN1D
L7 BLM18EG221SN1D
C75
100n
C59
100n
U20
SN74AVC1T45
P3V3
PS_DONE_LED
R55
261
D1
LED
R53
R54
4.7k
U12
KC2520B33.3333C1GE00
PS_REF_CLK_R
R21
40.1
PS_REF_CLK
Sheet Title
<Sheet>
Project Title
Tile Computer on Module (TileCoM)
Engineer
Fernando Carrió Argos
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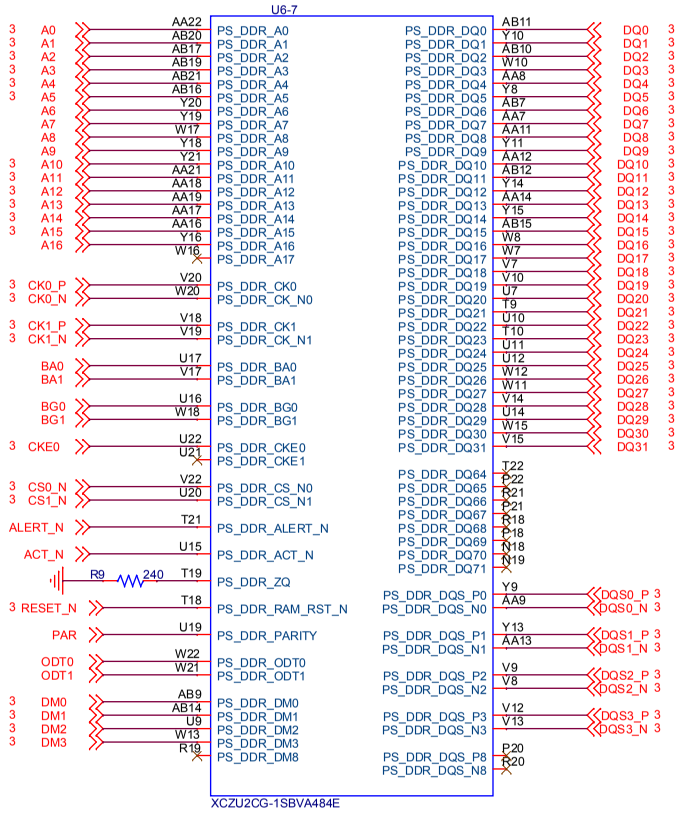
Company
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
Rev 0.0
Date: Tuesday, July 07, 2020
Sheet 7 of 12



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Sheet Title
ZYNQ PS DDR BANK

Project Title
Tile Computer on Module (TileCoM)

Engineer
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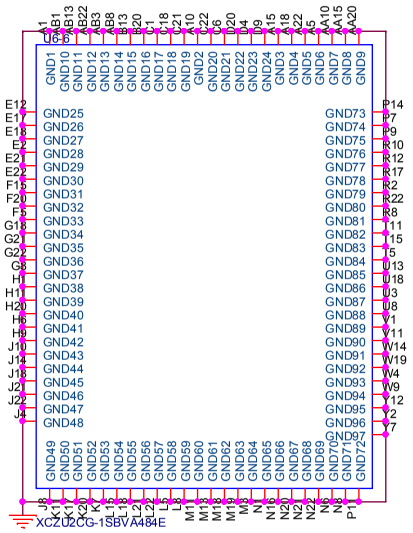
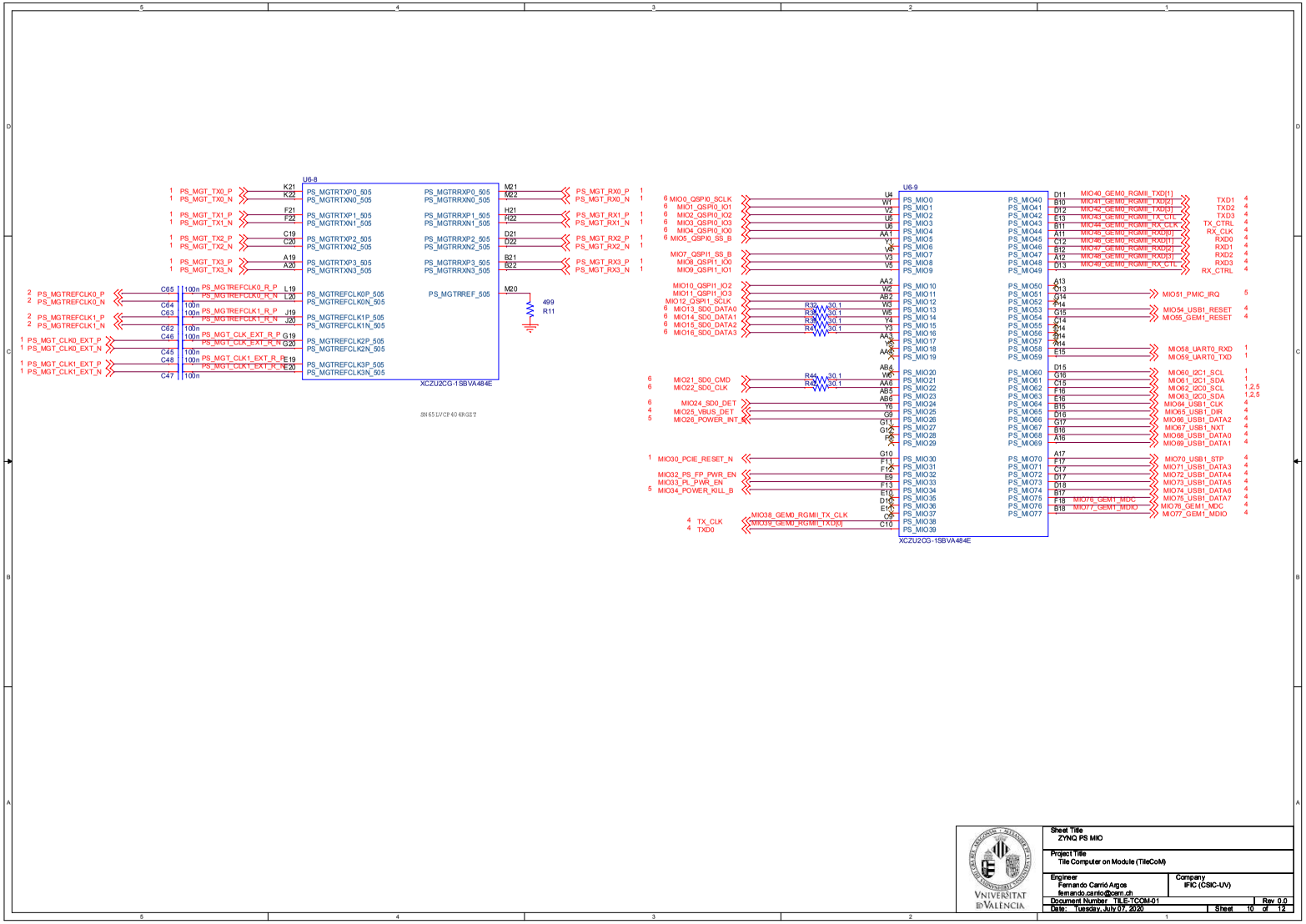
Company
IFIC (CSIC-UV)

Document Number TILE-TCOM-01 Rev 0.0

Date: Tuesday, July 07, 2020 Sheet 8 of 12



Sheet Title	<Sheet>
Project Title	Tile Computer on Module (TileCoM)
Engineer	Fernando Carrió Argos fernando.carrio@cern.ch
Company	IFIC (CSIC-UV)
Document Number	TILE-TCOM-01
Rev	0.0
Date:	Tuesday, July 07, 2020
Sheet	9 of 12


U6-8
XCZU2CG-1SBVA484E
U6-9
XCZU2CG-1SBVA484E
PS_MGTRREF_505
499
R11
SN65LVCP404RGZT
Sheet Title
ZYNQ PS MIO
Project Title
Tile Computer on Module (TileCoM)
Engineer
Fernando Carrió Argos
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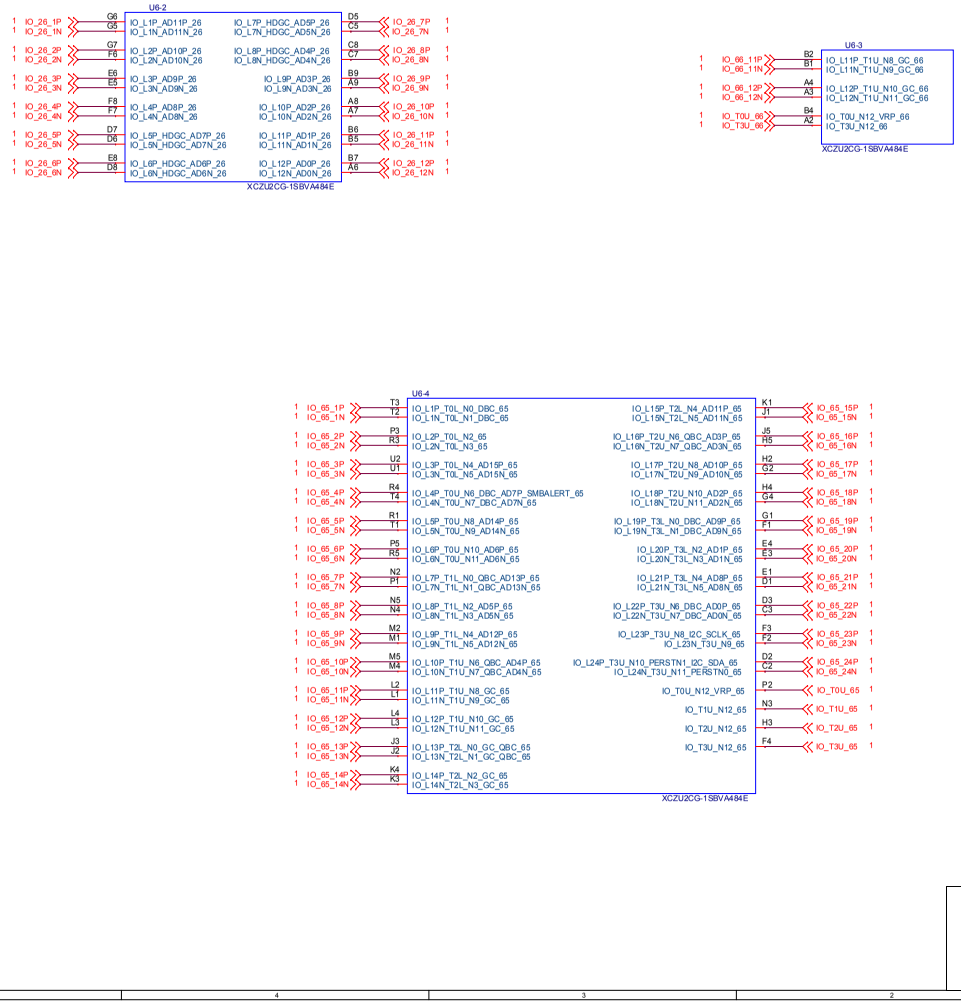
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
Rev 0.0
Date: Tuesday, July 07, 2020
Sheet 10 of 12


U6-2
IO_26_1P
IO_26_1N
IO_26_2P
IO_26_2N
IO_26_3P
IO_26_3N
IO_26_4P
IO_26_4N
IO_26_5P
IO_26_5N
IO_26_6P
IO_26_6N
G6
G5
G7
F6
E6
E5
F8
F7
D7
D6
E8
D8
IO_L1P_AD11P_26
IO_L1N_AD11N_26
IO_L2P_AD10P_26
IO_L2N_AD10N_26
IO_L3P_AD9P_26
IO_L3N_AD9N_26
IO_L4P_AD8P_26
IO_L4N_AD8N_26
IO_L5P_HDGC_AD7P_26
IO_L5N_HDGC_AD7N_26
IO_L6P_HDGC_AD6P_26
IO_L6N_HDGC_AD6N_26
IO_L7P_HDGC_AD5P_26
IO_L7N_HDGC_AD5N_26
IO_L8P_HDGC_AD4P_26
IO_L8N_HDGC_AD4N_26
IO_L9P_AD3P_26
IO_L9N_AD3N_26
IO_L10P_AD2P_26
IO_L10N_AD2N_26
IO_L11P_AD1P_26
IO_L11N_AD1N_26
IO_L12P_AD0P_26
IO_L12N_AD0N_26
D5
C5
C8
C7
B9
A9
A8
A7
B6
B5
B7
A6
IO_26_7P
IO_26_7N
IO_26_8P
IO_26_8N
IO_26_9P
IO_26_9N
IO_26_10P
IO_26_10N
IO_26_11P
IO_26_11N
IO_26_12P
IO_26_12N
XCZU2CG-1SBVA484E
U6-3
IO_66_11P
IO_66_11N
IO_66_12P
IO_66_12N
IO_T0U_66
IO_T3U_66
B2
B1
A4
A3
B4
A2
IO_L11P_T1U_N8_GC_66
IO_L11N_T1U_N9_GC_66
IO_L12P_T1U_N10_GC_66
IO_L12N_T1U_N11_GC_66
IO_T0U_N12_VRP_66
IO_T3U_N12_66
XCZU2CG-1SBVA484E
U6-4
IO_65_1P
IO_65_1N
IO_65_2P
IO_65_2N
IO_65_3P
IO_65_3N
IO_65_4P
IO_65_4N
IO_65_5P
IO_65_5N
IO_65_6P
IO_65_6N
IO_65_7P
IO_65_7N
IO_65_8P
IO_65_8N
IO_65_9P
IO_65_9N
IO_65_10P
IO_65_10N
IO_65_11P
IO_65_11N
IO_65_12P
IO_65_12N
IO_65_13P
IO_65_13N
IO_65_14P
IO_65_14N
T3
T2
P3
R3
U2
U1
R4
T4
R1
T1
P5
R5
N2
P1
N5
N4
M2
M1
M5
M4
L2
L1
L4
L3
J3
J2
K4
K3
IO_L1P_T0L_N0_DBC_65
IO_L1N_T0L_N1_DBC_65
IO_L2P_T0L_N2_65
IO_L2N_T0L_N3_65
IO_L3P_T0L_N4_AD15P_65
IO_L3N_T0L_N5_AD15N_65
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65
IO_L4N_T0U_N7_DBC_AD7N_65
IO_L5P_T0U_N8_AD14P_65
IO_L5N_T0U_N9_AD14N_65
IO_L6P_T0U_N10_AD6P_65
IO_L6N_T0U_N11_AD6N_65
IO_L7P_T1L_N0_QBC_AD13P_65
IO_L7N_T1L_N1_QBC_AD13N_65
IO_L8P_T1L_N2_AD5P_65
IO_L8N_T1L_N3_AD5N_65
IO_L9P_T1L_N4_AD12P_65
IO_L9N_T1L_N5_AD12N_65
IO_L10P_T1U_N6_QBC_AD4P_65
IO_L10N_T1U_N7_QBC_AD4N_65
IO_L11P_T1U_N8_GC_65
IO_L11N_T1U_N9_GC_65
IO_L12P_T1U_N10_GC_65
IO_L12N_T1U_N11_GC_65
IO_L13P_T2L_N0_GC_QBC_65
IO_L13N_T2L_N1_GC_QBC_65
IO_L14P_T2L_N2_GC_65
IO_L14N_T2L_N3_GC_65
IO_L15P_T2L_N4_AD11P_65
IO_L15N_T2L_N5_AD11N_65
IO_L16P_T2U_N6_QBC_AD3P_65
IO_L16N_T2U_N7_QBC_AD3N_65
IO_L17P_T2U_N8_AD10P_65
IO_L17N_T2U_N9_AD10N_65
IO_L18P_T2U_N10_AD2P_65
IO_L18N_T2U_N11_AD2N_65
IO_L19P_T3L_N0_DBC_AD9P_65
IO_L19N_T3L_N1_DBC_AD9N_65
IO_L20P_T3L_N2_AD1P_65
IO_L20N_T3L_N3_AD1N_65
IO_L21P_T3L_N4_AD8P_65
IO_L21N_T3L_N5_AD8N_65
IO_L22P_T3U_N6_DBC_AD0P_65
IO_L22N_T3U_N7_DBC_AD0N_65
IO_L23P_T3U_N8_I2C_SCLK_65
IO_L23N_T3U_N9_65
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65
IO_L24N_T3U_N11_PERSTN0_65
IO_T0U_N12_VRP_65
IO_T1U_N12_65
IO_T2U_N12_65
IO_T3U_N12_65
K1
J1
J5
H5
H2
G2
H4
G4
G1
F1
E4
E3
E1
D1
D3
C3
F3
F2
D2
C2
P2
N3
H3
F4
IO_65_15P
IO_65_15N
IO_65_16P
IO_65_16N
IO_65_17P
IO_65_17N
IO_65_18P
IO_65_18N
IO_65_19P
IO_65_19N
IO_65_20P
IO_65_20N
IO_65_21P
IO_65_21N
IO_65_22P
IO_65_22N
IO_65_23P
IO_65_23N
IO_65_24P
IO_65_24N
IO_T0U_65
IO_T1U_65
IO_T2U_65
IO_T3U_65
XCZU2CG-1SBVA484E
VNIVERSITAT DE VALÈNCIA
Sheet Title
ZYNQ PL IO
Project Title
Tile Computer on Module (TileCoM)
Engineer
Fernando Carrió Argos
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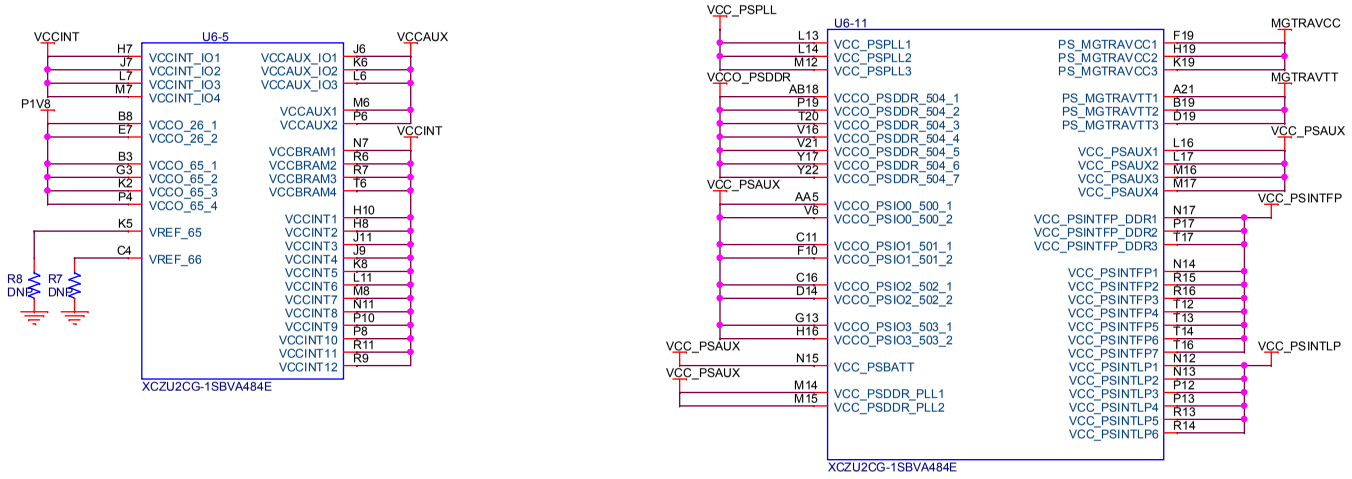
Company
IFIC (CSIC-UV)
Document Number TILE-TCOM-01
Rev 0.0
Date: Tuesday, July 07, 2020
Sheet 11 of 12



Sheet Title	ZYNQ POWER
Project Title	Tile Computer on Module (TileCoM)
Engineer	Fernando Carrió Argos fernando.carrio@cern.ch
Company	IFIC (CSIC-UV)
Document Number	TILE-TCOM-01
Rev	0.0
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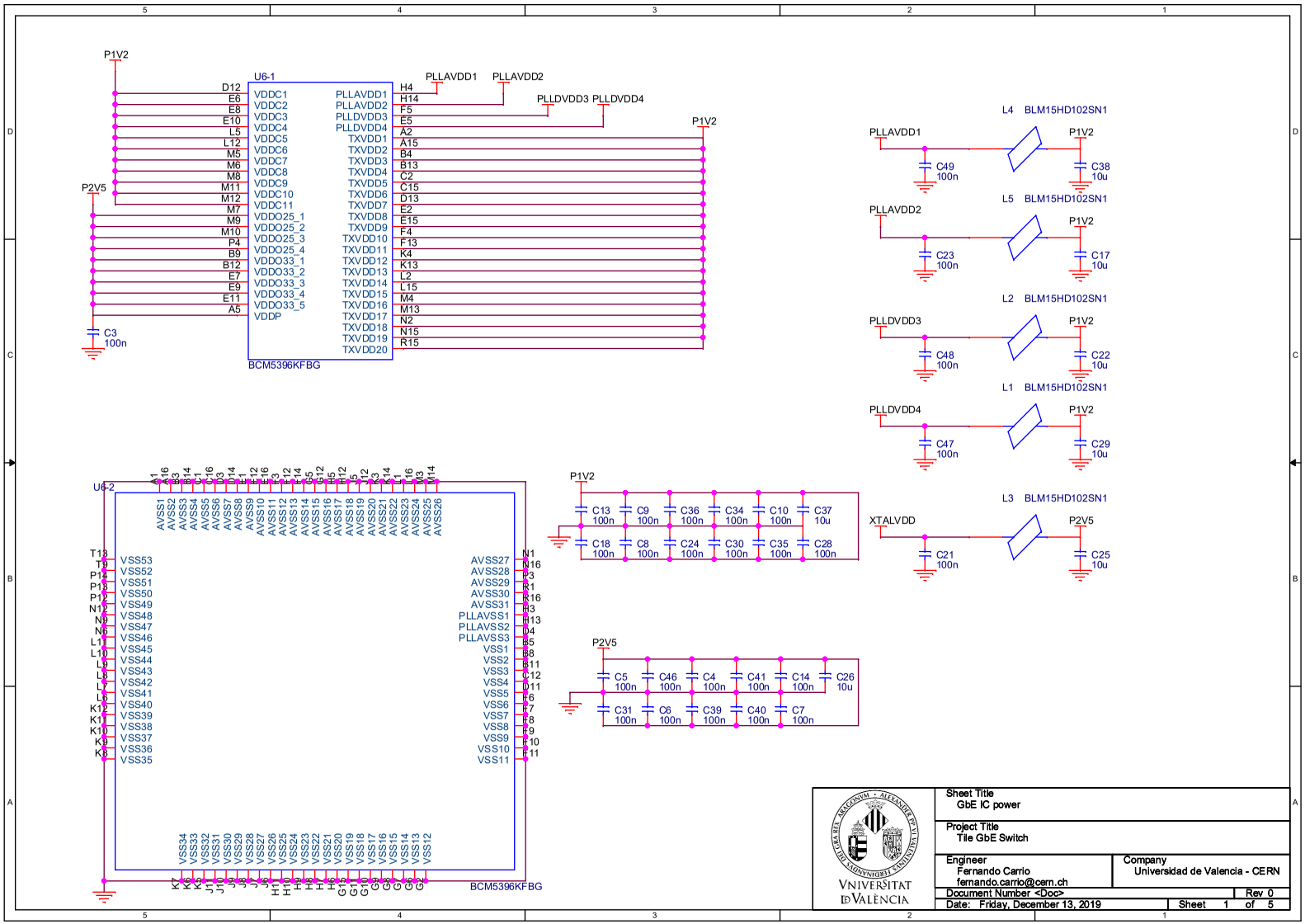
Appendix B

Tile GbE Switch Schematic design

Similarly to the TileCoM, the Tile GbE Switch design is also one of the main contributions of this thesis. The PCB layout presented in Chapter 4 is a result of the TileCoM schematic shown in this Appendix. This schematic shows the connection of all the components used in the design of the Tile GbE Switch.


P1V2
U6-1
PLLAVDD1
PLLAVDD2
PLLDVDD3
PLLDVDD4
P1V2
P2V5
C3
100n
BCM5396KFBG
L4 BLM15HD102SN1
PLLAVDD1
C49
100n
P1V2
C38
10u
L5 BLM15HD102SN1
PLLAVDD2
C23
100n
P1V2
C17
10u
L2 BLM15HD102SN1
PLLDVDD3
C48
100n
P1V2
C22
10u
L1 BLM15HD102SN1
PLLDVDD4
C47
100n
P1V2
C29
10u
L3 BLM15HD102SN1
XTALVDD
C21
100n
P2V5
C25
10u
U6-2
P1V2
C13 C9 C36 C34 C10 C37
C18 C8 C24 C30 C35 C28
100n
10u
P2V5
C5 C46 C4 C41 C14 C26
C31 C6 C39 C40 C7
100n
10u
BCM5396KFBG
Sheet Title
GbE IC power
Project Title
Tile GbE Switch
Engineer
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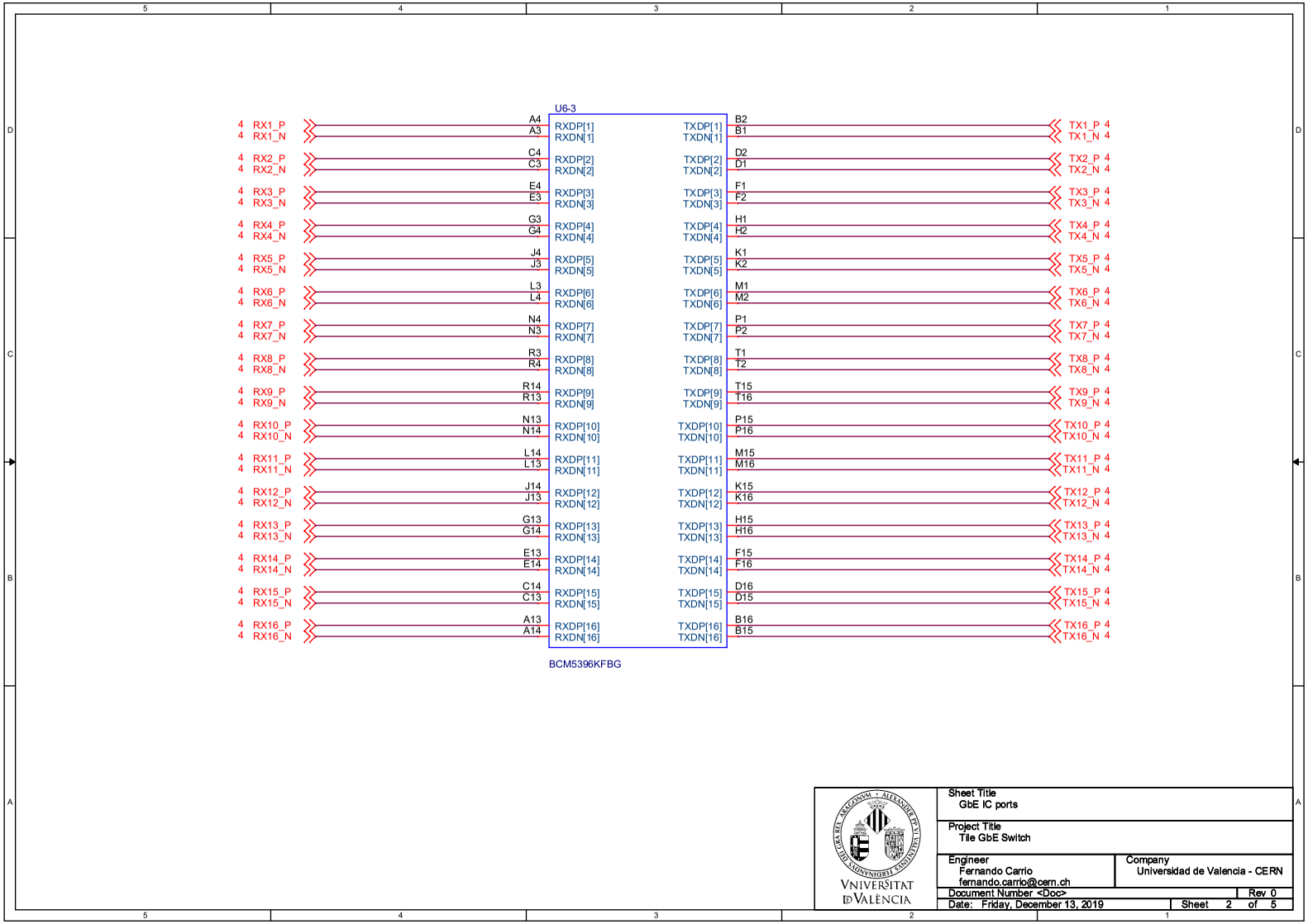
Company
Universidad de Valencia - CERN
Document Number <Doc>
Rev 0
Date: Friday, December 13, 2019
Sheet 1 of 5


U6-3
4 RX1_P
4 RX1_N
A4
A3
RXDP[1]
RXDN[1]
TXDP[1]
TXDN[1]
B2
B1
TX1_P 4
TX1_N 4
4 RX2_P
4 RX2_N
C4
C3
RXDP[2]
RXDN[2]
TXDP[2]
TXDN[2]
D2
D1
TX2_P 4
TX2_N 4
4 RX3_P
4 RX3_N
E4
E3
RXDP[3]
RXDN[3]
TXDP[3]
TXDN[3]
F1
F2
TX3_P 4
TX3_N 4
4 RX4_P
4 RX4_N
G3
G4
RXDP[4]
RXDN[4]
TXDP[4]
TXDN[4]
H1
H2
TX4_P 4
TX4_N 4
4 RX5_P
4 RX5_N
J4
J3
RXDP[5]
RXDN[5]
TXDP[5]
TXDN[5]
K1
K2
TX5_P 4
TX5_N 4
4 RX6_P
4 RX6_N
L3
L4
RXDP[6]
RXDN[6]
TXDP[6]
TXDN[6]
M1
M2
TX6_P 4
TX6_N 4
4 RX7_P
4 RX7_N
N4
N3
RXDP[7]
RXDN[7]
TXDP[7]
TXDN[7]
P1
P2
TX7_P 4
TX7_N 4
4 RX8_P
4 RX8_N
R3
R4
RXDP[8]
RXDN[8]
TXDP[8]
TXDN[8]
T1
T2
TX8_P 4
TX8_N 4
4 RX9_P
4 RX9_N
R14
R13
RXDP[9]
RXDN[9]
TXDP[9]
TXDN[9]
T15
T16
TX9_P 4
TX9_N 4
4 RX10_P
4 RX10_N
N13
N14
RXDP[10]
RXDN[10]
TXDP[10]
TXDN[10]
P15
P16
TX10_P 4
TX10_N 4
4 RX11_P
4 RX11_N
L14
L13
RXDP[11]
RXDN[11]
TXDP[11]
TXDN[11]
M15
M16
TX11_P 4
TX11_N 4
4 RX12_P
4 RX12_N
J14
J13
RXDP[12]
RXDN[12]
TXDP[12]
TXDN[12]
K15
K16
TX12_P 4
TX12_N 4
4 RX13_P
4 RX13_N
G13
G14
RXDP[13]
RXDN[13]
TXDP[13]
TXDN[13]
H15
H16
TX13_P 4
TX13_N 4
4 RX14_P
4 RX14_N
E13
E14
RXDP[14]
RXDN[14]
TXDP[14]
TXDN[14]
F15
F16
TX14_P 4
TX14_N 4
4 RX15_P
4 RX15_N
C14
C13
RXDP[15]
RXDN[15]
TXDP[15]
TXDN[15]
D16
D15
TX15_P 4
TX15_N 4
4 RX16_P
4 RX16_N
A13
A14
RXDP[16]
RXDN[16]
TXDP[16]
TXDN[16]
B16
B15
TX16_P 4
TX16_N 4
BCM5396KFBG
VNIVERSITAT DE VALÈNCIA
Sheet Title
GbE IC ports
Project Title
Tile GbE Switch
Engineer
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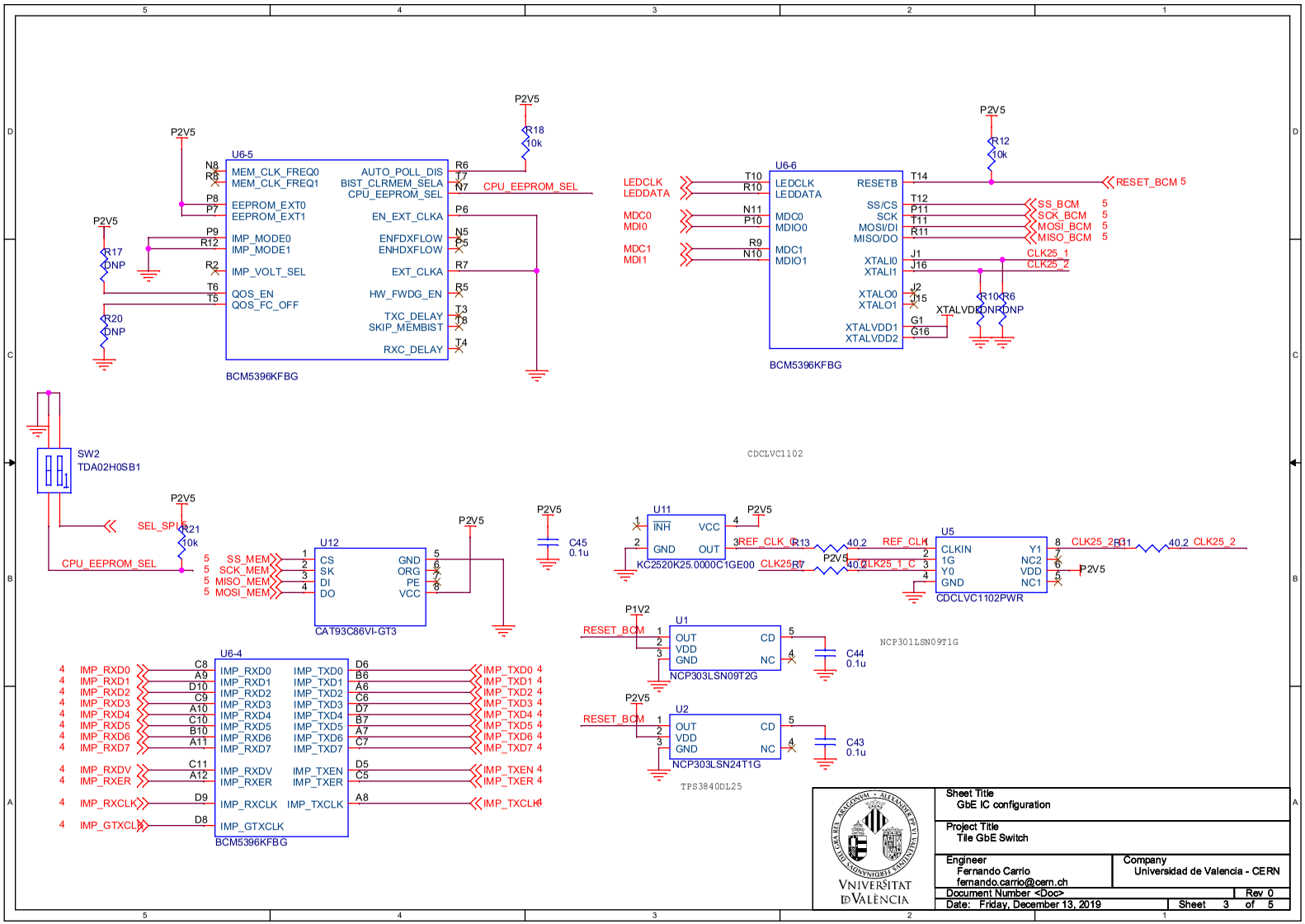
Company
Universidad de Valencia - CERN
Document Number <Doc>
Rev 0
Date: Friday, December 13, 2019
Sheet 2 of 5


U6-5
BCM5396KFBG
MEM_CLK_FREQ0
MEM_CLK_FREQ1
EEPROM_EXT0
EEPROM_EXT1
IMP_MODE0
IMP_MODE1
IMP_VOLT_SEL
QOS_EN
QOS_FC_OFF
AUTO_POLL_DIS
BIST_CLRMEM_SELA
CPU_EEPROM_SEL
EN_EXT_CLKA
ENFDXFLOW
ENHDXFLOW
EXT_CLKA
HW_FWDG_EN
TXC_DELAY
SKIP_MEMBIST
RXC_DELAY
CPU_EEPROM_SEL
P2V5
R18
10k
R17
DNP
R20
DNP
U6-6
BCM5396KFBG
LEDCLK
LEDDATA
MDC0
MDI0
MDC1
MDI1
RESETB
SS/CS
SCK
MOSI/DI
MISO/DO
XTALI0
XTALI1
XTALO0
XTALO1
XTALVDD1
XTALVDD2
RESET_BCM
SS_BCM
SCK_BCM
MOSI_BCM
MISO_BCM
CLK25_1
CLK25_2
R12
10k
R10
R6
DNP
XTALVDD
SW2
TDA02H0SB1
SEL_SPI
R21
10k
CPU_EEPROM_SEL
U12
CAT93C86VI-GT3
CS
SK
DI
DO
GND
ORG
PE
VCC
SS_MEM
SCK_MEM
MISO_MEM
MOSI_MEM
C45
0.1u
CDCLVC1102
U11
KC2520K25.0000C1GE00
INH
GND
VCC
OUT
REF_CLK
CLK25R
U5
CDCLVC1102PWR
CLKIN
1G
Y0
GND
Y1
NC2
VDD
NC1
CLK25_2R
CLK25_1_C
U6-4
BCM5396KFBG
IMP_RXD0
IMP_RXD1
IMP_RXD2
IMP_RXD3
IMP_RXD4
IMP_RXD5
IMP_RXD6
IMP_RXD7
IMP_RXDV
IMP_RXER
IMP_RXCLK
IMP_GTXCLK
IMP_TXD0
IMP_TXD1
IMP_TXD2
IMP_TXD3
IMP_TXD4
IMP_TXD5
IMP_TXD6
IMP_TXD7
IMP_TXEN
IMP_TXER
IMP_TXCLK
P1V2
U1
NCP303LSN09T2G
NCP301LSN09T1G
OUT
VDD
GND
CD
NC
C44
0.1u
U2
NCP303LSN24T1G
C43
0.1u
TPS3840DL25
Sheet Title
GbE IC configuration
Project Title
Tile GbE Switch
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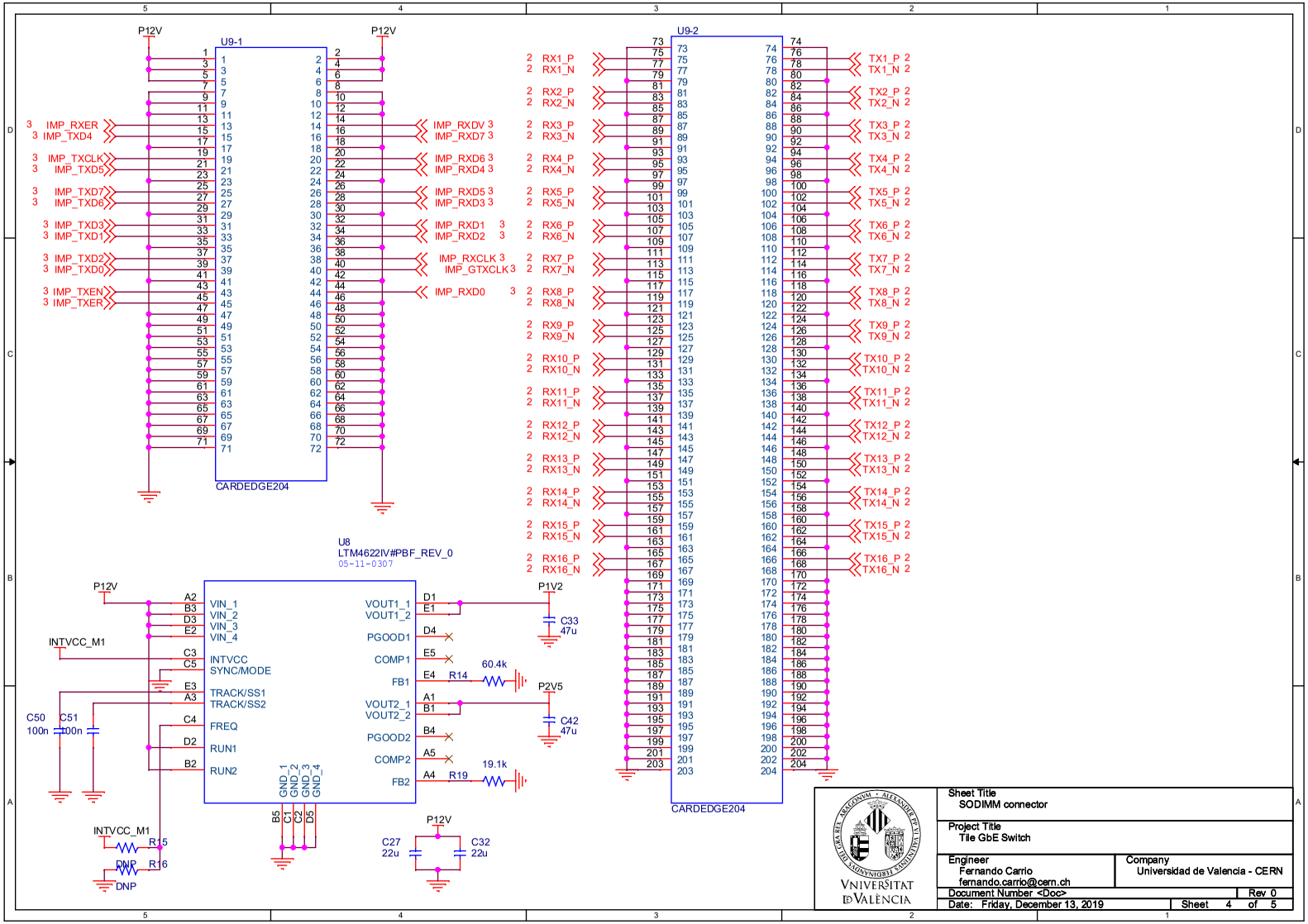
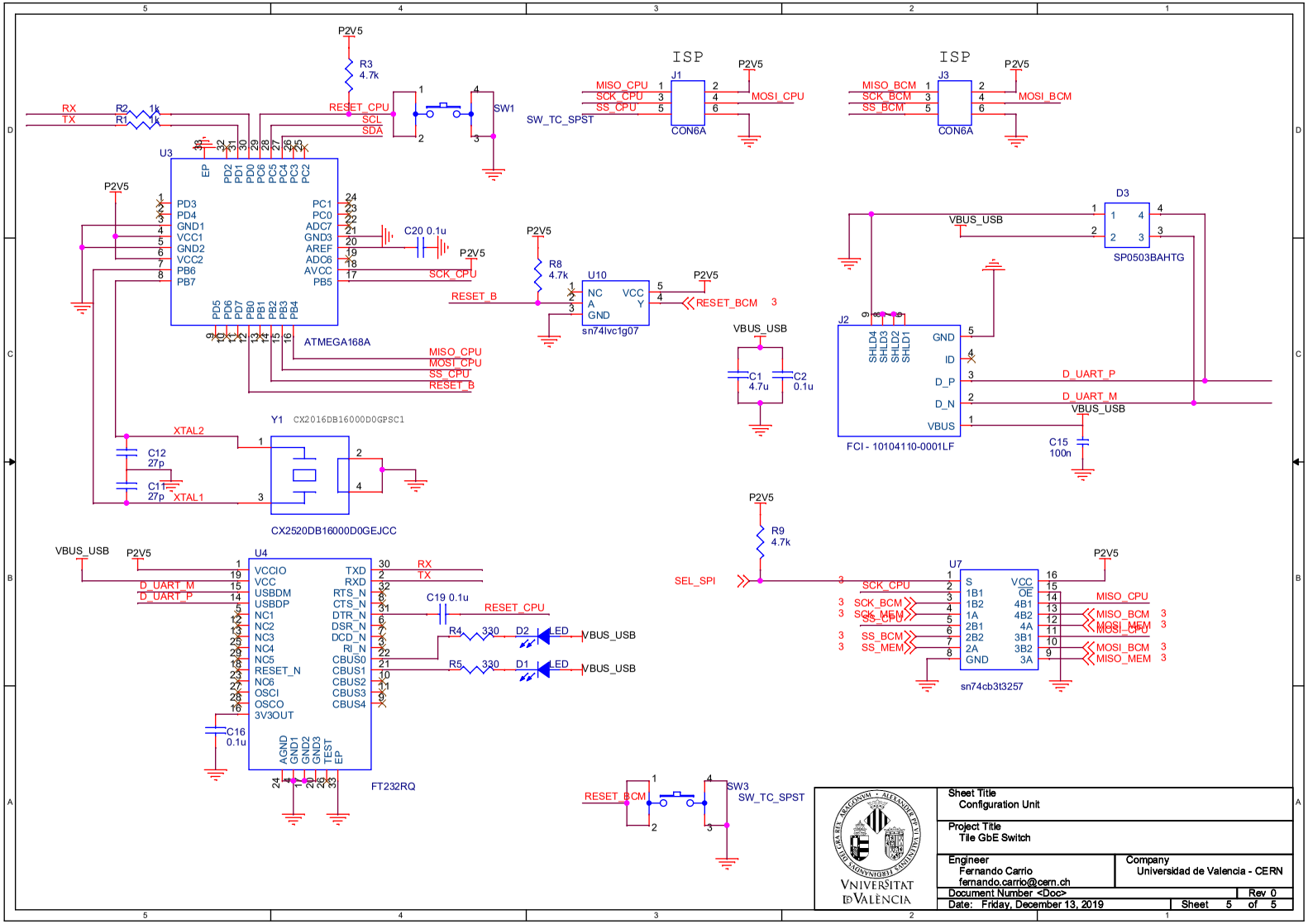
Company
Universidad de Valencia - CERN
Document Number <Doc>
Rev 0
Date: Friday, December 13, 2019
Sheet 3 of 5


U9-1
CARDEDGE204
U9-2
CARDEDGE204
U8
LTM4622IV#PBF_REV_0
05-11-0307
P12V
P1V2
P2V5
INTVCC_M1
C33 47u
C42 47u
C32 22u
C27 22u
C50 100n
C51 100n
60.4k
19.1k
R14
R15
R16
DNP
Sheet Title
SODIMM connector
Project Title
Tile GbE Switch
Engineer
Fernando Carrio
fernando.carrio@cern.ch
Company
Universidad de Valencia - CERN
Document Number <Doc>
Rev 0
Date: Friday, December 13, 2019
Sheet 4 of 5


P2V5
R3
4.7k
RX
TX
R2
1k
R1
1k
RESET_CPU
SCL
SDA
SW1
SW_TC_SPST
U3
EP
PD2
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PD0
PD6
PC5
PC4
PC3
PC2
PD3
PD4
GND1
VCC1
GND2
VCC2
PB6
PB7
PC1
PC0
ADC7
GND3
AREF
ADC6
AVCC
PB5
PD5
PD7
PB0
PB1
PB2
PB3
PB4
ATMEGA168A
C20 0.1u
SCK_CPU
MISO_CPU
MOSI_CPU
SS_CPU
RESET_B
ISP
J1
CON6A
MISO_CPU
SCK_CPU
SS_CPU
MOSI_CPU
J3
MISO_BCM
SCK_BCM
SS_BCM
MOSI_BCM
R8
4.7k
U10
NC
A
GND
VCC
Y
sn74lvc1g07
RESET_BCM
3
D3
SP0503BAHTG
VBUS_USB
J2
SHLD4
SHLD3
SHLD2
SHLD1
GND
ID
D_P
D_N
VBUS
D_UART_P
D_UART_M
FCI - 10104110-0001LF
C15
100n
C1
4.7u
C2
0.1u
Y1
CX2016DB16000D0GPSC1
XTAL2
XTAL1
C12
27p
C11
27p
CX2520DB16000D0GEJCC
U4
VCCIO
VCC
USBDM
USBDP
NC1
NC2
NC3
NC4
NC5
RESET_N
NC6
OSCI
OSCO
3V3OUT
TXD
RXD
RTS_N
CTS_N
DTR_N
DSR_N
DCD_N
RI_N
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
AGND
GND1
GND2
GND3
TEST
EP
FT232RQ
C16
0.1u
C19 0.1u
R4
330
R5
330
D2
D1
LED
R9
4.7k
SEL_SPI
U7
S
1B1
1B2
1A
2B1
2B2
2A
GND
VCC
OE
4B1
4B2
4A
3B1
3B2
3A
sn74cb3t3257
SW3
SW_TC_SPST
RESET_BCM
Sheet Title
Configuration Unit
Project Title
Tile GbE Switch
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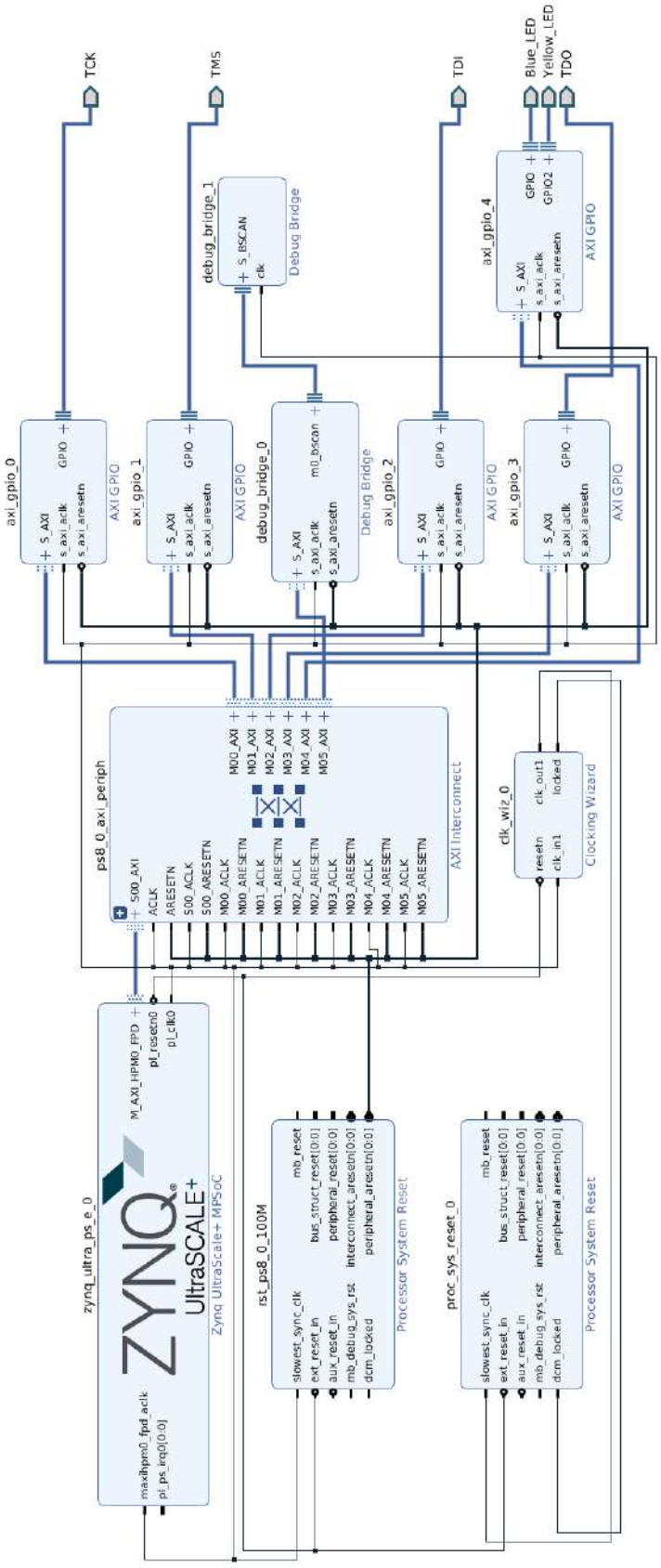
Date: Friday, December 13, 2019
Sheet 5 of 5

Appendix C

The PS and PL IP block design for remote programming

As discussed in Chapter 5, the remote programming functionality is divided into IP block design and software design. The block design shown in Appendix C shows the integration of IP block design with the PS of the TileCoM FPGA. The PS part of the TileCoM FPGA is denoted as Zynq UltraScale and the rest of the blocks are part of the PL part of the TileCoM FPGA.

C.1 Remote programming IP block design

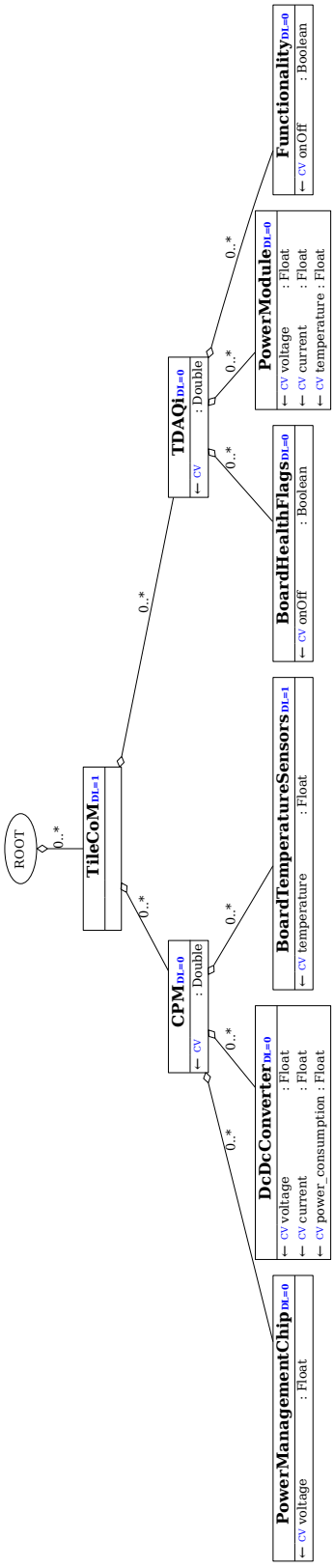


Appendix D

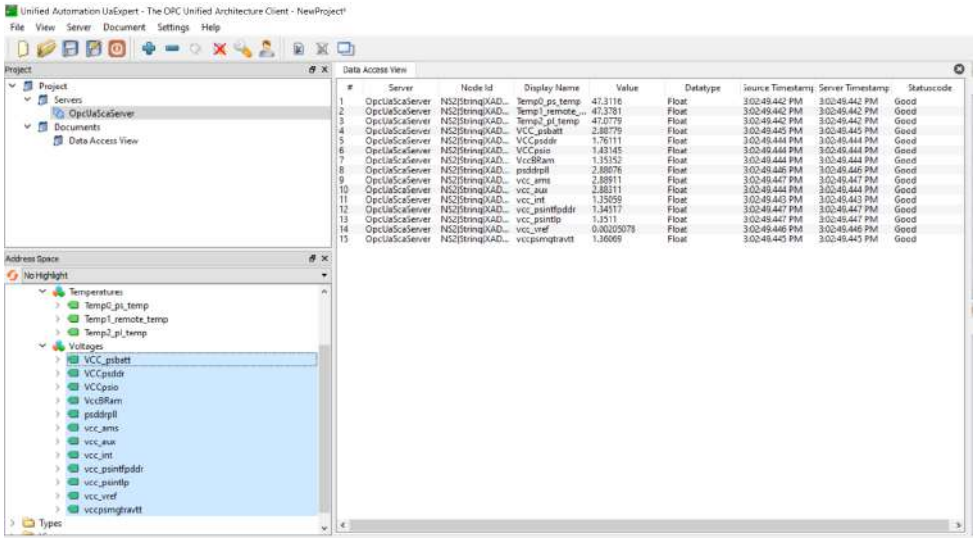
DCS block design and results

As detailed in the chapters above, OPCUA servers are implemented on the TileCoM to read out on- and off-detector electronics sensor data. In the final application, approximately 2,000 sensors from the on-detector electronics are monitored by each TileCoM module. These sensor data is transmitted in real-time to the DCS. Two client applications are available for publishing the sensor data, SCADA and UA expert. For this contribution, the UA expert is used to test the transmission of data in real-time. The figures in Appendix D show the Quasar+IPbus block design for DCS and a panel of the UA expert reading sensor data in real-time.

D.1 The Quasar+IPbus block design for DCS



D.2 XADC server results published on UA expert



Bibliography

[1] J. Emery et al. "First experiences with the LHC BLM sanity checks". In: *JINST* 5 (2010), p. C12044. DOI: 10.1088/1748-0221/5/12/C12044.

[2] M. Benedikt et al. *LHC Design Report, vol. III: The LHC Injector Chain. CERN, Geneva, 2004*. URL: https://cds.cern.ch/record/823808.

[3] O. Brüning et al. "LHC Design Report Vol.1: The LHC Main Ring". In: *Reports-CERN* (2004). DOI: 10.5170/CERN-2004-003-V-1.

[4] ATLAS Collaboration. *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*. 2012. URL: https://inspirehep.net/literature/1402887.

[5] G. Aad et al. "The ATLAS experiment at the CERN large hadron collider". In: *Journal of instrumentation* 3 (2008), S08003. DOI: 10.1088/1748-0221/3/08/S08003.

[6] CMS Collaboration et al. "The CMS experiment at the CERN LHC". In: *Jinst* 3 (2008), S08004. DOI: 10.1088/1748-0221/3/08/S08004.

[7] ALICE Collaboration et al. "The ALICE experiment at the CERN LHC". In: *Jinst* 3.420 (2008), S08002. DOI: 10.1088/1748-0221/3/08/S08002.

[8] A. Augusto et al. "The LHCb Detector at the LHC". In: *JINST* 3 (2008). Also published by CERN Geneva in 2010, S08005. DOI: 10.1088/1748-0221/3/08/S08005. URL: https://cds.cern.ch/record/1129809.

[9] F.C. Argos. "Development of readout electronics for the atlas tile calorimeter at the hl-lhc". PhD thesis. Universitat de València, 2017.

[10] G. Anelli et al. "The totem experiment at the cern large hadron collider". In: *Journal of Instrumentation* 3.08 (2008), S08007. DOI: 10.1088/1748-0221/3/08/S08007.

[11] O. Adriani et al. "The LHCf detector at the CERN large hadron collider". In: *Journal of Instrumentation* 3.08 (2008), S08006. URL: http://dx.doi.org/10.1088/1748-0221/3/08/S08006.

[12] J.L. Pinfold. "The MoEDAL Experiment at the LHC–a New Light on the Terascale Frontier". In: *Journal of Physics: Conference Series*. Vol. 631. 1. IOP Publishing. 2015, p. 012014. DOI: 10.1088/1742-6596/631/1/012014.

[13] G. Aad et al. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1–29. ISSN: 0370-2693. DOI: https://doi.org/10.1016/j.physletb.2012.08.020.

[14] S. Chatrchyan et al. "Evidence for the direct decay of the 125 GeV Higgs boson to fermions". In: *Nature Phys.* 10 (2014), pp. 557–560. DOI: 10.1038/nphys3005. arXiv: 1401.6527 [hep-ex].

[15] W.W. Armstrong et al. "ATLAS: Technical proposal for a general-purpose pp experiment at the Large Hadron Collider at CERN". In: (1994).

[16] ATLAS Collaboration. *Expected performance of the ATLAS experiment-detector, trigger and physics*. SLAC National Accelerator Laboratory (United States), 2008. URL: https://arxiv.org/abs/0901.0512.

[17] G. Aad et al. "Performance of the ATLAS detector using first collision data". In: *Journal of High Energy Physics* 2010.9 (2010), pp. 1–66. URL: http://hdl.handle.net/2078.1/138105.

[18] ATLAS Collaboration. "Studies of the performance of the ATLAS detector using cosmic-ray muons". In: *arXiv preprint arXiv:1011.6665* (2010). DOI: https://doi.org/10.48550/arXiv.1011.6665.

[19] D. V. Krasnopevtsev. "Tracking properties of the ATLAS Transition Radiation Tracker (TRT)". In: *J. Phys. Conf. Ser.* 798.1 (2017). Ed. by Arkady Galper et al., p. 012150. DOI: 10.1088/1742-6596/798/1/012150.

[20] G. Aad et al. "The ATLAS Inner Detector commissioning and calibration". In: *The European Physical Journal C* 70.3 (2010), pp. 787–821. DOI: 10.1140/epjc/s10052-010-1366-7.

[21] ATLAS Collaboration. *ATLAS inner detector: Technical Design Report, 1*. 1997. URL: https://inspirehep.net/literature/455673.

[22] S. Haywood et al. "ATLAS inner detector: technical design report, 2". In: *Technical Design Report ATLAS. CERN, Geneva* 28 (1997), pp. 29–32. URL: https://inspirehep.net/literature/455673.

[23] ATLAS Collaboration. "Operation of the ATLAS trigger system in Run 2". In: 15.10 (2020), P10004–P10004. DOI: 10.1088/1748-0221/15/10/p10004.

[24] A. Valero. "Operational experience and evolution of the ATLAS Tile Hadronic Calorimeter Read-Out Drivers". In: *22nd IEEE Real Time Conference*. Oct. 2020. DOI: 10.1109/TNS.2021.3084690. arXiv: 2010.13516 [physics.ins-det].

[25] G. Aad et al. "Readiness of the ATLAS Tile Calorimeter for LHC collisions". In: *Eur. Phys. J. C* 70 (2010), pp. 1193–1236. DOI: 10.1140/epjc/s10052-010-1508-y.

[26] ATLAS Collaboration. *ATLAS tile calorimeter: Technical design report*. CERN, 1996. URL: https://inspirehep.net/literature/432395.

[27] J. Abdallah, et al. "The optical instrumentation of the ATLAS Tile Calorimeter". In: *Journal of Instrumentation* 8.01 (2013), P01005. DOI: 10.1088/1748-0221/8/01/P01005.

[28] J. Abdallah et al. "The optical instrumentation of the ATLAS tile calorimeter". In: *JINST* 8 (2013), P01005. DOI: 10.1088/1748-0221/8/01/P01005.

[29] M. Agaras. "The ATLAS Tile Calorimeter performance and its upgrade towards the High-Luminosity LHC". In: (May 2021). DOI: 10.22323/1.364.0162.

[30] S. Berglund et al. "The ATLAS tile calorimeter digitizer". In: *Journal of Instrumentation* 3.01 (2008), P01004. DOI: 10.1088/1748-0221/3/01/P01004.

[31] P. Moreira et al. "TTCrx Reference Manual". In: *CERN, Internal document* (2003). URL: https://ttc.web.cern.ch/TTCrx_manual3.12.pdf.

[32] K. Anderson et al. "ATLAS tile calorimeter interface card". In: *In Proceedings of the 8th Workshop on Electronics for LHC Experiments.* (2022). URL: https://hep.uchicago.edu/atlas/tilecal/notes/Tangs_Interface_paper.pdf.

[33] A. Valero et al. "ATLAS TileCal read out driver production". In: *Journal of Instrumentation* 2.05 (2007), P05003. DOI: 10.1088/1748-0221/2/05/P05003.

[34] F. Trantou. "A program to drive the ATLAS Local Trigger Interface (ALTI) at the ATLAS experiment". In: *J. Phys. Conf. Ser.* 2105.1 (2021), p. 012024. DOI: 10.1088/1742-6596/2105/1/012024.

[35] CERN. *LHC/ HL-LHC Plan*. https://hilumilhc.web.cern.ch/content/hl-lhc-project.

[36] C.A. Sanchez. "The FELIX detector interface for the ATLAS TDAQ upgrades and its deployment in the ITk demonstrator setup". In: *Journal of Physics: Conference Series* 1525 (Apr. 2020), p. 012033. DOI: 10.1088/1742-6596/1525/1/012033.

[37] ATLAS Collaboration. "Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System". In: (). DOI: 10.17181/CERN.2LBB.4IAL.

[38] A. Paramonov. "FELIX: the Detector Interface for the ATLAS Experiment at CERN". In: *EPJ Web Conf.* 251 (2021), p. 04006. DOI: 10.1051/epjconf/202125104006.

[39] E. V. Santurio. "Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC." In: *J. Phys. Conf. Ser.* 928.1 (2017), p. 012024. DOI: 10.1088/1742-6596/928/1/012024.

[40] F. Tang, et al. "Design of Main Board for ATLAS TileCal Demonstrator". In: *19th Real Time Conference*. 2014. DOI: 10.1109/RTC.2014.7097541.

[41] E.V. Santurio et al. "A Revised Version of the ATLAS Tile Calorimeter Link Daughterboard for the HL-LHC". In: *IEEE Trans. Nucl. Sci.* 68.9 (2021), pp. 2414–2420. DOI: 10.1109/TNS.2021.3103408.

[42] E. Nkadimeng et al. "A monitoring and control test bench for assessing the upgraded low voltage power supplies for the ATLAS Tile Calorimeter Phase-II Upgrade front-end electronics". In: *Journal of Instrumentation* 17 (2022). DOI: 10.1088/1748-0221/17/07/P07025.

[43] E. V. Santurio. "Beam tests on the ATLAS tile calorimeter demonstrator module". In: *Nucl. Instrum. Meth. A* 936 (2019). Ed. by Giovanni Batignani et al., pp. 115–116. DOI: 10.1016/j.nima.2018.10.066.

[44] PCI Industrial Computer Manufacturers Group (PICMG). *Advanced Mezzanine Card Specification*. 2006. URL: https://www.picmg.org/openstandards/advanced-mezzanine-card/.

[45] F.C. Argos. "Design of the Compact Processing Module for the ATLAS Tile Calorimeter". In: *IEEE Trans. Nucl. Sci.* 68.8 (2021), pp. 1944–1951. DOI: 10.1109/TNS.2021.3085490.

[46] X. Yue. "Tile TDAQ interface module for the Phase-II Upgrade of the ATLAS Tile Calorimeter". In: *2019 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC)*. 2019, pp. 1–4. DOI: 10.1109/NSS/MIC42101.2019.9059861.

[47] A. Gomes. "The new front-end electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade". In: *JINST* 11.02 (2016), p. C02015. DOI: 10.1088/1748-0221/11/02/C02015.

[48] D. Bogavac. "The HL-LHC Upgrade of the ATLAS Tile Hadronic Calorimeter". In: *PoS* EPS-HEP2021 (2022), p. 838. DOI: 10.22323/1.398.0838.

[49] F. Tang et al. "Design of Main Board for ATLAS TileCal Demonstrator". In: *2014 19th IEEE-NPSS Real Time Conference*. IEEE. 2014, pp. 1–3. DOI: 10.1109/RTC.2014.7097541.

[50] S. Muschter et al. "Development of a readout link board for the demonstrator of the ATLAS tile calorimeter upgrade". In: *Journal of Instrumentation* 8.03 (2013), p. C03025. DOI: 10.1088/1748-0221/8/03/C03025.

[51] I. Hruska et al. "Radiation-Tolerant Custom Made Low Voltage Power Supply System for ATLAS/TileCal Detector". In: (2007). DOI: 10.5170/CERN-2007-007.369. URL: https://cds.cern.ch/record/1091490.

[52] G. Drake. "The new front-end electronics for the ATLAS tile calorimeter phase 2 upgrade". In: *2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. 2015, pp. 1–6. DOI: 10.1109/NSSMIC.2015.7581864.

[53] Linear Technology Corporation. *Dual Transistor Synchronous Forward Controller*. 2001. URL: https://www.analog.com/en/products/lt1681.html.

[54] R. Bonnefoy et al. *Performances of a Remote High Voltage Power Supply for the Phase II Upgrade of the ATLAS Tile Calorimeter*. CERN, 2014. URL: https://cds.cern.ch/record/2063682.

[55] ATLAS Tile Collaboration. *Initial Design for the Phase-II Upgrade of the 2 ATLAS Tile Calorimeter System*. Number ATL-COMTILECAL-2016-053. Geneva, 2016. URL: https://cds.cern.ch/record/2285583.

[56] A. Gomes et al. "Upgrade of the ATLAS Tile Calorimeter high voltage system". In: *Journal of Instrumentation* 17.01 (2022), p. C01061. DOI: 10.1088/1748-0221/17/01/c01061.

[57] F.C. Argos and A. Valero. "The PreProcessor module for the ATLAS Tile Calorimeter at the HL-LHC". In: *Nucl. Instrum. Meth. A* 958 (2020). Ed. by Manfred Krammer et al., p. 162487. DOI: 10.1016/j.nima.2019.162487.

[58] A.C. Duato et al. "The TileCal PreProcessor Interface with the ATLAS Global Data Acquisition System at the HL-LHC". In: (2022). URL: https://cds.cern.ch/record/2813414.

[59] Xilinx. *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics*. 2020. URL: https://docs.xilinx.com/v/u/en-US/ds922-kintex-ultrascale-plus.

[60] J. Munch. *Advanced Telecommunications Computing Architecture, a next generation PICMG specification*. October 2003. URL: http://pdf.cloud.opensystemsmedia.com/advancedtca-systems.com/Adlink.Oct03.pdf.

[61] ATLAS Tile Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*. Geneva: CERN, 2017. DOI: 10.17181/CERN.2LBB.4IAL. URL: https://cds.cern.ch/record/2285584.

[62] ATLAS Collaboration. *SoC for ATLAS subsystems: Requirements Document for HL-LH*. 2020. URL: https://indico.cern.ch/event/996093/contributions/4376640/attachments/2260095/3835911/ATLASSoCRequirements.pdf.

[63] Broadcom. *16-GE PORT SWITCH WITH INTEGRATED SerDes*. Apr. 2006. URL: https://www.datasheetq.com/BCM5396-doc-Broadcom.

[64] Microchip. *ATmega48A/PA/88A/PA/168A/PA/328/P*. Apr. 2020. URL: https://www.microchip.com/en-us/product/ATmega48A.

[65] Member of ICAPE Group. *Trax Interconnect (PTY) Ltd*. URL: https://www.trax.co.za/.

[66] Vinova Communications. *Jemstech | Turnkey Electronic Manufacturing Service Provider*. URL: https://www.jemstech.co.za/.

[67] J. Mendez et al. "Design of an AdvancedTCA board management controller (IPMC)". In: *JINST* 12.03 (2017), p. C03010. DOI: 10.1088/1748-0221/12/03/C03010.

[68] J. Mendez. *CERN-IPMC: Hardware guide*. 2017. URL: https://cern-ipmc.web.cern.ch/doc.

[69] XILINX. *UltraScale Architecture and Product Data Sheet: Overview*. 2022. URL: https://docs.xilinx.com/v/u/en-US/ds890-ultrascale-overview.

[70] Linear Technology. *30A DC/DC Step-Down µModule Regulator*. May 2016. URL: https://www.mouser.com/datasheet/2/609/4647fb-1271775.pdf.

[71] Linear Technology. *Quad DC/DC µModule Regulator with Configurable 4A Output Array*. May 2020. URL: https://www.farnell.com/datasheets/2187776.pdf.

[72] Linear Technology. *Dual 10A or Single 20A µModule Regulator*. Sept. 2018. URL: https://www.analog.com/en/products/ltm4646.html.

[73] Linear Technology. *16-Channel µModule PMBus Power System Manager*. July 2014. URL: https://www.analog.com/en/products/ltm2987.html#product-overview.

[74] F.C. Argos, P. Moreno, and A. Valero. "Performance of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade". In: *JINST* 11.03 (2016), p. C03047. DOI: 10.1088/1748-0221/11/03/C03047.

[75] F.C Argos. "The Data Acquisition System for the ATLAS Tile Calorimeter Phase-II Upgrade Demonstrator". In: *IEEE Trans. Nucl. Sci.* 69.4 (2022), pp. 687–695. DOI: 10.1109/TNS.2022.3143233.

[76] Xilinx. *Zynq UltraScale+ MPSoC Data Sheet: Overview*. 2021. URL: https://docs.xilinx.com/v/u/en-US/ds891-zynq-ultrascale-plus-overview.

[77] Xilinx. *1G/2.5G Ethernet PCS/PMA or SGMII v16.0*. 2017. URL: https://docs.xilinx.com/v/u/16.1-English/pg047-gig-eth-pcs-pma.

[78] Xilinx Mary Low. *Using the RGMII to Interface with the Gigabit Ethernet MAC*. 2006. URL: https://docs.xilinx.com/v/u/en-US/xapp692.

[79] Xilinx. *Zynq UltraScale+ MPSoC Processing System v3.2*. 2018. URL: https://docs.xilinx.com/v/u/3.2-English/pg201-zynq-ultrascale-plus-processing-system.

[80] Xilinx. *Zynq UltraScale+ MPSoC Data Sheet: Overview*. 2022. URL: https://docs.xilinx.com/v/u/en-US/ds891-zynq-ultrascale-plus-overview.

[81] Xilinx. *UltraScale Architecture DSP Slice: User Guide*. 2021. URL: https://docs.xilinx.com/v/u/en-US/ug579-ultrascale-dsp.

[82] Silicon labs. *I²C-PROGRAMMABLE ANY-FREQUENCY, ANY-OUTPUT QUAD CLOCK GENERATOR*. 2015. URL: https://docs.rs-online.com/dd52/0900766b814f6624.pdf.

[83] Renesas Electronics America Inc. *Low Skew, 1-to-6, Differential-to-LVDS Fanout Buffer*. 2017. URL: https://www.renesas.com/us/en/document/dst/ics8546-01-datasheet?r=9507.

[84] Texas instrument. *TPS650864 Configurable Multirail PMU for Xilinx® MPSoCs and FPGAs*. 2017. URL: https://www.ti.com/document-viewer/TPS650864/datasheet.

[85] Analog Devices. *Pushbutton On/Off Controller with µPower Interrupt*. 2006. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/2954fb.pdf.

[86] Texas instrument. *CSD87331Q3D Synchronous Buck NexFET™ Power Block*. 2017. URL: https://www.ti.com/product/CSD87331Q3D.

[87] Micron Technology Inc. *Micron Technology Inc. MT53D512M32D2DS-053 AIT:D*. 2020. URL: https://www.digikey.com/en/products/detail/micron-technology-inc/MT53D512M32D2DS-053-AIT-D/7597849.

[88] R. Spiwoks et al. "CentOS Linux for the ATLAS MUCTPI Upgrade". In: *22nd IEEE Real Time Conference*. Oct. 2020. DOI: 10.1109/TNS.2021.3084246. arXiv: 2010.08105 [physics.ins-det].

[89] Broadcom. *Single-Chip 16-Port SerDes Gigabit Switch*. 2016. URL: https://vdocument.in/single-chip-16-port-serdes-gigabit-switch.html?page=1.

[90] Microchip Technology Inc. *Microchip ATmega48A/PA/88A/PA/168A/PA/328/P*. 2020. URL: https://www.microchip.com/en-us/product/ATmega48A.

[91] Texas. *SN74CB3T3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER*. 2005. URL: https://www.ti.com/lit/ds/symlink/sn74cb3t3257.pdf.

[92] Catalyst Semiconductor, Inc. *CAT24C128128-Kb I^2C CMOS Serial EEPROM*. 2006. URL: https://docs.rs-online.com/4125/0900766b81573741.pdf.

[93] Linear Technology. *15A DC/DC µModuleRegulator*. 2006. URL: https://www.analog.com/en/products/ltm4627.html#product-overview.

[94] G. Stark. *Cookbook for Handling IPBus packets*. 2015. URL: https://iron-man.readthedocs.io/en/latest/cookbook.html.

[95] Xilinx. *PetaLinux Tools Documentation*. URL: https://docs.xilinx.com/v/u/2018.2-English/ug1144-petalinux-tools-reference-guide.

[96] C. Ghabrous Larrea et al. "IPbus: a flexible Ethernet-based control system for xTCA hardware". In: *JINST* 10.02 (2015), p. C02019. DOI: 10.1088/1748-0221/10/02/C02019.

[97] Xilinx. *AXI Basics 1 - Introduction to AXI*. 2021. URL: https://support.xilinx.com/s/article/1053914?language=en_US.

[98] D. Paul and U. Singh. *JarvisAI 3.9*. Release1.1.0-rc1-52-g9a543201f-dirty. 2020. URL: https://pypi.org/project/JarvisAI/.

[99] Twisted Matrix Labs. *Twisted Documentation*. Release 16.6.0. 2016. URL: https://twisted.readthedocs.io/_/downloads/en/twisted-16.6.0/pdf/.

[100] S. Schlenker et al. In: *quasar - A Generic Framework for Rapid Development of OPC UA Servers* 108.5 (2015), p. 4. DOI: 10.18429/JACoW-ICALEPCS2015-WEB3O02.

[101] J. Pina. "The Tilecal/ATLAS detector control system". In: *2004 IEEE Nuclear Science Symposium and Medical Imaging Conference*. 2. 2004, pp. 1201–1204. DOI: 10.1109/NSSMIC.2004.1462418.

[102] Open Source OPC UA licensed under the MPL v2.0. *open62541 Documentation*. 2022. URL: https://www.open62541.org/documentation/.

[103] F. Martins. "The ATLAS tile calorimeter DCS for run 2". In: *2016 IEEE Nuclear Science Symposium and Medical Imaging Conference*. 2016, p. 8069837. DOI: 10.1109/NSSMIC.2016.8069837.

[104] B. Hallgren et al. "The embedded local monitor board (ELMB) in the LHC front-end I/O control system". In: *7th Workshop on Electronics for LHC Experiments*. Sept. 2001, pp. 325–330. DOI: 10.5170/CERN-2001-005.325.

[105] F. Martins et al. "Control System of Upgraded High Voltage for Atlas Tile Calorimeter". In: *JACoW* ICALEPCS2021 (2022), pp. 443–446. DOI: 10.18429/JACoW-ICALEPCS2021-TUPV025.

[106] S. Schlenker. *DCS: Requirements Document for HL-LHC : ATLAS Phase-II Upgrade Project*. 2020.

[107] M.G.D. Gololo. "Developments on the Tile Computer on Module (TileCoM) mezzanine board for the ATLAS Tile Calorimeter off-detector electronics". In: (2020). URL: https://cds.cern.ch/record/2719375.

[108] Xilinx. *Designing an XVC project for Remote Debugging of Zynq UltraScale+ devices*. 000032879. 974879. Xilinx, 2021. URL: https://support.xilinx.com/s/article/974879?language=en_US.

[109] Redhat. "Red Hat Enterprise Linux". In: 2022. Chap. CHAPTER 23. DYNAMIC HOST CONFIGURATION PROTOCOL (DHCP). URL: https://access.redhat.com/documentation/en-us/red_hat_enterprise_linux/5/html/deployment_guide/ch-dhcp.

[110] R. Spiwoks. *CentOS For ZynqMP*. May 2019. URL: https://twiki.cern.ch/twiki/bin/view/SystemOnChip/CentOSForZynqMP.

[111] M.G.D. Gololo, F. Carrió Argos, and B. Mellado. "Tile Computer-on-Module for the ATLAS Tile Calorimeter Phase-II upgrades". In: *Journal of Instrumentation* 17.06 (2022), P06020. DOI: 10.1088/1748-0221/17/06/P06020.

[112] M.G.D. Gololo, F.C Argos, and B. Mellado. "South African contribution towards the ATLAS Tile Calorimeter PreProcessor". In: (2021), pp. 91 –95. URL: https://events.saip.org.za/event/206/page/446-the-proceedings-of-saip2021.

[113] M.G.D. Gololo et al. "Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter". In: *Journal of Physics: Conference Series* 1690.1 (2020), p. 012054. DOI: 10.1088/1742-6596/1690/1/012054.

[114] Soare Cristian-Valeriu. "OPC UA IPbus server". In: (2015). URL: https://cds.cern.ch/record/2055198.

[115] Xilinx. *VC707 Evaluation Board for the Virtex-7 FPGA User Guide*. 2019. URL: https://www.xilinx.com/support/documents/boards_and_kits/vc707/ug885_VC707_Eval_Bd.pdf.

[116] Avnet. *Ultra96-V2 Getting Started Guide*. 2020. URL: https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/ultra96-v2/.

[117] *Putty free and open-source terminal emulator serial console*. 2022. URL: https://putty.org/.

[118] Schroff. *ATCA System 450/40 Series, 2 Slot, AC, Node/Node*. Mar. 2018. URL: https://schroff.nvent.com/en-gb/products/enc11990-705.

[119] Kontron. *AT8404 Kontron User's Guide*. Mar. 2010. URL: https://www.kontron.com/download/download?filename=/downloads/manuals/xbd1m125.pdf&product=86768.

[120] Analog Devices. *±1°C Temperature Monitor with Series Resistance Cancellation*. 2003. URL: https://m.onsemi.com/download/data-sheet/pdf/nct72-d.pdf.

[121] Broadcom Limited. *BCM54680B0IFBG-ND*. 2011. URL: https://www.digikey.com/en/products/detail/broadcom-limited/BCM54680B0IFBG/6146638.

[122] Intel. *Intel 82580EB/82580DB Gigabit Ethernet Controller*. 2015. URL: https://www.mouser.com/datasheet/2/612/82580_eb_db_gbe_controller_datasheet-257707.pdf.

[123] *MCP9808: ±0.5°C Maximum Accuracy Digital Temperature Sensor*. Microchip Technology Inc., 2011. URL: https://www.microchip.com/en-us/product/mcp9808.

[124] Linear Technology. *LTM4601A/LTM4601A-1 12A µModule Regulators with PLL, Output Tracking and Margining*. 2022.

[125] Linear Technology. *6A DC/DC µModule Regulator with Tracking and Frequency Synchronization*. 2010. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/4618fb.pdf.

[126] Linear Technology. *Dual 8A or Single 16A DC/DC µModule Regulator*. 2010. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/4628fe.pdf.

[127] Linear Technology. *36VIN, 600mA Step-Down µModule Converter with 5µA Quiescent Current*. 2019. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/LTM8029.pdf.

[128] Linear Technology. *High Voltage Surge Stopper with Current Limit*. 2011. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/4363fb.pdf.