A HIGH SPEED DATA CAPTURE SYSTEM FOR USE IN THE ANALYSIS OF PARTIAL DISCHARGE ACTIVITY

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A project report submitted to the Faculty of Engineering, University of the Witwatersrand, Johannesburg, in partial fulfilment of the requirements for the Degree of Master of Science in Engineering

Johannesburg, 1985

DECLARATION

I declare that this project report is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of the Witwatersrand, Johannesburg. It has not been submitted for any degree or examination in any other University.

PIERRE DE VILLIERS

19th day of September, 1985.

ABSTRACT

A high-speed digital data capture system has been developed for on-line data recording and analysis as part of a long term-research program, concerned with the location and detection of partial discharges in electric insulation, currently being conducted at the University of the Witwatersrand.

ACKNOWLEDGEMENTS

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For Mrs. Mitchell

1 INTRODUCTION

The problem revolves around the detection of partial discharges in electric insulation. It is to this end that an high speed digital measurement system has been developed to enable on-line data recording and analysis. This system will, hopefully, ease the task of the researcher who, for well nigh 30 years, has attempted to isolate and describe the mechanisms responsible for the failure of insulation that has been in service for some time.

This insulation failure at values of electric stress well below its accepted breakdown value, is a result[1] of the basic processes of intrinsic and thermal breakdown. Conditions necessary to precipitate these mechanisms can be realised by a slow process of erosion caused by internal discharges in gaseous cavities within the mass of insulation. The energy spectrum of spark- or pulsed-type discharge patterns can be inferred by measuring the amplitude distribution of the discharge pulses using a pulse-height analyzer. Information on the discharge-energy spectrum is particularly important in studies concerning the relationship between the dissipated discharge energy and the ensuing degradation rate of dielectric materials exposed to electrical discharges.

In examining this phenomenon, researchers at the University of the Witwatersrand[2] have concentrated on the measurement and analysis of discharge current pulses. Unfortunately, pulse analysis instruments for partial discharge measurements are not commercially available as complete instruments and it is often necessary to build or assemble such tools. These constructed units have had numerous disadvantages - they have been too slow, their dynamic range has been very limited and they have exhibited unacceptable 'dead-times' between measurements. Also with the discharge measuring systems used to date, it has not always been possible to assess significant parameters. This

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is because much of the available information is inevitably discarded during high-voltage testing.

In measuring partial discharges, id est, magnitude and times of occurrence of individual discharges, the utilisation of a digital computer is particularly attractive. This is due to the fact that it allows the captured data to be recorded, thereby facilitating more efficient processing. In previous instances, however, the application of computers has been limited[3] by bandwidth considerations which have detrimentally increased the resolution time of the overall recording system.

The design developed for, and presented in, this report alleviates the problems previously experienced by taking advantage of the development of very high-speed semiconducting devices. The system detailed, herein, is microprocessor based and controlled. The microprocessor's inherent speed prevents it from being actively involved in the data capture. By virtue of this, it is relegated to the role of supervisor. It serves as a front end processor and is responsible for communication with the user; control of the data capture, and subsequent storage of the data captured. The actual data capture function, and monitoring thereof, is performed by a high speed finite state machine that allows the input to be sampled at speeds of up to 10MHz. The microprocessor enables the system to be "software tuned", via various programmable parameters, to meet a number of user requirements.

It is envisaged that the high-speed data acquisition capability offered by this system will allow the study of the important phenomenon of the "burst"[4] characteristics observed in insulation samples and structures. The system offers the capability for dealing with a large dynamic-signal input range, and as it permits on-line characterization of partial discharges, it is hoped that the results of discharge measurements will have greater significance than

at present. This is of special import in those borderline cases where the interpretation of results is difficult.

Outlined in the main body of this report will be a brief exegesis of the system's functions and capabilities. The design itself is dealt with greater length and in more depth in the appendices.

2 METHOD and DESIGN

2.1 PARTIAL DISCHARGE MEASUREMENT

A partial discharge is caused by charged particles moving across a gas space within an insulating medium or in a space between an insulating surface and a conductor. This charge movement results in a current pulse which can be electrically detected in the supply circuit to the insulation. It has been determined [2,8], that an instrumentation bandwidth of 400MHz is necessary to capture all the information contained in the faster pulses (ie. those having rise times of approximately 2,0ns). However, if the important information in a pulse can be confined to the charge it contains, a much lower bandwidth is adequate, provided a suitable "stretching" technique is applied to the pulse.

"Stretching" by integration produces a unidirectional pulse of much greater width, but having a peak magnitude proportional to the charge contained in the input pulse. The "stretching" technique used here will ensure that the pulse width will be in the range 3-10us with rise times of not less than 0,25-1,0us.

The bandwidth of the data capture system is determined by the pulse rise time, whereas the bandwidth of the "stretching" circuitry is dependent upon the pulse duration so the measurement system bandwidth will be limited by the "stretching" circuitry.Considering a pulse duration of 3us, the maximum partial discharge repetition rate that can measured, is 300KHz. Thus, in a 50Hz cycle, the "stretcher" will be capable of processing 300KHz/50Hz = 6×10^3 pulses per cycle. As measurements will take place at voltages very close to the inception voltage, it is expected that the number of pulses occurring per cycle will not exceed 100.

Hence, measurements will obviously not be impeded by the inherent bandwidth limitations imposed by the "stretching" circuitry.

2.2 REQUIREMENTS

A high speed digital data acquisition system is required for measurement of partial discharges. This system has to offer the following:

a. Variable sampling rates (1MHz to 10MHz)
b. Variable triggering levels
c. Variable sampling periods
d. An indication of the time of triggering for signals of .1Hz to 60Hz
e. Sufficient memory to permit the storage of a reasonable amount of continuously recorded data
f. Facilities to allow further processing of the data

2.3 OVERVIEW

In the system described (see Figure 1), a 16-bit microprocessor based computer (iSBC 86/12A) is used for overall control. The inherent "slow" speed of the microprocessor prevents it from being actively involved in the data capture, however, it supervises the data capture, controls the user interface and transfers the captured data to tape to allow further processing. 32K memory is available for the control and interface programs and their requisite variables and a further 64K high speed memory is available for the storage of the captured data. A programmable oscillator controls the sampling frequency and a programmable realtime clock permits accurate measurement of the time of occurrence of every recorded discharge. The data

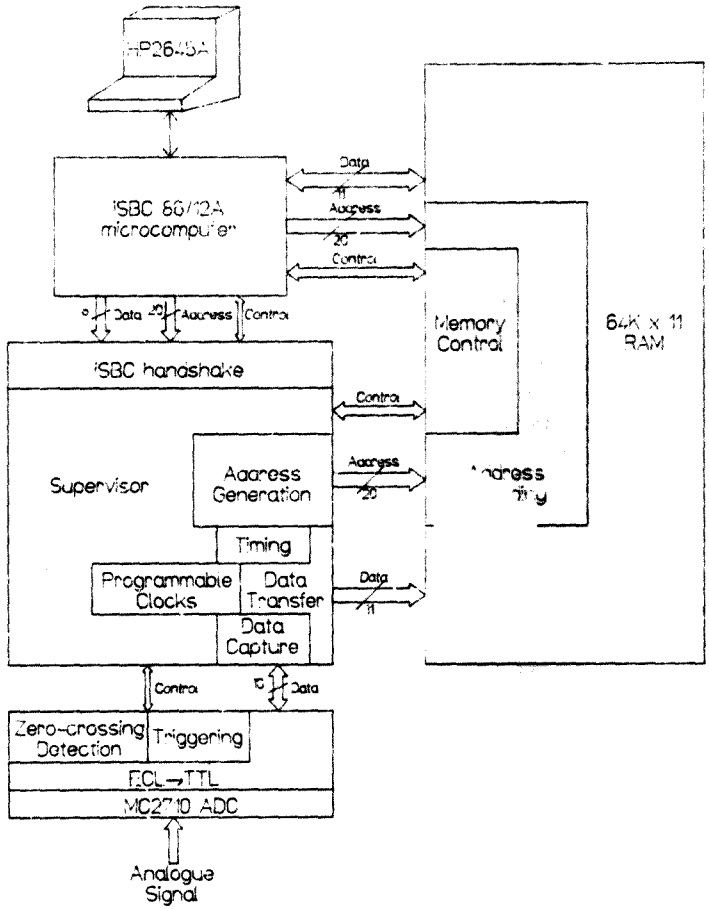

FIGURE 1. SYSTEM BLOCK DIAGRAM

capture circuits include a 10-bit analog-to-digital converter, a programmable level detector and an HP2645A workstation that provides the user interface and two tape drives for permanent data storage. The system can sample incoming data at a maximum rate of 10MHz for approximately 65000 samples.

2.4 MEMORY (see Appendix 1)

It was decided that 64K of memory would be sufficient to hold a useable quantity of sampled data. As the ADC (MC2710) offered 10 bits resolution, the memory bank would have to be at least 10 bits wide. An extra bit was included to differentiate between timing data and sampled data.

2.4.1 MEMORY ADDRESS CIRCUITRY (see Sheet 3)

The memory had to be accessed at speeds of up to 10MHz. The address was calculated using very fast binary counters whose output was latched and held for addressing the memory.

2.4.2 MEMORY ACCESS CONTROL CIRCUITRY (see Sheet 11)

The memory was written to by both the iSBC 86/12A and the data capture circuitry, whilst it was only read by the iSBC 86/12.

2.4.2.1 WRITE CONTROL (during sampling)

For writing, the chip select (CS) and write enable lines (WE) had to be synchronised with the addressing and data capture circuits. This

was achieved by clocking the address, data capture and memory with the same clock.

2.4.2.2 DUAL PORT ACCESS CONTROL

The sampling circuitry and the iSBC 86/12A present address and data to the memory on two separate sets of latches, only one of which is enabled at any time. Once sampling has commenced, the sampling circuitry has sole access to the memory, whilst before and after sampling, only the 8086 can access the memory.

2.4.2.3 ACCESS BY iSBC

It was decided to allow the 8086 to both write to and read from the memory. This allows the 8086 to test the memory and to transfer the captured data to tape for further processing.

2.5 DATA CAPTURE (see Appendix 2)

The data capture circuitry is divide into two sections. One that measures the discharge pulses and one that detects the zero-crossing of the AC signal.

2.5.1 PULSE CAPTURE & TRIGGERING (see Sheets 6 & 7)

The incoming data stream is sampled at a maximum rate of 10MHz by a 10-bit ADC. The digital data presented by the ADC is filtered through a set of comparators before being stored in memory. This filtration permits only the storage of data that are above a given positive value or below a given negative value.

2.5.2 ZERO-CROSSING CIRCUITRY (see Sheet 9)

The AC signal is monitored and every positive zero-crossing is used as a base-point from which the time of occurrence of each subsequent discharge is measured.

2.6 CONTROL CIRCUITRY (see Appendix 3)

The ADC and 8086 should be regarded as peripheries to this design. The design actually centres on the interfacing of the ADC, 8086 and the data capture memory, and the subsequent control of the data capture operation.

2.6.1 SUPERVISOR CIRCUITRY (see Sheet 2)

This controls the address generation and the data capture. It is responsible for ensuring that the memory control signals and the data/address inputs are synchronised. It starts the data capture operation when instructed to do so and then monitors the process to ensure that it stops before the memory overflows.

2.6.2 TIMING CIRCUITRY (see Sheet 5)

The data for each pulse must be stored with an indication of where it occurred relative to the AC signal. This indication is calculated by means of a "real-time" clock that is reset by every zero-crossing of the AC waveform. The timing circuitry is responsible for the storage of each discharge's timing information.

2.6.3 CLOCK CIRCUITRY (see Sheets 1 & 4)

The sampling frequency is variable between 1MHz and 10MHz. Because of the divider circuitry used for the ADC strobe pulse, this implies that the supervisor must be clocked at speeds ranging from 4MHz to 40MHz.

On the other hand, the system will only be required to monitor signals ranging from .1Hz to 60Hz. Thus, the timing need only be clocked at rates varying from 400Hz to 240KHz. These vast differences in operating speeds led to the use of two separate clocks - one for the supervisor circuitry and one for the timing circuitry. Because both clocks, by necessity, had to operate over a very wide frequency range, phase-locked-loops were used to achieve a reasonably stable operation.

2.7 INTERFACE (see Appendix 4)

The data capture circuitry is interfaced to a 16-bit microprocessor based single board computer - the INTEL iSBC 86/12A. Through this microcomputer, the data-capture circuitry is then interfaced to an HP2645A workstation (see Figure 2).

2.7.1 iSBC 86/12A

The iSBC 86/12A is required to transmit the following data to the sampling circuitry:

a. The sampling rate
b. The AC signal frequency
c. The upper and lower values for triggering
d. Signals to start and stop sampling

At the same time, the sampling circuitry gives the following signals to the iSBC 86/12A:

a. An indication that the memory is full.
b. The zero-crossings of the AC signal so that the AC frequency might be ascertained.

2.7.2 HP

The iSBC 86/12A has an RS232C compatible serial I/O port controlled by an 8251A USART chip and communication with the HP is EIA RS232-C serial synchronous, full duplex ASCII at 9600 bits/second.

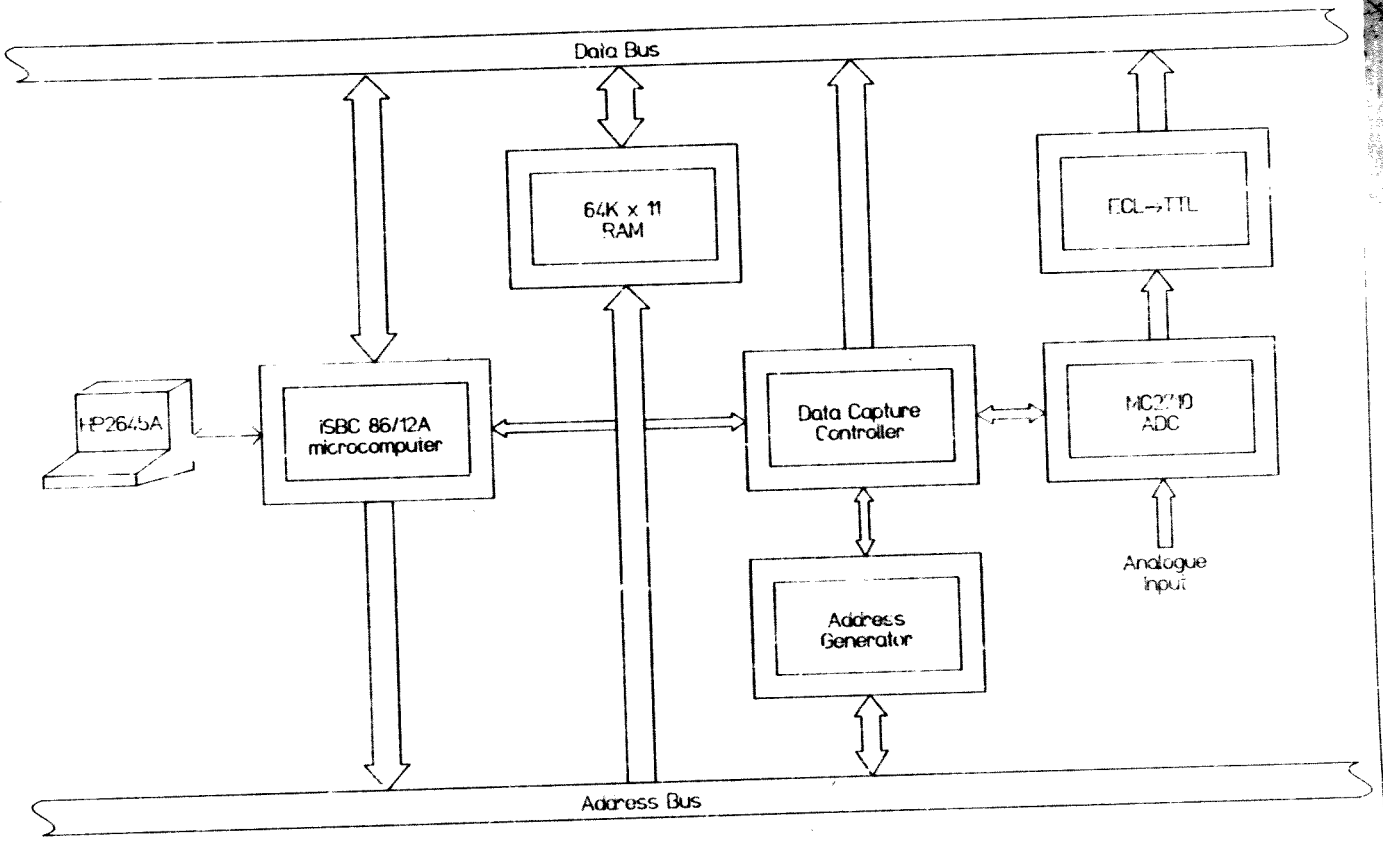

FIGURE 2. SYSTEM CONTROL & DATA FLOW

2.8 SOFTWARE DESIGN

The software allows the user to tailor the system to meet his requirements. In this respect it must permit the selection of variable sampling rates and variable triggering levels. The software is responsible for measurement of the AC frequency, for starting (and possibly halting) pulse capture and for transfer of information between the pulse acquisition system and the iSBC 86/12A and HP2645A display station.

For ease of use, the system is "menu-driven", i.e. the user is guided through the procedures he must perform by a number of menus displayed on the HP screen. The software is divided into three major sections:

a. The pulse acquisition routines which are responsible for the tuning of the system parameters and for monitoring the sampling process.
b. The memory access routines which transfer data to and from the data acquisition system memory.
c. The interface routines for communicating through the HP2645A with the user.

The software is written in Pascal to improve readability and maintenance. However, it is necessary that some of the routines be written in 8086 assembler. The programs were compiled, assembled and linked on an HP64000 system.

3 IMPLEMENTATION & EVALUATION

3.1 IMPLEMENTATION

The data capture circuitry was wire-wrapped on multibus boards for compatibility with the iSBC 86/12A. However, the boards were not new and in most cases, the edge-connectors had been worn off the boards. Thus it was decided to mount 3M multiway connectors to the boards and use these instead. The hardware was tested with a Nicolet analyser and the software and integrated system was tested using the HP64000 8086 emulator (borrowed from ESD).

3.2 OPERATION OVERVIEW

The user must enter a number of options before proceeding with data capture. The user communicates with the measuring system via the HP 2645A display station. The user is guided through the necessary "tuning" steps by a series of menus. The system will use defaults for any options not entered by the user. Once the user has requested that sampling commence, the system will determine the AC frequency and then allow data capture to start. The signal is then monitored for zero-crossings and partial discharge occurrence. Each partial discharge is stretched and passed through an ADC. The digital output of the ADC is then filtered before being stored in memory together with timing data indicating where it occurred in relation to the most recent zero-crossing.

As the data is stored in 10-bit words, the signal wavelength, T, (see Figure 3) can be divided into 2^{10} = 1024 time slots

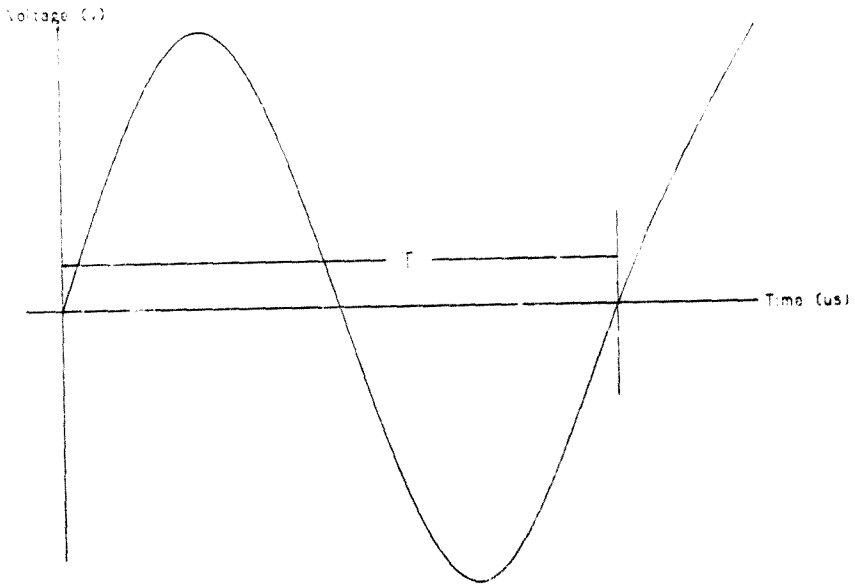

FIGURE 3. AC SIGNAL WAVELENGTH

EXAMPLE

T = 20ms :- 20 x 10^{-23} / 1000 = 20 x 10^{-6} seconds

i.e. the wavelength can be divided into 1000 20us time slots

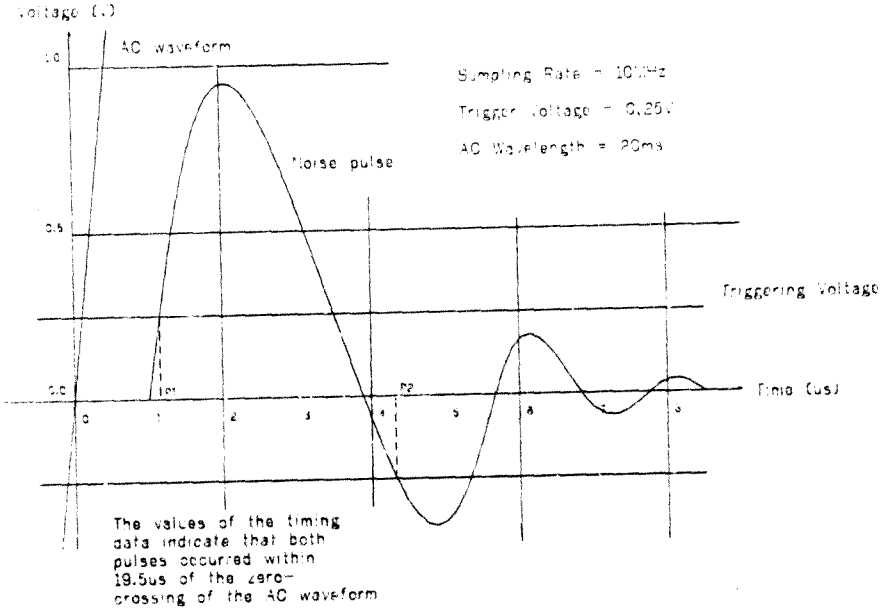

FIGURE 4. DISCHARGE PULSE

Figure 4 shows a discharge that has been measured to give the following memory configuration:

MEMORY ADDRESS	MEMORY CONTENTS	
0	00101100110	
1	00101000000	
2	00100011010	
3	00011110011	
4	00001101101	
5	00010110011	
6	00010001101	
7	00001110100	
8	00001011010	
9	00001000000	
10	00000110011	
11	00000110011	
12	00000100110	
13	00000111010	
14	00001010011	
15	00001101101	
16	00010001101	
17	00010101101	
18	00011001101	
19	00011110011	
20	00100100000	
21	00101000000	
22	00101101101	
23	10000000000	(Time P1)
24	01010000000	
25	01001111010	
26	01000110111	
27	01000010000	
28	01000101010	
29	01001111011	
30	100000000000	(Time P2)

As can be seen, the timing information is stored after the pulse information. In the example, both data capture triggers occurred within 20us of the first zero-crossing. One discharge may trigger the data capture

circuitry more than once during its occurrence. This seemingly confusing representation can easily be clarified by software during post-processing.

3.3 IMPROVEMENTS

MEMORY

The memory should have been implemented using larger and thus fewer chips. If this required the use of slower chips an interleaved design could have been used.

CLOCK 2

The Clock 2 crystal output should be filtered before being passed to the phase locked loop which is presently operating at one of the crystal's harmonics.

ADC RANGE & OFFSET

The MC2710 range and offset inputs have been fixed - these could be modified and offered as programmable features to allow enhanced flexibility.

VISUAL INDICATION

It is useful with any type of discharge measuring equipment to have a visual indication of what is being detected by the instrument.

SOFTWARE

The facilities presently offered could be reduced to allow further processing of the data by the iSBC 86/12A. Alternatively, the memory capacity of the 86/12A could be increased to allow the storage of a larger amount of software.

CONSTRUCTION

The equipment should be better "housed" and the cabling and interconnections between the various components can be improved.

4 CONCLUSION

The partial-discharge characteristics for a particular test condition and insulation arrangement can be of great importance in the choice of a suitable measurement system and in the interpretation of the readings. Previously, in studies of the current waveshapes of discharges in voids, the application of a computer has been limited by bandwidth considerations. The system presented offers a large bandwidth and sufficient flexibility to allow its use in numerous situations without further hardware modifications. In addition, the system has been designed to be particularly "user friendly" thus allowing system configuration to be achieved by pressing a few buttons rather than engaging in an extensive rewiring exercise.

Some of the advantages of this digital capture system are summarised below:

a. The system can be "user tailored" via software parameters.

b. The data can be recorded and processed more efficiently.

c. By their very nature, the digitally recorded are directly available for computer analysis.

d. The data captured can easily be related to time and voltage.

e. Calculations using discharge sequence parameters are simplified.

It is envisaged that the system presented in this report, serve only as a data capture instrument. To maximise the benefits of the digital nature of the data captured,

further processing is required, probably on a mainframe computer. With all the benefits offered, this system should prove an invaluable aid in partial-discharge analysis.

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APPENDIX 1 - MEMORY DESIGN

It was decided that 64K of memory would be sufficient to hold a useable quantity of sampled data. Initially it was felt that the memory chips had to be ordered as soon as possible, and hence, the memory design was oversimplified:

As the sampling rate is 10MHz the memory has to have a write cycle of less than 100ns. The Hitachi HM6147LP-3 1Kx1 bit memory has a write cycle of 55ns. The drawbacks involved became apparent after purchase. As the MC2710 offered 10 bits resolution, the memory bank has to be at least 10 bits wide. It was decided to include an extra bit to differentiate between timing data and sampled data. A 64K x 11 bit memory needed 176 chips - a prodigious number of chips which could have been avoided by using slower but larger (and cheaper) memory chips in an 'interlaced' memory bank. However, the speed offered by the Hitachi chips simplified the overall design.

MEMORY ADDRESS CIRCUITRY (see Sheet 3)

The address has to be calculated at speeds of up to 10MHz, and it has to be available to the memory chip for at least 55ns (including 10ns for write recovery). The obvious way to calculate the address is to use very fast binary counters. The 74S163 is a 4-bit counter that can operate at frequencies up to 70MHz. 4 of these counters are necessary to give a 16-bit address. The effective operating speed of these cascaded counters is 14MHz - 21MHz.

Because the address appearing on the counters is valid for so short period (see Figure 5 - Address on counters valid),

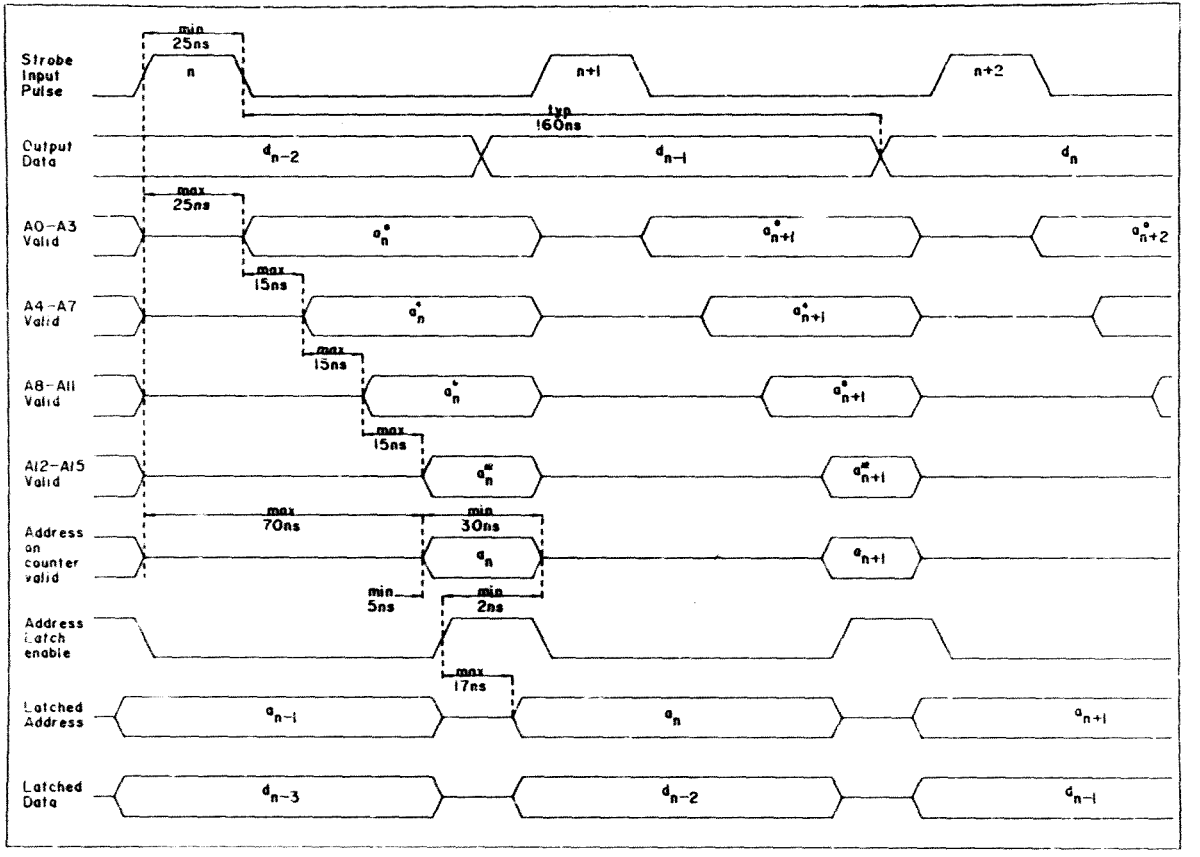

FIGURE 5. ADDRESS GENERATION TIMING

this has to be latched and held for addressing the memory, and at the same time the address has to be expanded to 20 bits to accommodate the addressing capabilities of 16 bit microprocessors. Two 74S374 latches (requiring a 5ns data setup time and 2ns data hold time) are used to hold the address formed on the counter outputs whilst a 74S373 is used to hold the expanded address portion.

The memory address space is from 20000H to 3FFFFH. Two 3-8 line decoders decode the addresses (see Sheet 10):

IC 87 decodes addresses 20000H - 2FFFEH
IC 88 decodes addresses 30000H - 3FFFEH

The data capture memory bank is only selected if /ADR13./ADR12.ADR11 = 1. The first 64K are addressed if ADR10 = 0 and the second if ADR10 = 1.

```
i.e. For IC 87 : G1 = /(ADR13+ADR12+/ADR11)
                 G2 = ADR10
     FOR IC 88 : G1 = ADR10
                 G2 = /(/ADR13./ADR12.ADR11)
     for both
                 Select A = ADRD
                 Select B = ADRE
                 Select C = ADRF
```

Memory	ADR							Y1								Y2								G	G	G	G
Address	1	1	1	1	F	E	D	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	1	1	2	2
	3	2	1	0																				1	2	1	2
20000	0	0	1	0	0	0	0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	1	0	0	0
22000	0	0	1	0	0	0	1	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	1	0	0	0
24000	0	0	1	0	0	1	0	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	1	0	0	0
26000	0	0	1	0	0	1	1	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	1	0	0	0
28000	0	0	1	0	1	0	0	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	1	0	0	0
2A000	0	0	1	0	1	0	1	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	1	0	0	0
2C000	0	0	1	0	1	1	0	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	1	0	0	0
2E000	0	0	1	0	1	1	1	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	1	0	0	0
30000	0	0	1	1	0	0	0	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	1	1	1	0
32000	0	0	1	1	0	0	1	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	1	1	1	0
34000	0	0	1	1	0	1	0	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	1	1	1	0
36000	0	0	1	1	0	1	1	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	1	1	1	0
38000	0	0	1	1	1	0	0	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	1	1	1	0
3A000	0	0	1	1	1	0	1	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	1	1	1	0
3C000	0	0	1	1	1	1	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	1	1	1	0
3E000	0	0	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	1	1	1	0

MEMORY ACCESS CONTROL CIRCUITRY (see Sheet 11)

The memory control circuitry can be divided into three parts:

a. Write control circuitry
b. Dual port access control circuitry
c. Control of memory access by iSBC 86/12A

WRITE CONTROL (during sampling)

For writing, the chip select (CS) and write enable lines (WE) must be synchronised with the addressing and data capture circuits. The CS line has to be LO for the entire write cycle, the address had to be valid for at least 45ns before the end of the write and remain valid for 10ns once the WE line has gone HI (see Fig. 6).

The WE line must only go LO if there is data available i.e. either sampled or timing data.

The memory is arranged in 16 banks of 11 bit words and the CS line is used to select which bank will be written to at any one time. The seven most significant address lines (using 19 address lines) are decoded to give a 1 in 16 selection.

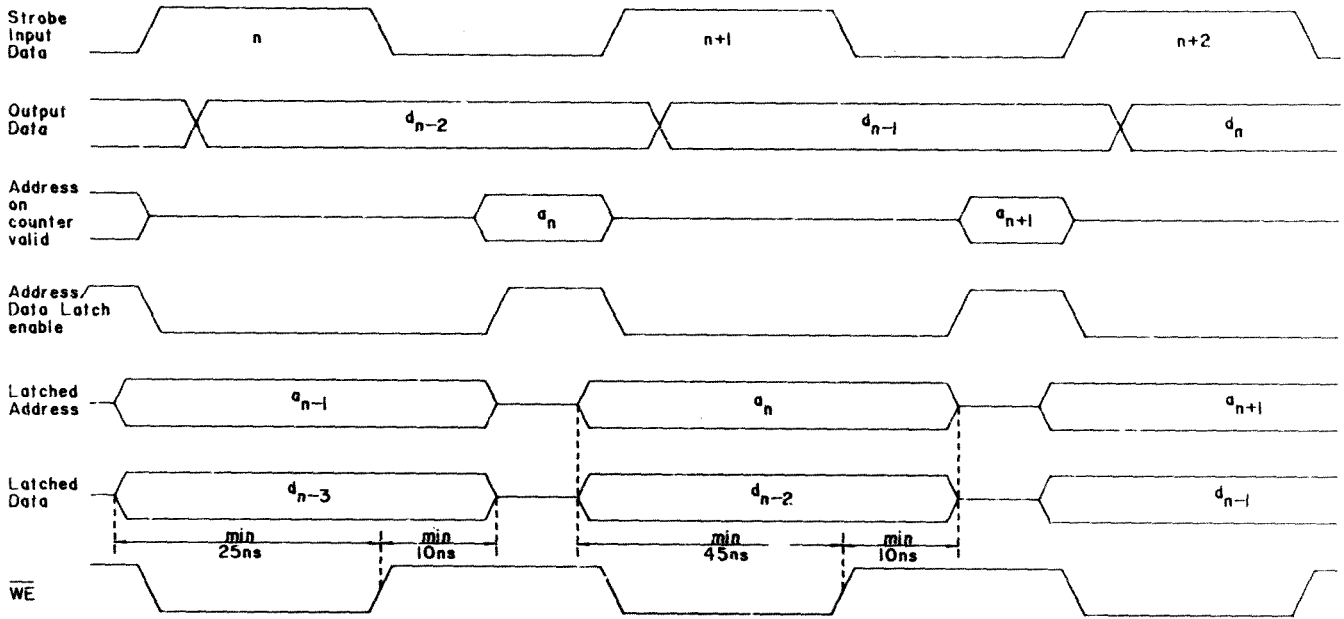

FIGURE 6. WE TIMING

DUAL PORT ACCESS CONTROL

As the RAM can be accessed by either the sampling circuitry or by the 8086, any possible contention must be avoided:

The sampling circuitry and the iSBC 86/12A present addresses (and data) to the memory on two separate sets of latches, only one of which is enabled at any time. Once sampling has commenced, the sampling circuitry has sole access to the memory, whilst before and after sampling, only the 8086 can access the memory.

ACCESS BY iSBC

It was decided to allow the 8086 to both write and read from the memory. Thus data has to be latched on bidirectional ports.

The decoding of the MWTC (Memory Write) and MRDC (Memory Read) lines is shown in Figure 7. As the memory used is very fast there is no necessity to add any further wait states during memory access (see iSBC Manual & Appendix 4)

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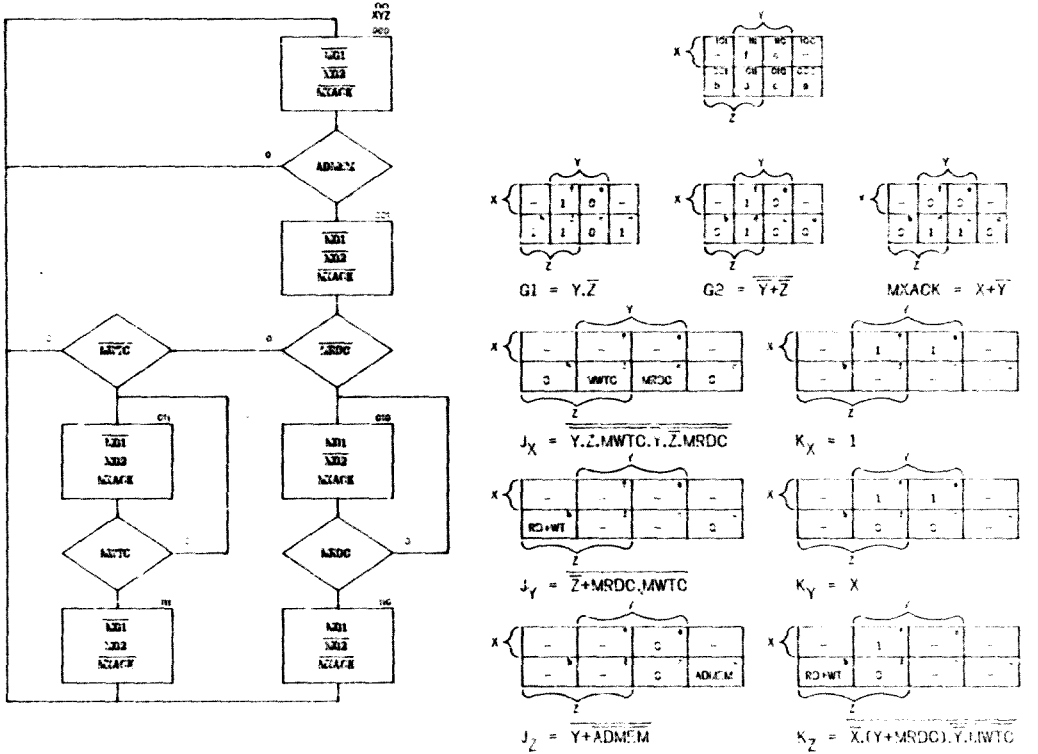


FIGURE 7. MEMORY ACKNOWLEDGE FSM

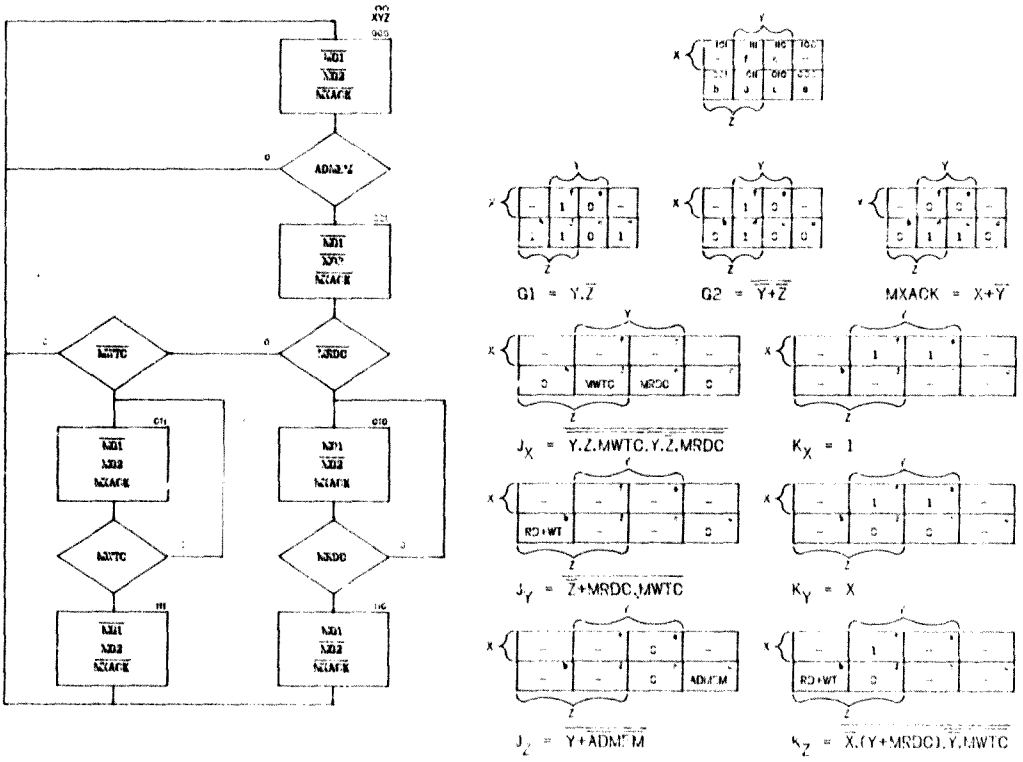


FIGURE 7. MEMORY ACKNOWLEDGE FSM

APPENDIX 2 - DATA CAPTURE CIRCUITRY

The data capture circuitry is divided into two sections. One that measures the discharge pulses and one that detects the zero-crossing of the AC signal.

PULSE CAPTURE & TRIGGERING (see Sheets 6 & 7)

The sampling must only commence once the pulse has risen above a given positive value or fallen below a given negative value. The 'pulse' is fed directly to two sets of comparators. One set triggers the data mechanism once the pulse has reached its positive threshold and the other triggers if it reaches the negative threshold. (These thresholds are soft programmable). The 'PULSE' line must be high for data capture to commence. Because of the delays introduced by the comparison, the PULSE line will only come HI a finite time after the ADC has actually captured the data (see Figure 8). Thus the data presented by the ADC must be held until the memory address lines have stabilised. This is done by passing the data through latches that are enabled once the previous data has been stored in memory (see Figure 6).

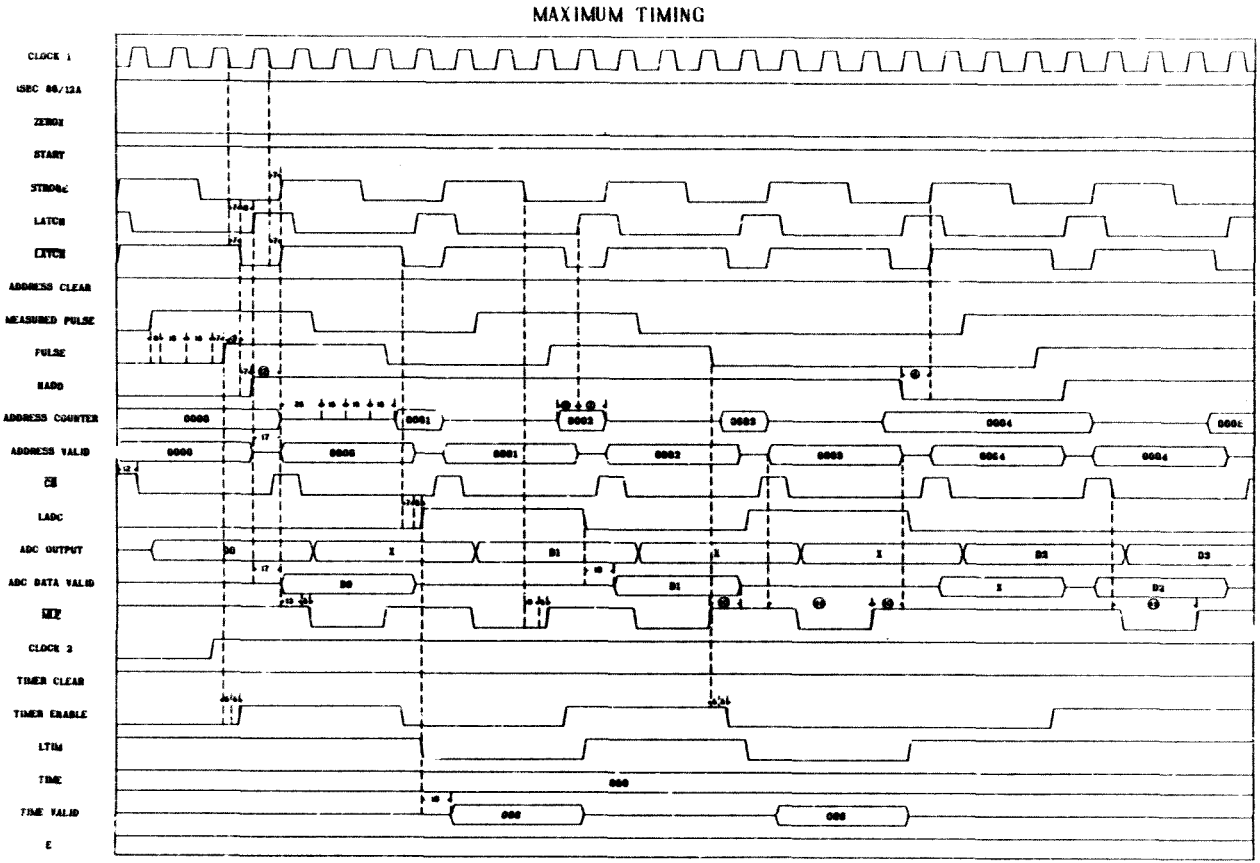


FIGURE 8. TIMING CONSTRAINTS

ZERO-CROSSING CIRCUITRY (see Sheet 9)

(cf. 'the Art of Electronics')

The circuit shown generates an output square wave for use with TTL logic (zero to 5V range) from an input wave of any amplitude up to 100 volts. R1, combined with D1 and D2, limits the input swing to between -0.6 and 5.6 volts approximately. Resistive divider R2/R3 is necessary to limit the negative swing to less than .3 volts, the limit for a 393 comparator. R5 and R6 provide hysteresis, with R4 setting the trigger points symmetrically about ground. The input impedance is nearly constant, because of the large R1 value relative to the other resistors in the input attenuator.

The output of the zero-crossing detector is fed through a monostable multivibrator with schmitt-trigger inputs, to give a 30ns pulse used to clear the timing counters, and also to synchronise the start of sampling with the 1st zero-crossing of the AC signal.

APPENDIX 3 - CONTROL CIRCUITRY

SUPERVISOR CIRCUITRY

This controls the address generation and the data capture. It is also responsible for ensuring that the memory control signals and the data/address inputs are synchronised. It starts the data capture operation when instructed to do so and then monitors the process to ensure that it stops before the memory overflows:

a. Measurements must commence with the first zero crossing (ZEROX - HI) of the AC waveform once the user has indicated (iSBC86/12A - HI) that sampling may start (see Figure 9). Measurements must cease once signalled by the user (iSBC86/12A - LO) or once the memory is full (ADROVR = HI).

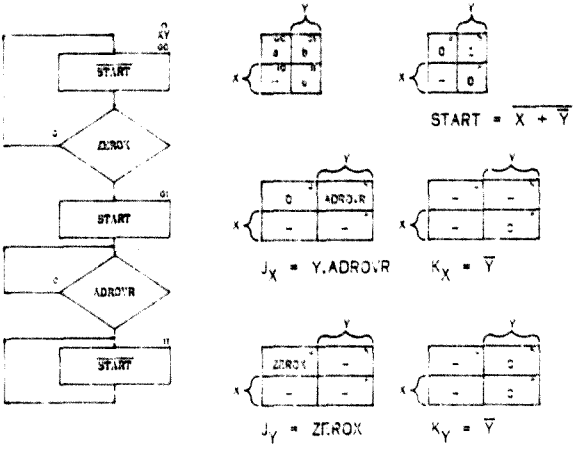
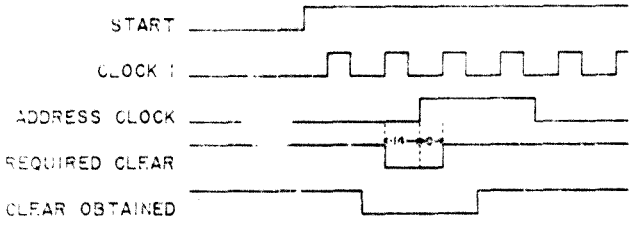
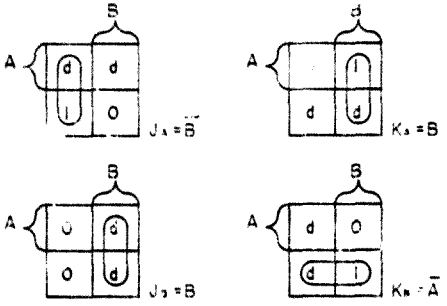


FIGURE 9. START SIGNAL SYNCHRONISATION

The address counters must be cleared to zero before data capture commences. This is achieved by ADCLR (see Figure 10)



A	B	J_A	K_A	J_B	K_B
1	1	d	1	d	0
0	1	0	d	d	1
0	0	1	d	0	d
1	0	d	0	0	d
1	0	d	0	0	d



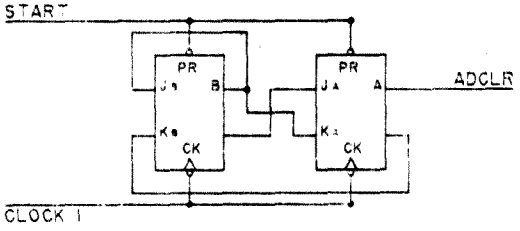


FIGURE 10. ADDRESS COUNTER CLEAR

c. Once enabled, the system must only record data whilst a discharge is detected. In addition to the pulse data, timing information must also be recorded. The necessary synchronisation and control is performed by six lines:

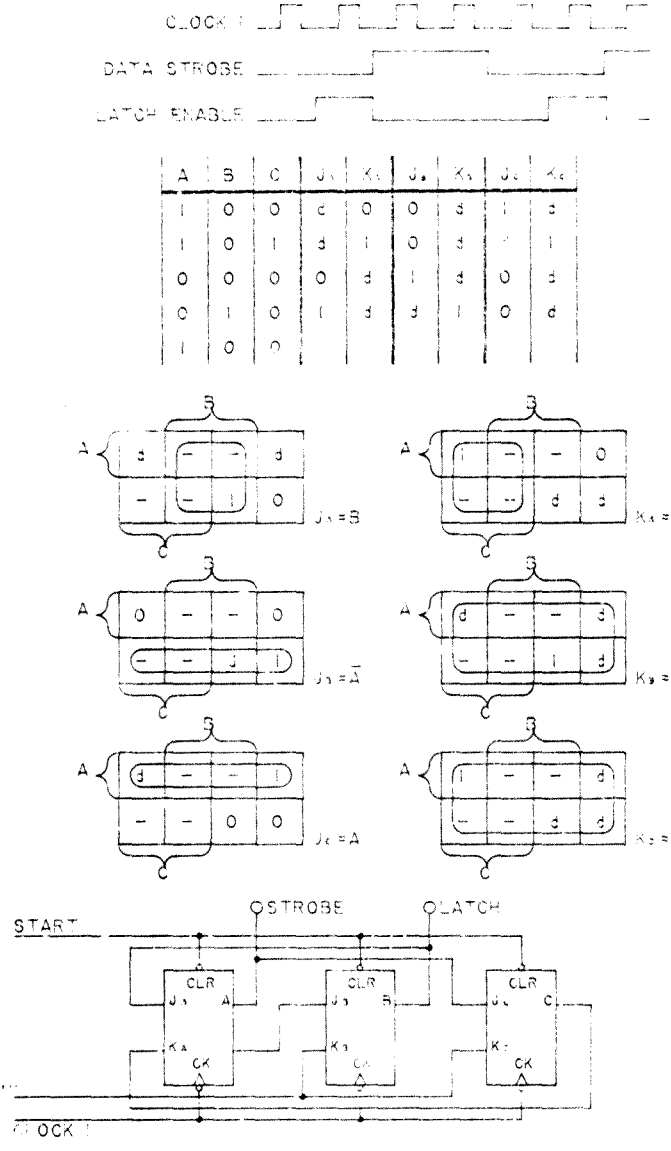
START : Allows data capture to commence.

STROBE : Strobes the ADC. The ADC must be be pulsed at speeds ranging from 1MHz to 10MHz. If the latch enable is HI for 25ns out of every 100ns (see Figure 11), the circuit can be driven by a 40MHz clock with strobe line HI for two out of four clock cycles and the latch enable HI for one of the 4. From Figure 16) it can be seen that if the strobe pulse were extended by +/-20ns and then inverted, it could serve as a WE line.

LATCH : Latches address and data. The address must be latched between 70 and 100ns after the rising edge of the strobe input pulse (see Figure 5). To achieve maximum overlap of the data and address fields, the data is latched at the same time as the address.

The following conditions must be met:

- The address must remain valid for at least 10ns after the WE line has gone HI (see Figure 6).
- The chip select lines (CS) must be LO for at least 45ns before the end of the write (see Figure 8).
- The data must be presented to the memory at least 25ns before WE goes HI and must remain these for at least 10ns after WE has gone HI (see Figure 6)



A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
1	0	0	d	0	0	d	1	d
1	0	1	d	1	0	d	1	1
0	0	0	0	d	1	d	0	d
0	1	0	1	d	d	1	0	d
1	0	0						

FIGURE 11. DATA STROBE & LATCH ENABLE GENERATION

HADD : enables the counters as soon as a pulse is detected and keeps them enabled for 100ns after the pulse has disappeared to allow the timing data to be stored. (see Figures 8 & 12)

LADC : enables the pulse data to be presented on the data lines during a discharge (see Figure 12).

LTIM : enables the timing data onto the data lines immediately after the pulse has vanished (see Figure 12).

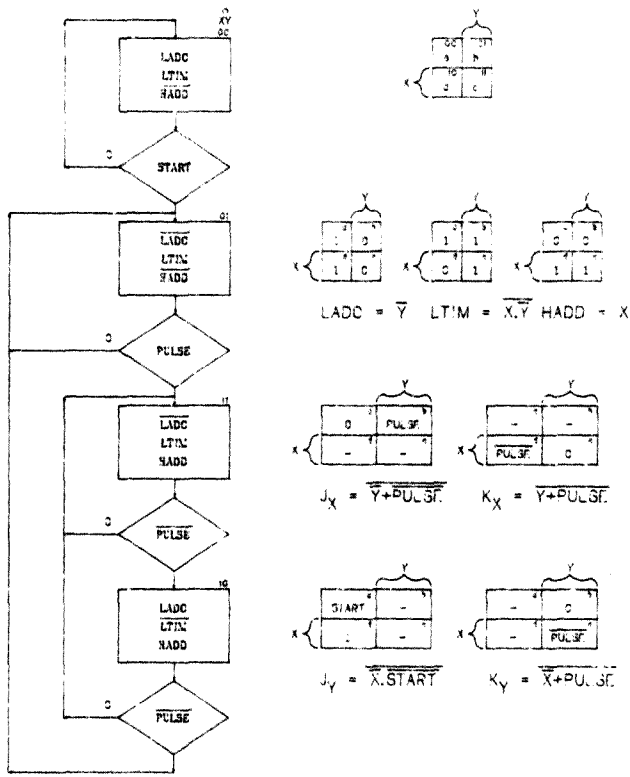


FIGURE 12. LADC, LTIM, & HADD FSM

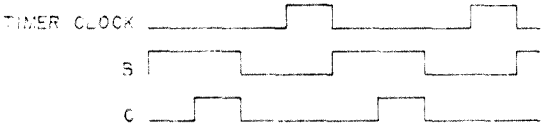
TIMING CIRCUITRY (see Sheet 5)

The data for each pulse must be stored with an indication of where the pulse occurred relative to the AC signal. The 10 bit wide memory word allows the AC wavelength to be divided into 1024 time slots e.g. a 60Hz wave could be divided into 1024 16,3us time slots. Obviously, the clock controlling the timing circuitry has to operate at a speed dependent on the AC frequency.

The time is "counted" on three cascaded 4-bit binary counters. These must be cleared asynchronously on every zero-crossing (+ve) of the AC signal and the value that appears on the counters when a pulse is detected, must be stored and presented on the data lines once the pulse has disappeared (see LTIM).

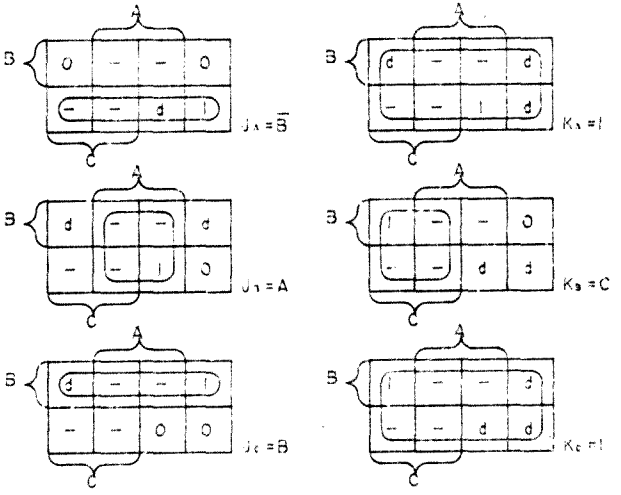
Because the AC wave and pulse occurrence are not synchronised, some mechanism must prevent the timing data from being updated whilst it is being stored in memory. The output from the counters is latched on level-triggered tri-state latches before being presented to the memory. The input to the latches is only enabled whilst a pulse is present if the counters are not being clocked. The latches must have a 10ns hold time before the counters are clocked (see Figure 13).

It is, however, conceivable that the pulse might end +/-6ns after the clock line has dropped and the length of the latch enable pulse would be too short to guarantee the values input to the latch. The hardware to avert this problem is unnecessarily complicated as post-processing software can "weed" out these glitches. An edge-triggered latch would go a long way in solving this problem but would introduce the possibility of the counters not being reset to zero at the next zero-crossing.



TIMER ENABLE = $\overline{START}$ + PULSE . F

A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	1	0	0	d	d	0	1	d
0	1	1	0	d	d	1	d	1
0	0	0	1	d	0	d	0	d
1	0	0	d	1	1	d	0	d
0	1	0						



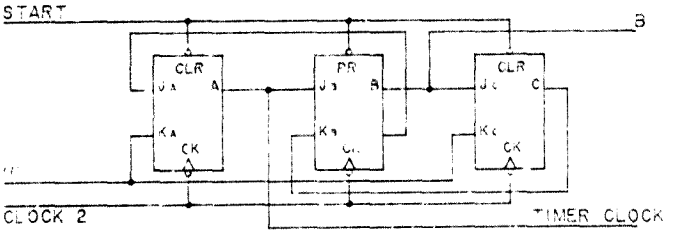


FIGURE 13. TIMER ENABLE

CLOCK CIRCUITRY (see Sheets 1 & 4)

The design of the Supervisor Clock will be described - the Timing Clock is similar.

The sampling frequency is variable between 1MHz and 10MHz. Because of the divider circuitry used for the ADC strobe pulse the driving clock must run at speeds from 4MHz to 40MHz. To achieve this very wide frequency range with a reasonably stable output, a phase-locked loop was used (see TTL Data Book - Typical Application Data for 74S124):

With fixed division rates for both M and N (see Figure 14),

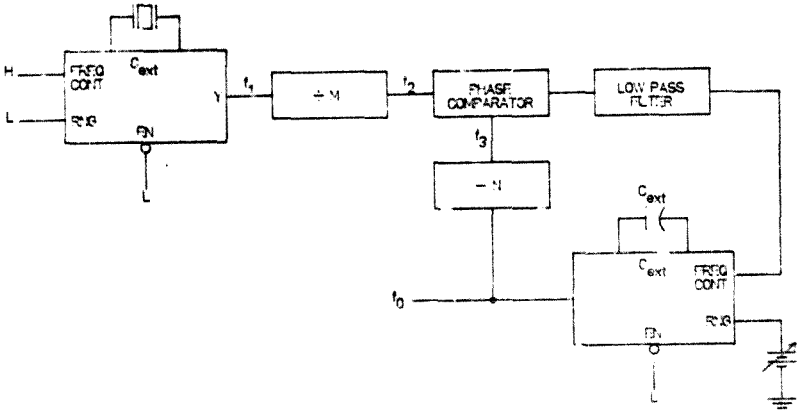


FIGURE 14. BASIC PHASE LOCKED LOOP

the output frequency (F_{ot}) will be stable at $F_{ot} = (N/M)F_{in}$. To allow F_{ot} to be as variable as possible, obviously both M and N must be allowed to take on a wide range of values. Using a synchronous 6-bit binary

multiplier (7497) $F_{ot} = (MF_{in})/64$ and can thus be varied from 0 to $(63/64)F_{in}$. Using an exclusive-or (IC4),a phase comparator, an RC low pass filter (see Figure 15)

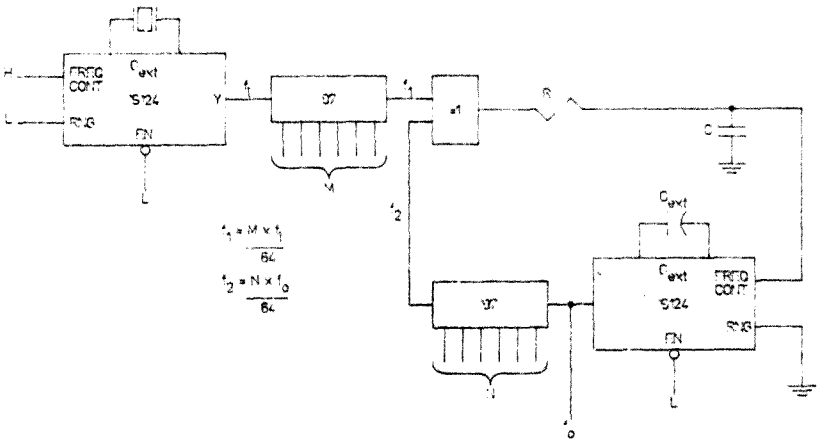


FIGURE 15. PHASE LOCKED LOOP WITH RC FILTER

and J-K flip-flops to "clean" the output of the 7497 before it enters the comparator. 4MHz <= F_{ot} <= 40MHz (see Sheet 1) but the maximum input clock frequency of the '97 is 25MHz. Thus F_{ot} must be halved before driving the 7497 - this is achieved with another J-K flip-flop.

Therefore $(M*F_{in})/64 = (N*F_{ot})/128$ $\quad 1 <= N <= 63$

$F_{ot} = (2*M*F_{in})/N$ $\quad 1 <= N <= 63$

Thus 0MHz <= F_{ot} <= $126*F_{in}$

But the output frequency of th 'S124 has a limited range e.g. for F_{ot} = 50MHz and Cext = 8pf and with Vi_{rng} = 5V

for Vi_{freq} = 1V, F_n +/- .42 => F_{o1} +/- 21MHz

Vi_{freq} = 5V, F_n +/- 1.2 => F_{o5} +/- 60MHz

Thus to achieve the full range of 4MHz to 40MHz, F_{ot} must be further divided. This is achieved by passing F_{ot} through a 4-bit counter (IC7). The outputs of which are demultiplexed to select the required frequency.

For 21MHz <= F_{ot} <= 60MHz

With S = 000, 21MHz <= CLOCK1 <= 60MHz

001, 10.5MHz <= CLOCK1 <= 30MHz

010, 5.25MHz <= CLOCK1 <= 15MHz

011, 2.625MHz <= CLOCK1 <= 7.5MHz

100, 1.3125MHz <= CLOCK1 <= 3.75MHz

As the frequency range of CLOCK1 now exceeds the required range, the variance of F_n can be reduced. i.e. .48 <= F_n <= .99 so Vi_{freq} need only range from 1.4V (24MHz) to 4.7V (50MHz).

APPENDIX 4 - INTERFACE

The pulse capture circuitry must be interfaced to the iSBC 86/12A and the HP2645A

iSBC 86/12A INTERFACE

In addition to the memory interfacing, the iSBC 86/12A is required to transmit the following data to the sampling circuitry:

a. The sampling rate
b. The AC signal frequency
c. The upper and lower values for triggering
d. Signals to start and stop sampling

At the same time, the sampling circuitry gives the following signals to the iSBC 86/12A:

a. An indication that the memory is full.
b. The zero-crossings of the AC signal so that the AC frequency might be ascertained.

The necessary signals are passed through three 8255 programmable interface chips located in the IO address space XXX00H -> XXX3EH (further decoding is not done as the IO address space is not fully utilised).

Each PPI has four addresses:
A1 A0
0 0 = DATA BUS - PORT A
0 1 = DATA BUS - PORT B
1 0 = DATA BUS - PORT C
1 1 = DATA BUS CONTROL
and these must be located at even-word boundaries in the iSBC 86/12A address space.

i.e. PPI 1 'resides' at I/O addresses XXX00H
XXX02H
XXX04H
XXX06H

Each PPI has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines (borrowing one from the other group) for handshaking. Data is transferred to and from external I/O devices through three 8-bit ports known as port A (PA0-PA7), port B (PB0-PB7), and port C (PC0-PC7).

The eight data lines of the PPI's are connected to the 8 least significant multibus data lines.

All PPI's are operated in MODE 0 with PORT's A, B and PORT C (lower) being selected as output ports. In PPI 1 PORT C (upper) is used as an output port.

PPI PORT ADDRESSES

PPI 1 - Write/Read	: Port A	: 00
PPI 1 - Write/Read	: Port B	: 02
PPI 1 - Write/Read	: Port C	: 04
PPI 1 - Write	: Control	: 06
PPI 2 - Write/Read	: Port A	: 08
PPI 2 - Write/Read	: Port B	: 0A
PPI 2 - Write/Read	: Port C	: 0C
PPI 2 - Write	: Control	: 0E

```
PPI 3 - Write/Read : Port A                    : 10
PPI 3 - Write/Read : Port B                    : 12
PPI 3 - Write/Read : Port C                    : 14
PPI 3 - Write      : Control                   : 16
```

PPI FUNCTIONS

```
PPI 1 (IC61 - sheet 1)
Port A          - Mode 0 Output : C1I0 - C1I5 (A0 - A5)
Port B          - Mode 0 Output : C1O0 - C1O5 (B0 - B5)
Port C (lower)  - Mode 0 Output : C1S0 - C1S2 (C0 - C2)
Port A (upper)  - Mode 0 Output : ZEROX        (C5)
                                  TIMOVR       (C6)
                                  ADROVR       (C7)

PPI 2 (IC62 - sheet 4)
Port A          - Mode 0 Output : C2I0 - C2I5 (A0 - A5)
Port B          - Mode 0 Output : C2O0 - C2O5 (B0 - B5)
Port C (lower)  - Mode 0 Output : C2S0 - C2S3 (C0 - C3)

PPI 3 (IC63 - sheet 7)
Port A          - Mode 0 Output : UL0 - UL7    (A0 - A7)
Port B          - Mode 0 Output : LL0 - LL7    (B0 - B7)
Port C (lower)  - Mode 0 Output : UL8,UL9      (C0,C1)
                                  LL8,LL9      (C2.C3)
```

When the CPU is accessing off-board memory (or I/O) via the Multibus Interface, the CPU must first gain control of the Multibus interface and after giving the command it must wait for the Transfer Acknowledge (XACK/) to be received (see Ref. 12). The 8255A requires a 400ns write cycle. This is achieved by holding the IOXACK line LO for 400ns after the write cycle has been initiated (see Figure 16).

HP2645A DISPLAY STATION INTERFACE

The iSBC 86/12A has an RS232C compatible serial I/O port controlled by an 8251A USART (Universal Synchronous/-Asynchronous Receiver/Transmitter) chip.

Thus communication with the HP2645A is EIA RS232-C serial synchronous, full duplex ASCII. Transmission is at 9600 bits per second, the necessary clock rates (for the iSBC USART) are supplied by an onboard programmable rate/time generator.

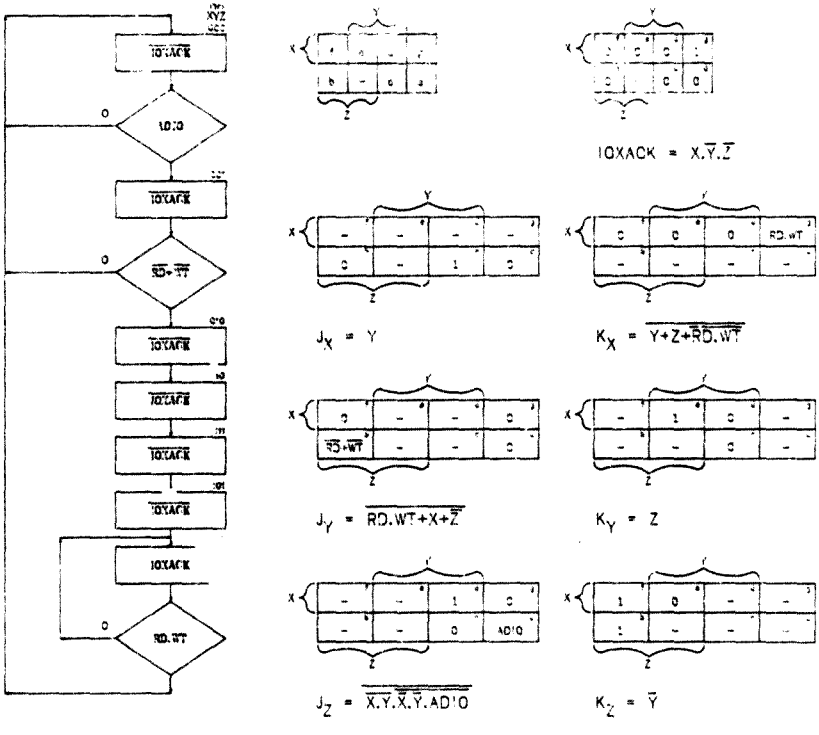


FIGURE 16. IOXACK FSM

APPENDIX 5 - iSBC 86/12A

The iSBC 86/12A Single Board Computer, which is a member of Intel's complete line of 8- and 16-bit single board computer products, is a complete computer system on a single printed-circuit assembly. The iSBC 86/12A board includes a 16-bit central processing unit (CPU), 32K bytes of dynamic RAM, a serial communications interface, three programmable parallel I/O ports, programmable timers, priority interrupt control, Multibus interface control logic, and bus expansion drivers for interface with other Multibus interface-compatible expansion boards.

iSBC 86/12A JUMPER CONFIGURATION

ROM/EPROM Configuration
Using 2732 EPROM chips:
Legal EPROM addresses : 0FC000H - 0FFFFFH
Legal RAM addresses : 0000H - 7FFFH
Jumpers E94 - E96 & E97 - E99 are inserted

No Wait Option
Jumper E3 - E4 is removed to create wait states after ROM/EPROM reads

Bus Clock
Jumper E105 - E106 routes the Bus Clock signal /BCLK to the multibus interface

Constant Clock
Jumper E103 - E104 routes the Constant Clock signal /CCLK to the multibus interface

Timer Input Frequency

Counter 0 has a 1.23MHz input frequency (E57 - E56)
Jumper E59 - E61 connects Counter 0 and Counter 1 in series in which the output of Counter 0 serves as the input clock to Counter 1.

Counter 2 will be the 8251A Baud Rate Clock with a 1.23MHz input frequency (E5 -E61)

Priority Interrupts

Counter 1 output (TIMR1) is connected to the 8259A PIC IR0 input (E91 - E81)

Programmable Peripheral Interface

PPI 0 - Write/Read	: Port A (J1)	: C8
PPI 0 - Write/Read	: Port B (J1)	: CA
PPI 0 - Write/Read	: Port C (J1)	: CC
PPI 0 - Write	: Control	: CE

Priority Interrupt Controller

PIC - Write	: ICW1, OCW2, OCW3	: C0 or C4
PIC - Read	: Status and Poll	: C0 or C4
PIC - Write	: ICW2, ICW3, ICW4, OCW1(mask)	: C2 or C6
PIC - Read	: OCW1(mask)	: C2 or C6

Although the system is presently not interrupt driven, this facility can be included - e.g. for interrupting at the end of the sampling period.

Programmable Interface Timers

PIT - Write/Read	: Counter 0	: D0
PIT - Write/Read	: Counter 1	: D2
PIT - Write/Read	: Counter 2	: D4
PIT - Write	: Control	: D6

Counters 1 & 0 are used to time the sampling period and to determine the AC signal frequency.

Counter 2 serves as the 8251A Baud Rate Clock

USART

USART - Write/Read	: Data (J2)	: D8 or DC
USART - Write	: Mode or Command	: DA or DE
USART - Read	: Status	: DA or DE

Used for communications with HP2645A.

APPENDIX 6 - HP 2645A

The HP2645A display station uses a microprocessor under firmware control. It operates in character or block mode, with full editing capability. The terminal is designed for such applications as data entry and preparation, information display and editing, interactive programming, data communications, and time-sharing operations. In addition to the facilities of the basic terminal, the HP2645A also provides an integrated mass storage capability of up to 220 kilobytes of data using two tape cartridges.

KEYBOARD INTERFACE STRAPPING OPTIONS FOR POINT-TO-POINT COMMUNICATIONS ON HP2645A

STRAP	FUNCTION
A - OPEN	The escape code sequences generated by all keys are transmitted to the computer
B - CLOSED	Spaces typed will overwrite existing characters
C - CLOSED	At the end of each line, a local Carriage Return and Line Feed are generated.
D - CLOSED	The terminal is set to transfer a line at a time in Block Mode.
E - CLOSED	When the READ key is pressed with AUTO/LF key latched down, each tape record begins with an LF and is terminated by a CR.

F - OPEN — When an ESC e (Fast Binary Read) is issued by the computer, the baud rate is switched automatically to 9600 baud (if the terminal is equipped with cartridge tape units).

G - OPEN — All Block Mode transfers (i.e., cursor sense, terminal and device status, device I/O responses, display memory, and function keys) are preceded by a DC2. The terminal sends the DC2 upon receipt of a DC1 from the computer. After the CPU receives the DC2 from the terminal, another DC1 is required to trigger transmission of data from the terminal.

H - CLOSED — During Block Mode Handshake transfers, the terminal sends a DC2 in response to a DC1 prior to sending data. (See Block Transfer Handshake strapping above.)

R - OPEN — The transition from receive state to transmit state occurs after CB (106) (Clear to Send) goes on.

S,T - CLOSED — Reverse Channel protocol (both switches closed).

U - OPEN — The terminal ignores all transitions on the SR (122) (Secondary Receive Data) line from the modem in the transmit state.

V - OPEN — Transitions of CF (109) (Carrier Detect) line have no effect on the terminal.

W - CLOSED — Enables DATA COMM SELF TEST from either the keyboard or escape sequence.

X - CLOSED Holds data speed signal low (CH (111) =0).

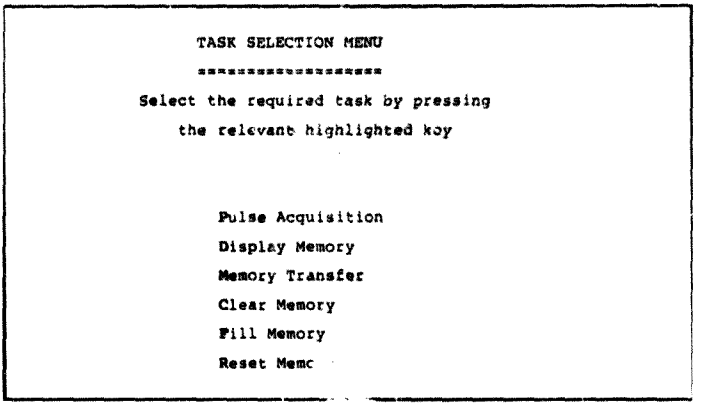
Y - CLOSED The TRANSMIT light on the keyboard il turned on when CB (106) (Clear to Send) line from the modem is high. It is turned off when the CB (106) line goes low.

The HP2645A is set to operate in full duplex, even parity mode at 9600 baud.

APPENDIX 7 - USER MANUAL

The user must proceed as follows:

1. Connect the data capture system to the signal to be measured.
2. Power-up the data capture system
3. The following menu will appear on the HP2645A screen



To tune the various parameters the user should press "P" (whilst the Task Selection Menu is displayed) and the following menu will appear:

```
                    SELECTION MENU
                    ==============
          Select the required item by pressing
              the relavant highlighted key


Sampling Rate                                : 10'
Upper voltage limit for pulse triggering     : .  .ts
Lower voltage limit for pulse triggering     : -.1Volts
Time limit for pulse triggering              : 1 seconds
Perform sampling
Exit from this menu
```

To adjust the sampling rate, press "S" (in the Selection Menu)

```
                    SAMPLING RATE MENU
                    ==================
The current sampling rate is 10MHz, should you wish to change
this you may select the required range by pressing the relevant key.
Fine adjustment is achieved by pressing either "I" to increase
the sampling rate, or "D" to decrease the sampling rate


                    1 - 2MHz
                    2 - 3MHz
                    3 - 4MHz
                    4 - 5MHz
                    5 - 6MHz
                    6 - 7MHz
                    7 - 8MHz
                    8 - 9MHz
                    9 - 10MHz
                    Increase sampling rate
                    Decrease sampling rate
                    Exit from this menu
```

Pressing "I" or "D" will increase or decrease the sampling frequency by approximately .002MHz.

To adjust the upper triggering voltage press "U" (in the Selection Menu)

```
                    UPPER LIMIT
                    ===========
The current upper limit for triggering the pulse
sampling mechanism is .1 Volts, should
you wish to change this  enter the new limit,
otherwise press the SPACE bar. The limit must lie
between 0 and 0.5 Volts.
```

The user must enter the upper limit (eg .49) followed by "RETURN"

To adjust the lower triggering voltage press "L" (in the Selection Menu)

```
                    LOWER LIMIT
                    ===========
The current lower limit for triggering the pulse
sampling mechanism is -.1 Volts, should
you wish to change this, enter the new limit,
otherwise press the SPACE bar. The limit must lie
between 0 and -0.5 Volts.
```

The user must enter the lower limit (eg -.49) followed by "RETURN"

To enter the sampling period time limit press "T" (in the Selection Menu)

```
                    TIME LIMIT
                    ==========

For how long do you wish to sample?
The present time limit is 1 seconds.
Should you wish to change this,
please enter the new limit, in seconds,
otherwise press the SPACE bar. The new limit
should lie between 0.1 and 300 seconds.
```

The user must enter the time limit (eg 100) followed by "RETURN"

Pressing "P" (in the Selection Menu) will cause sampling to commence and run until the memory is full or the time limit expires

```
                    SAMPLING
                    ========


Sampling Rate                                  : 10MHz
AC Frequency                                   : 60KHz
Upper voltage limit for pulse triggering       : .1Volts
Lower voltage limit for pulse triggering       : -.1Volts
Time limit for pulse triggering                : 1 seconds
```

The user may display the contents of the memory by pressing "D" whilst the Task Selection Menu is on the screen

```
                    MEMORY DISPLAY
                    ==============

Enter the segment (2 or 3), start address and
end address of the portion of memory you wish to view
eg. 2:000,00FF
Enter "E" as the segment to exit
Pushing "S" will stop the display, SPACE will continue it,
and "Q" will quit it
```

To store memory onto tape or restore the contents of memory from tape, press "M" in the Task Selection Menu

```
                MEMORY TRANSFER
                ===============

          T : store data on tape
          C : restore data from tape
          E : to exit
```

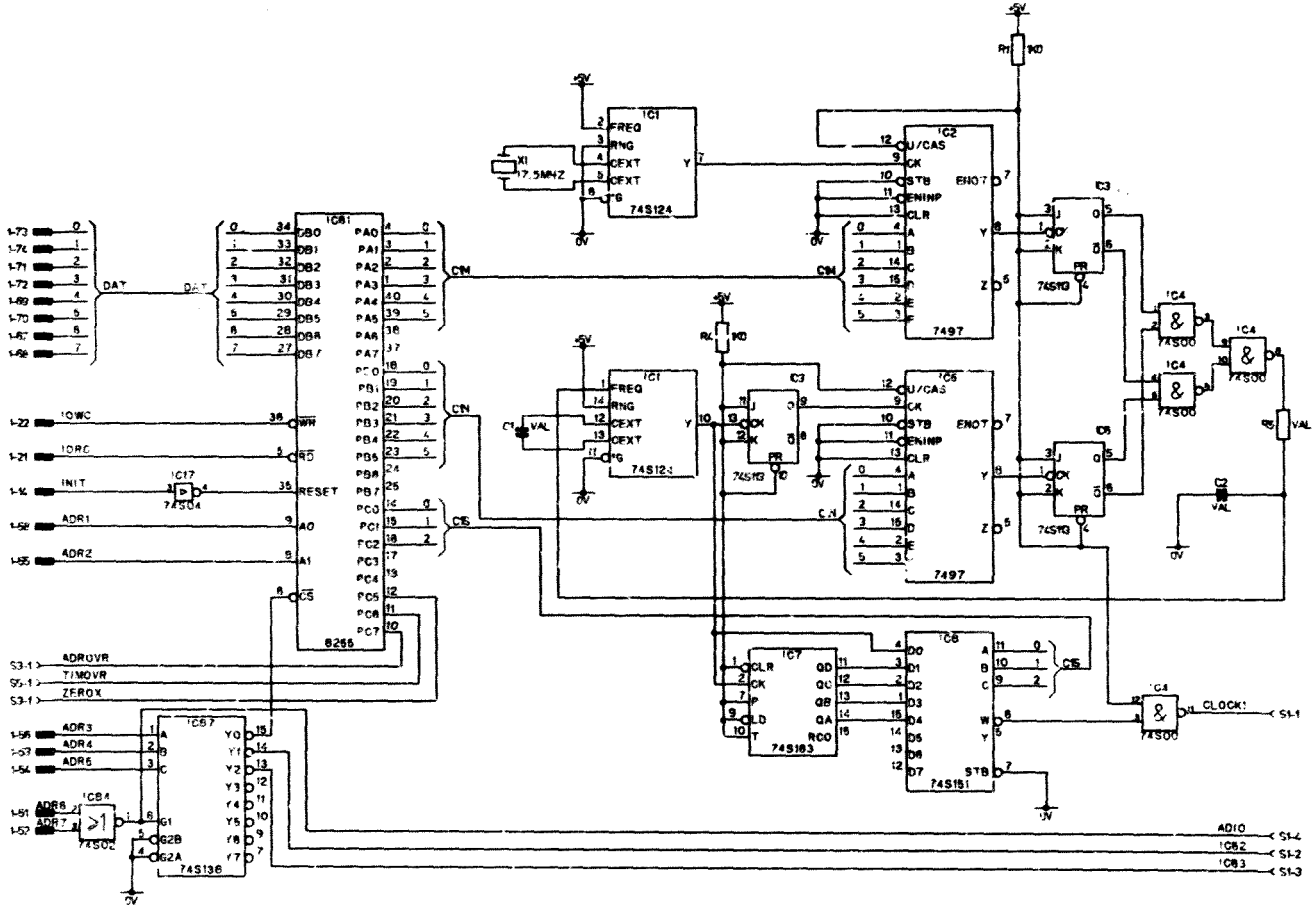
Press "T" to store memory

```
                 STORE MEMORY
                 ============

          1 : store first memory segment
          2 : store second memory segment
          B : store both memory segments
          E : to exit
```

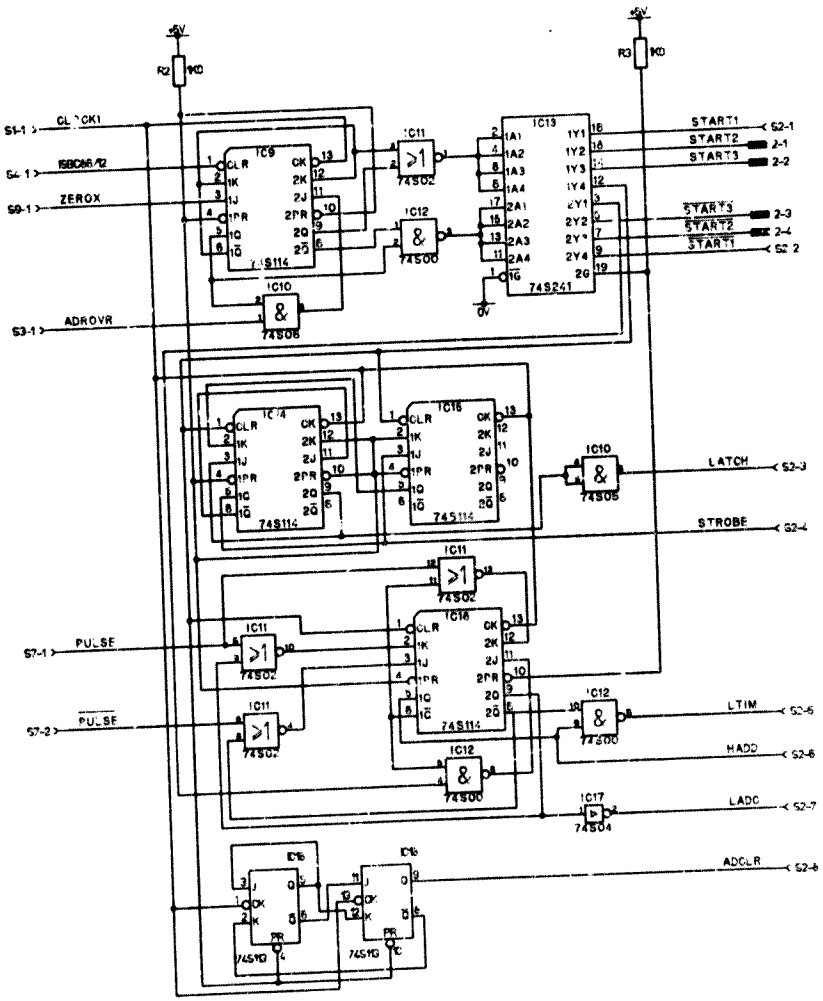
OR press "C" to restore memory

```
                RESTORE MEMORY
                ==============

          1 : restore first memory segment
          2 : restore second memory segment
          B : restore both memory segments
          E : to exit
```

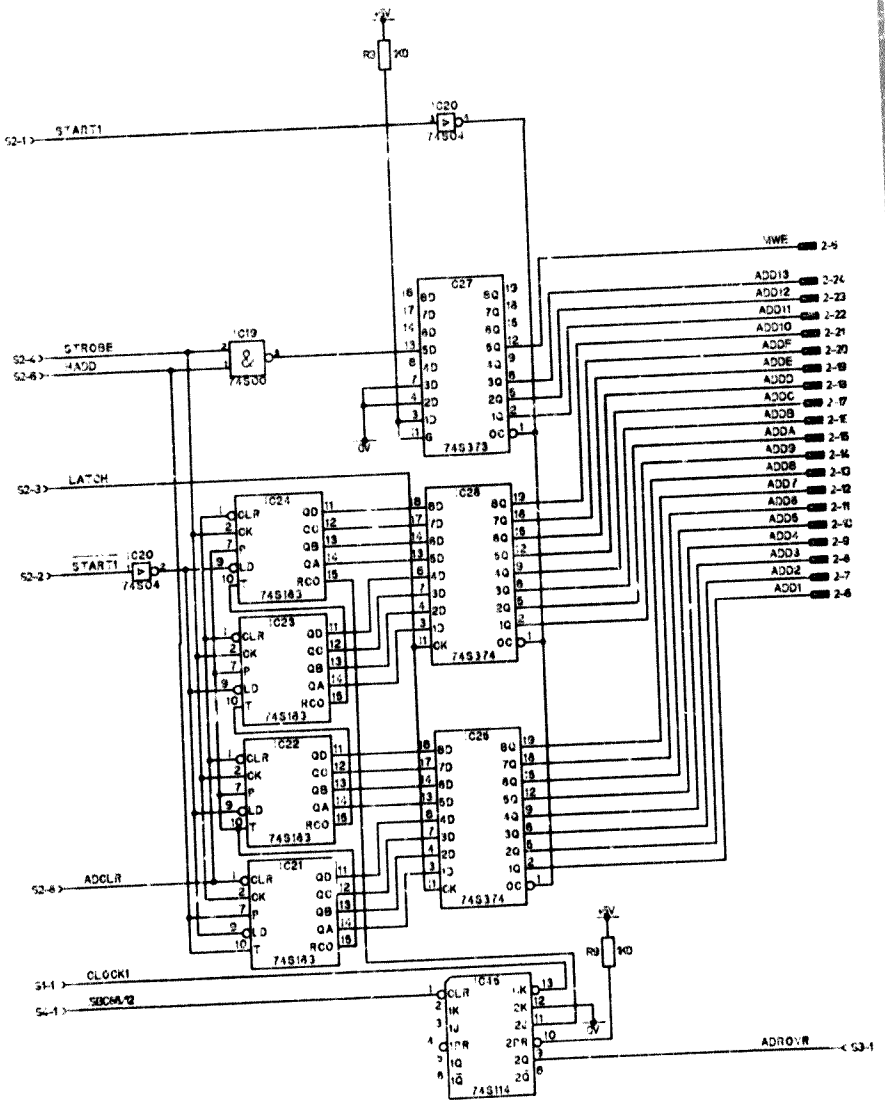
APPENDIX 8 - WIREWRAP BOARD LAYOUTS & CIRCUIT DIAGRAMS



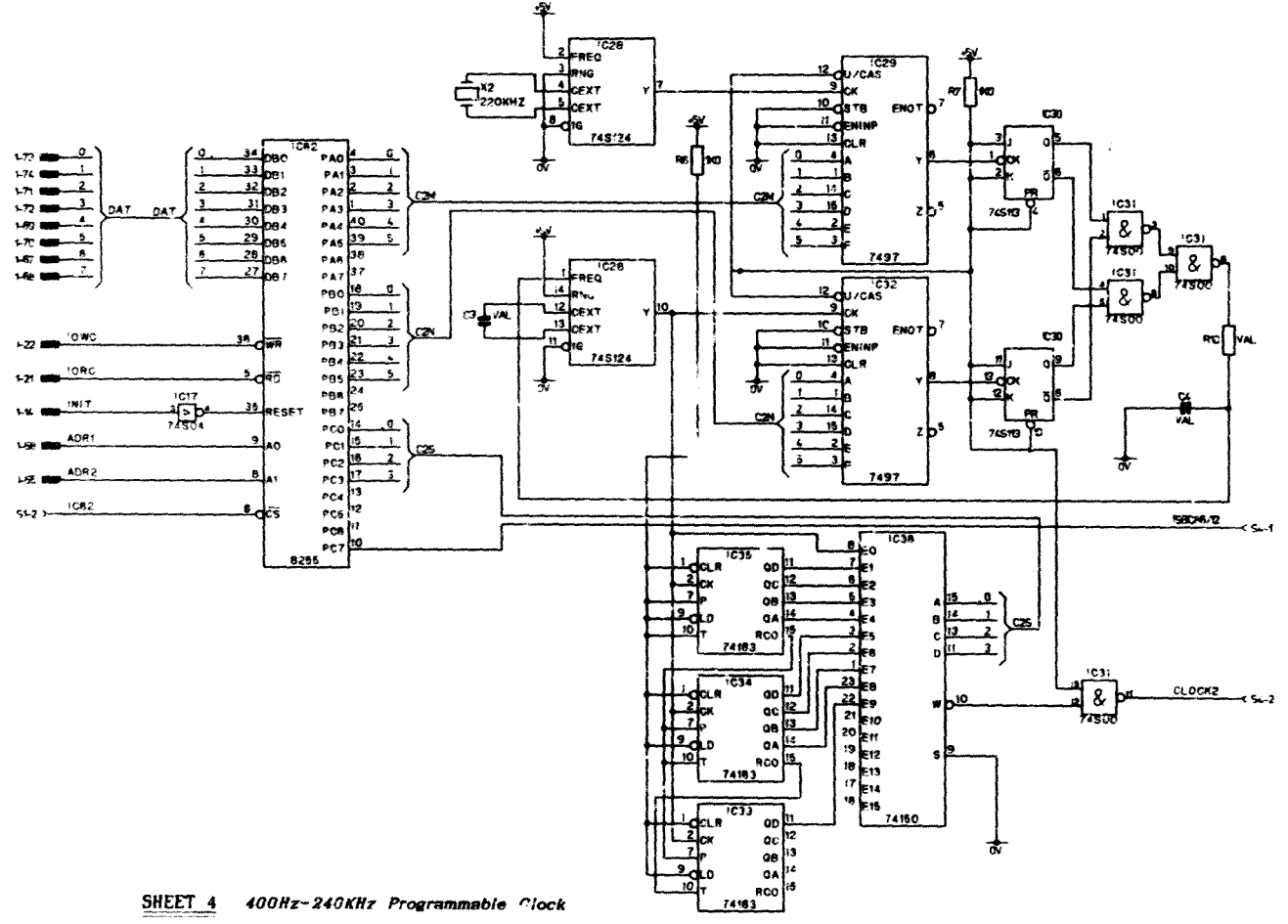
SHEET 1 *4-40MHz Programmable Clock*



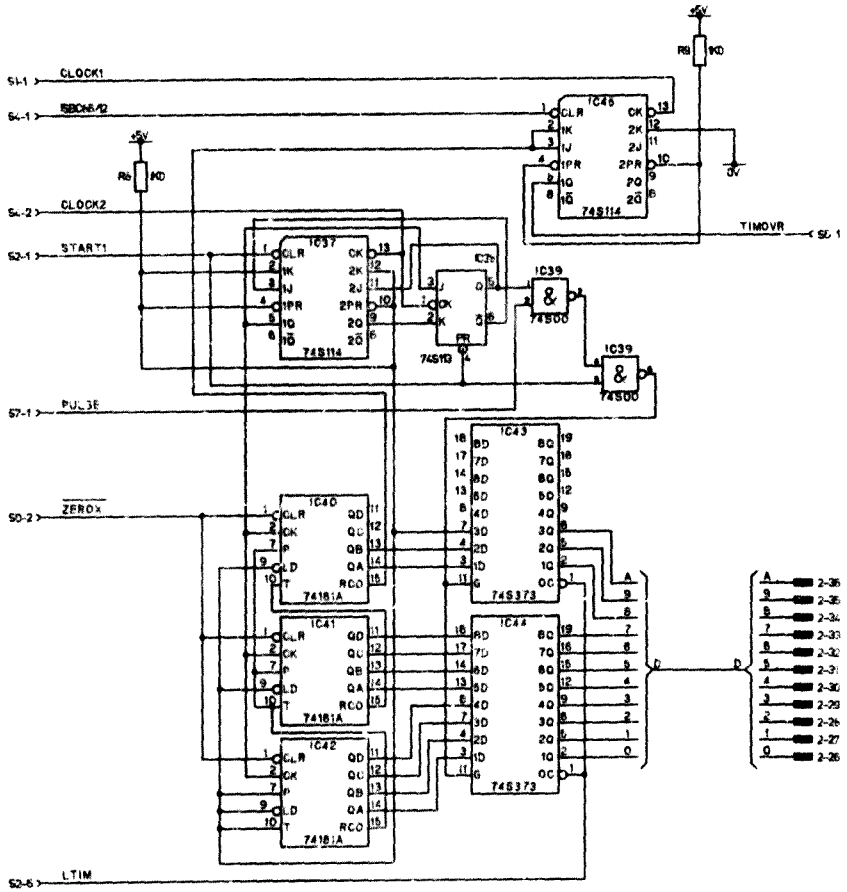
SHEET 2 *Supervisor Circuitry*



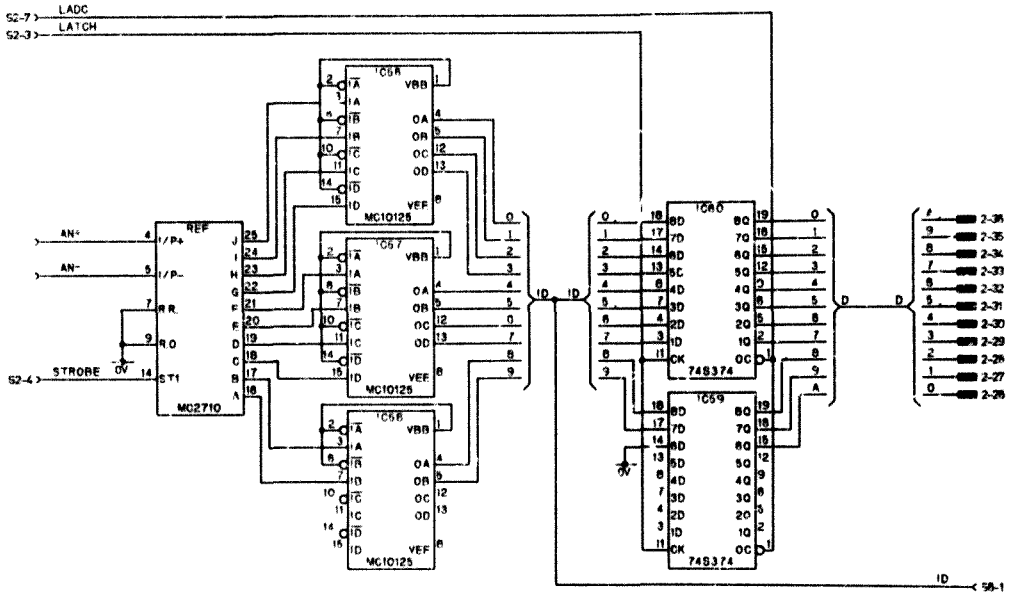
SHEET 3 *Address Generation Circuitry*



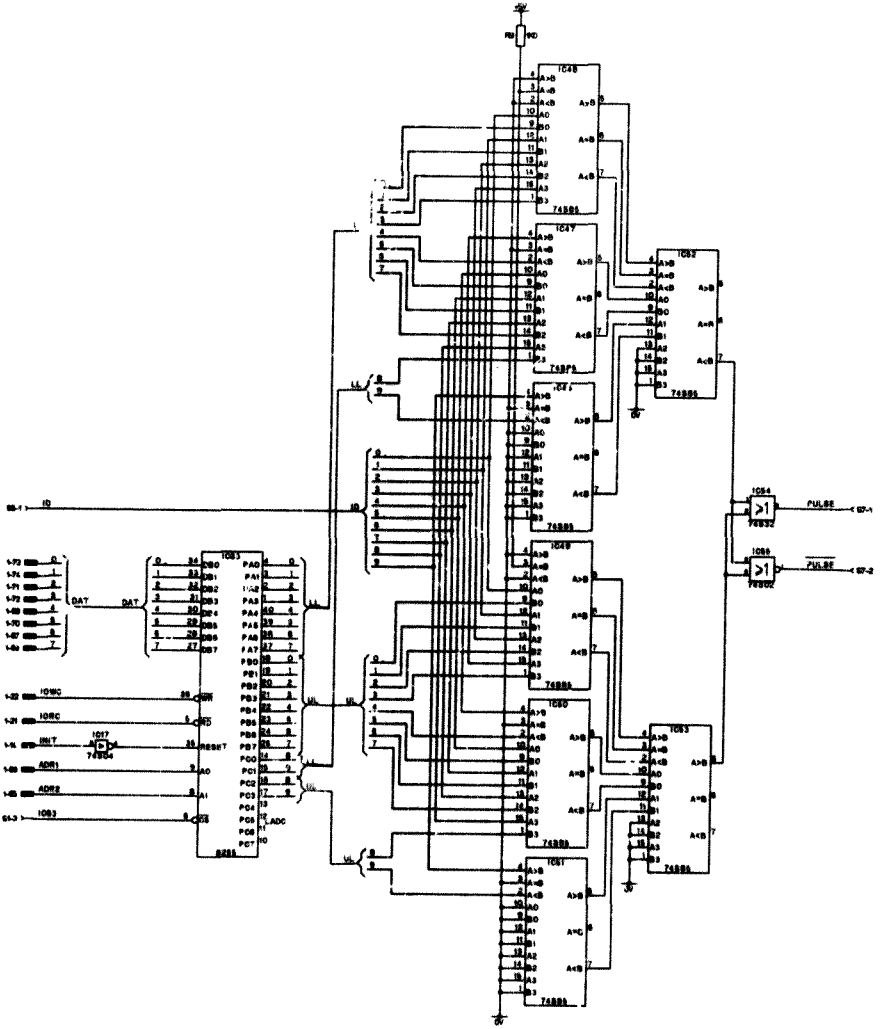
SHEET 4 *400Hz-240KHz Programmable Clock*



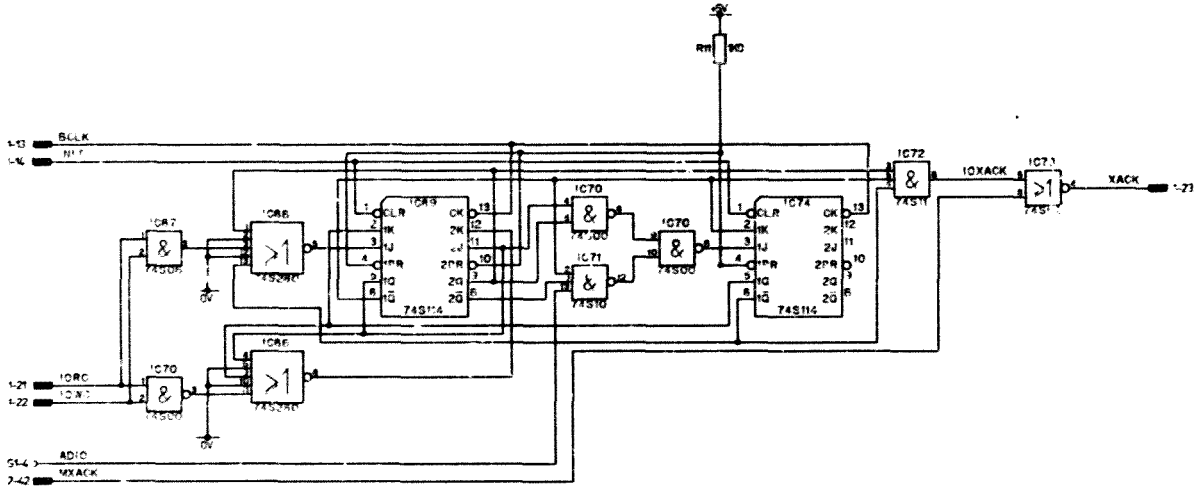
SHEET 5 *Timer Circuitry*



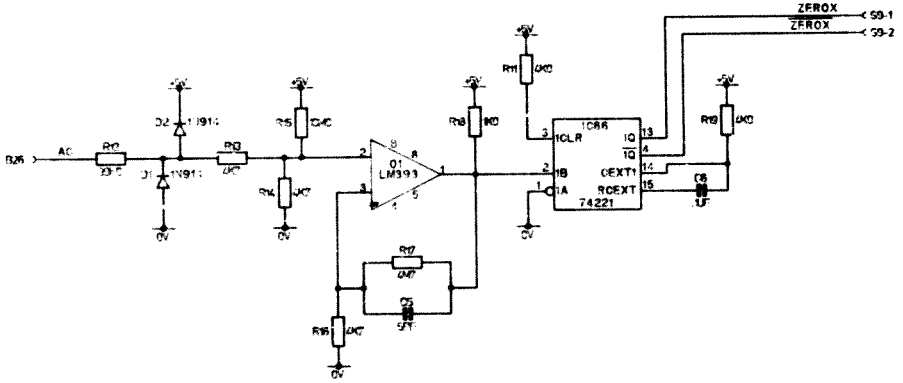
SHEET 6 *Data Capture Circuitry*



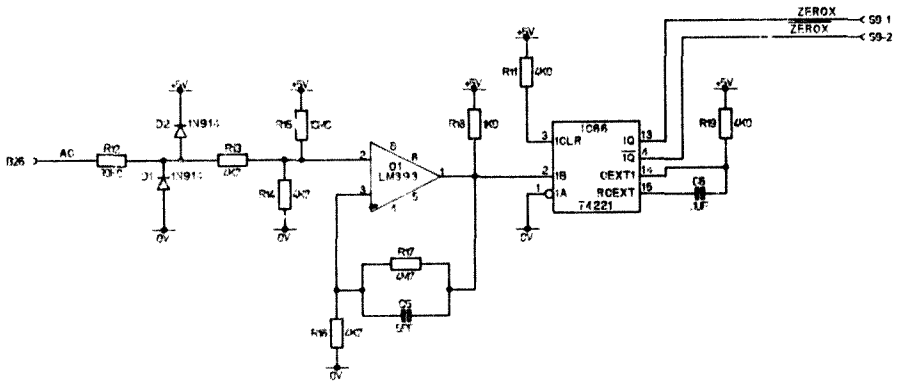
SHEET 7 *Triggering Circuitry*



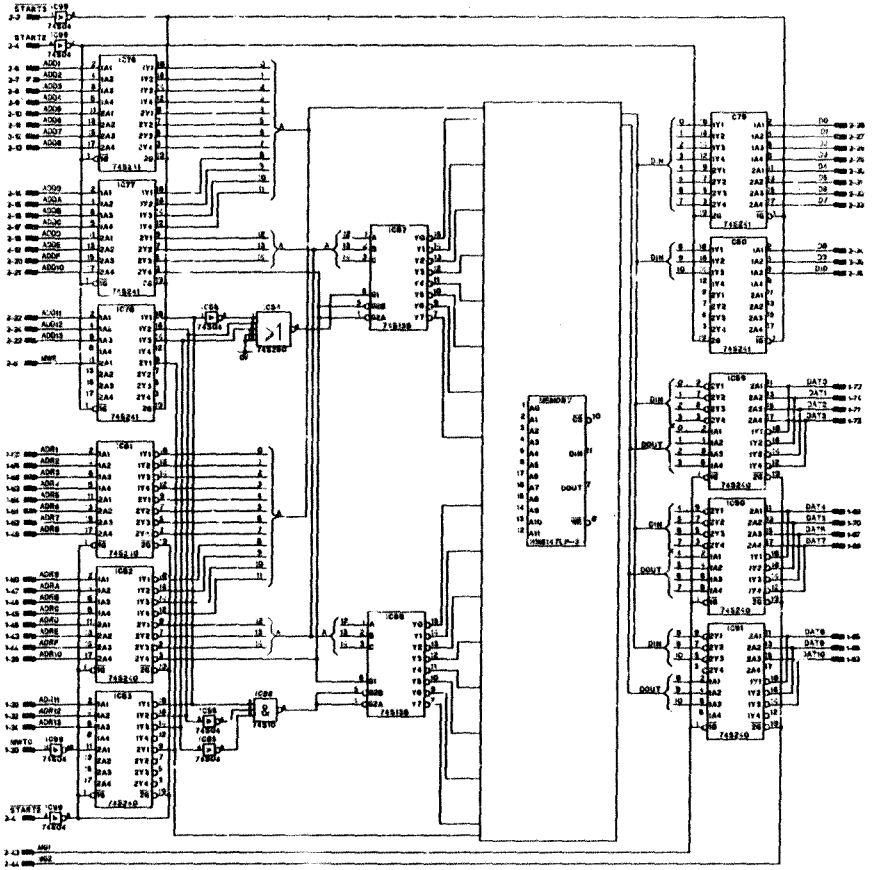
SHEET 8 *iSBC Handshake Circuitry*



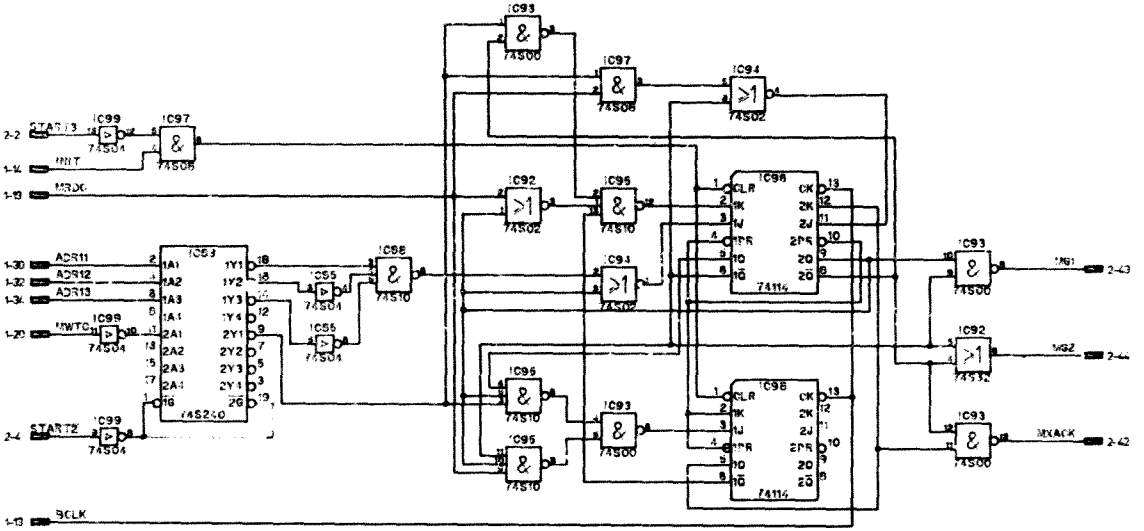
SHEET 9 *Zero Crossing Detector*



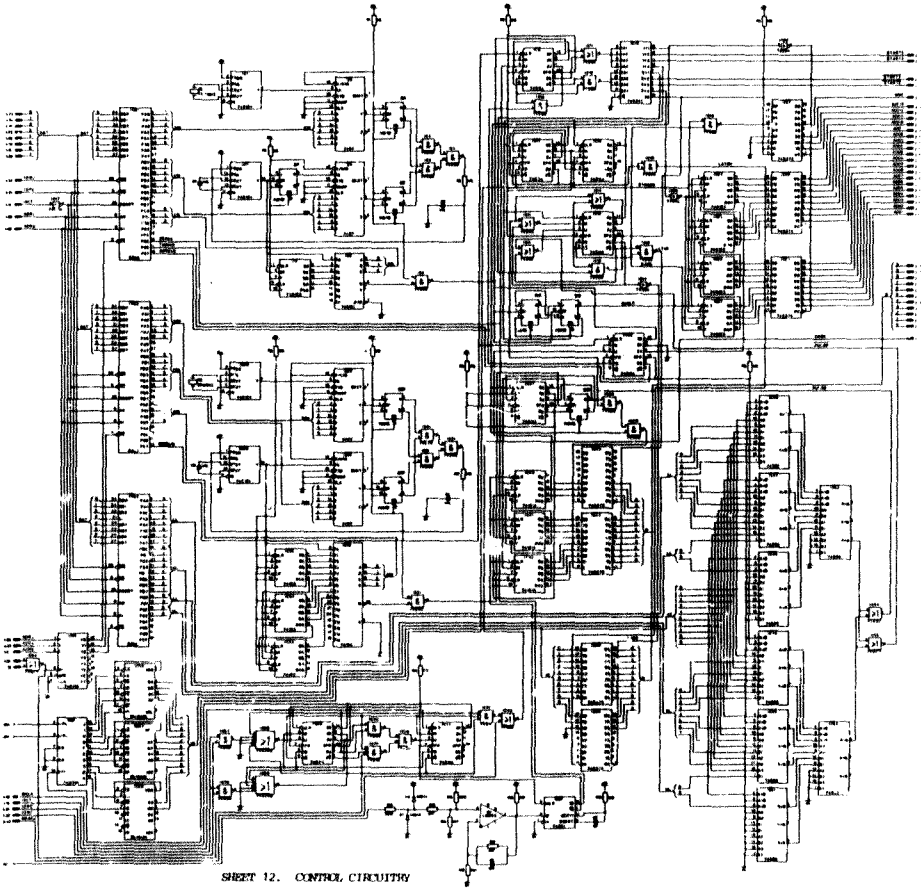
SHEET 9 *Zero Crossing Detector*



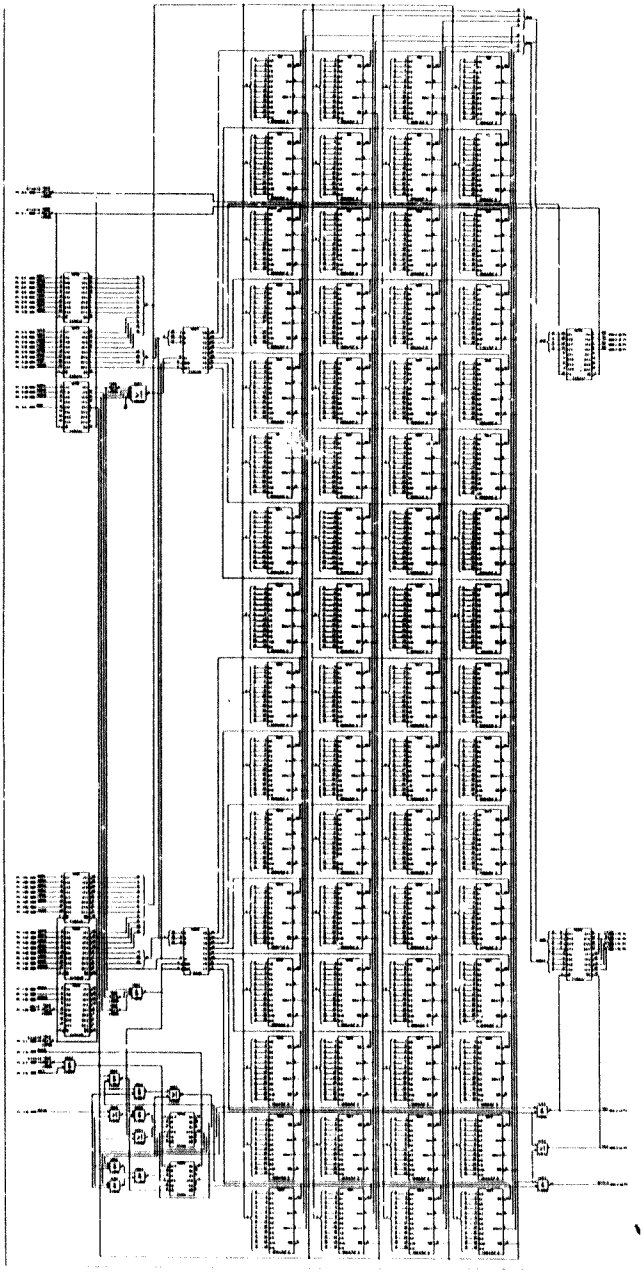
SHEET 10 *Memory Circuitry*



SHEET 11 *Memory Control Circuitry*



SHEET 12. CONTROL CIRCUITRY



SHEET 11. Entire Memory Circuitry

SHEET 14. CONTROL BOARD LAYOUT

SHEET 15. MEMORY BOARD 1 LAYOUT

SHEET 16. MEMORY BOARD 2 LAYOUT

SHEET 17. MEMORY BOARD 3 LAYOUT

APPENDIX 9 - SOFTWARE

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The software listings are contained in a separate document which may be found in the Engineering Library at the University of the Witwatersrand.