Assessment of DC-DC Converter Selection Metrics

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A dissertation submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, in fulfilment of the requirements for the degree of Master of Science in Engineering.

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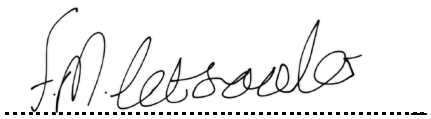
DECLARATION

I declare that this dissertation is my own unaided work. It is being submitted to the Degree of Master of Science at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination to any other University.



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To my wife Lebogang and son Hleloelihle,

To my family,

And to the creator of all, my Lord and Savior

ABSTRACT

The exponential growth of Internet of Things (IoT) devices, powered by diverse energy sources, poses significant challenges in power electronics. Despite advances in DC-DC converter topologies, a gap remains in the literature regarding standardized performance metrics for selecting suitable converters, making the selection process complex.

This study critically assesses metrics from seminal works of the 1960s to contemporary state-of-the-art, proposing a systematic approach to converter assessment. Two major categories of metrics are identified: averaging metrics and waveform-preserving metrics. Averaging metrics, grounded in Wolaver's foundational work, are effective for high-level comparisons among many converter options, establishing a performance baseline. The study introduces an average modeling tool to reveal core converter characteristics for objective comparison.

Waveform-preserving metrics, on the other hand, provide detailed performance insights and are suitable for a narrower set of converter options. The study further categorizes these metrics to assess converter switches and reactive components. A new RMS metric is proposed, refining the existing processed power metric for better accuracy.

By integrating both averaging and waveform-preserving metrics at relevant design stages, this study offers a systematic framework for converter assessment. This approach bridges the gap between high-level comparison and detailed performance evaluation, facilitating informed decision-making in converter selection.

PUBLICATIONS ARISING FROM STUDY

- F. Letsoalo and I. Hofsajer, “An Assessment of some Power Converter Topology Evaluation Metrics,” *Proc. 31st South. African Univ. Power Eng. Conf. SAUPEC 2023*, pp. 1–6, 2023, doi: 10.1109/SAUPEC57889.2023.10057746.
- I. Hofsajer, F. Letsoalo and A. de Beer, "An Investigation of Direct and Indirect Powers of DC-DC Conversion Systems," 2023 IEEE 2nd Industrial Electronics Society Annual On-Line Conference (ONCON), SC, USA, 2023, pp. 1-6, doi: 10.1109/ONCON60463.2023.10430487

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Chapter 1 Introduction

1.1 Research Background

The exponential growth of Internet of Things (IoT) devices has not only surpassed the global population but is projected to skyrocket further, with estimates reaching a staggering 75 billion devices by 2025[1]–[4]. With each device necessitating a reliable energy source, the complexity of powering these devices cannot be overstated. The varied nature of energy sources, ranging from batteries to grid connections, coupled with their diverse energy outputs, presents a formidable challenge. Moreover, the mismatch between the fluctuating nature of energy sources such as energy harvesters [5]–[7] and the steady power requirements of IoT devices emphasizes the critical role of power electronics in bridging this gap.

This brings us to power electronics, the cornerstone of energy conversion and processing for IoT devices. As the backbone of converting power from one form to another, power electronics enable the seamless operation of IoT devices by ensuring a consistent and suitable power supply. Amidst the plethora of power electronics converters, ranging from AC to DC and DC to AC, the spotlight in IoT applications falls predominantly on DC-DC converters, extensively documented in literature. To put this in perspective, the studies in [8]–[10] are focused on DC-DC converters topology synthesis. In [10] alone, a set of 400 feasible topologies are generated and reduced to 25 unique topologies.

Navigating through the vast number of DC-DC converter options presents a formidable task. The selection process is further compounded by the absence of a standardized approach and the lack of benchmarked performance metrics. While efficiency stands out as a commonly cited metric, a comprehensive evaluation encompassing various performance attributes is often overlooked. This lack of objective comparison mechanisms leaves IoT designers grappling with the intimidating task of topology selection. Often leading to selection of familiar topologies such as the traditional buck or boost. Whereas newer or less popular converter types such as the switched capacitor converter [11]–[15], hybrid converter [16]–[18] or resonant converter[18], [19] may be more suitable for the application

Recognizing this pressing need for a systematic and standardized approach, this study sets out to redefine the landscape of DC-DC converter selection. By correctly analyzing existing metrics and establishing a benchmark for converter performance, this research endeavors to provide a more objective and coherent methodology for topology selection. Through the development of high-level comparison metrics, simplification of converter structures, and the creation of a unified metric capturing detailed performance nuances, this study aims to demystify the complexities surrounding converter selection.

The underlying goal is clear: to empower IoT designers with the tools and insights necessary to navigate the intricate realm of DC-DC converter selection confidently. By addressing the existing uncertainties and complexities head-on, this research seeks to unlock the full potential of emerging converter technologies, paving the way for optimal energy solutions in the IoT landscape.

1.2 Related Work

At the forefront of related work in literature is Wolaver's seminal work [20]. Which lays the groundwork for understanding the fundamental limits of power processing. Through complex theoretical proofs, Wolaver describes the minimal effort required to process power, revealing the existence of an optimal performance boundary for power converters. In the same work, Wolaver introduces the distinction between "indirect power" and "direct power" within DC-DC converters, characterizing direct power as the energy transferred seamlessly from source to load without undergoing processing within the converter, while indirect power encompasses the energy routed through various converter components such as switches, inductors, capacitors, transformers, and rectifiers. Although initially underutilized, Wolaver's theoretical framework has gained renewed attention in recent years [20]–[22], and its adopted in this study as the fundamental performance limit.

Building upon Wolaver's foundational insights, Cobos and Cheng Li architectures [23]–[26] introduce the differential processed power metric and the VA Area modeling tool, which have since become staples in converter architecture analysis. By reframing Wolaver's concept of "indirect power" as "processed power," these authors provide a more tangible framework for evaluating converter performance. However, the absolute value definition inherent in the

processed power metric imposes limitations on its utility and interpretation, highlighting the need for further refinement.

In addition to processed power, the VA rating and switch utilization factor emerge as common metrics assessing switch stresses. Despite their critical relevance to converter performance, their intrinsic relationship to processed power and the fundamental performance limit remains underexplored, prompting a deeper investigation in this study.

Carsten [22] and Wittenbreder [27] contribute to the body of knowledge by introducing stress factors, which quantify the material requirements for converter implementation. While these metrics have seen some application and have been used with various modifications with some success by [8], [10]. However, the method itself has not been subjected to much scrutiny, particularly in the context of the systematic approach proposed herein.

Moving beyond stress factors, the fast-switching limit (FSL) and slow-switching limit (SSL) are metrics which offer valuable insights into the operational modes of active semiconductor devices and passive components within a converters [11], [15], [28]. Although primarily applicable to switched capacitor converters, their frequency and energy density dependence emphasizes their significance in evaluating converter performance.

Another notable metric, the energy factor, describes the ratio of AC energy stored in reactive components to DC energy in switch-mode power converters [29]. While Fryze theory used in [30] to propose a generalised energy factor similar to the power factor, its analysis is tangential to this study, given the conceptual overlap with Wolaver's work on fluctuating energy in converters.

When considering these diverse perspectives, it is evident that critical analysis and interpretation of existing metrics are paramount to developing a systematic approach to converter comparison. Hence, this study provides a comprehensive evaluation of Wolaver's fundamental limit, processed power, VA Rating, VA Area modeling, stress factors, and fast and slow switching limit metrics, with the aim of developing a rigorous framework for converter assessment and selection.

1.3 Research Scope

This work aims to reduce the complexity of selecting a suitable converter topology by providing a systematic approach. This work does not cover the design and optimization of topologies but high-level topological comparison to filter out unsuitable options from a vast number of options.

This is done by carrying out a critical assessment of high-level metrics in literature. Then development of a modelling tool for placing converters on equal footing. Finally, a proposal of a detailed performance metric, with the potential to unify several performance metrics. To assess the utility of the proposed average model and metric, four step-down converter topologies are analysed.

Since the topological level is considered, control techniques, materials, and technology to implement the circuit are not considered in the analysis.

1.3.1 Foundational Assumptions

In this study, the analysis is constrained to specific assumptions to streamline the complexity of topology selection. The following foundational assumptions guide the methodology

Zero loss

The analysis operates under the premise of zero loss, assuming ideal components with no power dissipation in switches or reactive elements. Consequently, input power equals output power, ensuring a balanced energy exchange over the complete switching cycle.

Zero Ripple

An assumption of zero ripple is employed, implying that inductors and capacitors are sufficiently large to eliminate current and voltage fluctuations. This simplification facilitates analysis by replacing inductors and capacitors with current and voltage sources, respectively, set at their average values. This assumption is typical when a topology's large signal transfer function is determined [31]. While concealing frequency-dependent performance nuances,

this assumption promotes fairer comparisons among topologies, as ripple is excluded as a parameter.

The assumption of zero-ripple is relaxed in Chapter 4 to assess the reactive components at different ripple scenarios.

Steady State

Implicitly, steady-state conditions are assumed in all analyses, overlooking initial transients in favour of balanced switching phases throughout a full cycle. This ensures consistent power distribution across phases and facilitates comparative assessments

Continuous Conduction Mode

Given the zero-ripple approximation, converters are evaluated under continuous conduction mode, optimizing component utilisation, and yielding favorable performance metrics for high-level comparison.

Bound to Circuit Domain

The above assumptions align with idealized component behaviour, consistent with fundamental circuit theory principles such as Kirchhoff's Voltage and Current Laws, and energy conservation. While confined to the circuit domain, the insights obtained from this study are extendable to experimental and optimization contexts.

1.4 Research Contributions

This study makes significant contributions towards streamlining the selection process of DC-DC converter topologies. The secondary sub-contributions made towards the main contribution include:

1) Critical analysis of state-of-the-art and fundamental performance metrics in literature;
2) Proposing an averaging modelling procedure which reveals the core topology structure of any converter;
3) Introducing a single potentially unifying metric for converter topology selection;

4) Developing a systematic approach to topology selection addresses the complexity inherent in the multitude of available options.

1.5 Dissertation Organisation

The dissertation is organized as outlined in Fig. 1.1 and described below:

Chapter 2, This chapter conducts a comprehensive examination of established metrics in the literature, commencing with an exploration of Wolaver's fundamental limit theory for DC-DC conversion performance. Each metric undergoes rigorous scrutiny and interpretation, with a particular focus on its application to a buck converter example. Furthermore, the chapter elucidates the inherent limitations of these existing metrics, providing valuable insights into their efficacy and scope.

Chapter 3 Here, a novel averaging modelling procedure is introduced, aiming to distill any converter to its core structure. By standardizing converters through this procedure, a level playing field for comparison is established. The chapter validates the averaged model against circuit theory principles, highlighting its potential as a powerful tool for high-level converter comparison and analysis.

Chapter 4 introduces an RMS metric which addresses limitations of the absolute value defined processed power metric.

Chapter 5 illustrates the utility of the metrics including the averaged topology model in assessing four converter topologies.

Chapter 6 then provides the final discussion on the metrics assessed and a potential systematic assessment approach is presented.

Lastly, the dissertation culminates with a concise summary of key findings and contributions followed by actionable recommendations for further research and application in Chapter 7.

1.6 Summary

This chapter lays the groundwork in addressing the critical issue of topology selection amidst a plethora of options, highlighting the necessity for a systematic approach. A

comprehensive overview of related literature spanning from seminal works in the 1960s to recent studies reveals the evolution of research in this domain. The chapter describes the methodology adopted in this study to mitigate uncertainty in converter comparison, including a thorough critique of existing metrics, the introduction of an averaging model to standardize converters for equitable comparison, and the proposal of an RMS-based metric for detailed evaluation. Furthermore, defining the research scope and outlining key assumptions such as zero-loss, zero-ripple, and operation in continuous current mode. Finally, the chapter outlines the research contributions, and provides a structured outline of the dissertation.

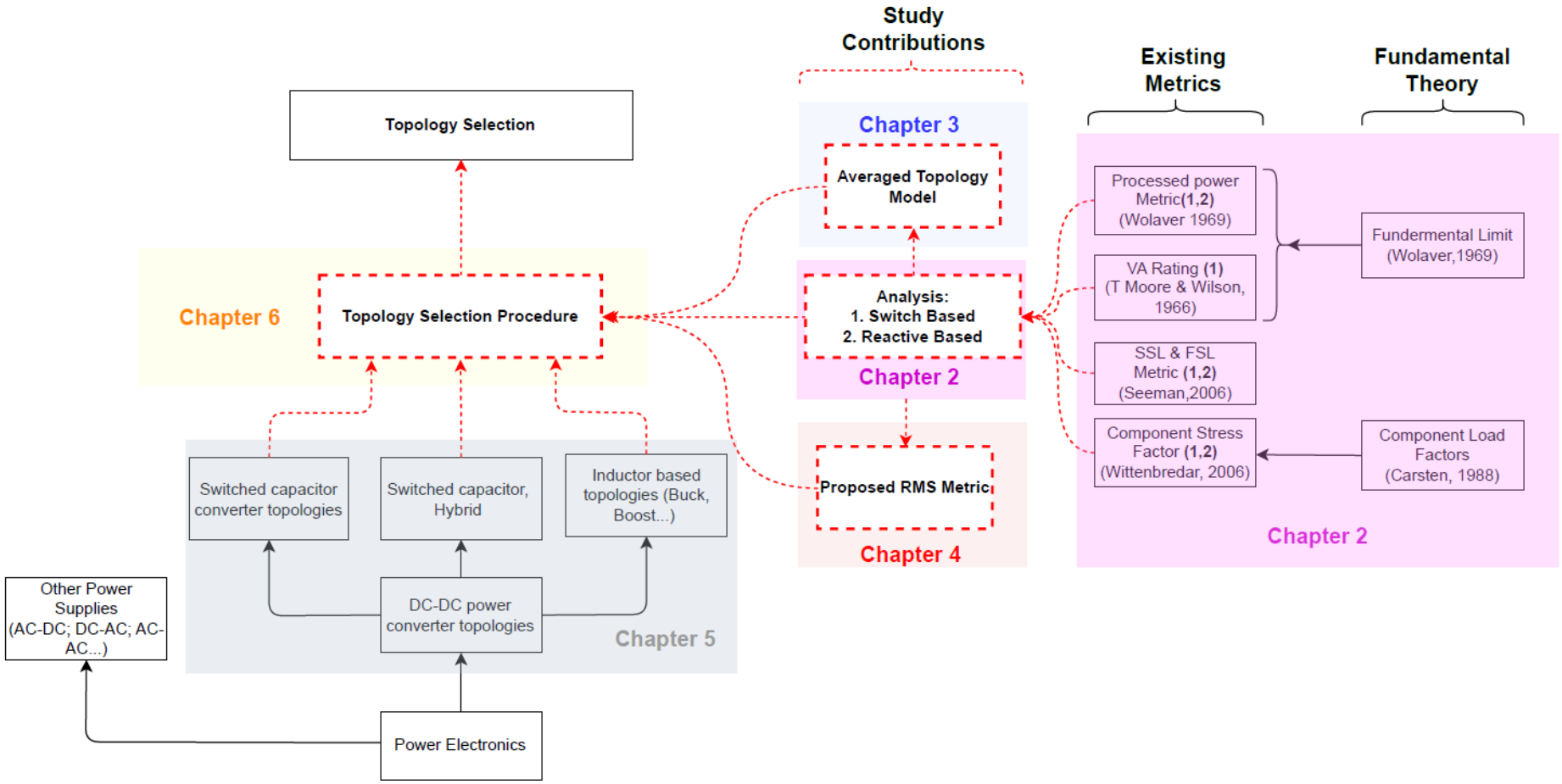


Fig. 1.1 Structure of Dissertation

Chapter 2 Assessment of Existing DC–DC Topology Metrics

2.1 Introduction

The problem of multiple existing metrics is demonstrated in this chapter, with four metrics looking at different performance aspects of the same buck converter example.

Four main metrics are assessed from literature in this section. Firstly, the Wolaver limit, which is an energy-based metric. Recent application of Wolaver's power transfer model and conceptualisation of the indirect power as processed power is discussed and its visualisation through VA Area modelling. Secondly, the switch-based metric, VA Rating related to the Wolaver limit is discussed. Thirdly a loss-based metric, the stress factors are presented. Then lastly, the output impedance-based metrics originally developed for switched capacitor converters, referred to as the fast and slow switching limit metrics are discussed.

2.2 Wolaver Fundamental DC-DC Performance Limit

D. Wolaver in the late 1960s defined a fundamental limit for DC-DC converter performance extended from the work of T. Moore and G Wilson [20], [32]. The fundamental limit is derived from the basics of DC-DC conversion with mathematical proofs and theorems from graph theory. This work has not found much utility until recently when it has been used with success by [15], [18], [23], [24], [33], [34] who have used it to analyse and derive new novel power conversion architectures and to visualize the power conversion process.

2.2.1 Direct and Indirect Power Paths

One of the key outcomes of the work is the conceptualization of power transfer in a switch-mode converter as two power transfer paths termed the direct and indirect power paths shown in Fig. 2.1

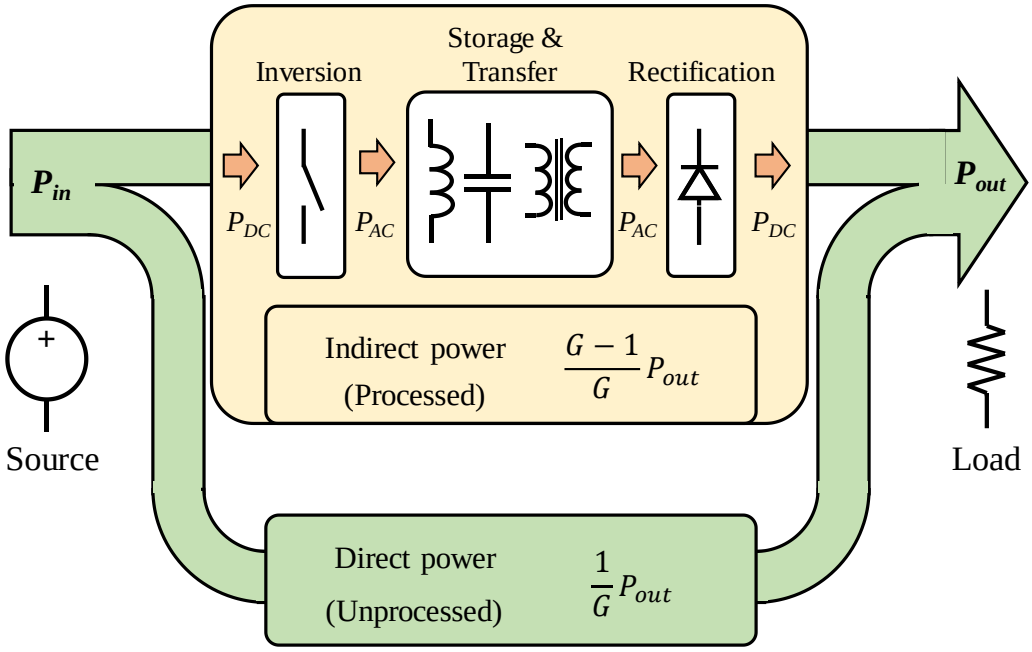


Fig. 2.1 DC-DC Power Transfer paths[35]

The direct power path transfers power directly from the input to the output, as shown in the bottom, green path. In a converter example, this occurs when there is a switching state where current flows directly from the input to the output, meaning there is a continuous current path between the two. The indirect path means power is transferred through, firstly inversion of the input power (P_{in}) to AC power by switches. The opposite and equal power can also be thought of as the power handled by the diode to rectify the AC power (P_{AC}) back to DC on the output. In between the switches and diodes, the "AC" power is stored by reactive components, inductors, and capacitors. This is the indirect power transfer and it is linked to converter performance.

Under steady state conditions the average power of all the reactive components is zero. This means that the total reactive power absorbed (or delivered) during the switches on state is delivered (or absorbed) back when the switch is open. The absolute value of power absorbed and delivered during a half cycle is referred to as the power processed by the reactive components. In a similar manner it can be shown that an AC power is produced by the switches in a converter which is rectified back to DC to be supplied to the load. The AC generated by the switches is equal to the DC power rectified by the diodes. Note that the power processed in the inversion and rectification complementary pair is not always equal to

that stored and transferred by the reactive components. The reactive components can process more power than the power inverted or rectified by the switches.

2.2.2 Wolaver Limit

According to Wolaver, there is a unique characteristic and fundamental constraint to the indirect transfer path of a converter topology in Fig. 2.1. This fundamental limit is given in equation (2.1) below.

$$Wolaver\ Limit: P_{indirect} \geq \frac{(G-1)}{G} P_{out} \tag{2.1}$$

where G is the voltage gain of a step-up converter or the current gain of a step-down converter.

The Wolaver limit can be interpreted as the minimum indirect power required by a converter to achieve power conversion from one form to another. For step-down and step-up conversion, the Wolaver limit is as shown in equations (2.2) and (2.3) respectively.

$$Wolaver\ Limit(step-down): P_{indirect} \geq \left(1 - \frac{V_{out}}{V_{in}}\right) P_{out} \tag{2.2}$$

$$Wolaver\ Limit(step-up): P_{indirect} \geq P_{in}\left(1 - \frac{V_{in}}{V_{out}}\right) \tag{2.3}$$

The limit equation for a buck converter is represented graphically in Fig. 2.2 against the converter gain. As the output voltage drops the conversion burden becomes larger and the amount of the total indirect power increases. For example, if the output voltage is close to the input voltage of the buck converter (Gain close to unity) then the conversion effort is small and the corresponding indirect power is also small. Conversely the direct power increases for conversion gain$\left(\frac{V_{out}}{V_{in}}\right)$ towards unity for the step-down case.

Not all topologies will lie along the dashed line in Fig. 2.2. That line shows the best possible case. Often the buck converter topology will have indirect powers that are much bigger than the minimum. From this a “good” topology is one which has the least indirect power, or close to the Wolaver limit. Thus, a topology that processes a lot more than the limit can be regarded as a “bad” topology.

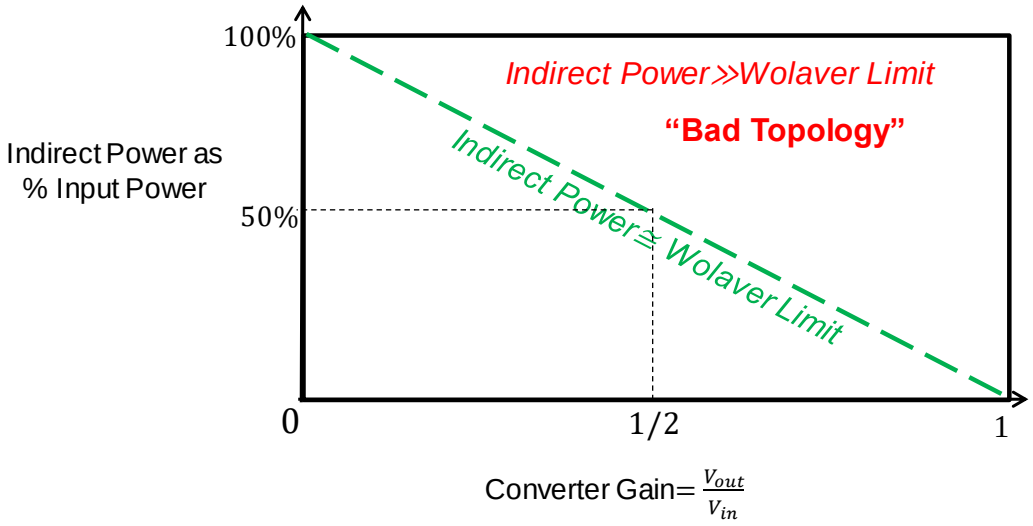


Fig. 2.2 Wolaver Limit graphical representation for a buck converter

This limit puts a constraint on the switches and reactive components in the indirect power path. According to Wolaver, both the switches and the reactive components have the same limit though derived under different conditions. The switch constraints are derived under average conditions and the reactive component limit is derived from time-varying voltage and current waveforms.

These characteristic constraints are used in later sections as a fundamental performance metric to compare topologies.

2.2.3 Switch Constraint

Wolaver in [20] provided proof for the requirements of switches and diodes for DC-DC conversion to occur, which leads to the switch constraint. The constraint on their handled indirect power is shown by the inequality in equation (2.4)

$$\sum_{switches} \mathrm{P_{DC}} \geq -\sum_{switches} \mathrm{P_{AC}} \geq -\sum_{diodes} \mathrm{P_{AC}} - \sum_{diodes} \mathrm{P_{DC}} \geq \frac{G-1}{G} P_{out} \qquad (2.4)$$

Fig 2.3 below is the original power transfer illustration from [20]. The Illustration shows the indirect path has the switch and diode which Wolaver referred to and are represented as the AC active resistors (R_{AC}) and dc active resistors (R_{DC}) respectively.

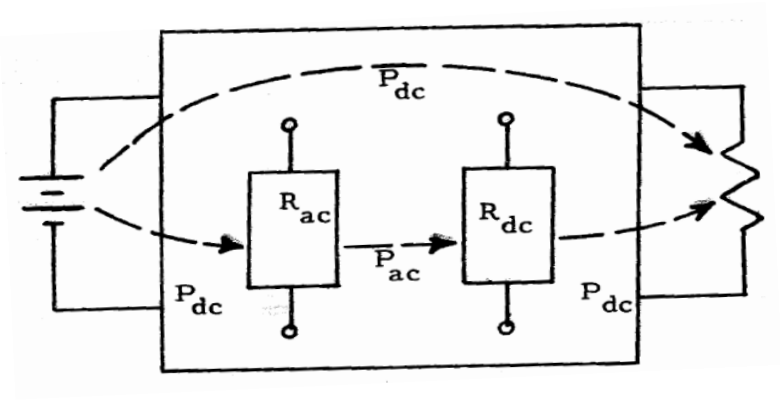


Fig. 2.3 Indirect power transfer mechanism for switches and diodes [20]

According to equation (2.4) and Fig 2.3, there is a minimum amount of power that the switches and diodes need to process for the G, $\left(\frac{V_{in}}{V_{out}}\ or \frac{i_{out}}{i_{in}}\right)$, to be greater than 1. The DC power (P_{DC}) absorbed by the switches is greater or equal to the AC power delivered back to the circuit by them $(-P_{AC})$. The inequality captures power handled in the inversion from DC to AC by the switches. The second last and third terms show that the diodes rectify the AC power back to DC power. The power delivered by the diodes is more or equal to the DC power supplied to the load. The power handled, absorbed, or delivered by the switch or diode is constrained by the Wolaver limit given in equation (2.1).

For both the switch and diode the power handled refers to the product of the average voltage and current, not resistive power loss or heat dissipation. The next section looks at the reactive component constraint which is the same as the switch constraint.

2.2.4 Reactive Component Constraint

We have considered the constraints on switches for DC-DC power conversion, now we consider the constraint on the reactive components. For the switch constraints in Section 2.2.3, the average of the voltage and current was considered to obtain the power processed by the switches. Taking the average model of the whole circuit results in the total power absorbed and released by reactive components being zero.

To analyse the constraints on the reactive components, their time-varying voltage and current waveforms are considered. According to the author(s) in [20], [23] the reactive

component power is defined as half of the average absolute value of the product of the voltage and current over the full period, see equation (2.5)

$$P_{component} = \frac{1}{2}\frac{1}{T}\int_0^T |\mathrm{v}(t)\cdot \mathrm{i}(t)|\cdot d(t) \tag{2.5}$$

The definition of the component power in equation (2.5) is somewhat intuitive, considering that the reactive component power represents the power absorbed and released by capacitors or inductors. These powers are expected to be equal but have opposite polarity, for a converter in steady state. Thus, the sum of the powers over a full cycle is zero. Thus, in [20] the absolute value of the power over the full cycle is taken. This results in twice the power, absorbed + released, of which only half of this is interpreted as the power handled by the component.

According to equation (2.6) from [20] the sum of the reactive components' power is also constrained by the same limit as the switches in equation (2.4).

$$\frac{1}{2}\sum_{\substack{reactive\\components}} \overline{|v\cdot \imath|} \geq \frac{G-1}{G}P_{Out}$$

or (2.6)

$$\frac{1}{2}\sum_{\substack{reactive\\components}} \left(\frac{1}{T}\int_0^T |v(t)\cdot \mathrm{i}(t)|\cdot d(t)\right) \geq \frac{G-1}{G}P_{Out}$$

2.2.5 Buck Example

An example of a 12V to 3.3V Buck converter is considered to numerically demonstrate the direct and indirect power paths; Wolaver limit; and the switch and reactive constraints. The converter circuit is shown in Fig. 2.4, the input and output power are taken as 15W.

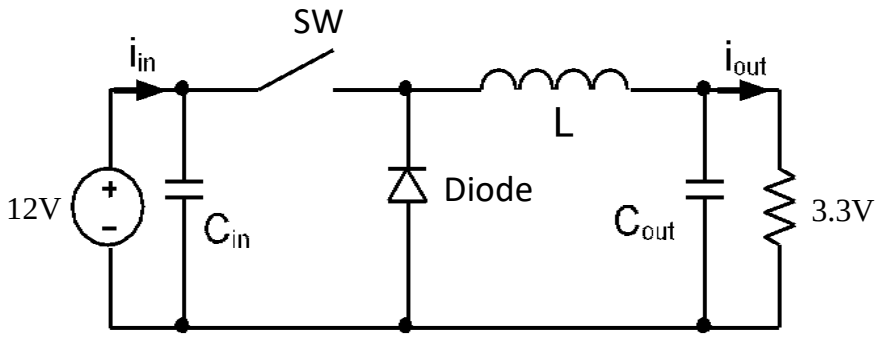


Fig. 2.4 12V to 3.3V buck converter circuit example

To determine the switch's indirect power, the average voltage and currents of the converter are considered from basic circuit analysis. In this specific case of the buck converter, its duty cycle (D) is equal to the conversion ratio, i.e. $\frac{V_{out}}{V_{in}}$, in this case, $D = 1/G$. The results with the powers as defined by the product of the average voltage and average current. are listed in Table 2.1. The detailed analysis of the buck converter is thoroughly done in Chapter 3.3. Note that the power referred to here is not the normal average power which would be zero for an ideal switch and diode. It is taken as the product of the average current and voltage of each component.

Table 2.1 Average model results

	Average Voltage[V]	**Average Current[A]**	**Average Power[W]**	$\frac{Average\ Power}{Input\ Power}$ **[%]**
V_{in}	12	-1.25	15	100
C_{in}	12	0	0	0
SW	8.7	1.25	10.88	73
L	0	4.55	0	0
$Diode$	3.3	-3.295	-10.88	73
C_{out}	3.3	0	0	0
V_{out}	3.3	4.55	15	100

To determine the reactive indirect power as defined in equation 2.5 the voltage and current waveforms of the converter are considered, with the results listed in Table 2.2. These results can be replicated using *Spice* simulation with the parameters in Table 2.3.

Table 2.2 Reactive components powers for 12V to 3.3V buck converter

Reactive Component	Power [W]
P_{Cin}	10.88
P_L	10.88
P_{Cout}	~0
P_{out}	15
$\frac{G-1}{G}P_{out}$	10.88

Table 2.3 Buck example component values

Component	Values
C_{in}	4.7uF
L	1.8uH
i_{ripple}	0.3
f_{SW}	1MHz
C_{out}	2.2uF
$V_{out(ripple)}$	2%

From the results, the buck converter for all conversion gains V_{out}/V_{in} meets the Wolaver limit since:

The power of the switch and diode meets the Wolaver limit

- $P_{switch}\ and\ -P_{diode}$ (Table 2.1) $= \frac{(G-1)}{G}P_{out}(\ Equation(2.1))$

The reactive components meet the Wolaver limit

- $\frac{1}{2}(P_L + P_{Cin}) = \frac{(G-1)}{G}P_{out}(\ Equation\ (2.6))$

It is further noted that the buck converter is at the Wolaver limit at all gains. The plot of the buck converter switch and reactive components' indirect power normalized by the input power is shown in Fig. 2.5. From the plot the indirect powers are at the Wolaver limit for all gains. The capacitor's indirect power is shaded in yellow and the inductor in green.

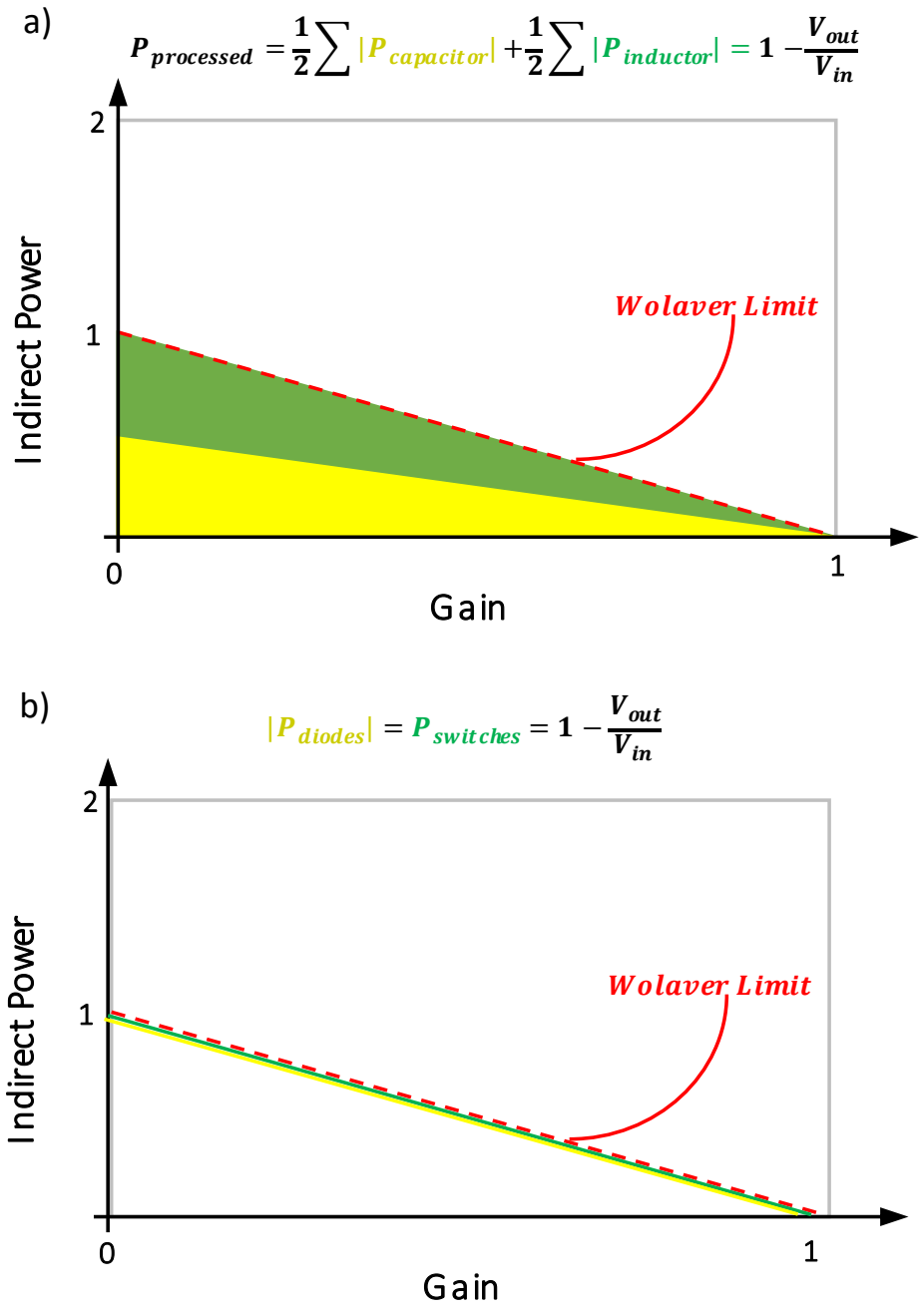


Fig. 2.5 Buck Converter Indirect Power, a) reactive components and b) switches

2.3 Processed Power Metric and VA Area Modelling Tool

The differential processed power metric, alongside the VA Area modelling tool originally introduced by authors Cobos and Li is widely applied to converter architectures [23]–[26]. The authors can be easily credited for popularizing the early work of Wolaver[20], [21] by conceptualizing “indirect power” as “processed power”. The differential processed power is the indirect power transfer path by Wolaver as shown in equation (2.7) below. The terms “partial,” and “differential” are used interchangeably in literature.

$$P_{diff} = P_{indirect} = \frac{1}{2}\frac{1}{T}\int_0^T |\mathrm{v}(t) \cdot \mathrm{i}(t)| \cdot d(t) \tag{2.7}$$

The VA Area modelling visualizes these power transfer paths within a topology. One major attribute of the VA Area model is the use of a topology’s terminal effects (input and output voltage and current) to reveal its internal workings. This makes it easy to use for the analysis and design of power architecture topologies. An example of where this is useful and finds most utility is in renewable power architecture analysis and design, such as solar [26], [36], [37].

Since the focus of this study is topological comparison, the modelling tool is applied to a buck converter example, in contrast to a no-direct power transfer, buck-boost converter, revealing its utility to topology level comparison. The advantages and shortcomings of the differential processed power metric and VA Area modelling tool for topology comparison are also outlined in this section.

2.3.1 VA Area Modelling

VA area modelling is a graphical tool for visualising the differential power from the direct and indirect powers of the input and output powers of the converter. In the first step, the voltage and current are drawn in the y and x-axis respectively to form input and output VA areas as illustrated in Fig. 2.6. In the second step, the two areas are overlaid as shown in Fig. 2.7.

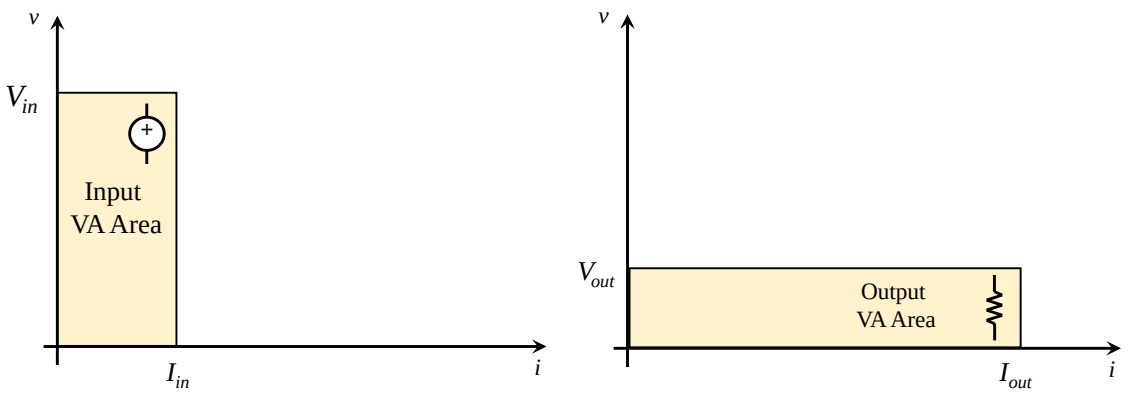


Fig. 2.6 Input and Output VA Area modelling

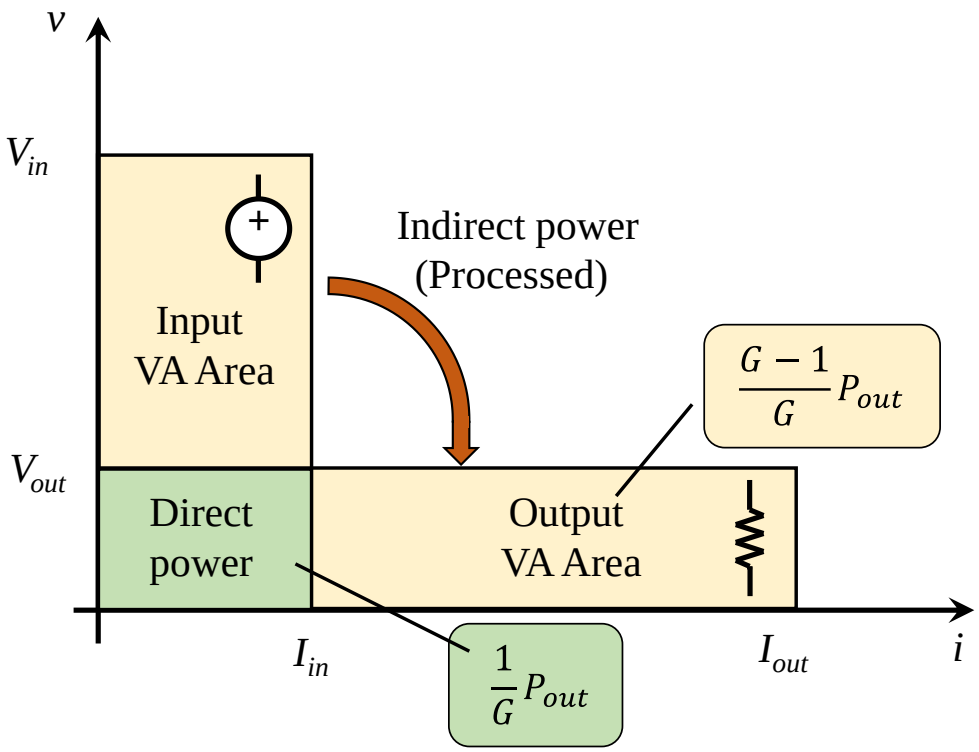


Fig. 2.7 VA Area showing indirect, direct and indirect power transfer [35]

The overlapping regions are defined as direct power and the non-overlapping regions, are indirect power or can also be referred to as processed power. The critical part of the modelling is the relative positioning and overlap or no overlap between the areas. The relative positioning depends on the electrical connection between the input and output. If current flows directly from the input to the output, then their widths are drawn from the same point. If no current flows directly from the input to the output, then their areas are drawn separately and thus no overlap.

The overlapping region of the areas is interpreted as the direct power transfer from the source to the load as illustrated in Fig. 2.7. This region represents DC power transferred directly to the output without being processed in the converter.

The non-overlapping regions are taken as indirect power, which is the second power transfer path. This region can be thought of as the power processed by the converter resulting in the output voltage. This represents AC power generated by switches from the DC input, absorbed or delivered by reactive components and rectified by diodes back to DC in the output as illustrated in Fig. 2.1. From an energy perspective the overlap region represents energy converted in the topology from one form to another, in this case from one potential level or current magnitude to another.

Typically for a lossless case, the input and output VA areas are equal, thus the input power is transferred to the output without losses. In the case of resistive loss, the input and output VA areas will not be equal.

2.3.2 VA Area Modelling Loss Case

As an example, consider a simple potential divider topology shown in Fig. 2.8 a), this represents a lossy scenario with a direct connection between the input and output. The voltage in the output, across Ro, is converted from 12V to 3.3V. To obtain this voltage conversion, power is lost through R1.

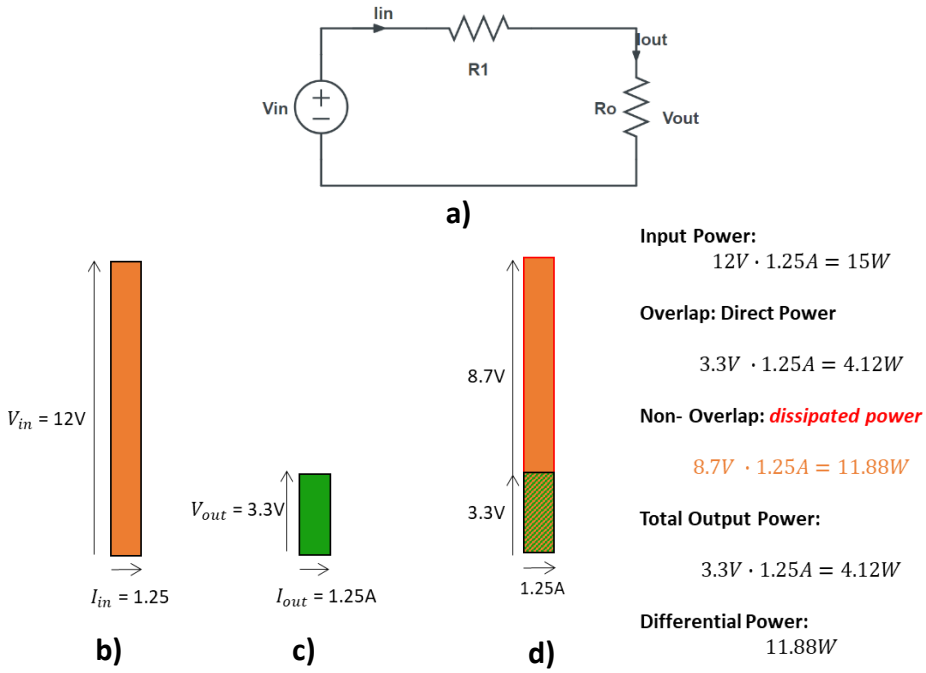


Fig. 2.8 a) Potential divider, b) Input, c) *Output, and d) Resultant VA Area model*

Drawing the VA Area for this example is as follows. The VA area model of the input is drawn as the height of the input voltage(12V) and the width is the input current shown by the orange area in Fig. 2.8 b). Similarly, the output VA area is drawn with the height and width of the output voltage and current respectively in Fig. 2.8 c). Since the source and load share the same current (thus direct electrical connection), their VA areas overlap. The two areas are overlaid in Fig. 2.8 d) resulting in an overlapping and non-overlapping region.

The overlapping area in this example represents power transferred directly to the output from the input. The non-overlapping VA area $(V_{in} - V_o) \cdot I$ represents the power dissipated by R1. Take note that this power is not indirect power, since it is not transferred to the output, as we will see in other non-dissipative power transfer examples with switches and reactive components.

2.3.3 VA Area Modelling Isolated Case

Now let us consider an ideal transformer as an isolated case with the same input and output voltage, shown in Fig. 2.9 a). In this case, all the power is indirectly transferred, since there is no direct current flow from the input and output, thus the VA areas are drawn as shown in Fig. 2.9 b) without an overlap. The VA areas are equal, one represents the power

delivered and the other the power absorbed. The delivered and absorbed powers have opposite directions considering the current flow.

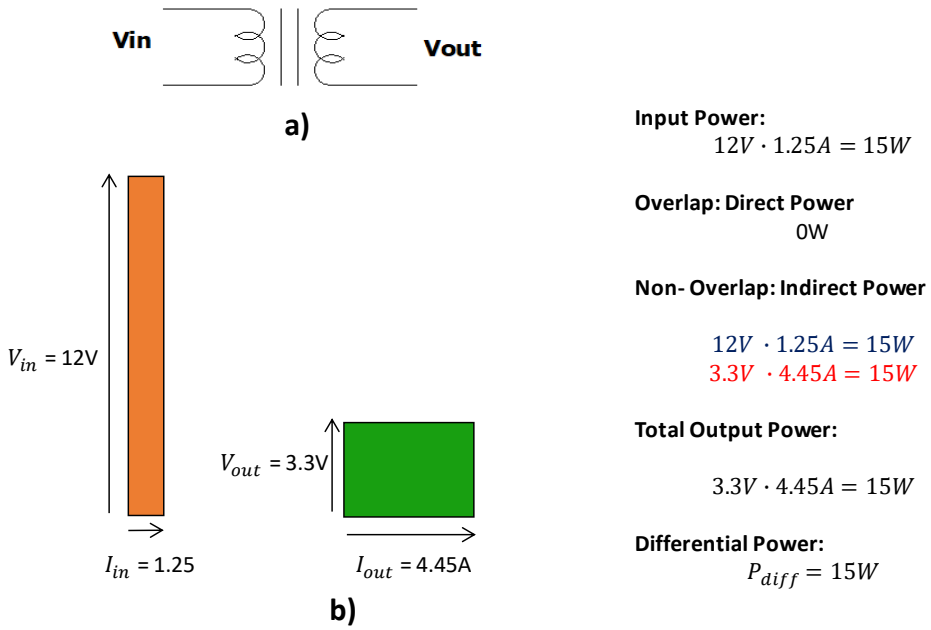


Fig. 2.9 Isolated example, a) Transformer circuit, b) non-overlap VA Areas,

2.3.4 Buck vs Buck-Boost Example

The utility of the VA Area modelling tool is made apparent when contrasting different topologies, in this section a buck converter and a buck-boost converter are compared. The buck converter is a Wolaver limit topology as detailed in Section 2.2 and the buck-boost converter is selected as an example of a common worst-case topology in terms of no-direct power transfer.

Consider the buck converter in Fig. 2.10, when the switch is conducting, the diode is reverse biased, and direct current flows directly from the constant voltage source (V_{in}) to the load illustrated in Fig. 2.10 b). The inductor in this cycle is also charged with fluctuating current from the equivalent voltage source capacitance (C_{in}). Thus, in this state power is transferred directly (P_{dir}) from the input to the output and the rest of the power, P_{AC}, is stored in the inductor.

In Fig. 2.10 c), when the switch is open, the diode has positive forward bias voltage and thus conducts. Then current flows from the charged inductor(discharges) to the load, rectified

by the diode. The input capacitor is charged in this phase. Note that the output capacitor (C_{out}) also charges and discharges but minimally so in the buck converter topology. Thus, power stored P_{AC} is released to the load as P_{DC}, resulting in the output power.

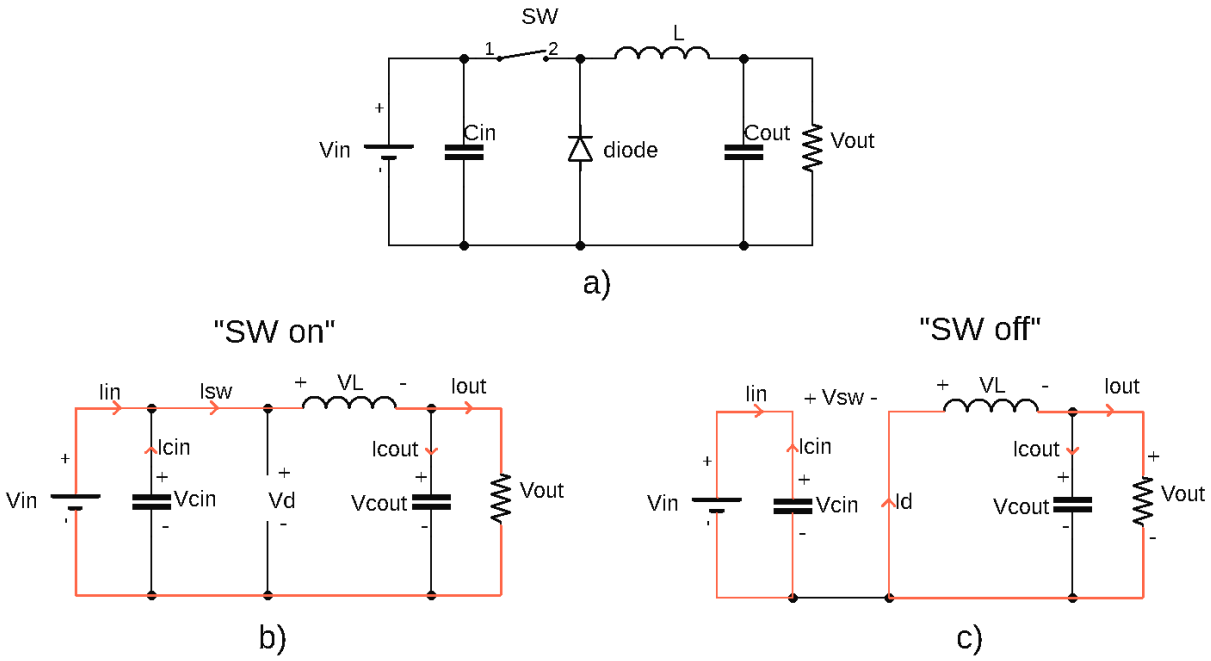


Fig. 2.10 a) Buck circuit, b) closed switch, and c) open switch equivalent circuits

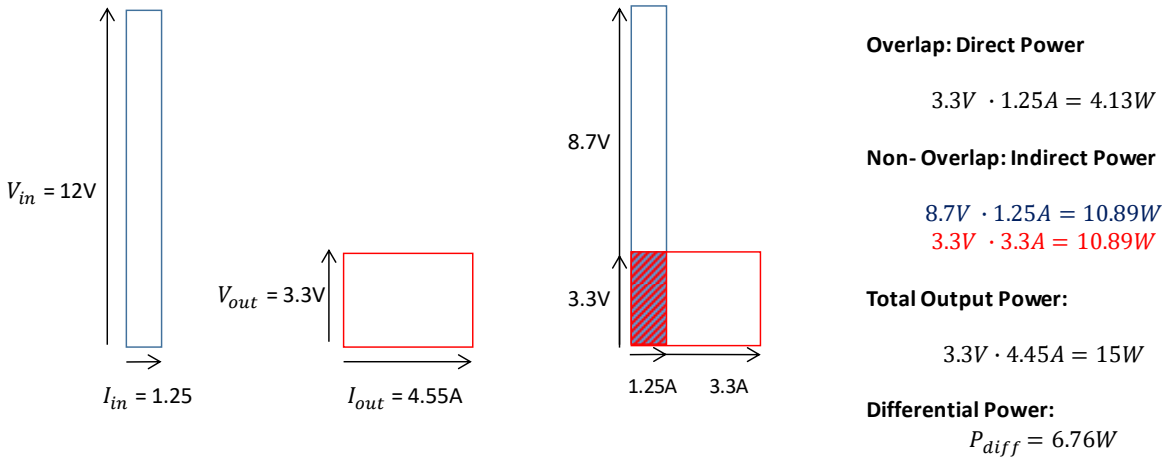


Fig. 2.11 Buck Converter VA Area Model, 73% indirect power

The VA Area model of the buck converter is shown in Fig. 2.11. The input VA area is shown as the area, with the blue outline, and it is equal to the output VA area with a red outline. The areas overlap representing 4.13 W direct power flow when the switch is closed. According to the model the rest of the power, ~73% of the input power is indirectly transferred. The differential power for this buck example is 6.76W which is about 45% of the input power. The direct and processed power add up to the output power as expected.

2.3.5 VA Area Modelling of Fully Indirect Power topology: Buck-Boost

Consider a fully indirect power transfer topology, the buck-boost converter shown in Fig. 2.12 b) and c), showing two separate current loops formed when the switch is conducting and not conducting respectively. There is no direct current path from the input to load similar to the transformer example in Section 2.2.3. According to the VA Area modelling procedure in Section 2.3.1, the VA areas are drawn separately with no overlap as shown in Fig. 2.13. The buck-boost has 100% indirect transfer of the input power to the output, and has zero direct power.

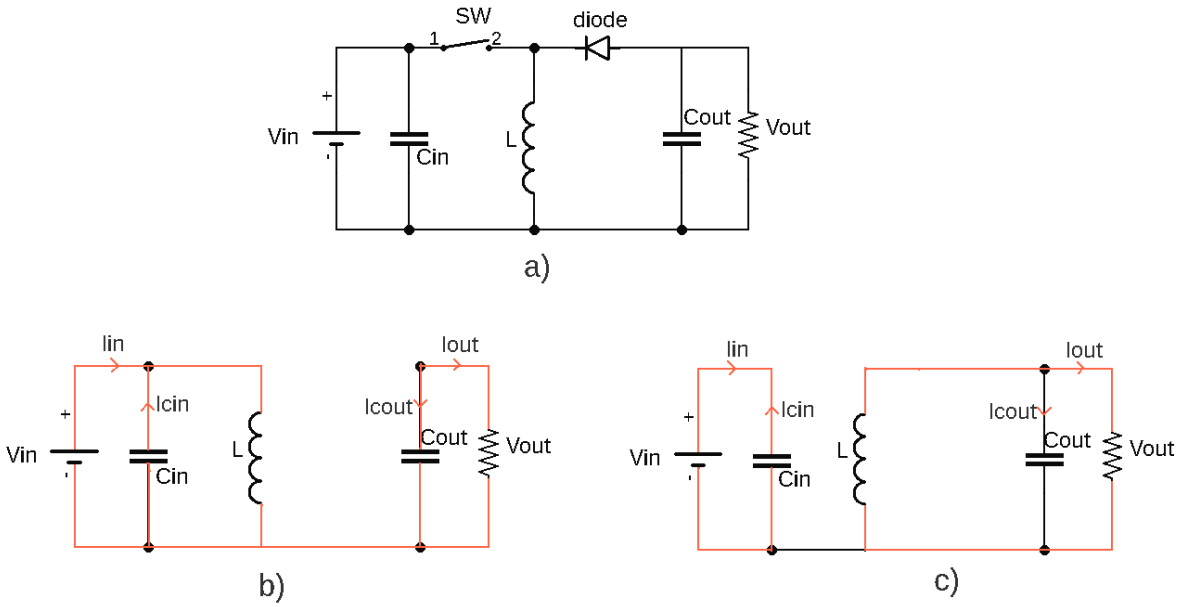


Fig. 2.12 a) Buck-Boost circuit, b) closed switch, and c) open switch equivalent circuit

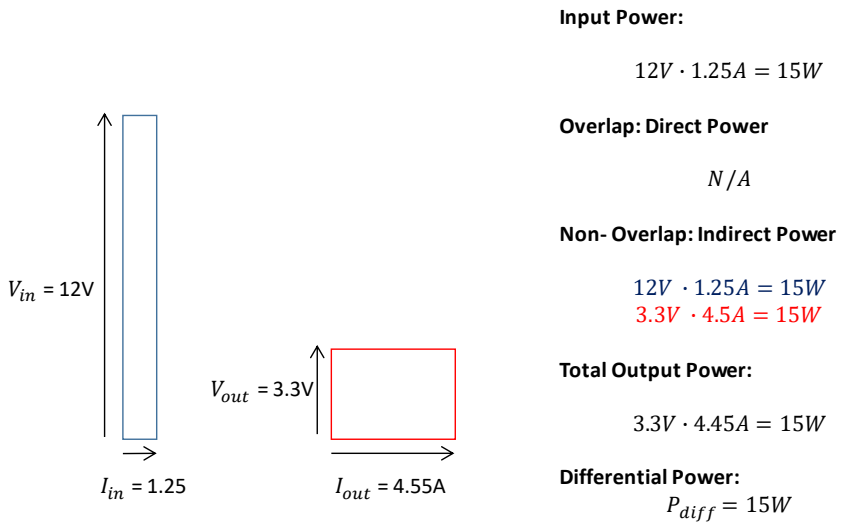


Fig. 2.13 Buck-Boost VA Area, no overlapping areas (no direct power)

In the comparison of the buck and buck-boost. The obvious advantage of the buck-boost is its ability to do both step-down and up applications. The buck will be the most suitable for fixed step-down gains when comparing their differential power. This is because the buck will always have some direct power transfer compared to the buck-boost, which has zero at all gains. This translates to higher cost and volume for the buck-boost vs a buck, which are the most common constraints. The VA Area modelling paints the buck-boost badly as we would expect, which gives confidence to the approach.

2.3.6 Limitations of Differential Power and VA Area Modelling

The differential power, which is the indirect power, provides the minimum required amount of power to be processed by a topology consistent with results obtained through Wolaver's analysis for different topologies. This approach provides insight into the internal power transfer mechanism of a topology from its terminal properties. This makes it easy to compare topologies based on their input and output voltage and current, as seen in the comparison of the buck and the buck-boost in Section 2.3.4 and 2.3.5.

However, there are limitations to considering the terminal properties of converters for comparison. This approach will not be able to distinguish topological differences; since multiple topologies can have the same terminal results. In [38] the need for a topological metric considering the components within the converter was highlighted. The VA Area modelling is limited in interpretation and utility to converters with single switches and diodes.

Having more than two switching states results in a complex analysis using the VA Modelling, where it is difficult to trace the power exchange between them.

When looking at the internal workings of a topology, being able to go down to the component level is critical to compare topologies, they can have the same salient features (Thevenin and Norton Equivalent) but completely different internal workings. The component-level power transfer perspective would provide deep insight into the topological differences.

2.4 VA Rating

The VA Rating is a common metric for the assessment of switches. This section shows the relation of the Wolaver fundamental limit for evaluating converter topology switches.

2.4.1 Definition of VA Rating

An ideal switch blocks the maximum voltage when open, and zero current flows through in this state. The switch conducts current when closed and has zero voltage drop across it. These two extreme points are the intersections of the vertical and horizontal axis as shown in Fig. 2.14. The average voltage and current of the switch are given by V_{ave} and I_{ave} shown on the plot. Typically, the switch voltage and current characteristics depend on the converter topology.

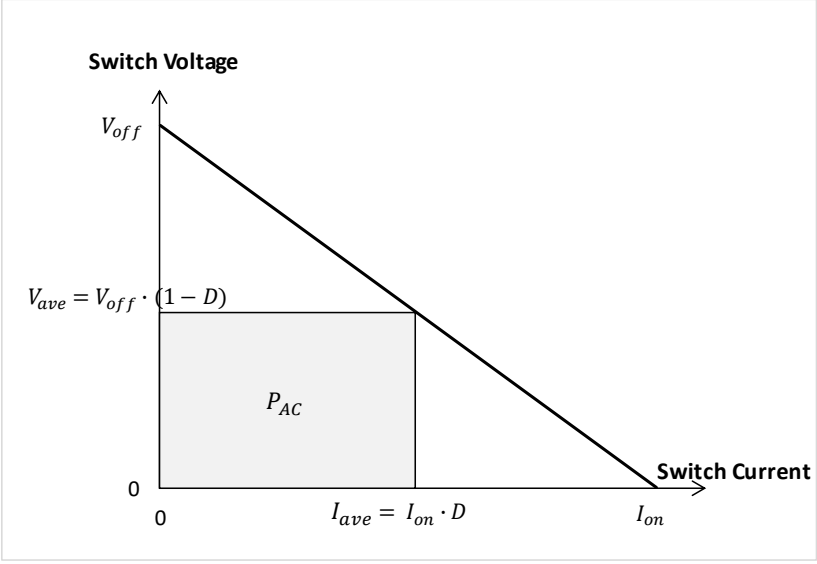


Fig. 2.14 Switch Operating Area

Some converters require higher-rated switches, which results in the selection of a bigger switch footprint/package with a higher cost. The focus of this section is not on switch selection, but understanding their selection aids in understanding the importance of a VA Rating metric that compares topologies based on their switches.

The switch volt-ampere (VA) rating and utilization factor are common concepts but their equations are given below to build up to the VA Rating metric for topology comparison. The VA rating of a switch is defined as the product of its maximum blocking voltage and maximum conduction current as shown in equation (2.8) [39].

$$VA = V_{SW(off)} \cdot I_{SW(on)} = V_{SW(peak)} \cdot I_{SW(peak)} \tag{2.8}$$

The utilisation factor U_f of a switch is defined as the topology output power ($P_{out} = V_{out} \cdot \mathrm{I_{out}}$) divided by the VA rating of the switch.

$$U_f = \frac{P_{out}}{VA} \tag{2.9}$$

The utilisation factor determines how well the switch capabilities are used in the converter[18], [22], [28], [40]. A factor of 1 means the switch is being fully utilized, and efficiently used. A low utilization factor means the switch has a higher VA rating compared to the output power, thus poorly utilised. The switch VA rating tends to be high for high gains, resulting in a low utilization factor. Low factors are common in non-isolated converters with high voltage gains, step-up, or step-down. The gain in a switch mode converter is controlled by the duty cycle. Thus, the VA Rating of a converter has a direct dependence on the converter duty cycle. Utilisation factor is a good engineering metric but its fundamental basis is limited.

We now consider the VA Rating metric as a converter metric by extending on the foundational work of Wolaver, whose work is not only applicable to converter topologies but any circuit which meets energy conservation.

According to Wolaver and Moore et al, to achieve conversion, switches need to generate(process) a certain minimum AC power for conversion to occur [20], [32]. Moore and Wilson in their paper in 1969 stated without proof, that the VA rating of a switch needs to be at least 4x the AC power generated [32].

Now using the foundation of Wolaver's theorems the relationship between the VA Rating and processed power processed by switches can be easily proven. The processed power of a

switch is taken from Wolaver's work discussed in the previous section, refer to Section 2.2.3. By taking an average model of a converter topology the average voltages and currents of the converter were shown to meet KVL and KCL. From this model, the processed power (P_{AC}) by the switches is defined as the product of the average voltage and average current, as shown in Fig. 2.14 and equation (2.10) below for a buck converter.

$$P_{AC(SW)} = V_{off}(1-D)\cdot I_{on}\cdot D = V_{off}\cdot I_{on}\cdot D\cdot(1-D)$$
$$P_{AC(SW)} = (VA)\cdot D\cdot(1-D) \tag{2.10}$$

From equation (2.10) the relationship between the VA Rating and the processed power of the switch is a function of the duty cycle D. The peak of the relationship is at half the duty cycle, $D = 0.5$. At a duty cycle of a half, the processed power of the switch is a quarter of the VA Rating, shown equation in (2.11).

$$P_{AC(SW)} = \frac{1}{4}\times(VA) \qquad @\ D = 0.5 \tag{2.11}$$

Put differently, the converter switch will have a VA Rating of at least four times the required generated Processed power, see equation (2.12).

$$VA\ Rating = 4\times(P_{AC(SW)}) \tag{2.12}$$

Fig. 2.15 shows the VA Rating of the switch divided by its processed power ($P_{AC(SW)}$). The best utilisation of the switch in a buck converter occurs at a gain of 0.5, this is where the converter has the lowest VA Rating to processed power ratio. At 50% gain, a switch with a VA Rating 4 times its power processed is required. The switch VA Rating required to implement the same buck operating at a conversion ratio higher or lower than 50% will be more than 4 times limit. At a conversion ratio of 0.275, the required switch VA rating is 5 times the power processed by the switch.

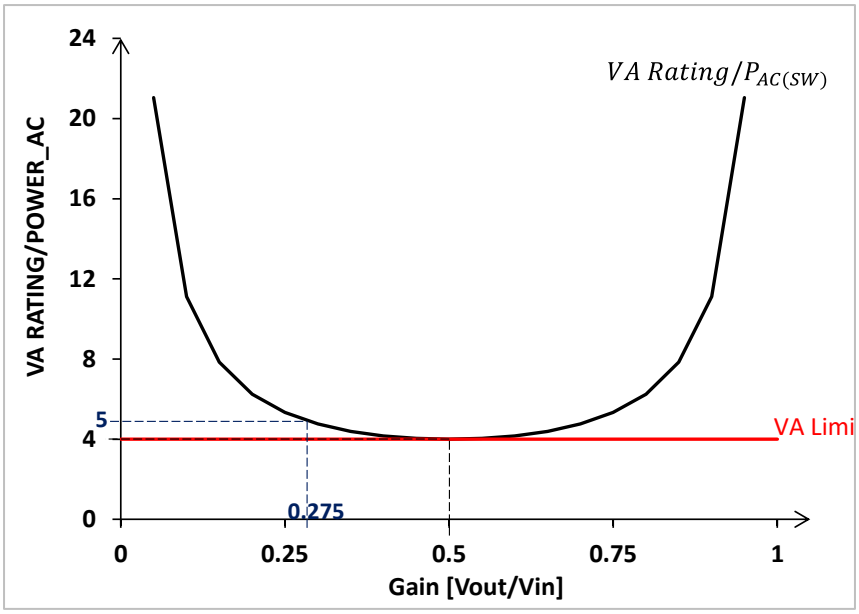


Fig. 2.15 VA Rating over processed power of a buck converter switch

2.4.2 Total VA Rating

The generated processed power by switches needs to be rectified by diodes or synchronous rectifiers with an equal VA rating. The total VA rating definition of a converter is given in (2.13). Thus, for multiple switches and diodes, the linear sum of the VA ratings of all switches and diodes should be used [23], [31].

$$VA_{total} = \sum VA_{switches} + \sum VA_{diodes} \tag{2.13}$$

As seen in equation (2.14) below, the minimum total VA rating becomes at least eight times the generated processed power when considering the diodes in the converter. This can be taken as the limit for VA Rating, or the best a converter can achieve. Thus, a converter that achieves a VA Rating close to $8 \times P_{AC}$ is a good converter and the opposite is true for a rating further from this limit.

$$VA_{total\ (minimum)} \geq 8 \times (P_{AC}) \tag{2.14}$$

2.4.3 VA Rating Buck Example

Consider the buck example shown in Fig. 2.10, its VA rating is calculated as shown in equation (2.15) below

$$VA_{total} = VA_{switch} + VA_{diode} = V_{in}\frac{I_{in}}{D} + V_{in}\frac{I_{in}}{D} \quad (2.15)$$

Substituting the input voltage of 12V and current of 1.25A, at a duty cycle of 0.275, results in a total VA rating of 110 VA, as shown in . The switch is poorly utilised with a utilisation factor of less than 0.2. The total VA rating is 10 times the processed power (P_{AC}) of the switch. This is expected when including the diode VA to the switch VA shown in Fig. 2.15. This means this converter is not at the minimum VA Rating which occurs at a gain of 0.5 for the buck.

Table 2.4 Buck Converter VA Rating Numerical Example

Buck Converter Parameters	Values
VA_{switch}	55.54 VA
VA_{diode}	55.54 VA
VA_{total}	109.1 VA
$U = P_{out}/VA$	0.199
P_{AC}	10.88 W

The fundamental limit on the VA rating and the combined ratings of the switch and diode for the buck example are plotted normalised by the input power ($V_{in} \cdot I_{in}$) in Fig. 2.16. The buck converter meets the fundamental VA rating at a gain of 0.5. The converter does not perform as well, at other gains, including at 0.275.

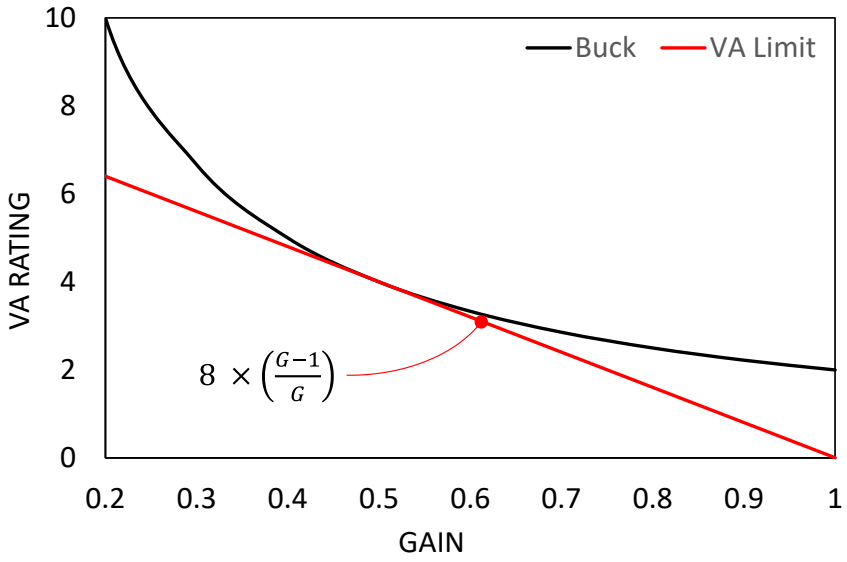


Fig. 2.16 Normalised VA Rating vs gain for buck converter and fundamental VA Limit.

If one were comparing converter topologies for the application of 12V to 3.3V solely using this VA Rating metric, a buck converter might not be the most suitable. The buck will be the most suitable for applications requiring 0.5 gain. Many other topologies with better VA Rating than the buck converter at this gain (0.275) exist and these will be explored later in Chapter 5.

2.4.4 Hybrid Switched Inductor vs Buck Converter

An example of a fundamental limit converter is the hybrid switched inductor shown in Fig. 2.17. Many other fundamental limit converter circuits exist, such as the zero-voltage switching converter, all interleaved buck converters and so on. For simplicity, the hybrid switched inductor is used to demonstrate the difference in VA rating performance. Note that the same analysis applies to all other topologies.

Fig. 2.17 B) and D); and C) and E) show the equivalent circuit of the hybrid switched inductor with switch "SW1" closed and opened respectively. The Hybrid converter has a gain of $G = \frac{D}{2-D}$, The full circuit analysis and average modelling for the Hybrid switched inductor is carried out in Appendix B.1. In preparation to plot the VA Rating over gain, $G = \frac{V_{out}}{V_{in}}$, the duty cycle can be expressed as a function of gain, $D = \frac{2G}{G+1}$.

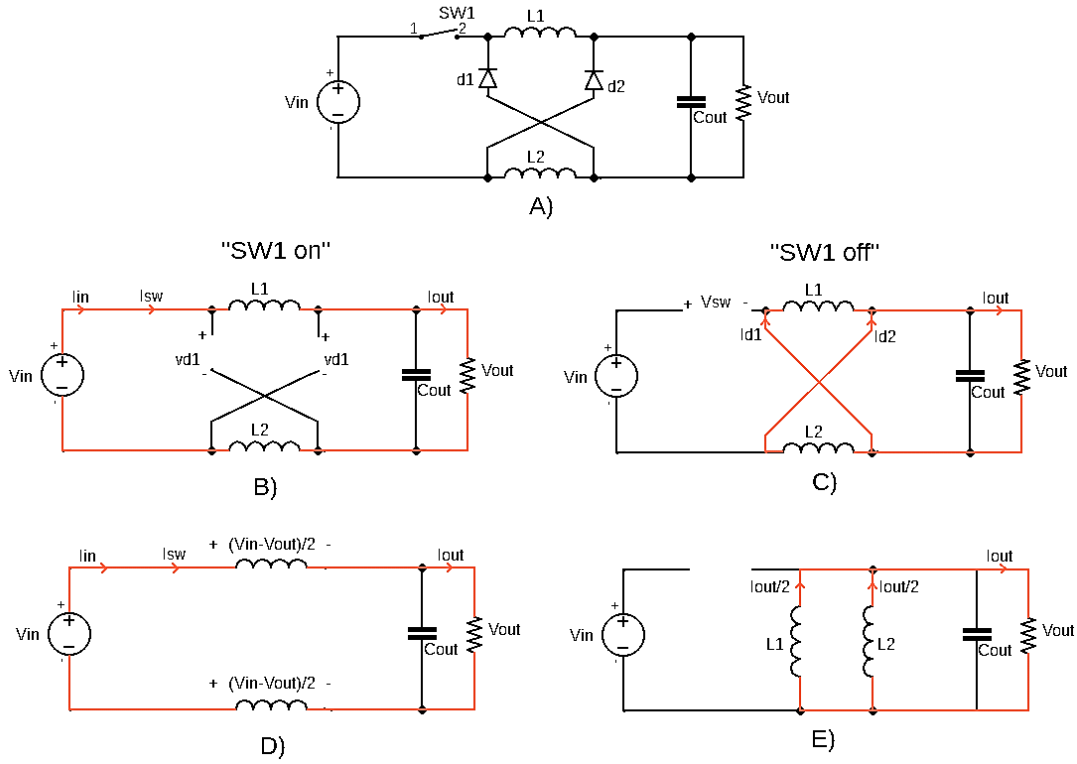


Fig. 2.17 Hybrid Switched Inductor Topology

The switch blocks the sum of the input and output voltage ($V_{in} + V_{out}$) when opened. When conducting, the maximum current through the switch is the output current (i_{out}). The VA Rating of the switch is given below in equation (2.16).

$$\begin{aligned} VA_{switch} &= (V_{in} + V_{out}) \cdot i_{out} \\ &= \left(\frac{V_{out}}{G} + V_{out}\right) \cdot i_{out} \\ &= V_{out} \cdot I_{out}\left(\frac{1}{G} + 1\right) \\ &= P_{out}\left(\frac{G+1}{G}\right) \end{aligned} \tag{2.16}$$

Each diode blocks half the switch voltage$\left(\frac{1}{2}(V_{in} + V_{out})\right)$ and conducts half the output current $\left(\frac{i_{out}}{2}\right)$. The VA rating of the two diodes is determined by the product of their blocking voltage and conducting current as shown in equation (2.17) below.

$$VA_{diode} = 2 \times \left(\frac{1}{2}(V_{in} + V_{out}) \cdot \frac{i_{out}}{2}\right)$$
$$= \frac{1}{2}\left(\frac{V_{out}}{G} + V_{out}\right) \cdot i_{out} \quad (2.17)$$
$$= \frac{P_{out}}{2}\left(\frac{G+1}{G}\right)$$

The total VA Rating of the converter is the sum of all the switch and diode VA Ratings as shown in equation (2.18).

$$VA_{total} = VA_{diode} + VA_{switches}$$
$$= \frac{P_{out}}{2}\left(\frac{1}{G} + 1\right) + P_{out}\left(\frac{G+1}{G}\right) \quad (2.18)$$
$$= \frac{3P_{out}}{2}\left(\frac{G+1}{G}\right)$$

The VA ratings of the buck converter and Hybrid switched inductor are plotted in Fig. 2.18 against the VA Limit ($VA_{LIMIT} = 8(1-G)$) derived in the VA rating chapter of this study. The plots are as expected, approaching high Ratings at the extreme duty cycles, i.e. close to 0. This is consistent with the common understanding that extreme duty cycles are unfavorable for DC-DC converters. This means the switches and other converter components have a limited time to transfer energy, which results in a number of losses, ripple, switch off losses, conduction losses, body-diode reverse-recovery loss, particularly at high frequencies [41]–[43]. This is a common theme amongst the topology metrics, such as stress factors, variance, and RMS as well as the fast-switching limit, except for the Wolaver limits.

Both converters approach the VA minimum limit at characteristic gains, where they have optimal switch utilization. The VA rating of the buck converter touches the minimum limit at 0.5 gain, this makes it optimal for halving applications based on its VA Rating. Whilst the hybrid switched inductor has its optimal at 0.3 and performs better for gains lower than 0.41. This characteristic makes the hybrid a better choice for high step-down conversion ratios.

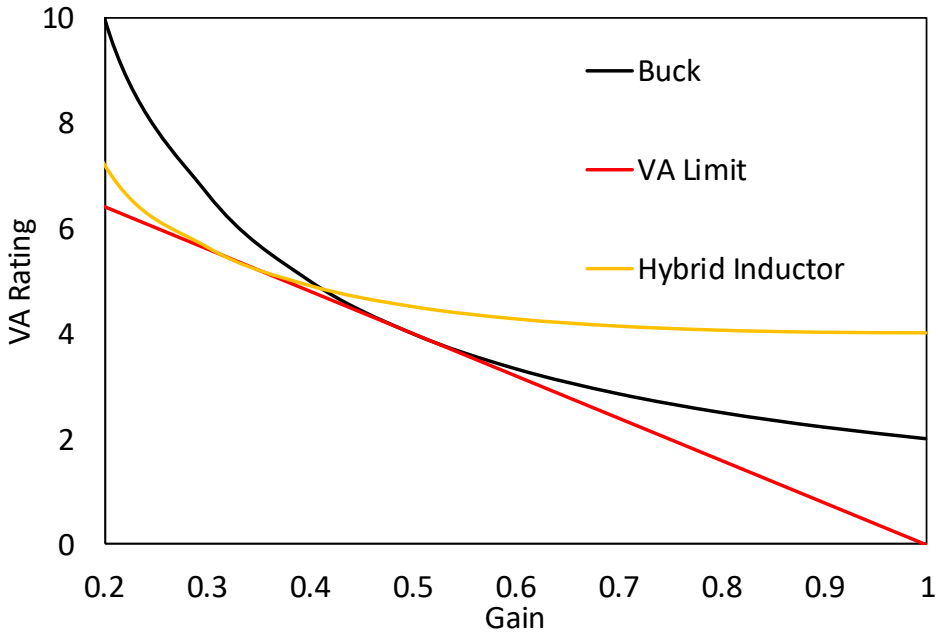


Fig. 2.18 VA Rating Buck and Hybrid Switched Inductor normalized by input power

2.4.5 Limitations of VA Rating

Adding a transformer with a suitable number of turns to a buck converter is one of several solutions [43]. This allows the buck converter to operate at its optimal duty cycle and thus VA Rating. Adding a transformer to the buck is not easy, but it will optimize the VA Rating at a tradeoff for other metrics. This can be achieved using the concept of partial power processing, discussed in [25].

The benefits of the VA Rating metric are apparent, from a single value of, VA Rating, a designer has insight into the cost and size of one of the most expensive and biggest components in the converter. These two properties (size and cost) are critical in converter comparison. VA rating metric also has a strong theoretical backing with the extension provided in this section from Moore et al and Wolaver's work.

One of the major shortcomings of the VA Rating as a sole metric is the focus on only the switches. Reactive components can be equally, if not more, costly and take up a lot more critical PCB real estate than switches.

2.5 Component Stress Factor

Another assessment strategy is the use of the stress factors. These metrics quantify the amount of resources needed to implement semiconductors, capacitors and inductors. As the metrics are technology independent it is possible to obtain a relative indication of the resources needed between different topologies.

The approach was originally suggested by Carsten [22] and refined by Wittenbreder [27]. It has been used with various modifications with some success by [13], [14]. However, the method itself has not been subjected to scrutiny. There have been cases where the three-stress factor have been added to produce a single metric [8], [10], they will not be added in this study.

A core assumption made in using this method is again the zero-ripple approximation. This removes the dependence of the inductor current ripple and gives a best case set of metrics. However, there is no fundamental reason why the assumption cannot be relaxed.

2.5.1 Semiconductor Stress Factor

Each type of component has a slightly different definition of the stress factor. The semiconductor stress factor is defined as the maximum voltage squared multiplied by the RMS current squared, normalized by the input power squared.

$$SF_{semi} = \frac{{I_{RMS}}^2 {V_{max}}^2}{{P_{in}}^2} \tag{2.19}$$

This attempts to find a device independent loss term. The resistance of the channel of a MOSFET is proportional to the square of the voltage, which multiplied by the RMS current can give a metric of the approximate comparative loss [27]. Using this metric exclusively assumes that all switches are MOSFET based, which while correct for synchronous rectifiers will not be accurate when using normal diodes. This metric also does not capture switching loss effects. In the examples given later the assumption of synchronous rectifiers will be used.

2.5.2 Capacitor Stress Factor

The capacitor stress factor is defined in a similar way with the square of the voltage being related to the volume (energy storage) and the RMS current related to the loss.

$$SF_{cap} = \frac{{I_{RMS}}^2 {V_{max}}^2}{{P_{in}}^2} \tag{2.20}$$

2.5.3 Inductor Stress Factor

The inductor stress factor is related to the RMS current as this gives the winding loss and the resistance is proportional to the number of turns (the applied voltage) and inversely proportional to the winding window area.

$$SF_{ind} = \frac{{I_{RMS}}^2 {V_{avg}}^2}{{P_{in}}^2} \tag{2.21}$$

The winding voltage average is defined as shown in equation (2.22).

$$V_{avg} = |D v_{Lon}| + \left|(1-D) v_{Loff}\right| \tag{2.22}$$

2.5.4 Buck Converter Example

To illustrate the utility of this approach the same buck example is considered. It is a simple matter to find the maximum voltages and the RMS currents under zero ripple conditions using the waveforms shown later in chapter 3, Fig. 3.3. The stress factors can be determined as a function of the converter gain as in equation (2.23) .

$$\begin{aligned} SF_{semi} &= \frac{1}{D} + \frac{1-D}{D^2} \\ SF_{cap} &= 4(D-1)^2 \\ SF_{ind} &= \frac{1}{D} - 1 \end{aligned} \tag{2.23}$$

The buck stress factors are plotted in Fig. 2.19.

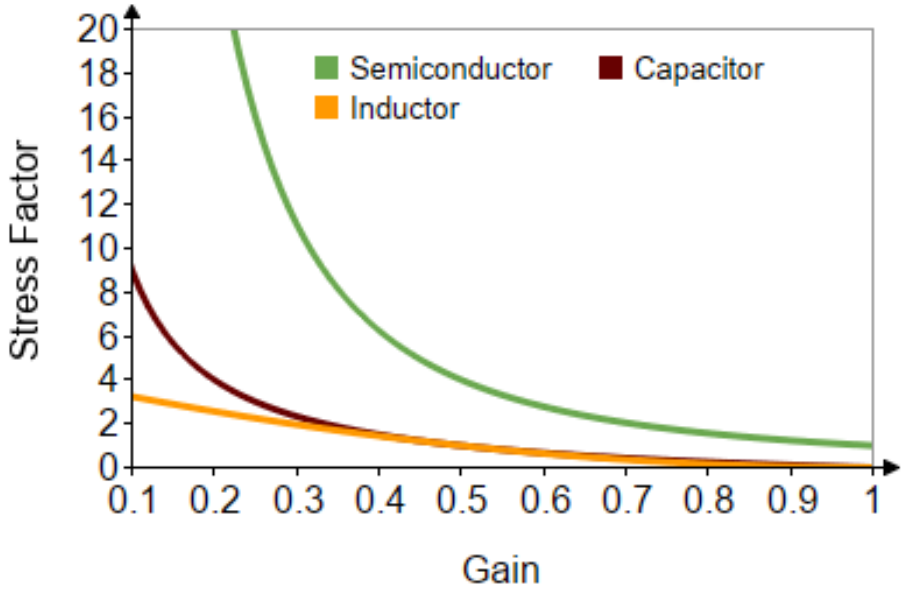


Fig. 2.19 Buck component stress Factor

At low gains, where the duty cycle becomes small there is a large stress on the switches. This points to the known difficulties of very small duty cycles. The capacitor and inductor stresses also tend to not favor low gains. At extreme duty cycles the stresses on the components particularly the switches are intense. This is because at a duty cylce of 10% as an example, the converter only has a tenth of the time to transfer power to the output. This is a common characteristic for switch mode converters revealed the metrics in the study and in literature.

2.6 Slow Switching Limit (SSL) and Fast Switching Limit (FSL)

The fast-switching limit (FSL) and slow-switching limit (SSL) are metrics for active semiconductor devices and passive components within a DC-to-DC converter [15]. The semiconductors were simply referred to as switches in the previous section, whilst passive components are reactive components. These metrics are based on the operational modes of switched-capacitors, at low and high operational frequencies. The switched capacitor converters are contenders for IoT applications due to their higher power density and efficiency relative to magnetic based converters. At low frequencies the impedance of switched capacitor converters becomes more capacitive, as the impedance of the switches

are negligible. Conversely the switch impedance becomes more dominant at higher frequencies, as the capacitor impedance drops significantly.

Though the metrics were originally developed for comparing switched capacitor converters, they are also applicable to other types. They have been extended to compare switched-capacitor converters with magnetic; hybrid; and resonant based converters [18], [28], [44].

The slow switching limit metric (M_{SSL}) defines the ratio of the converter output power $\left(\frac{V_{out}^2}{R_{SSL}}\right)$ and the power of the reactive components. The reactive component power is defined as a product of its energy density $\left(\frac{1}{2}CV_c^2\right)$ and switching frequency as shown in equation (2.24).

$$M_{SSL} = \frac{V_{OUT}^2/R_{SSL}}{\frac{1}{2}\sum_{capacitors} \mathrm{C} \cdot \mathrm{V_c^2} \cdot f_{sw}} \tag{2.24}$$

where V_{OUT} is the nominal voltage of the converter and R_{SSL} is the optimized SSL output impedance of the converter at low switching frequencies, i.e. impedance of capacitors.

The fast-switching limit metric (M_{FSL}) in equation (2.25) below is a ratio of the power handled by the converter $\left(\frac{V_{out}^2}{R_{FSL}}\right)$ and sum of power handled by each switch, i.e. product of the switch conductance (G_i) and the square of its blocking voltage (V_{sw}^2).

$$M_{FSL} = \frac{V_{OUT}^2/R_{FSL}}{\sum_{switches} G \cdot V_{sw}^2} \tag{2.25}$$

where R_{FSL} is the optimized output impedance of the converter at high frequencies, i.e. impedance of switches.

2.6.1 Metric Frequency Dependence

Appendix A: shows an example of the use of the SSL and FSL metrics with a doubler switched capacitor converter. The major result from the comparison is the frequency dependence of the converter output impedance. This directly translates to frequency dependence of the power handled by the converter plotted in . The plot shows the change in power handled by

the converter when frequency changes, whilst keeping the capacitance values the same. The plot at the low and high switching frequency shows the expected SSL and FSL metrics.

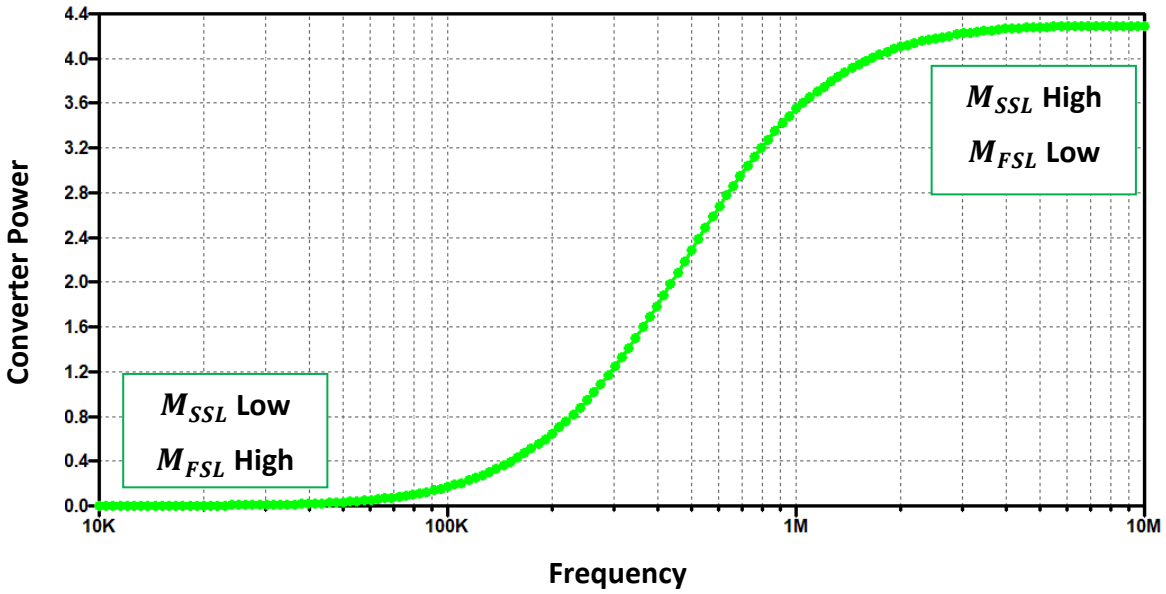


Fig. 2.20 Power Handled by Switched Capacitor Voltage Doubler vs Frequency

What we learn from this plot is that the topology performance at the high frequency depends on the switches. This is because the switch "on-resistance" (R_{FSL}) becomes more dominant. At high switching frequencies reactive components are miniaturized and their impedance (R_{SSL}) is negligible. Similarly, at the low frequencies the topology impedance is dominated by the reactive components (R_{SSL}). This coincides with the lower limit of the slow switching limit metric (M_{SSL}).

The frequency dependence of this metric provides a conceptual relation between the switch based and reactive component-based performance metrics. When comparing topologies with these metrics we expect to find topologies performing better at either extremes or a combination of the two.

In [28] and in [18] the ladder switched-capacitor converter topology, was found to be at the lower limit of SSL for integer conversion ratios compared to the inductor-based, hybrid and resonant switched capacitor converter counterparts. Another switched-capacitor topology, series-parallel, was also shown in both studies to be at the lower boundary of the FSL metric, this is attributed to the higher energy density of capacitors compared to inductors.

In [18] an energy based metric referred to as the passive volume is proposed related to the FSL and SSL metric.

The energy density and operational conditions such as frequency and conduction modes are not within the scope of this study. Since these are critical for converter, energy density is briefly mentioned below for use of the FSL and SSL.

2.6.2 Energy Density

The FSL and SSL metrics are energy-based metrics. Comparison of converters using energy-based metrics boils down to the energy density of the converters. When comparing different types of primary storage element converter types such as magnetic based, pure switched capacitor converter, resonant converters and hybrid converters, the energy density between converters is crucial. Even comparison of converters with the same type of primary storage elements.

The energy density between inductors and capacitors plays a huge role in their reactive component metrics. Capacitors have higher energy density compared to inductors, in the orders of hundreds to thousands. Thus, for the same PCB area, capacitors will have higher energy storage compared to inductors. This is a major reason why resonant switched capacitor converters are more favorable over pure switched capacitor converters.

So much so that even with the same topology by shifting the energy storage from inductors to capacitors has a significant impact on the performance metric. A typical example of this is, the trade-off of a smaller inductor in buck converter, thus bigger ripple, for bigger input and output capacitors.

2.7 Discussion and Summary

In this section, an introduction and examination of four distinct metrics, each targeting different performance aspects of a buck converter example: processed power, VA Rating, stress factors, and the Fast and Slow switching limit (FSL and SSL) metrics, the latter of which were specifically applied to a voltage doubler switched capacitor example. According to the Wolaver fundamental theorem, the traditional buck is at the Wolaver limit in terms of power processed, thus forms a baseline for other converter comparisons.

The results of the metrics show consistent but varying detail in performance of the buck example at varying duty cycles. A general increase in the metrics is observed at high conversion ratios. This is indicative of the buck converter processing more power while utilizing its switches less efficiently. The presence of higher stress factors at the extreme duty cycles signifies a greater need for resources such as inductor windings, capacitors, and semiconductors to implement the buck converter effectively. This phenomenon is particularly pronounced at duty cycles below 0.2, where the short time available for energy storage and release results in increased stresses and reduced performance.

While the results exhibited overall consistency, some variations were observed among the metrics. The processed power plot (Fig. 2.5) demonstrated a linear performance trend, whereas the VA rating (Fig. 2.16) and stress factors (Fig. 2.19) exhibited exponential decay at extreme duty cycles. These differences can be attributed to the absolute value definition of processed power versus the RMS-based definition of stress factors.

The processed power metric offers an averaging effect on performance, simplifying converter analysis and comparison, as demonstrated in the subsequent chapter. Conversely, the RMS-defined stress factors provide a more detailed performance metric by closely resembling converter waveforms. This insight is further developed in Chapter 4, where an RMS-based metric with the potential to unify diverse converter metrics into a cohesive framework is proposed.

Moreover, while the FSL and SSL metric are primarily applicable to switched capacitor converters, their inclusion in this discussion highlighted their relevance. These metrics highlight the dependence on frequency and energy density of primary storage elements, such as capacitors or inductors, essential factors for low-level converter comparison.

In summary, metrics from literature old and new are presented in this section. Each metric is defined and interpreted in the context of a buck example. Through this analysis, we showcase the efficacy of the processed power metric in establishing performance baselines, highlight the limitations at extreme duty cycles, and highlight the utility of stress factors in providing additional insights into converter performance. The differences observed between processed power and stress factors emphasize the importance of considering multiple metrics to gain a holistic understanding of converter behavior.

Chapter 3 Averaged Topology Modelling: (Switches)

3.1 Introduction

This chapter presents the process of averaged topology modelling as a tool to place converters on equal footing. This modelling tool reduces any converter topology to its fundamental shape or structure. This allows comparison of the fundamental properties of each converter.

To the authors knowledge the converter averaging proposed in this study does not exist in the form presented. Thus, a detailed modelling procedure is provided, including a motivation for the average model considering circuit theory and energy conservation. This chapter expands on existing converter analysis by presenting and demonstrating the utility of this tool for reducing complexity of any converter topology to its fundamental or core shape. An interpretation and relation to the Wolaver limit is also provided.

The chapter is arranged as follows: Firstly, the background of average topology modelling in literature is provided, followed by a step-by-step modelling procedure. The average topology model is shown to meet fundamental circuit theory. Thereafter standard topologies are presented followed by an analysis of converters at the fundamental limit. Finally, a discussion of the application of the modelling tool for converter assessment.

3.2 Background

Average topology modelling in this context is defined as the reduction of the circuit to its fundamental shape or structure. This averaging process is different from the low-frequency averaging that is commonly done to find the small signal analysis of the converter for control purposes. In [45], switch averaging shows the effects of the control signal. The approach preserves inductors and capacitors even after averaging. In [46] a similar modelling is applied as in [1] but omits the inductor and capacitor component in the equivalent average modelling of a Sepic and Cuk.

The circuit averaging presented in this chapter, results in a simplified electric circuit, containing the averaged switch elements. The average topology model is proven to meet

Kirchhoff's current and voltage laws and energy conservation principles. The resultant model omits all time dependent components including capacitors, inductors, even transformers. The process gives the theory its circuit independence by extracting the underlying DC circuit structure. Average topology modelling is motivated as a first step in assessing multiple converters since it provides a high-level converter assessment.

The next section provides a step-by-step procedure for average topology modeling. The outline of this section is shown in Fig. 3.1 below and each of the steps will be described in detail.

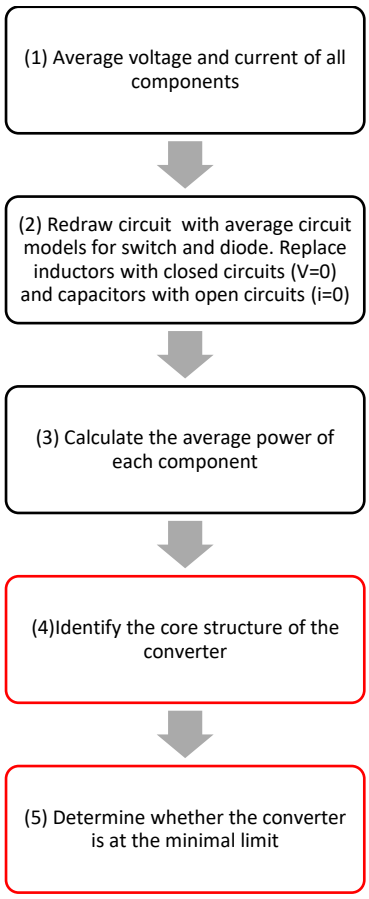


Fig. 3.1 Average Topology modelling procedure, validation, and benchmarking

3.3 Average Topology Modelling Procedure

This section goes into detail of the average topology modelling procedure illustrated in Fig. 3.1 . The procedure can be applied to any converter by replacing inductors with short circuit(s) and open circuit(s) for all capacitors. The remaining structure consists of a network of the average models of the diodes and switches, which is referred to as the core structure of the converter. The procedure from steps 1 to 3 is described in this section, and in detail for each component. Steps 4 and 5 are covered in the Sections 3.5, which presents the standard DC-DC converter topologies and identifies the type of topology using the average model. The subsequent section provides a topological interpretation of the fundamental Wolaver limit.

Step 1: Average Voltage and Current

The first step in determining the average topology model is taking the average voltage and current of all the converter components, the source, switches, diodes, capacitors, inductors, and the load. The process is detailed for each component in Sections 3.3.2 to 3.3.5.

To calculate the averages, the converter switching modes are identified. Take the trivial example of a buck converter in Fig. 3.2, it has two switching modes when the switch SW is closed, Fig. 3.2.b), and open, Fig. 3.2.c).

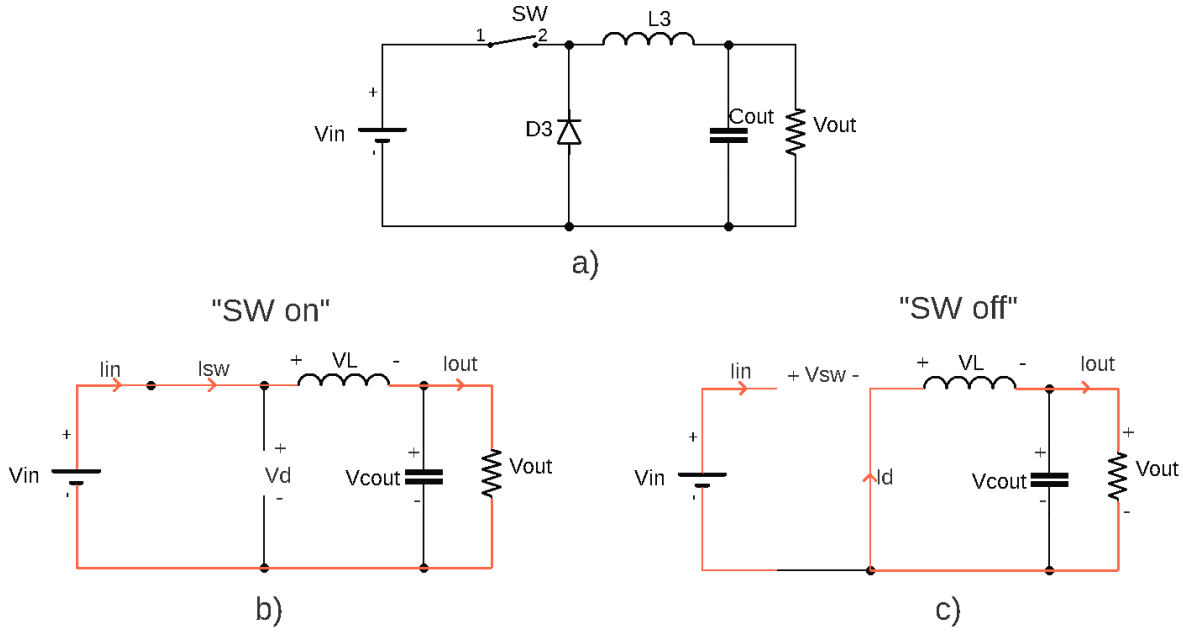


Fig. 3.2 a) Buck circuit, b) switch "on", and c) switch "off"

The waveforms of each component are then determined using circuit analysis, as shown in Fig. 3.3 for the buck example. From the waveforms, zero ripple is assumed. Ripple has no effect on the average transformation presented.

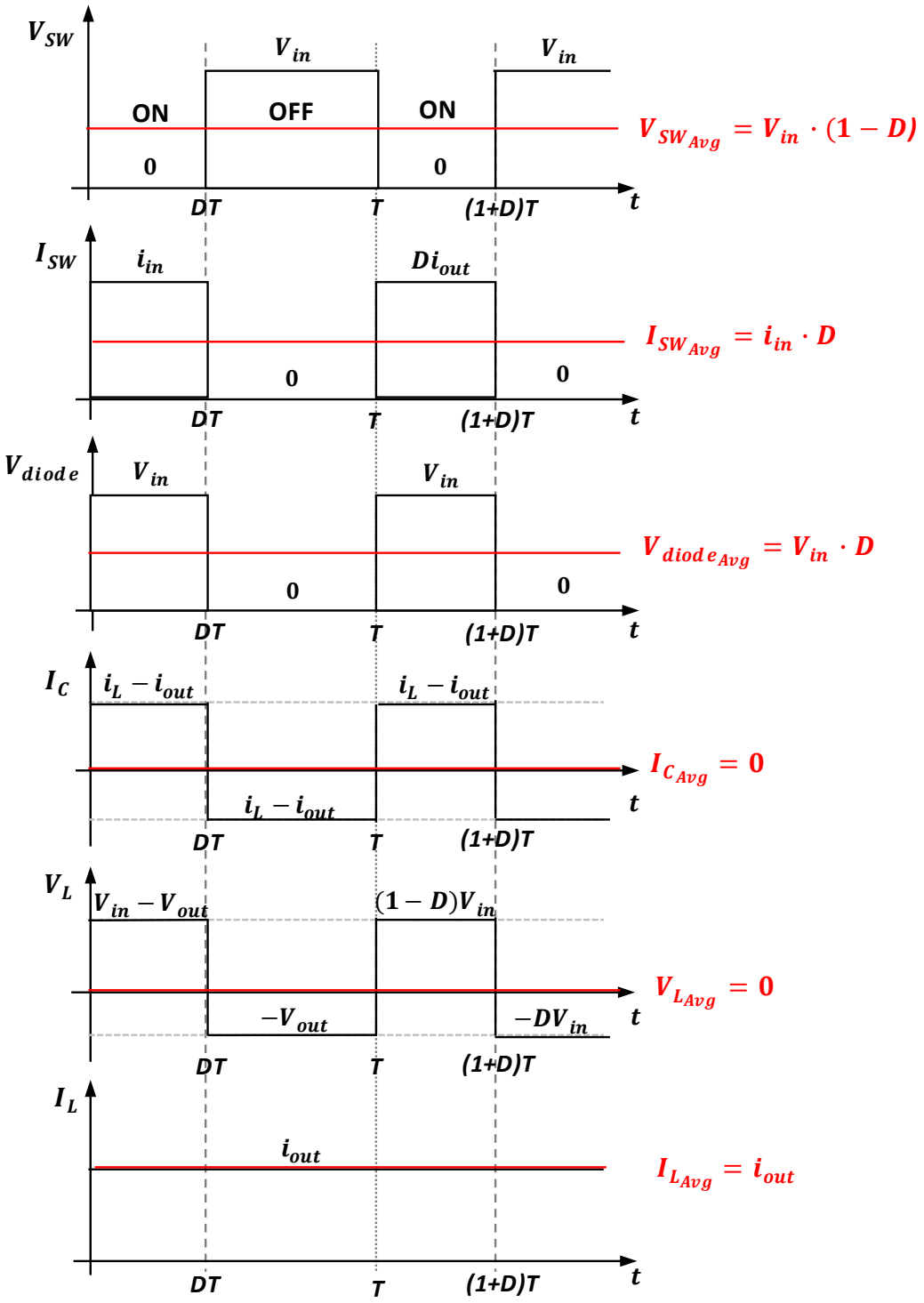


Fig. 3.3 Buck converter waveforms (zero ripple assumed)

Once the waveforms are determined the averages of each component (V_{Avg} , I_{Avg}) are calculated based on the timing for each mode as shown in equation (3.1) below for the buck converter.

$$V_{Avg} = v_{on} \cdot DT + v_{off} \cdot (1 - D)T$$
$$I_{Avg} = i_{on} \cdot DT + i_{off} \cdot (1 - D)T \quad (3.1)$$

where D is the duty cycle, v_{on}, i_{on} and v_{off}, i_{off} are the component voltages and currents when the switch is "on" and "off", T is the period.

For any other converter, the averages are determined as usual. Equation (3.2) below provides are general equation for determining average voltage and current with n switching states.

$$V_{Avg} = v_1 \cdot t_1 + v_2 \cdot t_2 \ldots + v_n \cdot t_n$$
$$I_{Avg} = i_1 \cdot t_1 + i_2 \cdot t_2 \ldots + i_n \cdot t_n \quad (3.2)$$

Step 2: Redraw the circuit replacing diodes and switches with their average models

Once the averages, V_{Avg} and I_{Avg} have been determined according to the equations above. The average model can be redrawn in this step with the equivalent average models of the switch and diode. The resultant circuit for the buck converter is shown in Fig. 3.4.

In the figure and in all other average models the reactive components "disappear", i.e., they become open for the capacitor or short circuit for the inductor. Sections 3.3.4 and 3.3.5 provide the motivation for this result based on volt-second balance and charge-balance principles.

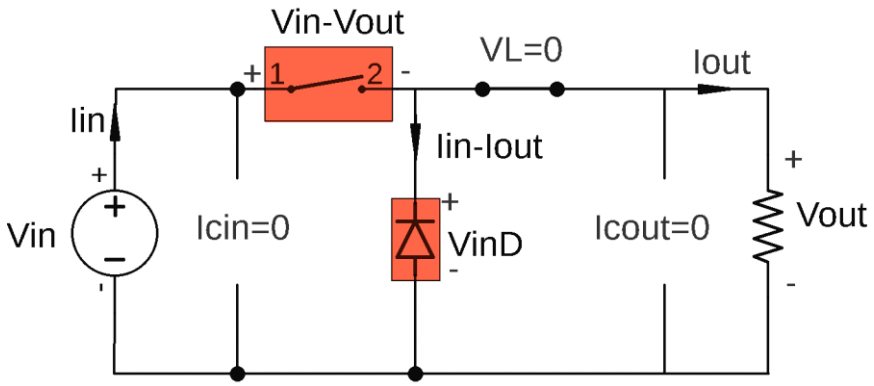


Fig. 3.4 Buck converter average components

Step 3: Calculate the dc power of each component

The third step is the calculation of dc powers, defined as a product of the average voltage and current. The sum of all dc powers should add up to zero, as an indication of energy conservation. This can thus be used as a validation step for the modelling.

This dc power is similar to and can be interpreted as power processed by the switches and diodes as in chapter 2.2.3. The average power of the switch can thus be thought of as the power required to converter the DC input power to "AC" or fluctuating power. The opposite and equal power can also be thought of as the power handled by the diode to rectify the AC power back to DC on the output.

So, the dc power can be used to determine whether a topology is at the Wolaver limit, i.e. $\left|P_{DC(diode)}\right| = P_{out} \cdot \left(\frac{G-1}{G}\right)$. Once we have the averages, the topology model can be obtained.

Step 4 and Step 5: Average Topology Model

By calculating the dc power in step 3, one can already mathematically determine if the converter is at the fundamental limit. Step 4 and step 5, provide a visual "topological" method of determining the same.

The circuit drawn in Step 2, Fig. 3.4, is simplified to create an average topology model. The switch and diode are replaced with rectangular symbols to form the model shown in Fig. 3.5. This figure represents the average topology model of the buck converter. It was

previously shown that the buck converter is at the fundamental limit mathematically. From the figure the average topology model is shown and is named a fundamental topology, this is explained in Section 3.5.

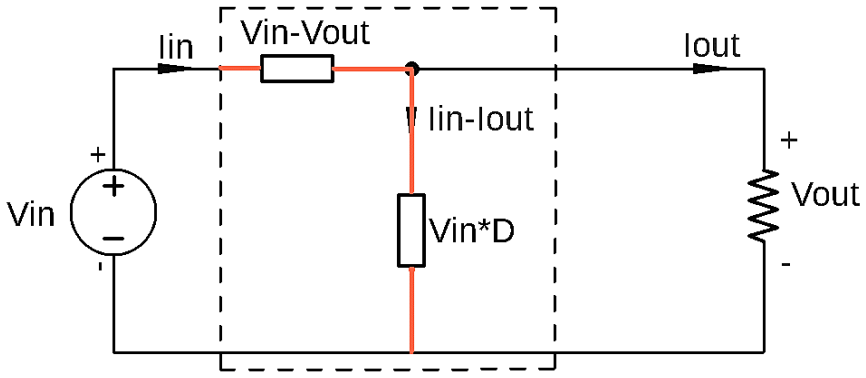


Fig. 3.5 Buck Converter Equivalent Average Topology Model

3.3.1 Average Power Formulation

The average power for each component is defined as the product of its average voltage and average current. According to the IEEE Std 1459-2010 average power is defined as shown in equation(3.3) below [47].

$$P_{Avg} = \frac{1}{T}\int_{0}^{T}\left(V_{Avg} + v_{AC}(t)\right)\left(I_{Avg} + i_{AC}(t)\right)dt \tag{3.3}$$

The resultant equation has a DC component (P_{DC}) and AC component (P_{AC}) shown in equation(3.4) below [35].

$$P_{Avg} = 0 = \underbrace{V_{Avg}I_{Avg}}_{P_{DC}} + \underbrace{\frac{1}{T}\int_{0}^{T} v_{AC}(t)i_{AC}(t)dt}_{P_{AC}} \tag{3.4}$$

The AC and DC part of the switches and diodes in a switched mode converter are opposite and equal, thus resulting in zero average power. The average converter topology model is based on the DC components of the average powers in (3.4). Though this formulation of dc power is not defined in IEEE, but it is useful and shown to meet fundamental circuit theory and energy conservation, in the next Section 3.4 .

3.3.2 Source and Load

This section looks at the averaging procedure for the source and load. The DC source remains unchanged since its equivalent to its average value. Thus, average model of the source is modelled as its DC voltage and current as seen in equation (3.5) below. As a result, the average source model is interpreted in the traditional sense. Modelling of the reactive "AC" component of the source is handled in the next chapter focusing on reactive components.

$$P_{in_{DC}} = I_{in} \cdot V_{in} \tag{3.5}$$

The load is assumed to be resistive, thus, the resultant component of the load is simply modelled as a resistor in the traditional sense, with the rated output voltage and current. The component model of the load thus remains unchanged from the converter circuit in Fig. 3.4 to the average model shown in Fig. 3.5.

3.3.3 Switches and Diodes

This section provides a procedure to calculate the average model, voltage, current, and power, of switches and diodes in a converter for Steps 1 and 4 in Fig. 3.1. The switch and diode block current in one cycle and conduct in the other. If we consider ideal switches and diodes, their losses are assumed to be zero. Taking power in the conventional sense for the waveforms in Fig. 3, will result in zero power over a full switching cycle since the voltage and current waveforms do not overlap. In this case, the dc power is taken as the product of the average voltage and average current over a full cycle shown in equation (3.6) for the switch

$$P_{SW_{DC}} = I_{SW_{Avg}} \cdot V_{SW_{Avg}} \tag{3.6}$$

where the average voltage ($V_{SW_{Avg}}$) for the buck converter according to (3.2) is given as

$$V_{SW_{Avg}} = V_{SW_{on}} \cdot DT + V_{SW_{off}} \cdot (1 - D)T \tag{3.7}$$

and the average current is given by

$$I_{SW_{Avg}} = I_{SW_{on}} \cdot DT + I_{SW_{off}} \cdot (1 - D)T \tag{3.8}$$

Similarly, for the diode, the power is given by equation (3.9).

$$P_{diode_{DC}} = I_{diode_{Avg}} \cdot V_{diode_{Avg}} \tag{3.9}$$

The average voltage ($V_{diode_{Avg}}$) and current ($I_{diode_{Avg}}$) for the diode are formulated similar to the switch equations (3.7) and (3.8).

Consider the same buck converter circuit in Fig. 3.2 and waveforms in Fig. 3.3 at the beginning of this subsection 3.3. Substituting the waveforms in into equation (3.6) and (3.9) results in non-zero average power equations listed in

Table 3.1 List of Buck converter average component voltage, current and power for the switch and diode. The diode and switch are represented by their average equivalent model in Fig. 3.5.

The resultant component(s) for the switch and diode are not resistors but average models with the component's average voltage and current. Thus, the power is not defined in the traditional sense and does not dissipate energy. This power can be interpreted as processed power, “absorbed” and “released” by switches and diodes to perform inversion and rectification functions respectively. The switch absorbs DC power (P_{DC}) from the source and releases fluctuating power ($-P_{AC}$). The diode absorbs fluctuating power and releases DC power to the load.

It is critical to assume that the sum of the dc powers of the switch(s) and diode(s) in a converter will be equal and opposite as illustrated in Table 3.1. This is expected since the input and output power are balanced, meaning the converter needs to a have balance as well. The balance within the converter is represented mathematically in equation below.

$$\sum P_{SW_{DC}} = -\sum P_{diode_{DC}} \tag{3.10}$$

The above equation can be proved as shown in equation below, by substituting the equations in .

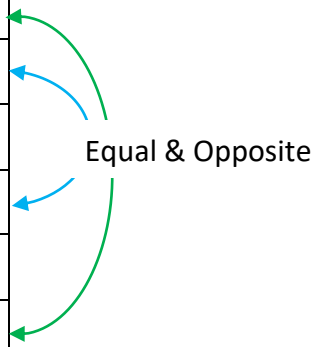
$$V_{in} \cdot (1 - D) \cdot I_{out} \cdot D = -V_{in} \cdot D \cdot I_{out} \cdot (1 - D) \tag{3.11}$$

This can be thought of as the same power inverted by the switch from DC to AC is rectified back to DC by the diode. For this case of a single switch and diode, we can easily say the power processed by the switch is exchanged equally and processed by the diode as illustrated in

Table 3.1. However, it gets complicated for two or more switches, which result in more than two switch states within a full cycle, to track the power exchange between the components, beyond observing the average balance. The interleaved buck converter is used as an example to show this limitation in Section 5.7.1.

Table 3.1 List of Buck converter average component voltage, current and power

	V_{AVG}	I_{AVG}	P_{AVG}
Input Supply	V_{in}	I_{in}	$V_{in} \cdot I_{in}$
SW	$V_{in} \cdot (1-D)$	$I_{out} \cdot D$	$V_{in} \cdot (1-D) \cdot I_{out} \cdot D$
L	0	I_{out}	0
diode	$V_{in} \cdot D$	$-I_{out} \cdot (1-D)$	$-V_{in} \cdot D \cdot I_{out} \cdot (1-D)$
C_{out}	V_{out}	0	0
Load	V_{out}	I_{out}	$V_{out} \cdot I_{out}$



3.3.4 Capacitor

This section shows why capacitors are replaced with open circuits in an average topology model using the principle of capacitor charge balance. It is expected that the average current of every capacitor in a DC-DC converter at steady state to be zero over a full cycle. This is due to the requirement of charge balance shown in equation (3.12) below:

$$Charge\ Balance:\ V_{c(T)} - V_{c(0)} = \frac{1}{C}\int_0^T i_C(t)\,dt = 0$$
$$\frac{1}{T}\int_0^T i_C(t)\,dt = I_{C_{Avg}} = 0 \tag{3.12}$$

where $V_{c(T)}$ and $V_{c(0)}$ is the capacitor (C) voltages at time $t = T$ and $t = 0$ respectively. $i_c(t)$ and $I_{C_{Avg}}$ is the instantaneous current and the average current over period(T) respectively.

To maintain steady-state, the charging ($I_{c_{on}} \cdot D \cdot T$) and discharging ($I_{c_{off}} \cdot (1-D) \cdot T$) phases need to be equivalent in Fig. 3.6, showing the capacitor current (i_C) waveform.

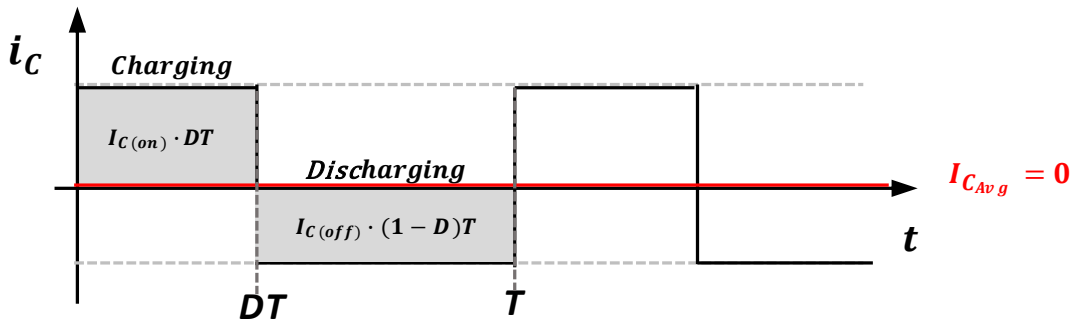


Fig. 3.6 Capacitor Charge balance (zero ripple)

This means the shaded areas under the graph are equal and opposite. Thus, the average capacitor current, shown as the red line in the figure, over a complete cycle will be zero for any capacitor in the converter, as shown in equation (3.13) below.

$$I_{C_{Avg}} = I_{c_{on}} \cdot D \cdot T + I_{c_{off}} \cdot (1-D) \cdot T = 0 \tag{3.13}$$

The average voltage across the input capacitor ($V_{C_{Avg}}$) is equal to the input voltage and equal to the output voltage for the output capacitor (C_{out}) in the case of the buck converter in Fig. 3.2. Thus, the dc power ($\mathrm{P_{C_{DC}}}$) of all capacitors is expected to be zero as shown in equation (3.14) below

$$P_{C_{DC}} = I_{C_{Avg}} \cdot V_{C_{Avg}} = 0 \tag{3.14}$$

As a result, capacitors are modelled as open circuits according to the procedure in Fig. 3.1 and represented as shown in the average model circuit in Fig. 3.4 and Fig. 3.5.

3.3.5 Inductor

This section motivates for modelling inductors as short circuits in the average topology model procedure in Fig. 3.1. Under steady-state conditions, the volt-second balance principle states that the average voltage across an ideal inductor must be zero. A mathematic definition of inductor volt-second balance is given in equation (3.15).

$$Volt - Sec\ Balance:\ I_{L(T)} - I_{L(0)} = \frac{1}{\mathrm{L}}\int_0^T v_L(t)\,dt = 0$$
$$\frac{1}{\mathrm{T}}\int_0^T v_L(t)\,dt = V_{L_{Avg}} = 0 \tag{3.15}$$

where $\mathrm{I}_{\mathrm{L(T)}}$ and $\mathrm{I}_{L(0)}$ is the inductor (L) current at time $t = T$ and $t = 0$ respectively. $v_L(t)$ and $V_{L_{Avg}}$ is the instantaneous and the average voltage over period(T) respectively.

Volt-second balance is shown graphically in Fig. 3.7. The total shaded area, i.e., volt-seconds, under the inductor current versus time waveform over a full cycle is zero. The dc power of inductors become zero since their average voltage is zero ($V_{L_{Avg}} = 0$), as shown in equation (3.16) below.

$$P_{L_{DC}} = I_{L_{Avg}} \cdot V_{L_{Avg}} = 0 \tag{3.16}$$

This means the inductor can be replaced with a zero-voltage source, which is simply a short-circuit as shown in Fig. 3.4 and Fig. 3.5.

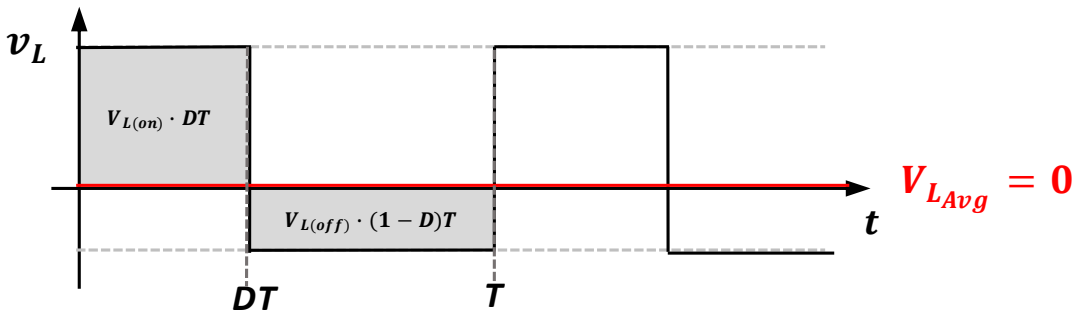


Fig. 3.7 Inductor volt second balance

3.4 Modelling Validation

This section shows that the average topology model discussed in the previous section meets basic circuit theory and thus energy conservation, though the process followed to determine dc power is non-conventional. However, the resultant average model is shown to meet fundamental circuit theory. The average topology model constructed in the previous section is shown to meet Kirchhoff's voltage (KVL) and current (KVL) laws and consequently, Tellegen's power theorem using a numerical example.

The average topology model must meet KVL and KCL because of the following reasons, firstly because the averaging transformation is linear. So, if we start with a circuit where Kirchhoff is valid, then the averaging operation preserves the validity.

Secondly, due to the energy and power conservation principle of Tellegen. Which states that in an electrical circuit network the sum of powers is equal to zero as shown in equation (3.17) below [48], [49].

$$\sum v \cdot i = 0 \tag{3.17}$$

The theorem further states that in the same network, if v and i are transformed into v' and i', in this case through averaging. Then the product of the transformed voltage and current, still meets the theorem as shown in equation (3.18) below.

$$\sum v' \cdot i' = 0 \tag{3.18}$$

Consider the buck converter example in the previous section, with a 12 V input voltage and 3.3V output. By applying KVL to all the loops of the average topology model as shown in Fig. 3.8 the three voltage equations are shown in (3.19) below.

$$\begin{aligned} KVL\ loop\ 1: &- V_{in} + V_{SW_{Avg}} + V_{d_{Avg}} = 0 \\ KVL\ \ loop\ 2: &- V_{d_{Avg}} + V_{out} = 0 \\ KVL\ \ loop\ 3: &- V_{in} + V_{SW_{Avg}} + V_{out} = 0 \end{aligned} \tag{3.19}$$

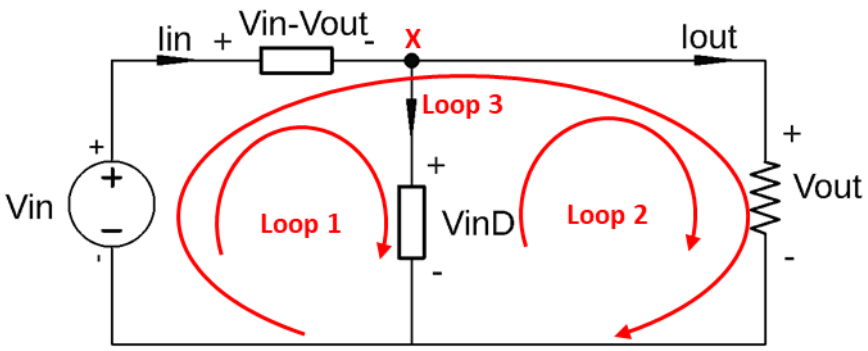


Fig. 3.8 KVL an KCL on the buck average topology model

Similarly applying KCL on the buck converter at the node marked X in the same figure results in equation (3.20) below, which leads to a trivial result.

$$KCL\ at\ Node\ X\ (in\ Fig.\ 3.8): i_{in} - i_{diode} - i_{out} = 0 \qquad (3.20)$$

where $i_{diode} = (i_{in} - i_{out})$.

The average voltages, currents and powers for each component are shown in Fig. 3.9 below for the same buck example used in Section 2.2.5. An absorbing convention is used and thus the negative input power signifies "delivering power" and positive power signifies absorbing. It is critical to note that the power "absorbed" and "delivered" by the switch and diode respectively are "power processed" by the components and not necessarily power dissipation in the traditional sense. Substituting numerical values for the buck converter into equations (3.19) and (3.20) proves that the average topology model meets KVL and KCL.

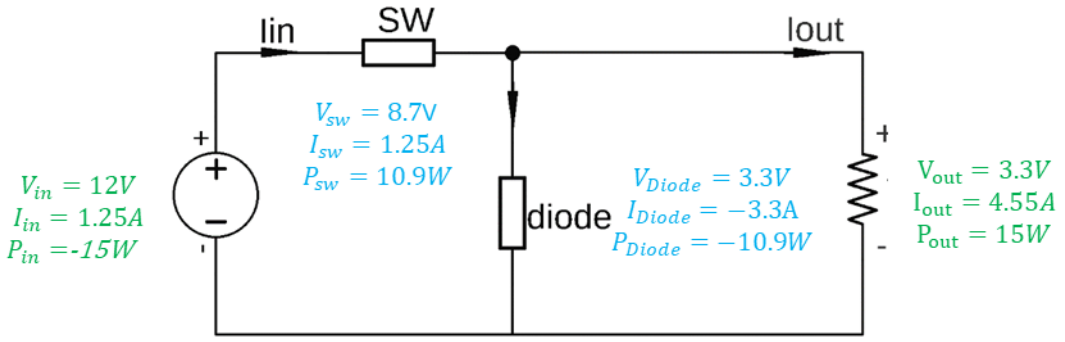


Fig. 3.9 Buck average model with values (absorbing Convection, negative is delivering)

A consequence of KVL and KCL is the Tellegen's theorem which states that the sum of power delivered by various elements in various branches is zero for any network. Tellegen Theorem is represented mathematically in equation (3.21) for a buck.

$$P_{in} + P_{SW} + P_{Diode} + P_{Load} = 0 \tag{3.21}$$

Substituting the average powers in Fig. 3.9 to (3.21) proves that that the buck converter meets Tellegen's theorem as expected.

Thus, because of the linear nature of the averaging transformation and Tellegen's theorem, the averaged topology model meets energy conservation. This proves the usefulness of the averaged topology model for any DC-DC converter circuit.

3.5 Standard Topologies

Understanding of standard topologies is crucial for DC-DC converter comparison. We can see the standard topologies as a benchmark of performance. A circuit topology is the shape taken by the network of interconnections of the circuit elements or components. So, a topology refers to how elements, electronic components, relate spatially to each other. It's noted that numerous circuit layouts exist that reduce to the same topology. A standard topology is the fundamental shape for achieving a specific function, step-up, or step-down. Identifying the core structure aids in topology comparison by placing the converters in equal footing.

Fig. 3.10 shows some of the standard topologies, the "L", "pi", "T", "H" shape and so on are the most common. Different converters result in one of the shapes shown in the figure.

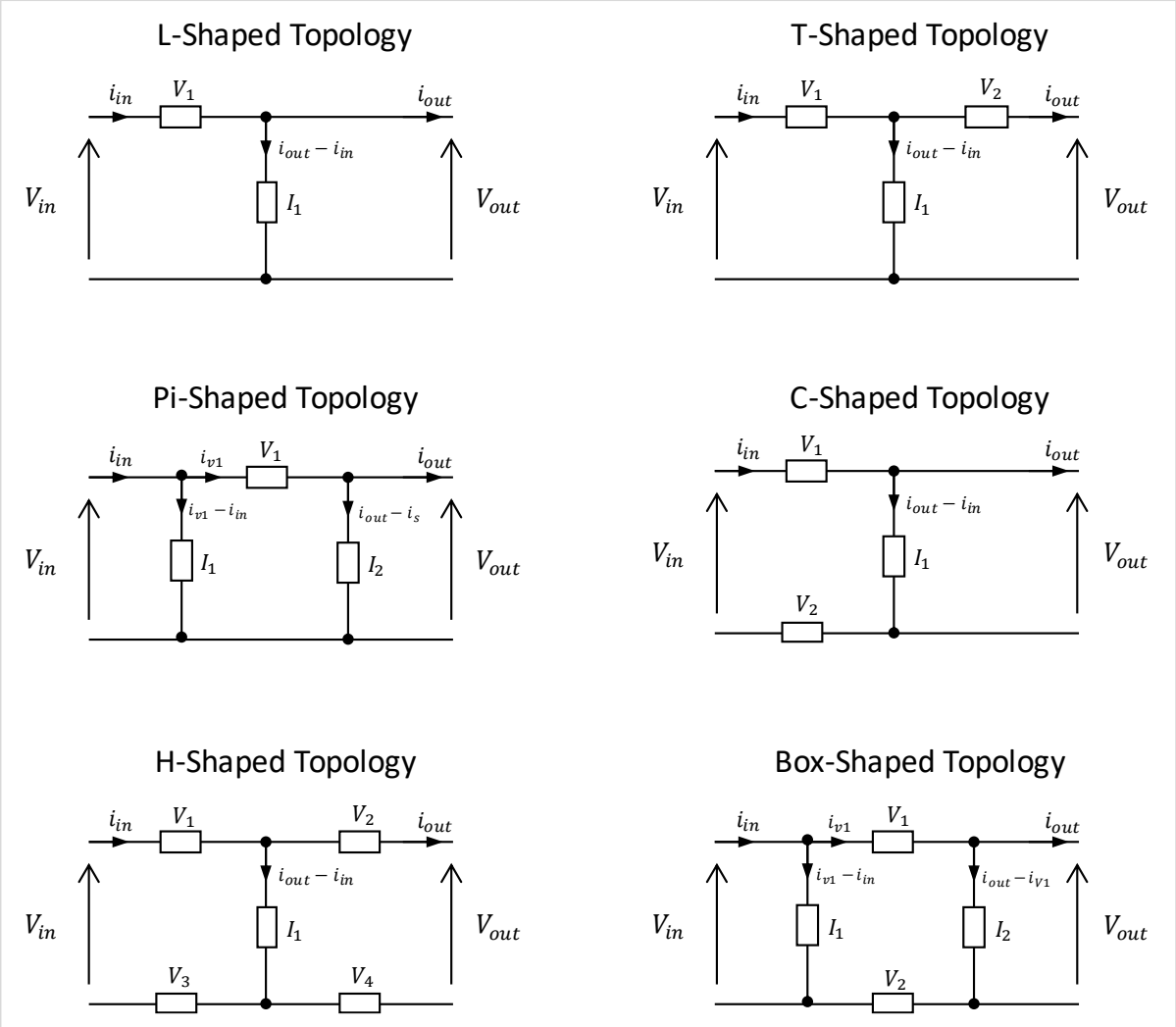


Fig. 3.10 Standard Topologies

3.5.1 Average Modelling and Standard Topologies

The process of "how to obtain the core shape" was discussed in the previous Section (3.3) on the averaged topology modelling procedure. It was highlighted that the averaged topology modelling provides the core shape of a converter. This core shape results in a network of elements, with averaged voltages and currents, representative of the operation of the converter. The resultant network is based solely from the switches and diodes since all the reactive components disappear, capacitors become open circuits and inductors short circuits. For the buck converter, the averaged topology model is shown in Fig. 3.11. The buck converter has the standard "L" shape highlighted in red on the circuit.

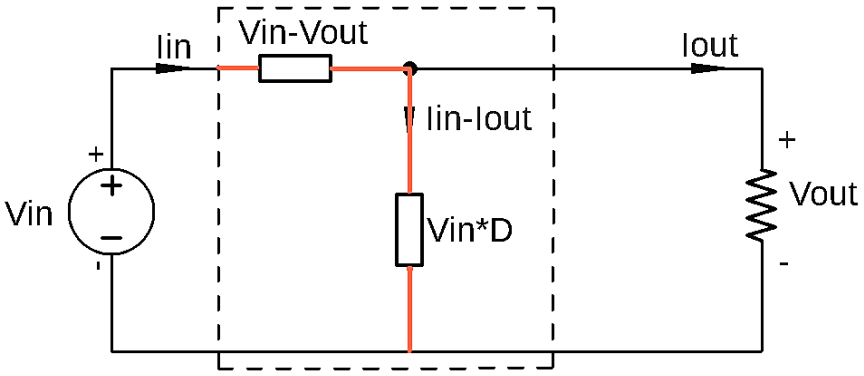


Fig. 3.11 Buck Converter has "L" shaped topology

One way to think about the topology in Fig. 3.11 is as a potential divider, with lossless elements. Consider a potential divider shown in Fig. 3.12, with two series elements R1 and R2.

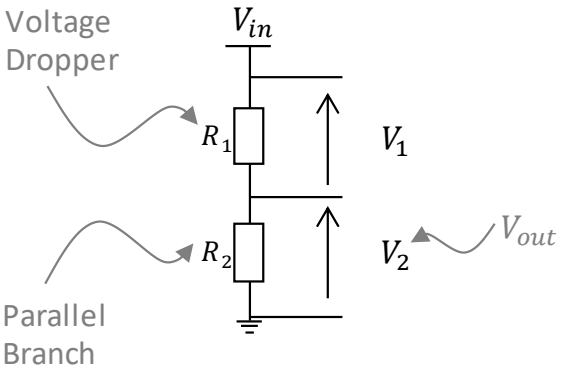


Fig. 3.12 Potential divider

The two elements divide the input voltage into V1 across R1 and V2 across R2. The output is connected across R2 with an output voltage V2. This illustrates how an L shaped step-down converter operates, where R1 is the voltage dropper whilst R2 is the "parallel current source". Thus, R1 and R2 represent an L shaped topology.

As an additional note, looking at the standard topologies one can see how a series dropper only converter cannot be a minimum topology for step down. Since it will drop both the current and voltage, and thus be a "lossy" converter. The presence of the parallel current source balances the output current to obtain the same power in the input.

3.5.2 "L" Shape: Minimum Step-Down Topology

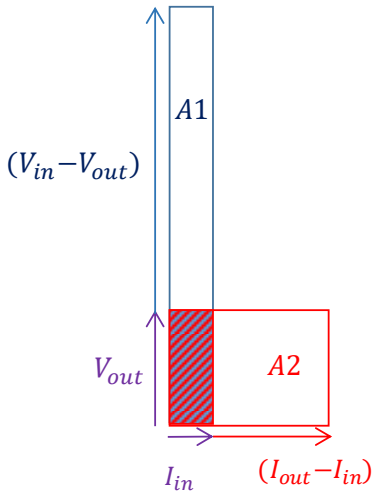
The L shape in Fig. 3.11 consists of a series voltage dropper, with voltage ($V_{in} - V_{out}$). It also has a parallel current source branch to supply the stepped-up current between the input and output ($I_{in} - I_{out}$). This is the minimum implementation to step down voltage because a single voltage dropper and current source are used.

According to Wolaver the resultant circuit model for a topology at the Wolaver limit is L shaped. This means it processes the least amount of power or has the least DC power given by $\left|P_{DC(diode)}\right| \geq P_{out} \cdot \left(\frac{G-1}{G}\right)$. This can be proved using the power of the diode in Fig. 11. The diode voltage is ($V_{diode} = V_{in} \cdot D$). For the buck converter the duty cycle is equal to the voltage gain and thus equal to inverse of current Gain $D = \frac{1}{G}$. Thus, the diode current is $i_{diode} = i_{in}\left(\frac{D-1}{D}\right)$. The product of the two is shown below in equation (3.14).

$$\begin{aligned} \left|P_{DC(diode)}\right| &= (V_{in} \cdot D) \cdot \left(i_{in}\left(\frac{D-1}{D}\right)\right) \\ &= V_{in} \cdot i_{in}(D-1) \\ &= P_{in}\left(\frac{1}{G} - 1\right) \\ &= P_{out} \cdot \left(\frac{1-G}{G}\right) \end{aligned} \tag{3.22}$$

From this equation the L shaped topology is equal to the Wolaver limit and thus a "fundamental limit topology".

Another way to visualize the topology processed power is the VA Area modelling discussed in Chapter 2.3. The VA Area model of the buck converter is visualized in Fig. 3.13. The areas for the output and input powers are marked A1 and A2. The shaded area where the two overlap represents the direct power $\left(P_{out} \cdot \frac{1}{G}\right)$. The non-overlapping areas represent the power processed by each component also referred to as "indirect power".



Input Power:

$$V_{in} \cdot I_{in} = P_{in}$$

Overlap: Direct Power:

$$V_{out} \cdot I_{in} = P_{dir} = P_{out}\left(\frac{1}{G}\right)$$

Non- Overlap: Indirect Power:

$$(V_{in}-V_{out}) \cdot I_{in} = A1$$
$$V_{out} \cdot (I_{out}-I_{in}) = A2$$

Total Output Power:

$$V_{out} \cdot I_{out} = P_{out}$$

Fig. 3.13 VA Area of L shaped topology (Buck)

From the diagram, it can be noted that increasing the voltage dropper $(V_{in} - V_{out})$ or the parallel current source $(I_{out} - I_{in})$ will result in bigger areas for A1 and A2. Thus, more power handled by the converter. This is the case for non-fundamental converters such as the T and Pi shape, due to an additional voltage dropper and current source branch respectively.

Note that the VA Areas of the Pi and T topologies are not provided due to the limitation of the VA Area modelling tool in visualising converters with a single switch and diode. One can intuitively see how these two will result in bigger A1 and A2 areas in comparison to the L-shaped VA Area model in Fig. 3.13. It will be difficult to interpret the transfer of powers for more than two switches and diodes. The topologies will be compared using numerical examples and later a comparative analysis and discussion of high gain converters with an example of a T and a Pi is provided in this section.

3.5.3 Inverted "L" Shape: Minimum Step-Up Topology

We have seen how the L shape represents the minimum standard topology for the voltage step-down function. With that in mind, one can also see how the inverted L shape (in Fig. 3.14), which consists of a voltage adder and a "current sink" is the minimum topology for the voltage step-up function. Thus, the boost converter which is the reverse of the buck, when the input and output are swapped, is at the fundamental limit, thus $P_{DC\,(boost)} = P_{out}\left(\frac{1/G-1}{1/G}\right) = P_{out}(1-G)$. The VA Area model will be like that of the buck in Fig. 3.14, with the Input and output VA areas swapped.

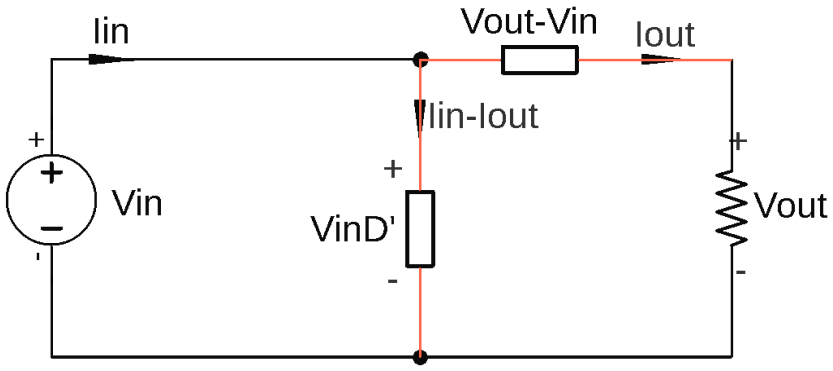


Fig. 3.14 Inverted "L" shaped topology, fundamental topology for voltage step-up

3.5.4 Comparison of Standard Topologies

Adding any other series or parallel element to the L shaped topology leads to the other topologies, such as the T or pi or so on. Due to additional components the converter handles more power, for the same gain compared to a buck converter. This can be illustrated with a numerical example with a 50% conversion ratio from 12V to 6V, rated at an input/output power of 12W assumed to be lossless. The numerical examples are given in Fig. 3.15 below for all the standard topologies given in Fig. 3.10.

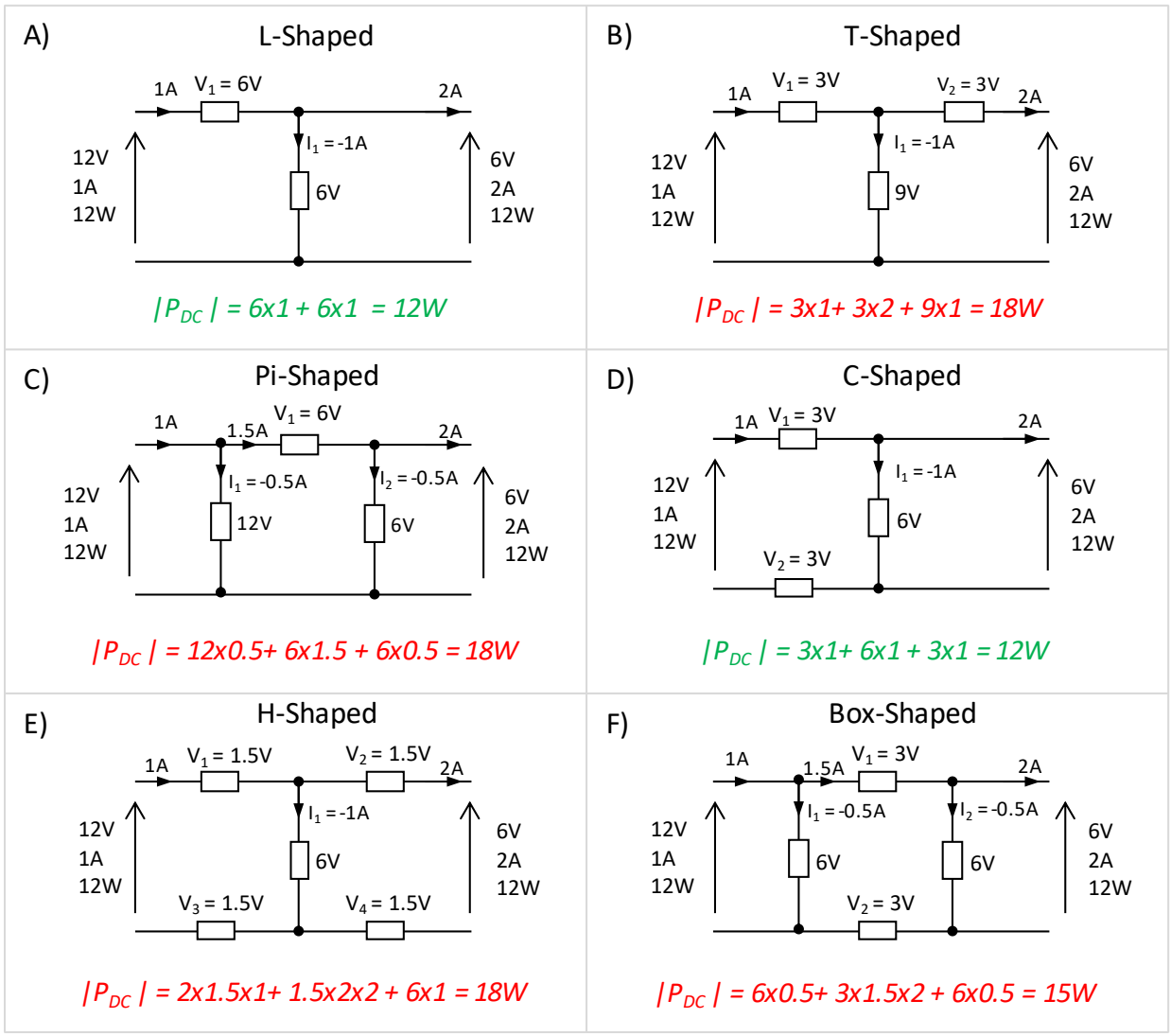


Fig. 3.15 Six Standard topologies processed power comparison at 50% gain

L-Shaped Topology: $|P_{DC}| = P_{out}$ ***(12W)***

Fig. 3.15 A) shows the L shaped topology, and as expected the power processed by the switch or diode alone is 50% of the output power. Note that the Wolaver limit is based on either one of the two. For this analysis the absolute value of the two are added and equate to the output power in the case of the L shape.

T-Shaped Topology: $|P_{DC}| > P_{out}$ ***(12W)***

For the T shaped topology in Fig. 3.15 B), the average model consists of two series voltage dropper elements (V_1 *and* V_2) and a single parallel current source (I_1). An example of a converter with a T-shaped average model is shown in Fig. 3.16. The circuit analysis and

average modelling is given in Appendix B.3. This converter processes more power than a buck converter at any given conversion ratio.

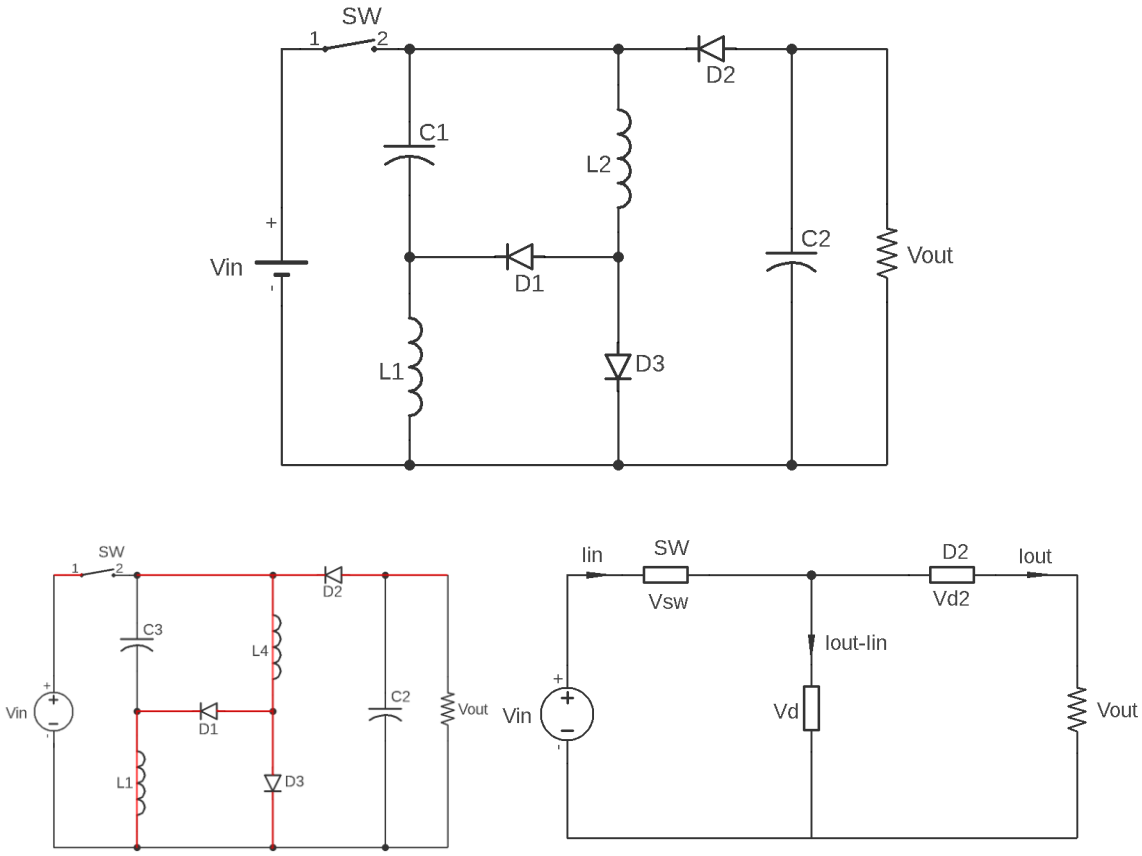


Fig. 3.16 Example of Converter Circuit with T-shaped topology

For the same input/output power and gain as an L shaped topology, the first element V1 has less voltage but handles all the input current like the L shape. The second voltage dropper (V_2) handles the output current (i_{out}), which is greater than the input current handled by (V_1) of an L-shaped topology. Thus overall, the T shape handles more power to achieve the same gain as an L shaped topology.

The reader will note that the T shape approaches an L shaped topology as the voltage dropper (V_2) approaches zero. The same observation can be made with the pi shape.

Pi-Shaped Topology: $|P_{DC}| > P_{out}$

An example of a pi shaped topology is the hybrid switched capacitor converter in Fig. 3.17 [42]. From the numerical example in Fig. 3.15 C), the Pi shaped topology as expected processes more power the output power. This is due to the additional current source (I_2) which causes the topology to process more power for the same gain as an L shaped topology.

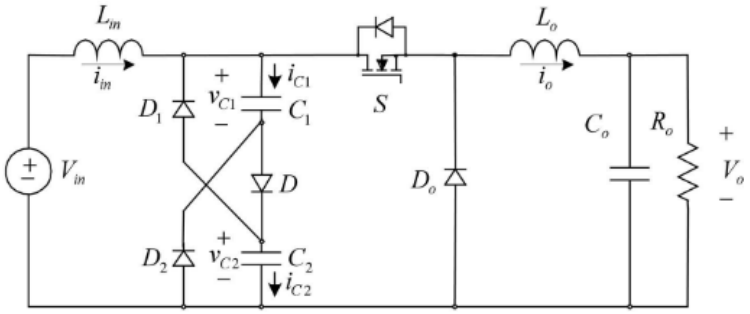


Fig. 3.17 Hybrid switched Capacitor [50]

C-Shaped Topology: $|P_{DC}| = P_{out}$

The C-shaped topology processes equal power within the converter as the output power and thus at a fundamental limit topology like the L-shaped. This is because the C-shaped "second" voltage dropper (V_2) is in series with (V_1). The two voltage droppers thus have the same current (i_{in}) flowing through them. So, the C-shape is topological the same as the L-shape topology.

H-Shaped Topology: $|P_{DC}| > P_{out}$

In the same way, the H-shaped converter is topologically equivalent to the T-shaped topology. Two pairs of the voltage droppers labelled V_3 & V_1 and V_4 & V_2 are in series resulting in a T-shaped topology.

Box-Shaped Topology: $|P_{DC}| > P_{out}$

Finally, the results for a Box-shaped topology in Fig. 3.15 F) show that it processes more power than the limit. However, it processes less power compared to the T and Pi.

The next section brings in duty cycle to the comparison of topologies. Note that the L-shaped topology is at the fundamental limit and thus the best topology in terms of processed power. However, as it will be shown, it does not necessarily mean it outperforms in all other metrics.

3.6 Averaged Model of a Fully Indirect Power Converter

We revisit the example of a buck-boost converter given in Fig. 2.12. The buck-boost average equivalent circuit and numerical example are shown in Fig. 3.18(a) and (b) with two separate current loops, for the input and output. This is consistent with its VA Area model determined in Fig. 2.13 with two non-overlapping VA areas. The average switch and diode powers reveal that each component processes 100% of the input power. This means the converter fully transfers power indirectly to the output. This results in a split shaped averaged topology model shown in Fig. 3.18(c).

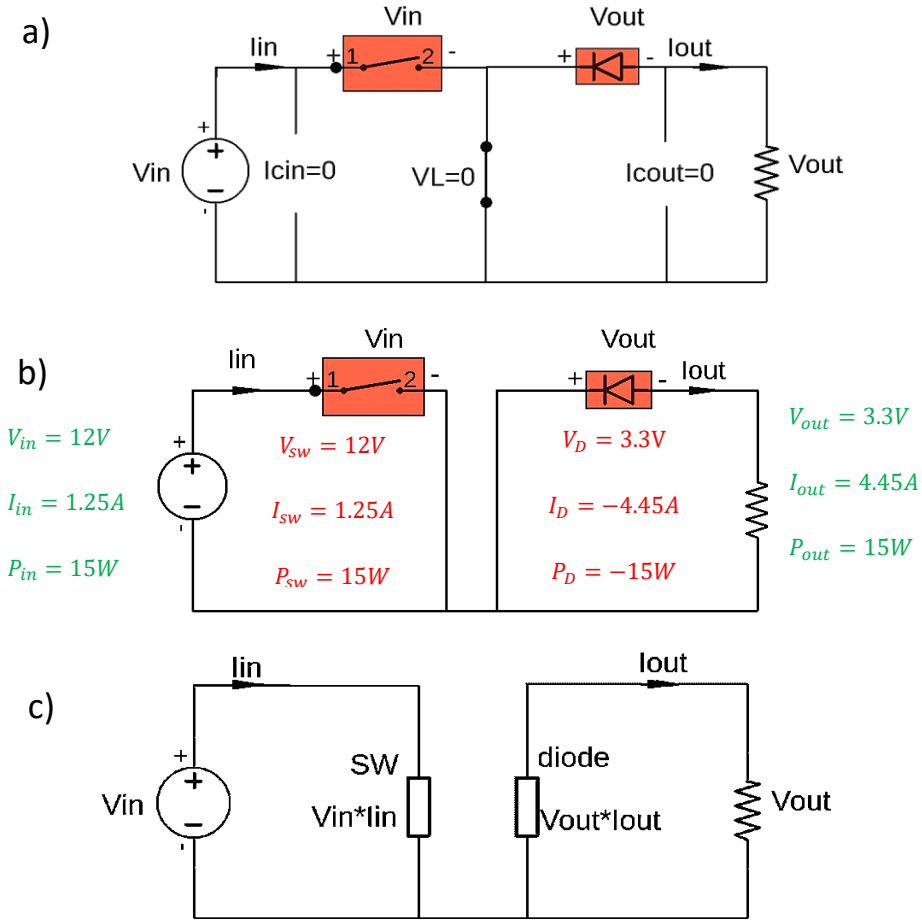


Fig. 3.18 Buck-Boost, a) Average equivalent, b) Numerical example, and c) "U-shaped" averaged model

The split is due to the inductor in the buck-boost converter being in parallel with the input. This result is not limited to the buck-boost but may be true for any converter with a similar circuit, i.e. inductor in parallel to the input. In addition, a converter with a capacitor in series with the output may also result in a split average topology model. The split equally means

that the reactive components, inductor, or capacitor, also process 100% of the input power, like the switches. This will be clearly visible when looking at the processed power of the buck-boost converter in Chapter 5 compared to other converters.

3.7 Duty Cycle and Switch Processed Power

The minimum or fundamental limit referred to thus far by the Wolaver limit is specific to the amount of processed power and should be interpreted as such. Thus, the L shape is optimised when looking at the amount of power processed within the topology.

This section goes deeper to differentiate converters by introducing the duty cycle. Two things are highlighted in this section; first the performance of converters at the fundamental limit are distinguished. Fundamental limit topologies have the same processed power but can have vastly different performance, when duty cycle is introduced into the analysis. This analysis is important because there are multiple converters at the limit but with different performance. Secondly it reveals some benefits of non-fundamental limit topologies, particularly for high voltage and high current gain applications.

The major limitation of the average topology comparison is that it hides the operational performance of topologies. Because of the nature of the average transformation, it is unable to provide time-based performance characteristics, based on duty cycle, and reactive components. This means there will be topologies that have the same fundamental limit in terms of processed power but have different performance. The reactive components will be considered in a separate chapter to further distinguish converters.

3.7.1 Duty Cycle and VA Rating

The duty cycle provides insight on the VA rating of the switches and diodes. The duty cycle (D) in the average power formulation shown in equation (3.1) provides a glimpse into the VA rating specifications of the switches. This concept is described in the VA Rating Section 2.4. A discussion is provided in this section for ease of reference. The processed power of a switch or diode is defined as shown below in equation (3.23), as the product of the average voltage and average current.

$$P_{DC} = V_{Avg} \cdot I_{Avg}$$
$$P_{DC} = (V_{on} \cdot D + V_{off} \cdot (1 - D)) \times (\mathrm{I}_{on} \cdot D + \mathrm{I}_{off} \cdot (1 - D)) \quad (3.23)$$

The VA rating is defined as the product of the maximum blocking voltage (V_{off}) and maximum possible current (i_{on}) handled by a component. This can be seen with an example of a switch in a buck converter in equation (3.24).

$$P_{DC(SW)} = V_{off}(1 - D) \cdot I_{on} D$$
$$P_{DC(SW)} = \underbrace{(\boldsymbol{V_{off}} \cdot \boldsymbol{I_{on}})}_{\text{VA Rating}} \cdot (1 - D) \cdot D \quad (3.24)$$

From the equation (3.25) below it is clear that the VA rating is a function of duty cycle.

$$VA_{SW} = P_{DC(SW)} \cdot \frac{1}{(1 - D) \cdot D} \quad (3.25)$$

A duty cycle D exists where the VA rating is the lowest. Remember from Section 2.42.4 that a converter with the lowest VA rating is desirable since it provides the best switch utilization. According to equation (3.25), this point (lowest VA rating) is when the duty cycle is equal to 50%, i.e. $D = 0.5$, for a buck converter. Thus, operation at a different duty cycle will result in switches with a higher VA rating. For an example operation at 20% duty cycle for a buck will result in a VA rating over 11 times the switch DC power as shown in equation (3.26) below.

$$VA_{SW} \text{ @ } 10\% \; duty \; cycle = \frac{1}{(0.2 - 0.2^2)} P_{DC(SW)}$$
$$\cong 6 \times P_{DC(SW)} \quad (3.26)$$

The above example considers the VA rating of the switch only, the total VA Rating is defined as a sum of VA ratings for all switches and diodes in the converter. The next section compares the VA rating of topologies at the fundamental limit.

3.8 Application of Averaged Topology Modelling

This section can be summarized with these two processes.

Firstly, any converter topology can be assessed using the averaged topology modelling procedure. The procedure yields a core structure of the converter circuit, for comparison to any other topology, complex or simple. The average model provides information on the amount of power processed by the topology. L shaped topologies have been proven to be fundamental limit topologies based on power processed.

Secondly, the converter circuits can be compared by introducing the duty cycle which reveals the VA ratings of the converter switches. VA rating provides a physical and practical metric for comparing converters.

Using this procedure any converter topology can be assessed. An example is taken from the converter topology comparison in [42]. The hybrid switched capacitor (in Fig. 3.17) and switched inductor (in Fig. 2.17) converters are compared to the quadratic converter shown in Fig. 3.19. The application considered in the paper is high voltage-conversion which would require the basic converters to operate at extreme duty cycles less than 0.1. Reduced reactive energy and similar voltage stresses were reported in [42] when comparing the hybrid switched inductor and hybrid switched capacitor to the quadratic converter.

The results from the paper are compared to the output of the assessment procedure presented in this chapter. For this section, consistency in terms of the voltage stresses is considered, the reactive components are covered in the next chapter. The hybrid converters have the same gain $G = \frac{D}{2-D}$ whilst the quadratic converter has a gain $G = D^2$. The quadratic converter is a cascade of a buck and buck-boost converter.

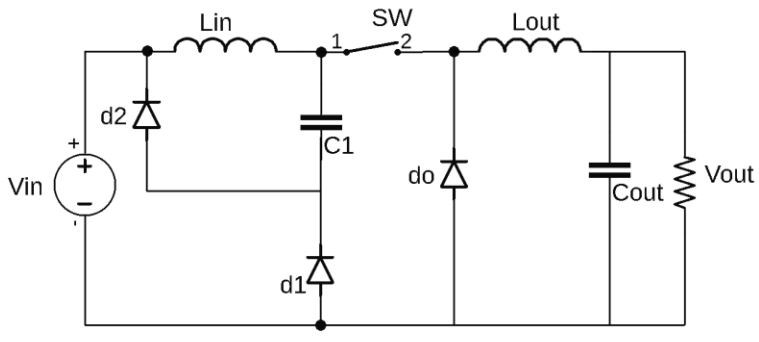


Fig. 3.19 Quadratic converter

Applying the average modelling procedure in Fig. 3.1 to the converters results in the average topology models in Table 3.2. The quadratic buck and the hybrid switched capacitor both have pi shaped topologies and the hybrid switched inductor has an L shaped core structure. This tells us that the hybrid switched inductor is at the fundamental limit in terms of processed power, thus processes the least amount of power compared to its counterparts.

To compare the voltage stresses amongst the converters, the VA ratings of the converters at a duty cycle of 0.25 are provided in Table 3.2. From the table and the VA rating plots against gain in Fig. 3.20, the rating of the quadratic converter is the highest at lower gains. This is consistent with [41], where a double quadratic converter is recommended over the traditional quadratic in order to reduce voltage stresses by half. The VA ratings of the hybrids are lower than the buck for higher gains, making them suitable for high conversion gains

Table 3.2 Comparison of Hybrid Switched converters with Quadratic Converter

Topology	Gain	Average Model
Hybrid Switched Inductor	$\frac{D}{2-D}$	L-Shaped
Hybrid Switched Capacitor	$\frac{D}{2-D}$	Pi-Shaped
Quadratic	D^2	Pi-Shaped

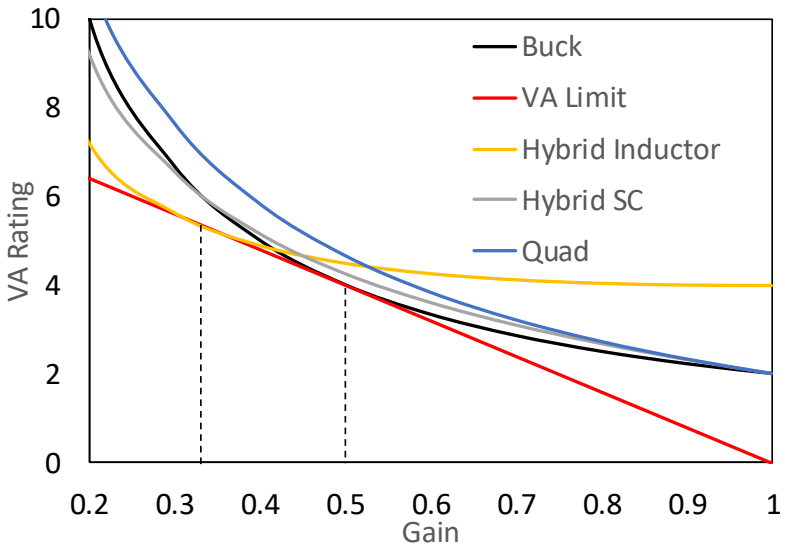


Fig. 3.20 VA Rating of Hybrid Converters vs Quadratic converter

3.9 Discussion and Summary

An averaging modelling procedure was proposed as a tool for reducing any converter to its core structure. The averaged topology model was shown to place different types of DC-DC topologies in equal footing for ease of comparison. The modelling procedure was validated by proving that it meets circuit theory and consequently conversation of energy. The results obtained provides confidence of the average modelling tool for high-level converter comparison. Relation of the average topology model to the Wolaver performance limit further provided evidence of its utility.

From this relation a crucial finding in this chapter is the proof of fundamental limit topologies. The L shaped and the inverted L shape standard topology resulting from a buck and boost converter are examples of fundamental limit topologies for step-down and step-up respectively.

The average modelling tool was applied to a hybrid switched inductor, hybrid switched capacitor, and quadratic converter resulting in an L-shaped, and two pi shaped models respectively. The hybrid switched inductor was shown to be at the fundamental limit like the buck. The performance of converters at the fundamental limit were demonstrated to be indistinguishable using the average topology model.

Since the average model is invariant to operational conditions such as duty cycle, the VA Rating was shown to be a further step to distinguish performance of converters at different duty cycles.

This section considered metrics focusing on the switches in the converter. From the switches, metrics such as VA rating and processed power were assessed. The next section looks at metrics considering reactive components for providing further insight to converter performance.

Chapter 4 Proposed RMS and Variance Metric (Reactive)

4.1 Introduction

This chapter highlights and addresses three limitations observed in the absolute value definition of the processed power metric. This definition hides power transfer information, and makes the metric invariant to performance differences at varying duty cycles. An enhancement of the processed power analysis using circuit analysis that preserves power transfer polarity and balance between reactive components is presented. Finally, a variance and root mean square based definition is shown to distinguish performance between converters operating at different duty cycles.

The chapter is arranged as follows, Section 4.2 outlines the major gaps identified to enhance the utility and generality of the processed power metric. Section 4.3 presents a holistic circuit analysis for determining reactive component processed power. The next section demonstrates the limitation of the absolute value definition followed by a proposal of an RMS based definition. Section 4.6 compares the two definitions at different duty cycle scenarios.

4.2 Average Absolute Value Definition of Processed Power

The definition of reactive component power from Wolaver applied by Cobos and Li is given in equation (4.1) below [20], [23]. Based on the equation this study refers to this definition as an average absolute value of power.

$$P_{reactive} = \frac{1}{2}\frac{1}{T}\int_0^T |\mathrm{v}(t)\cdot \mathrm{i}(t)|\cdot d(t) \tag{4.1}$$

This is a powerful metric for assessing topologies as discussed in chapter 2. From this definition the Wolaver limit emanates, which has recently started gaining acceptance in literature as a fundamental performance limit for converters[15], [18], [23], [24], [31], [45], [51]. Thus, the work in this section is not to take away from its definition, but to enhance its utility. The following gaps have been identified towards generality of the metric:

- The absolute value hides critical power transfer or flow information, which tells us whether power is absorbed or delivered. The metric can be applied without the absolute value, by purely applying circuit analysis. Preserving the sign of the power provides a better visualisation of the processed power in a converter. This is demonstrated with an example in Section 4.3.
- The exclusion of the reactive processed power of the source, which can be modelled as an input capacitor, hides the balance of the component powers. Inclusion of the source reactive component will be illustrated with an example of a buck converter in a comparative analysis in the next section. This has potential to double the fundamental limit, however, it does not take away from its interpretation.
- The average absolute value definition of power hides the performance differences expected at different duty cycles, particularly at extremes. Thus, a statistical based definition of the processed power is proposed.

4.3 Reactive Processed Power from Fundamental Circuit Analysis

The Wolaver analysis presented in the previous section can be used to assess the internal operations of any converter and assess how close it achieves the minimum required processed power. This section does the same using circuit analysis.

The conventional buck converter will be analysed over a sweep of gains from high step down($Gain \cong 0$) to low ($Gain \cong 1$).

The analysis is valid for any circuit in but for illustration a simplified version of the buck is used, with an assumption of zero-ripple; zero-loss; and operation in continuous conduction mode. Under these assumptions the best possible performance of the topologies analyses is expected. Inclusion of losses, ripple and operation in discontinuous conduction mode is expected to reduce performance. The buck converter circuit is shown in Fig. 4.1. with an input capacitor (C_{in}) included.

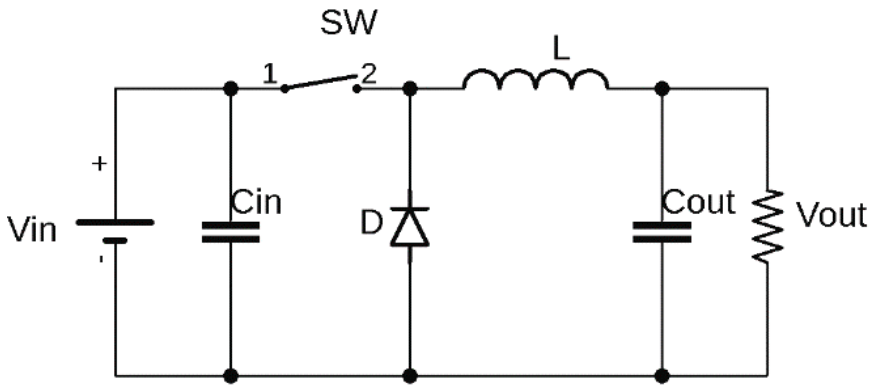


Fig. 4.1 Buck converter topology with input capacitor (Cin)

The input capacitor is included as the buck converter has a fluctuating input current and the capacitor will be used to carry the fluctuation current. The voltage source V_{Cin} carries the fluctuating power and will have a zero average over one switching cycle. Splitting the input and output sources in this way is useful as it allows the power processed by the source to be split apart from the average power delivered by the source. This modelling shown in Fig. 4.2 is in line with the Fryze theory covered in detail in Appendix C.1. The authors in [30] and [36] show that the reactive contribution from the source is vital to describe all the power processed by the converter.

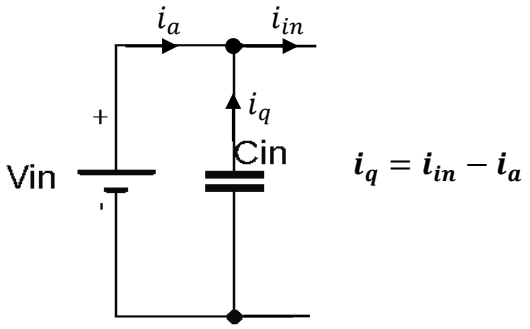


Fig. 4.2 Voltage source equivalent capacitor circuit

Thus, the circuit in Fig. 4.1 with the input capacitor is redrawn in Fig. 4.3 showing zero ripple modelling. In the Figure, the capacitors (C_{in}, C_{out}) have been replaced with voltage source(s) with the average value of the respective capacitor voltage. The inductor (L) is replaced with a current source with the average value of the current in the inductor. The converter's input and output are modelled as two voltage sources in parallel. The load resistor has been replaced by a voltage source at the output voltage. Since there are two parallel sourcesV_{cout} and V_{out}) with the same voltages, it is not possible to do normal circuit analysis

to determine the current. As a result, the split of current is done artificially as described previously.

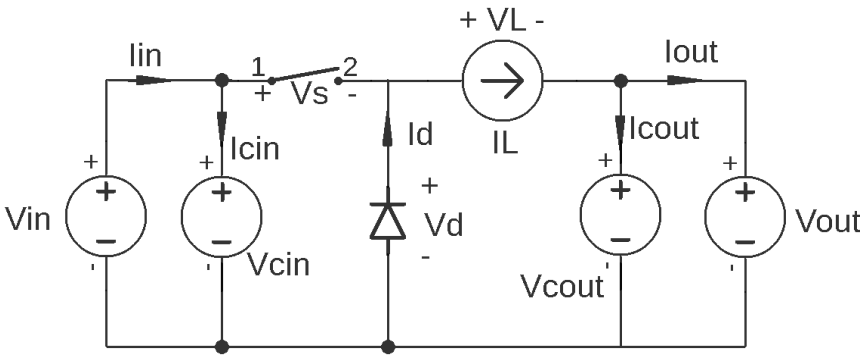


Fig. 4.3 Buck Converter Topology zero ripple modelling, with input Capacitor

Under the assumption of zero ripple, the voltages and currents have constant values during the on and off times of the switch as shown in Fig. 4.4.

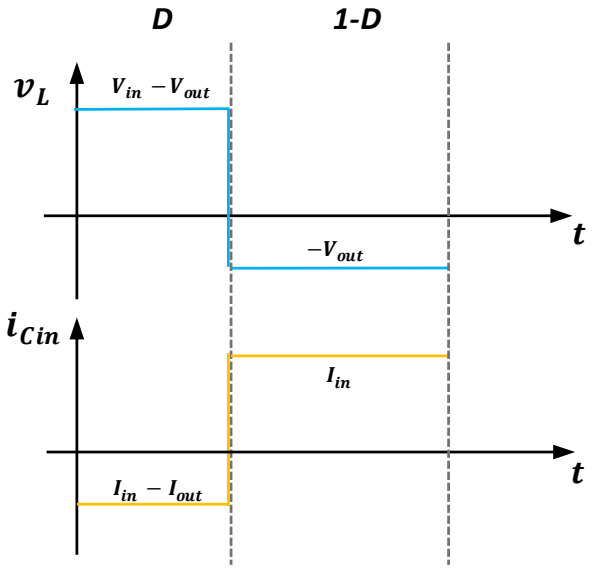


Fig. 4.4 Buck Inductor Voltage and Input Capacitor Current

During the "on" time of the switch, the inductor absorbs energy. The inductor then delivers energy during the "off" time. With these two simplifications, the processed power equation in (4.1) can be written as equation (4.2).

$$P_{component} = D \cdot (V_{onsate} \cdot I_{onstate}) \tag{4.2}$$

where $V_{onstate}$ and $I_{onstate}$ are the reactive component voltages and currents during the on-state of the switch, and D is the duty cycle.

In Fig. 4.3 circuit diagram, $V_{in}I_{in}$ is the constant input power which equals the constant output power $V_{out}I_{out}$. The voltage source equivalent capacitance, carries the fluctuating power and will have a zero average over one switching cycle. Splitting the input and output sources in this way, is useful as it allows the power processed by the source to be split apart from the average power delivered by the source. In [36], the importance of considering the reactive contribution of the source for holistic converter analysis is highlighted.

Under zero ripple conditions the output capacitor does not carry any current and its contribution to the processed power will be zero. The only reactive components remaining are the input capacitor represented by the source V_{Cin} and the inductor represented by the current source I_L. The waveforms of these components are shown in Fig. 4.5. Due to volt-second balance and charge balance discussed earlier on that for the inductor and input capacitor, their absorbing(A1) and delivering areas (A2) are equal. As proven earlier on due.

Applying equation (4.2) to the waveform in Fig. 4.5, the processed powers of the input capacitor and inductor can be found as:

$$P_L = D \cdot I_{out} \cdot (V_{in} - V_{out}) = V_{in} \cdot I_{in} \cdot (1 - D) \tag{4.3}$$

$$P_{Cin} = D \cdot V_{in} \cdot (I_{in} - I_{out}) = -V_{in} \cdot I_{in} \cdot (1 - D) \tag{4.4}$$

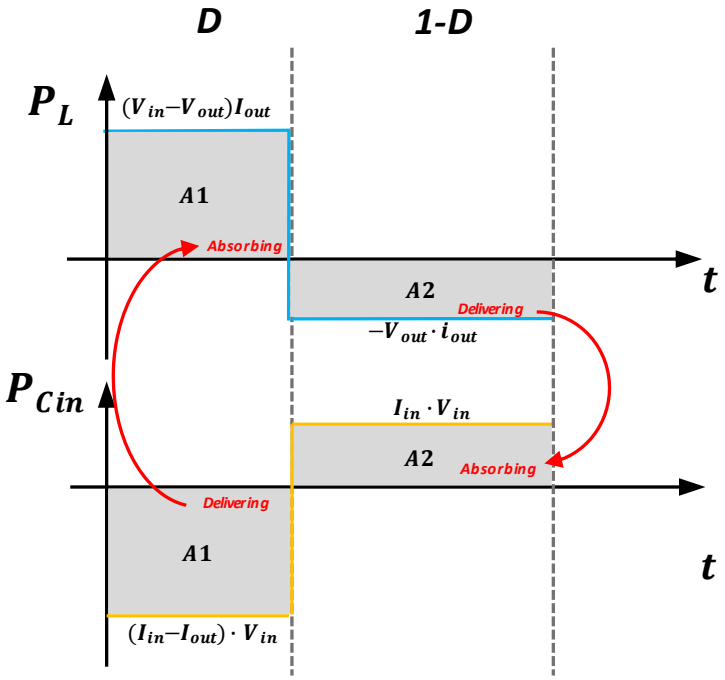


Fig. 4.5 Buck converter Inductor and Input Capacitor power, red arrow shows transfer

The processed powers of the different components determined in this way will always add to zero no matter the topology of the converter. This means the power delivered by the capacitor, labelled "*A1*" in the waveform, is absorbed by the inductor, ***"A1"*** in the first phase. The opposite is true in the second phase ("*1-D*"). The original definition of the processed powers includes the absolute value operator which hides this balance. For this reason, the definition of the processed power has been modified and is valid.

Taking the absolute value and half of equations and results in the processed power according to equation 1.1. The two are normalized with input power $V_{in}I_{in}$ and plotted as a function of the converter gain V_{out}/V_{in}, which for the buck converter is equal to the duty cycle D. This is shown in Fig 4.5 along with the Wolaver limit showing the minimum amount of processed power required. Equations and are also plotted with the polarity kept and shown in Fig. 4.7.

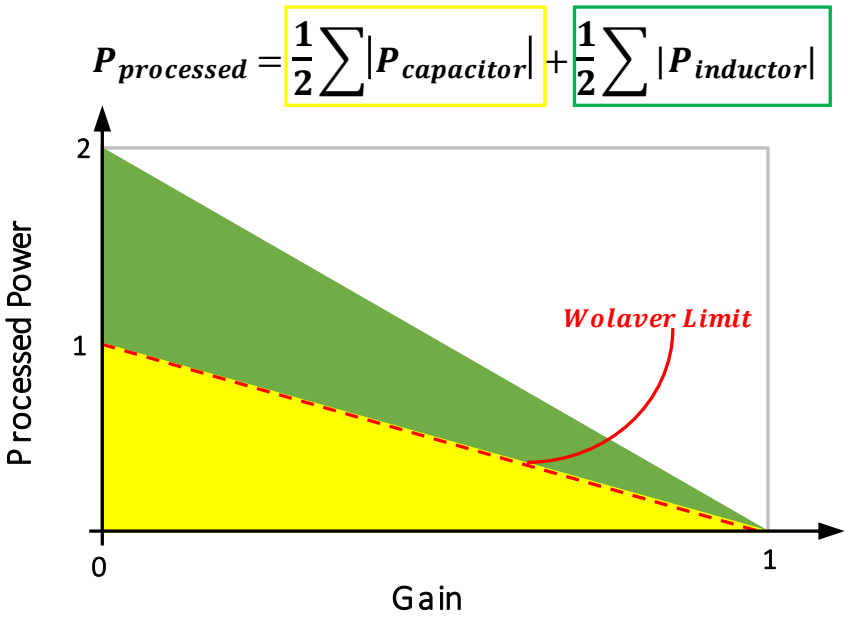


Fig. 4.6 Buck Processed Power using Absolute Value vs Gain

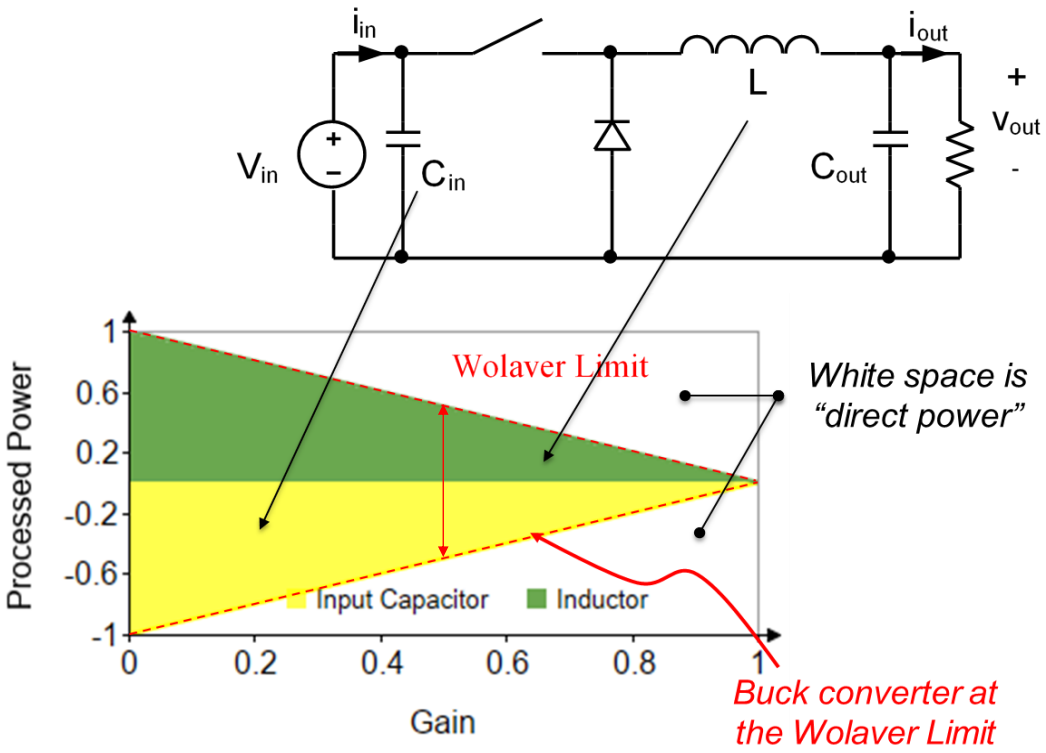


Fig. 4.7 Buck converter processed power

Both plots show the amount of input power processed through storage by the inductor at different gains as the green area. This power is stored in the inductor and is equally exchanged with the capacitor shown by the yellow area. So, the shaded areas show the processed power bouncing or slouching between the input and output. This power is reactive and manifests in terms of volume of these two components. The rest of the white space in both figures can be considered as direct power. Thus at 0.5 gain, the capacitor and inductor processes 50% of the input power.

Both plots, Fig. 4.6 and Fig. 4.7, have the same data but the major difference is the degree of how well they visualise power transfer. Fig. 4.7 clearly shows the reactive component power exchanged and balance between the inductor and the input capacitor more than the absolute values plotted in Fig. 4.6. Note however that the visualisation of the power transfer is limited to only two switching states. Its complex to keep track of the power exchange for more than two states, this will be discussed later in 5.7.1.

The next section discusses a major difference observed when determining the process power through circuit analysis and as shown in Fig. 2.7.

4.3.1 Buck Converter at Double the Wolaver Limit

The difference observed with the plots in Fig. 4.6 and Fig. 4.7 compared to the Wolaver limit plot in Chapter 2, is that the buck converter must be at twice the Wolaver limit, because of inclusion of the input capacitor. The switches show the Wolaver limit but the reactive components show twice the limit. This is an example where the switches and reactive component processed powers differ.

When the input capacitor is included in the analysis, the buck converter must be at double the limit. This means the buck processes double the Wolaver limit. The analysis thus far in literature including Wolaver, neglected the input reactive power in the analysis and only considers the inductor processed power. This omission limits the power transfer interpretation, since the processed power by the inductor must be exchanged with another reactive component. Excluding the input capacitor in the analysis hides half of the processed power. Thus, from this and the results obtained, the buck converter reactive components are at double the Wolaver limit. This does not take away from Wolaver's work, but proposed as an enhancement of its interpretation.

4.4 Processed Power Definition Invariant to Ripple and Duty Cycle for Inductor

Ripple in a converter is important since it is related to converter size, cost, and losses. When the inductor has more ripple, it stores more energy at an instant. Secondly, high ripple means more current goes through the input and output capacitors to maintain a constant DC output. The reactive component power definition in equation (4.1) is shown in this Section to be invariant at different current ripples for the same buck example used in previous Sections.

Assume the buck converter is operating at 50% duty cycle with an inductor voltage waveform shown in Fig. 4.8.

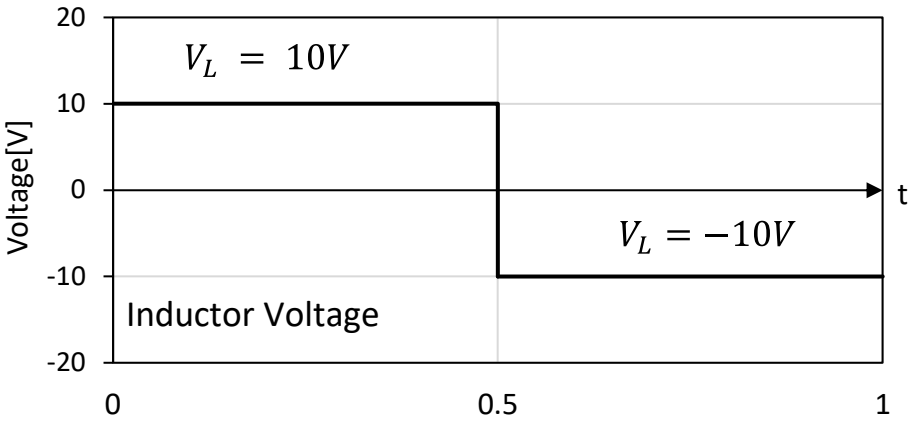


Fig. 4.8 Buck Inductor Voltage

The different current ripple scenarios are shown in Fig. 4.9.

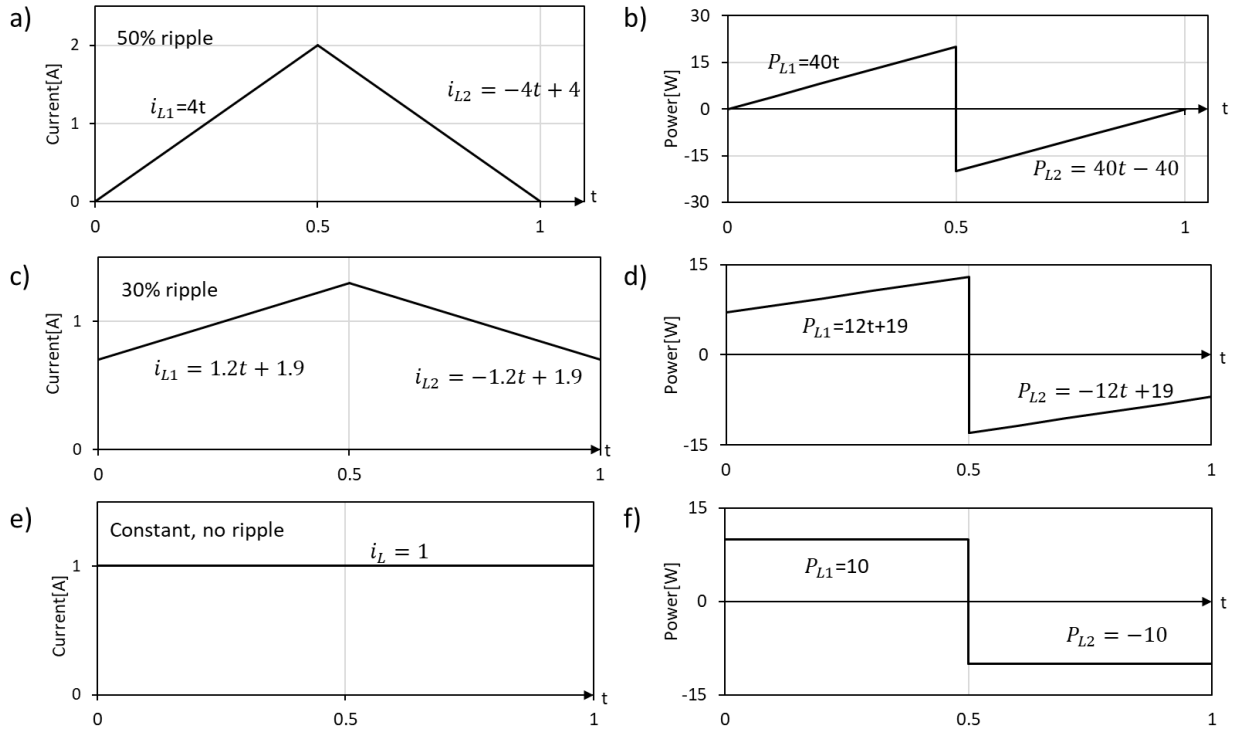


Fig. 4.9 Inductor current and power plots at ripple: a) - b) 50%; c)- d) 30%; and e)- f) no ripple

The choice of the different cases is to replicate the minimum to maximum current ripple scenarios in continuous conduction mode. The inductor current ripple and power waveforms for 50% ripple; 30% ripple and; DC constant current are shown in Fig. 4.9 a) to f) respectively.

All waveforms have the same average current value of 1A and power of 10W, with the voltage waveform in Fig. 4.8.

Using the definition of reactive component power in equation (4.1), the processed power for the inductor is calculated as shown in equations (4.5) to (4.7) below for the 30% , 50% ripple and zero ripple cases.

$$\mathrm{P_{processed}}(30\%) = \frac{10}{2} \cdot \left(\int_0^{0.5} |1.9 + 1.2t| dt + \int_{0.5}^{1} |1.9 - 1.2t| dt \right) = 5 \tag{4.5}$$

$$\mathrm{P_{processed}}(50\%) = \frac{10}{2} \cdot \left(\int_0^{0.5} |4t| dt + \int_{0.5}^{1} |-4\mathrm{t} + 4| dt \right) = 5 \tag{4.6}$$

$$\mathrm{P_{processed}}(\mathrm{zero-ripple}) = \frac{10}{2} \cdot \left(\int_0^{1} |1| dt \right) = 5 \tag{4.7}$$

For all scenarios the processed power as seen in equations (4.5) to (4.7) has the same result. The result means that the inductor processes 50% of the output power. This result is consistent with the plot in Fig. 4.7. However, this result is limited and may cause incorrect interpretation. If the three waveforms represented three different topologies, with different interconnections and components but same power output, this metric would not be able to distinguish them. This is because the Wolaver limit definition and processed power only depends on gain and output power.

Duty Cycle has the same effect

High ripple also occurs because of extreme duty cycles. Anything less than 0.2 can be considered extreme. This happens because at small duty cycles the reactive components have a short time to store energy, this manifests as high peak current or voltage. Thus, the exercise above can be done using different duty cycle scenarios as shown in Fig. 4.10. As a rule of thumb, operation at 50% duty cycle will provide the best performance for any converter. Because this provides the maximum time for reactive components to store energy.

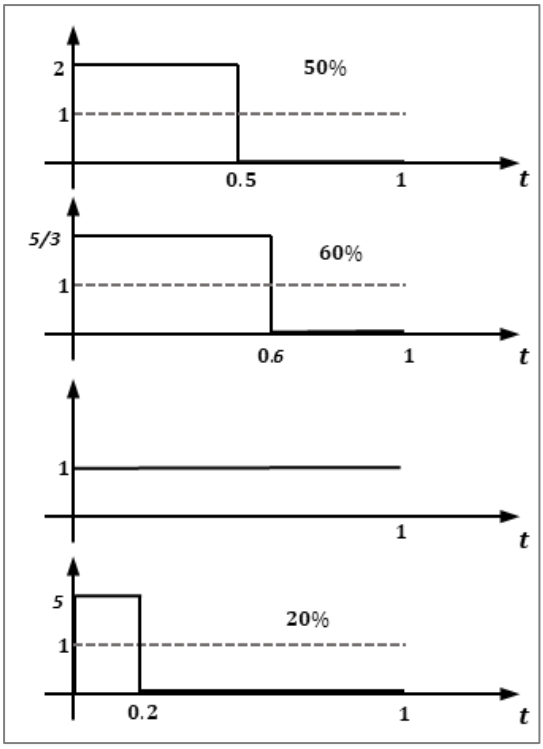


Fig. 4.10 Current plots at 50%, 60%, constant, and 20% duty cycle

The next section looks at a different definition of processed power which provides a metric that distinguishes performance of a converter at different ripple scenarios.

4.5 Variance and RMS Based Definition

The previous section showed the limitation of the processed power metric definition in differentiating reactive component power performance at different ripple percentages. Another definition is proposed in this section based on statistical variance, which is related to RMS.

Variance is simply a measure of how much a signal moves from its average. Mathematically there are two definitions of variance, one uses the root mean square and the other uses the average absolute value. Whilst both methods are valid, they have different results and interpretations. The RMS definition works well for quantifying the main variations in a waveform. This will be beneficial in capturing short duration peaks, i.e. ripple, in the converter waveforms. Whilst the average absolute approach is well suited for interpolation given

historical signal trends. The component power metric definition in equation (4.1) is similar to the average absolute value (AAV) definition of variance given in equation(4.8) below.

$$VAR_{AAV} = \frac{1}{T}\int |p(t)|\, dt \cong P_{reactive} \tag{4.8}$$

The definition of variance of power can be interpreted as the root mean square of the power and the DC power as shown in equation (4.9).

$$VAR(Power) = RMS^2 - DC^2 \tag{4.9}$$

The average DC power of a passive component over the full cycle of a converter topology is zero in steady state. This is to meet volt-second balance for the inductor and charge balance for capacitor. Thus, in steady state the power absorbed and released is equal. This leads to definition of the variance of power as the RMS of power, see equation (4.10).

$$VAR(Power) = RMS^2 = \frac{1}{T}\int \big(p(t)\big)^2\, dt \tag{4.10}$$

According to the Jensen inequality theorem covered in Appendix D:, the square root of the mean square of a signal is greater or equal to the mean absolute value of the signal, equation (4.11) below shows this mathematically.

$$\sqrt{\frac{1}{T}\int_0^T p^2\, dt} \geq \frac{1}{T}\int_0^T |p|\, dt \tag{4.11}$$

From this inequality it can be expected that the RMS based definition of component reactive power will be greater or equal to the average absolute value power, as shown in equation(4.12). The Jensen's inequality is intuitive since the "squaring" in the RMS will tend to amplify outliers compared to the average value.

$$Variance\ of\ Power(\ using\ RMS) \geq Processed\ Power \tag{4.12}$$

The RMS based definition of the reactive component power is given in equation (4.13).

$$\text{Reactive Component Power RMS } = \sqrt{\frac{1}{T}\int_0^T (v_i(t)\cdot i(t))^2 \cdot dt} \tag{4.13}$$

This definition is used in the next section for the ripple scenarios in the previous section.

4.6 RMS Metric Vs Processed Power Definition

Consider the ripple scenarios in Fig. 4.9 to assess the new RMS based metric. The definition in (4.13) is applied to the three cases as shown in equations (4.14) to (4.16) respectively.

$$RMS_{30\%} = 10 \cdot \sqrt{\int_0^{0.5} (1.9 + 1.2t)^2 \cdot dt \; + \int_{0.5}^{1} (1.9 - 1.2t)^2 \cdot dt} \; = 10.15 \tag{4.14}$$

$$RMS_{50\%} = \sqrt{\int_{0.5}^{1} (4\mathrm{t})^2 \cdot dt \; + \int_{0.5}^{1} (-4\mathrm{t} + 4)^2 \cdot dt} \; = 11.55 \tag{4.15}$$

$$\mathrm{RMS}_{zero-ripple} = 10 \cdot \sqrt{\left(\int_0^{1} (1)^2 dt \right)} = 10 \tag{4.16}$$

Table 4.1 summarizes the results for both metrics. The two metrics have a factor of 2 difference between them for the no ripple case. This is due to the 1/2 factor in the processed power definition, which is meant to account for only the delivered or released power. Thus, they are equal for the constant case if we take half of the RMS. The square root of the statistical variance in equation (4.9) correctly gives zero for the constant current case where RMS is equal to DC.

Table 4.1 Processed Power Metric vs RMS Metric at different current ripple scenarios

	RMS Metric	**Processed Power Metric**	$\sqrt{Statistical\ Variance}$ **(Equation (4.9))**
$\boldsymbol{P(i_1)\ 0\ \%}$	10	5	0
$\boldsymbol{P(i_2)30\%}$	10.15	5	0.15
$\boldsymbol{P(i_3)50\%}$	11.55	5	1.55

The inequality in the two metrics is clear when the current ripple is non-zero, in this case the RMS metric will be higher as seen in . This means the three topology scenarios, 30%, 50% and zero ripple shown in Fig. 4.9, process power differently. One converter has a higher peak power to process than the other. This also shows that the output and input capacitors will handle more power.

The next section shows that the RMS power also balances as we saw with the processed power, thus allowing similar graphical representation against gain.

4.7 Summary

To expand the utility of the Wolaver theory and processed power metric, this section highlighted and addressed three limitations of the metric for topology assessment.

Firstly, the metric's absolute value definition was shown to limit the interpretation and visualisation of power transfer within a converter. This was addressed by using fundamental circuit analysis to obtain the reactive component powers of a simplified buck. The reactive component powers were plotted based on their polarity or transfer direction, absorbing, or delivering. This formed a symmetrical plot from which power exchange and relation to the fundamental limit can be readily seen.

Secondly, the omission of the input capacitor in processed power analysis was mentioned as another gap identified which hides the holistic view of the power transfer mechanism within a DC-DC converter. This was addressed by splitting the input source into its fluctuating component and DC constant component. With this done a complete picture and interpretation of power exchange amongst reactive components was shown.

Thirdly the absolute value definition was shown to hide ripple and duty cycle effects in topology performance. An RMS based metric definition was proposed, from a statistical variance derivation. The new definition proved the ability to distinguish performance of a topology at different ripple cases. When applied to converters it revealed the high stresses at extreme duty cycles, in line with literature and other stress metrics such as the stress factors.

The next section will show a comparative analysis of all the metrics covered thus far including the proposed RMS metric from this section.

Chapter 5 Metrics Comparison Results

5.1 Introduction

This chapter aims to illustrate the utility of the metrics including the averaged topology model in assessing multiple converter topologies.

To illustrate the use of the metrics, four topologies including the buck converter will be compared to each other. The standard buck will be used as the baseline. The converters chosen for comparison are the conventional buck-boost in Fig. 5.1 (a), the basic switched inductor buck in (Fig. 5.1 b) and the switched inductor hybrid (Fig. 5.1 c). It is not immediately obvious as to which of the two switched inductor topologies will perform better or if indeed the standard buck will perform better.

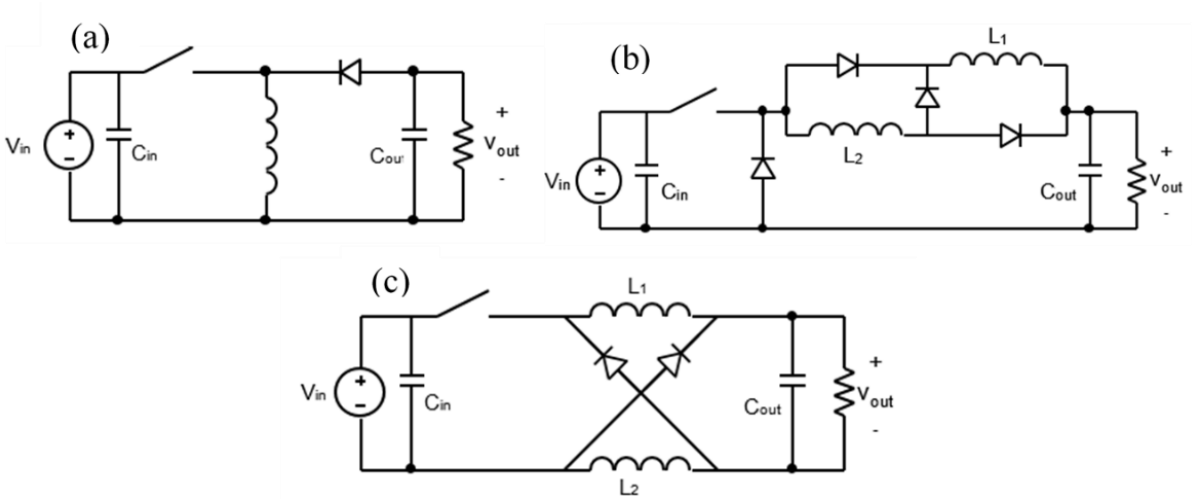


Fig. 5.1 (a) Buck Boost, (b) Switched Inductor, (c) Hybrid switched Inductor [52]

5.2 Average Topology Model

Applying the average topology modelling procedure outlined in chapter 3.3 to the converters in Fig. 5.1 yields the results tabulated in Table 5.1. The standard buck converter and hybrid switched inductor have an L-shaped core structure. This means both converters process the minimum power, and thus at the Wolaver limit. The Buck-Boost has a “U-shaped” topology or split topology as determined in chapter 3.6. It was observed that the buck-boost is a fully indirect power transfer converter, since the switches and reactive components

process the full input power, meaning no power is transferred directly to the output. The switched inductor converter circuit has a T-Shaped core structure. This means it's not at the Wolaver limit, but has a better core structure compared to the Buck-boost in terms of power processed.

Table 5.1 Comparison of Averaged topology models

Topology	Gain	Average Model
Standard Buck	D	L-Shaped *
Buck-Boost	$\frac{D}{1-D}$	U- Shaped "split"
Switched Inductor	$\frac{D}{2-D}$	T-Shaped
Hybrid Switched Inductor	$\frac{D}{2-D}$	L-Shaped*

*Minimum Limit topology

Using the averaged topology modelling procedure above is a quick and simple way to filter out unsuitable converters, and suitable converters to further consider for design.

5.3 Processed Power

The contribution of each of the converter's components to the processed power can easily be seen in Fig. 5.2 with the absolute value dropped as discussed in Section 4.3 . Along with the Wolaver limit shown as a red dotted line. For all three topologies the input and output capacitors contribute to the processed power and both capacitors are treated as voltage sources carrying the input and output current ripples respectively.

It is also clear that the hybrid switched inductor converter meets the Wolaver limit, while the switched inductor processes slightly more. The buck-boost always processes the total amount of power, that is 100% of the input power. It is also clear that for the switched inductor converters the input capacitors process much more power than the output capacitors.

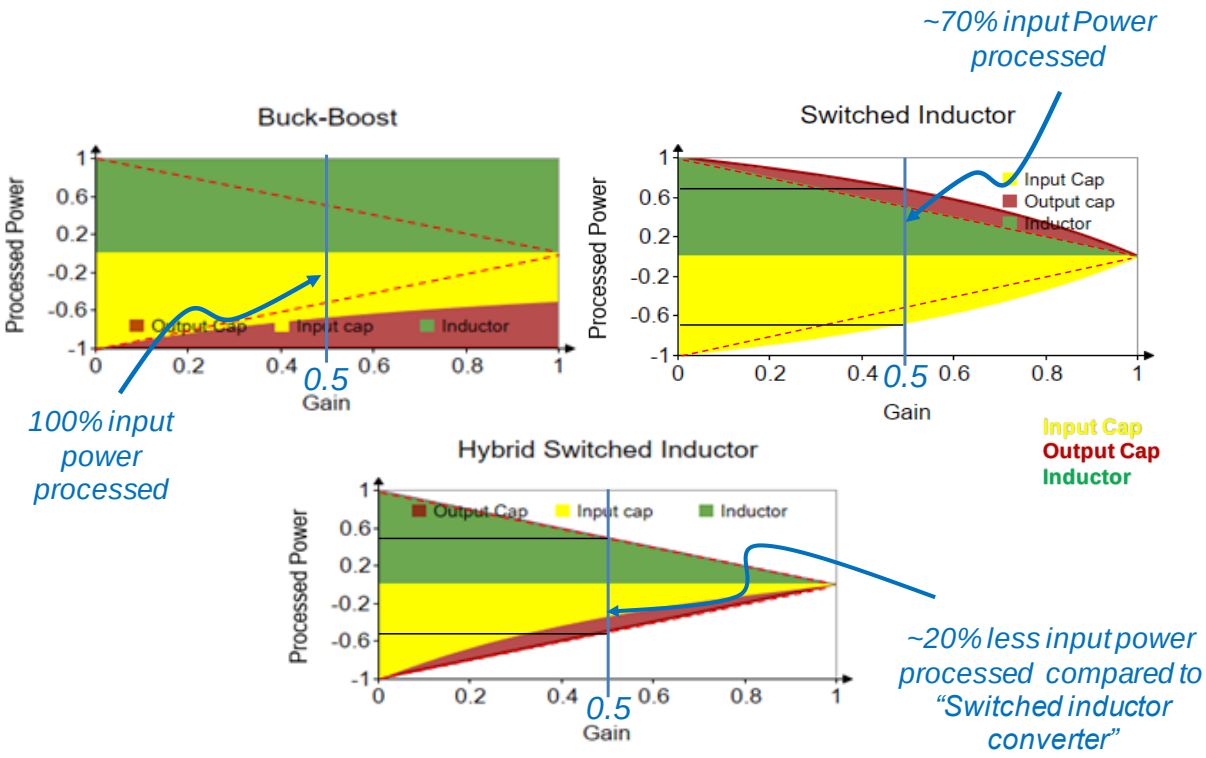


Fig. 5.2 Processed Power Plots, (a) Buck-Boost, (b) Switched Inductor, (c) Hybrid Switched Inductor

The utility of these plots is that they allow a quick visual comparison of the different converters with respect to the amount of power fluctuating inside the converter. At 50% duty cycle as an example, the switched inductor processes 70% of the input power whilst the hybrid converter processes about 20% less in comparison, similar to the buck converter shown in Fig. 4.7.

It is also easy to see if a converter is a minimum conversion topology or not. However, the problems due to extreme duty cycles are not visible using the absolute value definition of reactive processed power in (2.5) and in (4.1) by Wolaver.

5.4 VA Rating

The total VA ratings of the four converters with the fundamental VA limit are plotted against gain, V_{out}/V_{in}, in Fig. 5.3.

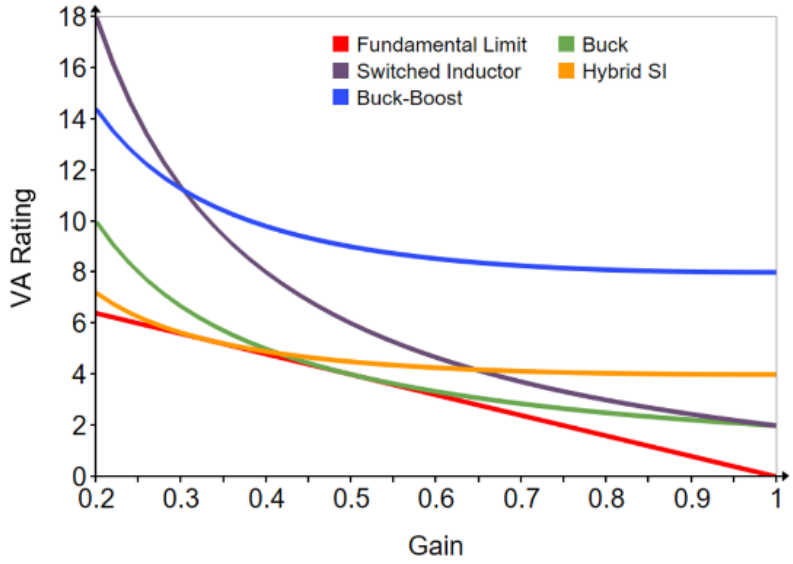


Fig. 5.3 VA Rating comparison of four topologies with VA Limit

The plots show the extent to which the topologies utilize the switches effectively. From the figure, the hybrid switched inductor utilizes the switches almost as well as the buck. Except at gains close to unity the basic switched inductor converter does not perform well. The buck-boost generally has the worst performance but outperforms the switched inductor for gains below 0.3. The two converters at the Wolaver limit, buck and hybrid, have the lowest and meet the fundamental VA Rating limit at gains of 0.5 and 0.33 respectively. At these gains the two topologies are have the best utilisation of switches.

5.5 Component Stress Factor

The inductor, capacitor, and semiconductor stress factors are plotted against gain in Fig. 5.4 a) to c) for the four converters. The stress factors quantify the amount of resources needed to implement the components, thus lower stress factors are desirable, since they translate directly to smaller volume, cost, and losses.

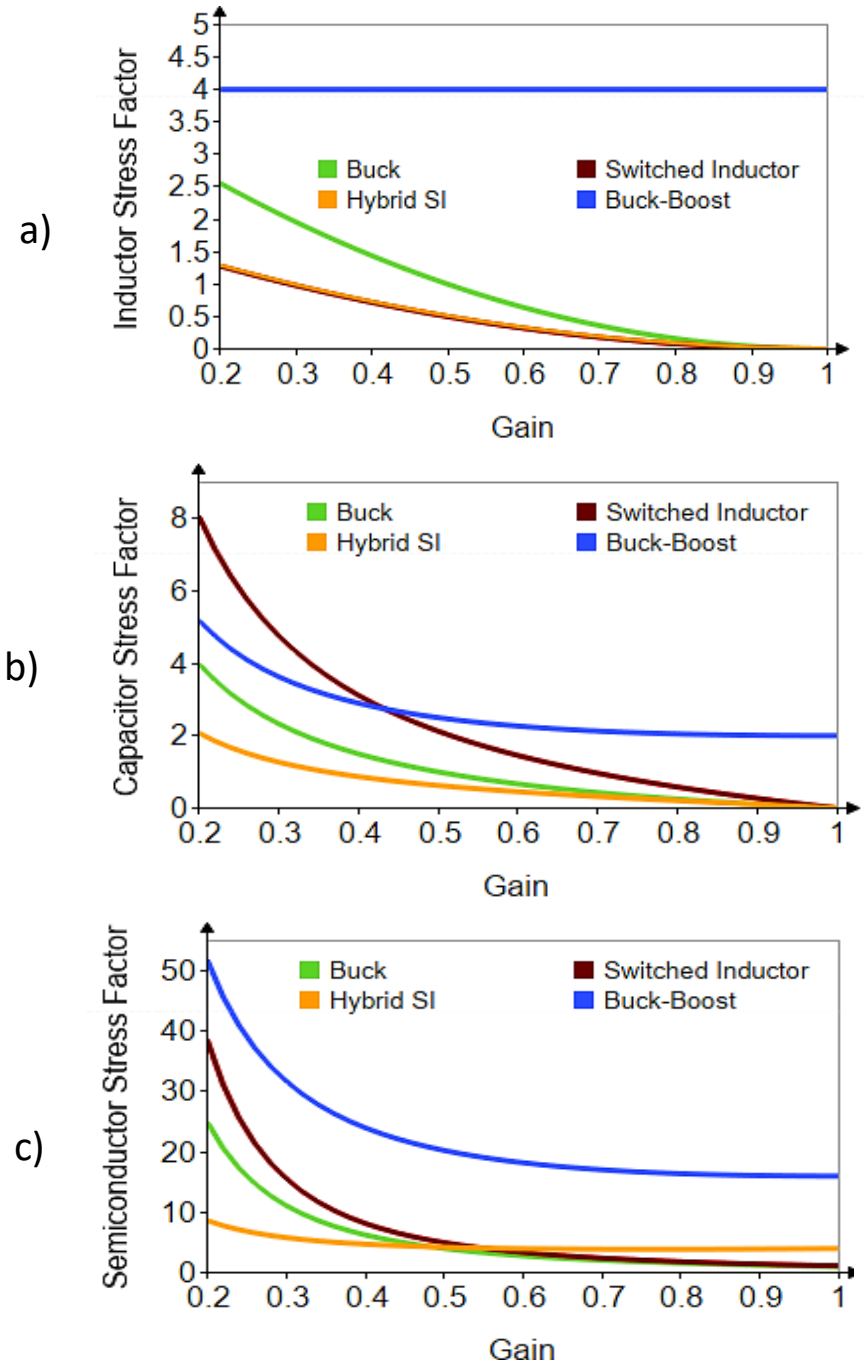


Fig. 5.4 Comparative stress factors: a) inductor, b) capacitor, and c) semiconductor stress factor for four topologies.

The semiconductor stress factor plots in Fig. 5.4 (c) are consistent with the switch VA ratings in Fig. 5.3. Again, the buck-boost has the worst performance at all gains.

The inductor stress factor is higher for the buck converter compared to the switched inductor topologies. This is due to the latter converters having two inductors with lower voltages and currents compared to the single buck inductor.

Looking at the capacitor stress factors the switched inductor has higher input and output capacitor stress factors than the hybrid and buck at all gains. This means selection of this converter requires higher rated, bigger volume and costlier capacitors.

The hybrid converter outperforms the standard buck for conversion ratios lower than 0.5, making it a suitable option according to the stress factors over the buck.

5.6 RMS Metric

The results of the RMS metric for the buck and hybrid topologies are given in Fig. 5.5. The RMS plot for the hybrid in Fig. 5.5 (b) is similar to the processed power plots in Fig. 4.7 and Fig. 5.2 (c) for the hybrid and buck respectively. The metric further captures the higher stresses on the inductor and capacitor at low gains due to ripple, previously captured by the stress factors in Fig. 5.4. Similar to the stress factors, the RMS metric paints the hybrid converter as a better topology compared to the buck. At 50% gain, the processed power metric shows the buck and hybrid with equivalent performance, but the RMS metric reveals that the Hybrid has 25% less variation in power compared to the buck.

This variation can be interpreted as how much the power varies from the average and thus relates to comparatively higher ripple and smaller duty cycle for the buck. This is intuitive because at gain of 0.5 the duty cycle of the hybrid is only 0.67.

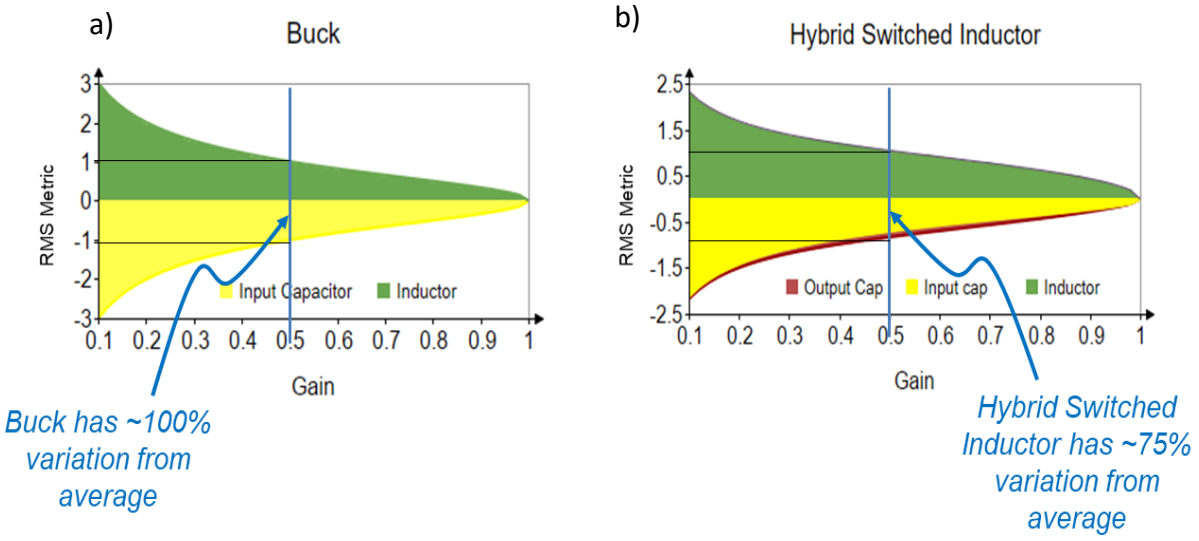


Fig. 5.5 RMS of power plots, a) Buck and b) Hybrid SI inductor and capacitor

The buck converter however has better performance for the switches at 50% duty cycle and this is visible when considering the total RMS performance. The total RMS power in Fig. 5.6 also provides similar curves to the semiconductor stress factor plots in Chapter 2. The RMS metric also paints the hybrid switched inductor in better light to the buck converter for gains below 0.5.

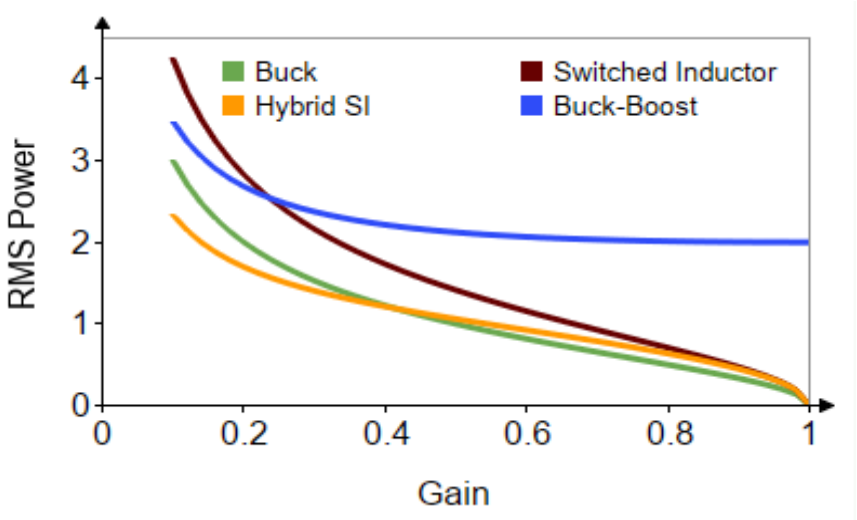


Fig. 5.6 Comparative RMS Power

5.6.1 The RMS Metric shows Balance

The RMS metric shows symmetry in the power absorbed and released by reactive components in Fig. 5.6, similar to the processed power using circuit analysis. This is an unexpected result due to the non-linear nature of the root mean square operation. The justification for this result is beyond the scope of this study. As a metric for converter comparison the RMS is proving to provide deeper insight more than the processed power.

5.7 Processed Power of Interleaved buck converter

This example demonstrates three things, Firstly, the utility of the metrics to a slightly more complex example. Secondly, it demonstrates different performance of converters with the same gain, and at the Wolaver limit. Lastly, it reveals the limitation in the power exchange within converters with more than two switching states.

Using the averaged topology modelling procedure, it can be show that any “n” phase interleaved buck converter has an L-shaped structure, and thus a fundamental limit topology like the buck and hybrid converter. The interleaved shows the best of all worlds, truly at the minimum limit at 50% gain.

The two-phase interleaved buck converter in Fig. 5.7 is a good example to illustrate the reactive performance differences between converters at the fundamental limit. The interleaved inductors alternate in providing current to the output, while the buck converter has a phase where current to the output is disconnected. This results in lower processed power handled by the input and output capacitors compared to the buck converter. The smaller current ripple on the inductor is due to “no dead” time where the output is disconnected from the output.

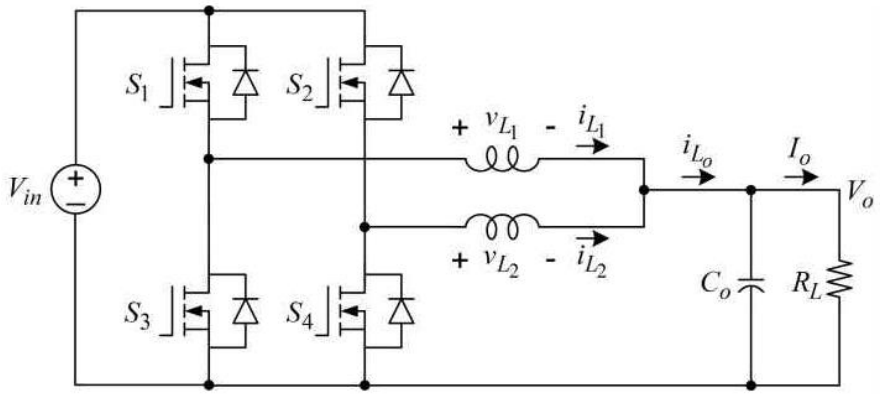


Fig. 5.7 Two phase Interleaved Buck Converter [53]

Using the same analysis in Section 4.3, the processed power for the interleaved buck is shown in Fig. 5.8 against gain.

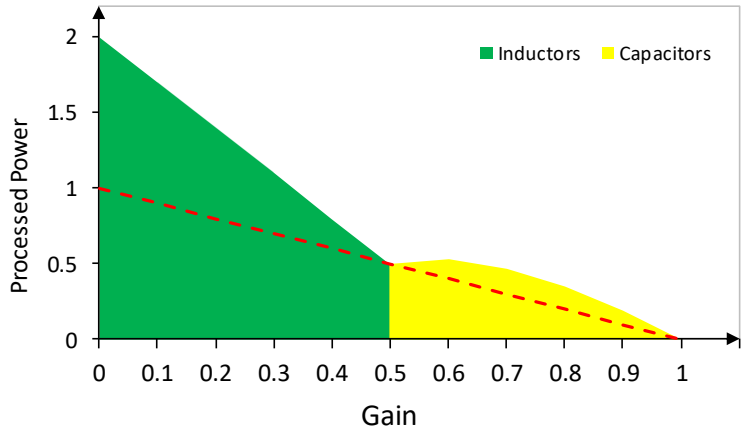


Fig. 5.8 Two Phase Interleaved buck converter processed power, and Wolaver limit

Only the absorbed power is shown due to the complexity in visualising more than two switching states, a discussion on this is provided in the following section. The processed power has two trends for duty cycles less and greater than 50%. The two-phase interleaved buck duty cycle is the same as its gain. The minimum processed power is observed at 50% gain, where the converter is at the fundamental limit. The converter in this mode only has two switching states, S1 closed and S2 open or S1 open and S2 closed, at 50% gain the interleaved operation is equivalent to a conventional buck.

For duty cycles greater than 50%, the interleaved processes less power, and has high direct power because S1 and S2 are closed for three out of the four phases, causing more direct current flow from the input to output. The voltage across the inductors and power approaches zero as the conversion gain approaches 1 as a result. For duty cycles less than 0.5, the converter processes more power than the fundamental limit as a result the reactive components process more power.

5.7.1 Limitations of Visualising converters with N states

The processed power plots considered so far consisted of a single switch with two switching states or phases. The processed power plots in Fig. 5.2 as an example represent one of these two switching states. In this state one component is absorbing and the other is delivering power. The plot is valid and can be easily visualized using only one, since the two phases are equivalent in terms of the power handled. However, applying the same to a converter with more than two states is complex.

For an example, the interleaved buck at duty cycles greater or smaller than 50% has four switching states. Fig. 5.9 shows waveforms with the four switching states for duty cycle less than 50%. Two of the switching states are repeated, so effectively three states. Though the power handled over a full cycle by each reactive component is balanced, the power at each state is not always equal to the other. This poses a challenge in visualising the metric using any of the states. The approach used in Fig. 5.8 to visualise the processed power, is by taking half of the total reactive component power.

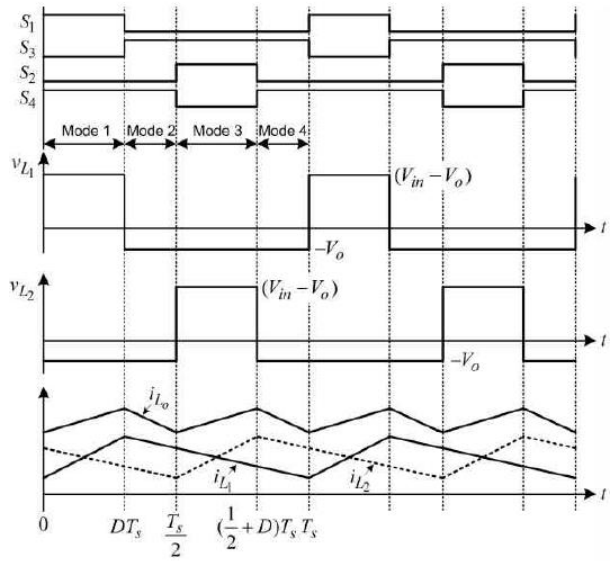


Fig. 5.9 Two Phase Interleaved Buck Converter waveforms[53]

5.8 Summary

Four step-down topologies were analysed including the buck converter as a baseline. The averaged topology model results show that the hybrid switched inductor is a minimum limit

topology like the buck. The metrics paint the topologies in the same light, with the hybrid converter being painted in better light for conversion gains less than 0.5. The metrics show agreement in the buck-boost worst performance. The proposed RMS metric gives similar results to all the metrics and power exchange balance similar to the processed power plots. Results of an interleaved converter were provided to show the limitation of the power processed exchange for topologies with more than two switching states.

The processed power and RMS metric favored a hybrid switched inductor when compared to three converters, conventional buck-boost, switched inductor, and the traditional buck. A two-phase interleaved converter was assessed using reactive component power plot which aided in visualising its power transfer mechanism and equivalence to the buck converter at 50% duty cycle. A discussion was provided addressing the limitation of the visualisation introduced in this section to only two states, due to the complexity introduced by more states, of converters such as the interleaved buck.

Chapter 6 Discussion

6.1 Summary and Categorisation of Topologies

In this study, DC-DC converter topologies were split into their switches and reactive components, as seen in Table 6.1. The metrics for analysing these topologies were split into those that describe the performance according to switches and reactive components. These metrics were further split into those that preserve the waveform information and those based on averaging. The metrics based on averaging have a fundamental limit, the Wolaver Limit.

Table 6.1 Metrics Summary and Relation

Including duty Cycle info

		Metrics based on Averaging $\boldsymbol{Wolaver\ Limit} \geq \frac{\boldsymbol{G-1}}{\boldsymbol{G}} \cdot \boldsymbol{P_{out}}$	**Metrics that preserve waveform**
DC-DC Converter Topology	**Switches**	$P_{Processed} = V_{Avg} \cdot I_{Avg}$ **Average Topology Model (Chapter 3)**	VA Rating Stress Factor_Semiconductor
	Reactive Components	$P_{component} = \frac{1}{2T} \int_0^T \lvert v(t) \cdot (t) \rvert \cdot d(t)$	$\boldsymbol{P_{component} = D(V_{onsate} I_{onstate})}$ **& RMS Metric (Chapter 4)** Stress Factor_Inductor Stress Factor_Capacitor

6.2 Metrics Based on Averaging

The averaging metrics, in Table 6.1, were shown to be bounded by a minimal performance limit, which is the Wolaver limit ($\frac{G-1}{G} \cdot P_{out}$). These metrics include processed power of the switches defined as the product of their average voltage and current. The absolute value defined processed power of the reactive components. Under the metrics based on averaging,

an average modelling tool was proposed and proven to meet fundamental circuit theory. The tools' ability to convert any converter to its core structure and thus placing converters on equal footing for comparison was demonstrated. The revised processed power metric for reactive components which eliminates the absolute value based on circuit analysis in chapter 4, also forms part of the averaging metric. This simple elimination of the absolute value proved to be vital in visualising the power transfer mechanism within any converter topology. Clearly showing the power exchange and balance along the indirect power transfer path amongst reactive components. At the same time visualising the direct power transfer path within a converter.

6.3 Metrics that Preserve Waveform Information

Metrics that preserve the waveform information for the converter switches are the VA Rating and the semiconductor stress factors as seen in Table 6.1. In chapter 3 the relationship and link between the switch processed power averaging metric and the VA rating was shown to be duty cycle. By including the duty cycle information of the processed power of the switches we obtain the VA Rating.

Within the waveform preserving metrics, under reactive components we have the inductor and capacitor stress factor and the proposed RMS metric in Chapter 4. The waveform preserving metrics reveal the stresses on the reactive components at extreme duty cycles, characterized by high ripple and voltage peaks. Redefining the reactive processed power metric without the absolute value results in the RMS metric. The RMS metric was derived mathematically using statistical variance and shown to enhance the reactive component processed power metric for comparison at different duty cycles.

6.4 Differences between RMS and Stress Factors

The major difference between the stress factors and the RMS metric, is that the stress factors are defined using the RMS of the current, and the latter the RMS of power. The two are the same (almost) if the voltage remains constant. Not always a good comparison when the duty cycle comes into play.

Which one is more appropriate to use depends on the results, and so far, the RMS metric because of the Wolaver limit is better preferred even though it is unusual to take the RMS of power. The interpretation of the RMS of power can be dealt with, because the RMS metric is simply variance. This should be enough interpretation since it is directly related to variations in current(ripple) and voltage peaks.

Whilst the metrics based on averaging provide a measure of how well the metric performs relative to the fundamental limit, they do not tell us much at the extreme duty cycles <0.2. The VA rating of the switches and the RMS metric for the reactive components incorporate the effect of the duty cycle to some extent, which provide more information on the performance. These metrics thus provide levels of component comparison; these levels can be used to form a systematic comparison approach.

6.5 Systematic Converter Comparison

High level metrics are categorized in the section above as averaging metrics and waveform preserving metrics for both the switches and reactive components. The two groups are at different levels and provide different levels of detail, with the waveform preserving providing more detailed information.

Introducing the average modelling tool provides a topological way to determine if a circuit is at the Wolaver limit or an excessively complicated structure. The average modelling also places the converters in equal footing, aiding objective comparison.

The systematic converter comparison thus starts with the average modelling procedure applied to a vast number of topologies, followed by a detailed comparison using the proposed RMS metric.

Chapter 7 Conclusion and Recommendations

7.1 Conclusion

In conclusion, this dissertation has introduced a systematic methodology for selecting topologies, aiming to streamline the complex process of converter assessment. Five key metrics from the literature, including a fundamental converter performance limit, were critically evaluated, with each metric defined and interpreted through application to a simple buck converter. Despite the distinct definitions of these metrics, the analysis revealed similarities in their outcomes, highlighting their consistent performance evaluation capabilities. However, notable gaps were identified, particularly regarding the limitations of the absolute value-defined processed power metric, which contrasted with the detailed performance insights provided by stress factors.

Contribution: Average modelling procedure which reveals the core topology structure of any converter. The contributions of this study are threefold: Firstly, Chapter 3 introduced an average topology modeling approach, offering a novel method to unveil the core structure of any converter circuit. This modeling procedure was shown to effectively determine if a topology operates at its fundamental limit, with the addition of duty cycle information further linking to the VA Rating, thus providing detailed insights into converter switch performance at varying duty cycles.

Contribution: Proposed a detailed(unifying) metric for converter topology selection. Secondly, Chapter 4 proposed an RMS-based metric derived from statistical variance, enhancing the processed power metric to reveal performance differences across converters at different duty cycles. Notably, this metric demonstrated the potential to consolidate multiple metrics into a unified assessment framework, streamlining the evaluation process.

Contribution: Developing a systematic approach to topology selection. Lastly, this dissertation presented a systematic approach to topology selection, categorizing metrics based on their utility levels. For initial high-level comparisons involving multiple topologies, the averaged topology modeling approach was recommended, offering a quick and efficient means to filter out unsuitable options. Subsequently, waveform-preserving metrics, such as the RMS metric, were suggested for detailed comparison among filtered options, providing comprehensive insights into converter performance at specific conversion ratios.

In essence, this study offers valuable contributions to the field of power electronics, providing a structured framework for topology selection that balances ease of use with detailed performance evaluation. By integrating novel methodologies and metrics, this approach promises to enhance decision-making in converter design and optimization processes.

7.2 Recommendations

Recommendations for future work to extend the research and its outcomes include:

- Application to Diverse Converter Types: Explore the potential of the proposed approach as a classification tool for various converter topologies, including hybrid, resonant, and switched capacitor converters, as well as comparison studies between isolated and non-isolated variants.
- Development of Topology Database: Consider the implementation of a topology database that categorizes converter topologies based on their performance metrics, providing a comprehensive resource for researchers and power electronics designers.
- Digital Implementation: Investigate the feasibility of digitally or software implementing the average topology modeling and converter topology selection approach, enhancing accessibility and usability.
- Incorporation of Operational and Technological Factors: Address the limitations of the study by incorporating operational and technological factors such as frequency, reactive component energy density, conduction modes (e.g., Continuous Conduction Mode or Discontinuous Conduction Mode), losses, non-resistive loads, etc., in future converter assessment studies to provide a more comprehensive analysis.

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Appendices

Appendix A: Switched-Capacitor Converter

A.1. Switched-Capacitor Converter Basics

This section provides the basics of switched-capacitor converters and highlights their main operational modes; slow switching limit (SSL) and fast switching limit (FSL), used in [15] for the SSL and FSL metric(s).

A switched-capacitor (SC) converter is a DC-DC converter without an inductor, consisting of capacitors and switches to convert one voltage level to another. This makes them ideal for implementation within integrated circuits. Consider Fig A.1 showing a traditional inductor-based converter and a switched-capacitor converter both having a conversion ratio of 10:1. The buck converter relies on magnetic energy storage to achieve this conversion. In, the SC converters energy flows from the input to the output by alternating the switch states to charge and discharge a several stages (of capacitors). Though the SC converter contains more components it is more suited for high power density and high-efficiency DC-DC applications due to the relative size of capacitors to inductors. The challenge is however maintaining a good efficiency over a range of conversion ratios.

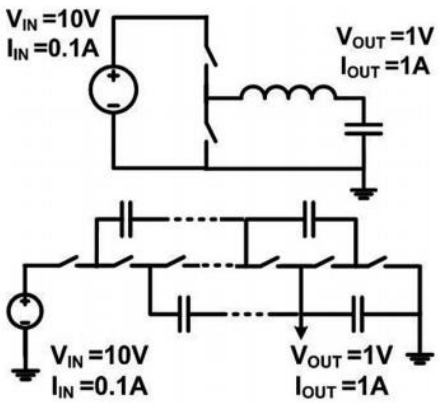

Fig A.1 2:1 Buck and Ladder-type Switched-Capacitor Converter[28]

Consider the ideal model of the SC Converter in Fig A.2 with a conversion ratio M, represented by the turns ratio of an ideal transformer. With a series resistance (R_o), representing the voltage across the capacitors to allow charge to flow and parasitic elements (capacitor ESR, parasitic inductance and resistance of the leads, and switch on-resistance).

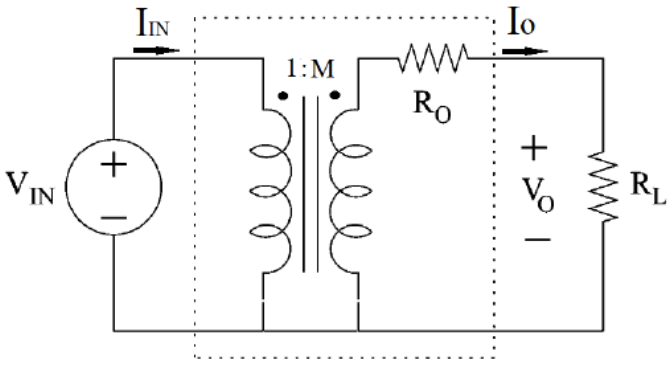

Fig A.2 SC Converter Equivalent Model [13]

The maximum achievable efficiency is:

$$efficiency = \left(\frac{V_o}{V_{in}}\right)\cdot\left(\frac{I_o}{I_{in}}\right) = \left(\frac{V_o}{V_{in}}\right)\cdot\left(\frac{1}{M}\right)$$

$$= \left(M \cdot V_{In} \cdot \frac{\left(\frac{R_L}{R_L + R_o}\right)}{V_{in}} \cdot \left(\frac{1}{M}\right) \right) \qquad \text{(A.1)}$$

$$= \frac{1}{1 + \frac{R_o}{R_L}}$$

It is worth noting from equation (A.1) that the output impedance of the converter (R_o) is never zero even in ideal conditions since it also represents the voltage ripple (due to periodic charge/discharge) required for charge balance. Charge balance is crucial for SC converters to ensure the capacitors do not short circuit. Increasing the output impedance, decreases the voltage to the load and thus the maximum power output. One way of reducing the resistance, in this case, is by increasing the frequency; this is covered in later sections. The output impedance of an SC converter is critical in determining the converter performance, i.e efficiency, output voltage, and overall volume, as will be discussed in the next sections.

A.2. SC Converter Operation

The operation of SC converters is best explained by circuit analysis of a simple 1:2 converter (shown in Fig A.3). The circuit has two capacitors C_{fly} and C_{out} and four switches labeled 1 and 2 according to their switching sequence.

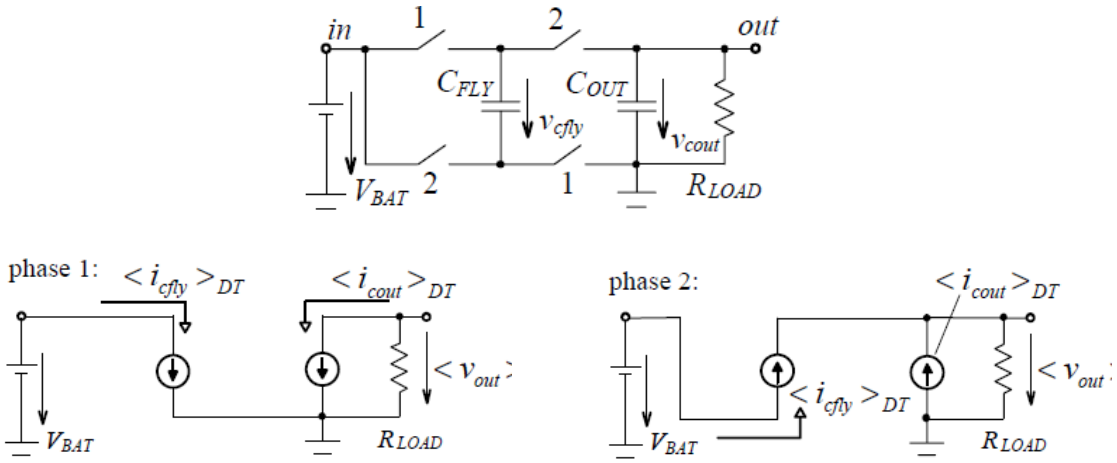

Fig A.3 1:2 Voltage Doubler, phase 1: SW1 "Closed", Phase 2: SW2 "Closed" [14]

Consider the following assumptions for analysis:

- Current sources represent the capacitors without parasitic elements (ignored for analysis),
- The capacitor charge time constant is shorter than the switching period
- The output capacitor is large, such that the output voltage is kept constant

In phase 1, the output capacitor discharges to the output,

$$i_{cout} = -\frac{V_{out}}{R_{load}} \tag{A.2}$$

$$V_{cout} = V_{out} \tag{A.3}$$

Whilst the fly capacitor is charged to the input voltage by the input current;

$$i_{cfly} = i_{bat} \tag{A.4}$$

$$V_{cfly} = -V_{bat} \tag{A.5}$$

At the beginning of phase 2, both capacitors discharge to the output;

$$\frac{V_{out}}{R_{load}} = i_{cout} + i_{cfly} = i_{cout} - i_{bat}\ ; \tag{A.6}$$

$$V_{out} = V_{cout} = V_{bat} - V_{cfly} \tag{A.7}$$

The equations above prove that charge balance is maintained since the average current for each capacitor is zero over a period. From equations (A.4) and (A.6) on average the output current is

$$I_{load} = \frac{V_{out}}{R_{load}} = \frac{1}{2}\left(-i_{cout} + i_{cout} + i_{cfly}\right) = \frac{1}{2}\left(i_{cfly}\right) = \frac{1}{2} i_{bat} \tag{A.8}$$

Assuming lossless conditions, then the output voltage will be twice the input ($V_{out} = 2V_{bat}$). Fig A.4 and Fig A.5 show the capacitor currents and voltage and the output voltage using parameters listed in Table A.1. The plots confirm the SC converter analysis above.

Table A.1 Simulation Parameters[54]

Parameter	Value
C_{fly}	$1\mu F$
C_{out}	$10\mu F$
f_{sw}	$650kHz$
$ESR(Cout/Cfly)$	1Ω
$R_{on}(SW1/2)$	1Ω

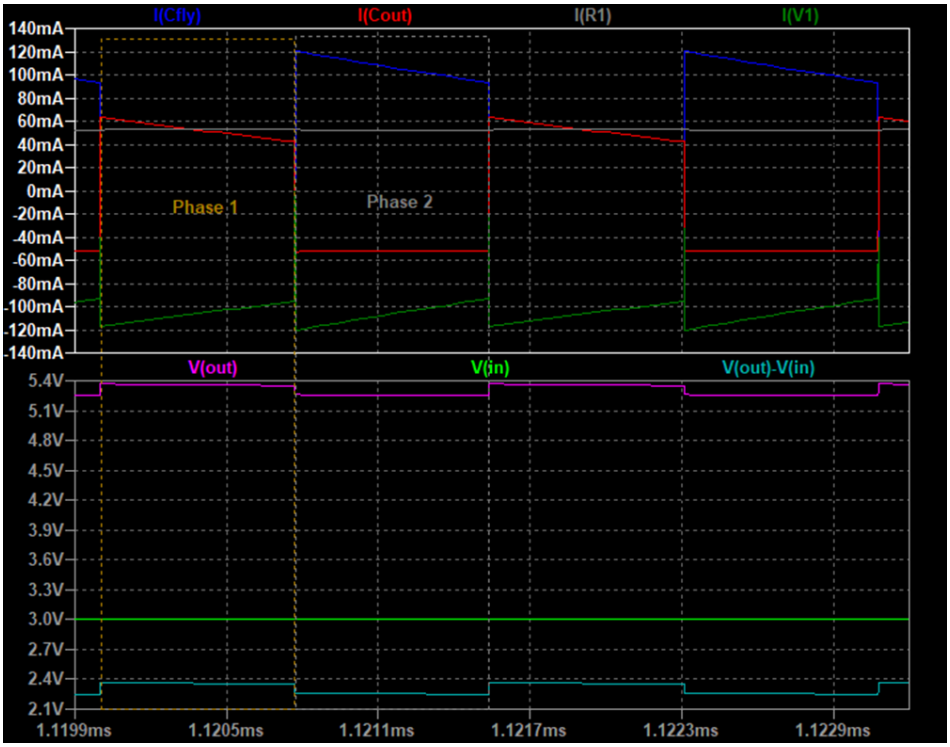

Fig A.4 Capacitor Voltages and Currents, Switching Phase 1 and 2

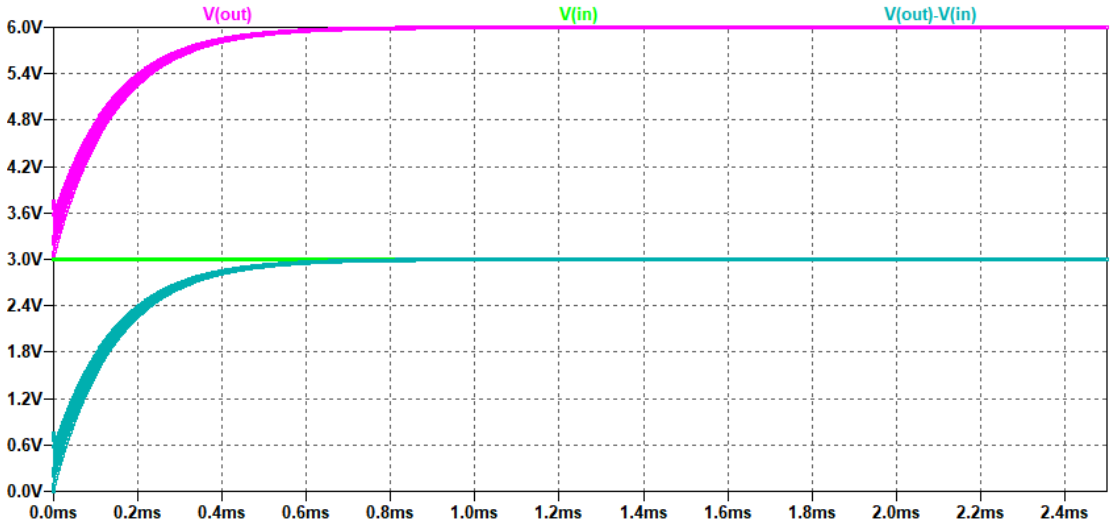

Fig A.5 Input and Output Voltages

A.3. SC Converter Output impedance

The output impedance of the SC converter is frequency-dependent as one would assume for a circuit consisting of reactive components, capacitors. The next section shows the effect of switching frequency on the SC converter operation.

A.4. Slow Switching Limit

The equivalent resistance of the SC converter can be derived from the equations in the previous section, the voltage across the fly capacitor is

$$\Delta V_{cfly} = 2V_{bat} = \frac{\Delta Q}{C_{fly}} = \frac{\Delta I}{f_{sw} C_{fly}} = i_{bat}\left(\frac{2}{f_{sw} C_{fly}}\right) = i_{bat}\, R_{c,equivalent} \tag{A.9}$$

where,

$$R_{c,equivalent} = \frac{2}{f_{sw} C_{fly}} \tag{A.10}$$

And f_{sw} is the switching frequency with a 50% duty cycle

Equation (A.10) can be used to determine the output impedance of the SC converter as long as the assumptions made initial hold. The equation holds when the switching frequency $(1/t)$ is sufficiently lower than the charge time constant RC of the circuit given by equation (A.11).

$$\mathrm{V_c(t)} = \mathrm{V_{in}}\left(1 - \mathrm{e}^{-\frac{\mathrm{t}}{\mathrm{RC}}}\right) \tag{A.11}$$

where R is the parasitic resistances of the circuit. According to equation (A.11) when period $t > RC$ then $V_c \approx V_{in}$, thus the parasitic resistance has no influence, and the output impedance at low frequencies resolves to equation (A.9).

By substituting equation (A.10) into (A.1) it can be shown that the efficiency, power loss, and voltage drop of the SC converter are dependent on the converter impedance.

A.5. Fast Switching Limit

In the previous subsection, the equivalent resistance of an SC converter was established assuming low switching frequency. When the switching frequency is greater than the time constant, the capacitor does not reach the final voltage as shown in equation (A.9) and thus the equivalent resistance in equation(A.10) does not hold. The equivalent resistance approaches zero at high frequencies, and the voltage across the capacitor is almost constant.

To ensure steady-state operation current still flows in the first and second phase of the circuit due to the voltage drop between the input and output

$$2V_{bat} = i_{bat}R \tag{A.12}$$

where the switches are modelled by an equivalent on switch resistance and parasitic resistance lumped into an equal resistance R, in both phases. This again leads to losses of and reduces the output voltage. The equivalent resistance of the SC converter over a switching period is given by

$$R_{sw,equivalent} = \frac{2V_{bat}}{i_{bat}} \tag{A.13}$$

A.6. Frequency Sweep Simulation

Using the *LTSpice* simulation parameters in Fig A.6, the output impedance of the SC converter is frequency-dependent(shown in Fig A.7). The frequency dependence is according to equations (A.10) and (A.13) with two limits, the slow switching limit (SSL) and fast switching limit [15], [16], [28].

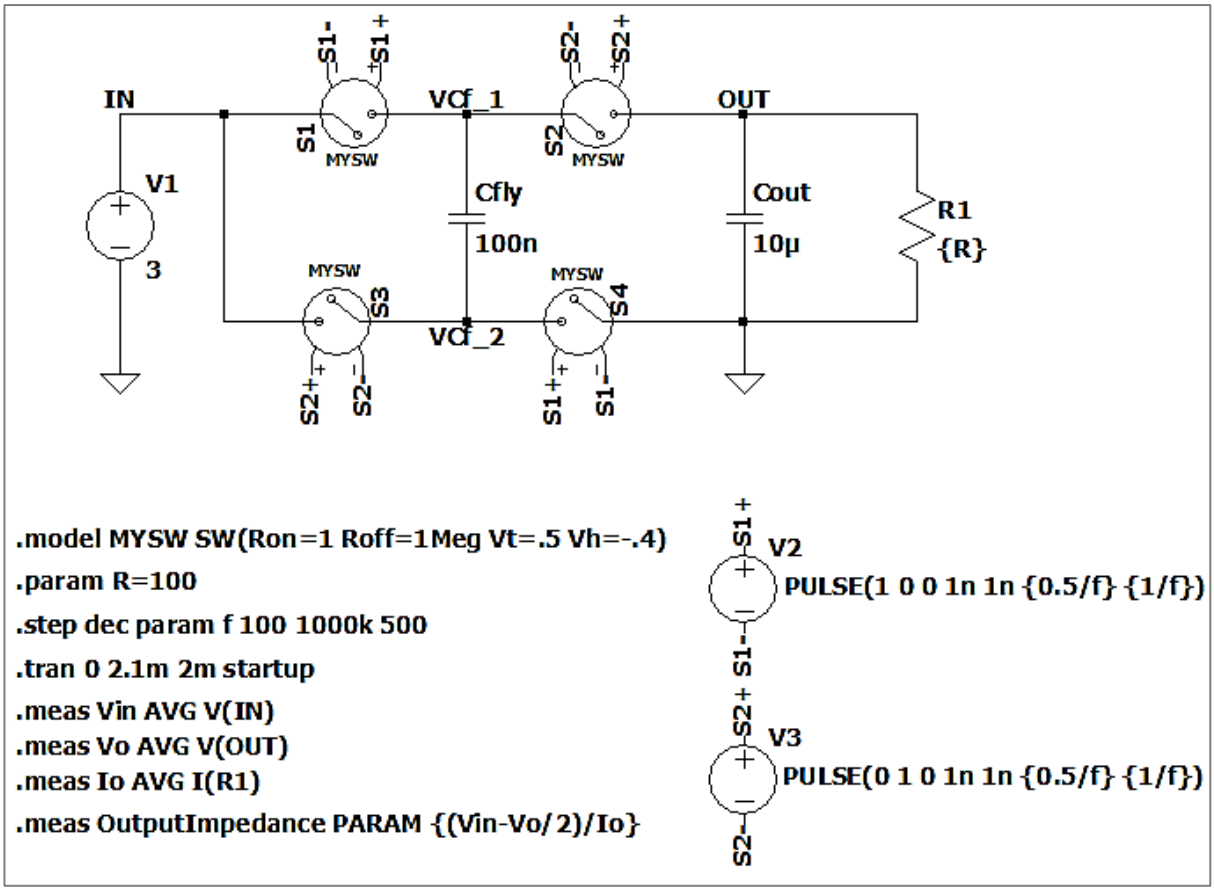

Fig A.6 Frequency sweep LTSpice parameter setup

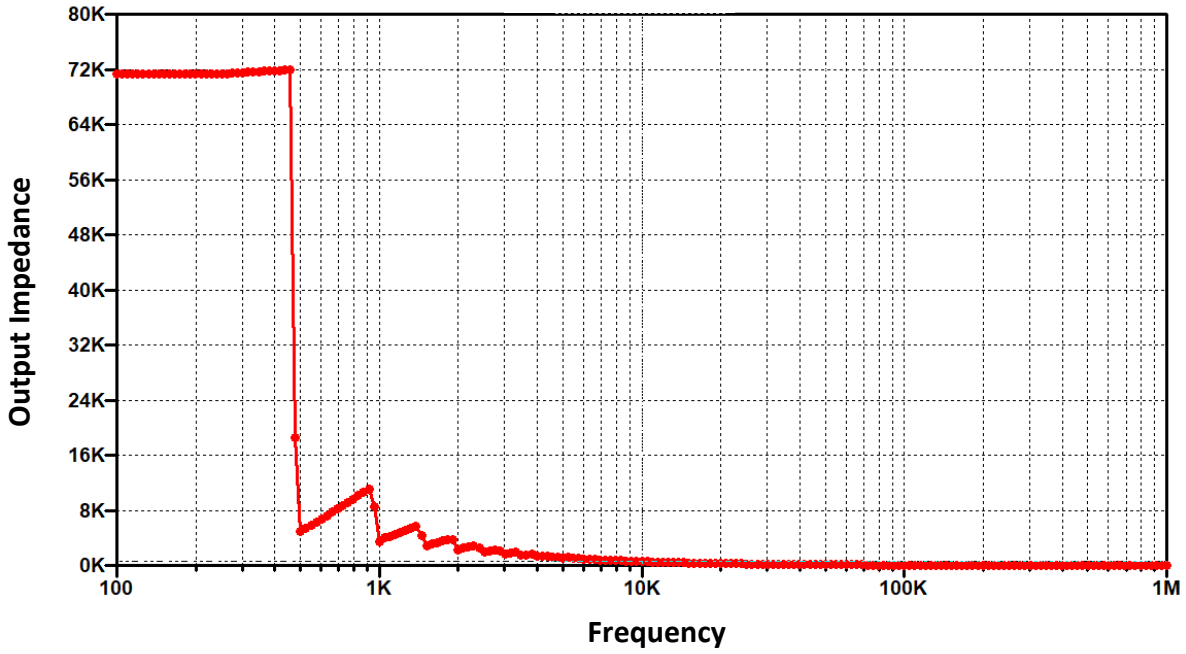

Fig A.7 Output Impedance vs Frequency

These limits represent the capacitor charge time constant providing two modes of operation. In the SSL mode, the capacitors charge to a final steady-state value due to a lower switching frequency, in this mode, the impedance appears capacitive at the load. In the FSL mode, on-switch resistance dominates and restricts the capacitor charge, as the switching frequency is higher. The converter thus appears resistive at the output. Operation in FSL or SSL, even in between, affects both performance and the overall converter volume. In the case of deep SSL operation, increasing the on-resistance has a minute effect on the output impedance. This allows the smallest size switches to be used and maintaining the same efficiency resulting in a smaller volume converter solution.

In deep FSL, reducing the capacitor size has little effect on the output impedance, meaning their sizes can be minimised for the same performance, output voltage and efficiency. Though outside the scope of this study, this can be demonstrated by doing a RLoad sweep and plotting the output voltage and efficiency smaller fly capacitance (Cfly) values. This was done with capacitance 10 times smaller than in the Fig A.6. The worst performance drop was observed at RLoad= 100, with the output voltage drop of 300mV to about 5.1V, and overall 6% drop in efficiency to 83% was observed.

A.7. Summary

The fundamentals and analysis of switched-capacitor converters and their advantages (and disadvantages) have been presented in this section. The fast and slow operating modes for switched-capacitor converters from which the FSL and SSL metrics are derived by Seeman's were presented for a simply voltage doubler example. The effect of frequency on the metrics were demonstrated and implications discussed.

Appendix B: Topology Circuit Analysis

B.1. Hybrid Switched-Inductor Topology

This section covers the circuit analysis, VA Rating, and average modeling for the Hybrid Switched-Inductor in Fig B.1.

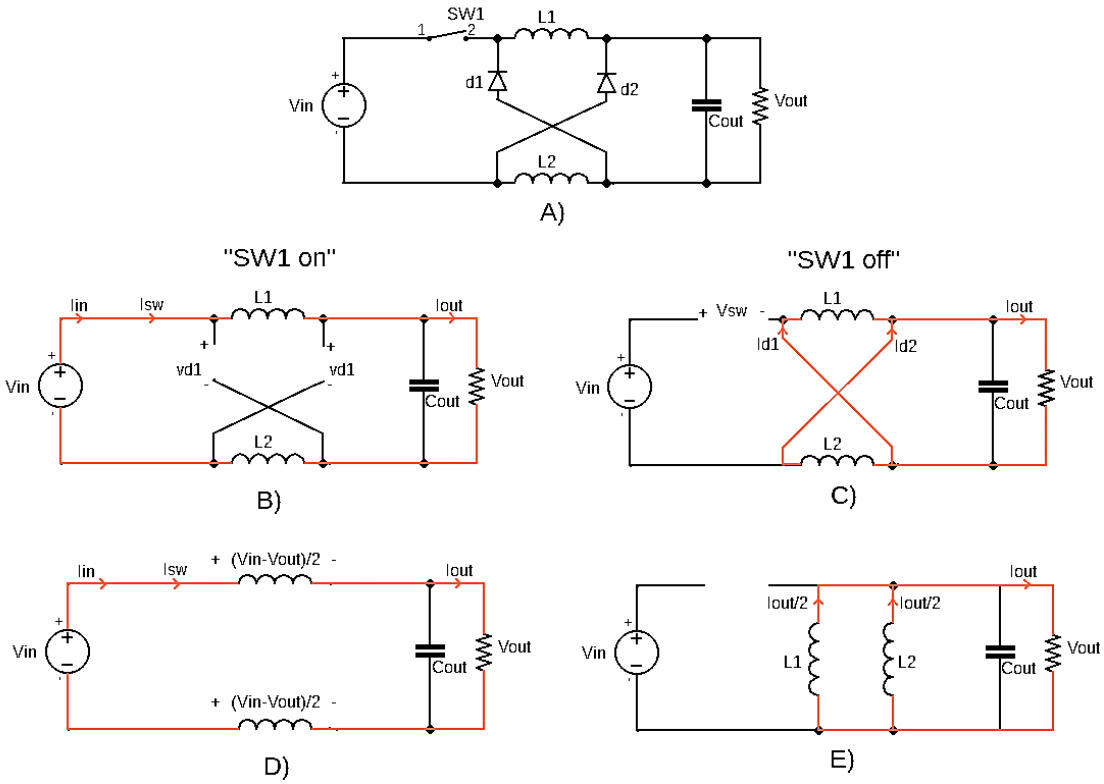

Fig B.1 Hybrid Switched Inductor circuit[42]

When the switch SW1 is "on":

The inductors are in series. The switch current (i_{sw}) is equal to the input current (i_{in}) and the inductor current(s) (i_{L1} i_{L2}) are equal to the output current.

$$V_{L1} = V_{L2} = \frac{1}{2}(V_{in} - V_o)$$

$$V_{D1} = V_{D2} = V_{in} - V_{L2} = \frac{1}{2}(V_{in} + V_o)$$

$$i_{sw} = i_{in}$$

$$i_{L1} = i_{L2} = i_{out}$$

When the switch SW1 is "off":

The inductors are parallel to the output. The diodes and inductors conduct half the output current.

$$V_{L1} = V_{L2} = -V_o$$

$$V_S = V_{in} - V_{L2} = V_{in} + V_o$$

$$i_o = i_{L1} + i_{L2}$$

$$i_{D1} = i_{D2} = i_{L1} = i_{L2} = \frac{i_o}{2}$$

With the equations above the hybrid switched inductor gain is determined as shown in equation (B.2) below using volt-second balance.

$$\begin{aligned} &(V_L)_{on} * DT + (V_L)_{off} * (1-D)T = 0 \\ &\frac{1}{2}(V_{in} - V_o) * D + (-V_o) * (1-D) = 0 \end{aligned} \tag{B.1}$$

$$\frac{V_o}{V_{in}} = \frac{D}{2-D} \tag{B.2}$$

B.1.1. Hybrid Switched Inductor has L-Shaped Average Model

Applying the average topology modelling procedure outlined in Chapter 3, where capacitors are replaced with an open circuit, inductor with short circuit and diodes and switches with average voltage and current results in the model shown in Fig B.2. The hybrid switched Inductor has an L-shaped average topology model, making it a Wolaver limit topology.

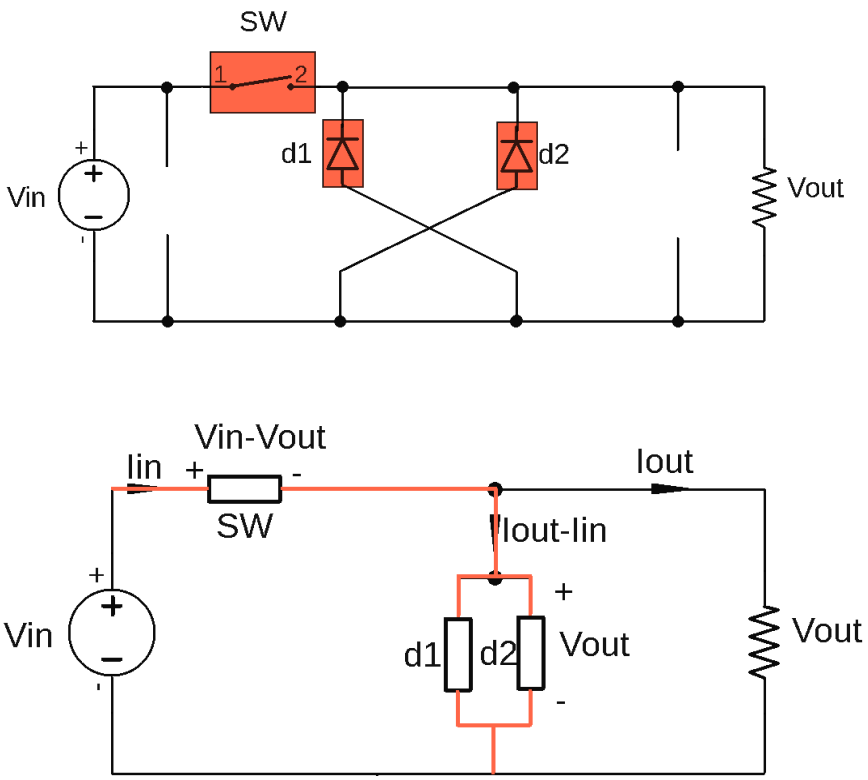

Fig B.2 Hybrid Switched Inductor L-Shaped Average Model

B.1.2. Average Modelling Validation

Using the average model obtained in Fig B.2, the equations below determine the average power, provide proof of Tellegen's power Theorem.

Diode and Switch Average Voltage and Current:

$$V_S = V_{in} - V_o$$

$$I_S = I_{in}$$

$$V_{D1} = V_{D2} = V_{in} - V_S = V_o$$

$$i_{D1} = i_{D2} = -(I_o - I_{in})$$

$$V_{S(ave)} = (V_s)\_on * DT + (V_S)\_off * (1 - D)T$$

$$V_{S(ave)} = (0) * D + (V_{in}) * (1 - D) = (V_{in})(1 - D)$$

$$I_{S(ave)} = (i_s)\_on * DT + (i_S)\_off * (1 - D)T$$

$$I_{S(ave)} = i_{in} * D + 0 * (1 - D) = i_{in} * D$$

Average Powers:

$$P_S = V_S * I_S = (V_{in} - V_o)I_{in}$$

$$P_{D1} = P_{D2} = V_o * (I_o - I_{in})$$

Proof of the Tellegen's power Theorem:

Tellegen Power Theorem: $P_{SW} + P_{D1} + P_{D2} = 0$

$$(V_{in} - V_o)I_{in} - V_o * (I_o - I_{in}) = 0$$

$$V_{in}I_{in} - V_oI_{in} - V_oI_o + V_oI_{in} = 0$$

Wolaver Limit Proof

The converter can be shown to meet the Wolaver limit by taking the processed power of the switch or diode as shown in the equation below.

$$P_{AC} = P_{SW} = (P_{D1} + P_{D2}) = P_{out}\left(1 - \frac{1}{G}\right)$$

B.1.3. VA Rating

VA Rating (see main document for derivation)

$$VA_{total} = VA_{diode} + VA_{switches}$$

$$= \frac{P_{out}}{2}\left(\frac{1}{G} + 1\right) + P_{out}\left(\frac{G+1}{G}\right)$$

$$VA_{total}(Hybrid\ Switched\ Inductor) = \frac{3P_{out}}{2}\left(\frac{G+1}{G}\right)$$

B.2. Hybrid Switched Capacitor

This section covers the circuit analysis, average modelling and VA Rating analysis of the Hybrid Switched Capacitor in Fig B.3. The hybrid switched capacitor has the same gain as the Hybrid switched inductor in Section B.1 but a different average model.

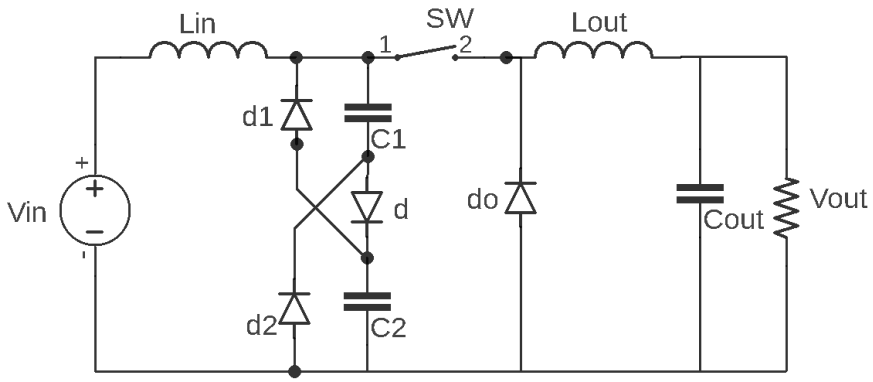

Fig B.3 Hybrid switched capacitor converter from [50]

$$V_C = \frac{V_{\text{in}}}{2-D}, \qquad V_o = \frac{D}{2-D}V_{\text{in}}$$

$$V_{D1} = V_{D2} = V_D = V_{D_o} = V_C$$

$$V_{L_{\text{in.max}}} = V_{\text{in}} - V_C = \frac{1-D}{2-D}V_{\text{in}}, \qquad V_{s.\max} = 2V_C$$

$$I_{\text{in}} \approx \frac{V_o I_o}{V_{\text{in}}} = \frac{D}{2-D}I_o, \qquad I_{D_o} = I_o(1-D)$$

$$I_{D_1} = I_{D_2} = \frac{1}{2}D(I_o - I_{\text{in}}) = D\frac{1-D}{2-D}I_o$$

$$I_D = I_{\text{in}}(1-D) = \frac{D(1-D)}{2-D}I_o.$$

Fig B.4 The component voltages and currents from [50]

B.2.1. Hybrid Switched Capacitor has Pi-Shaped Average Model

The equivalent switched capacitor circuit with inductor and capacitor replaced with short and open circuit respectively and the switch and diodes replaced with average models is shown in Fig B.5 a). The average topology model is pi-shaped as illustrated in Fig B.5 b), which is different to the hybrid switched inductor even though they have the same gain.

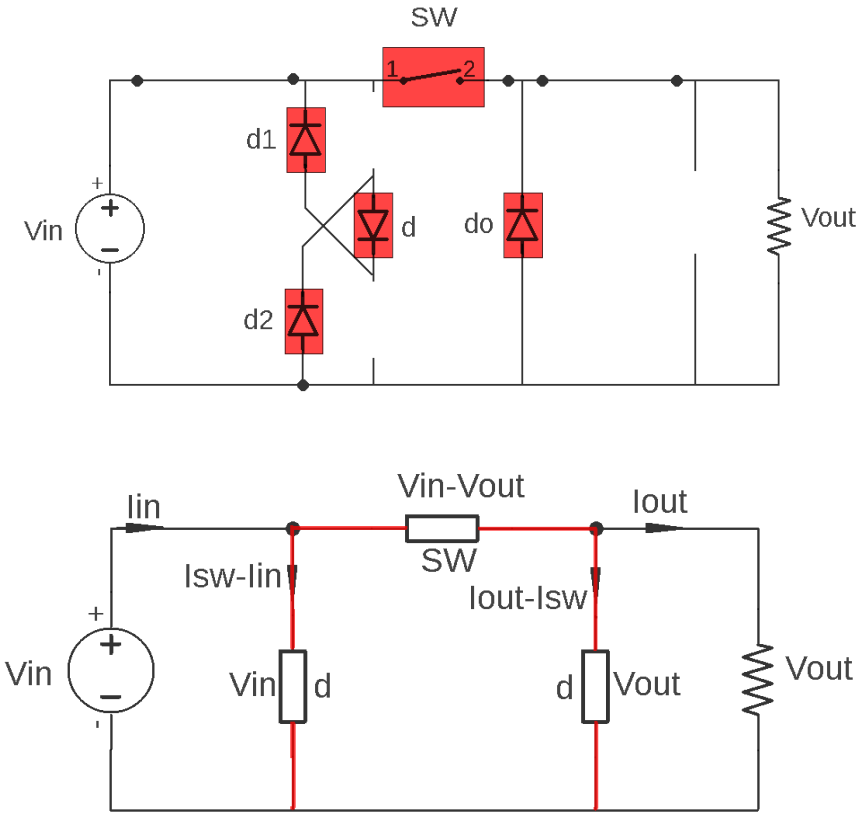

Fig B.5 Hybrid Switched Capacitor, a) Equivalent average circuit, and b) pi-shaped average topology model

B.2.2. VA Rating

Derivation of the hybrid switched capacitor converter total VA rating is given in the equations below.

$$VA_{total} = VA_{D1} + VA_{D2} + VA_{DO} + VA_{DI} + VA_{SW}$$

$$VA_{D1} = VA_{D2} = \frac{1}{2} P_{out}(1 - G)$$

$$VA_{DO} = \frac{1}{2} P_{out} \left(\frac{1-G}{G} \right)$$

$$VA_{DI} = \frac{1}{2} P_{out} (1-G)$$

$$VA_{SW} = P_{out} \left(\frac{1+G}{G} \right)$$

$$VA_{total} = 2 \times \frac{1}{2} P_{out} (1-G) + \frac{1}{2} P_{out} \left(\frac{1-G}{G} \right) + \frac{1}{2} P_{out} (1-G) + P_{out} \left(\frac{1+G}{G} \right)$$

$$VA_{total}(Hybrid\ Switched\ Capacitor) = \frac{P_{out}}{2} \left[\frac{G+3}{G} + 3(1-G) \right]$$

B.3. Example of Buck-Boost Converter with T-Shaped Average Topology

This section covers the circuit analysis, VA Rating, and average modeling for a series-parallel Buck-boost topology with T-shaped average model in Fig B.6.

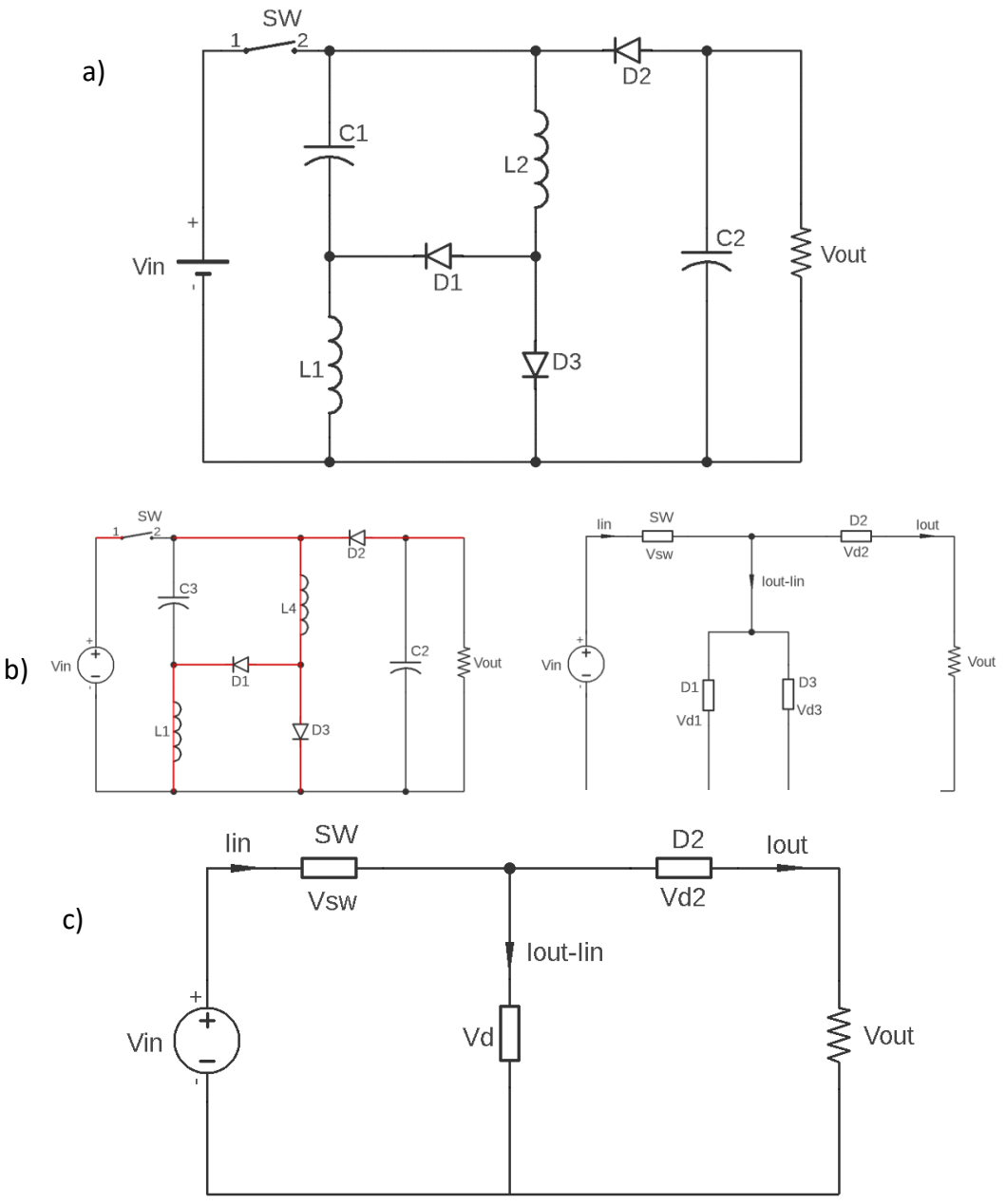

Fig B.6 a) Buck Boost circuit, b) average equivalent circuit, and c) resultant T-shaped average model

B.4. Quadratic Buck Converter

This section covers the circuit analysis, VA Rating and average modeling for a quadratic buck shown in Fig B.7. Quadratic buck has square of a buck converter $\frac{V_{out}}{V_{in}} = D^2$.

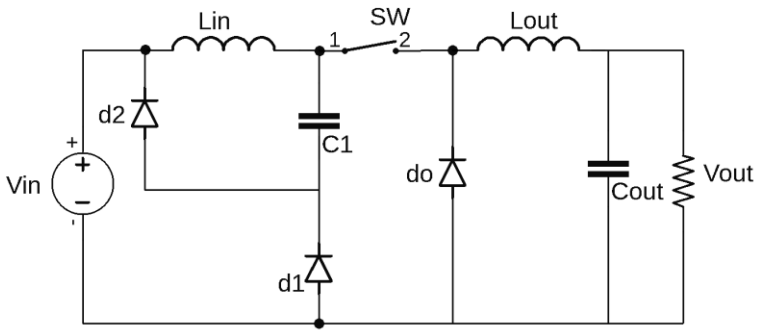

Fig B.7 Quadratic Buck Converter Circuit Analysis

B.4.1. VA Rating

Derivation of the quadratic buck capacitor total VA rating is given in the equations below.

$$VA_{total} = VA_{D1} + VA_{D2} + VA_{DO} + VA_{SW}$$

$$VA_{D1} = VA_{D2} = V_{in} * i_{in} \frac{(1-D)}{D} = P_{in}\left(\frac{1}{G^{1/2}} - 1\right)$$

$$D^2 = G$$

$$VA_{DO} = DV_{in} * i_{in} \frac{(1-D)}{D^2} = P_{in}\left(\frac{1}{G^{1/2}} - 1\right)$$

$$VA_{SW} = V_{in}(1+D) * \frac{i_{in}}{G} = P_{in}\left(\frac{1+G^{1/2}}{G}\right)$$

$$VA_{total}(Quadratic\ Buck) = P_{in}\left[2\left(\frac{1}{G^{1/2}} - 1\right) + \left(\frac{1}{G^{1/2}} - 1\right) + \left(\frac{1+G^{1/2}}{G}\right)\right]$$

$$= P_{in}\left[3\left(\frac{1}{G^{1/2}} - 1\right) + \left(\frac{1+G^{1/2}}{G}\right)\right]$$

B.4.2. Quadratic Buck has Pi-Shaped Model

The quadratic buck has a Pi-shaped topology like the hybrid switched capacitor. The average modelling outline for the quadratic is shown in Fig B.8. The resultant average model is the same as the Pi-shaped model shown in Fig B.5.

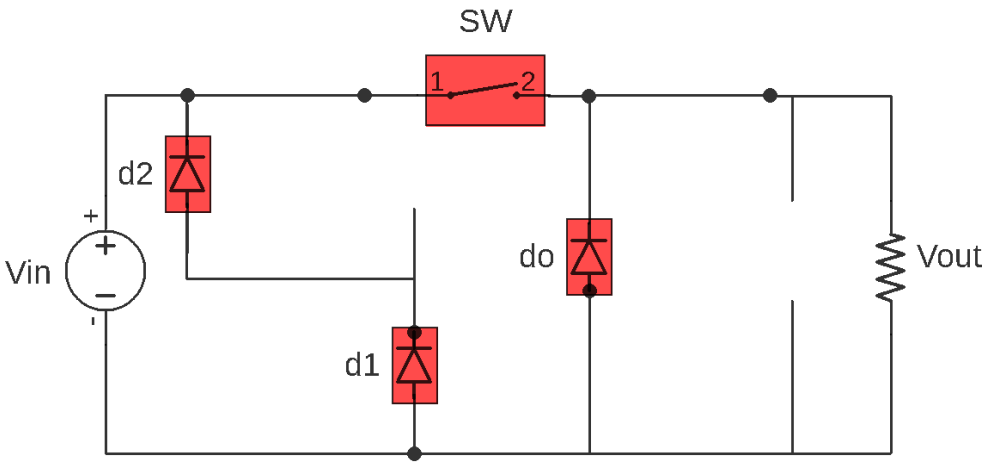

Fig B.8 Quadratic Buck Average Topology modelling

Appendix C: Fryze Theory

C.1. Fryze Theory: Motivation for Including Source Capacitance

The work of Fryze is from the early 1930s [55]. According to Fryze theory, the input current i can be divided into two components, active i_a and non-active current i_q. This idea can be conceptualised/modelled as an ideal source with an effective parallel capacitance as shown in Fig C.1.

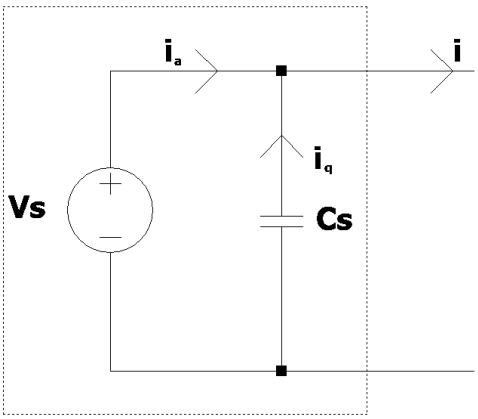

Fig C.1 Voltage source equivalent capacitor circuit

The addition of the capacitor is important for understanding the Fryze theory and later when comparing topologies, which a few authors omitted because of the simplicity. There the pure dc current (i_a) has the same wave shape as the ideal input voltage source (V_s), the other component is found by subtracting the active current from the total input current, as shown in equation (C.1)

$$i_q = i - i_a \tag{C.1}$$

The active current component is responsible for the active power P as shown in equation (C.2).

$$P = \frac{1}{T}\int_0^T V_s \cdot i dt = \frac{1}{T}\int_0^T V_s \cdot i_a dt \tag{C.2}$$

The power across the capacitor is on average zero but has a non-active component q, as in equation (C.3).

$$q = V_s \cdot i_q \tag{C.3}$$

Consider a system with a converter connected to the source in Fig C.1 with a purely resistive load as shown in Fig C.2. The input current ($i_a + i_q$) for different topologies differs based on their effective impedance, looking from the source. For a linear converter, the input current is active only, since its impedance is resistive. Whilst switch mode converter, with overall reactive impedances, either capacitive or inductive, are expected to draw both non-active and active current components. Thus, magnetic based converter topologies such as the buck will have a significant active current component. Similarly switched capacitor converter-based topologies. Furthermore, topologies within the same converter type, magnetic based or capacitor based, will have different non-active current components.

Note that converters with a non-active current thus ripple current will have higher input RMS current compared to the average (DC) input current.

Adding the capacitor in this model not only provides better visualisation and understanding of the Fryze theory, but has practical relevance and implications. Power sources are not ideal in nature and thus contain some equivalent capacitance or inductance, some are even capacitors (Super-capacitor and batteries). Also, in most applications a filtering/reserve capacitor is placed in close proximity to a converter to eliminate fluctuations or voltage drop due to effective inductance and resistance in the circuit. Thus, the input capacitor has practical significance in terms of volume and loss.

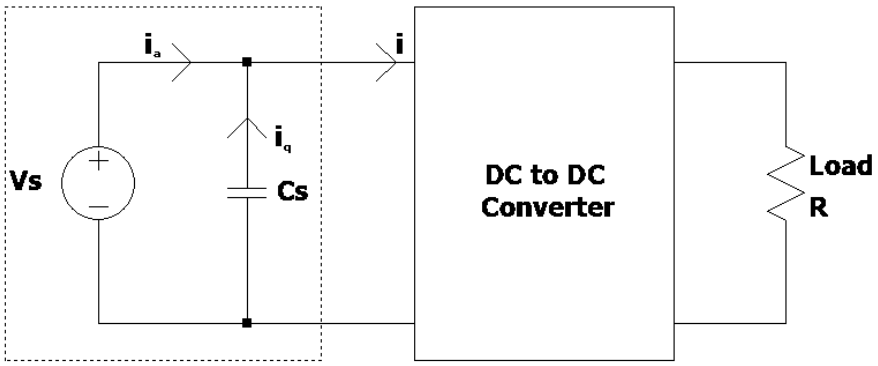

Fig C.2 Voltage source with parallel capacitance to converter and resistive load

Appendix D: Statistical Variance Properties Related to Power Electronics

Understanding the differences between root mean square (RMS) and average/mean absolute value (AAV) is crucial in assessing topologies, especially when dealing with waveforms and performance metrics. RMS amplifies short duration peaks in a waveform due to its squaring operation, while the average absolute value does not, leading to slight but important differences. When writing this dissertation, I did not find much literature on this topic related to power electronics, indicating a potential gap in the research.

D.1. Historical Context

Historically, squaring a value was used to ignore the direction/sign, focusing only on magnitude, simplifying analytical equations. With computational advancements, the square operation became computationally costly compared to logical conditions that handle signed values more efficiently. Absolute value computations, while simpler numerically, remain computationally intensive for symbolic computations.

D.2. RMS vs. Average Absolute Value

When averaging different waveforms like quadratic or triangle, results differ. This difference can be explained using Jensen's inequality, which states that the convex transformation of a mean is less than or equal to the mean after convex transformation[56]:

$$f\left[\sum_{i=1}^{n} p_i x_i\right] \leq \sum_{i=1}^{n} p_i f(x_i) \tag{D.1}$$

In power electronics, this inequality translates to:

$$\sqrt{\frac{1}{T}\int_0^T p^2\, dt} \geq \frac{1}{T}\int_0^T |p|\, dt \tag{D.2}$$

This highlights that the RMS value is always greater than or equal to the average absolute value for the same dataset.

D.3. Analytical vs. Computational Use

RMS has historically been favoured in analytical equations due to its simplicity in handling and solving equations. However, with advanced computation power, the average absolute value has gained prominence due to reduced computational run-time. The choice between RMS and average absolute value depends on the specific application and waveform characteristics.

D.4. Practical Implications

- **RMS**: Amplifies outliers, making it useful for capturing peak or short-lived behaviours such as ripple. It relates easily to the Pythagorean theorem, making the analysis intuitive.
- **Average Absolute Value (AAV)**: Better for capturing average behaviour over time, making it suitable for forecasting and longer-term analysis.

D.5. Conclusion

The choice between RMS and average absolute value in power electronics depends on the desired outcome. RMS is ideal for highlighting extreme behaviours and detailed analysis, while AAV is better for average performance evaluation. Both have their place in a systematic approach to converter topology assessment, as discussed in the main dissertation. By understanding these metrics' nuances, one can make more informed decisions in the design and evaluation of power converters.