# NON-INVASIVE DC-DC BUCK CONVERTER LOAD CURRENT ESTIMATION TECHNIQUE FOR EMBEDDED SOFTWARE POWER ESTIMATION

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A dissertation submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, in fulfilment of the requirements for the degree of Master of Science in Engineering.

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## DECLARATION

I declare that this dissertation is my own unaided work. It is being submitted to the degree of Master of Science in Engineering at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination at any other university.

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## ABSTRACT

The objective of the research was to achieve a non-invasive, DC-DC buck converter load current estimation technique in embedded systems. Buck converters supply power to the processor and peripherals in an embedded system. The DC supply voltage is specified and the power is dependent on the current consumed. The current consumed by the processor and peripherals is dependent on the embedded software. Hence, estimation of buck converter load current is required for embedded software power estimation and optimisation.

Current sensing techniques that exist for this purpose are invasive and require modification of hardware. A non-invasive technique to determine buck converter load current was developed in this work. A model for steady-state load current and dynamic load current was derived. The steady-state model formed the basis of the current estimation technique. The model applies Ohm's law across the inductor in the buck converter to compute the DC current. The inputs of the model are the inductor DC resistance (DCR) and the DC components of the voltages across the inductor. This includes the DC component of the switch-node voltage which is a fast-switching voltage. A low-pass filter was justified and incorporated into the technique to provide an analogue average of the switch-node voltage.

Simulations were conducted to validate the current estimation technique. Experimental characterisation and validation of the technique was conducted on a power supply module where the load resistance and current were known. The technique was applied to a dynamic load and the technique estimated the waveform of a switching DC load current with an overall error of the average current of approximately 6 %. It was shown to be applicable for use in the software power optimisation processes. The current estimation technique was tested on a single board computer and current estimation results were obtained for ten seconds of software execution for three test cases. The results of the current estimation were as expected, based on the type of software operations performed in the test cases.

This work did not include the temperature dependence of the DCR of the inductor. For future work, the effect of DCR temperature drift can be included in the model. Furthermore, automation of the data capturing process and measurement technique can be developed.

## ACKNOWLEDGEMENTS

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# 1 INTRODUCTION

## 1.1 Introduction

This chapter provides the background for the research conducted in this dissertation as well as the formulation of the research objective and a review of the relevant literature. The background includes an explanation of power consumption in embedded systems and highlights the impact of the embedded software on overall power consumption. Thereafter, background on the need for software power estimation is explained and existing methods of software power estimation are discussed. The background gives rise to the identification of a problem in the field and the research objective is formulated therefrom. Lastly, a review of relevant work, that provides possible solutions to the problem, is presented.

## 1.2 Background

### 1.2.1 Power Consumption in Embedded Systems

An embedded system is a computing system, with highly integrated hardware and software that is designed to perform a dedicated function for a specific application [1]. Embedded systems are ubiquitous in the home, work and leisure environments. Examples include appliances, auto electronics and digital cameras. An embedded system typically consists of the embedded processor, peripherals and the power supply. The embedded processor is normally a specialised processor, such as a microcontroller that has built-in integrated devices [2], [3]. Examples of peripherals are clocks, memory units and input and output devices. The complexity of an embedded system varies depending on the task for which it is designed [1].

Power in an embedded system is delivered by stepping down the primary supply voltage to the voltage requirements of the processor and peripherals. This is

typically achieved using a power management unit with built-in DC-DC converters as is shown in Figure 1.1(a). Alternatively, it is achieved using point-of-load (POL) buck converters at the loads (CPU and peripherals) as shown Figure 1.1 (b) [4]. In Figure 1.1(a), the primary voltage supply, which could be from a DC power supply, USB or a battery, is the supply voltage of the power management unit (PMU). The PMU has various DC-DC buck converters integrated within, with output voltages that meet the specifications of the loads. In Figure 1.1(b), the primary voltage supply is stepped-down by a front-end DC-DC buck converter to a distributed bus voltage. The bus voltage is the input voltage to the POL buck converters at the loads. This shows that irrespective of the adopted power supply topology in an embedded system, the power consumed by each load is typically supplied by a buck converter.

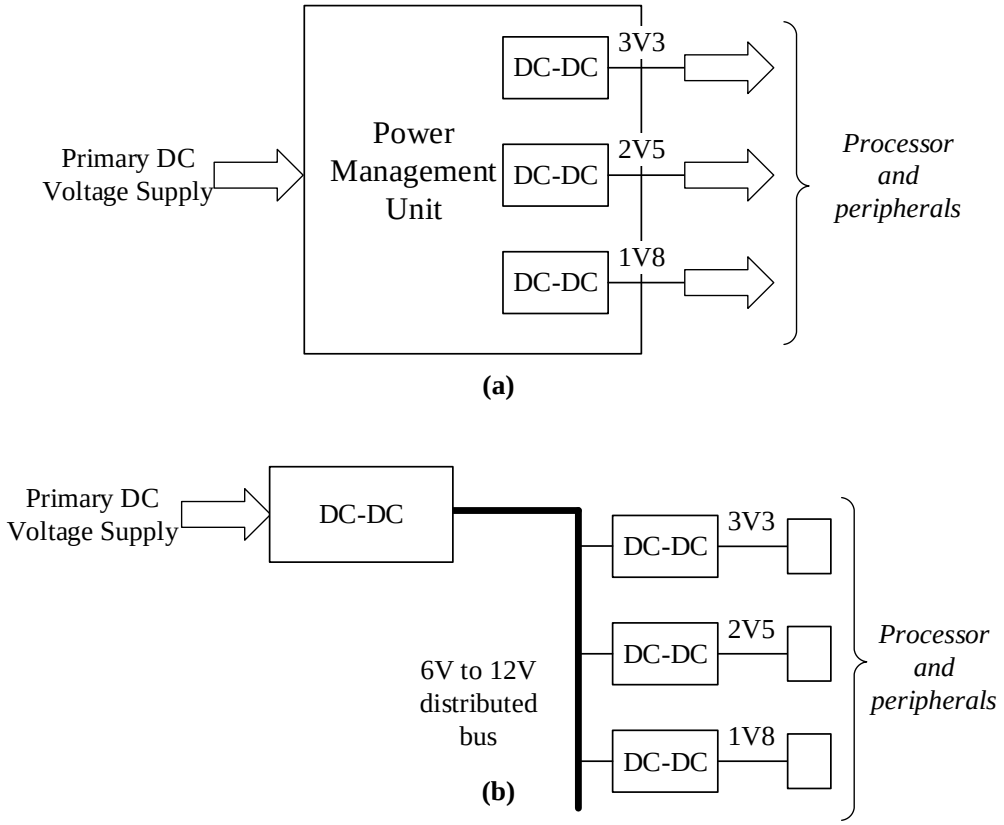



**Figure 1.1: Power delivery topologies in an embedded system**

Power consumption of the processor (or a peripheral device) in an embedded system is given by: $P = V \times I$, where $V$ is the buck converter output voltage i.e. the

supply voltage specification of the load and $I$ is the average current drawn by the load (the processor or peripheral device) . The voltage $V$ of each load remains within fixed limits and can be considered constant; therefore, the average power consumption of each load is proportional to the average current drawn by the load.

The hardware design of an embedded system contributes to the power consumption due to the overhead power cost of each load [5]. This implies that each load draws a standby current whilst switched on although it may not be performing any function. In addition to these overhead hardware power costs, software instruction execution affects power consumption. Embedded software is written in a high-level programming language which is compiled and thereafter converted into machine code that is stored in the memory of the embedded processor. The processor will execute the instructions determined by the machine code and as a result it will draw the required current and consume power. It will communicate with peripherals if necessary and these too will draw current and consume power. The design of the software thus contributes to the overall power cost by intrinsically determining when each component will draw current as well as the amount of current each load will draw.

Power consumption is a key design constraint in the development of embedded systems, particularly in battery-operated devices. Lower power consumption is desired because it is environmentally friendly since it results in less heat dissipated by a device and longer battery life. Estimating the contribution of the software to the power consumption of a component in an embedded system is necessary to minimise power consumption. This necessity is discussed in the next section.

### 1.2.2 Embedded Software Power Estimation

To minimise the power consumption in an embedded system, the hardware needs to be well designed [5] and the software written needs to run the hardware as efficiently as possible i.e. software needs to be optimised to consume minimum power. Two pieces of software code could have the same result but have different

power costs i.e. the current drawn by the processor or peripheral hardware as a result of each piece of code could differ [6]. The estimation of the software power costs is thus essential for software power optimisation.

Typically, power estimation of just the processor in an embedded system is performed for the minimisation of the processor's power cost in an embedded system. Especially in the case where embedded processors have built-in memory and on-board peripherals, the power consumed by the processor represents a significant contribution to the overall power costs in an embedded system. Measurement-based methods and simulation-based methods to estimate software power costs of embedded processors are discussed below. (In some cases, power costs of external peripherals are considered as well.)

The concept of current measurements for software power minimisation was introduced by Tiwari in [6]. The Tiwari method involved supply current measurements for the processor and memory of an embedded system, in an experimental test setup and used an ammeter to measure the supply current to the IC's. Instruction-level energy costs were determined from current measurements for an infinite loop of a given instruction and the processor's clock frequency. Current measurements for the sequential execution of two different instructions were also recorded to determine the inter-instruction energy costs. The instruction-level current measurements were used to develop an energy profile for the processor's instruction set. An energy model was developed based on these measurements. Thereafter, the energy cost of a software program was determined from its code and the energy model. From the current measurements, Tiwari achieved a significant reduction in energy cost for a test program by optimising the code.

The Tiwari method was the foundation of the work in [7]–[9], where instruction-level current measurements on a test platform were necessary for energy profiling for specific processors. Energy models for the specified processor were developed. From the energy model of the specified processor, software in an embedded system

can be optimised for the processor in an embedded system to consume minimum power.

In [10], an approach for modelling the energy consumption of a complete embedded system built around a microcontroller, a memory unit, and an A/D converter is proposed. The software tasks that were executed by the microcontroller were analysed by a profiling procedure. The energy behaviour of each component in the system both during its active state and during its standby operation were modelled. The total energy consumption was obtained by adding the individual energy amounts of these components. The limitations of measurement-based approaches are discussed in the next section because it results in the formulation of the research problem.

Simulation-based methods for processor power estimation calculates the energy consumption of code from an average current value that is assumed for each instruction cycle [11], [12]. Alternatively, the current for each instruction is approximated based on the architecture of the processor [13]. The simulation-based methods avoid instruction-level physical measurements and an approximation of the power consumed by a program is calculated. A limitation of simulation-based methods is that for a developer to optimise software in an embedded system, the developer is limited to the usage of the specific processors for which a simulation-based energy model exists.

## 1.3 Formulation of Research Objective

The problem in the field of software power optimisation stems from the limitations of the existing measurement-based approach of software power estimation. The main disadvantage is that a separate test platform is required to perform instruction-level profiling for the processor of an embedded system as mentioned in the previous section. Also, the power estimations do not include the effect of other hardware peripherals in an embedded system.

The abovementioned problem can be avoided if current measurements are performed directly on a complete embedded system rather than on just the processor or a selected peripheral on a test platform. In a complete embedded system, a piece of software can be programmed onto the processor following the complete manufacturing of the system. Measuring the average current drawn by the processor and other hardware during the software execution would allow for the average power cost of the piece of software to be determined. This is a functional-level analysis rather than instructional-level. It will avoid the need for a processor instruction-level profiling on a test platform and will provide a more robust estimation of the overall average power consumed by a piece of software in a complete embedded system.

However, the measurement-based methods are not adaptable to perform functional-level software power estimations on a complete system. The reason for this is that the current sensing techniques adopted are required to be in series with the supply as shown in Figure 1.2, on the next page. A brief review of these series techniques is:

- In Tiwari's work [6], a digital ammeter was connected in series with the microprocessor supply current path and current measurements were manually recorded.

- In [7], [10], the processor current flows through half of a *current mirror*. A current mirror consists of four transistors and duplicates the processor current through an output resistor. The details of the operation of a current mirror is presented in [14].

- In [8], a resistor was connected in series with the supply current path and the voltage across it was measured with an oscilloscope for processing.

- In [15], a current shunt amplifier (CSA) is presented. The CSA consists of a resistor in line with the supply current path and amplification circuitry

across it, which converts measured current to voltage, and later to pulse-width. The pulse-width is then measured, using a high-frequency oscillator as the reference signal and processed to calculate current.

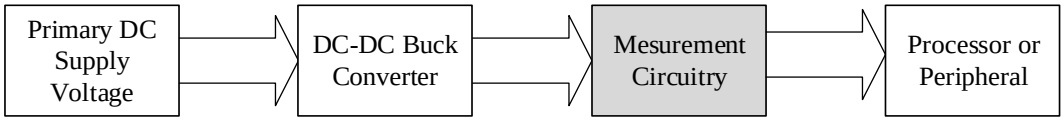



**Figure 1.2: Required placement of current sensing in a complete embedded system**

The components in an embedded system are typically surface mounted onto a PCB and the buck converter load current or processor supply current trace is usually inaccessible. If the processor supply current path is accessible, *invasive* hardware modifications would be necessary to integrate a series current sensing technique. Invasive, in this context, refers to interruption of the current carrying trace by cutting the track to connect hardware in series with the current path as shown in Figure 1.2. This is undesired, particularly in low voltage applications because it increases power loss in the system. Invasive also refers to cutting the track and extending the current path to place a sensor around the current trace. This will introduce additional noise to the system.

Hence, for a complete embedded system, software developers cannot achieve functional-level software power optimisation because the current drawn by the processor or a peripheral is not known and is not easily measurable. Typical current measurement techniques are invasive and not easily integrated onto a PCB of an embedded system. The research objective is *to find a non-invasive supply current estimation technique, for the processor (or a peripheral) in an embedded system, that does not involve cutting or modifying the processor (or peripheral) supply current-carrying trace and that can be used for software power estimation.*

Relevant non-invasive current sensing techniques that exist, but have a different purpose, are reviewed in the next section. The research methodology adopted to achieve the research objective is explained in Chapter 2.

## 1.4 Review of Non-invasive Current Sensing Techniques in DC-DC Converters

The non-invasive current sensing techniques reviewed in the subsections below are among the techniques discussed in [16]–[18]. These techniques are non-invasive *inductor current sensing* techniques used for control and protection in power electronics. They are relevant to this work because the load current in a buck converter can be approximated by the average inductor current, as will be detailed in Chapter 3. Furthermore, the inductor of a buck converter is typically accessible. This is unlike the switching and control circuitry of a buck which are typically enclosed within an IC. The inductor is external, making buck converter inductor current sensing techniques relevant for reviewing.

These techniques (reviewed in the subsections below) are usually integrated during the manufacturing process of the buck converter and are not intended for application of software power estimation in embedded systems. There is no evidence, to the authors' knowledge, of non-invasive current estimation techniques that are intended for current measurements for software power estimation in embedded systems. Thus, the techniques below will be discussed with respect to applying them to the purpose of this work. The *matched filter*, *observer* and *average inductor current sensing* techniques are reviewed below.

### 1.4.1 Matched Filter

The *matched filter* technique, shown in Figure 1.3, is used for inductor current sensing in buck converters. The nodes $v_{sw}$ and $v_{out}$ represent the switch-node and output voltage node of the buck converter, respectively. The inductor $L$ at the filter stage of a buck converter has a winding resistance, or DC resistance (DCR). This resistance is modelled by $R_L$. A low-pass RC filter is connected across the inductor as shown by $R_F$ and $C_F$.

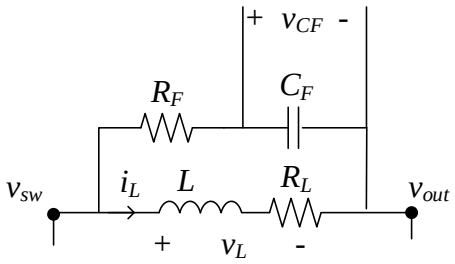



**Figure 1.3: Matched filter technique of current sensing**

Referring to Figure 1.3, the time constant $\frac{L}{R_L}$ of the inductor with its DCR is matched with the time constant $R_F C_F$ of the RC filter. Solving for the inductor voltage yields the expression in (1.1).

$$v_L = L\frac{di_L}{dt} + i_L R_L = R_F C_F \frac{dv_{CF}}{dt} + v_{CF} \tag{1.1}$$

Due to the matched time constants, $\frac{L}{R_L}$ can be substituted for $R_F C_F$ in (1.1). Also, the term $L\frac{di_L}{dt}$ in (1.1) can be multiplied by $\frac{R_L}{R_L}$. This is shown in (1.2) and is equivalent to (1.3).

$$\left(L\frac{di_L}{dt} \times \frac{\boldsymbol{R_L}}{\boldsymbol{R_L}}\right) + i_L R_L = \frac{\boldsymbol{L}}{\boldsymbol{R_L}}\frac{dv_{CF}}{dt} + v_{CF} \tag{1.2}$$

$$\Rightarrow \frac{L}{R_L}\frac{d\boldsymbol{i_L R_L}}{dt} + \boldsymbol{i_L R_L} = \frac{L}{R_L}\frac{d\boldsymbol{v_{CF}}}{dt} + \boldsymbol{v_{CF}} \tag{1.3}$$

In order for the left-hand side of (1.3) to equal to the right-hand side of (1.3), the expression in (1.4) must be true.

$$v_{CF} = i_L R_L \tag{1.4}$$

Hence, by matching the time constants, the inductor current can be inferred from the capacitor voltage. A condition for this expression to be valid is that the time constant $\frac{L}{R_L} = R_F C_F$ must be much larger than the switching period of the converter [16].

To apply this technique, firstly, the values of $L$ and $R_L$ will need to be accurately measured to calculate the time constant $\frac{L}{R_L}$ and design the matched filter. The inductor will need to be removed in order to perform these measurements. The inductance $L$ is generally known from the part number, but there is a manufacturing tolerance and it is frequency dependent. The inductance value at the converter switching frequency will need to be measured using an LCR meter. The DCR can be measured with a precision multimeter. The RC filter can then be designed based on these measurements. This is possible, but the requirement to remove and replace the inductor is a disadvantage. This issue is dealt with in [19], where the time constant $\frac{L}{R_L}$ is sensed and calibrated at startup to digitally tune the time constant of the matched filter.

Secondly, a differential voltage measurement is required across $v_{CF}$ rather than with respect to ground. This is a disadvantage because a differential voltage measurement is difficult to achieve experimentally. A differential amplifier will need to be integrated in order to measure $v_{CF}$. Alternatively, in [20], the design of the matched filter is adjusted using an operational amplifier to produce an output voltage with respect to ground. Including operational amplifiers adds sources of error and complexity to the sensing technique.

Thirdly, errors are introduced due to tolerances of the components or when the inductor DCR and $R_F$ drifts due to temperature. This causes a mismatch in the time constant. Consequently, $R_F C_F \neq \frac{L}{R_L}$ and $v_{CF} \neq i_L R_L$. An analysis on the effect of the mismatch is presented in [21] where a correction factor is derived linking $v_{CF}$ to $i_L$. Typically theses errors are included within the tolerance of the measurement technique, as reported in [20]. A digital method to overcome this problem is proposed in [22]. In [22], the controller measures the sensed capacitor voltage $v_{CF}$. during transients to detect if there is a mismatch. It is shown that a time constant mismatch can be detected from the transient response of $v_{CF}$. If a mismatch is detected, it digitally adjusts a variable resistor to match the time constants.

In general, despite being non-invasive, the matched filter technique has the above-mentioned disadvantages and sources of error. However, possible methods to overcome these are discussed above as well.

### 1.4.2 Observer Approach

The *observer* approach of inductor current sensing is presented in [23]. An operational amplifier integrator is connected across the buck converter inductor as shown in Figure 1.4. The basis of this method is the fundamental inductor voltage and current relationship in (1.5) and (1.6). The factor $\frac{1}{L}$ is multiplied to the output of the differential amplifier to obtain the inductor current waveform.

$$v_L = L\frac{di_L}{dt} \tag{1.5}$$

$$i_L = \frac{1}{L}\int v_L dt \tag{1.6}$$

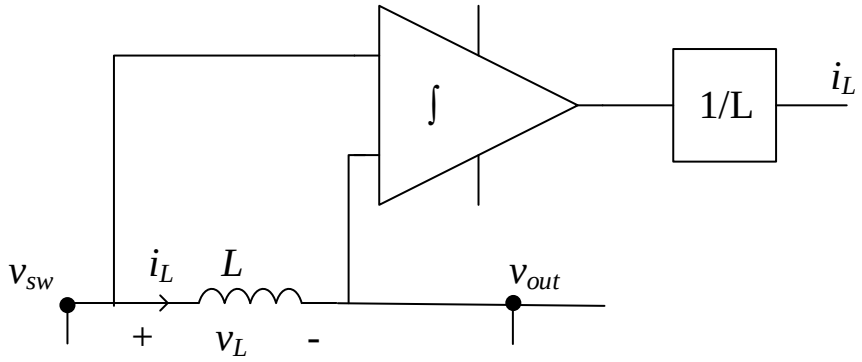



**Figure 1.4: Observer approach to inductor current sensing**

This technique relies on the knowledge of the inductance *L*. As in the previous review, an accurate measurement of the inductance can be achieved by removing the inductor. Alternatively, the inductance from the datasheet can be used and the tolerance of the inductance will impact the measurement.

The assumption is that the inductor DCR is negligible and the output waveform is equivalent to the inductor current. However, as shown in the previous section $v_L =$

$L\frac{di_L}{dt} + i_L R_L$. Integrating and multiplying by $\frac{1}{L}$ will result in an output equal to $i_L + \frac{R_L}{L}\int i_L dt$, thus introducing an offset error.

This technique can be applied to an embedded system. The impact of the error term $\frac{R_L}{L}\int i_L dt$ on the measurement can be experimentally determined and the tolerance of the measurement can be measured.

### 1.4.3 Average Current Sensing

The current sensing scheme adopted in [24] is shown in Figure 1.5. The nodes $v_{sw}$ and $v_{out}$ represent the switch-node and output voltage node of the buck converter, respectively. The inductor and its DCR are represented by $L$ and $R_L$ respectively. A low-pass RC filter with cut-off frequency $\frac{1}{R_F C_F}$ is connected at the switch-node of the buck. The circuit analysis in [24] shows that the *average* inductor current $I_L$ is given by (1.7), where $V_{CF}$ is the *average* capacitor voltage and $V_{out}$ is the DC output voltage of the buck converter. As mentioned in the beginning of this section, the average inductor current in a buck converter is equivalent to the load current.

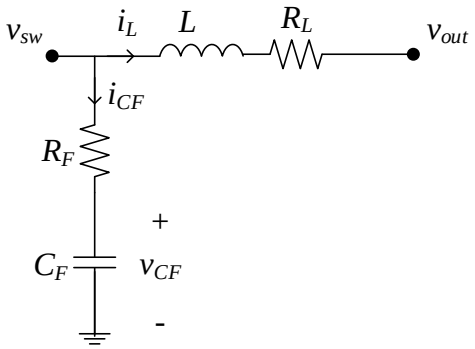



**Figure 1.5: Average current sensing technique**

$$I_L = \frac{V_{CF} - V_{out}}{R_L} \quad (1.7)$$

An observation from Figure 1.5, is that the switch-node voltage signal $v_{SW}$ is the input to the low-pass filter created by $R_F C_F$. The output of the filter is the capacitor voltage $v_{CF}$. It can be deduced that the average capacitor voltage $V_{CF}$ from expression (1.7) is equivalent to the DC component of the switch-node voltage. This is explained as follows. In an ideal buck converter, the switch-node voltage waveform is a switched voltage signal, as shown in Figure 1.6. In Figure 1.6, the duty cycle of the converter is denoted by $D$, the switching period is denoted by $T_s$ and the input voltage of the converter is given by $V_{in}$. The dashed line representing the DC component of the switch-node voltage is explained below the figure.

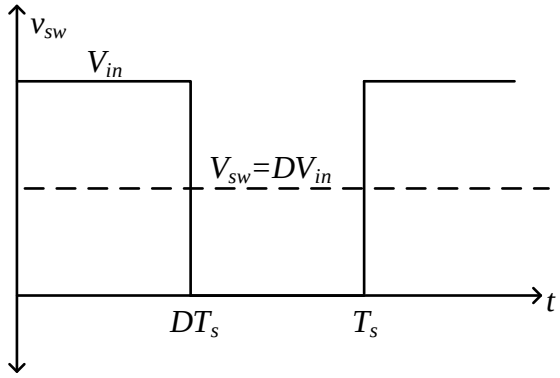



**Figure 1.6: Ideal switch-node voltage in a buck converter**

The mathematical expression for the average of a periodic signal $x(t)$ with period $T$ is given by $\langle x(t) \rangle$ in (1.8).

$$\langle x(t) \rangle = \frac{1}{T} \int_0^T x(t) dt \tag{1.8}$$

From (1.8), the average switch-node voltage is given in (1.9). Since the average of a periodic signal is equivalent to its DC component [25], the result in (1.9) is the DC component of the switch-node voltage denoted by $V_{sw}$. It is solved in (1.10) and is indicated by the dashed line on the waveform in Figure 1.6

$$\langle v_{sw}(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_{sw}(t) dt \tag{1.9}$$

$$\langle v_{sw}(t) \rangle = V_{sw} = \frac{1}{T_s} ( DT_s V_{in} ) = DV_{in} \tag{1.10}$$

Filtering the switch-node voltage through the low-pass $R_F C_F$ filter results in the filter output voltage waveform $v_{CF}$ given in [24], shown in Figure 1.7. The peak-to-peak voltage or ripple $\Delta v_{CF}$ is dependent on the time constant $R_F C_F$ which controls the low-pass filter cut-off frequency $\frac{1}{R_F C_F}$. The time constant is required to be larger than the switching period $T_s$ to achieve the shape of $v_{CF}$ shown in Figure 1.7 . The larger the time constant (the lower the cut-off frequency of the low-pass filter), the smaller the peak-to-peak or ripple voltage. The DC component or average of the input signal $V_{SW}$ from (1.10) is maintained at the output and is thus equivalent to $V_{CF}$.

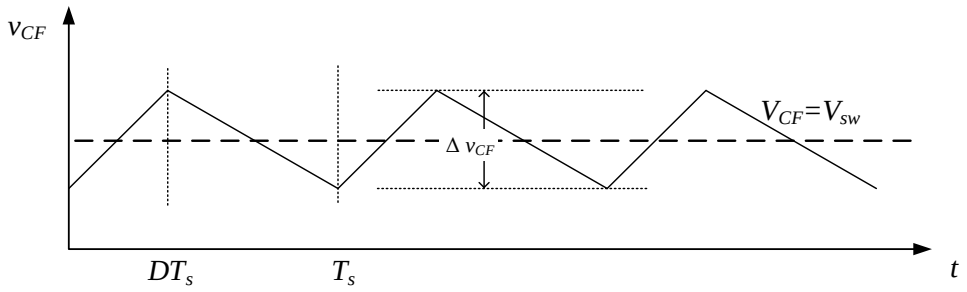



**Figure 1.7: Low-pass filter capacitor voltage from the average inductor current sensing technique**

Hence, the average output voltage of the low-pass filter $V_{CF}$ is the average of the switch-node voltage i.e. $V_{CF} = V_{SW}$. This implies that the original expression in (1.7) that defines the *average current sensing* technique can be expressed by (1.11). From the circuit in Figure 1.5, this appears to be Ohm's law across the inductor using average voltages. (The detailed derivation of this relationship is shown in Chapter 3.)

$$I_L = \frac{V_{sw} - V_{out}}{R_L} \tag{1.11}$$

From the work in [24], $V_{CF}$ essentially provides an analogue average of the switch-node voltage for (1.11) to be computed.

## 1.5 Conclusion

In summary, this chapter provides some background, formulates the research objective and reviews work relevant to the research conducted in this dissertation. The background for this work includes an explanation of how power is consumed in embedded systems. Background on the importance of software power estimation and the techniques that are currently adopted to achieve it are discussed. The problem in the field is identified from the existing current estimation techniques for software power estimation. The problem is that existing techniques are invasive and are not applicable on complete embedded systems. The research objective is to find a non-invasive technique for current estimation in embedded systems that can be used for software power estimation. Existing non-invasive current sensing techniques for control in DC-DC converter control are reviewed for applicability to the research objective. The next chapter presents the methodology that was adopted to achieve the research objective.

# 2 RESEARCH METHODOLOGY

## 2.1 Introduction

The objective of this work was to find a non-invasive current estimation technique for the supply current of the processor or peripheral in an embedded system. This chapter explains the steps that were taken to achieve the research objective.

The steps that were taken to achieve the objective is shown in Figure 2.1. The non-invasive current estimation technique was developed by firstly modelling the buck converter that delivers power to the processor or peripheral. Thereafter, for the second phase of the development of the current estimation technique, a low-pass filter, was designed and tested. The developed technique was then simulated and experimentally tested.

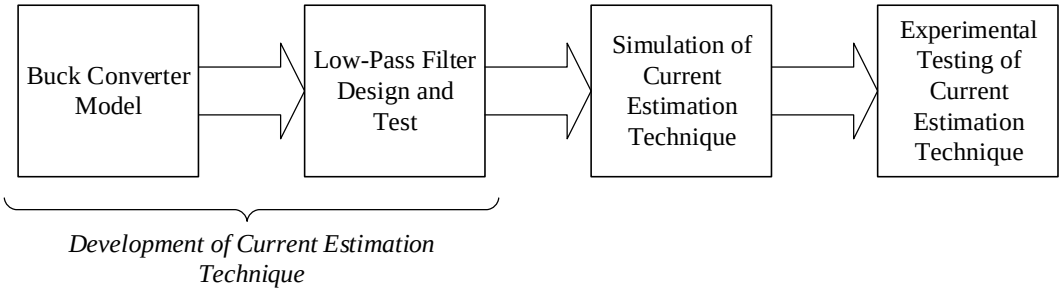



**Figure 2.1: Procedure followed to achieve the research objective**

The progression of the steps shown in Figure 2.1 are from standard engineering practices, i.e. design from theoretical knowledge, simulate and experimentally test. This methodology is valid because it leads to the solution of a problem that has been established. According to Vincenti in [26], this is the criterion for validity of knowledge in engineering. This also applies if the results from the experimental testing does not validate the design. The knowledge produced is nevertheless new and is considered useful.

Each of these steps shown in Figure 2.1 is explained separately, in detail, in the following sections of this chapter.

## 2.2 Buck Converter Model Development

The first step in the research procedure was to develop a model of the buck converter that supplies power to the processor or peripheral in an embedded system. The buck converter load current is the supply current of the processor or peripheral as discussed in Section 1.2.1 in Chapter 1. The intention was that, by deriving a mathematical and an equivalent circuit model of the buck converter, the load current can be approximated in terms of other parameters, that perhaps could be measured non-invasively or modelled themselves. This would then give rise to a non-invasive current estimation technique for the buck converter load current.

Also, in Section 1.4 in Chapter 1, non-invasive *inductor* current sensing techniques in DC-DC converters were discussed. The understanding was that buck converter load current can be approximated by the average inductor current. This was also to be confirmed in the model.

In general, when performing electronics modelling or analysis, it is common practice that the DC and AC behaviours are studied. Therefore, a steady-state and a dynamic model of the load current in a buck converter was derived based on techniques established in [27]. Mathematical and equivalent circuit models were derived. The model boundary conditions, a detailed step-by-step derivation, a discussion on the model application and its exclusions is shown in Chapter 3.

The expression in (1.11) for average inductor current from *the average current sensing technique* [24] was validated by the model in Chapter 3. The load current in the model was dependent on three parameters. Two of the parameters were easily obtainable by non-invasive methods, whilst one required the non-invasive integration of a low-pass filter. This led to the next step in the development of the current estimation technique that is discussed in the next section.

## 2.3 Low-Pass Filter Design and Testing

From the steady-state model of the buck converter, an expression for load current that was dependent on three parameters was derived. One of the parameters (the switch-node voltage, explained in Chapters 3 and 4) required its average value to be estimated. The low-pass filter was required to provide an estimated average of this parameter. The reason for selecting a filter to perform averaging is due to data sampling limitations of the oscilloscope. This justification is explained in Chapter 4.

In *the average current sensing technique* [24], discussed in in Section 1.4 in Chapter 1, a filter is also implemented for averaging. However, it was for the purpose of control in a buck converter and a simple first order filter was sufficient. In this work, the purpose was for estimating load current and a higher order filter was required. An explanation of this and the design of the filter is presented in Chapter 4.

Lastly, as an isolated device, the filter was tested experimentally. The frequency response of the filter was plotted to validate its design. The DC response was plotted to determine the DC gain and offset that were present. Since the input of the filter, for the purpose of this work, was a pulsed voltage (the switch-node voltage, explained in Chapters 3 and 4), the pulse-train response at a typical switching frequency was performed to validate the frequency and DC responses of the filter. The experimental testing is detailed in Chapter 4.

## 2.4 Simulation of the Current Estimation Technique

The non-invasive current estimation technique incorporated the steady-state model of the buck converter (derived in Chapter 3) and the low-pass filter (designed in Chapter 4.) The next step of the procedure was to validate the technique by testing it in a simulation environment. Since simulations are based on mathematical models

of the circuit components, its results can be used to validate the design of the current estimation technique.

In *LTSpice* [28], a simulation circuit of the low-pass filter was integrated with the simulation circuit of a buck converter. The buck converter was simulated under various load conditions and the current estimation technique was tested to determine if it could estimate the current.

The load conditions that were simulated are: a DC load, two AC load conditions and a transient load. The DC load was simulated to validate the technique for steady-state load current. For AC loads, the model in Chapter 3 had a frequency limitation. Therefore, a low frequency AC load was simulated below the frequency threshold and a high frequency AC load was simulated above the threshold frequency. This was to validate the AC model and its frequency limitation. The transient load was simulated to analyse the effects of a load transient on the current estimation technique.

## 2.5 Experimental Testing of the Current Estimation Technique

The last stage of the research procedure was to perform experimental validation of the current estimation technique. Two phases of experimental validation were conducted:

Physical circuit measurements on a test device with a controllable load was performed. The test device was a synchronous buck within a *Power Supply Module* which allows for a known load to be connected at the output. The load current was computed, and the current estimation technique was used to estimate the load current. The accuracy of the current estimation technique was measured for fixed loads and switching loads. The experiments are described and the results are shown in Chapter 6.

The measurement technique was applied in a real-life test case embedded system, with the load of the buck converter being an actual processor running software operations. The processor current was estimated for various software benchmark tests. The benchmark test cases of the test device were standby mode, memory write operations and 3D graphics operation. It was expected that the current consumption would be the lowest for standby mode and highest for displaying 3D graphics. In Chapter 7, the experimental setup and procedure are explained and the results are discussed.

## 2.6 Conclusion

The procedure followed in this work consisted of development, simulation and experimental testing of a non-invasive current estimation technique for buck converter load current. This is in accordance with standard engineering practice. The development of the technique consisted of the derivation of the steady-state and dynamic model of the load current in a buck converter as well as the design and testing of a low-pass filter. Simulation of the technique was performed in *LTSpice* [28] and experimental validation was performed on physical circuits. The subsequent chapters hereafter, detail each step of the research procedure.

# 3 DC-DC BUCK CONVERTER LOAD CURRENT MODEL

## 3.1 Introduction

In this chapter, a mathematical model for a DC and AC load current is derived. The load current is also represented within an equivalent circuit model of the buck converter. The model boundary conditions are described, and the detailed derivation of the steady-state and dynamic load current models is presented. The application of the model to the research problem is explained. Lastly, the rationale behind certain model exclusions is discussed.

## 3.2 Model Boundary Conditions

For the purpose of this work, the model development will be restricted to synchronous buck converters operating in continuous conduction mode (CCM).

The reason for these boundary conditions is because synchronous buck converters operating in CCM [29], [30] are typical in low voltage applications such as mobile embedded systems. Synchronous bucks are typical because they are more efficient than non-synchronous buck converters [31]. Hence it is the load current of a synchronous buck converter that will typically supply the loads in an embedded system. Therefore, the model is based on a synchronous buck converter. The operation of a synchronous buck converter is explained in the first subsection below.

The operating condition CCM is typical in synchronous buck converters whereas the converse, discontinuous conduction mode (DCM) is typical in non-synchronous buck converters [29], [30]. Since the model is restricted to synchronous buck converters, the operating mode of CCM is the second boundary condition. A description of the CCM operation is explained in the second subsection below.

### 3.2.1 Operation of a Synchronous Buck Converter

A synchronous buck converter circuit appears in Figure 3.1 [32]. The voltage $V_{in}$ is the DC input voltage to the converter. The switching circuit consists of two fast-switching MOSFETs. The MOSFET switches are controlled by a PWM signal, with duty cycle $D$, to synchronously switch on and off with a period $T_s$, called the switching period. The high-side MOSFET($Q_1$) switches on for the duration of the period $DT_s$ and the low-side MOSFET($Q_2$) switches on for the remaining duration $(1-D)T_s$ or $D'T_s$, where $0 < D < 1$ and $D' = 1 - D$. This results in a pulse train signal i.e. a periodically switched signal, $v_{sw}$ at the switch-node of the converter (the node between the two MOSFET switches). This signal will be shown in the model derivation in the next section. It is passed through a low-pass *LC* filter to filter out switching harmonics and obtain the required stepped down DC component of the output voltage $V_{out}$. An explanation of the operation of the control system follows Figure 3.1.

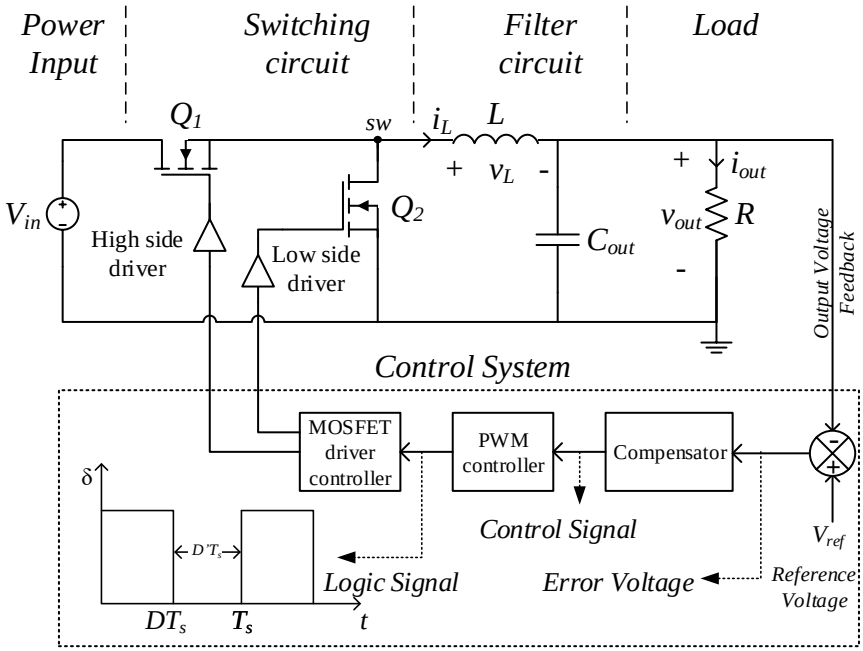



**Figure 3.1: Synchronous buck converter circuit**

The output voltage $v_{out}$ is predominantly a DC voltage $V_{out}$ with some small AC ripple at the switching frequency. Ideally, $V_{out}$ is given by $DV_{in}$. However, system

losses, load fluctuations or source voltage fluctuations cause $V_{out}$ to deviate from its designed value. The feedback loop created between the output voltage and the control system allows the control system to detect if there is an error in the output voltage from the designed output. It uses a reference voltage $V_{ref}$ to determine the error voltage and employs either voltage-mode control or current-mode control to adjust the duty cycle in order to maintain the output voltage at the required level [33], [34].

The control system in Figure 3.1 employs voltage mode control. The error voltage is the input to a compensator that generates the control signal required to adjust the duty cycle. The control signal determines the pulse-width of the PWM signal that controls the MOSFET drivers via a controller. The MOSFET driver controller controls the high-side MOSFET driver to switch on the high-side MOSFET during the interval $DT_s$ . It also controls the low-side MOSFET driver to switch on during the interval $D'T_s$. There is typically a short period of dead time, before either MOSFET conducts, during which neither MOSFET conducts. This is to avoid the possibility of both MOSFETS conducting and the input voltage being shorted. This dead time is also controlled by the MOSFET driver controller [35]. If current-mode control is employed, a sensed current is included in the control system [35].

### 3.2.2 Description of CCM

Referring to the circuit from Figure 3.1, CCM implies that the inductor current $i_L$ is continuous for all output currents $i_{out}$ as shown in Figure 3.2. This is explained as follows. During each interval $DT_s$ of the switching period, the inductor voltage is positive and thus the inductor current slope $\frac{di_L}{dt} = \frac{v_L}{L}$ is positive. (The inductor voltage waveform will be shown in the model derivation in the next section.) During the interval $D'T_s$, the inductor voltage is negative and $\frac{di_L}{dt}$ is negative. This creates a triangular waveform for the inductor current with DC component $I_L$. The AC component of the current apparently "flows through" the output capacitor $C_{out}$ whilst the DC component $I_L$ flows through the output load $R$. This is due to the

principle of capacitor-charge balance that is valid in steady-state [36]. The principle states that the average current in the output capacitor in steady-state is zero. Hence, in steady-state ideally, $I_L = i_{out}$. The difference between DCM and CCM can be is explained when the output current is low. An explanation on the inductor current waveform when the output current is low appears below Figure 3.2.

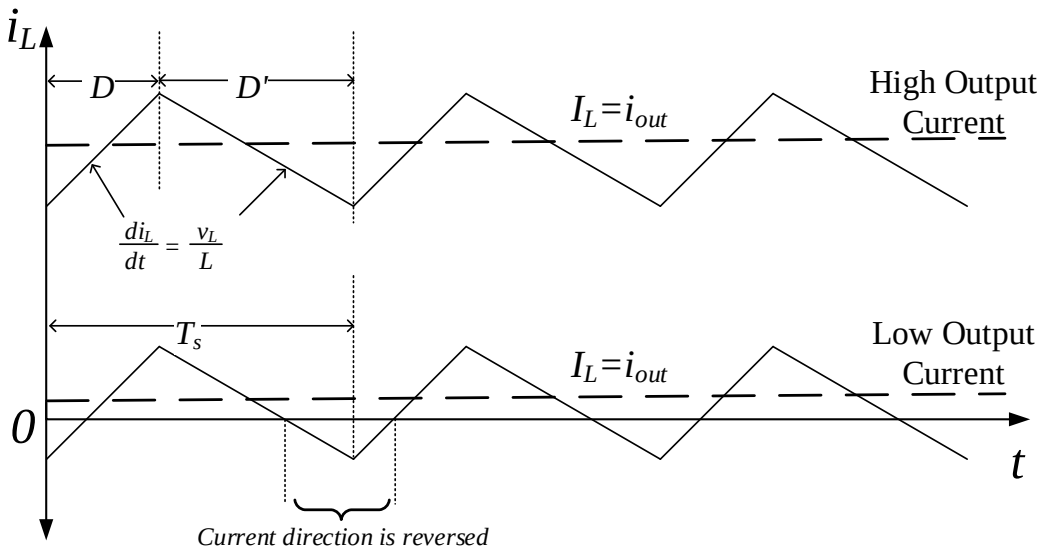



**Figure 3.2: Steady-state inductor current waveform for high and low output currents in a synchronous buck converter**

When the load current is low, the average inductor current is also low and the current reverses direction for a portion of the switching period as shown in Figure 3.2. This is unlike the discontinuous conduction mode (DCM) case, where for low output currents, instead of reversing direction, the inductor current becomes discontinuous or zero for that portion of the switching period where the sign of the current is reversed. Typically, synchronous bucks operate in CCM and it's non-synchronous bucks that operate in DCM at low load currents [37] (a non-synchronous buck replaces the low-side MOSFET with a diode). However, some synchronous buck controllers enable DCM for a synchronous buck. The model derived in this chapter applies to a synchronous buck operating in CCM.

## 3.3 Model Derivation

### 3.3.1 Steady-State Load Model

***Defining the Load Current and Inductor Current***

A synchronous buck converter, with switching period $T_s$, operating in steady-state is shown in Figure 3.3. The load $R$ is a constant load that draws a constant current $i_{out}$. As described earlier, in steady-state, the DC load or output current is equivalent to the DC component $I_L$ of the inductor current $i_L$ as shown in Figure 3.4. The buck converter steady-state load current modelling approach is explained below. Thereafter, each step of the derivation of the model is shown.

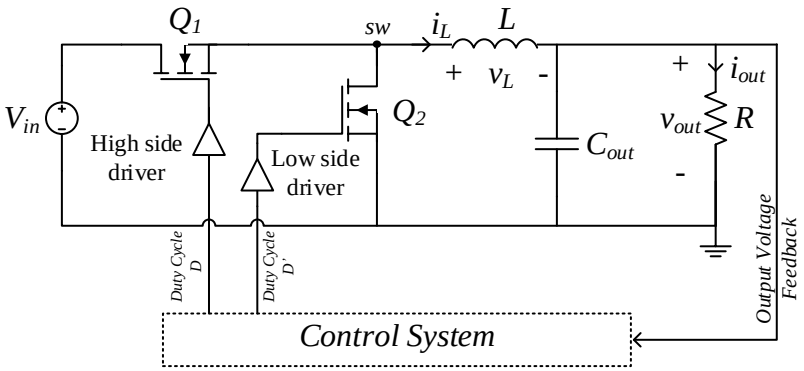



**Figure 3.3: Synchronous buck converter in steady-state**

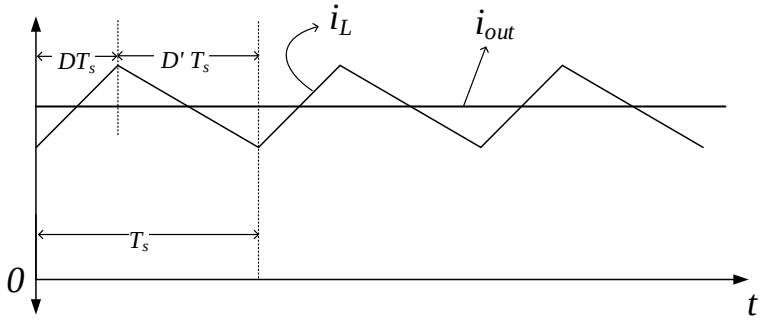



**Figure 3.4: Output load current and inductor current waveform in steady-state**

***Steady-State Modelling Approach***

The steady-state modelling approach below is adapted from the method presented in [38]. In [38], this approach forms a part of the method used by Erickson in the development of the *DC Transformer Model* of a buck converter. In this work, the approach is used to develop the load current model of a buck converter. The approach is described hereunder and each step is shown separately thereafter.

1) For one switching period, consider the intervals $DT_s$ and $D'T_s$ separately. Represent the buck converter by its equivalent circuits during the intervals $DT_s$ and $D'T_s$. Include the drain-source conduction losses of the MOSFETS and the inductor DCR in the equivalent circuits.
2) From each equivalent circuit, derive the expression for the inductor voltage $v_L$.
3) Simplify the expressions for $v_L$ by applying the *small- ripple approximation* to the steady-state output voltage and the steady-state inductor current. This means approximating that the output voltage is approximately equal to its DC component $V_{out}$ and the inductor current is estimated by its DC component $I_L$ [36].
4) Use the expressions for $v_L$ to obtain the inductor voltage waveform in steady-state.
5) Apply the principle of *inductor volt-second balance* to the inductor voltage waveform. The principle states that the average value of the inductor voltage $v_L$ in steady-state is zero [36]. This principle can be proven by integrating the fundamental inductor voltage and current relationship over one switching period, for example between 0 and $T_s$ as shown in (3.1).

$$\int_0^{T_s} v_L dt = \int_0^{T_s} L \frac{di_L}{dt} dt \tag{3.1}$$

This yields the result in (3.2).:

$$\frac{1}{L}\int_0^{T_s} v_L dt = i(T_s) - i(0) \tag{3.2}$$

From the steady-state inductor current waveform in Figure 3.4, the net change in inductor current, $i(T_s) - i(0)$, for one switching period, is zero. This means that the integral from (3.2) can be expressed as shown in (3.3):

$$\int_0^{T_s} v_L dt = 0 \tag{3.3}$$

Given that the average or DC component of a periodic signal $x(t)$ with period $T$ is given by $\langle x(t) \rangle$ in (3.4), the expression in (3.5) defines the principle of *inductor volt-second balance.*

$$\langle x(t) \rangle = \frac{1}{T} \int_0^T x(t) dt \tag{3.4}$$

$$\therefore \langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L dt = 0 \tag{3.5}$$

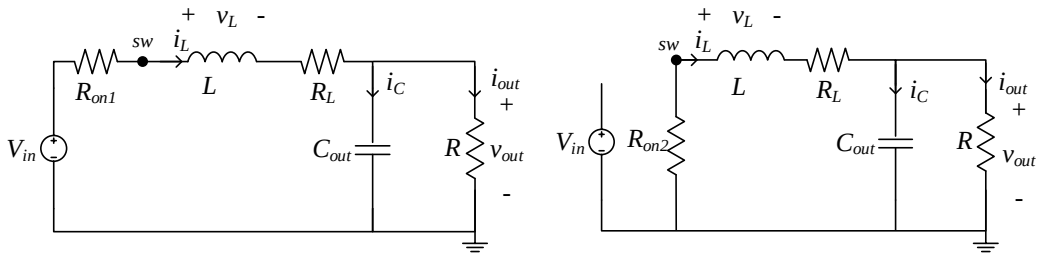
To apply this principle, compute the average inductor voltage from the waveform and equate it to zero.

6) Simplify the average inductor voltage expression by substituting the average switch-node voltage expression into the average inductor voltage expression. This step is unique to this work and is not included in [38]. It is substantiated further in the *Step Six* subsection below.
7) Represent the average inductor voltage expression from the previous step by an equivalent circuit and solve for average inductor current $I_L$ (which has been previously established to be equivalent to the steady-state load current).

***Step One: Equivalent Circuits of Synchronous Buck in Steady-State***

The equivalent circuits of a synchronous buck converter during one switching event with period $T_s$ is shown in Figure 3.5. The equivalent circuit for the portion of the period $DT_s$, when the high-side MOSFET conducts is shown in Figure 3.5 (a) and the equivalent circuit for the portion $D'T_s$, when the low-side MOSFET conducts is shown in Figure 3.5 (b). Due to the forward drain-source voltage that is seen across a MOSFET during conduction, the high and low-side MOSFETs are modelled by resistors with resistances $R_{on1}$ and $R_{on2}$, respectively. These are referred to as on-resistances. The inductor DCR is modelled by resistance $R_L$. Typically, there is a short period of dead time between these two circuits during which neither MOSFET

conducts. This is to avoid the possibility of both MOSFETS conducting and the input voltage being shorted. The dead time is typically much smaller than the switching period and the effect on the model will be neglected.




(a)High-Side MOSFET conducting (b) Low-Side MOSFET conducting

**Figure 3.5: Equivalent circuits of a synchronous buck converter during one switching event in steady-state**

***Step Two: Inductor Voltage Expressions in Steady-Sate***

From the equivalent circuit in Figure 3.5 (a), when the high-side MOSFET conducts, the inductor voltage is given by:

$$v_L = V_{in} - i_L R_{on1} - i_L R_L - v_{out} \tag{3.6}$$

From the equivalent circuit in Figure 3.5 (b), when the low-side MOSFET conducts, the inductor voltage is given by:

$$v_L = -i_L R_{on2} - i_L R_L - v_{out} \tag{3.7}$$

***Step Three: Small-Ripple Approximation***

The *small-ripple* approximation made by Erickson in [38] is the approximation that the AC ripple in the inductor current and the AC ripple the output voltage are small in comparison to the DC components [36].

The peak-to-peak voltage of steady-state inductor current shown in Figure 3.2, is given by $\frac{v_L}{L} DT_s$ where $v_L$is given by (3.6) above. The ripple is thus determined by the inductance $L$. The ripple is typically designed to be small in comparison to the DC component and is usually designed to be between 10 % and 20% of the full load

current [36]. Particularly in embedded systems, designing the buck with an inductor ripple current that is too high is undesirable because it increases the peak current requirements in the semiconductor devices, hence requiring larger devices [36]. Therefore, it is usually justified to approximate the inductor current by its DC component:

$$i_L \approx I_L \tag{3.8}$$

The output voltage $v_{out}$ is predominantly a DC voltage $V_{out}$ with some small AC ripple at the switching frequency [36]. The small ripple is typically much smaller than the DC component and is usually designed to be less than 1% of the designed output voltage [36]. The output voltage is thus also approximated by its DC component:

$$v_{out} \approx V_{out} \tag{3.9}$$

The above approximations simplify the inductor voltage expressions from the previous step. The simplified inductor voltage is given by (3.10) when the high-side MOSFET conducts and (3.11) when the low-side MOSFET conducts:

$$v_L \approx V_{in} - I_L R_{on1} - I_L R_L - V_{out} \tag{3.10}$$

$$v_L \approx -I_L R_{on2} - I_L R_L - V_{out} \tag{3.11}$$

***Step Four: Inductor Voltage Waveform in Steady-Sate***

From the expressions in (3.10) and (3.11), the inductor voltage waveform for one switching period is given in Figure 3.6, on the next page. The shaded area is explained in the next step.

***Step Five: Average Inductor Voltage Expression in Steady-State***

Recall, from the *Modelling Approach* subsection, that the average inductor voltage is given by (3.5), repeated below. This is the principle of *inductor volt-second balance* [36]. The integral in (3.5) can be computed from the inductor voltage waveform in Figure 3.6 by calculating the area under the curve as shown in (3.12).

$$\langle v_L \rangle = \frac{1}{T_s}\int_0^{T_s} v_L dt = 0 \qquad (3.5)$$

$$\langle v_L \rangle \approx \frac{1}{T_s}(Area\ under\ the\ v_L\ curve\ for\ one\ switching\ period) \approx 0$$

$$\langle v_L \rangle \approx \frac{1}{T_s}\left(DT_s(V_{in} - I_L R_{on1} - I_L R_L - V_{out}) + D'T_s(-I_L R_{on2} - I_L R_L - V_{out})\right) \approx 0$$

$$\langle v_L \rangle \approx D(V_{in} - I_L R_{on1} - I_L R_L - V_{out}) + D'(-I_L R_{on2} - I_L R_L - V_{out}) \approx 0 \qquad (3.12)$$

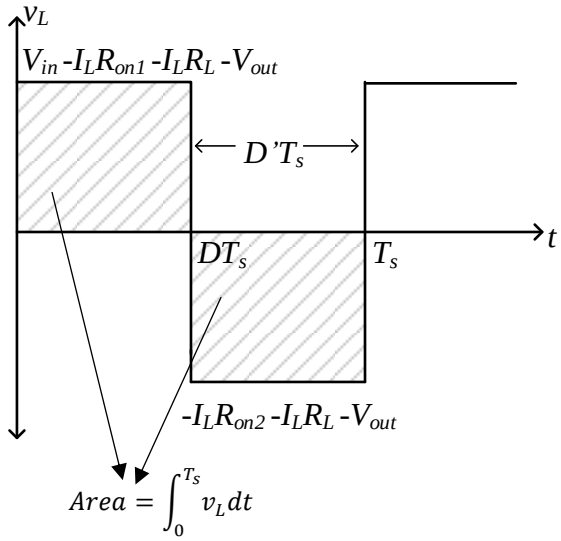



**Figure 3.6: Inductor voltage waveform in steady-state showing the area under the curve**

***Step Six: Simplify Average Inductor Voltage Expression in Steady-State***

The reason for this step is to simplify the average inductor voltage expression $\langle v_L \rangle$ from the previous step in (3.12). The expression is dependent on duty cycle *D* and MOSFET on-resistances $R_{on1}$ and $R_{on2}$. These parameters are challenging to measure and are explained below.

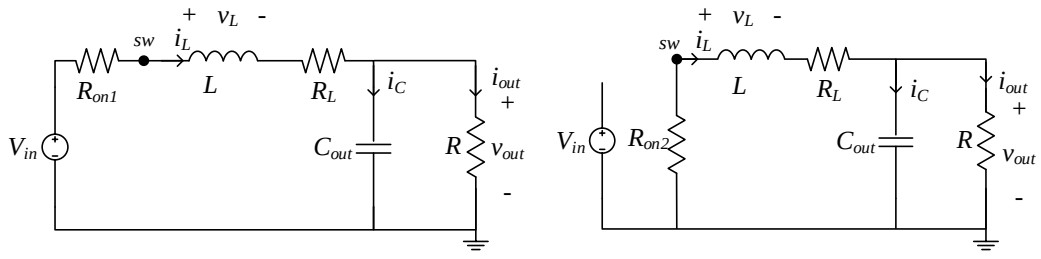
The duty cycle measurement is not easily measurable. Consider the example of two different steady-state currents, that correspond to two different duty cycles. Since the switching frequencies are usually high (say 1 *MHz)*, the switching period is very small (1 $\mu s$). The difference in the two duty cycles would be very small, much

smaller than the switching period (typically in the *ns* range). Measuring this difference in the time domain, would be dependent on the sampling frequency of the oscilloscope that is used to obtain the measurement.

The MOSFET on-resistances are also not easily measurable. The MOSFETs are typically enclosed within an IC and their on-resistances cannot be directly measured. Estimating their on-resistances would require precise calibration of the buck converter circuit.

Simplifying the average inductor voltage expression $\langle v_L \rangle$ in (3.12) by replacing the abovementioned parameters ($D, R_{on1}, R_{on2}$) with a single parameter will eliminate the need for the above-mentioned procedures. The procedures can be replaced by a single procedure to determine the simplified parameter. The simplification is shown below.

The average inductor voltage expression $\langle v_L \rangle$ can be simplified by substituting the average switch-node voltage $\langle v_{sw} \rangle$ into (3.12). The average switch-node voltage $\langle v_{sw} \rangle$ is determined from the equivalent circuits during each switching interval repeated below in Figure 3.7.




(a)High Side MOSFET conducting (b) Low Side MOSFET conducting

**Figure 3.7: Equivalent circuits of a synchronous buck converter during one switching event**

Applying the *small- ripple approximation* for inductor current, $i_L$ in Figure 3.7 is replaced with $I_L$. The switch-node voltage $\langle v_{sw} \rangle$ is then given by $V_{in} - I_L R_{on1}$ when the high-side MOSFET conducts. When the low-side MOSFET conducts, it is given

by $-I_L R_{on2}$. This yields the switch-node voltage waveform in Figure 3.8. The average or DC component of the switch-node voltage is given by (3.13) by equating the integral to the area under the curve from Figure 3.8.

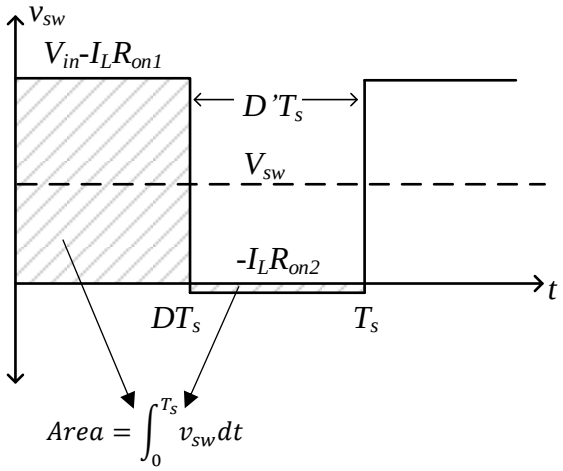



**Figure 3.8: Switch-node voltage waveform for a synchronous buck converter**

$$\begin{aligned}\langle v_{sw} \rangle = V_{sw} &= \frac{1}{T_s}\int_0^{T_s} v_{sw}\,dt \\ &\approx \frac{1}{T_s}(Area\ under\ \ v_{sw}\ curve\ for\ one\ period) \\ &\approx \frac{1}{T_s}\big(DT_s(V_{in} - I_L R_{on1}) + D'T_s(-I_L R_{on2})\big) \\ &\approx \big(D(V_{in} - I_L R_{on1}) + D'(-I_L R_{on2})\big)\end{aligned} \tag{3.13}$$

The inductor voltage expression derived in the previous step in (3.12) is repeated below. Rearranging (3.12) shows that the average switch-node voltage in (3.13), above, can be substituted into (3.12) as shown below.

$$\begin{aligned}\langle v_L \rangle &\approx \frac{1}{T_s}\big(DT_s(V_{in} - I_L R_{on1} - I_L R_L - V_{out}) + D'T_s(-I_L R_{on2} - I_L R_L - V_{out})\big) \\ &\approx \frac{1}{T_s}\big[\big(DT_s(V_{in} - I_L R_{on1}) + D'T_s(-I_L R_{on2})\big) + (DT_s + D'T_s)(-V_{out} - I_L R_L)\big] \\ &\approx \underbrace{\big(D(V_{in} - I_L R_{on1}) + D'(-I_L R_{on2})\big)}_{\langle v_{sw} \rangle} + \underbrace{(D + D')}_{1}(-I_L R_L - V_{out})\end{aligned} \tag{3.12}$$

This simplifies the average inductor voltage expression from (3.12) in the previous step to the expression in (3.14) below:

$$\langle v_L \rangle \approx \langle v_{sw} \rangle - I_L R_L - V_{out} \approx 0 \tag{3.14}$$

The advantage of this step is that it eliminates the duty cycle as well as the MOSFET on-resistances from the expression (and hence removes it from the model shown in the next step).

***Step Seven: Obtain Steady-State Load Current Equivalent Circuit Model and Expression***

The expression for average inductor voltage in (3.14) from the previous step can be expressed by an equivalent circuit as shown in Figure 3.9 where $V_{sw}$ is the DC component (average) of the switch-node voltage i.e. $\langle v_{sw} \rangle$. Solving for the current $I_L$ in (3.14) or in Figure 3.9 yields the model for the steady-state output or load current of the buck converter given in (3.15). Recall that in steady-state, the DC component of the inductor current $I_L$ is the buck converter load current $i_{out}$.

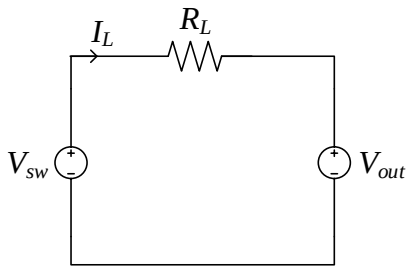



**Figure 3.9: Equivalent circuit model of the buck converter for steady-state load current**

$$i_{out} = I_L \approx \frac{1}{R_L}(V_{sw} - V_{out}) \tag{3.15}$$

This linear result essentially yields Ohm's law across the inductor for the DC components of the current and voltage signals. It shows that, given the inductor DCR and the average voltages $V_{sw}$ and $V_{out}$, the steady-state load current can be

computed. This result is consistent with the average inductor current expression in (1.11) from the literature review in Section 1.3.2 in the previous chapter.

### 3.3.2 Dynamic Load Model

***Defining the Load Current and Inductor Current***

A synchronous buck converter, with switching period $T_s$, with a dynamic or time-varying load is shown in Figure 3.10. Suppose that the dynamic load results in a time-varying output load current $i_{out}(t)$ defined in (3.16)

The output current $i_{out}(t)$ from (3.16) consists of its DC component $I_{out}$ and a superimposed sinusoidal modulation current denoted by $\hat{\imath}(t)$where $\hat{\imath}(t) = I_m \sin(\omega_m t)$. This is shown in Figure 3.11. The amplitude of the modulated output current signal is $I_m$ and $\omega_m = 2\pi f_m$ defines the modulation frequency. The corresponding inductor current waveform $i_L(t)$ is given by the waveform shown in Figure 3.11. The DC components $I_{out}$ and $I_L$ of both currents are equal. The relationship between the load current $i_{out}(t)$ and the inductor current $i_L(t)$ is explained below.

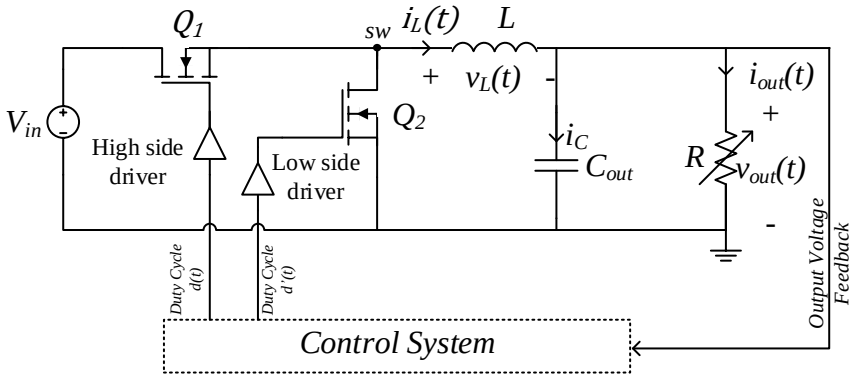



**Figure 3.10: Synchronous buck-converter with a time-varying load**

$$i_{out}(t) = I_{out} + I_m \sin(\omega_m t) \qquad (3.16)$$
$$= I_{out} + \hat{\imath}(t)$$

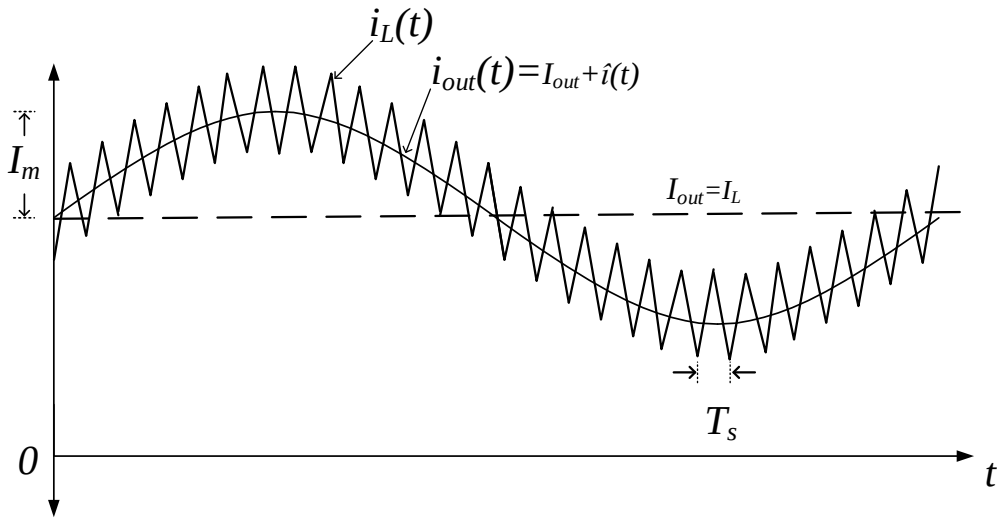



**Figure 3.11: Dynamic load current waveform and corresponding inductor current waveform**

In this case, unlike in the steady-state case, the net change in inductor current for each switching period is non-zero. The inductor current consists of high frequency switching ripple, low-frequency modulation and the DC component. The low-frequency and DC components of the inductor current are determined by the output current drawn by the load $i_{out}$. The switching ripple apparently "flows through" the capacitor $C_{out}$ in Figure 3.10 i.e. $i_C = i_L - i_{out}$. Hence, the DC and low-frequency component of the inductor current $i_L(t)$ is equivalent to the output current $i_{out}(t)$. The inductor current and output current can be related mathematically by computing the *moving average* of the inductor current. This implies averaging over each switching period and allowing the average to change from one switching period to the next. This technique is employed in [39] and shown in (3.17) where $\langle i_L(t)\rangle_{T_s}$ denotes the *moving average* of $i_L(t)$ over an interval $T_s$. The resulting waveform is approximately equivalent to the output current waveform as expressed in (3.18).

$$\langle i_L(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_L(\tau)d\tau \tag{3.17}$$

$$\langle i_L(t)\rangle_{T_s} \approx i_{out}(t) = I_{out} + \hat{\imath}(t) \tag{3.18}$$

***Frequency Limitation of the Dynamic Load Model***

The frequency limitation of the dynamic model is explained as follows. From the steady-state model in (3.15) in the previous section, the load current is proportional to the average switch-node voltage. From *Step Six* in the steady-state model derivation, a relationship between the average switch-node voltage and duty cycle can be determined from (3.13), repeated below and expanded to yield (3.19). It is deduced from (3.19) that the switch-node voltage is directly proportional to the duty cycle. Hence, the load current is directly proportional to the duty cycle.

$$V_{sw} \approx \left(D(V_{in} - I_L R_{on1}) + D'(-I_L R_{on2})\right) \quad (3.13)$$

$$V_{sw} \approx \left(D(V_{in} - I_L R_{on1}) + (1-D)(-I_L R_{on2})\right)$$

$$V_{sw} \approx DV_{in} - DI_L R_{on1} - I_L R_{on2} + DI_L R_{on2}$$

$$\therefore V_{sw} \approx D(V_{in} - I_L R_{on1} - I_L R_{on2}) - I_L R_{on2} \quad (3.19)$$

Thus, for the AC analysis, it is assumed that the duty cycle $d(t)$ modulates approximately in phase with the current to keep the output voltage constant, as defined in (3.20). $D$ is the DC component of the duty cycle $d(t)$ that results in the DC component of the load current $I_{out}$ and $\hat{d}(t) = D_m \sin(\omega_m t)$ is superimposed onto $D$ with the same modulation frequency given by $\omega_m = 2\pi f_m$ to maintain the output voltage at the required level. The inverse of $d(t)$ is $d'(t) = 1 - d(t) = D' - \hat{d}(t)$.

$$d(t) = D + \hat{d}(t) \quad (3.20)$$

$$where\ \hat{d}(t) = D_m \sin(\omega_m t)$$

$$and\ d'(t) = 1 - d(t) = D' - \hat{d}(t)$$

This assumption above that the duty cycle $d(t)$ modulates approximately in phase with the current is valid when the modulation frequency of the current is lower than the bandwidth of the controller [34]. At higher load current frequencies, or if there is a step change in load current, there will be a time delay in the response of the duty cycle to the change in load current. For a modulating current, this will cause

a phase shift between the modulating current and the duty cycle. Without knowledge of the controller transfer function, the response time of the duty cycle to the change in output current is unknown. Hence, only if the load current frequency is sufficiently small (less than the bandwidth), the duty cycle will modulate approximately in phase with the current. The output voltage can then be approximated as a constant, neglecting the small error. This effect will be evident in the simulation results in Chapter 5.

This is the limitation of the AC model for a buck converter whose control system dynamics are unknown. Nonetheless, it will become clear in Chapter 5 that the low-frequency load current model is useful. (It will explain certain effects that are present in the current measurement technique when a step change in current occurs.) The buck converter AC load current modelling approach, that is valid when the current and duty cycle are approximately in phase, is explained below. Thereafter, each step of the derivation of the model is shown.

***Dynamic Modelling Approach***

The dynamic modelling approach below is adapted from the *Basic AC Modelling Approach* presented in [39] and is based on the steady-state modelling approach in the previous section. In [39] an open loop analysis of a buck converter is performed i.e. an analysis with the absence of the feedback loop and control system. A small AC signal is superimposed onto the duty cycle signal and the resulting currents and voltages are derived to develop a small-signal model. The method from [39] was adapted to the closed loop converter in Figure 3.10 to derive the dynamic load current model in a buck converter . The approach is as follows.

1) For one switching period, consider the interval when $Q_1$ conducts and the interval when $Q_2$ conducts, separately. Represent the buck converter by its equivalent circuits during these two intervals. Include the conduction losses of the MOSFETS and the inductor DCR in the equivalent circuits.

2) From each equivalent circuit, derive the expression for the inductor voltage $v_L(t)$.
3) Apply the small-ripple approximation for the dynamic quantities. This is done by eliminating the switching harmonics and averaging the waveforms over one switching period yielding the *moving average*. The *moving average* of a signal $x(t)$ over an interval $T_s$ is given by (3.21) [39]:

$$\langle x(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} x(\tau)d\tau \tag{3.21}$$

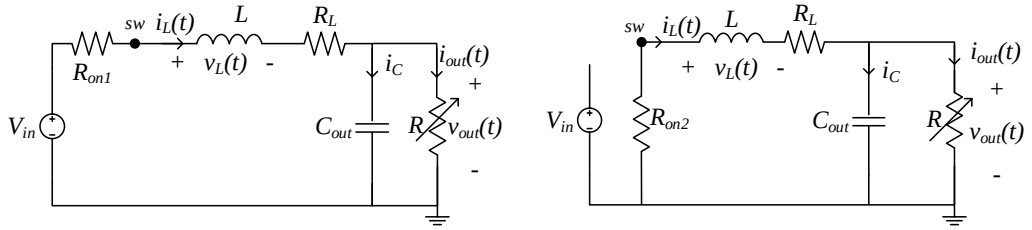
Applying (3.21) to the inductor current will eliminate the switching ripple.
4) Use the expressions for $v_L(t)$ to obtain the inductor voltage waveform during one switching period.
5) Determine the *moving average* of the inductor voltage from the waveform. Applying this *moving average* integral to both sides of the fundamental inductor voltage and current relationship yields:

$$\langle v_L(t)\rangle_{T_s} = L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} \tag{3.22}$$

Hence, equate the *moving average* of the inductor voltage from the waveform to $L\frac{d\langle i_L(t)\rangle_{T_s}}{dt}$.
6) Simplify the *moving average* of the inductor voltage by substituting the *moving average* of the switch-node voltage into the expression.
7) Separate the DC and AC terms to obtain an expression and equivalent circuit for the AC component of the load current.

***Step One: Equivalent Circuits of Synchronous Buck for Dynamic Load***

The equivalent circuits for one switching event for an AC load, defined previously, is given in Figure 3.12. The MOSFET on-resistances and the inductor DCR have been modelled as described in the steady-state case.




(a)High-Side MOSFET conducting (b) Low-Side MOSFET conducting

**Figure 3.12: Equivalent circuits for one switching event with a dynamic output current**

***Step Two: Inductor Voltage Expressions***

From Figure 3.12, the inductor voltage $v_L(t)$ when the high-side MOSFET conducts is given by:

$$v_L(t) = V_{in} - i_L(t)R_{on1} - i_L(t)R_L - v_{out}(t) \tag{3.23}$$

When the low-side MOSFET conducts, the inductor voltage is given by:

$$v_L(t) = -i_L(t)R_{on2} - i_L(t)R_L - v_{out}(t) \tag{3.24}$$

***Step Three: Small-Ripple Approximation***

Applying the small-ripple approximation to inductor current in the dynamic case involves removing the switching ripple and maintaining the DC and low-frequency components of the inductor current signal. This was shown previously in Figure 3.11. Recall that the low-frequency components of the inductor current are computed by the *moving average* in (3.17), repeated below, which acts as a mathematical low-pass filter for the inductor current signal. The resulting low-frequency component is equivalent to the load current expressed in (3.18) repeated below.

$$\langle i_L(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_L(\tau)d\tau \tag{3.17}$$

$$\langle i_L(t)\rangle_{T_s} \approx i_{out}(t) = I_{out} + \hat{\imath}(t) \tag{3.18}$$

Since the DC components of the inductor current and the output current are equivalent, the inductor current can be approximated by its DC component and the

low-frequency component of the modulated output current as expressed in (3.25) below. This substitution is made for consistency because the steady-state model was dependent on $I_L$.

$$i_L(t) \approx \langle i_L(t) \rangle_{T_s} \approx I_L + \hat{\imath}(t) \tag{3.25}$$

With regards to the output voltage, it is assumed that it remains constant. The small error resulting from the changing load current can be neglected because the duty cycle changes in phase with the current to keep the output voltage constant. Furthermore, the small-ripple approximation from the steady-state case applies as well. Hence, the output voltage is approximated by its DC component:

$$v_{out}(t) \approx V_{out} \tag{3.26}$$

The expressions from (3.25) and (3.26) simplify the inductor voltage expressions from the previous step. By replacing $i_L(t)$ and $v_{out}(t)$ with the above approximations, the inductor voltage is simplified to the expression in (3.27) for when the high-side MOSFET conducts and (3.28) for when the low-side MOSFET conducts.

$$v_L(t) \approx V_{in} - (I_L + \hat{\imath}(t))R_{on1} - (I_L + \hat{\imath}(t))R_L - V_{out} \tag{3.27}$$

$$v_L(t) \approx -(I_L + \hat{\imath}(t))R_{on2} - (I_L + \hat{\imath}(t))R_L - V_{out} \tag{3.28}$$

***Step Four: Inductor Voltage Waveform for Dynamic Load***

From the expressions in (3.27) and (3.28), the inductor voltage waveform for one switching period is given in Figure 3.13. Recall that the duty cycle is given by $d(t) = D + \hat{d}(t)$ where $\hat{d}(t) = D_m \sin(\omega_m t)$. Thus, for each switching period interval $T_s$ the duty cycle is determined by $d(t)$. (In [39] the duty cycle for the time period $T_s - 0$ is determined by $d(T_s)$.) The dashed lines in Figure 3.13 indicates the approximation that is necessary for the next step and is explained below.

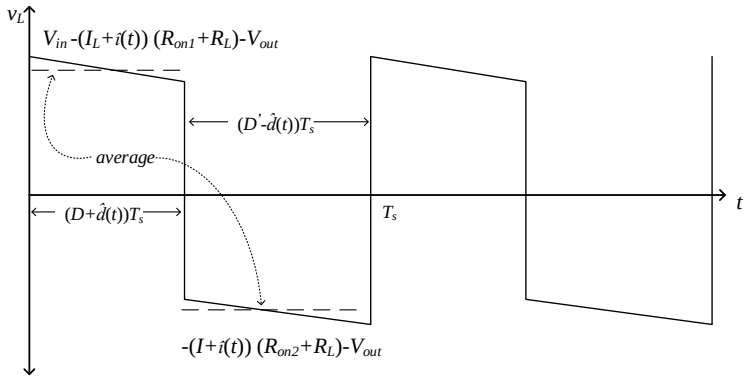



**Figure 3.13: Inductor voltage waveform for dynamic load current**

The slope of upper and lower limits in Figure 3.13 are decreasing due to the time varying current $I_L + \hat{\imath}(t)$. The dashed lines representing the average of the sloped lines which will be useful to determine the area under the curve in the next step. The dashed line is obtained by averaging $I_L + \hat{\imath}(t)$ for the duration of one period $T_s$ i.e. applying the *moving average* integral. Hence, the upper limit can be approximated to:

$$v_L(t) \approx V_{in} - \langle I_L + \hat{\imath}(t)\rangle_{T_s} R_{on1} - \langle I_L + \hat{\imath}(t)\rangle_{T_s} R_L - V_{out} \qquad (3.29)$$

The lower limit can be approximated to:

$$v_L(t) \approx -\langle I_L + \hat{\imath}(t)\rangle_{T_s} R_{on2} - \langle I_L + \hat{\imath}(t)\rangle_{T_s} R_L - V_{out} \qquad (3.30)$$

***Step Five: Moving Average Inductor Voltage Expression for Dynamic Load***

In the steady-state case, the average inductor voltage is zero. In this case, the *moving average* of $v_L(t)$ is given by (3.22) repeated below:

$$\langle v_L(t)\rangle_{T_s} = L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} \qquad (3.22)$$

This is obtained by applying the *moving average* integral $\langle x(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} x(\tau)d\tau$ to both sides of the fundamental inductor voltage and current relationship. (The average computed every $T_s$ seconds).

Expanding the left-hand-side of (3.22) yields (3.31) which is solved by computing the area under the curve in Figure 3.13 in the previous step.

$$\langle v_L(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} v_L(\tau)d\tau \tag{3.31}$$

$$= \frac{1}{T_s}\begin{pmatrix}\left(D+\hat{d}(t)\right)T_s\left(V_{in}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on1}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_L-V_{out}\right)\\+\left(D'-\hat{d}(t)\right)T_s\left(-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on2}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_L-V_{out}\right)\end{pmatrix}$$

$$= L\frac{d\langle i_L(t)\rangle_{T_s}}{dt}$$

From the small ripple approximation in *Step Three*, the inductor current on the right-hand-side of (3.22) can be approximated by:

$$i_L(t) \approx I_L + \hat{\imath}(t) \tag{3.32}$$

Hence, the last line of (3.31) becomes (3.33) which is the expression for the *moving average* of the inductor voltage.

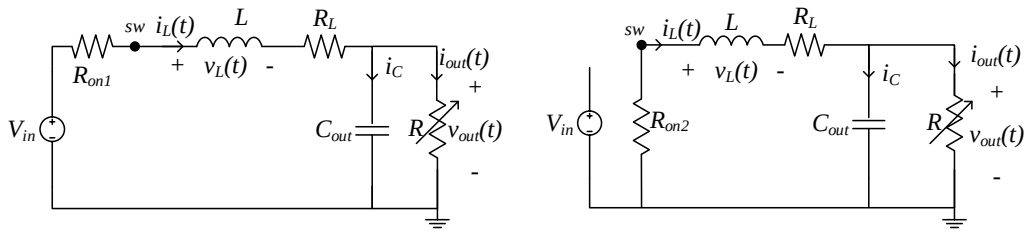
$$\langle v_L(t)\rangle_{T_s} = \tag{3.33}$$

$$= \frac{1}{T_s}\begin{pmatrix}\left(D+\hat{d}(t)\right)T_s\left(V_{in}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on1}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_L-V_{out}\right)\\+\left(D'-\hat{d}(t)\right)T_s\left(-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on2}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_L-V_{out}\right)\end{pmatrix}$$

$$= L\frac{d\langle I_L+\hat{\imath}(t)\rangle_{T_s}}{dt}$$

***Step Six: Simplify Moving Average Inductor Voltage Expression***

As was done in the steady-state case, the expression can be simplified by analysis of the switch-node voltage. From the equivalent circuits in *Step One*, repeated below in Figure 3.14, the switch-node voltage waveform is shown in Figure 3.15. The small-ripple approximation for $i_L(t)$ from *Step Three* was applied replacing $i_L(t)$ with $I_L + \hat{\imath}(t)$.




(a)High-Side MOSFET conducting (b) Low-Side MOSFET conducting

**Figure 3.14: Equivalent circuits for one switching event with a dynamic output current**

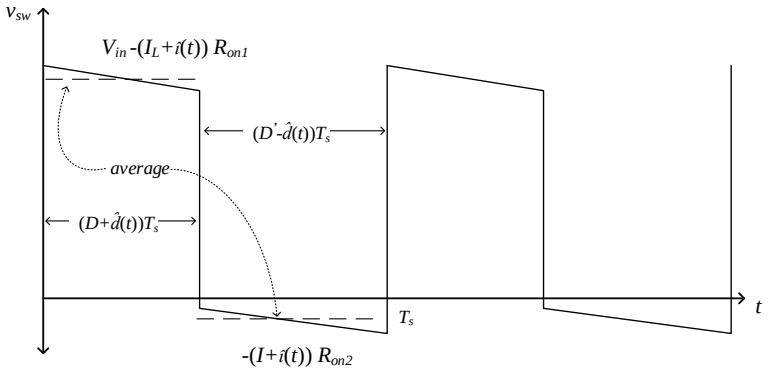



**Figure 3.15: Switch-node voltage waveform with dynamic load current**

Applying the same current averaging techniques from the previous step to obtain the averages indicated by the dashed lines in Figure 3.15, the *moving average* of the switch-node voltage is given by:

$$\langle v_{sw}(t)\rangle_{T_s} \approx \tag{3.34}$$
$$= \frac{1}{T_s}\begin{pmatrix}\left(D+\hat{d}(t)\right)T_s\left(V_{in}-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on1}\right)\\+\left(D'-\hat{d}(t)\right)T_s\left(-\langle I_L+\hat{\imath}(t)\rangle_{T_s}R_{on2}\right)\end{pmatrix}$$

Substituting (3.34) into the *moving average* of the inductor voltage from the previous step, simplifies it to:

$$\langle v_L(t)\rangle_{T_s} \approx \langle v_{sw}(t)\rangle_{T_s} - \langle I_L+\hat{\imath}(t)\rangle_{T_s}R_L - V_{out} \approx L\frac{d\langle I_L+\hat{\imath}(t)\rangle_{T_s}}{dt} \tag{3.35}$$

***Step Seven: Obtain Dynamic Load Current Equivalent Circuit Model and Expression***

To obtain the dynamic or AC equivalent circuit, the *moving average* inductor voltage expression from (3.35) in the previous step needs to be expanded and separated into DC and AC terms. To do this, first the term $\langle v_{sw}(t)\rangle_{T_s}$ (the *moving average* of the switch-node voltage) from (3.35) needs to be separated into DC and AC terms. This is done by expanding $\langle v_{sw}(t)\rangle_{T_s}$ from (3.34) in the previous step. This is shown below and yields the DC and AC components as well as the non-linear terms of $\langle v_{sw}(t)\rangle_{T_s}$.

$$\langle v_{sw}(t)\rangle_{T_s} = \big(D(V_{in} - I_L R_{on1}) + D'(-I_L R_{on2})\big) + \cdots$$ — *DC Terms= $V_{sw}$*

$$\ldots \Big(D\big(-\langle \hat{\imath}(t)\rangle_{T_s} R_{on1}\big) + D'\big(-\langle \hat{\imath}(t)\rangle_{T_s} R_{on2}\big)\Big) \ldots$$

$$+ \Big(\hat{d}(t)(V_{in} - I_L R_{on1}) - \hat{d}(t)(-I_L R_{on2})\Big) \ldots$$ — *AC Terms= $\hat{v}_{sw}(t)$*

$$+ \Big(\hat{d}(t)\big(-\langle \hat{\imath}(t)\rangle_{T_s} R_{on1}\big) - \hat{d}(t)\big(-\langle \hat{\imath}(t)\rangle_{T_s} R_{on2}\big)\Big)$$ — *Non-linear 2nd Order Terms*

From the above, the DC terms equate to the DC component of the switch-node voltage $V_{sw}$ from the steady-state analysis in the previous section:

$$V_{sw} \approx \big(D(V_{in} - I_L R_{on1}) + D'(-I_L R_{on2})\big) \tag{3.36}$$

The AC terms represent a sinusoidal signal in phase with the current and duty cycle. Note that the modulation frequency of $\langle \hat{\imath}(t)\rangle_{T_s}$, is approximately the same as the modulation frequency of $\hat{d}(t)$. (This is explained further on in this step.) Therefore, the modulation frequency of the sum of the *AC Terms* is equal to the modulation frequency of $\hat{d}(t)$ and $\langle \hat{\imath}(t)\rangle_{T_s}$. The sum of the AC *Terms* represents the low-frequency component of the switch-node voltage. Let the low-frequency component of the switch-node voltage be $\hat{v}_{sw}(t)$. From the *AC Terms* above, it is defined in (3.37):

$$\hat{v}_{sw}(t) \approx (-DR_{on1} - D'R_{on2})\langle \hat{\imath}(t)\rangle_{T_s} + (V_{in} - I_L R_{on1} + I_L R_{on2})\hat{d}(t) \tag{3.37}$$

The non-linear terms are second order terms due to the multiplication of two sinusoidal signals. These are small in comparison to the DC and AC components and their effect can be neglected [39]. Furthermore, if $R_{on1} \approx R_{on2}$ the non-linear terms would equate to zero. (This is not always the case but if identical MOSFETS are used it could be true).

Hence, the DC and AC components of $\langle v_{sw}(t)\rangle_{T_s}$ is expressed in (3.38) where $V_{sw}$ is the DC component of the switch-node voltage defined in the steady-state model and $\hat{v}_{sw}(t)$ is the low-frequency component of the switch-node voltage.

$$\langle v_{sw}(t)\rangle_{T_s} \approx V_{sw} + \hat{v}_{sw}(t) \tag{3.38}$$

Now, (3.38) can be substituted into the inductor average voltage expression from (3.35) in the previous step. This is shown below in (3.39) and the DC and AC terms are identified.

$$\underbrace{V_{sw} - I_L R_L - V_{out}}_{DC\ Terms} + \underbrace{\hat{v}_{sw}(t) - \langle \hat{\imath}(t) \rangle_{T_s} R_L}_{AC\ Terms} \approx \underbrace{0}_{DC\ Term} + \underbrace{L \frac{d\langle \hat{\imath}(t) \rangle_{T_s}}{dt}}_{AC\ Term} \tag{3.39}$$

Equating the DC terms yields the steady-state model from the previous section. Equating the AC terms yields:

$$\hat{v}_{sw}(t) - \langle \hat{\imath}(t) \rangle_{T_s} R_L \approx L \frac{d\langle \hat{\imath}(t) \rangle_{T_s}}{dt} \tag{3.40}$$

Recall that $\langle \hat{\imath}(t) \rangle_{T_s}$ denotes the *moving average* of $\hat{\imath}(t)$, where an average for intervals $T_s$ are calculated moving along the waveform from one interval to the next. However, the period of $\hat{\imath}(t)$ is much larger than the switching period $T_s$. Thus, if a moving average is recorded after every interval $T_s$, the resulting moving average waveform, will approximately be the original waveform. Hence $\langle \hat{\imath}(t) \rangle_{T_s} \approx \hat{\imath}(t)$, and the current averaging brackets can be dropped from the expression. This yields the expression approximately describing the AC component of the load current in (3.41) below.

$$\hat{v}_{sw}(t) - \hat{\imath}(t) R_L \approx L \frac{d\hat{\imath}(t)}{dt} \tag{3.41}$$

The expression in (3.41) can be expressed by an equivalent circuit shown in Figure 3.16. Let the amplitude of $\hat{v}_{sw}(t)$ in (3.37) be defined as $V_m$ and recall that $\hat{\imath}(t) = I_m \sin(\omega_m t)$ as defined in the beginning of this section. A frequency domain representation of the circuit in Figure 3.16 appears in Figure 3.17 with phasor diagrams for the voltages and current.

This result shows that for an AC load current, the reactance of the inductor causes a phase shift between the low-frequency component of the switch-node voltage and the AC load current.

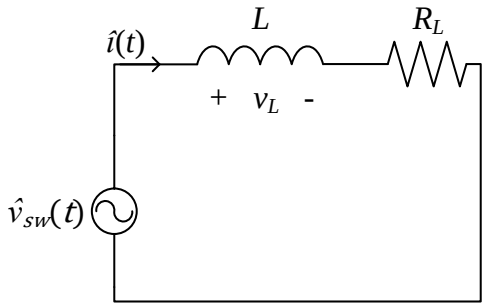



**Figure 3.16: Time domain equivalent circuit model for AC load current component**

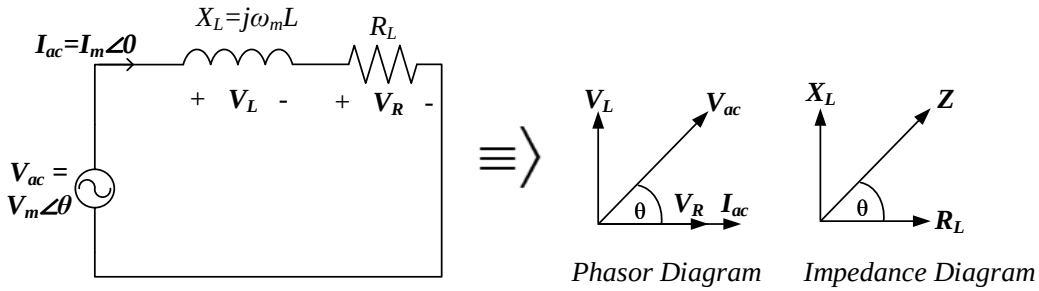



**Figure 3.17: Frequency domain equivalent circuit model for AC load current component**

## 3.4 Application of the Model

A buck converter model for steady-state load current and low-frequency dynamic load current is derived in the previous section. A microprocessor will typically draw current in steps since, internally, it operates with logic signals that are switching states. Application of the steady-state model to this type of load will be discussed below. (The microprocessor will not typically draw an AC current, but the AC model will be useful in Chapter 5 when simulating the step response of the averaging filter.)

Consider the example of an arbitrary load current drawn by a microprocessor as shown in Figure 3.18. The total duration of the current is given by $T_x$ in seconds and $T_x \gg T_s$ where $T_s$ is the switching period of the buck converter. The switching

period $T_s$ is typically larger than the clock cycle of the processor in the embedded system. (Clock frequencies are typically in the *GHz* range whilst converter switching frequencies are in the 100 *kHz* or *MHz* range) For each clock cycle, the processor will draw current determined by the machine code. The load current can switch from one level to another at the clock frequency of the processor. However, assume that the current for each period $T_s$ is represented by its average. Suppose that the load current in Figure 3.18 for the total duration $T_x$ (defined by the software developer) is for a set of instructions. The current is unknown but its average is required by the software developer for average software power estimation. The current can be modelled by its DC component $I_{load}$ as shown by the approximated dashed line in Figure 3.18. The steady-state model from (3.15), repeated below can then be used to estimate the average current $I_{load}$. This is elaborated below.

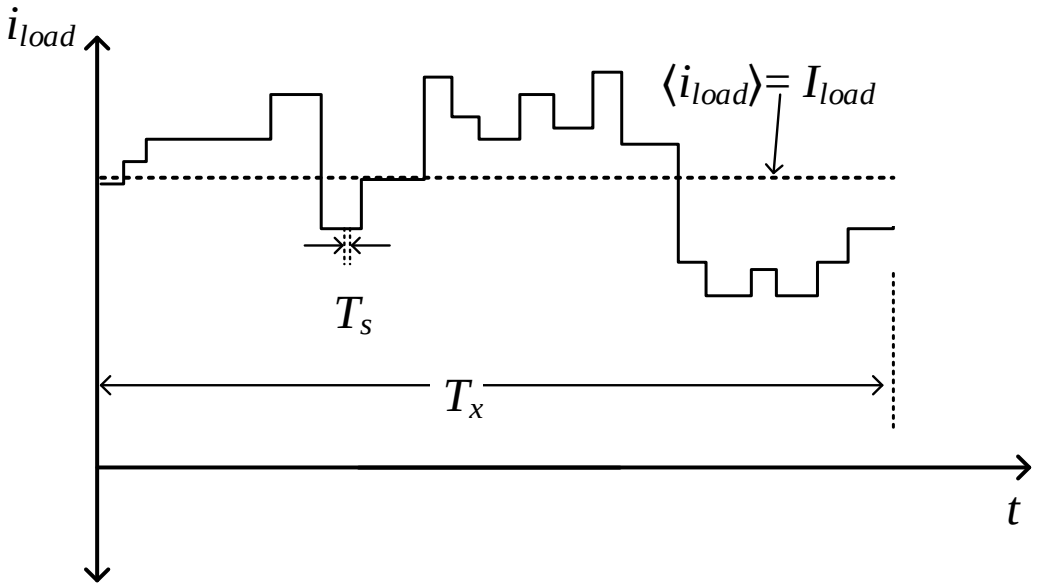



**Figure 3.18: Arbitrary load current drawn by a microprocessor**

$$I_{load} \approx \frac{1}{R_L}(V_{sw} - V_{out}) \qquad (3.15)$$

Assume that the DC components of the switch-node voltage and output voltage for the duration $T_x$ were known. The DCR, $R_L$, can be measured at start-up. (This can be done by using a precision multimeter across the inductor terminals when the

buck converter in unenergised.) Substituting into (3.15) will yield the overall average load current $I_{load}$ shown in Figure 3.18.

The model can also be applied for smaller instruction sections, where the average voltages $V_{sw}$ and $V_{out}$ can be computed for shorter periods of time $T_1$-$T_6$ measured in seconds, as shown in Figure 3.19 . This will yield the average current for shorter intervals as shown in Figure 3.19. For each period of time $T_1$-$T_6$, the model is applied to determine the average current (approximated by the horizontal dashed lines) over that period. This gives a clearer indication of the load current's behaviour over time. In the example in Figure 3.19, a significant decrease in the average current is visible at duration $T_5$.

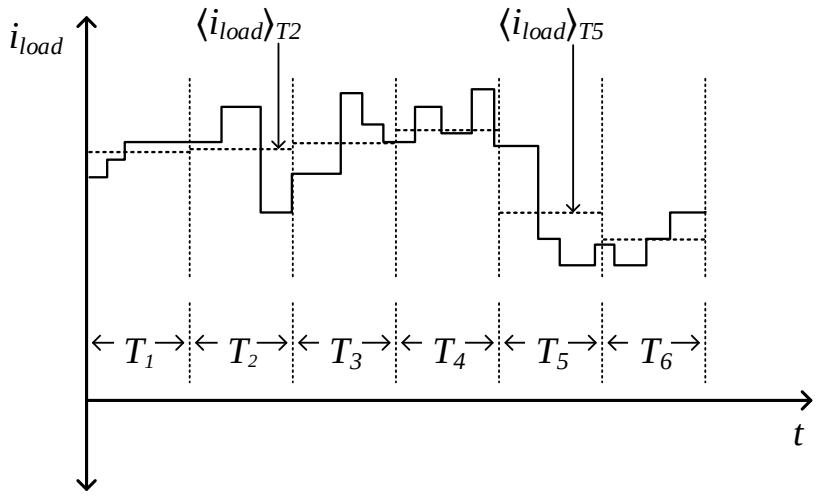



**Figure 3.19: Applying the steady-state load current to shorter periods for an arbitrary load current**

## 3.5 Discussion on Some Model Exclusions

The steady-state and dynamic load current models of a buck converter derived in the above section are based on the approach by Erickson in [27]. The non-ideal effects included in the model consisted of the conduction losses of the MOSFETS and the inductor DCR. Other non-ideal effects were excluded in the approach by Erickson. Erickson claims in [27] that the modelling approach in [27] models the

dominant behavior of the currents and voltages in the buck converter. Hence by exclusion, Erickson deemed the following non-ideal effects insignificant in the basic buck converter model:

- The equivalent series resistance (ESR) of the capacitor
- The temperature dependence of the inductor DCR
- Stray inductances at the switch-node and MOSFET parasitic capacitances that cause switch-node ringing

These non-ideal effects and the rationale for excluding them are discussed below.

### 3.5.1 Output Capacitor ESR

***Justification for Exclusion***

The capacitor $C_{out}$ at the output voltage node of the buck converter inherently contains an ESR. This is modelled by $R_C$ in Figure 3.20 which shows the filter and output stages of a buck converter. The DCR of the inductor $R_L$ is also modelled in the figure.

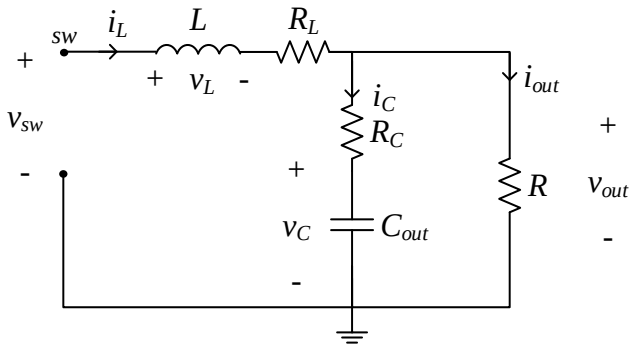



**Figure 3.20: Filter and output stages of a buck converter**

From Figure 3.20, the current through the ESR is $i_C = i_L - i_{out}$ and is also expressed by $i_C = C\frac{dv_c}{dt}$. The output voltage $v_{out}$ is given by (3.42):

$$v_{out} = v_C + C\frac{dv_c}{dt}R_C \tag{3.42}$$

Due to the *small-ripple approximation* from *Step Three* in the model derivation (for the steady-state and dynamic load models), the output voltage was approximated to be equal to its DC component $V_{out}$. Furthermore, the inductor current $i_L$ was approximated to be equal to the load $i_{out}$ essentially stating that in the model $i_C = C\frac{dv_c}{dt} = 0$ and $v_c = 0$ . Hence, $R_C$ in the model was unnecessary based on these approximations.

As a side note, the ESR would be relevant in a transient analysis when there is a step change in current and $v_{out}$ responds according to the controller dynamics by containing a voltage spike (either upwards or downwards depending on the current step) before stabilising. During this time, $\frac{dv_c}{dt} \neq 0$ and $i_C \neq 0$, therefore current flows through the ESR. However, without knowledge of the controller dynamics, the closed loop model was limited to steady-state and low-frequency currents.

***Average Power Analysis Model***

To validate the exclusion of the ESR in the model, consider modelling the $L$ and $C$ filter stages of the buck converter within the circuit shown in Figure 3.21, on the next page. The circuit in Figure 3.21 is an alternative model of the buck converter that is independent of a duty cycle. The buck converter load is replaced by a constant current source to model the buck converter steady-state load current. The switch-node voltage is modelled by a DC voltage source in series with an AC source. Since the switch-node-voltage is a pulse train voltage consisting of a DC component and an infinite number of harmonics at multiples of the switching frequency, as will be shown in Chapter 4, it can be modelled as an AC source superimposed with a DC source. The average power consumed by the load in this circuit can be analysed to determine if there is a dependence on ESR of the capacitor $R_C$.

Based on the steady-state model of the buck converter, it can be claimed that the average load current in Figure 3.21 can be estimated by applying Ohm's Law across

the inductor using DC components of the voltages. Hence, it can be claimed that the average power consumed by the load is given by (3.43). The estimated average power $\langle P \rangle_{estimated}$ is dependent purely on DC components of the node voltage, the output voltage and on the inductor DCR $R_L$. It is completely independent of capacitor ESR $R_C$.

$$\langle P \rangle_{estimated} \approx \frac{(V_{node} - V_{out})}{R_L} V_{out} \tag{3.43}$$

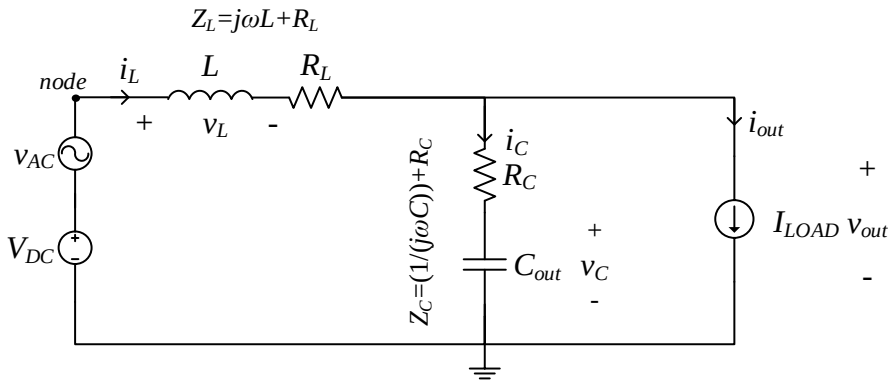



**Figure 3.21: Alternative model of the buck converter filter and output stages in steady-state**

An analysis on the **actual** power consumption vs. the power consumption **estimated** in (3.43) using the buck converter load current model, can be performed. If the actual average is also independent of ESR and is equivalent to the estimated average power in (3.43), it can be deduced that neglecting the ESR from the original model was valid. This analysis is shown below.

From the definition of average power for a period of time $T$, the **actual** average power consumed by the load in Figure 3.21 is given in terms of the integral in (3.44) below:

$$\langle P \rangle_{actual} = \frac{1}{T} \int_0^T i_{out}(t) v_{out}(t) dt \tag{3.44}$$

The output current is the current consumed by the load that is modelled by the constant current source i.e. $i_{out}(t) = I_{LOAD}$. This simplifies the expression to:

$$\langle P\rangle_{actual} = I_{LOAD}\frac{1}{T}\int_0^T v_{out}(t)dt \tag{3.45}$$

The voltage $v_{out}(t)$ can be determined by applying the superposition theorem. This is shown in Figure 3.22 (a)-(c) where each source excites the circuit separately (whilst the remaining voltage sources are shorted and current sources are open).

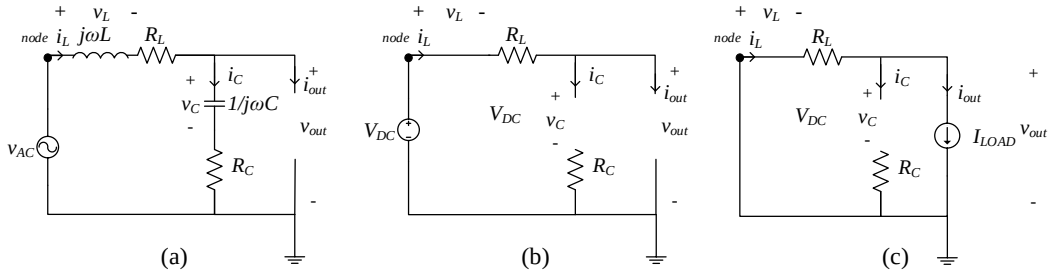



**Figure 3.22: Effect of each source on the circuit in Figure 3.21 (with the remaining voltage sources shorted and current sources opened)**

From Figure 3.22, the output voltage $v_{out}(t)$ is calculated as follows:

From Figure 3.22 (a), let $v_{AC}(t) = A\sin(\omega t + \varphi)$. Using phasor notation, the source voltage and impedances can be expressed as:

$\boldsymbol{V_{AC}} = A\angle\varphi$

$\boldsymbol{Z_L} = R_L + j\omega L = Z_L\angle\varphi_L$

$\boldsymbol{Z_C} = R_C - j\dfrac{1}{\omega C} = Z_C\angle\varphi_C$

$\boldsymbol{Z_T} = \boldsymbol{Z_C} + \boldsymbol{Z_L} = Z_T\angle\varphi_T$

By voltage divider: $\boldsymbol{V_{out}} = \boldsymbol{V_{AC}}\dfrac{\boldsymbol{Z_C}}{\boldsymbol{Z_T}} = A\angle\varphi\dfrac{Z_C\angle\varphi_C}{Z_T\angle\varphi_T} = A_{out}\angle\varphi_{out}$

$\Rrightarrow v_{out(a)}(t) = A_{out}\sin(\omega t + \varphi_{out})$

From Figure 3.22 (b): $v_{out(b)}(t) = V_{DC}$

From Figure 3.22 (c): $v_{out(c)}(t) = -I_{LOAD}R_L$

$\therefore\ v_{out}(t) = A_{out}\,sin(\omega t + \varphi_{out}) + V_{DC} - I_{LOAD}R_L$ (3.46)

Substituting (3.46) into the average power expression in (3.44) yields:

$$\langle P\rangle_{actual} = I_{LOAD}\frac{1}{T}\int_0^T v_{out}(t)dt$$

$$= I_{LOAD}\left(\frac{1}{T}\int_0^T (A_{out}\, sin(\omega t + \varphi_{out}) + V_{DC} - I_{LOAD}R_L)dt\right)$$

For simplification, assume that the averaging interval $T$ is a multiple of the period of $v_{out}(t)$. Since the average of a sinusoidal signal over one full period is zero, the expression simplifies to (3.47) as shown below.

$$\langle P\rangle_{actual} = I_{LOAD}\left(\frac{1}{T}\int_0^T (A_{out}\, sin(\omega t + \varphi_{out}) + V_{DC} - I_{LOAD}R_L)dt\right)$$

$$= I_{LOAD}(0 + V_{DC} - I_{LOAD}R_L)$$

$$\therefore \langle P\rangle_{actual} = I_{LOAD}V_{DC} - I_{LOAD}^2R_L \quad (3.47)$$

Next, the average power estimated in (3.43) using the steady-state load current model is evaluated below:

$$\langle P\rangle_{estimated} \approx \frac{(V_{node}-V_{out})}{R_L}V_{out} \quad (3.43)$$

The voltage $V_{node}$ is the DC component of the node voltage and by superposition using Figure 3.22 (a)-(c):

From Figure 3.22 (a): $V_{node(a)} = 0$

From Figure 3.22 (b): $V_{node(b)} = V_{DC}$

From Figure 3.22 (c): $V_{node(c)} = 0$

$$\therefore\ V_{node} = V_{DC} \quad (3.48)$$

The voltage $V_{out}$ is the DC component of the output voltage $v_{out}(t)$ calculated previously by superposition in (3.46):

$$v_{out}(t) = A_{out}\, sin(\omega t + \varphi_{out}) + V_{DC} - I_{LOAD}R_L \quad (3.46)$$

As stated above if the interval $T$ is a multiple of the period of $v_{out}(t)$, the DC component of the output voltage $V_{out}$ simplifies to:

$$V_{out} = \frac{1}{T}\int_0^T v_{out}(t)dt = V_{DC} - I_{LOAD}R_L \quad (3.49)$$

Substituting (3.48) and (3.49) into the expression in (3.43) yields:

$$\langle P\rangle_{estimated} \approx \frac{(V_{node} - V_{out})}{R_L}V_{out}$$

$$\approx \frac{(V_{DC}) - (V_{DC} - I_{LOAD}R_L)}{R_L}(V_{DC} - I_{LOAD}R_L)$$

$$\approx I_{LOAD}V_{DC} - I_{LOAD}^2 R_L$$

$$\therefore \langle P \rangle_{estimated} \approx I_{LOAD}V_{DC} - I_{LOAD}^2 R_L \quad (3.50)$$

Hence, the **actual** average power and the average power **estimated** using the model are equivalent i.e. $\langle P \rangle_{estimated} = \langle P \rangle_{actual}$. Neither expression is dependent on capacitor ESR $R_C$, thus validating the model and its exclusion of the capacitor ESR.

### 3.5.2 Switch-Node Ringing

The effect of parasitic inductances and capacitances at the switching circuit of the buck converter were excluded from the model. Theses parasitics are indicated in bold in Figure 3.23 [40]. In Figure 3.23, there are stray parasitic inductances at the drain and source terminals of each MOSFET. There are also parasitic capacitances across the drain and source of each MOSFET. These parasitics result in switch-node ringing in the buck converter and will be explained below.

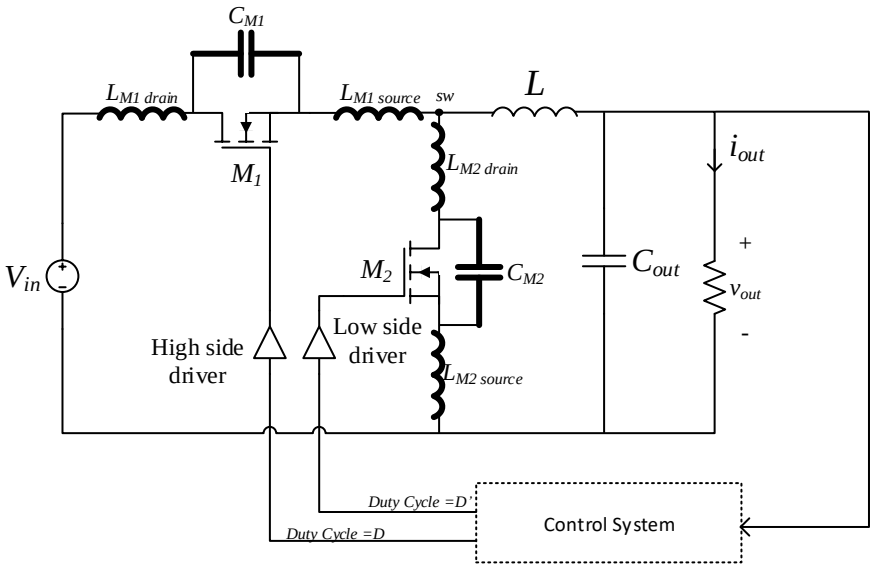



**Figure 3.23: Synchronous buck converter with parasitic inductances and capacitances responsible for switch-node ringing**

Assume that the converter is in steady-state. When the low-side MOSFET conducts, the power to the load is being provided only from the output inductance and capacitance and energy ($E = \frac{1}{2}LI^2$) is being stored in the parasitic inductances of the low-side MOSFET [40].

Thereafter, assume that the low side MOSFET is turned off quickly, and there is a relatively short period of dead time where the current is transferred to the body diode of the low-side MOSFET. The energy remains in the parasitic drain and source inductances of the low-side MOSFET. After the dead time, the high side MOSFET conducts and the low and high-side MOSFET parasitic inductances creates a resonance circuit resulting in high frequency switch ringing. This is shown in an oscilloscope trace of a switch-node voltage from an actual circuit in Figure 3.24 [40].

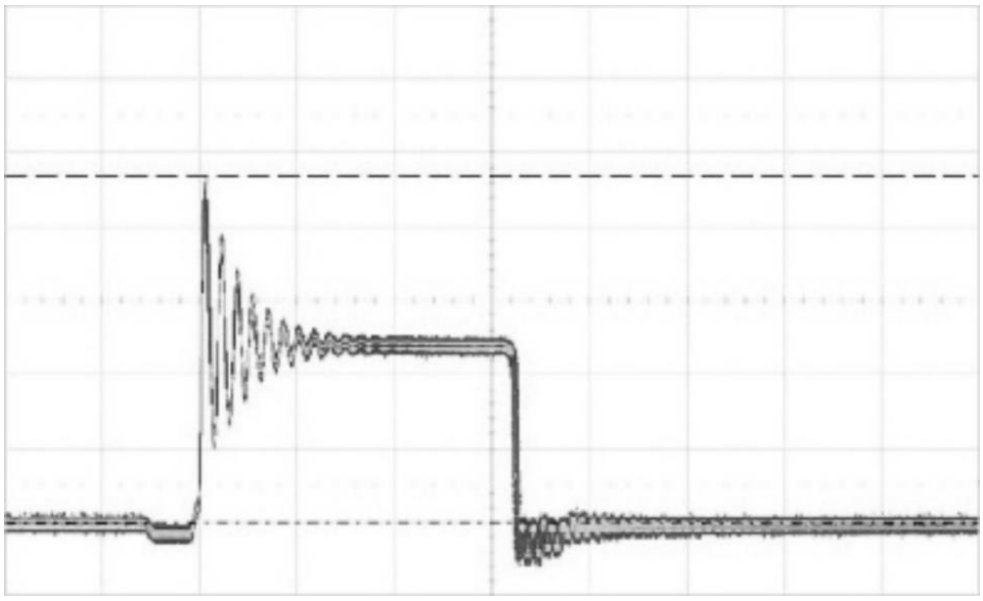


**Figure 3.24: Ringing at 12 *V* input switch-node due to parasitic inductances and capacitance described in [40] ( Time: 50 ns/div and Voltage 5 V/div)**

The parasitic effects are typically modelled in the design of buck converters. This is because the voltage spike caused by the ringing needs to be known to prevent damage to the semiconductors due to it being above the rated voltage.

With regards to this application, the ringing is described as high frequency AC ringing superimposed on to the signal without altering the DC component of the signal. The models derived describes low-frequency and DC behaviour of load current and voltages in the buck converter. Accordingly, the high switching frequency has been removed from the steady-state and AC models by applying the small-ripple approximation (in *Step Three* of both model derivations). The ringing frequency is much greater than the switching frequency and hence also deserves to be excluded from the model.

Furthermore, the sensing technique adopted is a low-pass filter based technique shown in Chapter 4. The low-pass filter will attenuate the switch-node ringing and thus it will not affect the output of the model.

### 3.5.3 Inductor DCR Temperature Drift

In the steady-state and dynamic models derived in Section 2.3, the inductor DCR $R_L$ is considered constant. However, in practice, this is not the case.

When the buck converter is switched on, the flow of current through the inductor causes power to dissipate in the inductor DCR by $P = I^2 R_L$ (where $P$ is average power and assuming a steady-state load current $I$). This power dissipation is in the form of heat and causes the temperature of the inductor to increase. The increase in temperature will cause $R_L$ to increase according to its temperature coefficient of resistance $\alpha$ (with units $℃^{-1}$). If the current decreases the power dissipated will decrease and the temperature of the inductor will decrease according to its thermal resistance (with units K/W ) until it settles. In general, the DCR will vary with its temperature according to the expression in (3.51).

$$R_L = R_{L_{ref}}\left[1 + \alpha\left(T - T_{ref}\right)\right] \tag{3.51}$$

The parameters in (3.51) are defined below:

$R_L =$ inductor DCR at temperature $T$

$R_{L_{ref}} =$ inductor DCR at reference temperature $T_{ref}$

$\alpha =$ temperature coefficient of resistance for the inductor material at reference temperature $T_{ref}$

$T =$ conductor temperature in ℃

$T_{ref}$ =reference temperature at which $\alpha$ is specified at for the inductor material

To relate the temperature effect in (3.51) to the model, presume that the buck converter is in steady-state and the DCR was calibrated at $T_{ref} = 20$ ℃ and recorded as $R_{L_{ref}}$. (This can be done by using a precision multimeter across the inductor terminals when the buck converter in unenergised.) Say that the actual inductor DCR after the temperature of the inductor rises from $T_{ref}$ to $T_{actual}$ is given by $R_{L_{actual}}$. Using the model to estimate buck converter load current (based on the DCR at reference temperature) results in the expression given in (3.52). The actual load current at inductor winding temperature $T_{actual}$ is given by (3.53).

$$I_{estimated} \approx \frac{1}{R_{L_{ref}}}(V_{sw} - V_{out}) \tag{3.52}$$

$$I_{actual} \approx \frac{1}{R_{L_{actual}}}(V_{sw} - V_{out}) \tag{3.53}$$

Let $x$ be the percentage temperature drift of the DCR from $R_{L_{ref}}$ to $R_{L_{actual}}$ when the temperature of the inductor rises from $T_{ref}$to $T_{actual}$. The actual resistance can be expressed as:

$$R_{L_{actual}} = R_{L_{ref}}\left(1 + \frac{x}{100}\right) \tag{3.54}$$

Thus, the relationship between the actual and estimated load current is given by:

$$I_{actual} = \frac{1}{R_{L_{ref}}\left(1 + \frac{x}{100}\right)}(V_{sw} - V_{out})$$

$$= \frac{I_{estimated}}{\left(1 + \frac{x}{100}\right)}$$

$$\therefore \frac{I_{estimated}}{I_{actual}} = \left(1 + \frac{x}{100}\right)$$

The percentage error in the estimated load current from the actual load current is thus also given by the percentage in temperature drift, as shown below:

$$\begin{aligned} \%Error &= \frac{|I_{estimated} - I_{actual}|}{I_{actual}} \times 100 \\ &= \left|\left(\frac{I_{estimated}}{I_{actual}} - 1\right)\right| \times 100 \\ &= \left|\left(\left(1 + \frac{x}{100}\right) - 1\right)\right| \times 100 \\ &= |x| \end{aligned}$$

Therefore, given that the percentage error of the estimated current is equal to the percentage drift of the DCR temperature, a relationship between the inductor temperature and the resultant error on the estimated current using the model can be deduced. This is shown in Figure 3.25, assuming a copper conductor with temperature coefficient of 0.393 %/℃**.** It can be seen in Figure 3.25 that if the temperature of the inductor stays below approximately 45 ℃, the percentage error of the model stays below 10 %. The temperature of the inductor is dependent on the power and hence the current flowing through it.

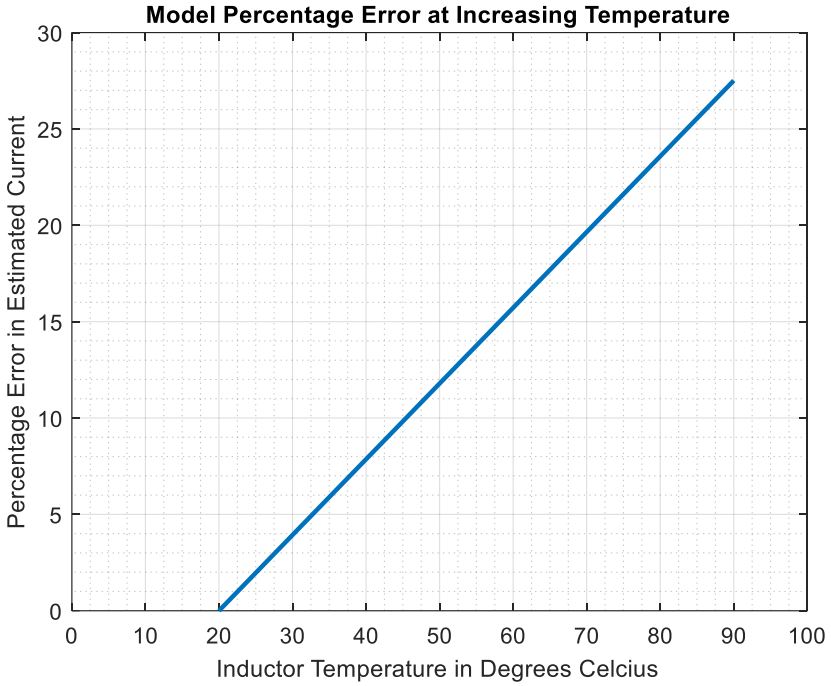


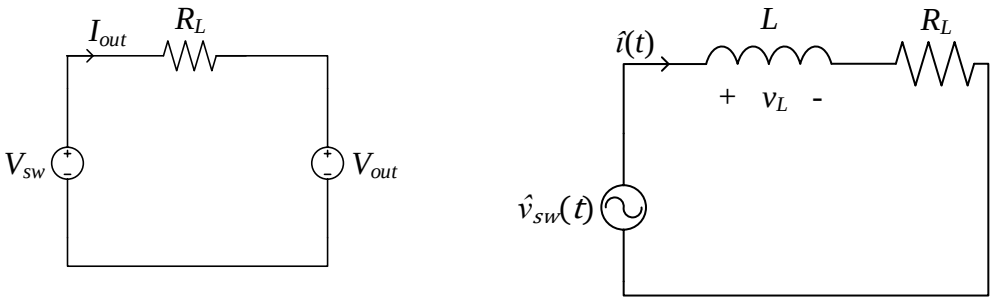

**Figure 3.25: Effect of increasing temperature on steady-state model**

In this work, the above effect was excluded from the buck converter model and the measurement technique presented. Excluding the effect contributed to the error in the technique and will be shown in Chapter 6. The effect of temperature on the DCR and the model is suggested as future work in Chapter 8.

## 3.6 Conclusion

This chapter began with an explanation of the model boundary conditions i.e. a synchronous buck converter operating in CCM. The steady-state load current model of the buck converter was derived and showed that given inductor DCR, a simple measurement of average voltages across the inductor will estimate the steady-state load current $I_{out}$. A dynamic load current model was derived that was limited to low- frequency dynamic currents. For a low-frequency dynamic current $\hat{\imath}(t)$, it was shown that the impedance of the inductor causes a phase shift between the AC component of load current and the low-frequency component of the switch-node

voltage. The equivalent circuits are summarised in Figure 3.26 and the mathematical models are expressed in (3.55) and (3.56) below.




(a) (b)

**Figure 3.26: (a) Equivalent circuit for DC component of load current in a buck converter**
**(b) Equivalent circuit for low-frequency AC component of load current in a buck converter**

$$I_{out} \approx \frac{1}{R_L}(V_{sw} - V_{out}) \tag{3.55}$$

$$\hat{v}_{sw}(t) - \hat{\imath}(t)R_L \approx L\frac{d\hat{\imath}(t)}{dt} \tag{3.56}$$

It was shown that the steady-state model can be applied to determine overall average current of any buck converter load current. Applying the model over consecutive smaller intervals for a given time duration, gives a better indication of load current behaviour with time.

An analysis on model exclusions was performed. It was deduced that the capacitor ESR and switch-node ringing did not affect the model and were justified for exclusion. However, inductor DCR temperature drift was shown to introduce error to the model. Including the effect of temperature on inductor DCR will be suggested as future work.

In order to apply the steady-state model to determine load current, a low-pass filter at the switch-node will be required to average the switch-node voltage. This will

allow the low-frequency components of the switch-node voltage to be determined. The next chapter justifies the need for the filter and details the design of the low-pass filter that will be used in the current estimation technique.

# 4 SWITCH-NODE LOW-PASS FILTER DESIGN AND TESTING

## 4.1 Introduction

In Chapter 3, the steady-state and dynamic load current models of the buck converter were derived. The steady-state load current model was dependent on the average or DC component of the switch-node voltage. The dynamic load current model was dependent on the low-frequency component of the switch-node voltage. To obtain the DC and low-frequency components of the switch-node voltage, a low-pass filter will be employed to achieve this.

This chapter presents the justification for the requirement of a low-pass filter to filter the switch-node voltage. Thereafter, the design of the low-pass filter is shown. The results from simulation and practical testing of the filter is discussed. Lastly, the current estimation technique, incorporating the use of the filter into the load current model, is presented.

## 4.2 Justification for Filtering the Switch-Node Voltage

Recall that the steady-state model of a buck converter, expressed in (4.1) and shown in Figure 4.1, can be applied to determine the average or DC component of a buck converter load current. It is dependent on $V_{sw}$, the DC component of the switch-node voltage. This section justifies the requirement for using an analogue filter to obtain the DC component of the switch-node voltage rather than digitally calculating the mean of the switch-node voltage signal with an oscilloscope.

$$I_{out} \approx \frac{1}{R_L}(V_{sw} - V_{out}) \tag{4.1}$$

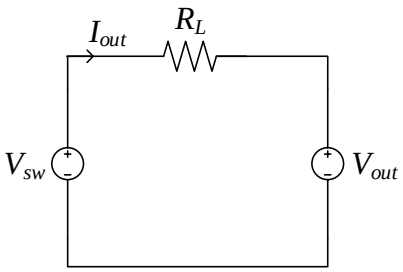



**Figure 4.1: Equivalent circuit for DC component of load current in a buck converter**

***Digital Calculation of the Mean from Raw Data***

To explain digitally calculating the mean of a signal, consider the following example. Consider two switch-node voltage signals approximated by $v_{sw1}(t)$ and $v_{sw2}(t)$ with a difference in duty cycle $\Delta D$ as shown in Figure 4.2. Assume that an oscilloscope with sampling frequency $\frac{1}{T_{sample}}$ was used to sample and plot the voltages. The voltage value plotted every $T_{sample}$ seconds are indicated by the stars.

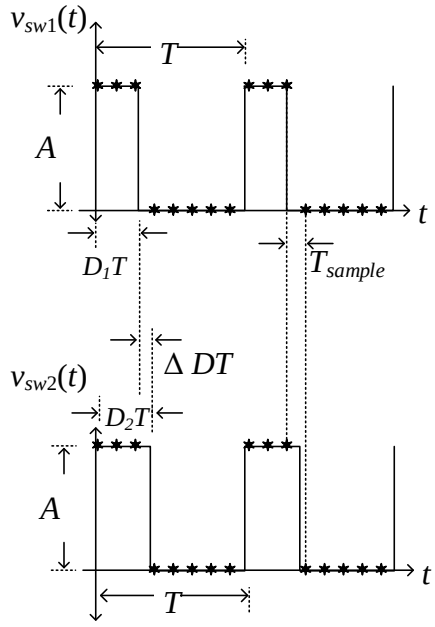



**Figure 4.2: An example of two switch-node voltage signals with a difference in duty cycle being digitally sampled to calculate the mean**

The voltages displayed on the oscilloscope will be constructed by joining the stars in Figure 4.2. Examining Figure 4.2, shows that, despite the duty cycles being different, the duty cycle of both voltages displayed on the oscilloscope screen will be the equal because $T_{sample} > \Delta DT$. By the averaging integral, the actual mathematical mean of the signals are: $\langle v_{sw1}(t) \rangle = AD_1$ and $\langle v_{sw2}(t) \rangle = AD_2$. The oscilloscope will calculate the mean as $\frac{Sum\ of\ sample\ values}{Total\ number\ of\ Samples}$. Due to the values of each sample being identical for both signals being sampled in Figure 4.2, the mean will be calculated as equal, despite their difference. For the oscilloscope to detect the difference in duty cycle between the signals, the sampling frequency must be increased to increase the number of samples. The accuracy of the calculated mean is thus proportional to the number of samples.

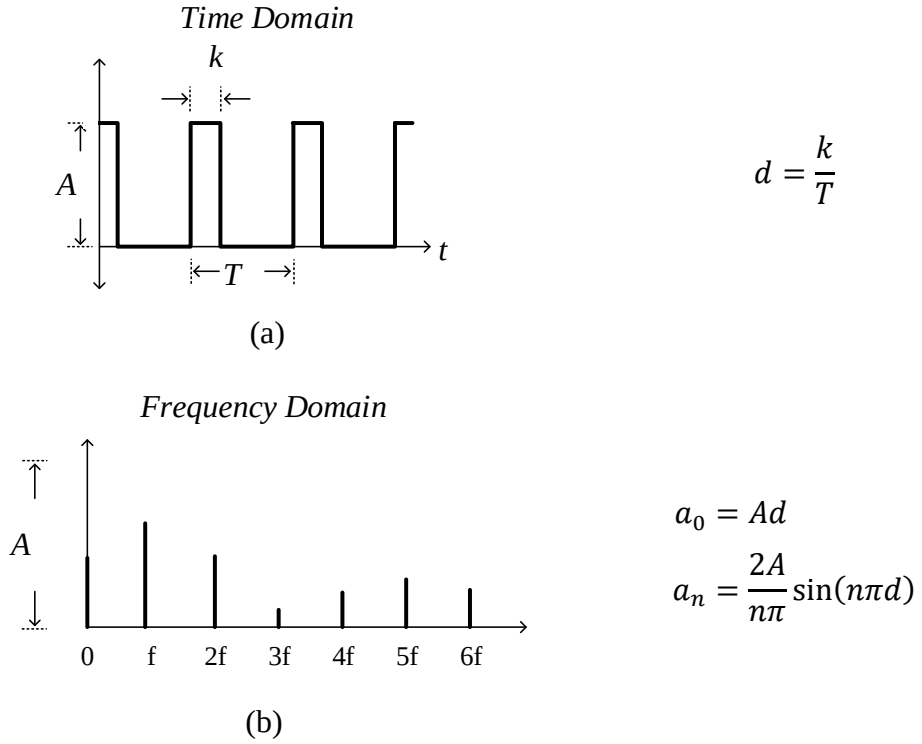
Say, however, that the number of samples shown in Figure 4.2 are the maximum number of samples that the oscilloscope can plot. To plot a larger time duration of the switch-node voltages, the oscilloscope will reduce the sampling frequency to accommodate for more switching periods to be sampled. The number of samples per period are thus inversely proportional to the signal duration. Thus, the longer the signal, the lower the accuracy of the calculated mean.

The above example shows that digital calculation of the mean from raw data is problematic. An analysis on filtering the switch-node voltage is presented below.

***Low-Pass Filtering the Switch-Node Voltage***

Consider the harmonics of the switch-node voltage waveform. The switch-node voltage waveform can be represented by a pulse train with a frequency equal to the switching frequency of the buck converter. Figure 4.3 (a), shows an ideal pulse train in the time domain with frequency $\frac{1}{T}$. The corresponding harmonics in the frequency domain is shown in Figure 4.3 (b) where the DC component is given by $a_0 = Ad$

and the Fourier coefficient $a_n$ represents the amplitude of the $n^{th}$ frequency harmonic [25].




$$d = \frac{k}{T}$$

$$a_0 = Ad$$

$$a_n = \frac{2A}{n\pi}\sin(n\pi d)$$

**Figure 4.3: (a) A pulse-train signal waveform in the time domain**
**(b) Harmonics of a pulse-train signal**

In steady-state, the switch-node voltage contains the pulse train harmonics above, with the lowest harmonic, after the DC component, being the switching frequency. (The harmonics probably include high frequency switch-node ringing harmonics as discussed in Chapter 3 as well as high frequency noise). Passing the switch-node voltage through an analogue low-pass filter, with a cut-off frequency below the switching frequency will maintain the DC component of the signal and attenuate the higher frequency components. This is illustrated in Figure 4.4, on the next page. The sampling of the filter's output signal is explained below.

If the filtered signal is sampled by an oscilloscope to calculate the mean as shown by the stars on the filter output signal in Figure 4.4, the samples oscillate about the DC component. Calculating the mean from these samples will yield a more accurate DC component calculation as compared to the example from Figure 4.2, in the

previous subsection. The higher the order of the filter, the better the representation of the DC component. This is especially true if the number of samples per period are reduced. Therefore, given the existing oscilloscope with its limitations, adding the low-pass filter to the technique will give better results than using the oscilloscope on its own.

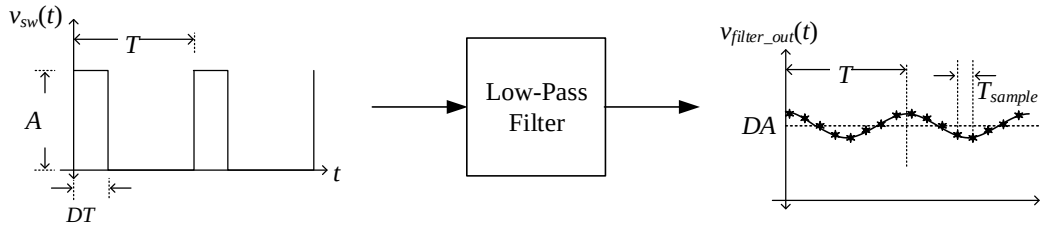



**Figure 4.4: Passing the switch-node voltage through a low-pass filter**

## 4.3 Filter Frequency Response Design

The low-pass filter design is separated into the cut-off frequency selection and the filter order selection described below.

### 4.3.1 Cut-off Frequency

It has been established in the previous section that the low-pass filter cut-off frequency needs to be less than the switching frequency of the buck converter. However, this requirement alone is not-sufficient. The bandwidth of the controller needs to be considered. This is explained below.

The bandwidth of a controller is related to its transient response as discussed in [41]. When there is a step change in load current, the inductor current and output voltage respond to the transient with a settling time that is dependent on the controller bandwidth. In general, the higher the bandwidth, the quicker the response or settling time [42]. In [35] it is stated that point of load buck controllers are typically designed with a bandwidth that is approximately $1/10^{th}$ or $1/12^{th}$ of the

switching frequency. (It could be designed to lower than 1/12$^{th}$ the switching frequency, according to some examples in [34]. However, it is unlikely that a controller bandwidth will be higher than 1/10$^{th}$ of the switching frequency).

The requirement of the switch-node voltage filter is to have the same bandwidth as the controller (or higher) to allow the transient response time of the filter to be approximately equal to the controller. For example, if there is a step change in a DC current from $I_{low}$ to $I_{high}$, the output of the filter needs to respond to this change at the same rate as (or faster than) the output voltage, in order for the model to be applied separately for the current $I_{low}$ and $I_{high}$. Thus, the cut-off frequency $f_c$ of the filter should be approximately equal to the controller bandwidth $f_{bw}$, or between $f_{bw}$ and the switching frequency $f_{sw}$ i.e. $f_{bw} \leq f_c < f_{sw}$.

From the above limitations, the bandwidth and switching frequency of the target test devices need to be considered. Recall from the Research Methodology in Chapter 2, that the experimental analysis of this technique will be conducted on two target devices. Firstly, on a synchronous buck within a *Power Supply Module*, where the load is controllable, which can be referred to as *Test Device A.* Secondly, on a buck converter within an embedded system, which can be referred to as *Test Device B.* For *Test Device B*, the load of the buck converter is an actual processor running software operations. The details and schematics of these devices appear in Appendices A and B and their operation will be discussed in detail in Chapters 6 and 7. For the purpose of the filter design, only the controller bandwidths of the test devices are discussed below.

When the filter was designed, it was designed for its applicability to *Test Device A.* *Test Device A* has a switching frequency of 600 *kHz*. There is no evidence of converter bandwidths designed for $f_{bw} > \frac{f_{sw}}{10}$. So at most, the bandwidth of *Test Device A* is $f_{bw} = 60\ kHz$. The cut-off frequency of the filter was selected to be approximately 100 *kHz* to fulfil the requirement that $f_{bw} \leq f_c < f_{sw}$ for *Test Device A.*

The decision to include *Test Device B* in the testing of this technique, was made subsequent to the filter cut-off frequency selection and design. The switching frequency of *Test Device B* is 1.5 *MHz.* If at most, the bandwidth of *Test Device B* is $f_{bw} = \frac{f_{sw}}{10}$ , then it can be assumed that $f_{bw} \leq 150\ kHz$. The cut-off frequency requirement at approximately 100 *kHz* is 50 *kHz* less than the maximum possible bandwidth. This is insignificant when compared to a decade on the logarithmic frequency scale on a Bode plot. Therefore, the filter with the cut-off at 100 *kHz* could also be applied to *Test Device B.*

### 4.3.2 Filter Order

In order to preserve the DC component of the switch-node voltage, the gain of the filter is expected to be 0 *dB* for the filter's passband frequencies. For a *100kHz* cut-off frequency, the ideal first to fourth order low-pass filter responses are shown on the Bode Plot in Figure 4.5. For a switch-node voltage signal with 600 *kHz* switching frequency (based on *Test Device A*), the first order RC filter (like the filter designed in [24], reviewed in Chapter 1) will yield a 15 *dB* attenuation at the switching frequency. This corresponds to approximately 18 % of the magnitude of the switching frequency harmonic. From the description in Section 3.2 on oscilloscope sampling, the requirement is to reduce the switching frequency harmonic to produce an approximately DC result. Hence the switching ripple of 18 % is too high and a higher order filter is required.

For a switch-node voltage signal with a 600 *kHz* switching frequency, the second to fourth order responses yield a filter output attenuation of 30 *dB*, 47 *dB* and 62 *dB* respectively. The greater the attenuation of the switching frequency component, the better the measurability of the DC and low-frequency components of the signal. If the attenuation of the switching frequency is not large enough, an undesired ripple voltage will be seen at the output of the filter resulting in measurement errors dependent on sampling rate as mentioned above in Section 3.2.

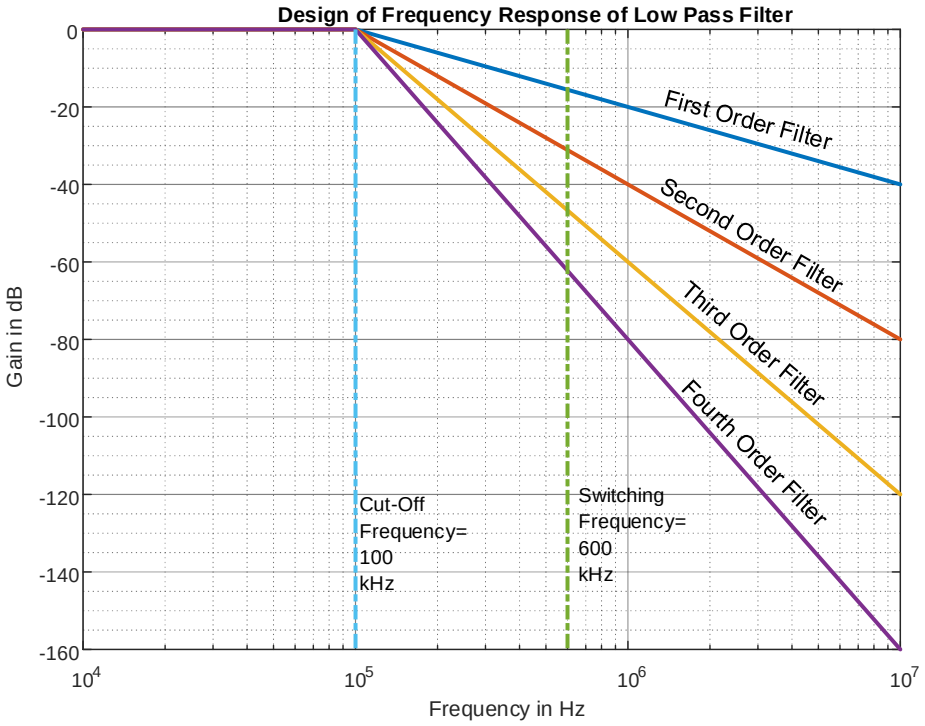



**Figure 4.5: Ideal frequency response Bode plot of first to fourth order low-pass filters with a 100 *kHz* cut-off frequency**

Generally, in practice, noise, component tolerances and parasitic effects affect the filter performance. Typically, a fourth order filter, for example, does not exactly behave as such but it behaves as a lower order filter. This effect is evident in the filter testing in Section 3.5. The attenuation of the switching frequency for a third order filter for *Test Device A* is 47 *dB* which corresponds to approximately 0.5 % of the magnitude of the switching frequency harmonic. This attenuation is good and would result in an acceptable filtering of the switch-node voltage. However, to allow for noise interference and parasitic effects, the filter order was selected as fourth order, resulting in ideally a 62 *dB* attenuation at the switching frequency. This corresponds to 0.08 % of the switching frequency harmonic. This should safely yield a filter output that appears as DC for the switch-node voltage with a steady-state load on *Test Device A.*

For the switching frequency of *Test Device B* the attenuation at the 1.5 M*Hz* switching frequency is approximately 85 *dB* which results in greater attenuation

than that of *Test Device A.* Hence, applying a filter with this frequency response to the switch-node of *Test Device B* will also provide good attenuation at its switching frequency.

Figure 4.5 also shows that for a fourth order filter, if the cut-off frequency is increased, the attenuation of the switching frequency component will be reduced. This is unwanted. The desired response is therefore given by the 100 *kHz* fourth order low-pass filter frequency response.

## 4.4 Filter Circuit Design

For this application, the DC component of the input signal needs to be preserved, ideally with a *0dB* gain, and a sharp roll-off at the cut-off frequency is required. A Butterworth filter provides maximum passband flatness and was thus selected for this application [43].

There were two possibilities with regards to the type of filter circuit design:

1) An active fourth order Butterworth filter designed using a filter design technique presented in texts such as [43] and constructed with discrete op amps, and external capacitors and resistors.
2) A filter designed with a dedicated filter IC with enclosed op amps and accurately trimmed capacitors and resistors i.e. the value of the capacitances and resistors are exactly known, and tolerance errors are eliminated.

Several filters were designed, each using a dedicated filter IC. These filters were compared with a filter that was constructed using discrete op amps. The results of the comparison is given in Appendix C. The filters constructed with filter IC's behaved closer to the designed frequency response when compared to the filter constructed with discrete op amps. The filters constructed with dedicated filter ICs were advantageous due to the minimisation of tolerance errors. Also, the enclosed capacitors and resistors endure less electromagnetic interference when compared to external capacitors and resistors. As a result, the DC behaviour of the discrete filter

was also more susceptible to noise compared to filters constructed with filter IC's. This is evident in the results in Appendix C. The best performing filter IC, based on the results in Appendix C, was selected for this work and is discussed below.

The *LTC1563* [44] was selected for this application. It contains two active second order filter blocks and is designed to give a unity-gain fourth order Butterworth response. The cut-off frequency is selected by a single resistor value $R$ calculated using (4.2) where $f_c$ is the cut-off frequency [44]. The value of $R$ was selected at $R = 22\ k\Omega$ (1% tolerance) to achieve a cut-off frequency of 116 *kHz*. The resistors with value $R$ were connected to the filter IC as indicated in the datasheet [44]. The circuit diagram is given in Figure 4.6 where $V_{in}$ is the filter input and $V_{out}$ is the filter output voltage with respect to ground. A simulation model of the *LTC1563* by *Linear Technology* is found in the *LTspice* component library. The simulated frequency response is shown with the results in the next section.

$$R = 10k\left(\frac{256\ kHz}{f_C}\right) \tag{4.2}$$

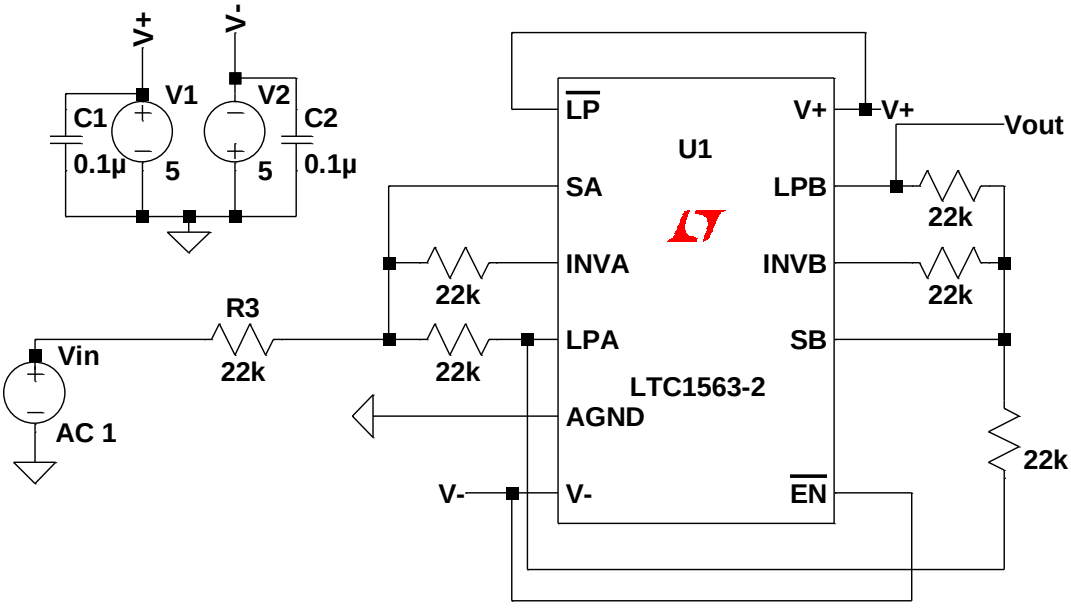



**Figure 4.6: Low-pass filter circuit diagram using LTC1563 filter IC**

## 4.5 Filter Circuit Experimental Testing

The filter circuit from Figure 4.6 was tested experimentally under three conditions. Firstly, an AC sweep of the input voltage was performed to test the frequency response. Secondly a DC sweep was performed to test the gain of the filter with a pure DC input. Lastly, a pulse train with varying duty cycles was applied and the DC components at the input and output of the filter were measured.

### 4.5.1 Frequency Response

The circuit from Figure 4.6 was built and a function generator [45] was used to produce a 2 *V* input sine wave. The frequency was swept from 1 *Hz* to 1 *MHz*. The input and output peak voltages ($v_{in_{peak}}$ and $v_{out_{peak}}$ respectively) were measured on a digital oscilloscope [46] and the gain was calculated according to (4.3).

$$Gain_{AC} = 20 \log \left| \frac{v_{out_{peak}}}{v_{in_{peak}}} \right| \tag{4.3}$$

A simulation of the circuit in Figure 4.6 was performed as well. A simulation model of the *LTC1563* by *Linear Technology* is found in the *LTspice* component library. The circuit was simulated in *LTspice* by performing an *AC analysis* with a 2 *V* sine wave to yield the simulated frequency response over the range 1 *Hz* to 1 *MHz*.

The results of the experimental frequency response testing were compared to the simulation results as well as the response of an an ideal fourth order low-pass Butterworth filter with transfer function given in (4.4) [43]. The results are given in Figure 4.7.

$$G(s) = \frac{1}{(1+0.7654s+s^2)(1+1.8478s+s^2)} \tag{4.4}$$

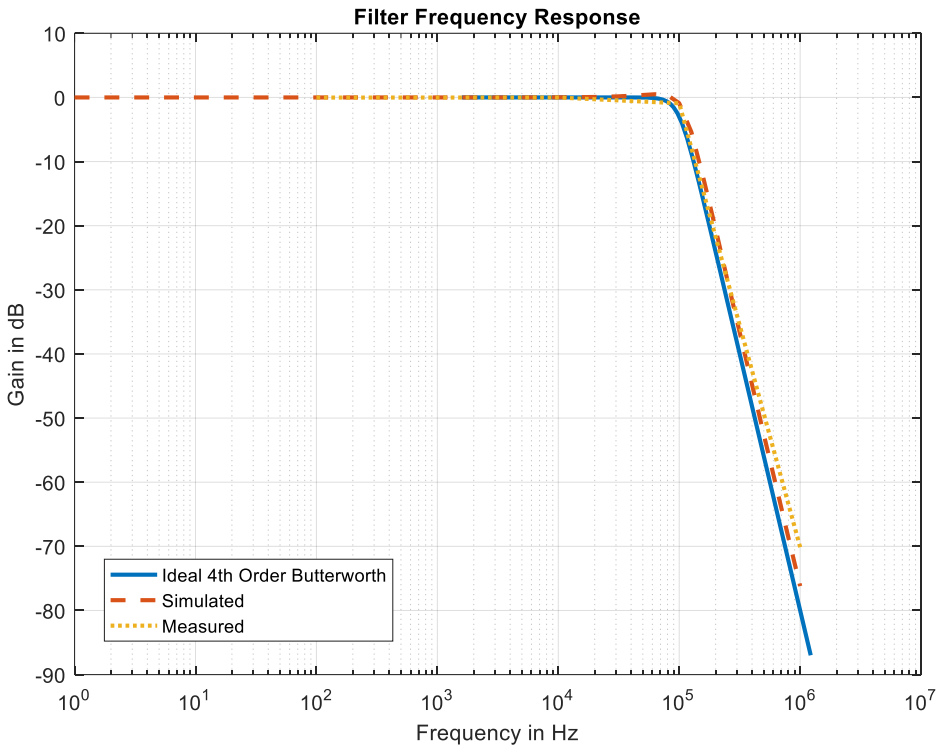



**Figure 4.7: LTC1563 filter circuit frequency response testing**

The results from Figure 4.7 show that there is approximate agreement between the frequency response of an ideal fourth order Butterworth Filter, shown by the solid line, and the simulated frequency response of the *LTC1563*, shown by the dashed line. As predicted in the previous section, the frequency response from the practical measurements on the built circuit, showed a slightly lower order than fourth order as shown by the dotted line in Figure 4.7 . Nonetheless, the practical filter has an attenuation of approximately -60 *dB* at the 600 *kHz* frequency. This is in accordance with the required attenuation mentioned in Section 4.3.2 under the filter frequency response design.

### 4.5.2 Pure DC Response

A DC sweep of the input voltage from Figure 4.6 was performed. The voltage was swept from 1 *V* to 5 *V* using a precision voltage source [45]. The input and output

voltages ($V_{in}$ and $V_{out}$ respectively) were measured with a digital multimeter (DMM) [47]. The DC gain was calculated from (4.5). The results are shown in Figure 4.8.

$$DC\ Gain_{DC} = 20 \log \left|\frac{V_{out}}{V_{in}}\right| \tag{4.5}$$

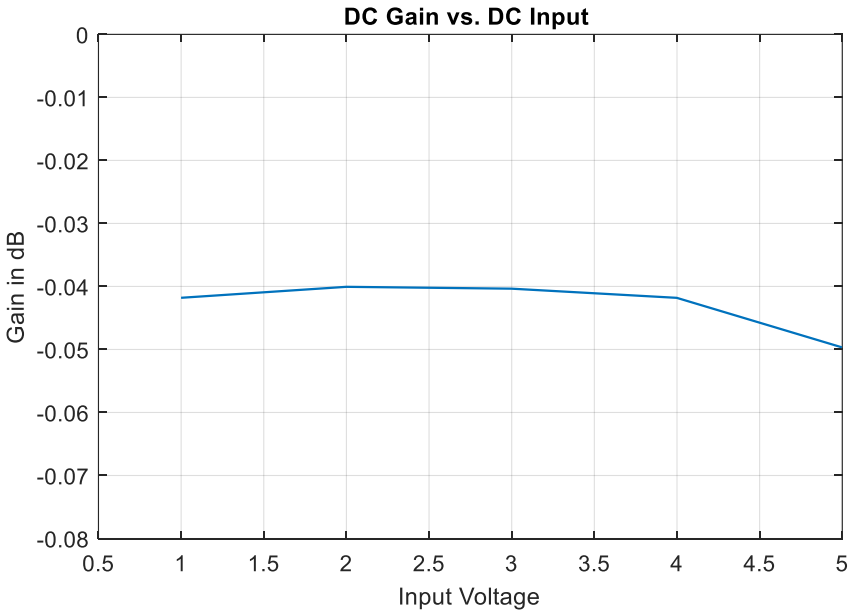



**Figure 4.8: Filter response to a pure DC input signal**

The results in Figure 4.8 show that the DC gain remained approximately constant for input voltages less than the rail voltage of 5 *V*. The reason for the deviation at a DC input of 5 *V* is that according to the *LTC1563* datasheet [44], the typical output voltage swing for a ±5 *V* supply is 4.9 *V*. Therefore, it is not possible for a DC input of 5 *V* to follow the trend because it is not within the specified operating conditions. This is acceptable since the maximum DC component of the signal required to be filtered by the test devices (in Chapters 6 and 7) is not expected to exceed 3.3 *V*.

### 4.5.3 Pulse-Train Response

A 600 *kHz* 5 *V* pulse-train was applied at the input of the filter circuit in Figure 4.6. The signal was generated using a function generator [45]. The duty cycle of the

signal was varied from 30 % to 70%. The DC component of the input and output voltages ($V_{in}$ and $V_{out}$ respectively) were measured with a digital multimeter (DMM) in DC Mode [47]. The gain of the DC components of the pulse-train was calculated from (4.5). The results are shown in Figure 4.9 as a function of the duty cycle (top x-axis) as well as the DC component of the input voltage signal (bottom x-axis). The DC component of the input signal is referred to as $V_{in}$ in (4.6)

$$DC\ Gain_{PT} = 20 \log \left| \frac{V_{out}}{V_{in}} \right| \tag{4.6}$$

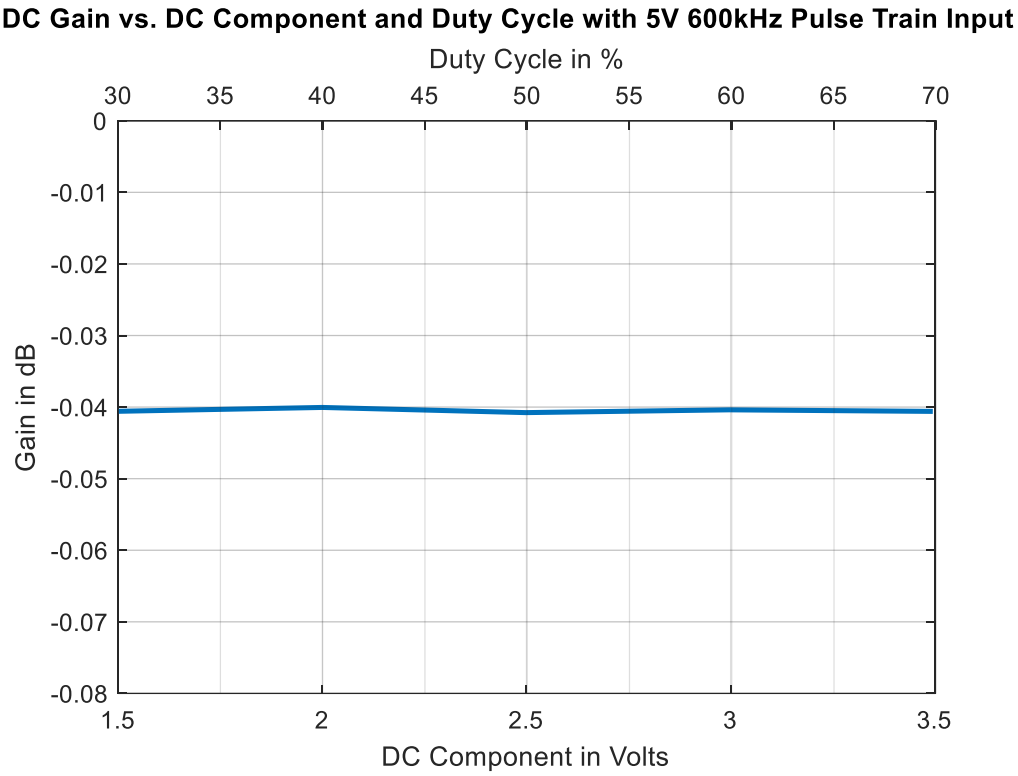



**Figure 4.9: Pulse train response of the filter**

The results in Figure 4.9 show that the DC gain with a pulse-train input agreed with the pure DC gain measured in the previous subsection. The DC gain measured from the pulse-train input thus validates the DC gain measured with pure DC input signals. These results are discussed below.

## 4.6 Discussion

The frequency response results of the low-pass filter showed that at 600 *kHz* as well as at 1.5 *MHz* (the switching frequencies of the test devices) the attenuation is greater than 60 *dB.*

The DC gain that was measured was approximately constant for the required range of pure DC input voltages. The DC gain was validated by measuring the same DC gain with a pulse-train input instead of a pure DC input.

The filter can therefore be employed to average the switch-node voltage in a buck converter with a switching frequency greater than 600 *kHz.* The DC gain can be factored out of the filter output voltage to estimate the DC component of the switch-node voltage.

The filter can be incorporated into the current estimation technique using the steady-state model from Chapter 3 as illustrated by the block diagram in Figure 4.10. This technique solves for average current for a given period of time.

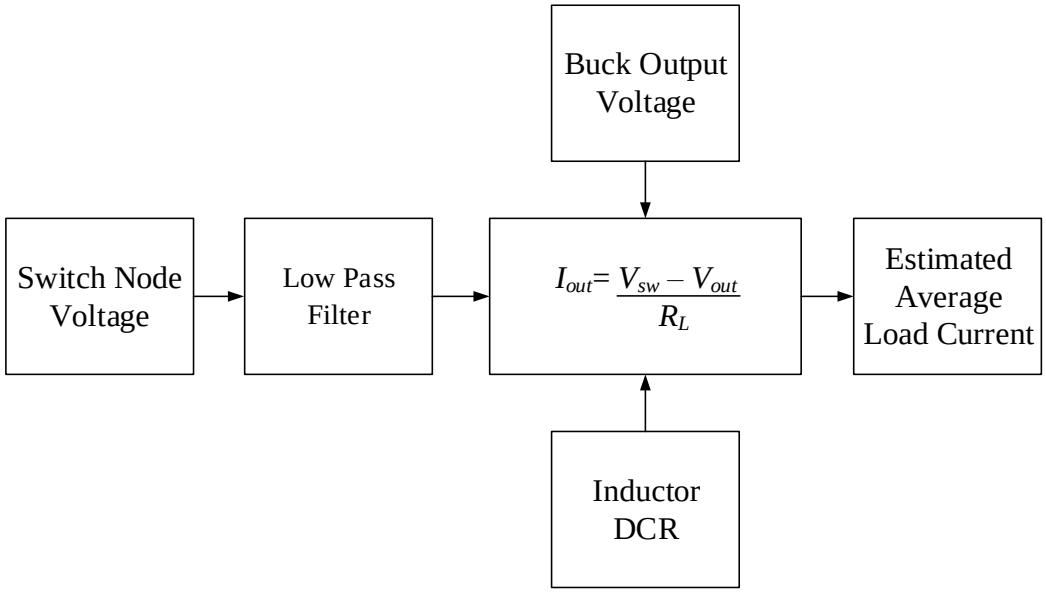



**Figure 4.10: Incorporating the low-pass filter into the average current estimation technique**

## 4.7 Conclusion

A justification for the requirement of a low-pass filter for this current estimation technique was presented. A low-pass filter obtains a more accurate DC component compared to a calculation of the DC component from samples of the switch-node voltage.

The frequency response of the filter was required to have:

- A 0 *dB* gain for the passband frequencies
- A cut-off frequency that is greater than the bandwidth but less than the switching frequency
- A steep roll-off to attain good attenuation at the switching frequency

Based on the switching frequencies of the target test devices, the cut-off frequency was selected at 100 *kHz* and the order of the filter was selected as fourth to achieve good attenuation at the switching frequency of the test devices.

The circuit was designed using a dedicated filter IC. The circuit was built and tested under three input conditions i.e. AC sweep, DC sweep and pulse-train with varying duty cycles. The performance of the filter was close to that of an ideal fourth order Butterworth filter and the DC gain was consistent for the DC sweep and pulse train conditions. The filter was incorporated into the current estimation technique using the steady-state model derived in the previous chapter.

The next chapter presents the simulation of a point of load buck converter with the low-pass filter connected at the switch-node. Various load current conditions are simulated, and the filter output is analysed to validate the current estimation technique.

# 5 SIMULATION VERIFICATION OF THE CURRENT ESTIMATION TECHNIQUE

## 5.1 Introduction

In Chapter 3, a steady-state and dynamic model of the load current in a buck converter is derived. In Chapter 4, a low-pass filter is designed such that the steady-state model and low-pass filter form part of the average load current estimation technique. This chapter shows the results and analysis of simulating this technique under various load conditions. Since simulation results are based on mathematical models of the circuit components, if there is agreement between the simulation results and the load current models, the simulation results can validate the load current models derived. The simulation results presented in this chapter validate the derived models from Chapter 3 using the filter designed in Chapter 4. Hence the overall current estimation technique is validated. It also shows and explains the effect of a load transient on the filter output voltage.

## 5.2 Simulation Circuit

A 1 *MHz* 5 *V to* 1.8 *V* point of load (POL) synchronous buck converter simulation circuit was designed in the *Advanced Controller Techniques* course presented on the Coursera platform by *The University of Colorado Boulder* [35]. This course is a design course for the design of current mode controllers. The content from this course is open-source and the simulation circuit designed in [35] was used to test the low-pass filter current estimation technique. The complete circuit diagram of the simulation circuit appears in Figure 5.1 and each section of the circuit is described thereunder.

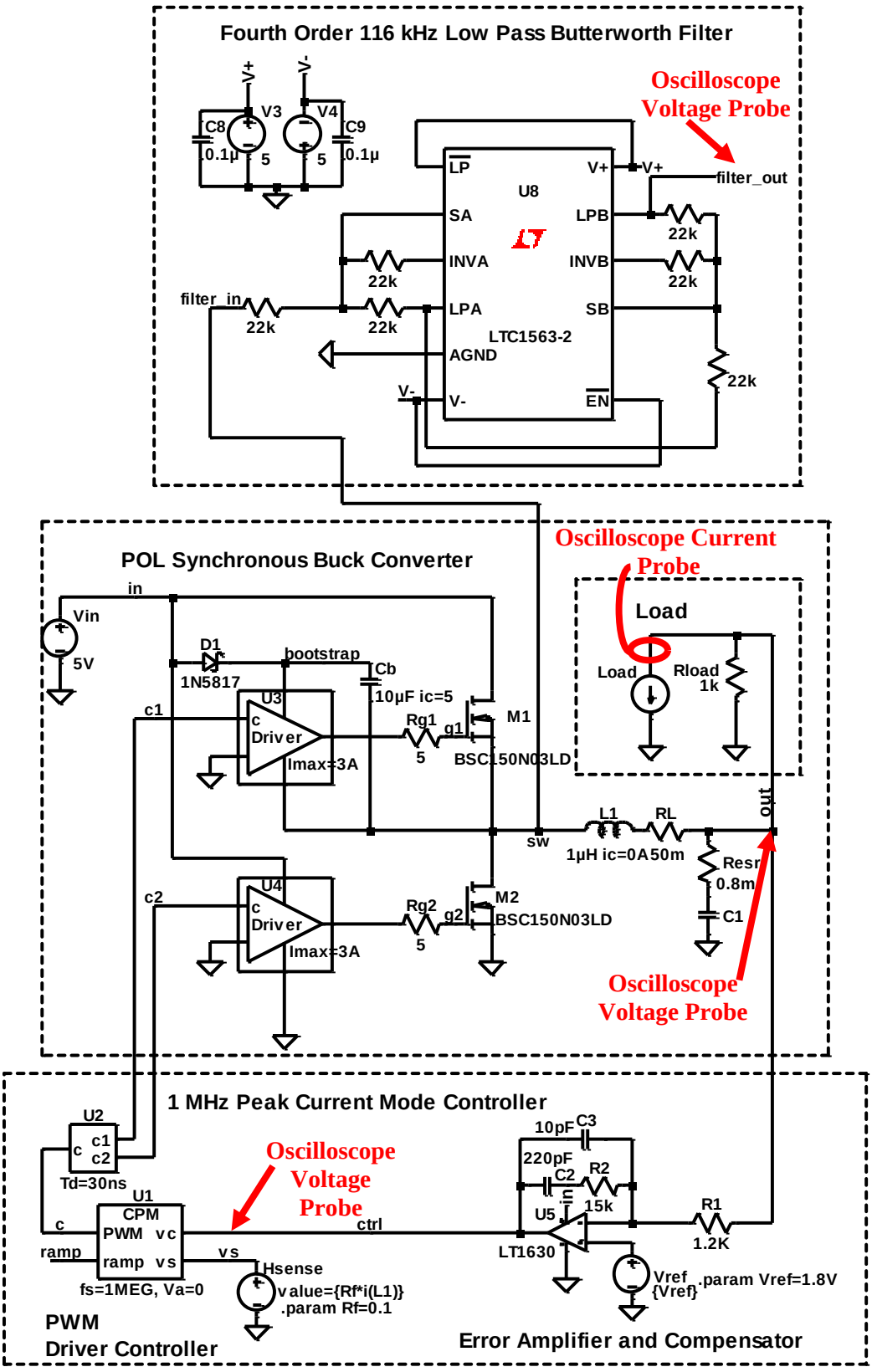



**Figure 5.1: Simulation circuit of a synchronous buck converter with the low-pass filter connected at the switch-node**

In the circuit in Figure 5.1, there are three distinct parts i.e. the POL synchronous buck converter, its controller and the low-pass filter connected at the switch-node of the buck converter.

In the buck converter, *M1* and *M2* are the switching high and low-side MOSFETS respectively. The inductor *L1* and capacitor *C1* are the filter stage of the synchronous buck. The DCR of the inductor is modelled by a 50 $m\Omega$ series resistor. The load of the buck converter is represented by a 1 $k\Omega$ resistor in parallel with a current source. The 1 $k\Omega$ resistor ensures that the minimum load current is 1.8 *mA* given that the buck converter output voltage is 1.8 *V*. As will be discussed, the range of load currents used in the simulations shown in this chapter are between approximately 180 *mA* and 800 *mA*, which is large in comparison to 1.8 *mA*. The current source in these simulations thus dominates the current requirements of the load.

The controller employs inductor current sensing to perform peak current mode control of the buck converter with a 100 *kHz* bandwidth [35], [48]. Recall that the requirement of the filter cut-off frequency is for it to be greater than or equal to the bandwidth of the controller (and less than the switching frequency). Given the 100 *kHz* bandwidth of this simulated controller, the design specifications of low-pass filter designed in the previous chapter may be applied. The switch-node of the buck converter circuit is hence connected to the input of the fourth order low-pass filter circuit designed in the previous chapter.

The output of the filter is connected to an oscilloscope voltage probe with respect to ground for analysis. Oscilloscope voltage probes with respect to ground are also connected at the controller input and at the buck converter output. A current probe is connected at the load to analyse the load current. The reason for connecting

oscilloscope probes for analysis of these voltage and current signals is elaborated in the next section.

## 5.3 Simulation Procedure

The simulation circuit was run under four different load conditions. These conditions are listed and explained as follows:

1) *DC load.* The DC load was run to validate the steady state load current model of the buck converter.
2) *Low-frequency AC load.* Low frequency in this context refers to lower than or equal to the bandwidth of the controller. The dynamic current model of the buck converter is valid for frequencies less than the controller bandwidth hence the low-frequency AC load was run to validate the dynamic current model of the buck converter.
3) *High frequency AC load*. High frequency in this context refers to greater than the bandwidth of the controller. The high-frequency AC load was run to show the frequency limitation of the dynamic current model of the buck converter.
4) *Load transient.* A transient load was run because typically, in an embedded system, it is expected that the processor draws current and there is a transient between one current level and the next. The effect of a load current transient on the current estimation technique was hence simulated. (The results from the AC simulations help to explain the transient effects.)

For each load, the waveforms recorded were:

1) The load current waveform *I(load).* This was to observe the load and the load fluctuations if present.
2) The duty cycle control voltage waveform *V(ctrl).* The control voltage signal controls the pulse width of the PWM signal controlling the gate drivers of the MOSFETs and thus is proportional to the duty cycle of the converter. It was plotted to note the variation in duty cycle.

3) The output of the low-pass filter *V(filter_out)*. This signal is essentially the analogue average of the fast-switching switch-node voltage which the model is dependent on. The switch-node is labelled *sw* in the simulation circuit in Figure 5.1. The switch-node voltage is the input of the low-pass filter.
4) The output of the buck converter *V(out).* This was plotted to obtain the output voltage of the buck converter since the buck converter load current model from Chapter 3 is dependent on the output voltage of the buck converter.

For each load, except for the transient load, the limits of the time axes were equal. This is to be able to clearly note the effect that each load has on the waveform over the given time period. It should also be noted that the resolution of the voltage measurements was 0.1 *mV*. This is typical for simulations but is not always a realistic resolution in practical measurements. The description and results of the simulation of each load appears below. The results are analysed to determine the validity of the current estimation technique.

## 5.4 Simulation Results and Analysis

### 5.4.1 DC Load

To validate the steady-state model, the current source representing the load was set to a DC value of 700 *mA*. This current value was chosen because it represents typical operating current in the *Test Devices A and B* in Chapters 6 and 7. The corresponding waveforms are shown in Figure 5.2 and an analysis appears below.

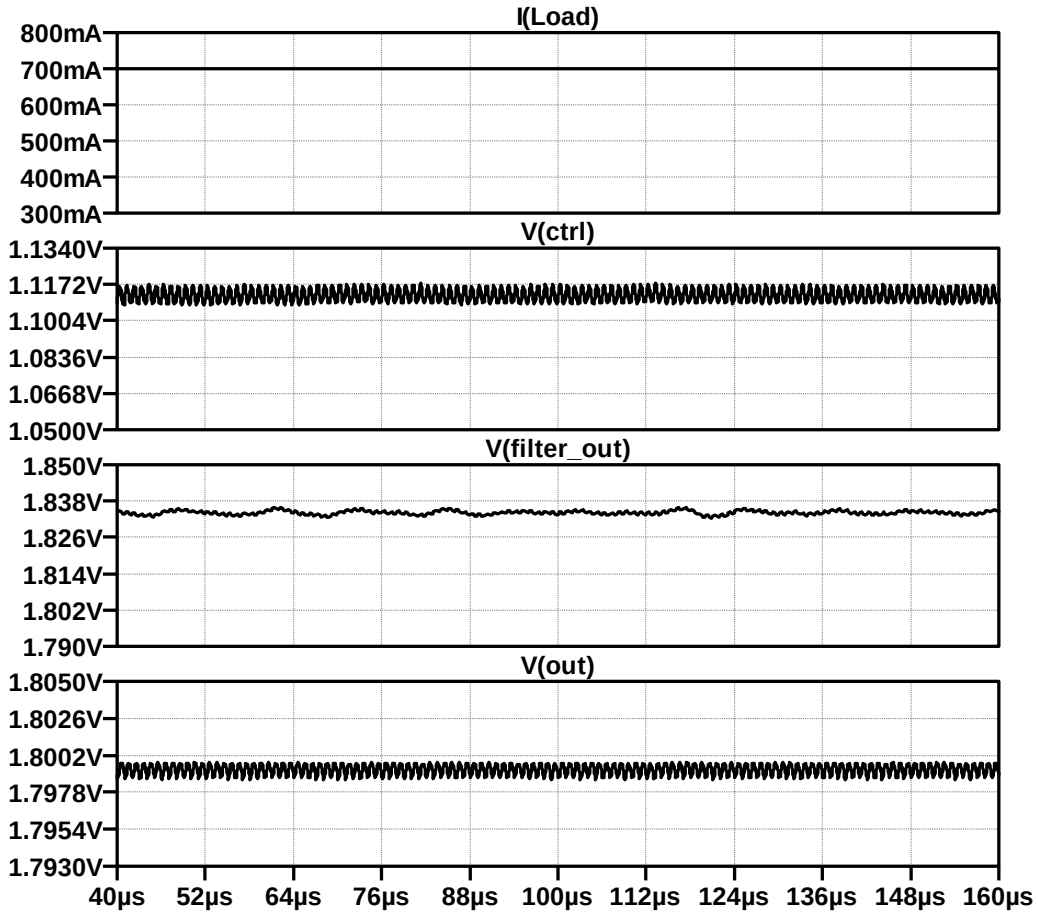



**Figure 5.2: Simulation waveforms for a DC load current**

From the waveforms in Figure 5.2, it can be seen that while the current is constant, the duty cycle control voltage *V(ctrl)* does not modulate and only contains switching ripple. Similarly, since the converter is in steady-state, the output voltage *V(out)* does not contain any variations other than switching ripple.

The switching ripple in the filter output voltage *V(filter_out)* is attenuated more than the switching ripple of the output voltage. However, the filter output voltage contains some small low-frequency components that have passed through the filter. These low-frequency components are present in the inductor current plotted in Figure 5.3. The time domain signal of the inductor current in Figure 5.3, does not clearly show the low-frequency components. An FFT analysis of the inductor current and filter output waveform was performed in *LTspice* and the results are shown in Figure 5.4. (The Fourier components are normalised to correspond to the

time domain RMS amplitude.) In Figure 5.4, it can be seen that the low-frequency components (below 100 *kHz*) of the inductor current are also present at the filter output. This is suspected to be the effect of the PWM driver within the controller, shown in the simulation circuit in Figure 5.1. The PWM driver contains a clock and performs discrete sampling in order to synchronise the switches to the controller. This introduces the additional harmonics to the inductor current. Since the low-frequency components of the switch-node voltage is dependent on inductor current (as shown in *Step Six* of Section 3.3.2), the low frequency components of the inductor current are seen at the filter output. These controller effects do not affect the current estimation results as will be shown below.

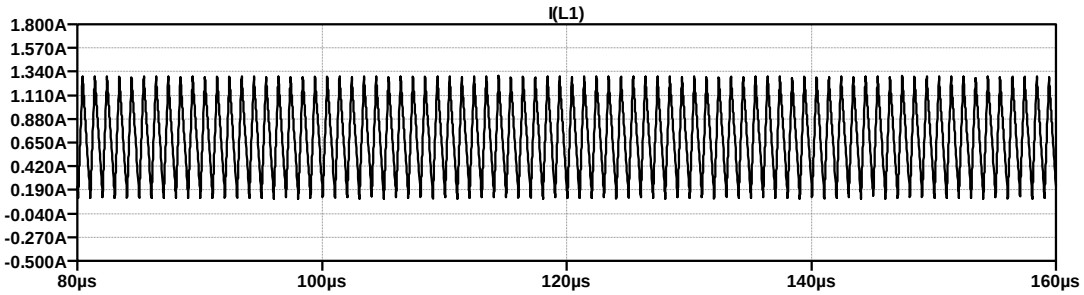



**Figure 5.3: Simulated waveform of inductor current**

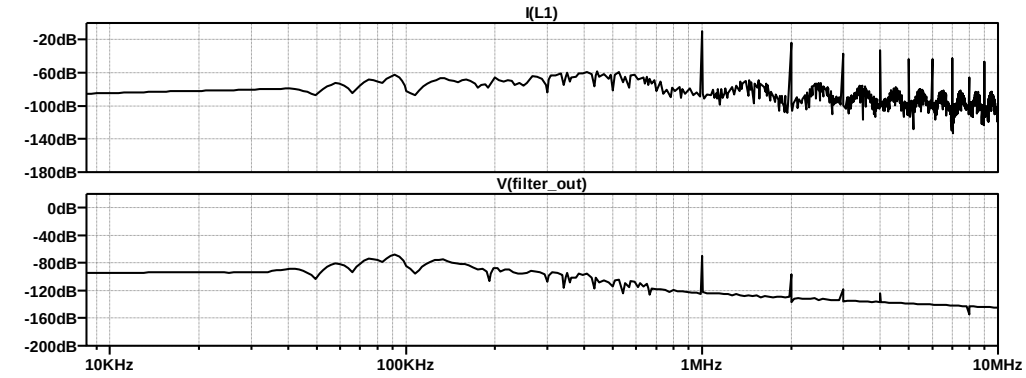



**Figure 5.4: FFT of the simulated inductor current and filter output voltage showing the frequency harmonics**

To apply the model (to calculate the DC current from the filter output voltage signal and the output voltage signal) the DC components of *V(filter_out)* and *V(out)* and the DCR value need to be substituted into the steady-state model in (5.1).

$$I_{out} \approx \frac{1}{R_L}(V_{sw} - V_{out}) \quad (5.1)$$

The *LTspice* waveform viewer can integrate a trace to produce the average or RMS value over a given region. This function was used to determine the following DC voltages from the waveforms:

$V_{sw} = 1.8342\ V$

$V_{out} = 1.7993\ V$

The DCR is given as $R_L = 50\ m\Omega$. Note the precision of the voltage measurements, as discussed earlier, is 4 digits or a resolution of 0.1 *mV*. Maintaining this precision improves the accuracy of the estimated current. Maintaining this precision when substituting steady-state load current model in (5.1) yields an estimated DC current of 698 *mA.* This corresponds to an error of 0.3 %. This mathematically validates the steady-state model and use of the low-pass filter to average the switch-node voltage.

The above simulation experiment was repeated for a range of DC load currents in 200 *mA* increments from 200 *mA* to 1.2 *A.* This range was chosen because it represents typical operating conditions of *Test Devices A and B* used for experimental validation of this work as shown in Chapters 6 and 7. For the entire range of DC currents simulated, less than 1 % error in the estimated load current was evident.

### 5.4.2 Low-frequency Dynamic Load

To validate the dynamic load current model, a 10 *kHz* 300 *mA* sinusoidal load with a DC offset of 500 *mA* was simulated. The choice of frequency was chosen to be significantly below the 100 *kHz* bandwidth of the controller due to the frequency limitation of the dynamic current model presented in Chapter 3. This type of load is not expected in an embedded system but it was simulated to validate the dynamic current model, which helps to explain transient effects that will be discussed further

on in Subsection 5.3.4. The simulation waveforms are given in Figure 5.5 and is analysed below.

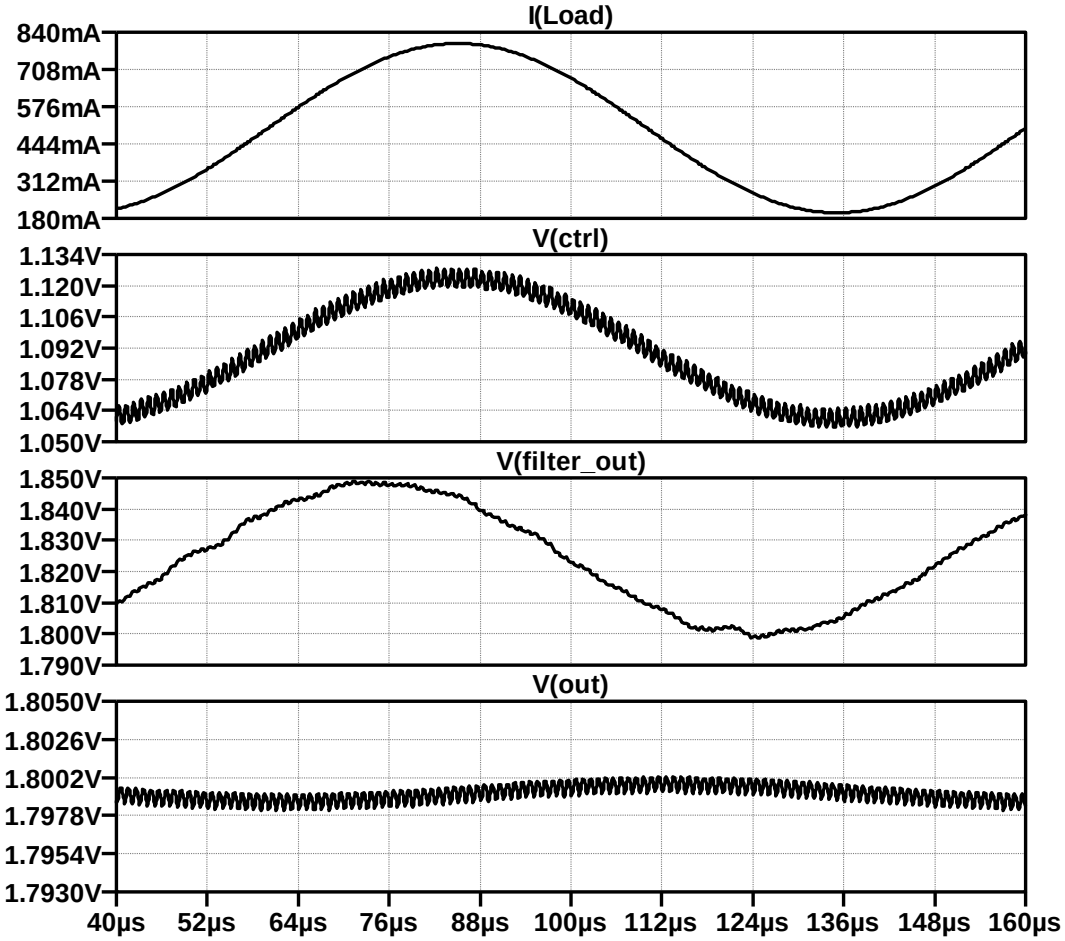



**Figure 5.5: Simulation waveforms for a low-frequency load current**

From the duty cycle control voltage *V(ctrl)* waveform in Figure 5.5 which controls the duty cycle, it can be seen that the duty cycle is approximately in phase with the load current *I(Load)* as stated in the AC model derived in Section 3.3.2 in Chapter 3. Next, refer to the load current *I(Load)* and filter output voltage *V(filter_out)* waveforms. The frequency of *I(Load)* and *V(filter_out)* is 10 *kHz* as expected. The amplitude of the low-frequency component of the voltage is approximately 25 *mV* (the peak-peak voltage is approximately 50 *mV)* and the amplitude of the AC load current is 300*mA.* There is a time delay between the voltage and current waveforms of approximately 11 *µs (*measured using cursors in *LTSpice*). According to the dynamic model, the AC component of the load current and the filter output voltage

behave according to the equivalent circuit in Figure 5.6 and the expression in (5.2). The AC component of the load current *I(Load)* corresponds to $\hat{\imath}(t)$ and the filter output voltage *V(filter_out)* corresponds to $\langle \hat{v}_{sw}(t) \rangle_{T_s}$ in Figure 5.6 and in (5.2).

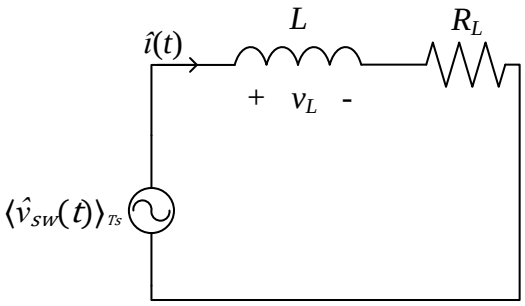



**Figure 5.6: Dynamic load current model of a buck converter**

$$\langle \hat{v}_{sw}(t) \rangle_{T_s} - \hat{\imath}(t) R_L \approx L \frac{d\hat{\imath}(t)}{dt} \tag{5.2}$$

The phasor representation of the model is shown in Figure 5.7. To validate the AC model, the model can be used to calculate the amplitude of the current *I(Load)*, given the filter output voltage waveform *V(filter_out)*. The time delay can also be calculated given the *V(filter_out)* voltage waveform. If the calculated time delay and current amplitude are equal to the simulated time delay and load current amplitude respectively, the AC model is validated. This will be shown below.

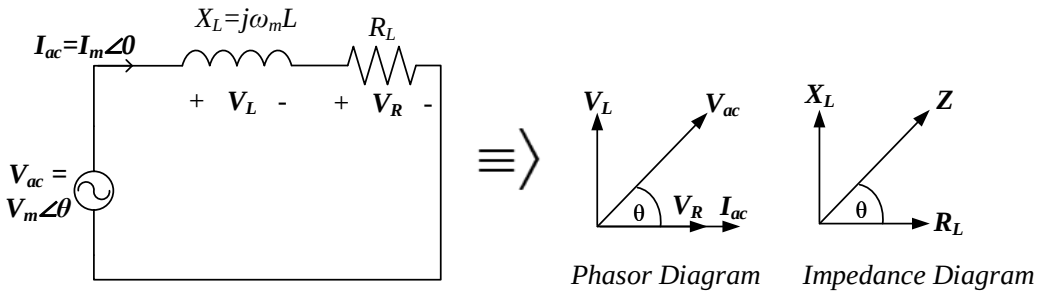



**Figure 5.7: Phasor diagram and impedance diagram representation of dynamic load current model of a buck converter**

First, the time delay visible between the *I(Load)* and *V(filter_out)* waveforms in the in Figure 5.5 will be calculated from the model. The angle $\theta$ in Figure 5.7 is

calculated by $\theta = \tan^{-1}\left(\frac{\omega_m L}{R_L}\right) rad/s$, where $L = 1\ \mu H$ and $R_L = 50\ m\Omega$ from the simulation circuit. This corresponds to a time delay of approximately 14 $\mu s$ at the modulation frequency of 10 *kHz*. The additional 3 $\mu s$ in the time delay is explained from the time delay introduced by the low-pass filter. The simulated frequency response of the low-pass filter is shown in Figure 5.8. It shows that the group delay (represented by the dotted trace) for a 10 *kHz* input signal is approximately -3.6 $\mu s$ at 10 *kHz*. Adding both time-shifts results approximately in the 11 $\mu s$ time shift that is visible.

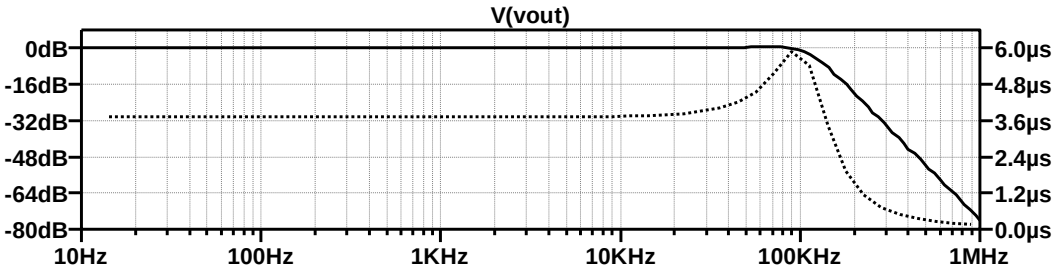



**Figure 5.8: Zoomed in frequency response of the low-pass filter**

Next, from the phasor diagram in Figure 5.7 the magnitude of the current can be calculated from (5.3). The calculation is shown in (5.4) below. The result has an approximately 3.6 % error from the actual load current of 300 *mA*, validating the AC model in Figure 5.6 and Figure 5.7.

$$I_m = \frac{|\boldsymbol{V}_{ac}|}{|Z|} = \frac{V_m}{|\boldsymbol{R}_L + \boldsymbol{X}_L|} \tag{5.3}$$

$$\begin{aligned} &At\ 10\ kHz\ X_L \approx 62.83 m\Omega \\ &I_m \approx \frac{|\boldsymbol{V}_{ac}|}{|Z|} \\ &\approx \frac{25}{\sqrt{50^2 + 62.83^2}} \\ &\approx 311 mA \end{aligned} \tag{5.4}$$

The above calculations validate the dynamic or AC model in Chapter 3. Lastly, refer to the output voltage waveform in Figure 5.5. There is a small modulation

equal to the modulation of the current, but the DC component is maintained. The voltage appears stable within reasonable limits. It is thus valid to approximate the output voltage by its DC component in the AC model.

The DC component of the current can be computed by applying the steady-state model in (5.1). Integrating the voltage waveforms, as was done in the simulation of the DC load in the previous subsection, yielded:

$V_{sw} = 1.8242\ V$

$V_{out} = 1.7993\ V$

Substituting into the steady-state model in (5.1) yields an estimated DC current component of 498 *mV*. This is an error of 0.4 % from the actual DC component. This shows that the steady-state model can be applied to modulating current to determine the DC component of the current.

### 5.4.3 High-Frequency Dynamic Load

The dynamic model validated in the previous subsection was limited frequencies below the bandwidth of the controller as is explained in Chapter 3. To validate the frequency limitation of the dynamic model, a 200 *kHz* 300 *mA* sinusoidal load current with a DC offset of 500 *mA* was simulated. At this modulation frequency, the 100 *kHz* bandwidth of the controller is exceeded. The simulation waveforms are shown in Figure 5.9 and an analysis appears below.

Refer to the *I(load)* and *V(ctrl)* waveforms in Figure 5.9, on the next page. The amplitude of the control voltage signal *V(ctrl)* is lower than the amplitude of the control signal in the low-frequency case in Figure 5.5, despite the current amplitude being the same for both cases. The current is modulating faster than the controller can handle and the duty cycle does not have time to respond and reach the required value. Thus, the output voltage ripple is higher due to the duty cycle being lower than it should be. The output voltage thus contains switching ripple as well as modulation ripple.

Recall that for the AC model to apply, the AC component of duty cycle must be given by $\hat{d}(t) = D_m \sin(\omega_m t)$, where $D_m$ is the duty cycle value that corresponds to the peak current value. For this fast-changing load, this does not apply and the AC model does not apply when the load current bandwidth is exceeded.

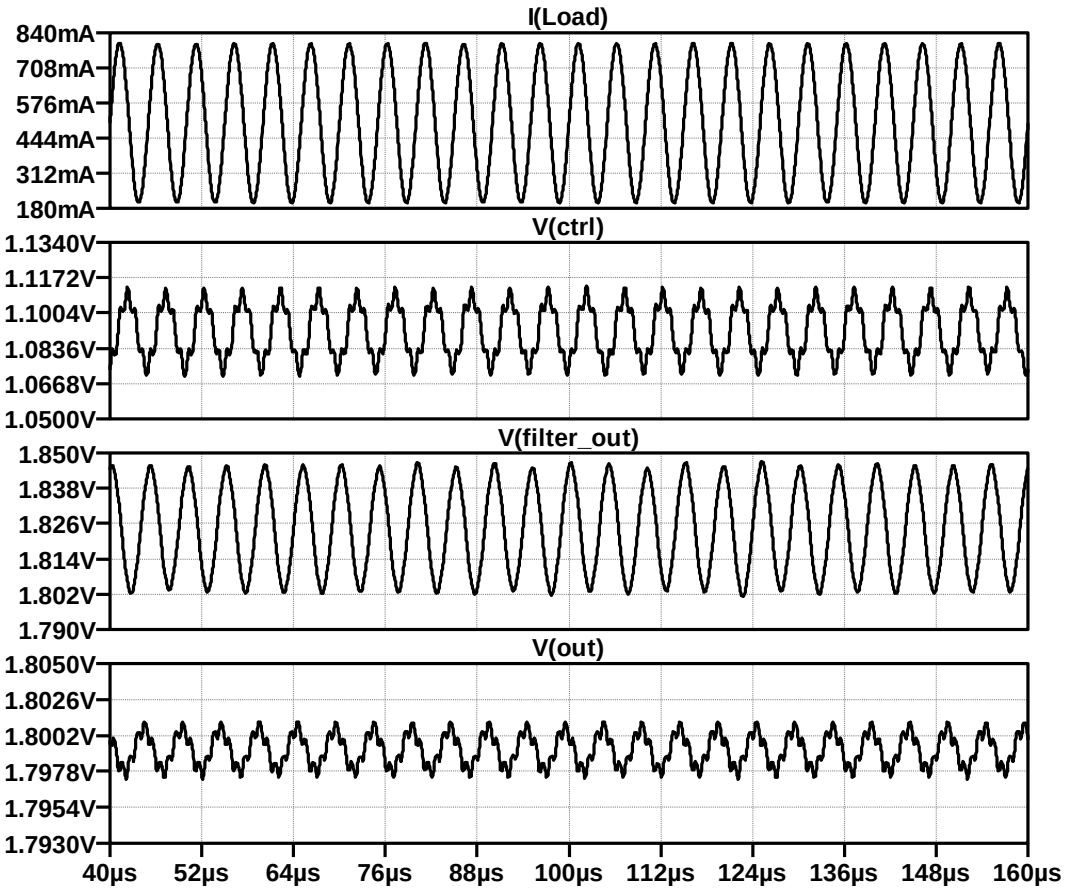



**Figure 5.9: Simulation waveforms for a high frequency loaf current**

However, the steady-state model applies to determine the DC component of the load current. The DC component of the current can be computed by applying the steady-state model in (5.1). Integrating the *V(filter_out)* and *V(out)* waveforms yields:

$V_{sw} = 1.8242\ V$

$V_{out} = 1.7993\ V$

Substituting into the steady-state load current model in (5.1) yields an estimated DC current component of 498 *mV*. This is an error of 0.4 % from the actual DC

component. This shows that the steady-state model can be applied to modulating current, even for high frequencies, to determine the DC component of the current.

### 5.4.4 Transient Load

To determine the effect of a load transient on the developed current estimation technique, a transient load current was simulated by stepping up the load current from 200*mA* to 1 *A* and back down to 200 *mA*. The reason for simulating a transient load is that load transients are expected to occur in embedded systems due to the load being a microprocessor or peripheral device. The low and high values of the transient were chosen based on typical minimum and maximum load current values in the test devices used in this work. The simulation waveforms are given in Figure 5.10 (on the next page) and an analysis appears below.

During the load transients in Figure 5.10, on the next page, the control voltage that controls the duty cycle *V(ctrl)* and the buck converter output voltage *V(out)* respond to the transient according to the dynamics of the controller. Both of these voltages take approximately 10 $\mu s$ to respond to the transients. To explain the behaviour of the *V(filter_out)* waveform at the transients, the inductor current needs to be plotted as well. This is shown by *I(L1)* in Figure 5.11. The filter output voltage *V(filter_out)* is also plotted in Figure 5.11. Figure 5.11 shows that the response time of the inductor current *I(L1)* is also approximately 10 $\mu s$ and a transient spike in the inductor current is observed. The filter output waveform is discussed below Figure 5.11.

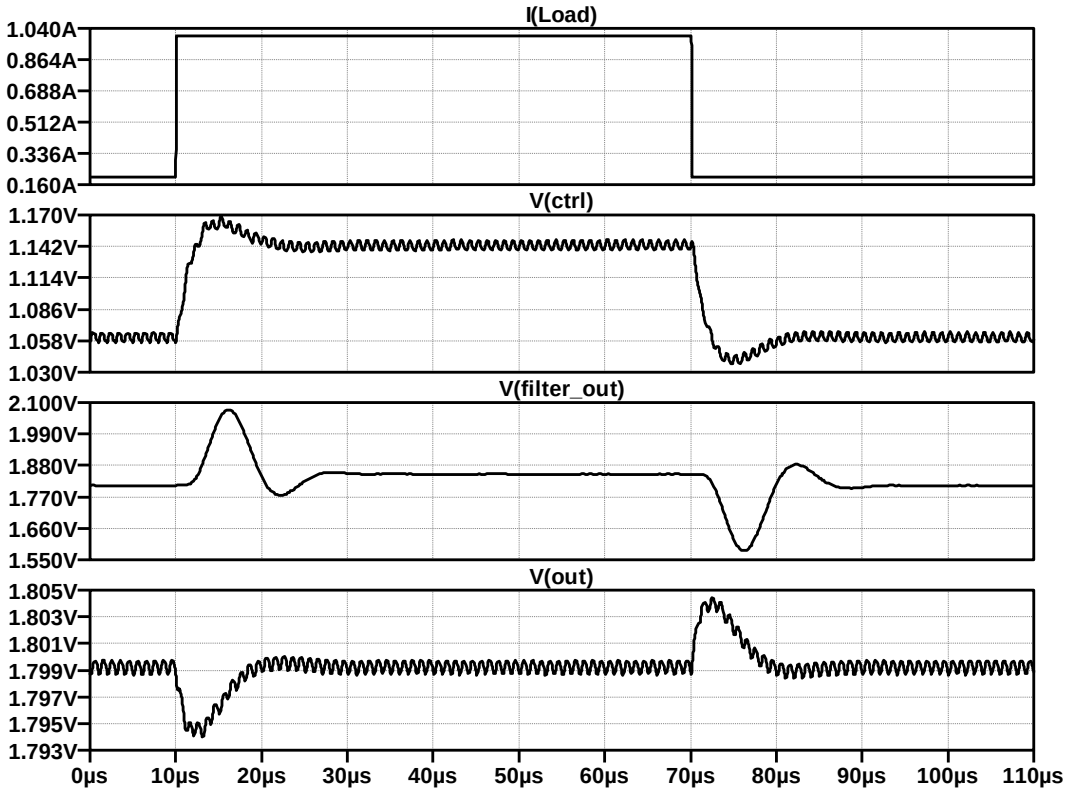



**Figure 5.10: Simulation waveforms for a transient load**

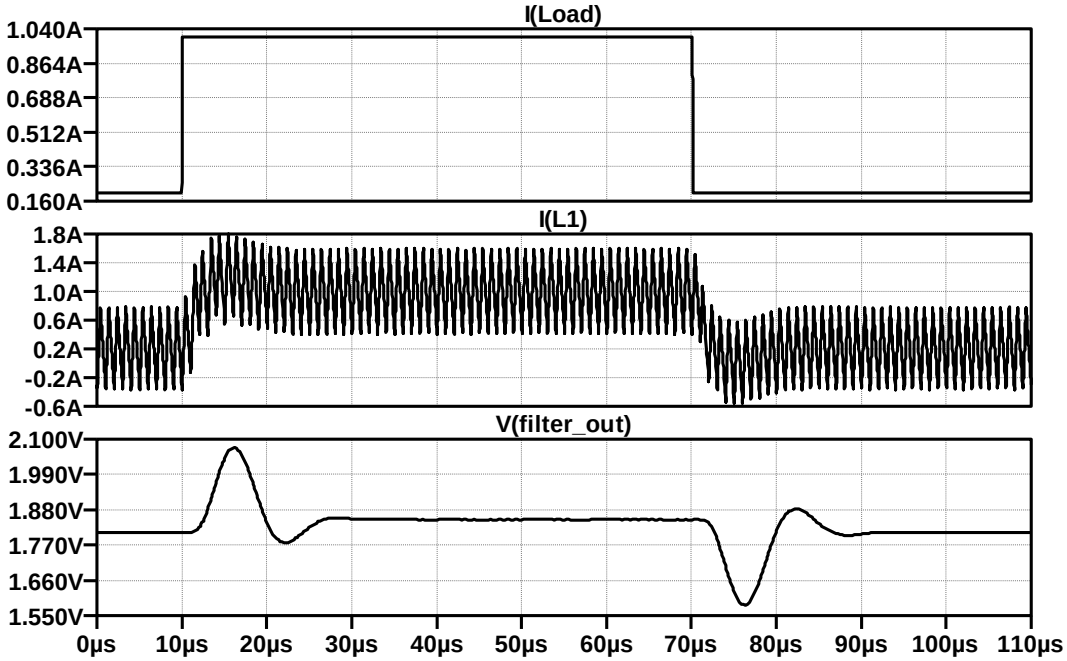



**Figure 5.11: Effect of simulated transient on inductor current and filter output voltage**

The filter output voltage waveform *V(filter_out)* in Figure 5.11 contains a visible spike at the transients. This spike is explained as follows. When the load current contains a transient, the inductor current *I(L1)* in Figure 5.11 responds according to the controller dynamics. For this period of inductor current, the low-frequency dynamic load model in Figure 5.6 (shown in the low-frequency load current simulation in Section 5.3.2) applies. The height of the spike of *I(L1)* is thus dependent on the impedance of the inductor at the low-frequency component of the load transient. This is shown in the calculations in (5.5) – (5.9), below, from the low frequency model explained as follows. Since the response time is approximately 10 $\mu s$, it corresponds to a sinusoidal frequency of 100 *kHz* where the inductance of the inductor is defined in (5.5). The height of the current spike in *I(L1)* was measured using cursors in *LTSPice* and is given by (5.6). The height of the *V(filter_out)* spike is calculated to be approximately 504 *mA*. This agrees with the height of the *V(filter_out) spike* in the simulated waveform, shown in Figure 5.11.

$$At\ 100\ kHz, X_L \approx 628.3 m\Omega \tag{5.5}$$

$$\left|I_{transient_{spike}}\right| \approx 800\ mA \tag{5.6}$$

$$\left|V_{filter_{spike}}\right| \approx \left|I_{transient_{spike}}\right| \times |Z| \tag{5.7}$$

$$\approx (800 \times 10^{-3}) \times \sqrt{(50 \times 10^{-3})^2 + (628.3 \times 10^{-3})^2} \tag{5.8}$$

$$\approx 504\ mV \tag{5.9}$$

The simulation results highlight that during a transient there will be a spike in the filter output voltage. During the spike, the AC model of load current applies, and the steady-state model does not apply. This is the effect of a load transient on the filter output voltage.

## 5.5 Conclusion

Analysis of the simulation results, of a steady-state load, validated the steady-state load current model derived in Chapter 3. The use of the filter to determine average switch-node voltage when the load is DC was also validated.

Analysis of the simulation results of the low-frequency AC load validated the AC model derived in Chapter 3. It was shown that the DC component of load current could be determined from the filter output voltage and the steady-state load current model.

Analysis of the simulation results of a high-frequency load showed that the AC model has a frequency limitation and does not apply when the bandwidth of the controller is exceeded. This was deduced in Chapter 3 and validated in the simulation. It was also shown that for high-frequency load currents the DC component of load current could be determined from the filter output voltage and the steady-state load current model.

The transient load that was simulated showed that during the transients, the filter output voltage exhibits a voltage spike. This is due to the transient response of the inductor current obeying the AC load current model of the buck converter at the transients.

In the next chapter, an experimental validation of the current estimation technique is performed. The low-pass filter is connected to a practical buck converter circuit and experiments are performed to test the accuracy of the current estimation technique using the average current estimation model and the switch-node voltage filter.

# 6 EXPERIMENTAL VALIDATION OF THE CURRENT ESTIMATION TECHNIQUE

## 6.1 Introduction

In the previous chapter, a simulation verification of the steady-state and AC load current models is shown. The simulation verification includes validating the use of the low-pass filter to average the switch-node voltage and apply the steady-state model to estimate average load current. The simulation also revealed non-ideal effects in the filter output voltage during a transient.

This chapter shows the experimental validation of the steady-state model. This validation is the first phase of the physical circuit measurements performed in this research work. The target test device used in this chapter is a buck converter from a *Power Supply Module* that requires a load to be connected to it. This allows for flexibility with regards to the choice of load that is connected. Hence, the load current is known in order to validate the current estimation technique.

The experimental set-up is explained which describes the device under test and includes photographs of the device as well as the low-pass filter module. The circuit diagram of the experimental set-up is shown. Two experiments are conducted on the test device. First, for constant resistive loads i.e. steady-state loads, the current estimation technique is characterised and validated. Thereafter, for a switching load, the current estimation technique is applied using characterisation results from the preceding steady-state experiments. The experimental procedure is explained for each experiment and the results are presented, analysed and discussed.

## 6.2 Experimental Setup and Initialisation

A description of the target test device is presented below. Next, the low-pass filter module (based on the design in Chapter 4) that requires connection to the switch-

node of the test device is presented. Thereafter a modification of the buck converter DCR that was necessary is explained. Lastly, a circuit diagram of the complete experimental setup is shown.

### 6.2.1 Device Under Test

The target test device for this chapter is a synchronous buck converter in a power supply module developed by *Analog Devices.* The details of the power supply module are given in Appendix A. The synchronous buck from the module is a 600 *kHz* 6~14 *V* input 3.3 *V* 2 *A* buck converter. The circuit diagram that is extracted from the schematics of the power supply module appears in Figure 6.1. An input voltage of 9 *V* was selected. The *ADP1872* [49] is a synchronous buck controller IC that controls the switching MOSFETS *M1* and *M2.* The switching MOSFETS are enclosed within an IC and are not accessible. The output filter of the buck is indicated by *L1* and $C_{out.}$ The voltage divider at the output node provides the feedback signal to the *ADP1872.* A labelled photograph of the test device from the power module is given in Figure 6.2.

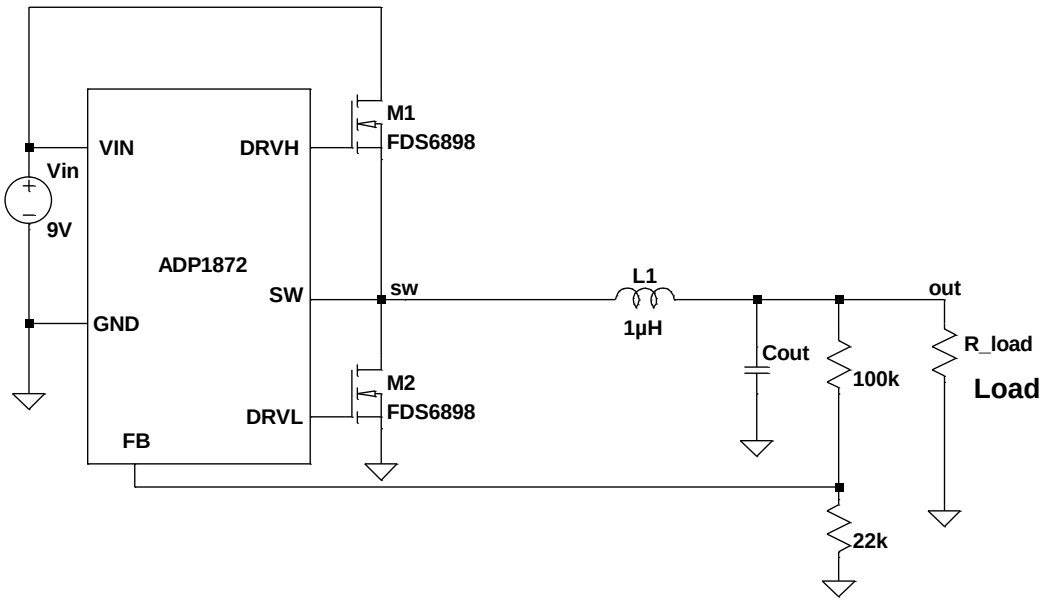



**Figure 6.1: Circuit diagram of the synchronous buck converter test device**

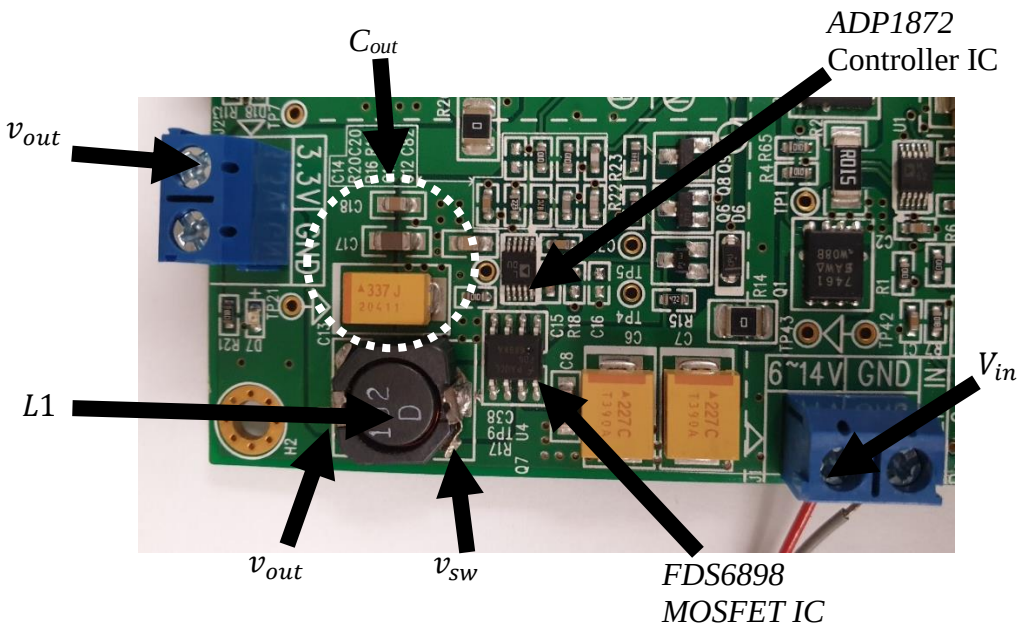



**Figure 6.2: Labeled photograph of the synchronous buck converter test device from the power supply module**

### 6.2.2 Low-Pass Filter Module

Recall that the model is dependent on the average switch-node voltage and a low-pass filter is required to be connected at the switch-node to obtain its average voltage. The circuit diagram of the fourth order low-pass filter circuit using the *LTC1563* filter IC is shown in Figure 6.3. (The design and testing of the circuit appears in Chapter 4.) In Figure 6.3, all resistor tolerances are 1 %. A voltage divider is included at the input of the filter. This is because the voltage rail requirements of the filter are +/-5 *V* and the input voltage of the test device, described above, is greater than 5 *V*. Hence, the upper limit of the switch-node voltage will exceed the rail voltage and a voltage divider is necessary. A photograph of the low-pass filter module including the voltage divider is shown in Figure 6.4.

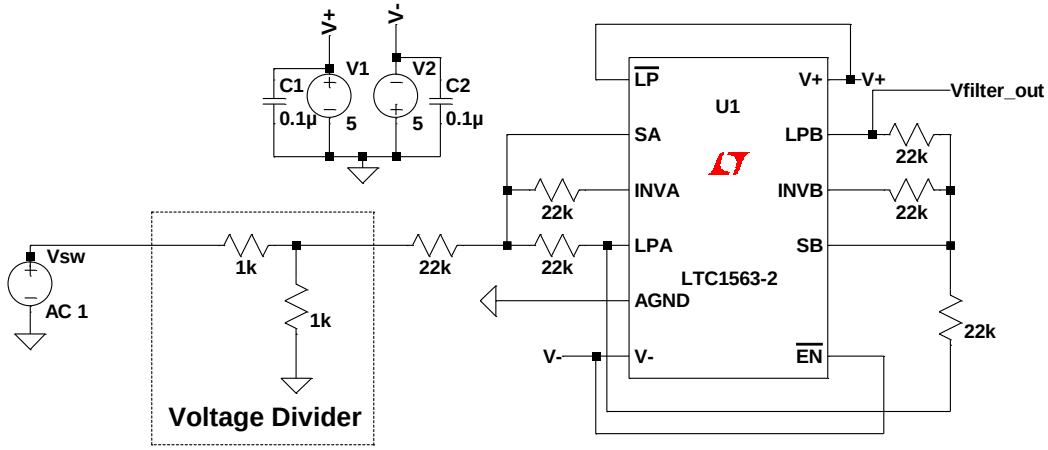



**Figure 6.3: Circuit diagram of the low-pass filter module that requires the switch-node voltage of the test device as the input**

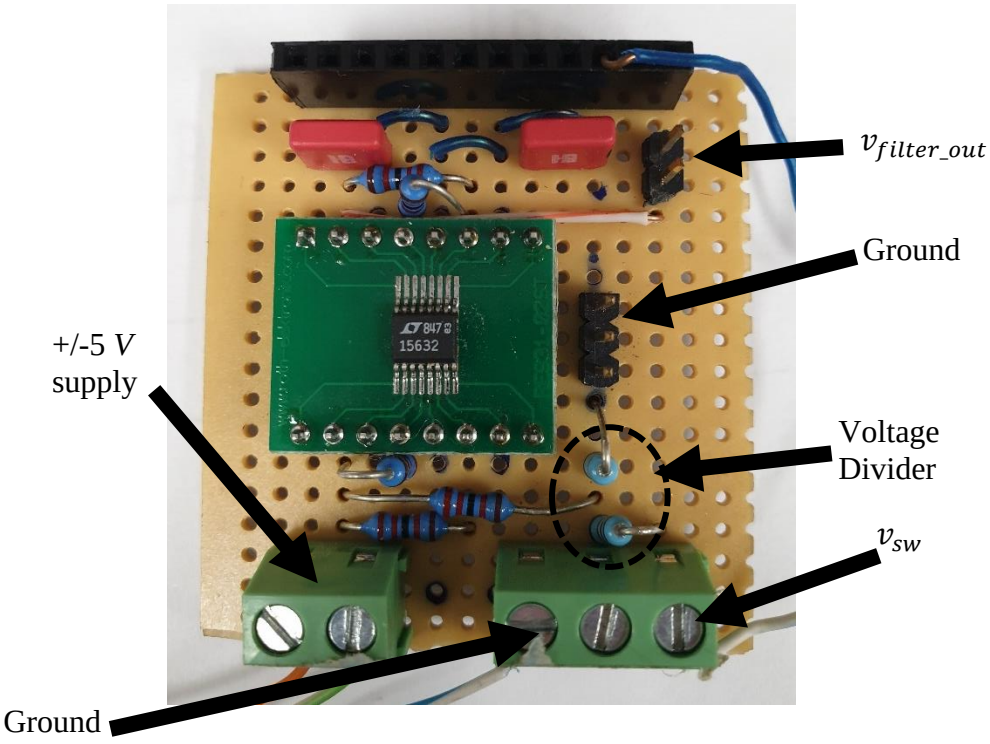



**Figure 6.4: Photograph of the low-pass filter module to be connected at the switch-node of the test device**

### 6.2.3 DCR Measurement and Adjustment

A characterisation of inductor *L1* from the test device in Figure 6.1 with respect to temperature was performed in Section A.3 in Appendix A. The DCR at ambient temperature was approximately 4 $m\Omega$. Whilst this measurement implies minimal conduction losses and is favourable for efficiency, it is too small to detect a significant change in current from the steady-state model.

For example, to detect a 100 *mA* change in current, a 0.4 *mV* voltage difference needs to be measurable across the inductor. This implies that a precision of 0.1 *mV* is required from the measuring instruments. This precision may be obtainable with the DMM [47] (0.1 *mV* precision with 5 *V* range) but the last digit does not always give a reliable measurement. The resolution of the oscilloscope [46] that was available to the author depends on the *V/div* that is displayed but typically a difference of less than a *mV* is challenging to detect on an oscilloscope. Hence, the decision to adjust the effective DCR of the inductor was made. A precision multimeter was made available at a later stage in this work after the following adjustment was made.

To reduce the required precision, a 40 $m\Omega$ surface mount resistor was soldered in series with the inductor increasing the effective DCR. This means, to detect 100 *mA* of current, the voltage difference must be 4.4 *mV*. This was a more achievable measurement. This is an invasive intervention that was necessary for testing of the non-invasive current measurement technique, given the available instruments. It introduces a limitation to the technique based on the value of DCR and the required precision of the measuring instruments. However, the next stage of testing, shown in the next chapter, takes place on the *Cubieboard2* which is a real-life application. The DCR adjustment was not needed for those experiments. The adjustment in this case was purely for experimental validation of the technique.

The inclusion of the series resistor reduces the heating effect (discussed in Chapter 3) due to a surface mount resistor having a lower thermal resistance than the DCR

of the inductor. This is due to the inductor winding being contained in in a closed casing and preventing heat dissipation in the environment. Including a surface mount resistor as part of the overall DCR reduces the overall thermal resistance and minimises the effect of increased temperature on DCR for this experimental case.

The combined DCR was measured using a precision multimeter [50] across the inductor and series resistor whilst the circuit was unenergised. It was measured at **48.1 $m\Omega$.**

### 6.2.4 Test Circuit Diagram

The circuit diagram of the complete setup is shown in Figure 6.5 (on the next page). The switch-node of the synchronous buck converter test device is connected to the filter module. The filter module includes the voltage divider. The series resistor described in the above section is depicted by $R_{series}$. The load is depicted by a single resistor $R_{Load.}$

The experiment is divided into two sections based on the two types of loads that were connected at the output of the synchronous buck in Figure 6.5. First, constant resistors (rated 10 $W$) were connected at the output to allow a steady-state load current to flow. Second, a switching load was connected at the output to represent microprocessor load conditions. The experimental procedure, results and analysis for each of these load conditions is given below.

## 6.3 Steady-State Loads Experiment

The experimental procedure followed for the steady-state load conditions, the results and an analysis of the results appears below.

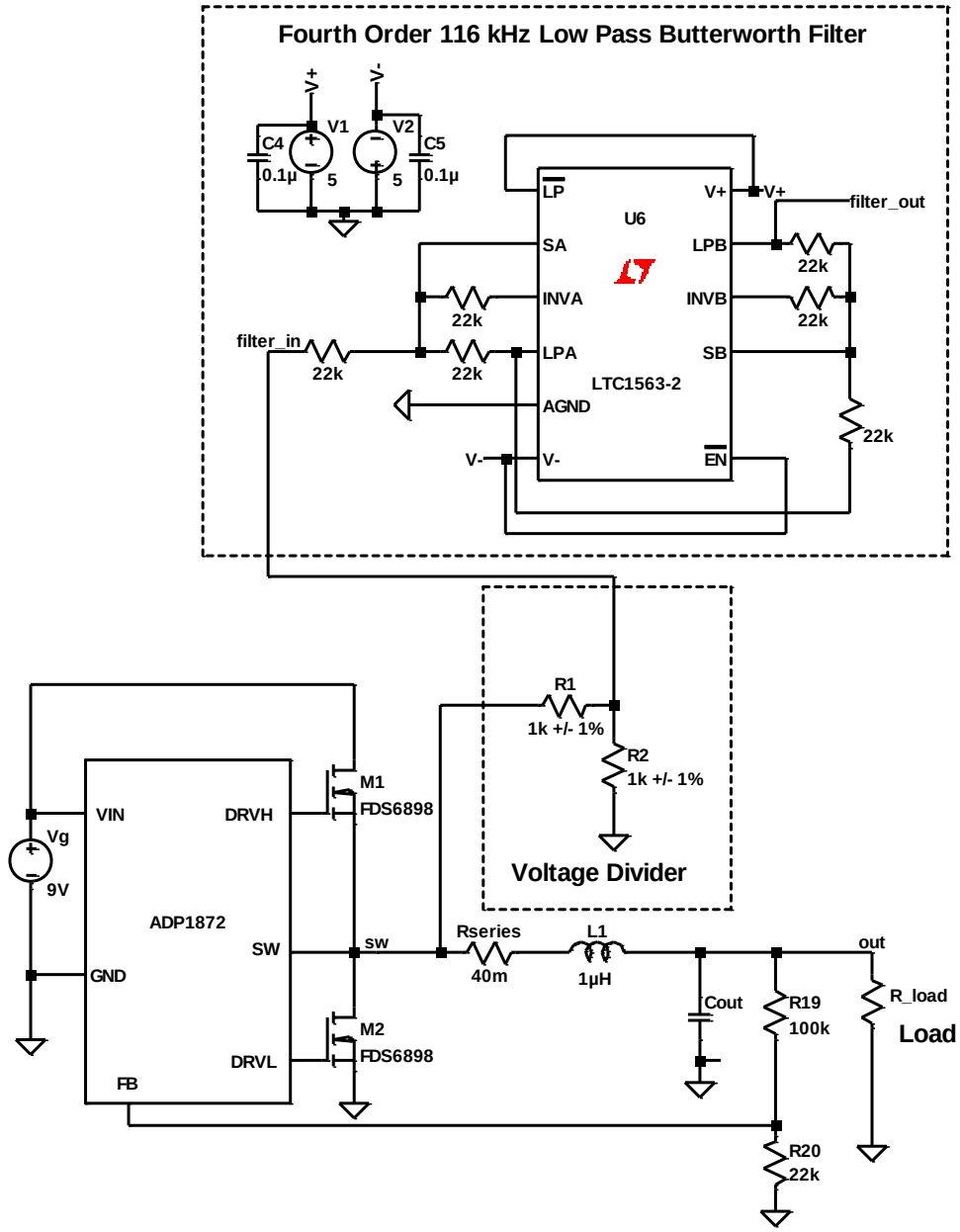



**Figure 6.5: Circuit diagram of the complete experimental setup**

### 6.3.1 Experimental Procedure

The experimental procedure is as follows:

1. First, select 6 load resistors $R_{load_1}$ to $R_{load_6}$, to allow the steady-state load current, $I_{out_1}$ to $I_{out_6}$, to vary from approximately 500 *mA* to 1.5 *mA* i.e.

$R_{load_{1-6}} = \frac{V_{out}}{I_{out_{1-6}}}$ where $V_{out}$ is the output voltage of the buck converter. The rated current of the converter is 2 $A$, thus this current range is within current limits. Connect each load at the output separately. The load resistor will naturally heat up due to power dissipated in the resistor. Allow the circuit to operate for a fixed period of time, hence allowing the resistor to heat up. Measure the output voltage $V_{out}$ then remove the resistor, measure it's resistance $R_{load}$ and calculate the actual load current $I_{out} = \frac{V_{out}}{R_{load}}$.

2. Next, reconnect each load and wait for a fixed period of time. Measure the DC component of the voltages at the following nodes marked (a) to (d) in Figure 6.6 (on the next page):
    a. The switch-node i.e. $V_{sw}$. This is the DC input to the voltage divider.
    b. The filter input voltage node i.e. $V_{filter\_in}$. This is the output of the voltage divider.
    c. The filter output voltage node i.e. $V_{filter\_out}$.
    d. The output voltage node i.e. $V_{out}$.

3. From the measurements in Step 2(a) and (b) of $V_{sw}$ and $V_{filter\_in}$, characterise the voltage divider ratio and offset voltage (the evident offset voltage will be explained in the next subsection).

4. From the measurements in Step 2(b) and (c), of $V_{filter\_in}$ and $V_{filter\_out}$, characterise the DC gain of the filter and the and the filter's output DC offset voltage.

5. For each load current, use the characterisation results from Step 3 and Step 4 to determine the estimated DC component of the switch-node voltage $V_{sw\_estimated}$ from the DC component of the filter output voltage $V_{filter\_out}$ as illustrated in Figure 6.7 (on the next page).

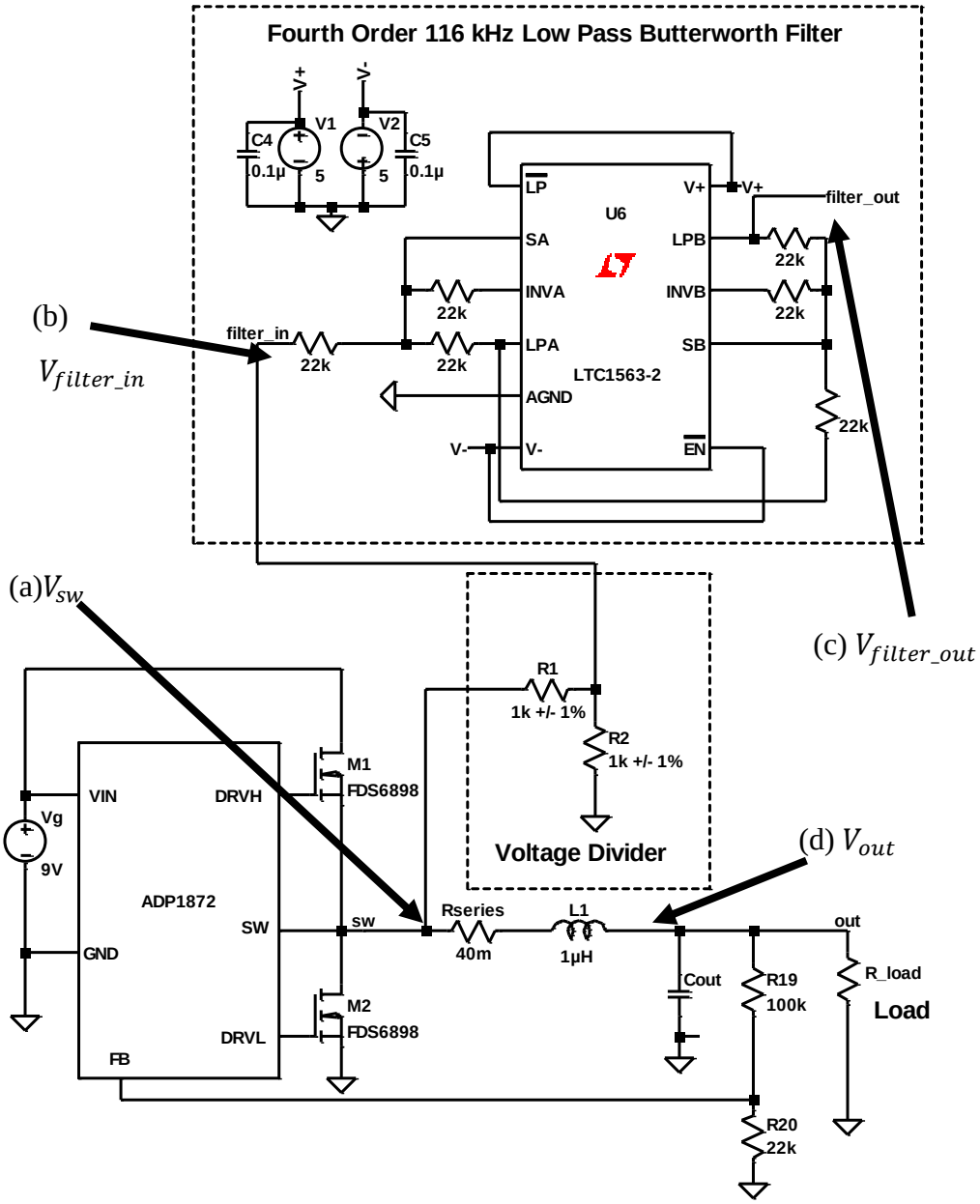



**Figure 6.6: Circuit showing nodes (a) to (d) where measurements must be taken**

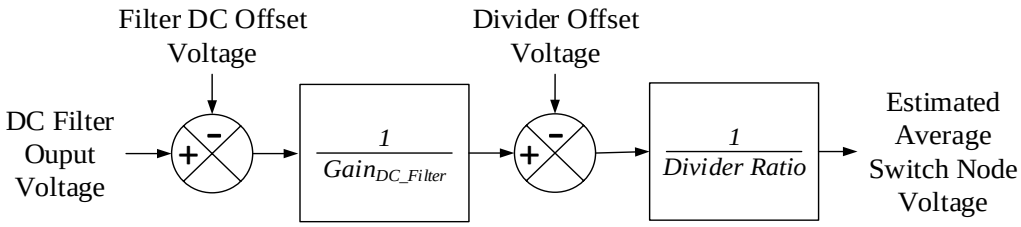



**Figure 6.7: Estimating the switch-node voltage from the characterisation results of the voltage divider and the filter**

6. For each load, use the estimated DC component of the switch-node voltage $V_{sw\_estimated}$ from the previous step, the measured output voltage from Step 2(d) $V_{out}$ and the DCR measurement from the initialisation process and substitute into the steady-state current model in Figure 6.8.

7. Determine the accuracy of the current estimation technique.

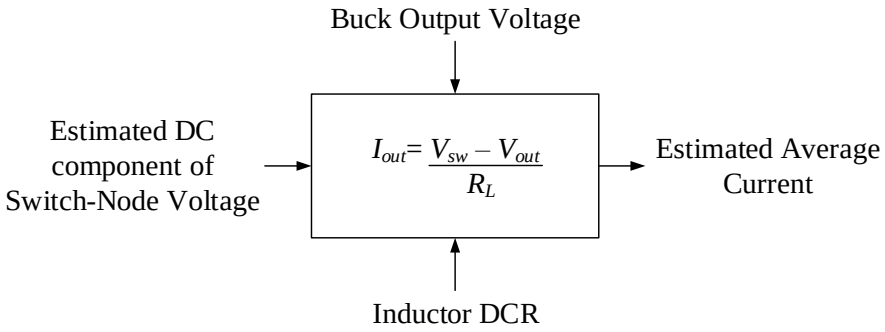



**Figure 6.8: Estimating the average current for each load using the steady-state load current model**

### 6.3.2 Experimental Results and Analysis

***Actual Load Current Calculations***

To calculate the actual current for each load, a precision, 8.5 digit resolution multimeter was used [50] to measure the voltage and resistance of each load.. This allowed for a high resolution of measurements and accurate calculation of the actual load current. The results are given in Table 6.1, on the next page.

***Measured Voltages vs. Load Current***

The voltages measured at the nodes (a) to (d) from Figure 6.6 in the previous subsection (Section 6.3.1, Step 2) were measured with a DMM with a resolution of 0.1 *mV* [47]. The switch-node voltage and the filter input voltage were non-DC

voltages. The DMM on DC Mode performs internal averaging to determine the DC component of these non-DC voltages [47]. The results of the voltages measured are shown in Figure 6.9. As expected, for increasing load currents, the increased duty cycle causes an increase in the DC component of the switch-node voltage (Step 6 in Section 3.3.1). Hence, there is an increase in the filter input and output. The DC component of the output voltage is approximately constant for all load currents, as expected.

**Table 6.1: Actual load current calculation results**

| **Load Number** | **1** | **2** | **3** | **4** | **5** | **6** |
|---|---|---|---|---|---|---|
| $V_{out}$ **measured (V)** | 3.3130 | 3.3108 | 3.3122 | 3.3107 | 3.3100 | 3.3098 |
| $R_{Load}$ **measured (Ω)** | 6.7810 | 5.0242 | 3.3370 | 3.0695 | 2.5850 | 2.2650 |
| $I_{out}$ **calculated (A)** | **0.489** | **0.659** | **0.993** | **1.079** | **1.282** | **1.461** |

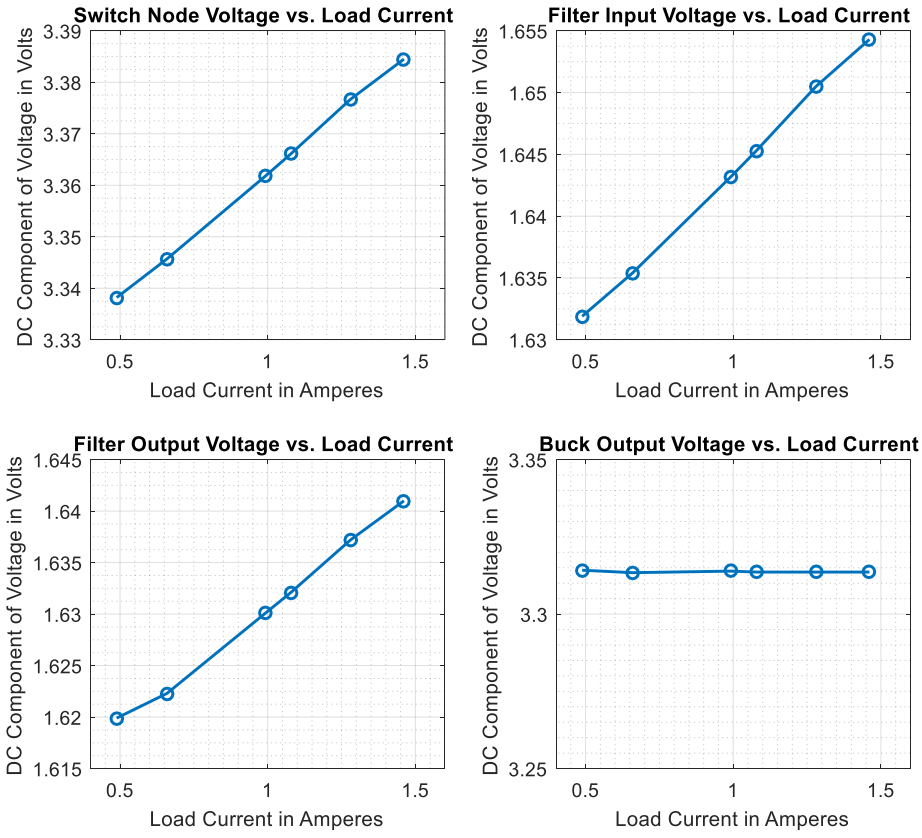



**Figure 6.9: DC component of voltages measured vs. load current**

***Characterisation of Voltage Divider***

The switch-node and filter input voltages from Figure 6.9 represent the input and output of the voltage divider respectively as shown in Figure 6.10. These voltages were used to calculate the voltage divider ratio by being plotted as *voltage divider output vs. voltage divider input*. Using the *polyfit* command in *MATLAB* a linear approximation of the data was obtained and plotted. The *polyfit* command returns the coefficients for a polynomial of specified degree given a data set. Since for a linear approximation, the degree is 1, the coefficients returned are the gradient and intercept of the linear approximation. A plot of the measured data points and the linear approximation appears in Figure 6.11. It is analysed below.

From Figure 6.11, the measured values and linear approximation are approximately equal as is expected with a voltage divider. The voltage divider ratio is given by the gradient of the linear approximation. However, what is unexpected is that a voltage divider would have an offset voltage. In this case, due to the voltage divider connected at the input of the filter, due to input bias current flow, there is a voltage across the voltage divider resistor $R_{div2}$ when the input is zero. These values for voltage divider ratio and offset were stored in the *MATLAB* program and are indicated on Figure 6.11. The precision of this data will be maintained in *MATLAB* to minimise error in the final estimated current result. This is discussed in more detail in Section 6.5.

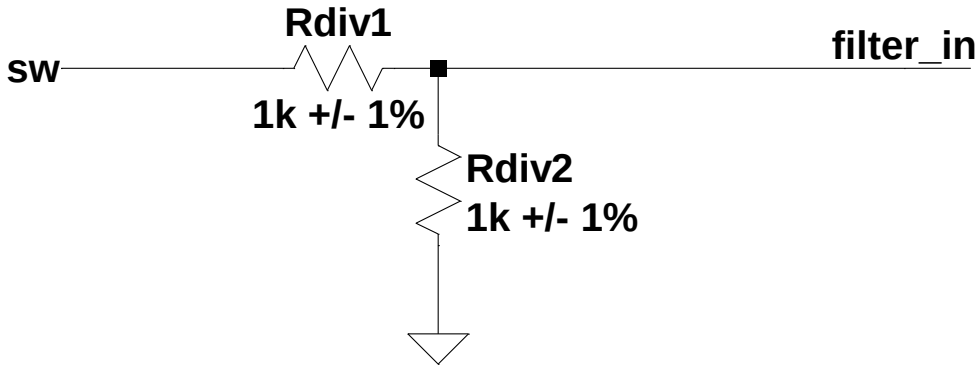



**Figure 6.10: Voltage divider at filter input**

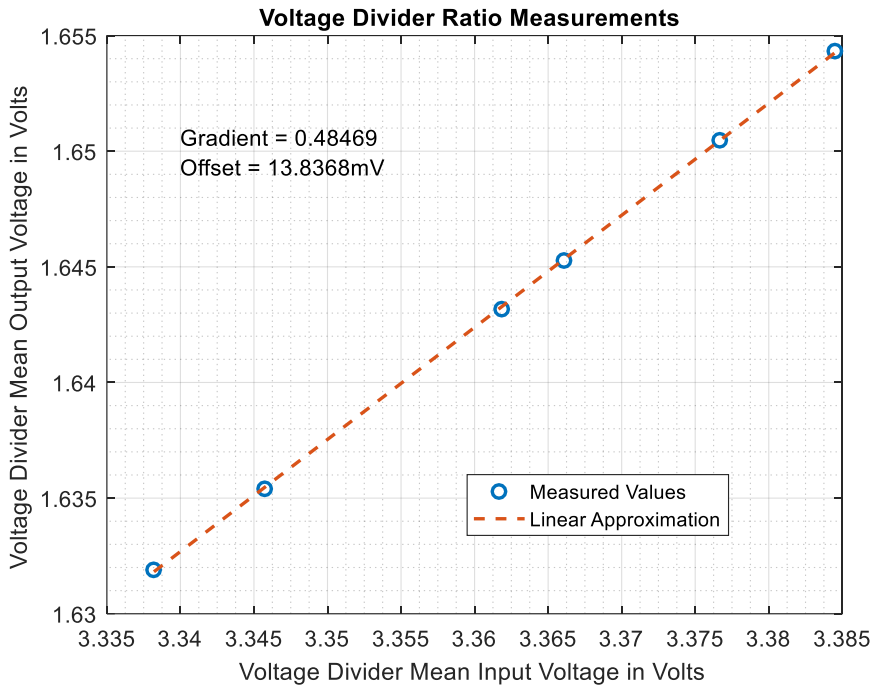



**Figure 6.11: Voltage divider characterisation data and linear approximation**

### *Characterisation of Filter DC Gain and Offset*

Similar to the voltage divider, the DC gain and DC output offset voltage were determined by plotting the DC component of the filter output vs. the DC component of the filter input. The DC gain is given by the gradient and the DC offset is given by the offset of the linear approximation of the results plotted in Figure 6.12, on the next page. These values for DC gain and DC offset of the filter were stored in the *MATLAB* program. The precision of this data will be maintained in *MATLAB* to minimise error in the final estimated current result. This is discussed in more detail in Section 6.5.

### *Application of the Current Estimation Technique*

The voltages measured at nodes (c) to (d) from Figure 6.6 i.e. the filter output voltage and the buck converter output voltage were applied to the current estimation technique. The DC component of the switch-node voltage was estimated using the

process in in Figure 6.13. This was then used in the model shown in Figure 6.14. This was achieved in *MATLAB*. Recall that the DCR was initialised as 48.1 $m\Omega$.

Figure 6.13. and Figure 6.14 represent the block diagram for the current estimation technique. It should be noted that in steady-state, the filter is not technically required to estimate the current because the DC component of the switch-node can be directly measured with a DMM and the value can be applied to the model. However, the characterisation of the technique based on the steady-state measurements allow for the filter to be used to estimate the average of a dynamic load current as it is switched. This is shown in the next experiment.

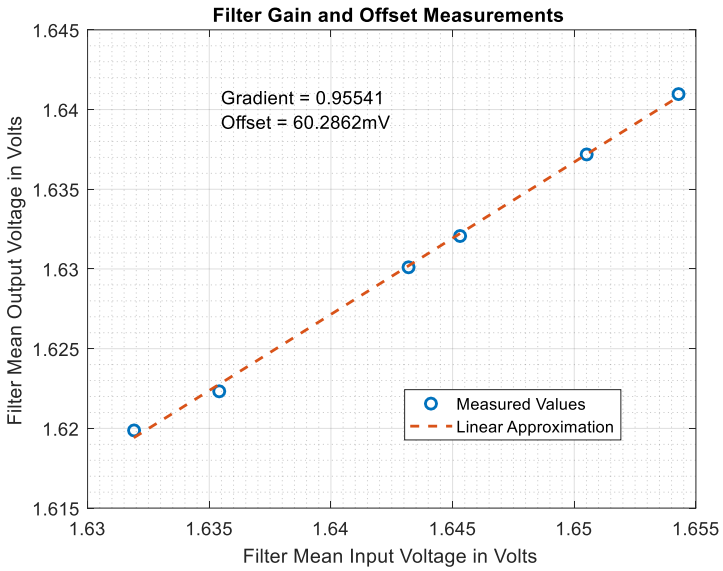



**Figure 6.12: Filter characterisation data and linear approximation**

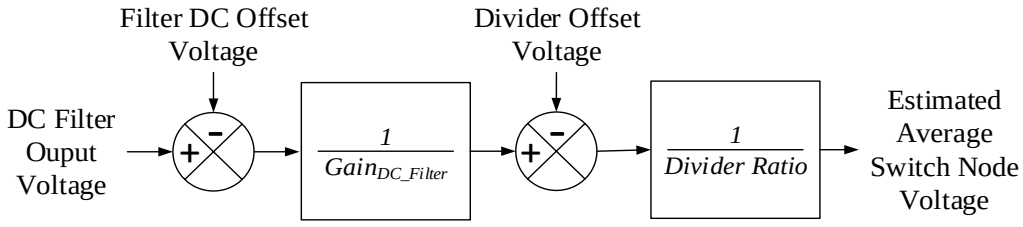



**Figure 6.13: Estimating the average switch-node voltage from the filter output voltage**

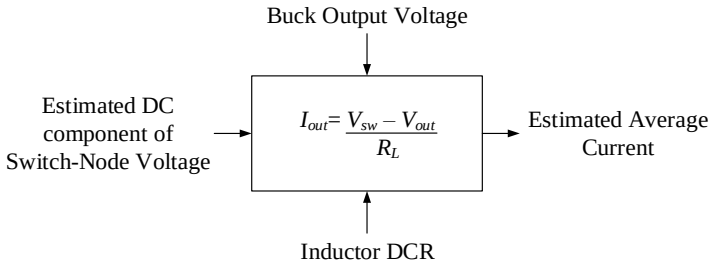



**Figure 6.14: Estimating the average current for each load using the steady-state load current model**

### *Estimated Average Load Current*

The results for the estimated current for each load, computed in *MATLAB* as described above, is shown in Figure 6.15. It is compared with the actual current calculated at the beginning of the experiment. The results show that there is good agreement between the actual and estimated load currents for DC loads. The percentage error of each measurement is shown in Figure 6.16. Most of the percentage errors are low, with a less than 3 % deviation from the actual load current. At the lowest load current, the percentage error is higher. The percentage error, however, is still below 10 % which, in general, is a fair tolerance.

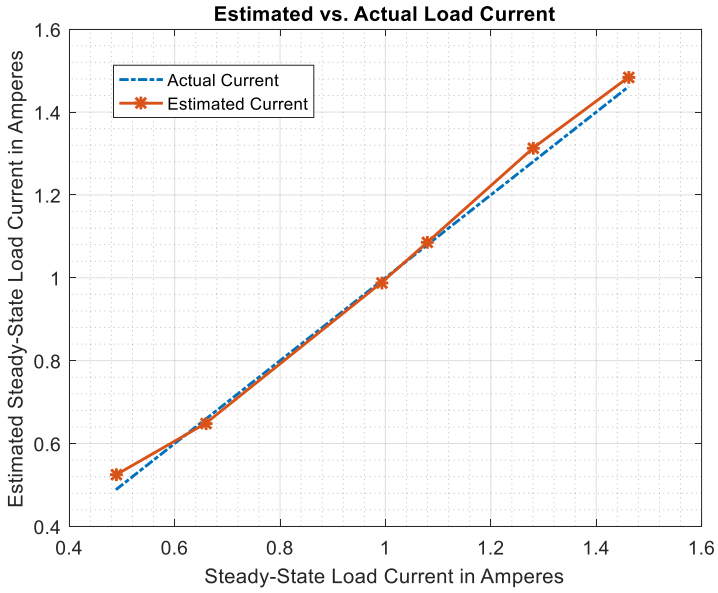



**Figure 6.15: Estimated vs. actual load current using the current estimation technique for DC loads**

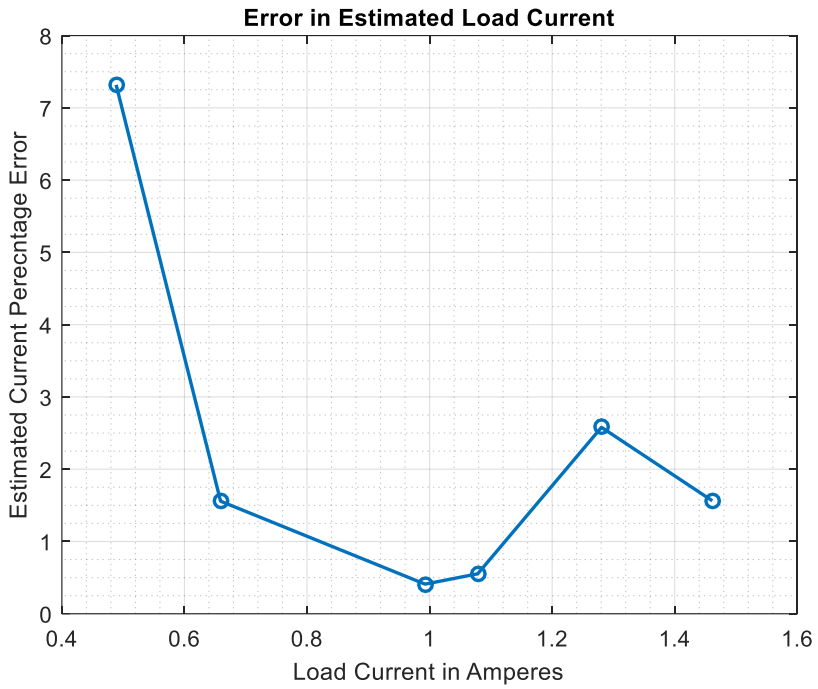



**Figure 6.16: Percentage error of each estimated current value**

## 6.4 Switching Load Experiment

The experimental procedure for a switching load condition, the results and an analysis of the results appears below.

### 6.4.1 Experimental Procedure

1. Connect a switching load at the output. This circuit diagram for the switching load is show in Figure 6.17. It consists of a 555 timer IC in astable operation [51]. The frequency and the on-period of the oscillation is calculated from *RA*, *RB* and *C*. The output of the timer drives the power MOSFET, *M1* to periodically switch on a dynamic resistance *R2* of 2.7 Ω in parallel with a static resistance *R1* of 10 Ω. Based on the values in the

circuit the oscillation frequency is calculated to be approximately 18.2 *Hz* with an on-period of 67% [51].

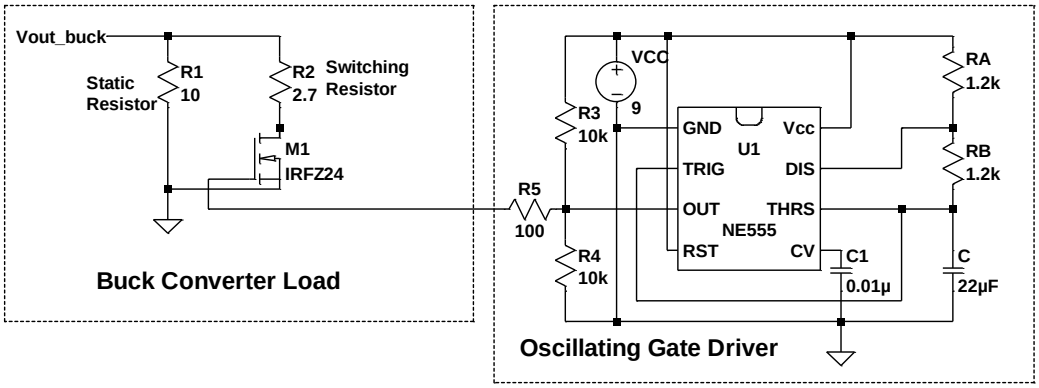



**Figure 6.17: Switching load circuit**

2. Calibrate the oscilloscope [46] voltage probes to ensure an approximately zero reading when the probes are connected together. Connect the oscilloscope voltage probes (Channels 1 and 2) at the switch-node of the test device and the filter output node as shown in Figure 6.18. Connect a current probe (Channel 3) at the load as shown in Figure 6.18.

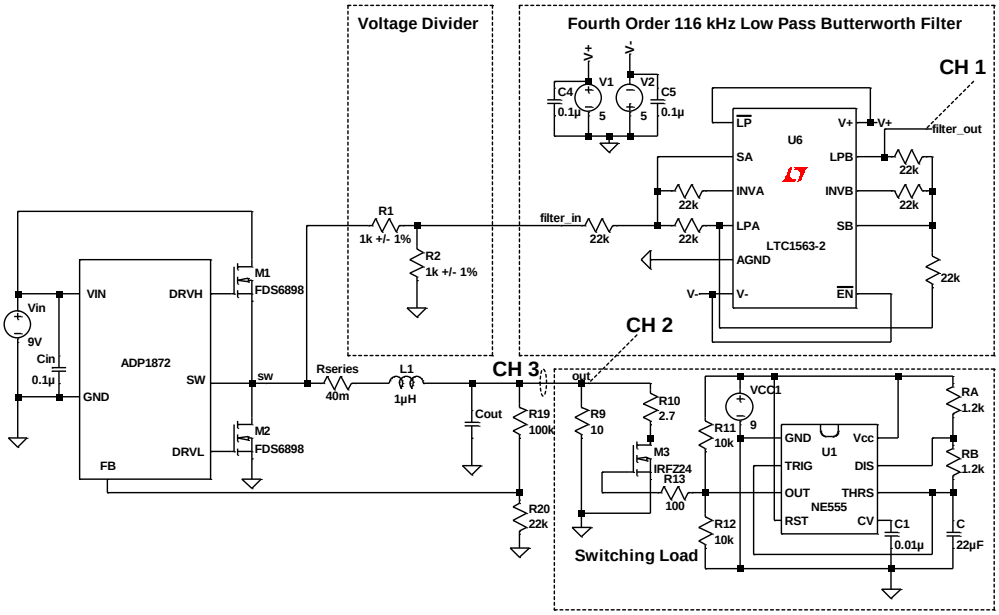



**Figure 6.18: Connection of oscilloscope voltage and current probes to the circuit**

3. Save an image of the oscilloscope waveforms to get visual representation of the load current and the filter and buck output voltages. Save all the data to *.csv* files. The voltage data will be used to estimate the current using the technique. The estimated current will then be compared with the original current waveform data. The following steps explain how this will be done.

4. Apply a moving average filter to the filter output voltage data and the buck output voltage data to eliminate noise as well as the transient effects. The transient effects are is explained in Section 5.3.4 And Section A.2 in Appendix A.

5. Process the filter output voltage data using Figure 6.13 from the previous experiment to determine the estimated average of the switch-node voltage. (This average will switch as the current switches.)

6. Apply the model in Figure 6.14 from the previous experiment to the complete data set to estimate the average load current. (This average will switch as the current switches.)

7. Determine the accuracy of the current estimation technique by comparing the estimated current with the actual current.

### 6.4.2 Experimental Results and Analysis

***Oscilloscope Waveforms***

The load current, buck converter output voltage and filter output voltage waveforms are shown in Figure 6.19 and labelled as follows:

- Channel 1: Filter output voltage $v_{filter\_out}$
- Channel 2: Buck converter output voltage $v_{out}$
- Channel 3: Load current $i_{out}$

From Figure 6.19 , the measured frequency of the load oscillation is 20 *Hz* instead of the calculated 18.2 *Hz.* This is possibly due to the component tolerances. The transient spikes at the filter output voltage are unclear but more visible in the AC coupled, smaller time-scale waveforms in Figure 6.20 and Figure 6.21 (on the next page and the following page, respectively)

From Figure 6.20 and Figure 6.21, the AC coupled (Channel 1) waveform shows that there is a difference in DC level before and after the transient. As predicted by the simulation (Section 4.3.4) and confirmed by the AC model (Section 2.3.2), the transient current causes a low-frequency spike at the filter output voltage dependent on the impedance of the inductor. This comes through the 116 *kHz* filter. This will be addressed by applying an additional digital low-pass filter to the signal to filter out these transient effects.

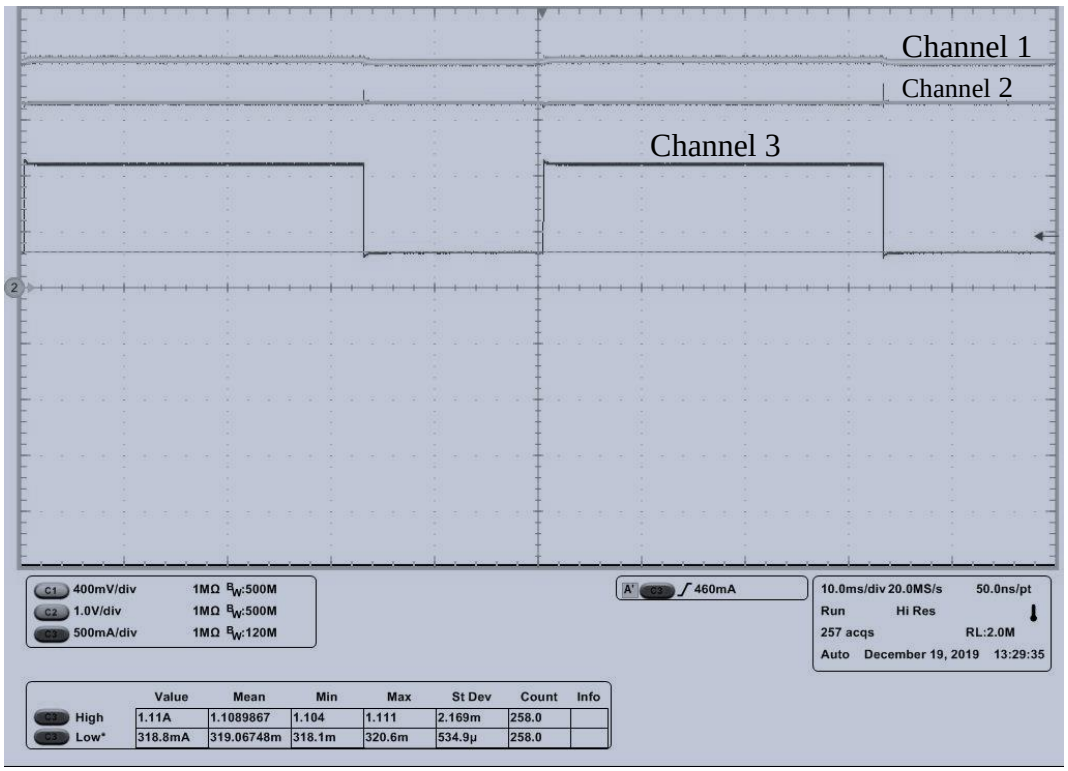



**Figure 6.19: Waveforms for a dynamic (switching) load current**

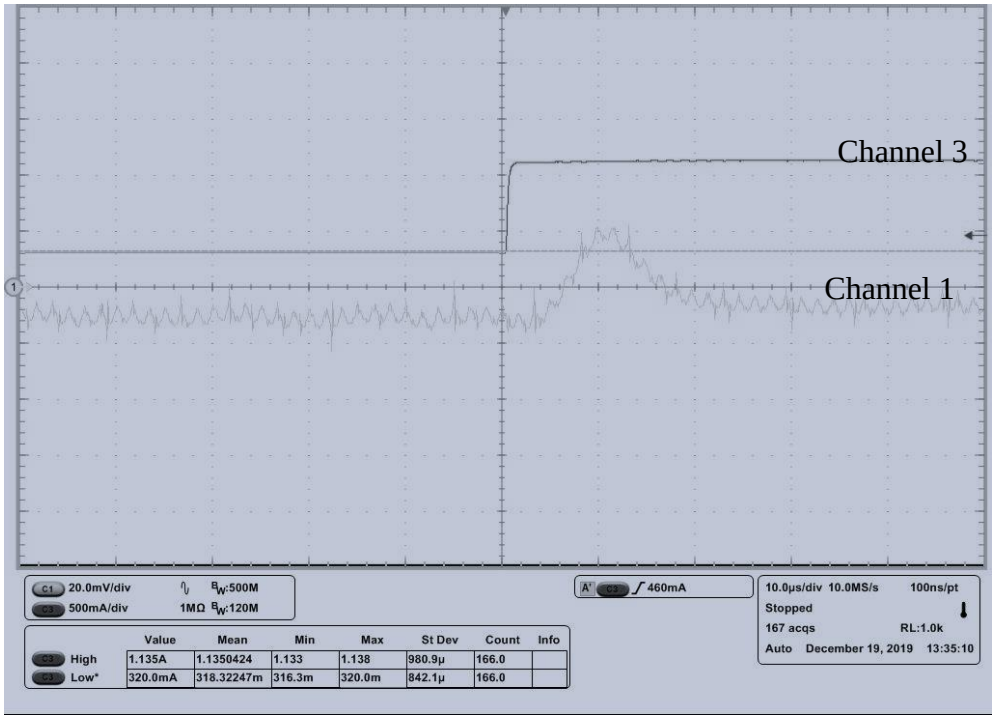



**Figure 6.20: AC coupled filter output voltage waveform at positive current transient**

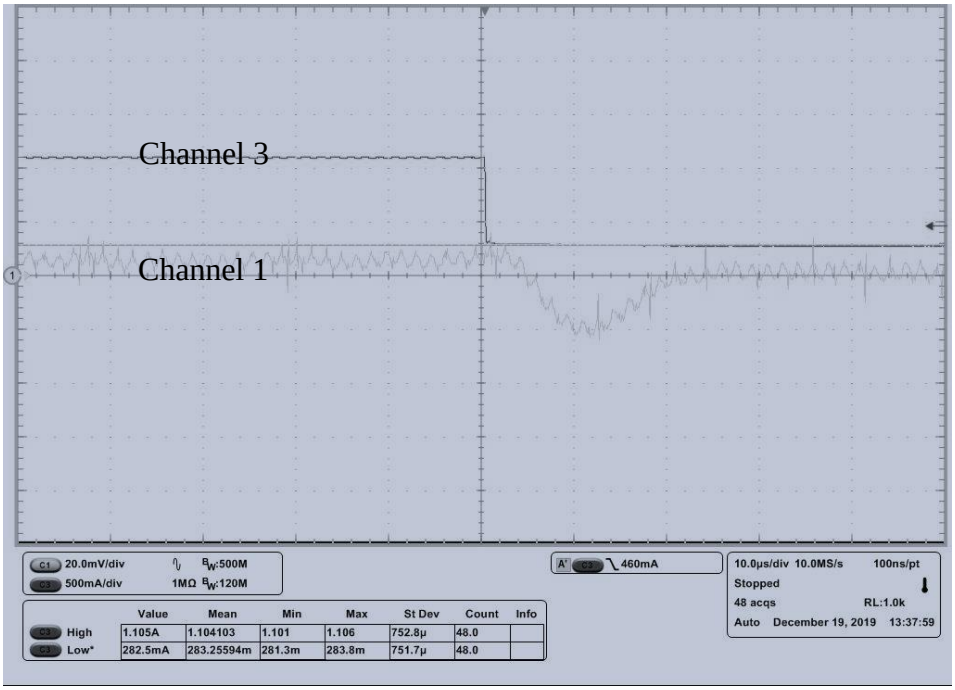



**Figure 6.21: AC coupled filter output voltage waveform at negative current transient**

***Oscilloscope Voltage Data and Processing***

The original filter output voltage $v_{filter\_out}$ and the buck converter output voltage $v_{out}$ that is plotted using *MATLAB* from the data saved in the *.csv* files is shown in Figure 6.22. The data was sampled at 20 *MS/s* and contains high frequency noise. To eliminate the noise the data will be put through a low-pass moving-average 1D digital filter [52]. A low-pass moving-average filter slides a window of length window size along the data, computing averages of the data contained in each window. The expression in (6.1) defines a moving-average filter of vector *x* resulting in filter output *y* where *n* is the data point number. The application of this filter to the data will be discussed below.

$$y(n) = \frac{1}{windowSize}\Big(x(n) + x(n-1) + \cdots + x\big(n-(windowSize-1)\big)\Big) \quad (6.1)$$

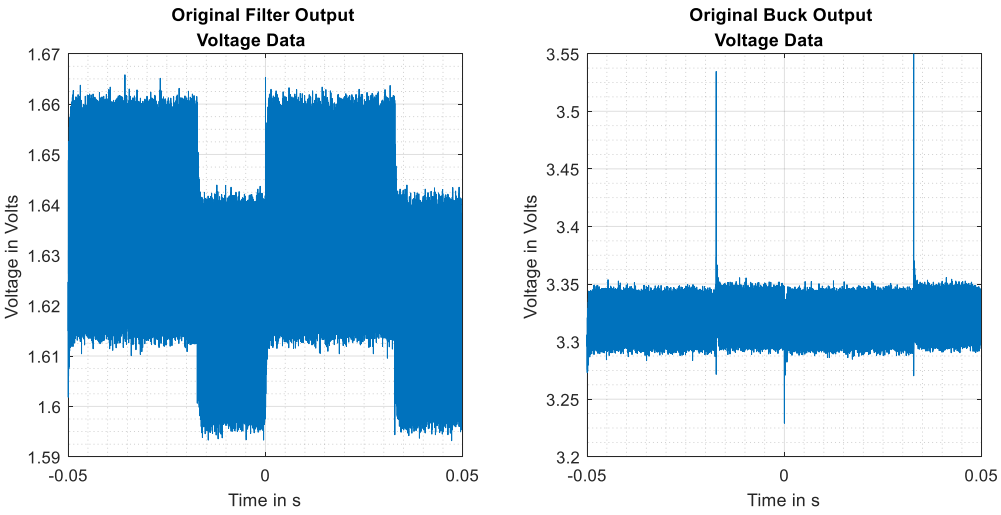



**Figure 6.22: Plots of original noisy voltage data saved**

The moving average filter is explained in detail in [53]. It is essentially a smoothing filter in the time domain and is the optimum choice for eliminating random noise from time domain signals, whilst retaining a sharp step response [53]. However, in the frequency domain, the stop-band attenuation oscillates. The transfer function in the frequency domain is given in (6.2) where $M$ denotes the window size.

$$H(f) = \frac{\sin(\pi M f)}{M \sin(\pi f)} \tag{6.2}$$

Selection of the window size $M$ affects the frequency response of the digital low-pass filter. The *spectral zero frequency* $f_s$ of the moving-average filter is given by (6.3) [54]. This frequency is defined as the frequency, after which, the attenuation oscillates rather than goes to zero. An example is given below.

$$f_s = \frac{Sampling\ Rate}{windowSize} \tag{6.3}$$

As an example, consider the cut-off frequency of the of the analogue filter employed in the test-setup circuit i.e. 116 *kHz* (designed in Chapter 3). Say that the spectral zero frequency is also chosen as 116 *kHz*. Given the 20 *MS/s* sampling rate. This corresponds to a window size of 172. The *spectral zero frequency* $f_s$ is shown in the normalised frequency response in Figure 6.23. The Bode plot of the frequency response is shown in Figure 6.24 where $f_s = 116\ kHz$ .

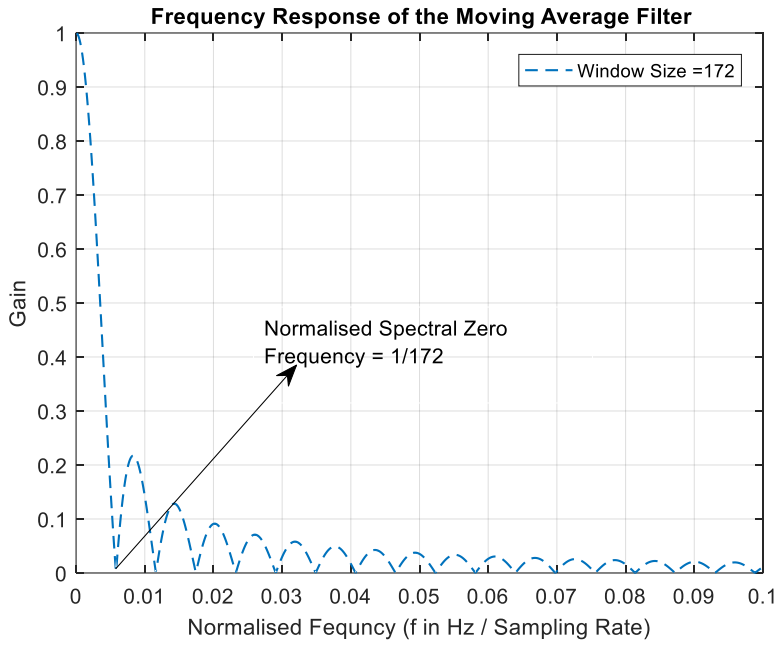



**Figure 6.23: Normalised frequency response of the moving average filter with window size of 172**

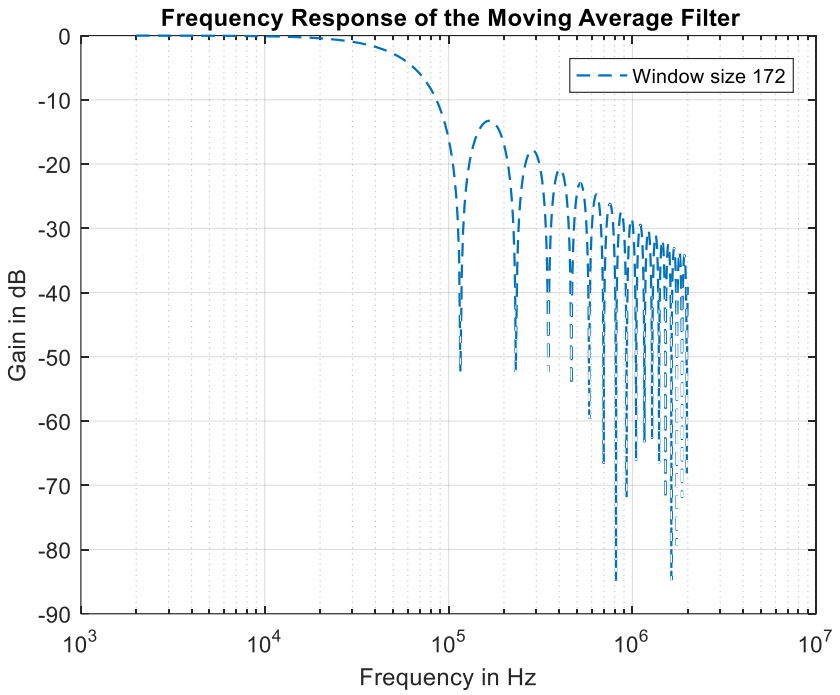



**Figure 6.24: Frequency response bode plot of the moving average filter with window size of 172**

Despite the visible "loops" in the attenuation in the frequency response in Figure 6.23 and Figure 6.24, there is a roll off evident that preserves the DC component of the signal and the low-frequency 18.2 *Hz* switching current. Applying the above moving-average filter to the data will attenuate unwanted high frequency noise that has been saved. The results of this filtered data is shown in Figure 6.25. It can be seen from the figure that the high frequency noise is eliminated and there is a better representation of the behaviour of the signal. The transient effects visible in the data will be discussed below.

At the current transients, the filter output voltage as well as the buck converter output voltage contain transient spikes, visible in Figure 6.25. The window size of the low-pass moving-average 1D digital filter can be adjusted to eliminate this effect. From the AC coupled waveforms shown previously in Figure 6.20 and Figure 6.21, the time duration of the filter output voltage spike is 20 $\mu s$. To eliminate this effect, the spectral zero frequency of the moving average filter can be selected at $\frac{1}{20\ \mu s} = 50\ kHz$. For this frequency, a window size of 400 is required

calculated from (6.3) above. A comparison of the normalised frequency response of the moving-average filter with both window sizes (172 and 400) is shown in Figure 6.26. This shows that increasing the window size reduces the spectral zero frequency and results in more "smoothing" in the time domain. Using this new window size of 400 in the digital filter and applying it to the original data yields the filtered data in Figure 6.27, on the next page.

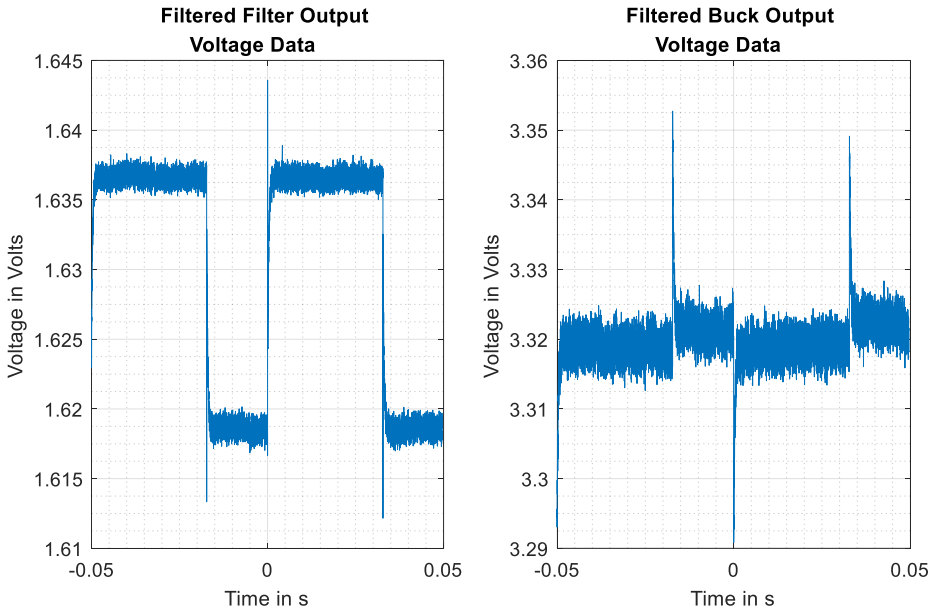



**Figure 6.25: Results of applying a low-pass moving average filter with window size of 172 (116 *kHz cut-off)* to the noisy data**

From Figure 6.27, the transient voltage spike for the filter output voltage is eliminated but the voltage spike at the output voltage is still present. This is due to the unusually slow transient response of the device under test. An analysis of the transient response of this converter appears in Appendix A (Section A.2). The bandwidth was estimated to be approximately 2 *kHz*. The effect of this transient spike will not be removed due to the large window size (10000) required and the latency that it will introduce. It will contribute to the error in the estimation of the current during the transient period.

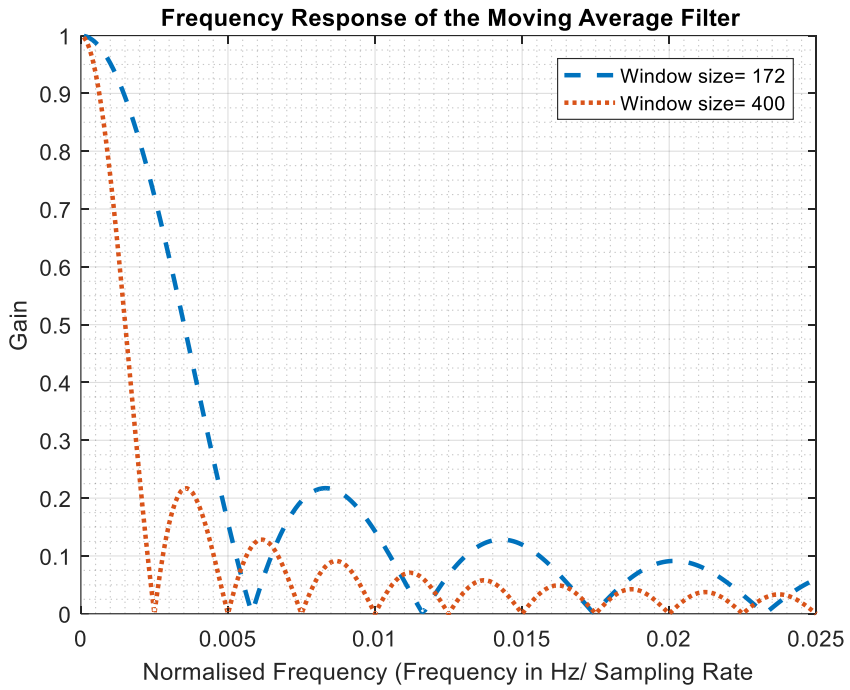



**Figure 6.26: Comparison of two normalised frequency responses of moving-average filter**

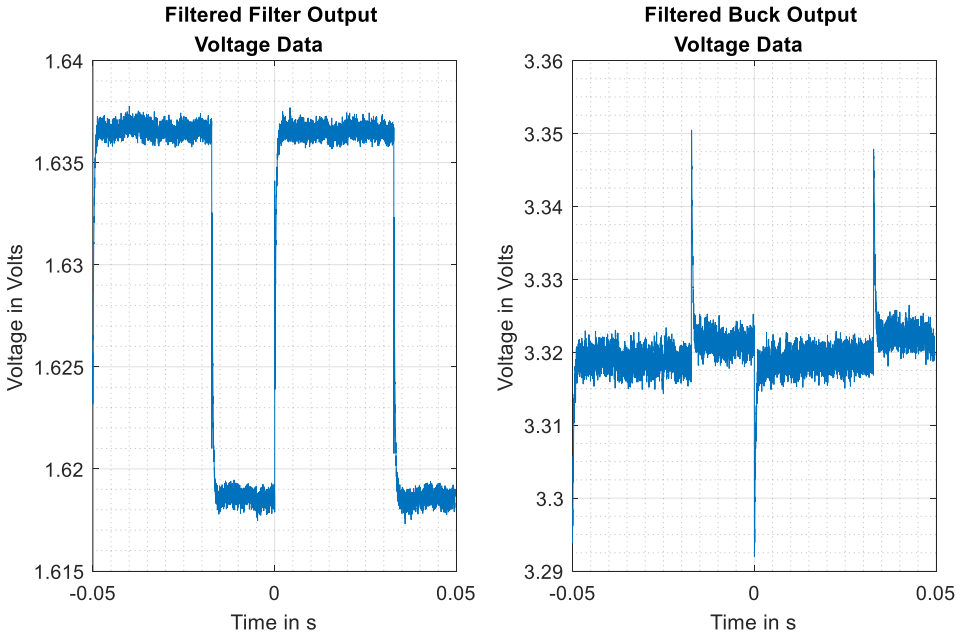



**Figure 6.27: Results of applying a low-pass moving average filter with window size of 400 (50 *kHz cut-off)* to the noisy data**

***Application of Technique***

For the entire data set in Figure 6.27, the estimated dynamic average switch-node voltage was determined from the procedure shown in Figure 6.28, below. The original noisy data was digitally filtered as discussed in the previous subsection. The filter DC offset and gain (determined from the *Characterisation of Filter DC Gain and Offset* in Section 6.3.2 in the previous experiment) were subtracted and factored out of the data, respectively. Thereafter, the voltage divider offset and ratio (determined from the *Characterisation of Voltage Divider* in Section 6.3.2 in the previous experiment) were subtracted and factored out of the data, respectively. This results in an estimate of the dynamic average switch-node voltage.

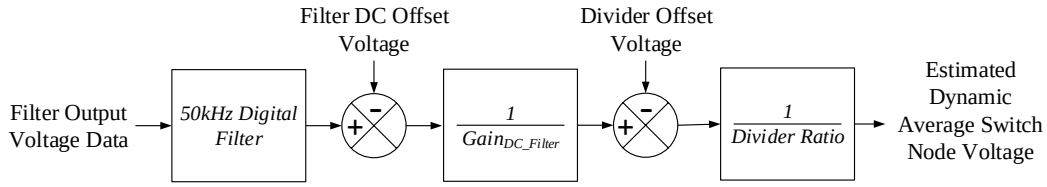



**Figure 6.28: Estimating the average switch-node voltage from the filter output voltage data**

The estimated dynamic average switch-node voltage was then used as an input to the current estimation technique in Figure 6.29. The buck converter output voltage data and DCR were also used as inputs. The buck converter output voltage was digitally filtered as discussed in the previous subsection. The result of the technique in Figure 6.29 was the estimated dynamic average current. The DCR was measured before startup at approximately **48.8 *m*Ω** using a precision 8 1/2 digit multimeter [50]. This value differed from the value measured for the steady-state experiments due to additional solder that was subsequently added to the circuit connection.

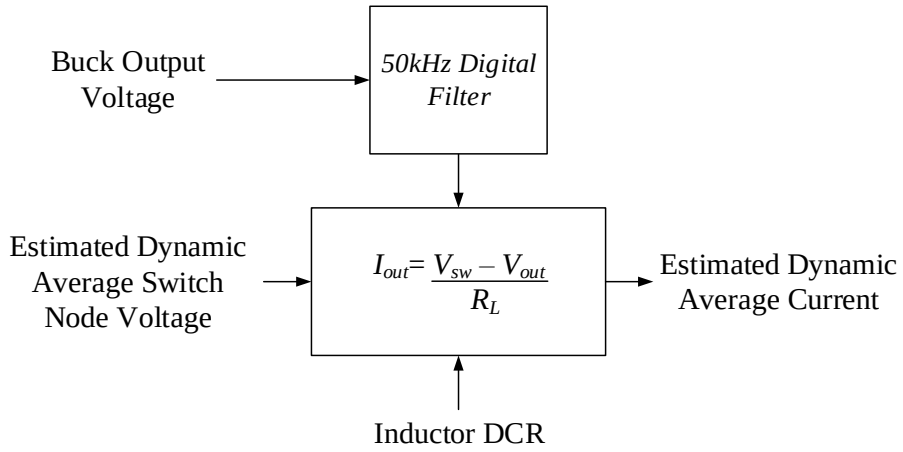



**Figure 6.29: Estimating the average current data from the estimated dynamic average of the switch-node voltage and the buck output data**

***Estimated Current Waveform***

Applying the current estimation technique in the previous step yielded data for the estimated current. The estimated current data can be plotted and compared with the actual current data that was initially saved. This is shown in Figure 6.30. The smooth waveform is the actual current data that was saved in the beginning of the experiment. The non-smooth waveform is the estimated current data. There is good agreement between the two waveforms i.e. the estimated current waveform generally follows the actual current waveform with an exception at the transients. (This is expected due to the output voltage transient spike discussed earlier.) The mean value calculated in *MATLAB* for the actual and estimated current data is shown on Figure 6.30. The error of the estimated mean current is less than 3 % of the actual mean current value.

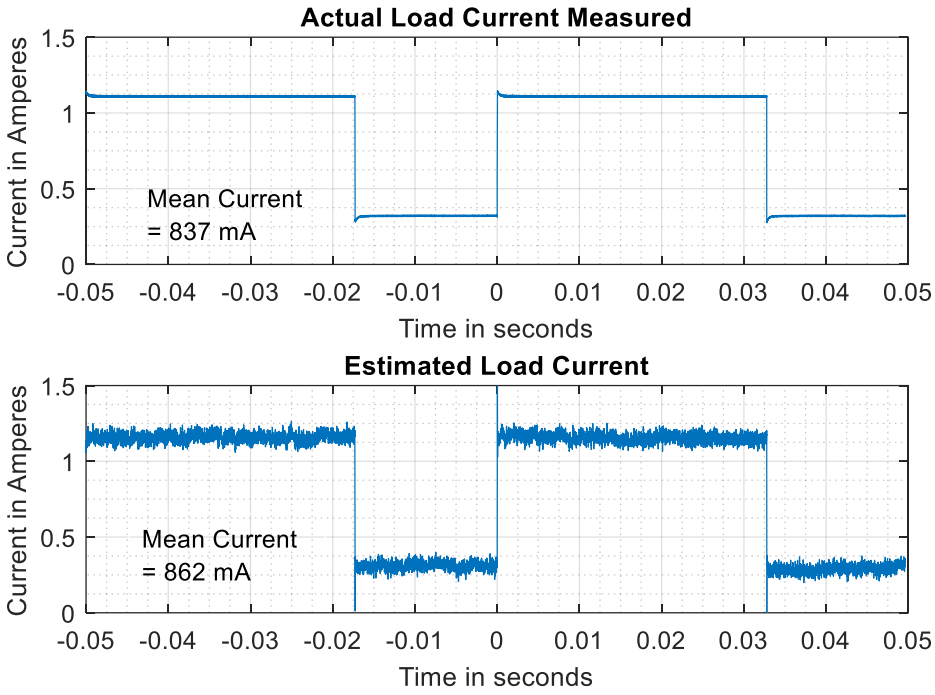



**Figure 6.30: Plot of actual current vs. time (smooth trace) and estimated current vs. time (noisy trace)**

The percentage error of the estimated data vs. time is shown in Figure 6.31 (on the next page). Note that the limit on the y-axis is 100 % despite the error during transients being higher than 100 %. This is due to the high output voltage spike. Since the error at the transients is expected, it is not fully shown in the error plot. This gives a clearer indication of the lower percentage errors.

As in the previous experiment (with steady-state loads), the error is higher at lower currents. Since the deviation from the actual current looks approximately equal for both current levels, at a lower current, this results in a higher percentage error. The overall mean of the error for the continuous signal is approximately 6 %. This is good, despite the transient spike that increases the mean error.

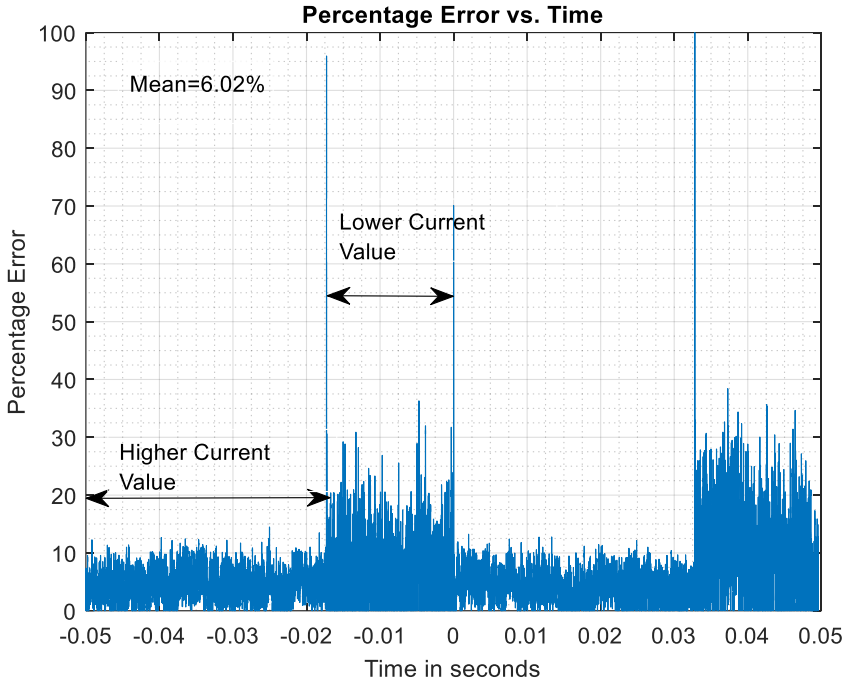



**Figure 6.31: Percentage error of estimated data vs. time**

## 6.5 Discussion

In the steady-state experiments, the filter module was connected to the test device to characterise the parameters that describe the voltage divider and the DC behaviour of the filter. These characterisation parameters (voltage divider and filter offsets and gains) were then incorporated into the current estimation technique that consisted of the steady-state load current model of the buck converter. The technique was then applied to estimate the DC current and compare it to the actual current, thereby validating the technique.

For a switching load, dynamic voltage data from the filter output was stored, and the current estimation technique was applied. The current estimation technique first subtracted and factored out the relevant characterisation parameters (voltage divider and filter offsets and gains) from the previous experiments. This resulted in an estimation of the switch-node voltage data. After applying the steady-state load current model to the data, an estimate of the load current was obtained.

The characterisation parameters are specific to the test device on which they were performed and may vary if the switch-node voltage of a different buck converter is connected to the filter module. However, it can be generalised to be applicable to other buck converters with similar voltage output requirements. The calibration procedure of the filter module with the buck converter integration is thus necessary to accurately determine the voltage divider and filter parameters. An alternate approach to characterise the offset and gain of the voltage divider and filter is to use a function generator as an input rather than the switch-node voltage of the buck converter. However, the author noted that this method does not yield similar characterisation results. The results were approximately equal if a low precision was required. Due to high precision required in this work, the characterisation procedure with the buck converter was necessary to obtain high accuracy characterisation parameters and final estimated current results. The reason for high precision is discussed below.

The measurement precision for these experiments was kept high. The voltage measurements had a resolution of 0.1 *mV*, the load resistance was measured with a resolution of 0.1 Ω, and the linear approximated gain values were saved in *MATLAB* with 5 significant digits of precision. This was necessary to maintain accuracy of the final result. Since the DCR is typically in the *m*Ω range, the difference in average voltage across the inductor is small and can be expected to be in the *mV* range. Furthermore, since the DC component of the switch-node voltage is processed through the voltage divider and the filter, the integrity of the DC component needs to be maintained to detect the small difference between the average switch-node voltage and the output voltage. This is achieved with maximum precision measurements.

When considering the purpose of this work, the minimum objective for this technique is that it must estimate the average current for a given time. If the average current for one program is higher than another, the results must indicate this. Hence there is no actual accuracy requirement, but a comparative analysis must be

possible. The technique presented in this chapter will allow this. It is also capable of estimating the DC current at a particular point in time (excluding transients) with an accuracy of less than 10 %. This may be useful to software developers to get an indication of the current (and power) behaviour at a particular time in the software code.

## 6.6 Conclusion

The test device for the experiments in this chapter was a synchronous buck converter within a power supply module developed by *Analog Devices*. The switch-node of the buck converter was connected to the low-pass filter circuit, designed in Chapter 4, via a voltage divider (so as not to exceed the rail voltage of the filter). The effective DCR was increased to reduce the required precision of the voltage measurements, thereby allowing for testing of the current estimation technique.

Two experiments were performed on the test device. The first experiment was conducted whilst constant resistors were connected at the load. The second experiment was conducted for a load that was periodically switching a dynamic resistor on and off, in parallel with a static resistor. This created a dynamic switching load current.

The steady-state load current experiments allowed for the characterisation parameters of the filter and voltage divider to be determined. It also allowed for validation of the current estimation technique using the filter output voltage as a system input.

For the switching load, the oscilloscope data for the voltage and load current were saved in *MATLAB*. The voltage data required a digital filter to remove high frequency noise in the signal as well as transient voltage spikes. The model was applied to the data and the estimated current waveform was obtained. The mean value of the percentage error with time was approximately 6 %. For the estimated average current, the error was approximately 3 %.

The technique fulfils the minimum requirement of this research. A comparative analysis resulting in two current values is possible based on the results achieved. It is also possible to use this technique to get an indication of the load current behaviour at a given time. The technique can thus be used by software developers for estimation of embedded software power costs. The next chapter shows the application of this technique to estimate the current for actual software operations in an embedded system. A development board will be used as the target test device.

# 7 EMBEDDED SYSTEM EXPERIMENTS

## 7.1 Introduction

In the previous chapter, the current estimation technique developed in this work was tested. The target test device was a synchronous buck converter within a power supply module. The load of the buck converter was accessible; hence the load current of the converter was known in order to validate the current estimation technique. The relevant parameters were calibrated, and the accuracy of the technique was determined.

In this chapter the target test device is an example of an embedded system application device. It is a development board that contains a processor running software operations. Power is delivered to the processor via a synchronous buck converter. The current estimation technique was applied to the buck converter whilst the processor was running various software operations. A description of the target test device is provided and the experimental procedure that was followed is explained. Thereafter, the results of the experiment is shown. The accuracy of the technique was not known but the results are analysed and discussed.

## 7.2 Device Under Test

The test subject for this work is a single-board computer and development board called the *Cubieboard2* [55]. The *Cubieboard2* uses an *AllWinner A20* system on chip (SoC) processor [56]. The power supply to the processor is via the *AXP209* which is the power management unit (PMU) of the device and controls the DC-DC converter that supplies power to the processor [57].

Images of the *Cubieboard2* can be found in Appendix B. The power management unit, the inductor and the processor are labelled on the images in Appendix B. A detailed schematic of the power supply circuit to the CPU is also shown in the

appendix [58]. The relevant sections of the schematic were extracted and are included in the circuit diagram in the next section. A photograph of the complete setup is also shown.

## 7.3 Experimental Setup

A keyboard, screen and mouse were connected to the *Cubieboard2* to allow conduction of the experiments described in this chapter. When switched on, the *Cubieboard2* operates using the Android operating system.

The circuit diagram of the experimental setup showing the buck converter and the processor of the *Cubieboard2* is shown in Figure 7.1 (on the next page). The *AXP209* is the power supply module that contains the switching and control circuitry of the buck converter [57] that supplies the processor. The inductor *L1* and output capacitors $C_{out}$ of the buck are external to the *AXP209*. The output voltage of the buck converter is 1.25 *V* which is the input voltage requirement of the processor.

The connection of the low-pass filter at the switch-node of the buck converter is also shown in the figure. Unlike in the experiments from the previous chapter, the voltage divider was not necessary in this experiment. This is due to the supply of the *Cubieboard2* being a USB 5 *V* supply. This is equal to the positive rail voltage of the filter. Hence the voltage divider was bypassed when connecting the switch-node to the filter module. Oscilloscope probes were connected at the filter output voltage (Channel 1) node and at the buck converter output voltage node (Channel 2) to record the data for various software operations [46]. This is indicated on Figure 7.1. A labelled photograph of the setup is shown in Figure 7.2. (Refer to Section 5.2.2 for a photograph of the filter module.)

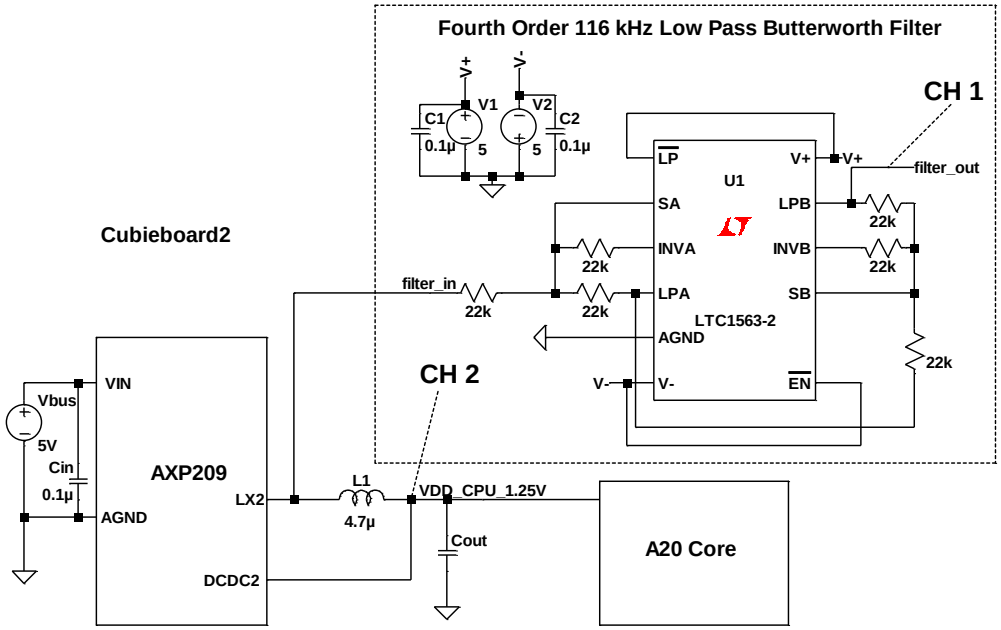



**Figure 7.1: Circuit diagram of the experimental setup**

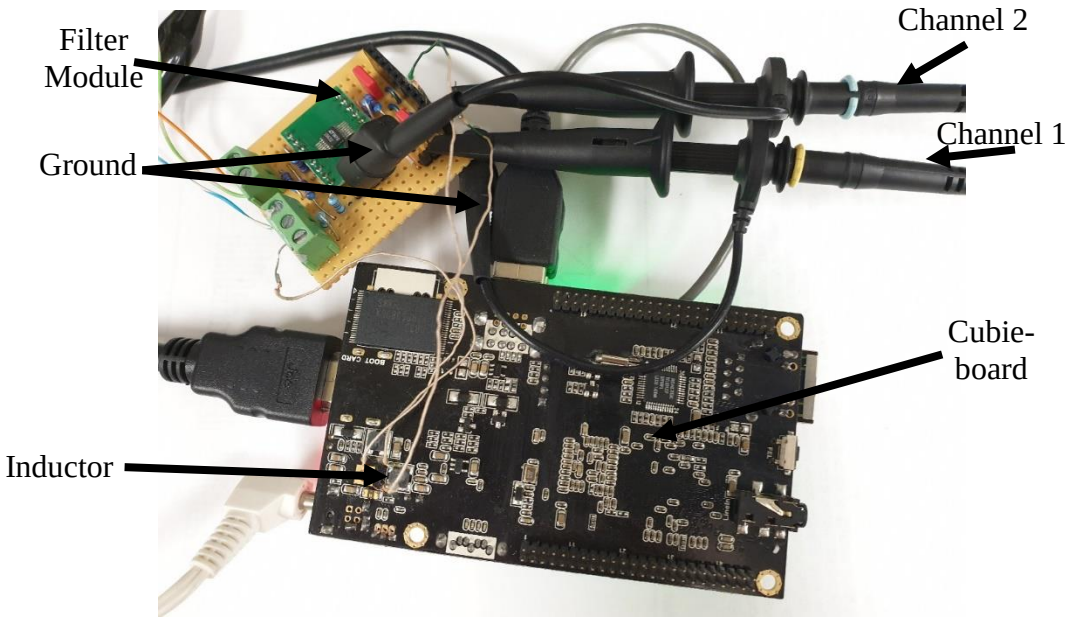



**Figure 7.2: Photograph of experimental setup**

## 7.4 Experimental Procedure

The following experimental procedure was followed.

1. The DCR of the inductor was measured before startup at ambient temperature, using a precision multimeter [50].
2. The oscilloscope time scale was set to 1 *s/div* to allow for 10 *s* of recorded data. The sampling frequency was 500 *kS/s* at high resolution implying that data can be recorded every 2 $\mu s$. This corresponds to a data point being recorded every 3 switching periods for the *Cubieboard's* switching period of 1.5 *MHz* [57].
3. A CPU Benchmark Test application was downloaded on the *Cubieboard2* called *PassMark Performance Test* [59] that allows speed testing and benchmarking for mobile devices. The *Cubieboard2* was operated for the following three test cases using this application:
   - During idle operation or standby when no applications were running
   - During a memory write operation
   - Whilst rendering 3D graphics

   These three test cases were chosen because they are typical operations for testing the performance of a processor. It is expected that the idle operation will consume the least current whilst the 3D graphics operations will consume the most. If the current estimation technique yields this result it can be validated.
4. For each test case, the oscilloscope was run for approximately 10 *s* until being stopped. The data was then saved to *.csv* files.
5. Due to the high sampling rate of 500 *kS/s*, the raw data over the full time period was noisy as was shown in the previous chapter [52]. To eliminate the noise, a digital moving-average filter was applied. The window size was set to 100 implying that a moving average was computed every 200 $\mu s$ (i.e $\frac{1}{200\ \mu s} = 5\ kHz$ cut-off frequency) eliminating any dynamic effects within that period. It also implies that a delay in the filtered data of 200 $\mu s$ was evident at data transients.

6. The current estimation technique was applied to the data in each test case using *MATLAB*. This is shown in the flow diagram in Figure 7.3. The filter output voltage data and the buck output voltage data are first digitally filtered (as per the previous step) to eliminate high frequency noise and transient spikes. The filter offset voltage and gain were the same values characterised in the previous experiment. (The reason for this is that in the previous experiment, due to the voltage divider, the input average switch-node voltages were approximately 1.65 *V*. In this case it is similar because the supply voltage of the processor is 1.25*V*. Hence, the average switch-node voltage will be higher than this and will be similar to values in the previous experiment. Thus, the filter should behave in the same way.) After processing the filter voltage data and the buck output data as shown in Figure 7.3, the data and the DCR were inserted into the steady-state current model to estimate current. The results from each test case are presented in the next section.

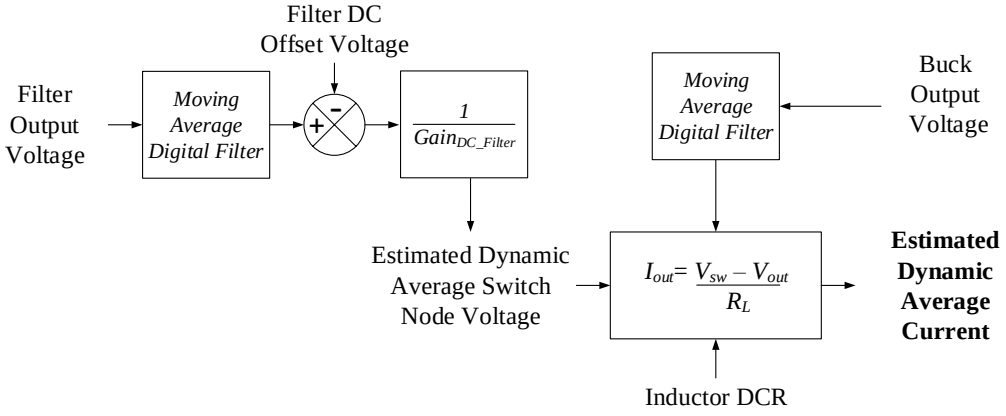



**Figure 7.3: Data processing and application of steady-state model to estimate average load current**

## 7.5 Results and Analysis

Before start-up, the DCR of the inductor was determined at **72.5 mΩ** at ambient temperature. The results and analysis of each test case is presented below, and an overall discussion appears thereafter.

### 7.5.1 Test Case 1: Standby Mode

***Results***

For this test case, the *Cubieboard2* was switched on and was left in in standby mode i.e. no applications were open. The original data that was saved is shown in Figure 7.4. Applying the digital filter to the data (1 D moving-average with a window size of 100 data points), yielded the waveforms in Figure 7.5. This data was applied to the technique in Figure 7.3 to yield the estimated current waveform in Figure 7.6. A zoomed-in view of 110 *ms* of data in Figure 7.7 shows the estimated current behaviour during the voltage spikes that occur approximately every 2 *s* in standby mode. An analysis of the results appears after the figures.

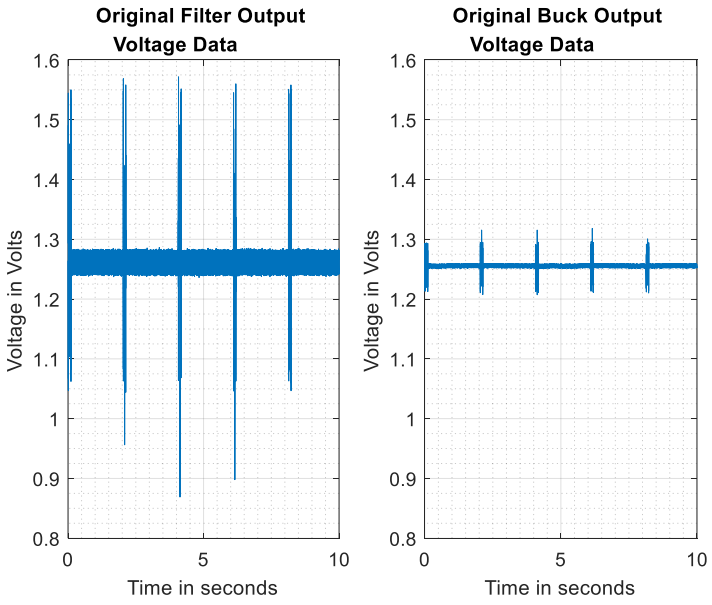



**Figure 7.4: Original data for standby mode operation of the *Cubieboard2***

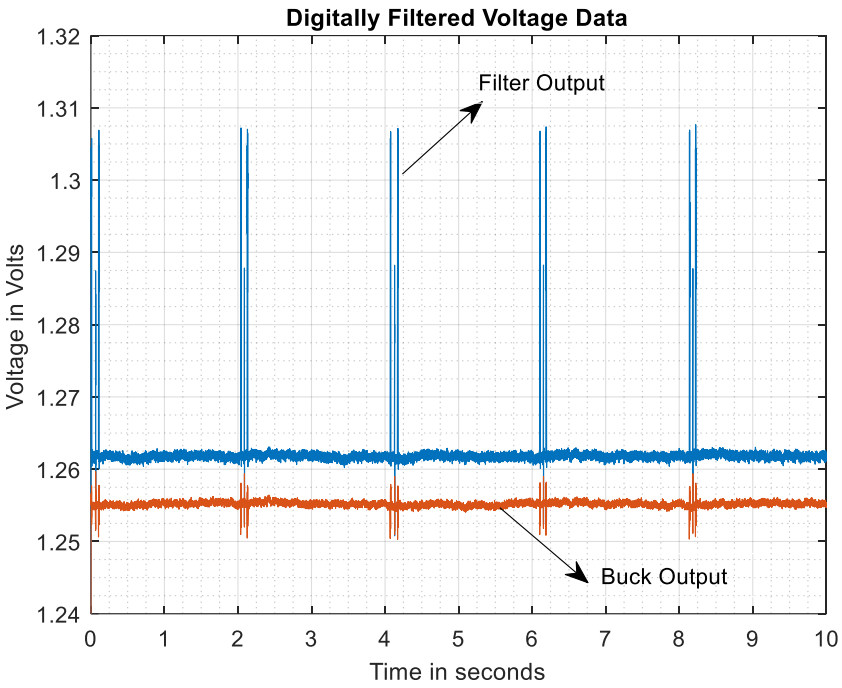



**Figure 7.5: Digitally filtered data of filter output and buck converter output for standby mode operation of the *Cubieboard2***

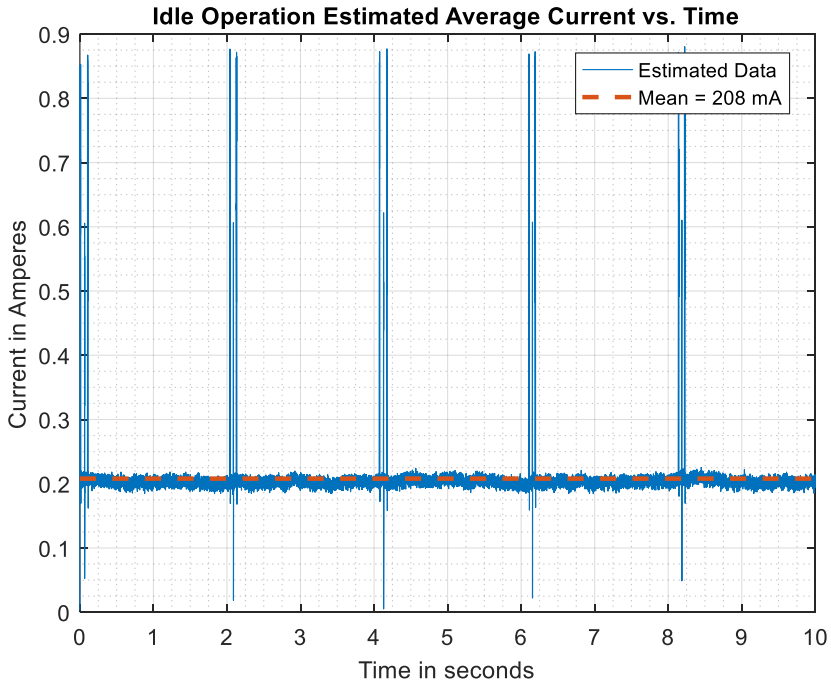



**Figure 7.6: Estimated average processor current vs. time for standby mode operation of the *Cubieboard2***

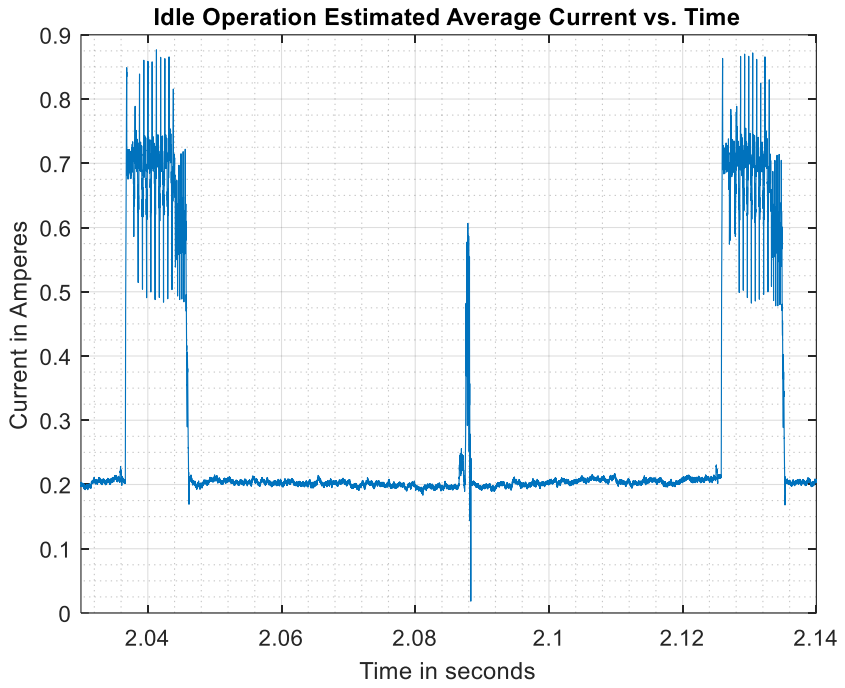



**Figure 7.7: Zoomed-in estimated average current vs. time for standby mode operation of the *Cubieboard2***

***Analysis***

The results in Figure 7.6 show that the processor draws a baseline of approximately 200 *mA* of current in standby mode, with a transient occurring approximately every 2 *s*. The zoomed-in view in of the transient, shown Figure 7.7, shows that the apparent transients in Figure 7.6 actually consists of two transients that rise from 200 *mA to* approximately 700 *mA*, thereafter the 700 *mA* transitions to 600 *mA* before switching back to 200 *mA* (around the 2.04 *s* and 2.14 *s* mark). Between these two time periods, there is a quick transient that is not fully captured in the data and requires a more zoomed-in view with a smaller timescale. The calculated mean value of the current drawn in standby mode is 208 *mA*.

### 7.5.2 Test Case 2: Memory Write Operation

***Results***

For this test case, the *Cubieboard2* performed a memory write operation. The original data that was saved is shown in Figure 7.8. Applying the digital filter to the data (1 D moving-average with a window size of 100 data points) yielded the waveforms in Figure 7.9. This data was applied to the model in Figure 7.3, shown in the previous section, to yield the estimated current waveform in Figure 7.10. A zoomed-in view of the data in Figure 7.11 shows the estimated current behaviour during a random interval of 110 *ms* of data. An analysis of the results appears after the figures.

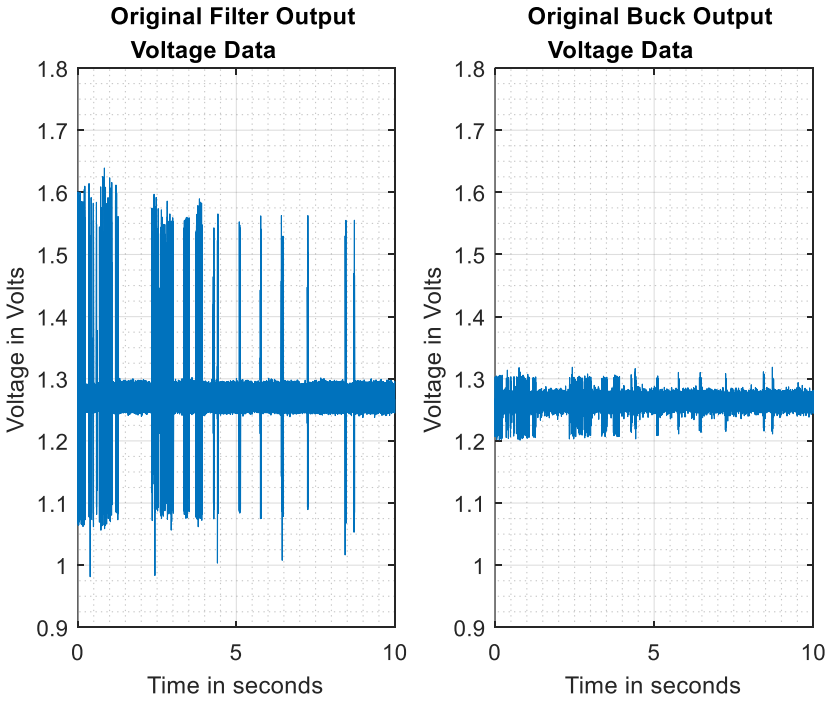



**Figure 7.8: Original data for memory write operation of the *Cubieboard2***

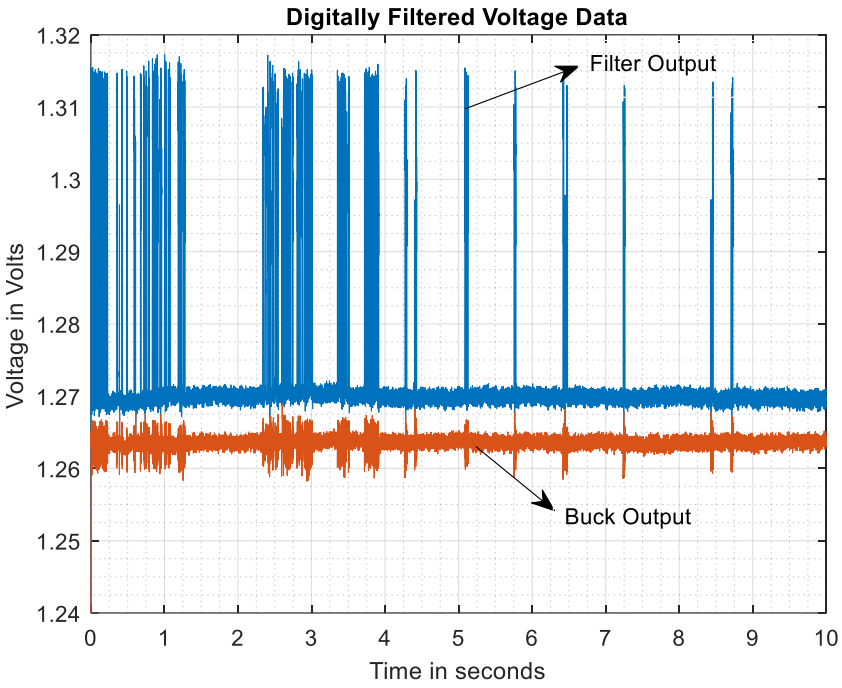



**Figure 7.9: Digitally filtered data of filter output and buck converter output for memory write operation of the *Cubieboard2***

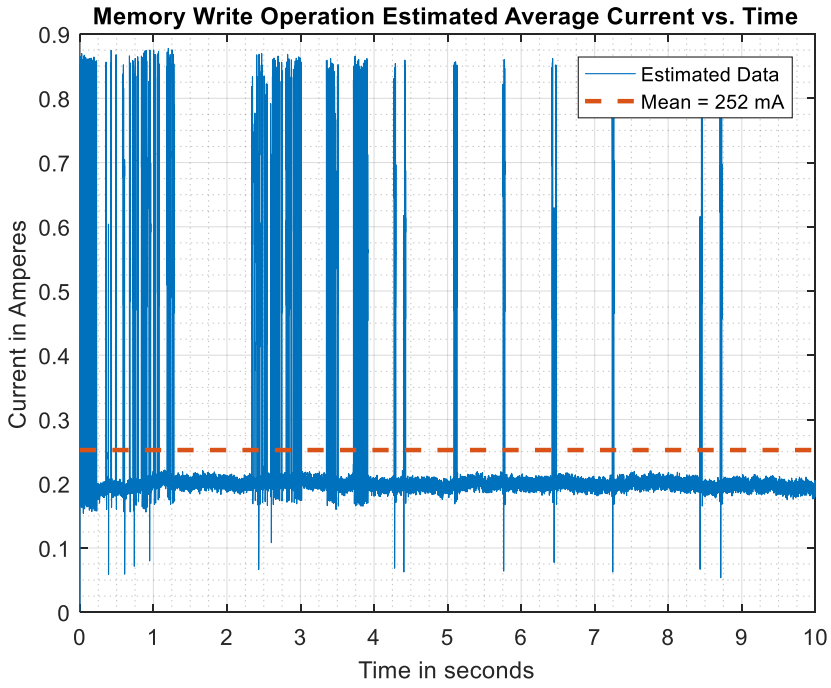



**Figure 7.10: Estimated average processor current vs. time for memory write operation of the *Cubieboard2***

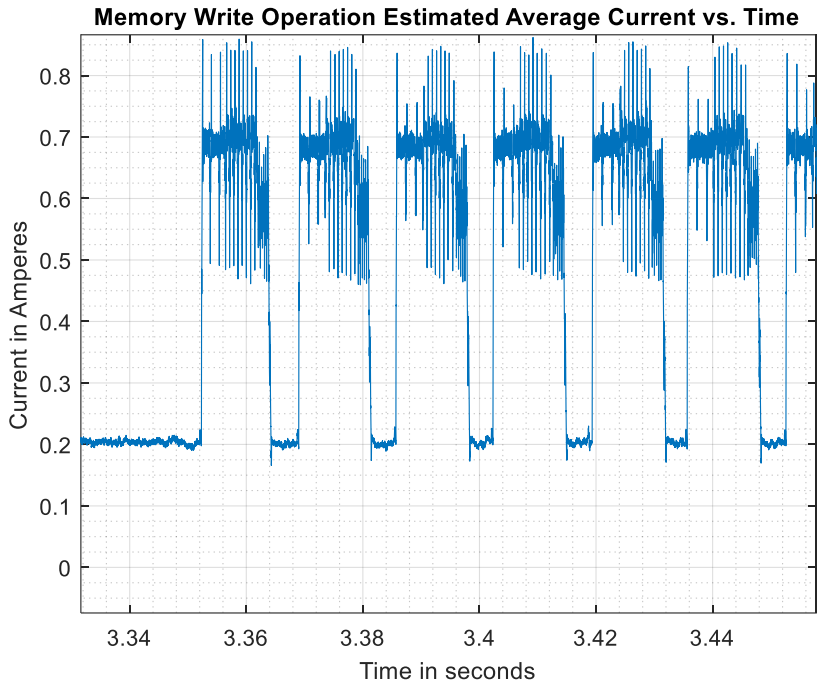



**Figure 7.11: Zoomed-in estimated average current vs. time for memory write operation of the *Cubieboard2***

***Analysis***

The results in Figure 7.10 show that the baseline of current drawn by the processor is approximately 200 *mA*. There are more frequent transients in the first 5 *s* of the data compared to the last 5 *s* of data. A zoomed-in view of the data shown Figure 7.11 shows that these transients switch from 200 *mA to* approximately 700 *mA*. Thereafter the 700 *mA* transitions to 600 *mA* before switching back to 200 *mA*. This is approximately equal to the transients visible in standby mode. However, these are more frequent, resulting in an increased mean value of the current drawn whilst a memory write operation is taking place. i.e. 252 *mA*.

### 7.5.3 Test Case 3: 3D Graphics

***Results***

For this test case, a 3D graphics CPU Benchmark Test was performed on the *Cubieboard2* (using the *PassMark Performance Test* application) [59]. The original data that was saved is shown in Figure 7.12. Applying the digital filter to the data (1 D moving-average with a window size of 100 data points) yielded the waveforms in Figure 7.13. This data was applied to the model in Figure 7.3, shown in the previous section, to yield the estimated current waveform in Figure 7.14. A zoomed-in view of 100 *ms* of data in Figure 7.15 shows the estimated current behaviour during 100 *ms* of the *3D graphics test* operation,

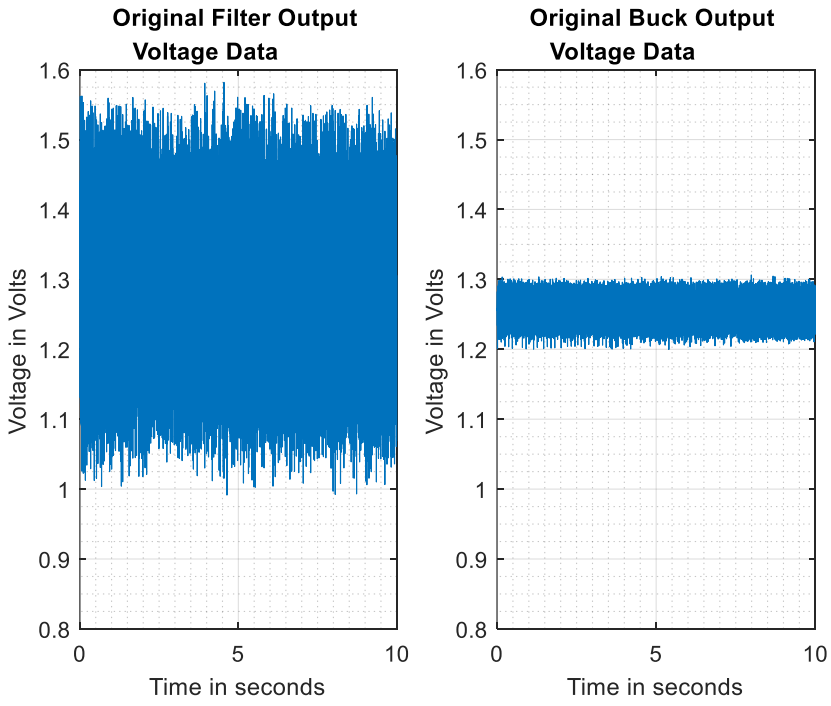



**Figure 7.12: Original data for 3D graphics operation of the *Cubieboard2***

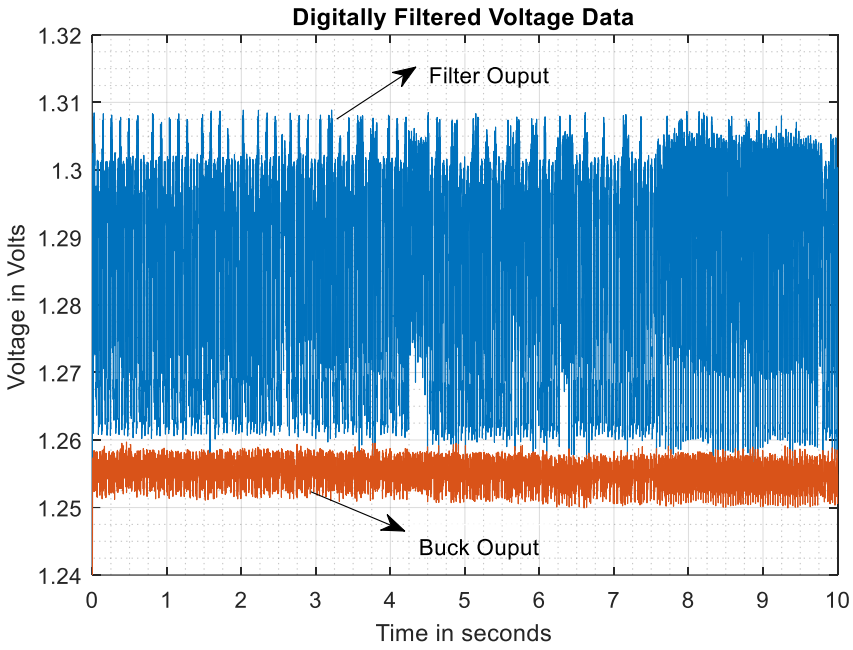



**Figure 7.13: Digitally-filtered data of filter output and buck converter output for 3D graphics operation of the *Cubieboard2***

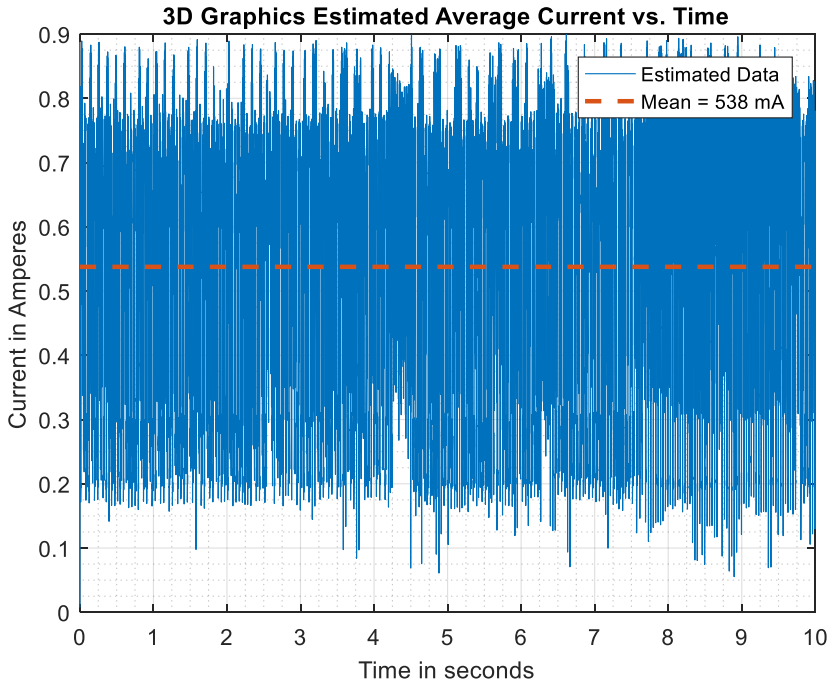



**Figure 7.14: Estimated processor average current vs. time for 3D graphics operation of the *Cubieboard2***

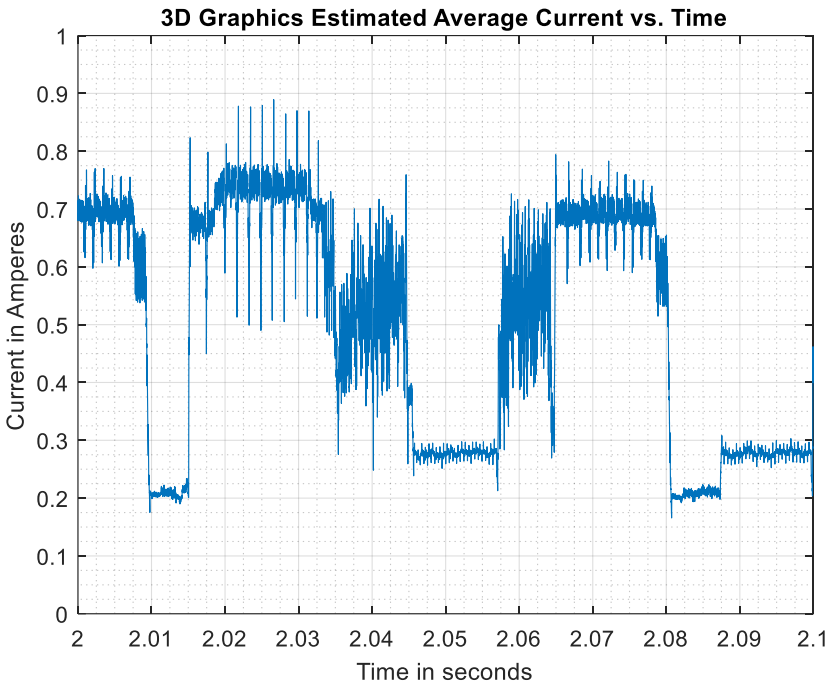



**Figure 7.15: Zoomed-in estimated average current vs. time for 3D graphics test case**

***Analysis***

The estimated current data in Figure 7.14 shows that there are frequent transients in the processor current for a 3D graphics operation. The mean value of the estimated current is the highest for this test case at approximately 538 *mA* . This is as expected due to the rendering of 3D graphics being a processor intensive operation. Figure 7.15 shows that the upper limit of the current is the same as the previous cases (an average of approximately 700 *mA*). The baseline current is also the same as the previous cases (an average of approximately 200 *mA*). There are other transient current values occurring in between these transitions that are visible on Figure 7.15.

## 7.6 Discussion

The estimated mean average current consumed during standby is the lowest among the three test cases. This as one would expect. There is a small increase in the estimated mean average current during a memory write operation. The highest estimated mean average current among the test cases was for the rendering of 3D graphics operation.

Due to the high sample rate, a zoomed-in view was possible showing more detail of current behaviour. Depending on the type of information required by the software developer, the sample rate and window size selection can be adjusted.

The exact error of the results is unknown, but a tolerance of 10 % on the average current values can be assumed, based on the results from the previous chapter. Even if the exact error is unknown, this technique can be used to perform a comparison analysis between two software operations.

If the power consumption data is required, it can be computed from the current data by $P = VI$. However, since the voltage is approximately fixed, the power consumption is proportional to the current consumption and the current data is sufficient for a comparison analysis.

## 7.7 Conclusion

The processor current estimation technique presented in this work was tested on the *Cubieboard2* to represent the application of the technique in an embedded device.

The current estimation technique was tested for three test cases on the *Cubieboard2*. The mean of the estimated current was as expected overall i.e. low for standby, slightly higher for memory writing operation and the highest for rendering 3D graphics.

A tolerance of 10 % on the results was characterised by the experiments in the previous chapter. This technique could be used by software developers to estimate software power and optimise the software. The next chapter provides an overall summary of this dissertation.

# 8 CONCLUSION

## 8.1 Overall Summary

The objective of the research was to achieve a non-invasive processor current estimation technique for software power estimation in embedded systems. Current sensing techniques that exist for this purpose are invasive and require modification of hardware.

Non-invasive current sensing techniques are employed in DC-DC converter control for inductor current sensing rather than load current estimation. It was shown that the average inductor current in a DC-DC converter is equal to its load current and hence the processor current in an embedded system. Thus, non- invasive inductor current sensing techniques are applicable to the research objective. A review of these techniques was performed. *The average current sensing technique* that was reviewed, employs a filter at the switch-node of a buck converter and was adapted for this work.

A model for steady-state current and dynamic current in a buck converter was derived using techniques established by Erickson [27]. The steady-state model was dependent on the DC component of the switch-node voltage while the AC model was dependent on the low-frequency AC component of the switch-node voltage. The application of the steady-state model to the research objective was shown. A discussion on parameters that were excluded from the model showed that the exclusions were valid.

Since the steady-state model was dependent on the DC component of the switch-node voltage, it was determined that a low-pass filter will be employed to provide an analogue average of the switch-node voltage. Analogue filtering was preferred to digital filtering because digital filtering is dependent on sampling of the switch-node voltage. Due to fast-switching in a buck converter, this would require a large

sample rate, that may not be possible for the time duration of the signal. The filter cut-off frequency was designed to be lower than the switching frequency, to eliminate switching effects. The minimum cut-off frequency was required to be equal to the bandwidth of the controller in order to have a transient response that is on par or faster than the controller. The filter order was selected to be fourth to allow attenuation of the switching harmonics and maintain the low-frequency components of the signal with minimal ripple voltage. The filter was designed and tested. A current estimation technique was developed based on the filtering of the switch-node voltage and the steady-state load current model.

Simulation experiments were conducted to validate the steady-state and dynamic models and to test the accuracy of the current estimation technique. The simulation experiments validated the steady-state and dynamic models. It verified that the low-pass filter output voltage could be used to compute the load current.

A power supply module consisting of a buck converter that provides a 3.3 $V$ output voltage, with maximum 2 $A$¸ was used as a test device to experimentally validate the current estimation technique. This was achieved by connecting known steady-state loads at the output voltage of the power supply module to calibrate the necessary parameters and validate the technique for the steady-state current values. A switching load was connected to validate the technique for a switching dynamic current. The results from the experiments validated the technique and estimated the load current with an overall error of the average current less than 10 %. This was considered good because the accuracy requirements of this technique ae not required to be high for the minimum objective of this work i.e. software power optimisation.

The current estimation techniques were tested on the *Cubieboard2* which represents an embedded system application. Current estimation results were obtained for ten seconds during three test cases. The test cases were during standby, during a memory write operation and during rendering of 3D graphics. A characterisation of the average current vs. time was obtained and the computed average of the

estimated current was as expected, based on the test case i.e. it was highest during rendering of 3D graphics and lowest during standby. Based on the power supply module experiments, the tolerance of the results was approximated to be 10 %. It was concluded that whilst the exact error of the current estimation technique is unknown in an embedded system such as the *Cubieboard2*, it can be employed by software developers to perform a comparison analysis and achieve software power optimisation.

## 8.2 Future Work

This work did not include the thermal resistance of the inductor. For future work, the effect of DCR temperature drift on the model can be included. This can be achieved by tracking the temperature of the inductor using a temperature sensor and recording the temperature of the inductor as it varies with time. The temperature coefficient of resistance can be used to produce a time-varying waveform of DCR from the time-varying temperature data.

Another approach that can be used to include the effect of temperature drift is to include the thermal resistance of the inductor into the model. It can be included to create a time varying DCR dependent on current. At each predicted value of current, the DCR for the next predicted value can be adjusted based on the current and the thermal resistance.

Furthermore, for future work, a program can be written in conjunction with the measurement instrument. It can be such that the user can select the time duration, sampling rate and window length of the digital filter. The user can then provide the real-time measured filter output data, the real-time buck output data and DCR data as inputs to estimate and display the real-time moving average of the current. This will provide a real-time power estimation to an embedded software developer during the software development phase which can be used to improve power efficiency during coding.

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# APPENDIX A ANALOG DEVICES SYNCHRONOUS BUCK CONVERTER TEST DEVICE

## A.1 Synchronous Buck Description and Schematics

The synchronous buck converter test device is part of the CN-0190 (A robust, multivoltage, 25 *W* Universal Power Supply Module with 6 *V* to 14 *V* input) manufactured by *Analog Devices.* A photograph of the complete module appears in Figure A.1.

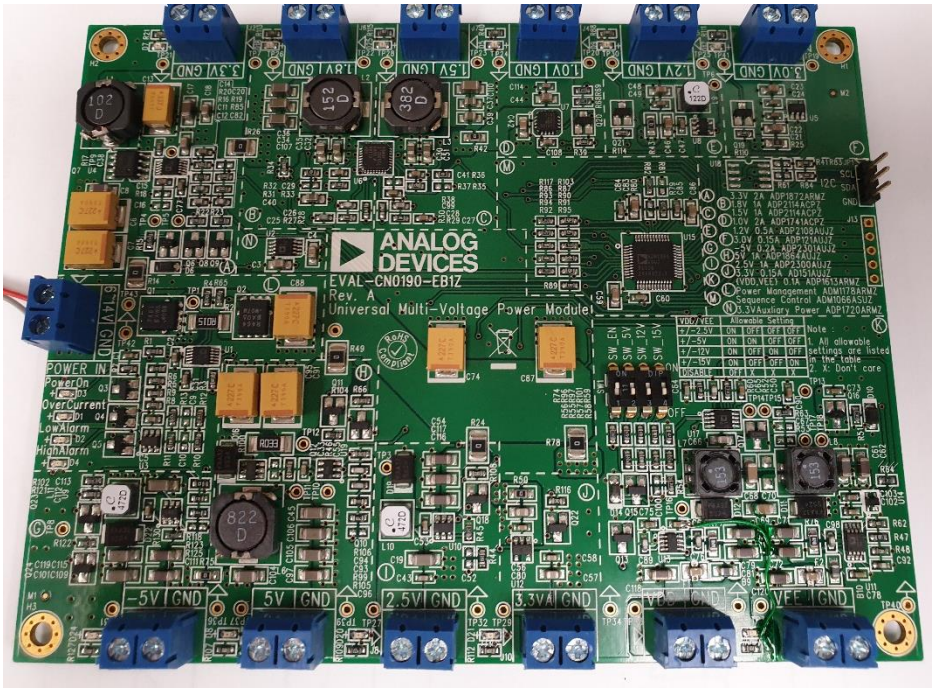



**Figure A.1: Photograph of the CN-1090 Power Supply Module**

Figure A.1 shows that there are ten possible voltage outputs where a load can be connected. For this work, the 3.3 *V* 2 *A* output from a synchronous buck converter was selected for the experiments. The synchronous buck converter has a default switching frequency of 600 *kHz* and employs the *ADP1872* [49] for control of the synchronous buck. The schematics of the 600 *kHz* 6~14 *V* input 3.3 *V* 2 *A* output synchronous buck converter are extracted from the CN-0190 schematics and shown in Figure A.3 [60].

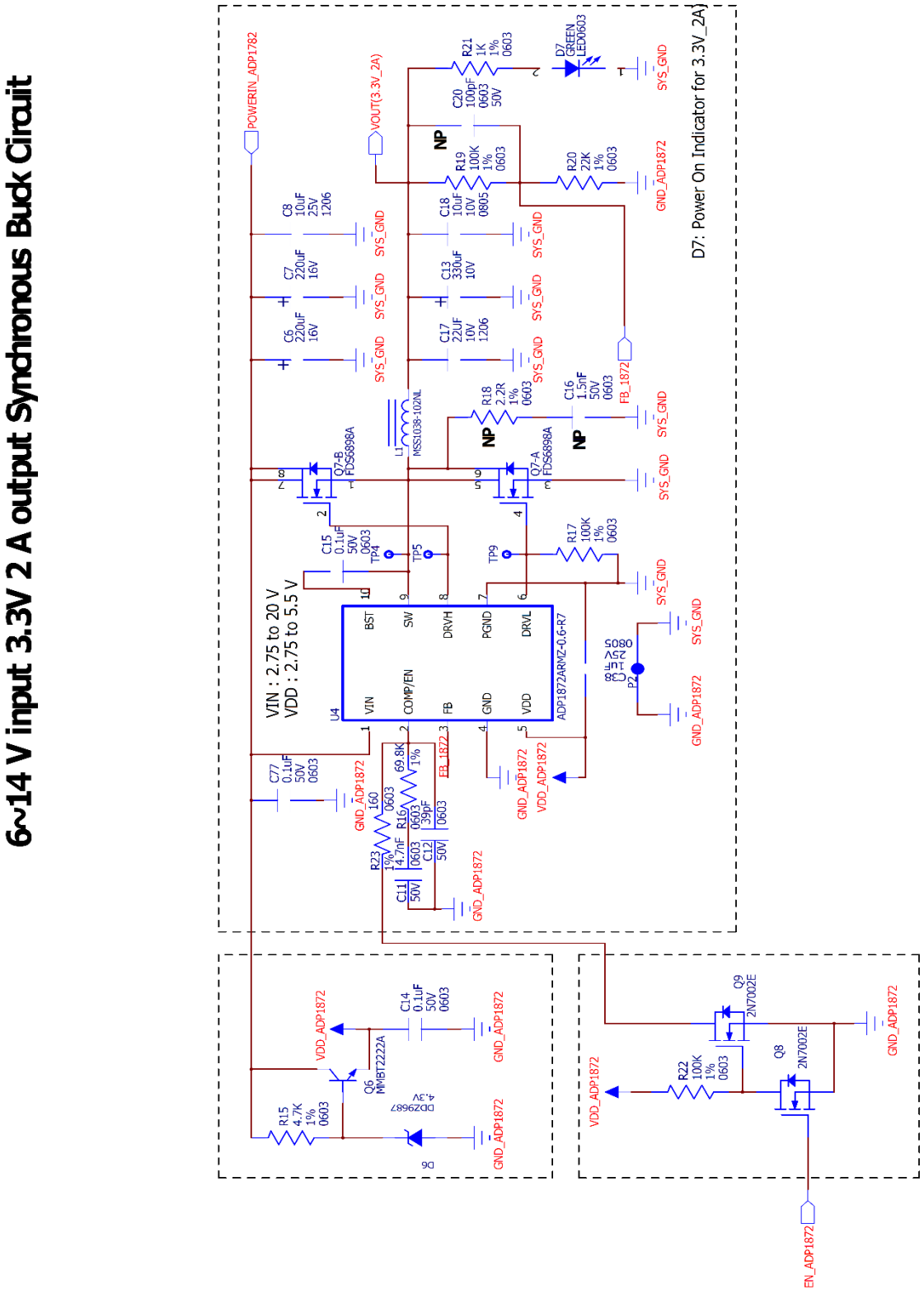



**Figure A.2: Schematics of the 600 *kHz* 6~14 *V* input 3.3 *V* 2 *A* output synchronous buck converter**

## A.2 Experimental Validation of Synchronous Buck Controller Bandwidth

### A.2.1 Objective

The objective of this experiment was to experimentally validate that the bandwidth of the controller is consistent with the bandwidth calculated from the controller's datasheet information (*ADP1872* [49]).

### A.2.2 Experimental Procedure

The experimental procedure is as follows:

1. Calculate the bandwidth given the buck converter schematics and controller datasheet information.
2. Apply a step change in load current to the buck converter.
3. Approximately measure the ringing frequency of the output voltage which represents the bandwidth of the controller [42] by applying a slow switching load.
4. Verify the bandwidth by applying a load that switches faster than the approximately measured bandwidth in the previous section.

### A.2.3 Results

***Bandwidth Calculation***

An excerpt from the *ADP1872* datasheet appears in Figure A.3 showing that the cut-off frequency is controlled by $R_{COMP}$ and $C_{COMP}$ [49]. Examining the circuit in Figure A.2 and substituting the values $R_{COMP} = 69.8\ k\Omega$ and $C_{COMP} = 4.7\ nF$, the expected bandwidth of the control loop was calculated to be 1.94 *kHz.*

**Crossover Frequency**

The crossover frequency is the frequency at which the overall loop (system) gain is 0 dB (H = 1 V/V). It is recommended for current-mode converters, such as the ADP1872, that the user set the crossover frequency between 1/10th and 1/15th of the switching frequency.

$$f_{CROSS} = \frac{1}{12} f_{SW}$$

The relationship between $C_{COMP}$ and $f_{ZERO}$ (zero frequency) is

$$f_{ZERO} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}$$

The zero frequency is set to 1/4th of the crossover frequency.

Combining all of the above parameters results in

$$R_{COMP} = \frac{f_{CROSS}}{f_{CROSS} + f_{ZERO}} \times \frac{2\pi f_{CROSS} C_{OUT}}{G_M G_{CS}} \times \frac{V_{OUT}}{V_{REF}}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{ZERO}}$$

**Figure A.3: Datasheet information on bandwidth**

***Bandwidth Measurement***

A switching load was connected the output of the synchronous buck under test, as shown in Figure A.4. A 555 timer IC in monostable operation [51] was used to switch a dynamic resistance *R2* in parallel with static resistance *R1* at a frequency of 21.8 *Hz*. The output current was thus switched from 485 *mA* to 1.7 *A*. The resulting gate voltage waveforms and AC coupled output waveforms are shown in Figure A.5 to Figure A.7. From [42], it is stated that the ringing frequency at the transient response indicates the bandwidth. Due to the high phase margin of this controller, the ringing is minimised [34], [42]. Upon inspection, based on the rise time of the transient voltage peak, the ringing frequency would have been approximately $\frac{1}{0.5ms} = 2\ kHz$ which is consistent with the calculated bandwidth.

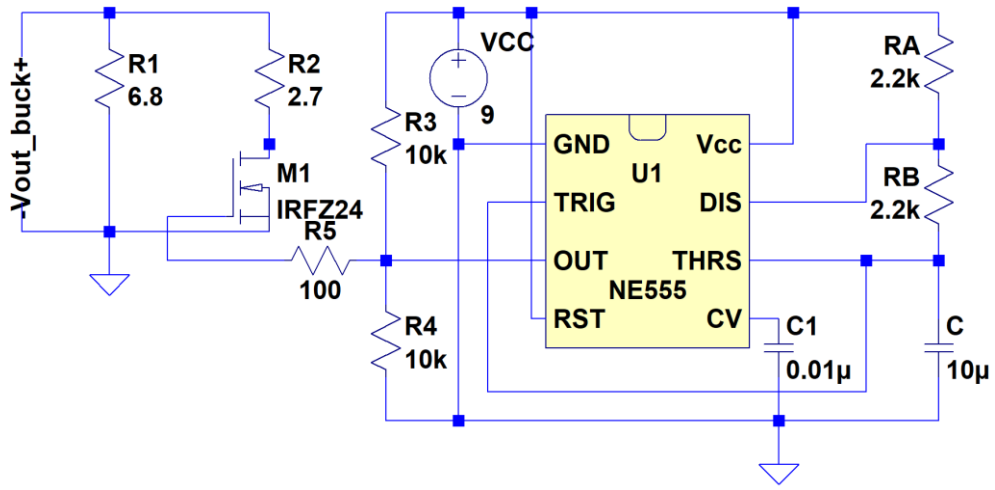



**Figure A.4: Buck converter load connection switching the load current from 485 *mA* to 1.7 *A* at a frequency of 21.8 *Hz***

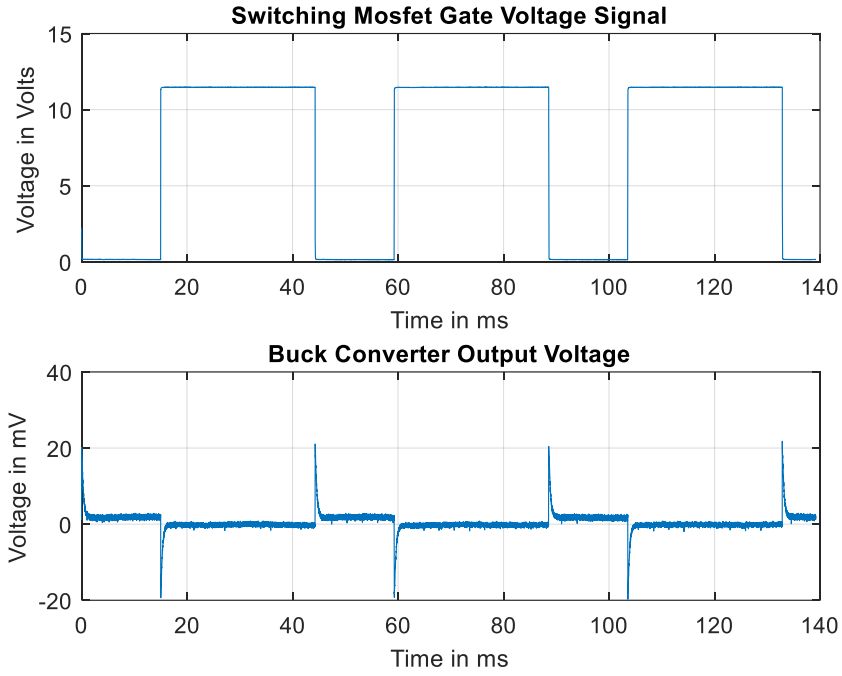



**Figure A.5: Waveforms with load current changing at a frequency of 21.8 *Hz***

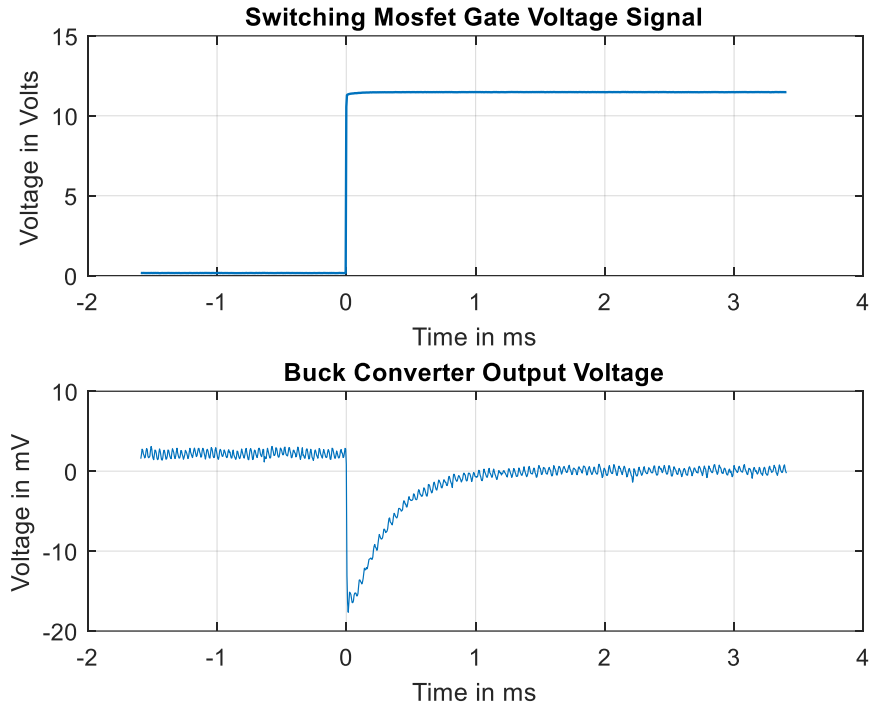



**Figure A.6: Waveforms for a step up in load current**

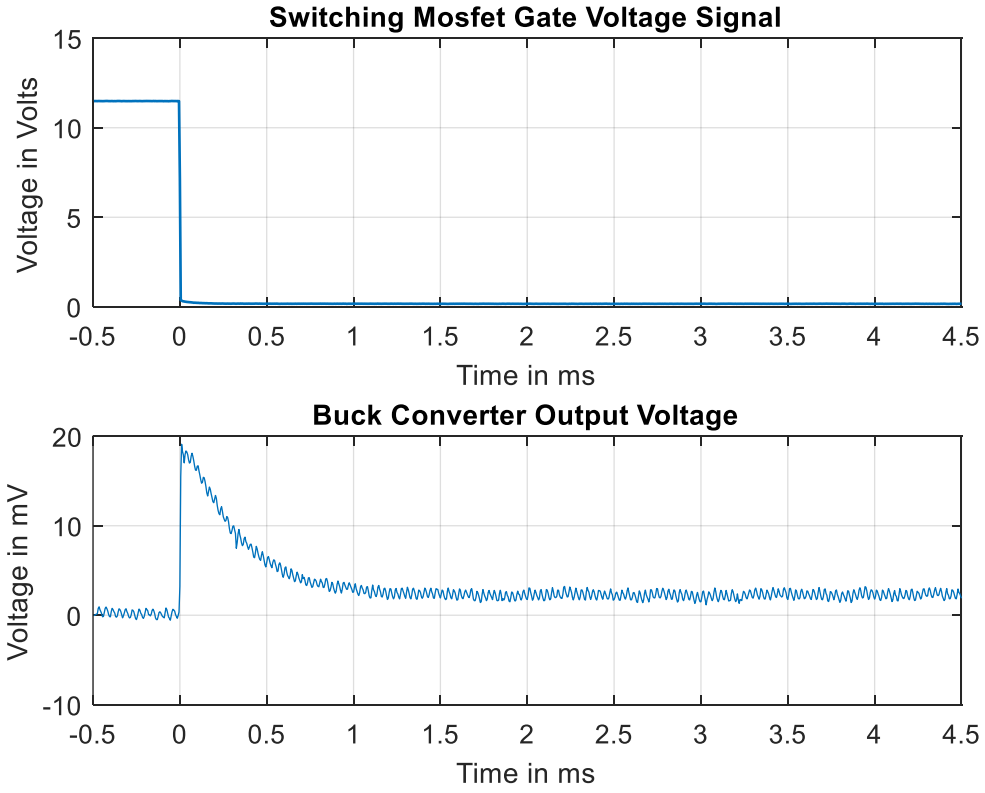



**Figure A.7: Waveforms for a step down in load current**

***Verification of Bandwidth Measurement***

The switching frequency of the load in Figure A.4 was adjusted to 4.8 *kHz* i.e. above the approximated bandwidth of +/- 2 *kHz*. The resulting waveform at the gate of the switching MOSFET and the AC coupled output voltage are given in Figure A.8 - Figure A.10. There is no "settling" of the output voltage, instead only the +/-20 *mV* peaks evident in Figures A.5 and A.6 occur before the load switches again preventing the output voltage from settling. This validates the calculation that the bandwidth is approximately 1.9 *kHz* because no settling is evident with the load switching at a greater rate than the calculated bandwidth.

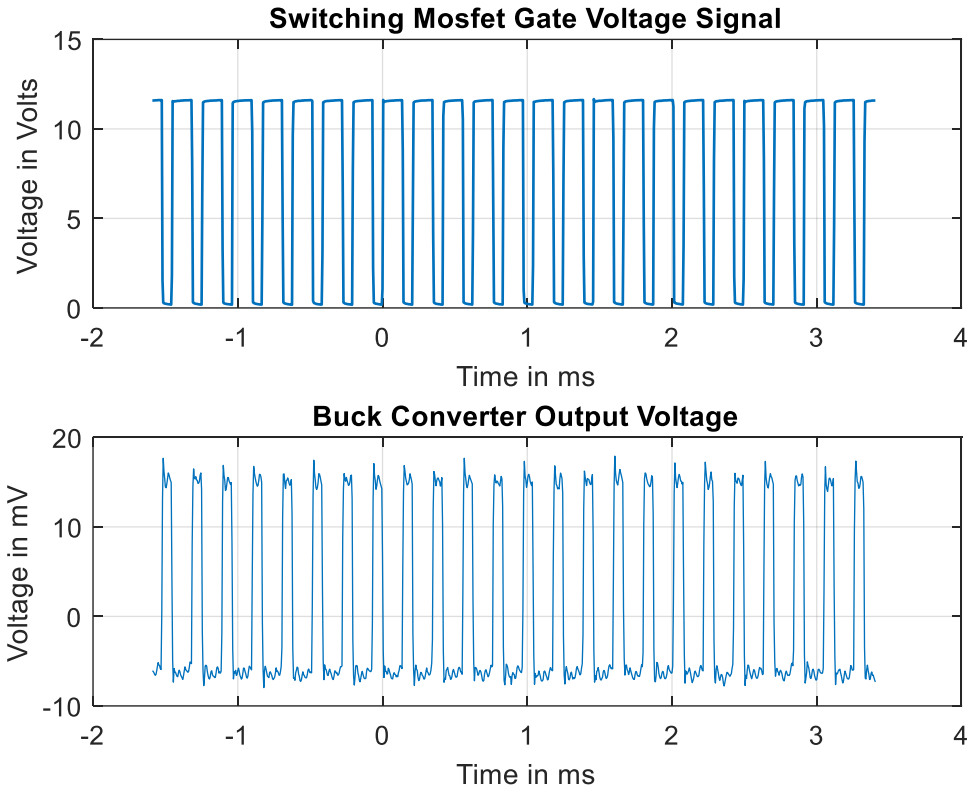



**Figure A.8:Waveforms with load current changing at a frequency of 4.8 k*Hz***

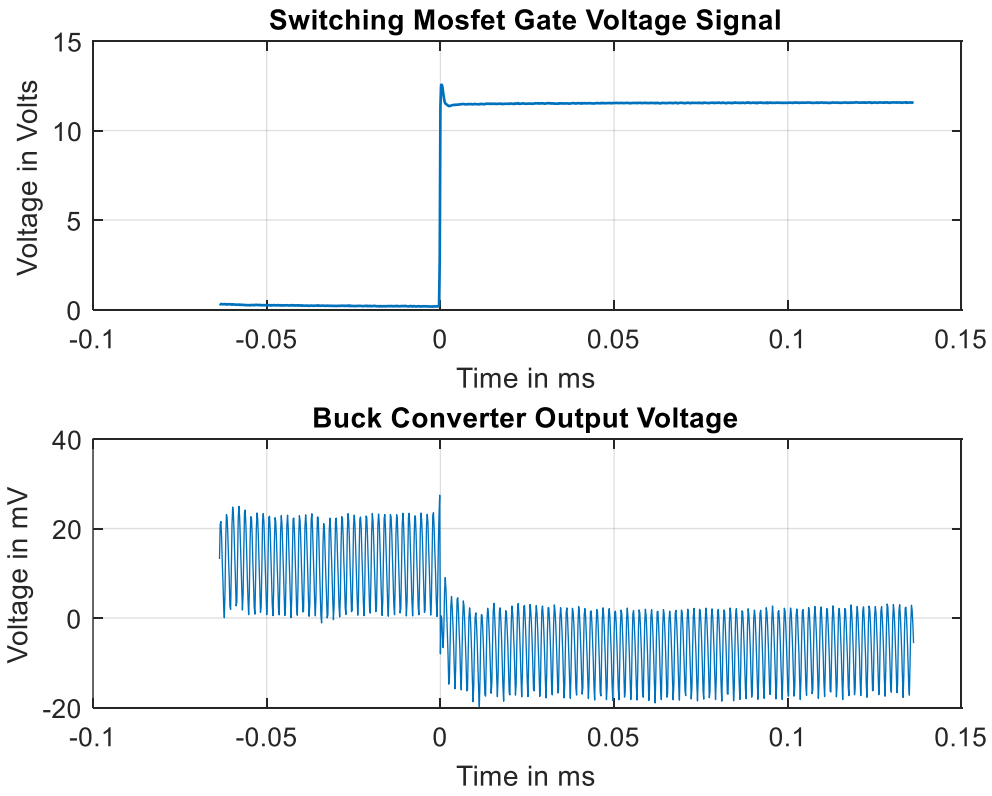



**Figure A.9: Waveforms with a step up in load current**

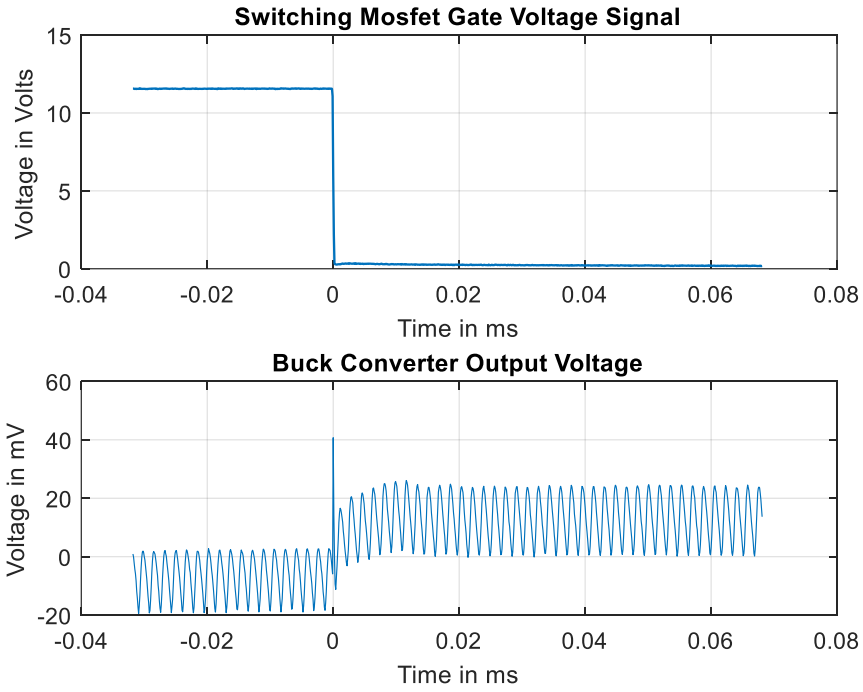



**Figure A.10: Waveforms with a step down in load current**

### A.2.4 Conclusion

The bandwidth of the controller was calculated to be 1.9 *kHz* based on the compensation circuit and the design equations from the datasheet.

The experiments validated the calculated bandwidth of the controller. The bandwidth was measured to be to be approximately 2 *kHz* with a slow switching load (21.8 *Hz*) . When a faster switching load was applied (4*kHz*), the output voltage did not settle, thereby also validating the bandwidth of approximately 2 *kHz.*

## A.3 Experimental Determination of Effect of Temperature on DCR

### A.3.1 Objective

The objective of this experiment is to determine the effect the temperature has on the DCR of inductor *L1* from the synchronous buck test device in Figure A.3.

### A.3.2 Experimental Procedure

1. The inductor, $L_1$ , in is a 1 $\mu H$ inductor with a maximum DCR of 6 mΩ and maximum operating temperature of 125 °C [61]. The inductor was removed and placed in a temperature chamber with a precision digital multimeter connected across the probes as shown in Figure A.11.

2. The temperature of the chamber was increased in steps of 10 °C from 20 °C until 90 °C and the corresponding resistance of the inductor was recorded when the temperature stabilised.

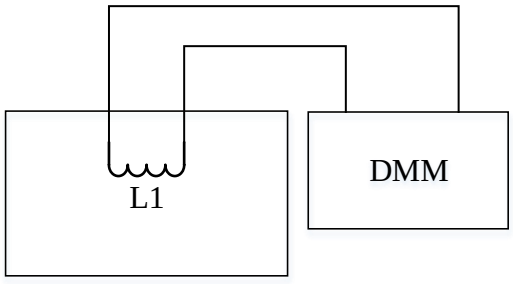



**Figure A.11: Test Setup**

### A.3.3 Results

The results are given in Figure A.12. As predicted, the resistance increases linearly with temperature. The linear approximation of the results yielded a temperature coefficient for the inductor winding of 0.00354 which is a 9.69% difference from the temperature coefficient of annealed copper.

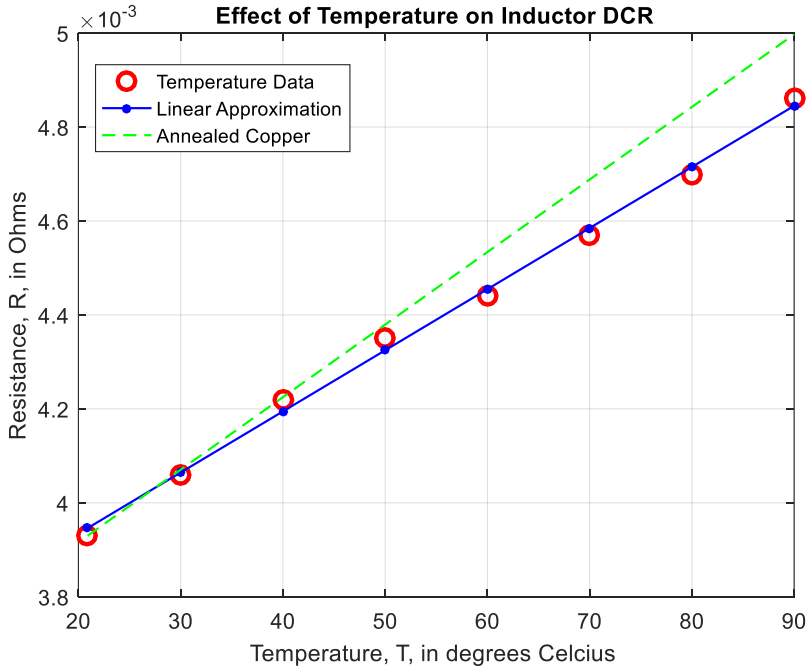



**Figure A.12: Results of temperature experiment**

### A.3.4 Conclusion

A temperature characterisation of the DCR was performed. The resistance vs. temperature plot in Figure A.12 shows that the resistance of the inductor increases with a temperature coefficient of 0.354 %/°C**.** The temperature effect is similar to that of a copper conductor.

# APPENDIX B CUBIEBOARD2 TEST DEVICE

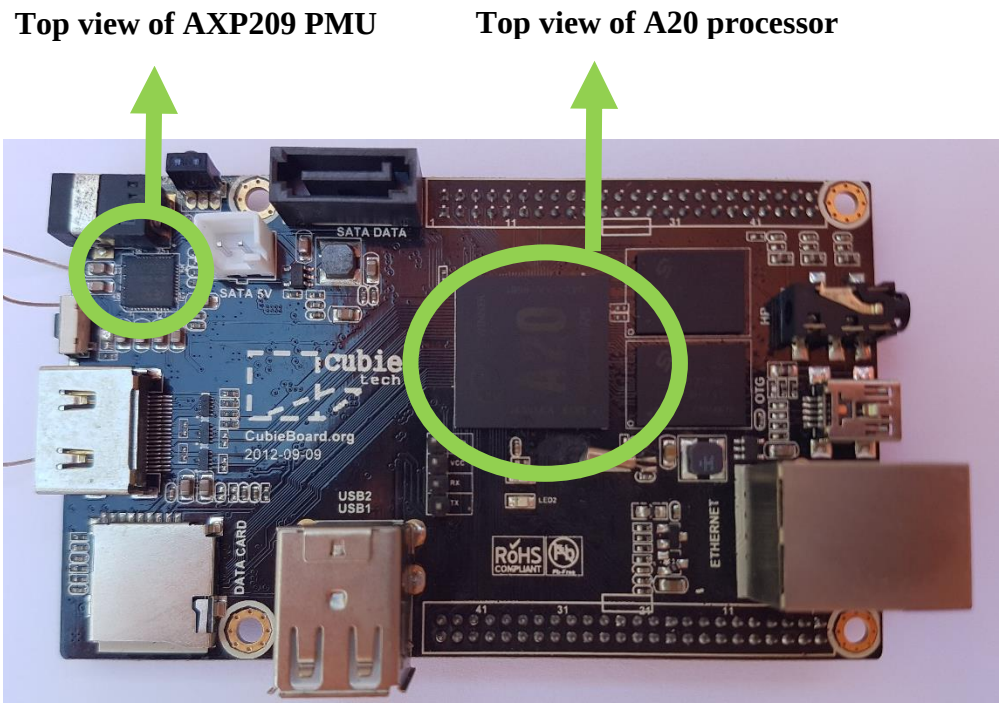
## B.1 Cubieboard2 Processor and Power Supply Description

The test subject for this work is the *Cubieboard2* [58]. It is a single-board computer and development board. The *Cubieboard2* uses an *AllWinner A20* system on chip (SoC) processor [56].

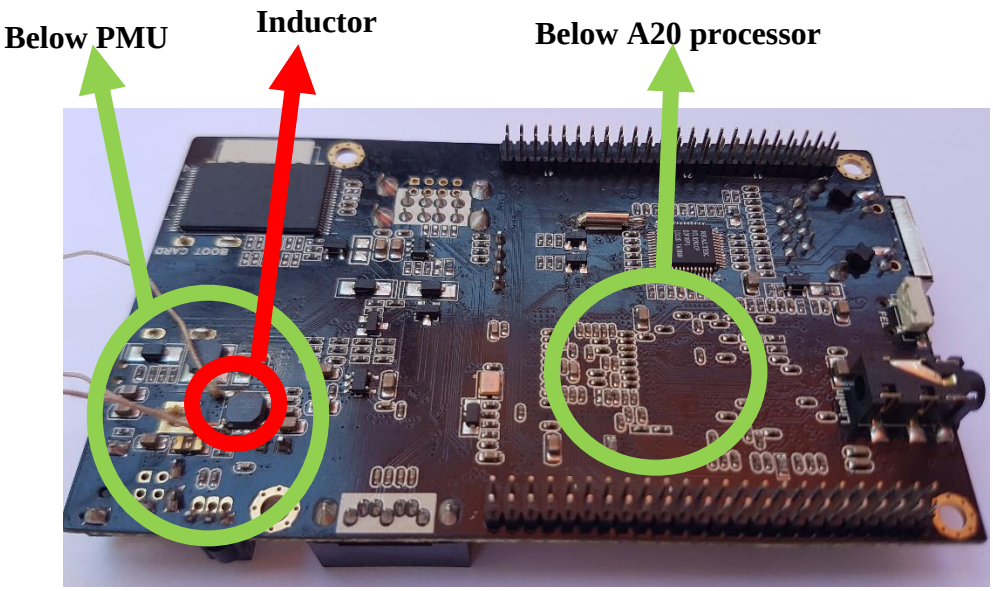
The power supply to the processor is via the *AXP209* which is the power management unit (PMU) of the device. It contains the DC-DC converter that supplies power to the processor [57].

## B.2 Images and Power Supply Schematics

Figure B.1 shows images of the top and bottom view of the *Cubieboard2* and indicates the position of the processor and PMU, described above, on the board. The processor is a surface mounted ball grid array (BGA) packaged chip and Figure B.1 shows that there is no access to the pins of the processor. It also shows that the current traces are inaccessible, and interruption of the current traces is difficult on this board. The circled inductor on Figure B.1 (b) is identified from the schematics of the power supply circuit to the CPU as shown in Figure B.2. [57], [58].




**(a): Top view of *CubieBoard2***




**(b): Bottom view of the *CubieBoard2***

**Figure B.1: Photographs of the *CubieBoard2***

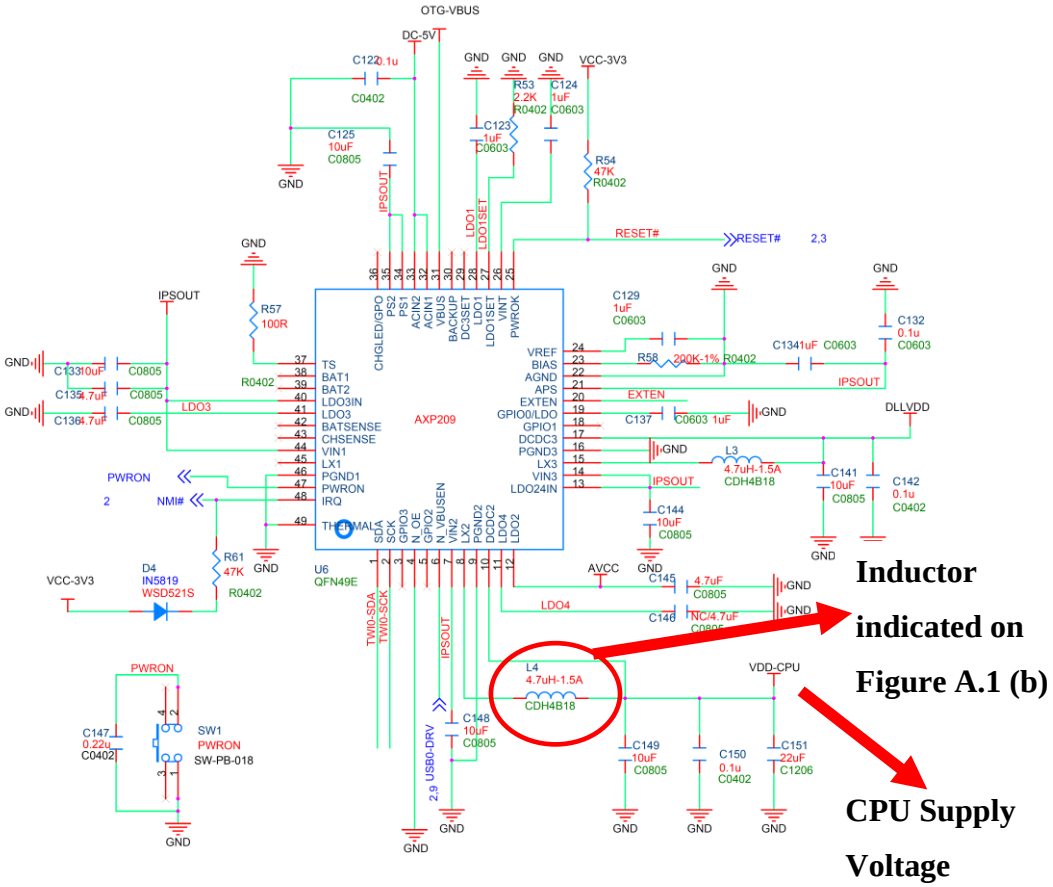



**Figure B.2: Excerpt from *Cubieboard2* schematics showing the supply voltage to the CPU from the *AXP209* PMU**

# APPENDIX C EXPERIMENTAL COMPARISON OF FILTER ICs

## C.1 Objective

The objective of this experiment was to experimentally compare the behaviour of the following:

- An active fourth order low-pass Butterworth filter designed and constructed with discrete components and op amps.
- Five fourth order low-pass Butterworth filter circuits, each constructed using a dedicated filter IC.

A simulation comparison of the filters which have available simulation models is also included.

## C.2 Procedure

The experimental procedure is as follows:

1. Design each circuit for the cut-off frequency and filter order requirements given in Chapter 4.
2. For the IC's that have available simulation models, plot the simulated frequency response to verify the designs.
3. Physically implement the circuits. Perform an AC sweep to determine the frequency response and plot the results together.
4. Perform a DC sweep to determine the DC gain of the filters. Plot the results for each case.
5. Apply a pulse-train input (representing the switch-node voltage) with increasing duty cycles. Determine and plot the DC gain for each case.
6. Analyse the results.

## C.3 Filter Circuits

The first filter circuit that was designed did not consist of a dedicated filter IC. Instead, discrete OP37 op amps [62] were used to design an active filer.

Thereafter, filter circuits were designed using the following five filter IC's:

- UAF42-*Universal Active Filter* [63]
- *LTC1562- Very Low Noise, Low Distortion Active RC Quad Universal Filter*[64]
- *LTC1563- Active RC, 4th Order Lowpass Filter* [44]
- *LTC1564- 10kHz to 150kHz Digitally Controlled Antialiasing Filter and 4-Bit P.G.A* [65]
- *LTC1569- Linear Phase, DC Accurate, Tunable, 10th Order Lowpass Filter* [66]

The above filter IC's were selected for comparison due to their cut-off frequency and roll-off specifications being applicable to this work. The filter circuit designs are discussed below.

***Active Fourth Order Low-pass Butterworth Filter***

The filter design technique in [43] was used to design a fourth order Butterworth filter using *OP37* [62] operational amplifiers. The transfer function of an ideal fourth order Butterworth filter with unity gain is given in (C.1). The filter, shown in Figure C.1 consists of two second order, low-pass, Sallen-Key topology filters with the resistor and capacitor values closest to those calculated according to (C.1) [43].

$$G(s) = \frac{1}{(1 + 0.7654s + s^2)(1 + 1.8478s + s^2)} \tag{C.1}$$

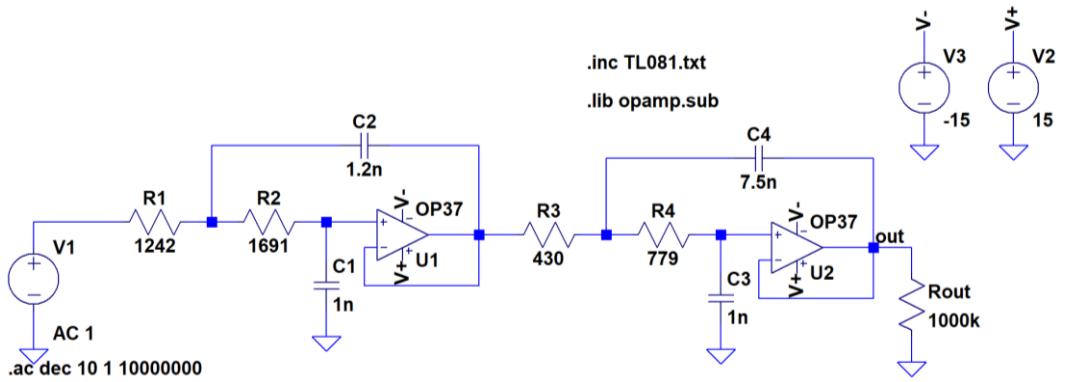



**Figure C.1: Fourth order Butterworth filter designed with OP37 op amps**

***UAF42-Universal Active Filter***

Each *UAF42AP* IC contains two first order filter op amps that can be configured with external resistors to achieve the desired gain, cut-off frequency and Q-factor [64]. The design equations given in *UAF42* datasheet were solved to design a 100 *kHz* low-pass filter with a DC gain of 1. Two IC's were used to achieve a fourth order response. The circuit diagram is shown in Figure C.2. The internal gain setting resistor was used, therefor the input of the filter is connected to pin 2. Pin 3 was left unconnected as $R_Q$ was selected as infinite to achieve a DC gain of 1.

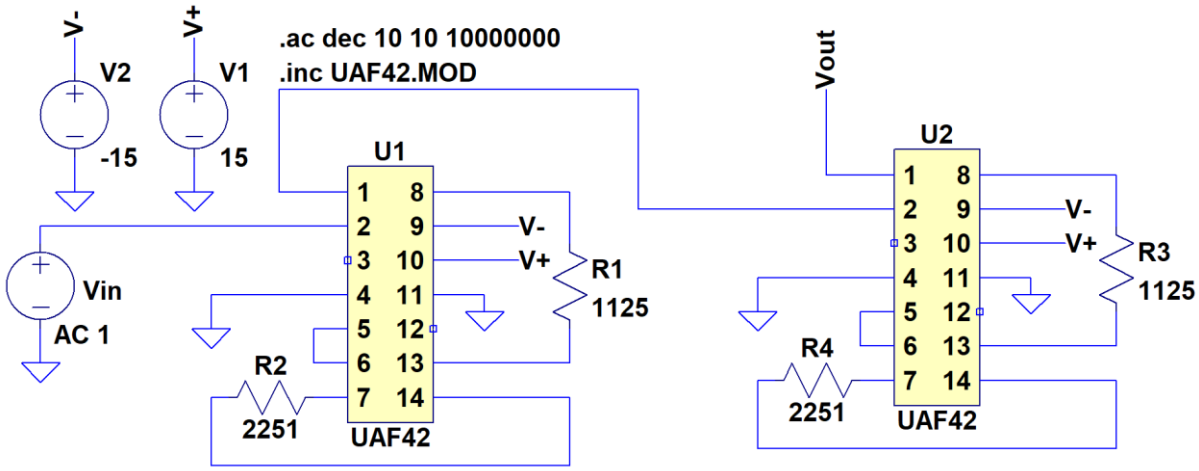



**Figure C.2: Low-pass filter circuit diagram using UAF42 filter IC.**

***LTC1562- Very Low Noise, Low Distortion Active RC Quad Universal***

The *LTC1562* contains four independent second order filter blocks [64]. Each block's response is programmed with three external resistors for gain, cut-off frequency and Q-factor. The IC was connected according to the *Typical Application* information given in the datasheet for a fourth order 100*kHz* low-pass filter with a DC gain of 1. The circuit diagram is given in Figure C.3.

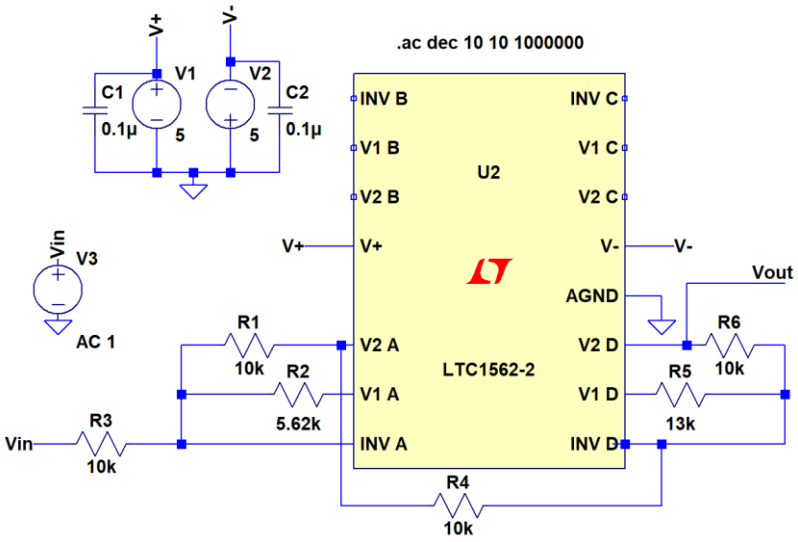



**Figure C.3: Low-pass filter circuit diagram using LTC1562 filter IC**

***LTC1563- Active RC, 4th Order Low-pass Filter***

The *LTC1563* contains two active second order filter blocks [44]. The *LTC1563*, with a single resistor value, gives a unity-gain fourth order Butterworth response. A 22 *k*Ω resistor was selected to achieve a cut-off frequency of 116 *kHz*. The circuit diagram appears in Figure C.4.

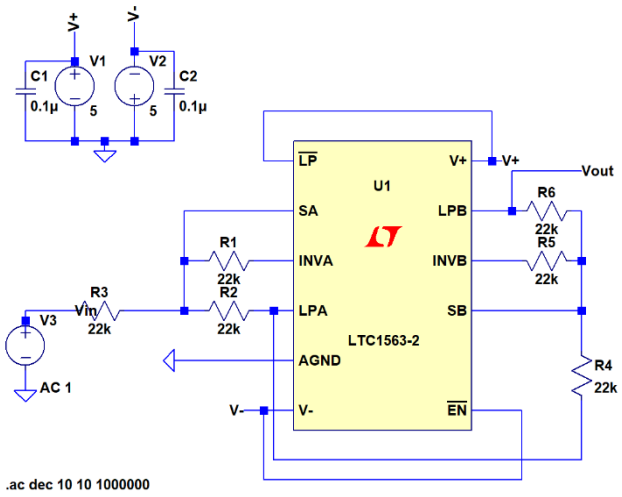



**Figure C.4: Low-pass filter circuit diagram using LTC1563 filter IC**

***LTC1564- 10kHz to 150kHz Digitally Controlled Antialiasing Filter and 4-Bit P.G.A***

The *LTC1564* is an eighth order low-pass filter with a fixed shape frequency response given in [65]. The cut-off frequency and gain are digitally programmable. No external analogue components are required. The circuit was connected as given in Figure C.5 with the gain code set to 1 *V/V* and the cut-off frequency set to 100 *kHz*.

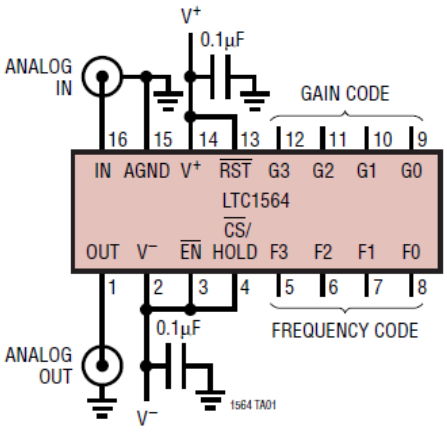



**Figure C.5: Low-pass filter circuit diagram using LTC1564 filter IC with gain code set to 0 *dB* and frequency code set to 100 *kHz***

***LTC1569- Linear Phase, DC Accurate, Tuneable, 10th Order Low-pass Filter***

The *LTC1569* is a tenth order low-pass filter with a fixed shape frequency response given in [66]. The gain is set by an external resistor which programs an internal oscillator whose frequency is divided by either 1, 4 or 16 prior to being applied to the filter network. Pin 5 determines the divider setting. Pin 5 was connected to the negative supply rail to select a divider setting of 1 and the external gain resistor was set to 12.8 *k*Ω to select a frequency of 100 *kHz* as shown in Figure C.6 [66].

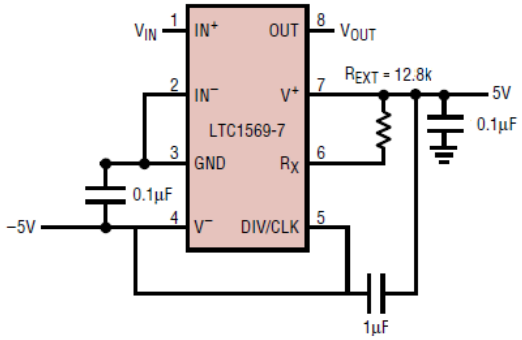



**Figure C.6: Low-pass filter circuit diagram using LTC159 filter IC**

## C.4 Results and Analysis

***Simulated Frequency Response***

The simulated frequency response of the OP37 Butterworth filter and the filter IC circuits which had available simulation models on *LTSpice* is given in Figure C.7. The simulation showed a fourth order response for all except. The results of the *LTC1562 filter IC*, however showed that the inherent Q-factor caused the cut-off frequency to be greater than the designed value. The design of all the other simulated filters were validate by the frequency response in Figure C.7.

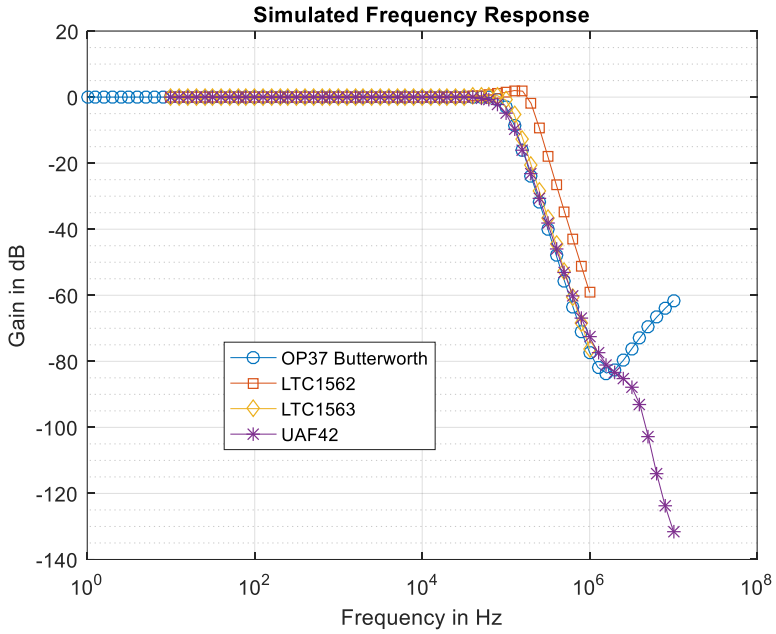



**Figure C.7: Comparison of simulated frequency responses**

***Experimental Frequency Response***

Figure C.8 shows the results from the frequency response measurements taken from each of the filters built in the lab. The frequency response of each of the filters yielded a low-pass filter response indicating that each of the filters built were indeed operating as expected in the general sense. The filter that behaved closest to the desired behaviour was the *LTC1563*. It did not exhibit an exactly fourth order roll-off but rather a 35 *dB*/decade roll-off. The Butterworth filter built with OP37 op amps and the *LTC1562* displayed a less than 3$^{rd}$ order roll-off. The other filters rolled off between third and fourth order. This includes the *LTC1569 IC* which was required to have a 10$^{th}$ order roll-off.

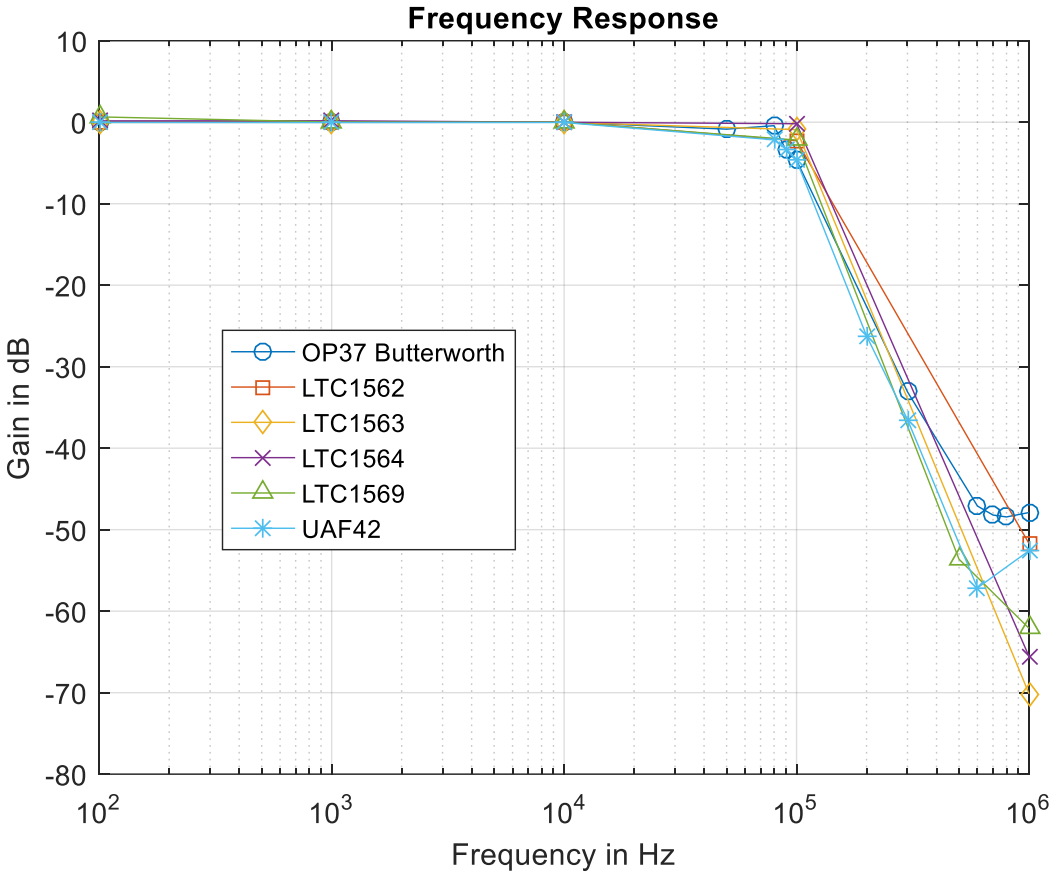



**Figure C.8: Frequency response of the filters built in lab with a 2 $V_{p\text{-}p}$ sinusoidal input**

***Experimental DC Behaviour***

Figure C.9 and Figure C.10 show the pulse train and DC sweep responses of the filters respectively. The DC gain in both cases was calculated using (C.2) where $V_{out}$ and $V_{in}$ are the DC components of the signals measured.

$$Gain_{DC} = 20 \log \left| \frac{V_{out}}{V_{in}} \right| \quad \text{(C.2)}$$

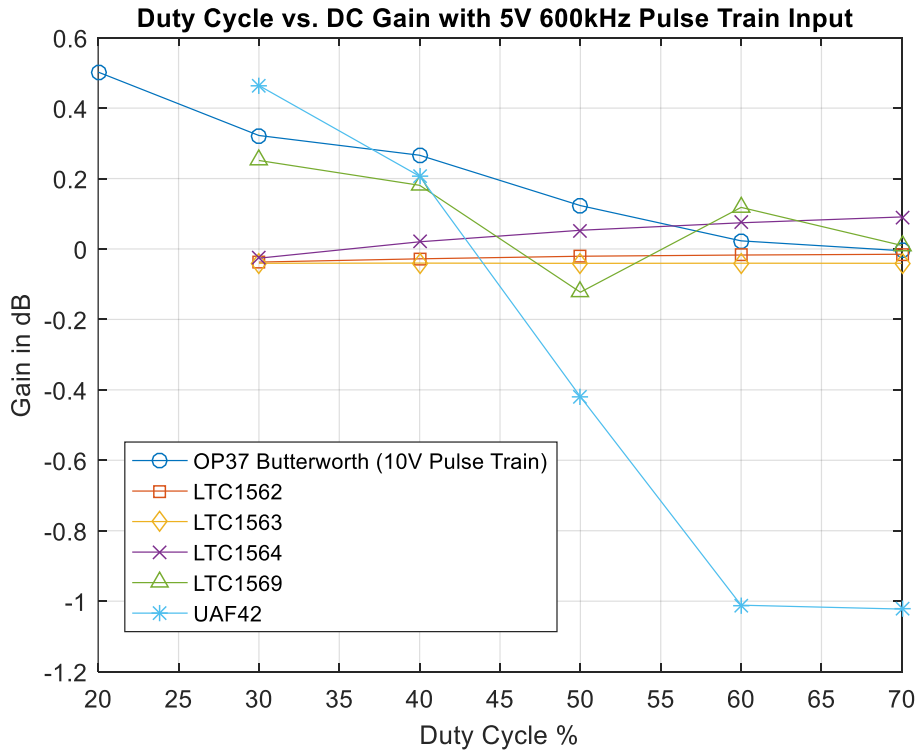



**Figure C.9: Pulse-train response of the filters**

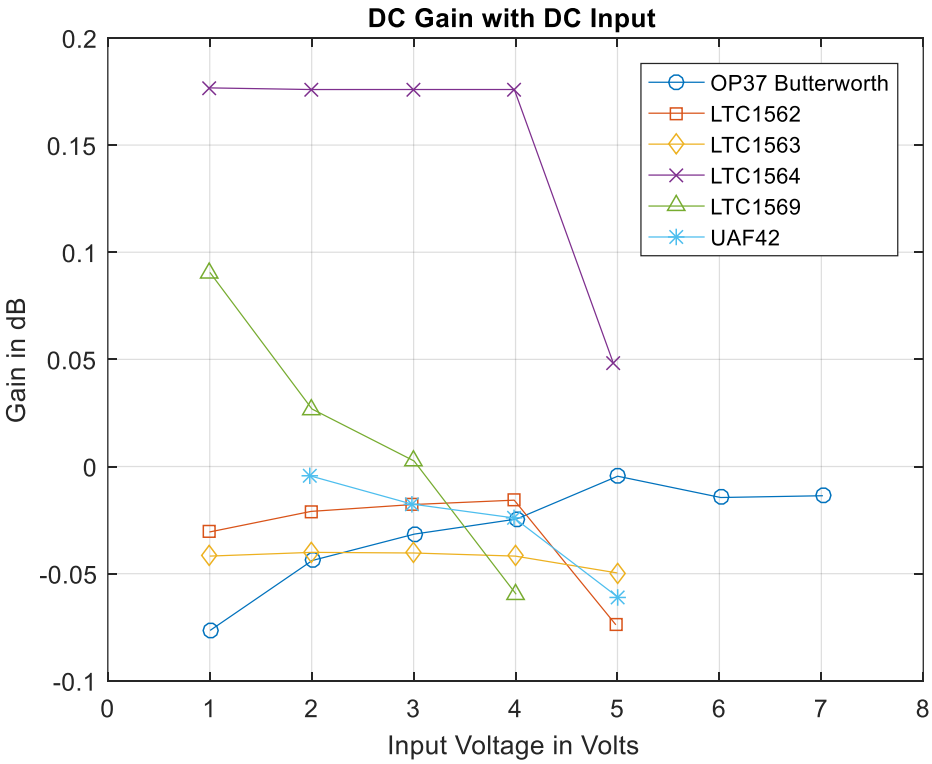



**Figure C.10: DC response of the filters**

From Figure C.9, the OP37 Butterworth filter, and the UAF42 and LTC1569 IC's showed some noise in the DC behaviour. There seemed to be an offset voltage present, causing the gain to decrease. The *LTC1562*, *LTC1563* and *LTC1564* IC's had more favourable pulse-train responses. The *LTC1563* appeared to have no offset and displayed a constant DC gain. The *LTC156* and *LTC1564* showed a small increase in gain and hence an offset voltage.

The pure DC response of the filters is given in Figure C.10. The DC responses of the *LTC1562*, *LTC1563* and *LTC1564* were approximately consistent with their pulse-train responses (except at the 5 *V* rail voltage). The remainder of the IC's DC Gain for a pure DC input vs. a pulse-train input did not agree. This could have been due to the effects of AC components of the pulse-train signal causing parasitic effects. It could have been due to noise interference in the case of sensitive IC's.

## C.5 Conclusion

In conclusion, an experimental comparison of five low-pass Butterworth filters constructed with filter IC's and a filter constructed with discrete op amps (OP37's) was performed. The same input conditions were applied to the filters and an analysis of the results was conducted. The filters constructed with dedicated filter IC's, particularly the *LTC1562*, *LTC1563* and *LTC1564* were the least susceptible to noise and parasitic effects. The *LTC1563* produced a consistent DC gain and was chosen for the filter design in Chapter 4 of this work.