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A GENERAL SOLUTION TO OPTIMISING THE DC-BUS ENERGY STORAGE REQUIREMENTS IN SINGLE PHASE INVERERS

Francois Paulus du Toit

A dissertation submitted to the Faculty of Engineering and Built Environment, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Master of Science in Engineering.

Johannesburg 2018

DECLARATION

I, Francois P. du Toit, declare that the content of this report is my own unaided work, unless otherwise stated, and that I own copyright to this. The research is being submitted for the Degree of Master of Science in engineering at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination at any other university.

Signed:_____

Francois du Toit

Date:_____ day of_____ 20 _____

Abstract

Power electronic converters that convert DC to AC, or vice versa, require an energy buffer between the AC and DC ports of the converter to compensate for the instantaneous power mismatch. Electrolytic capacitors are mostly used for these buffering applications because of the high energy density when compared to other capacitors, but unfortunately this type of capacitor also has low reliability. This dissertation proposes a general solution from a fundamental approach to solve the required capacitor power requirements on the DC-bus of an inverter. From the resulting model, an alternative active filter design technique to reduce the required capacitance of the DC-bus capacitor of a single phase inverter is presented. In this model, the minimum and maximum voltages of the capacitor can be chosen and the corresponding waveforms are calculated. An optimum region for the choice of capacitor voltage is shown to visually illustrate the trade-offs between the capacitor voltage, capacitance and converter losses. In this optimum area the reduction in capacitance is enough to allow the elimination of electrolytic capacitors, while maintaining comparable volume.

In this technique, the DC-bus capacitor is decoupled from the DC-bus to allow wide voltage variation and the power processed by the capacitor is directly controlled, instead of the bus voltage. The allowable voltage variation of the capacitor can also be selected to fit the application or traded off in favour of capacitance as chosen by the designer. This general solution is applicable to any bi-directional converter used to decouple the capacitor from the DC-Bus

Acknowledgments

I would like to gratefully thank and acknowledge everyone who helped and contributed to this Dissertation.

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1 INTRODUCTION

1.1 BACKGROUND

Power electronics is a term that describes a very wide range of technology and products that convert and control the flow of electrical energy. This energy processing capability of power electronics have become part of our everyday lives. From cell phones and tablets, to cars and power systems, almost all forms of modern technology use power electronics to function.

Renewable energy power sources also require power electronics for the generated energy to be used effectively. Solar panels generate Direct Current (DC) which has to be processed and converted to Alternating Current (AC) in order for it to be used elsewhere or in a normal household.

In these solar applications, the energy flow from the panels must be DC. Any variation will lower the overall average power output of the panels. In cases where the load is DC, like in LED applications, any variation of the DC will cause lamp flicker, which is also an undesirable effect. Thus it is very important to keep the DC power as constant as possible.

The same as in DC is applicable to AC as well. Very strict grid codes govern the requirements of grid-connected converters to carefully shape the voltage and current of the port that is connected to the AC side of the converter. The AC port of the converter must usually be able to deliverer power at a very high power factor at twice the line frequency [1]–[3].

The result of the applications mentioned above is a converter with a DC port on the input or output side and an AC port on the other side. The converter is then responsible to interface between the constant power DC port and the variable power AC port.

An instantaneous power mismatch will occur when the instantaneous power generated by the source and consumed by the load does not match. An example of this can be seen when looking at a single phase inverter or rectifier as seen in Figure 1-1. The DC side supplies or consumes constant power at the average power value, where the AC side supplies or consumes power at twice the line frequency [4]–[7].

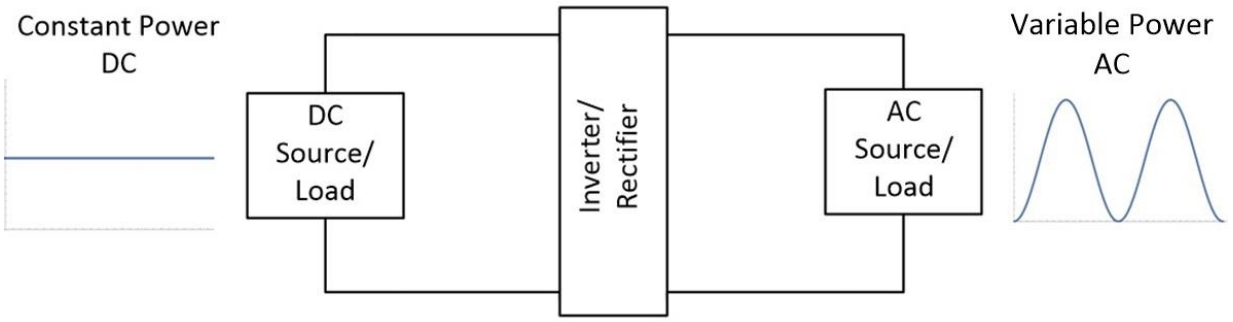


Figure 1-1: General arrangement of an AC to DC or DC to AC converter indicating power waveforms of the source and load.

The design challenge in the figure above is that the inverter or rectifier must provide internal energy storage to support the conservation of energy between the two ports.

The DC power in Figure 1-1 will take the form:

$$P_{DC} = P_{avg} \tag{1}$$

and the AC power will take the form of:

$$P_{AC}(t) = P_{avg} + P_{avg}\sin(2\omega t) \tag{2}$$

Traditionally the instantaneous power mismatch problem has been solved by introducing a large capacitor over the DC-bus to buffer the energy mismatch as seen in Figure 1-2 and Figure 1-3. This method is called passive filtering. The energy storage device will store energy in the part of the cycle where the instantaneous AC power is less than the average DC power, and then supply that stored energy in the part of the cycle where the AC power is more than the DC power. In steady state conditions the amount of energy supplied and stored by the energy storage device will be equal [4].

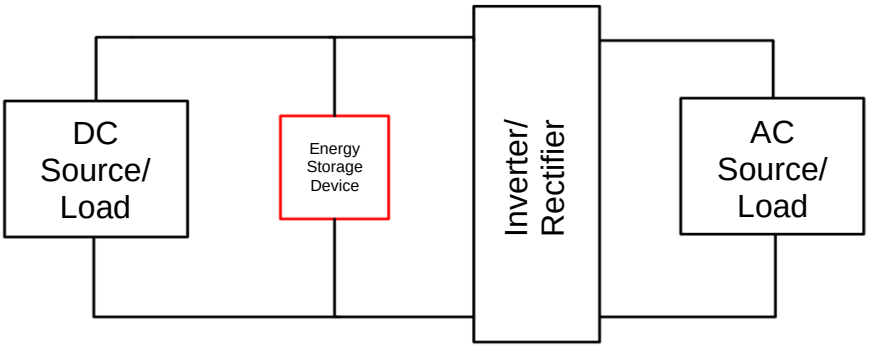


Figure 1-2: General Arrangement of an AC to DC or DC to AC converter with an energy storage device included.

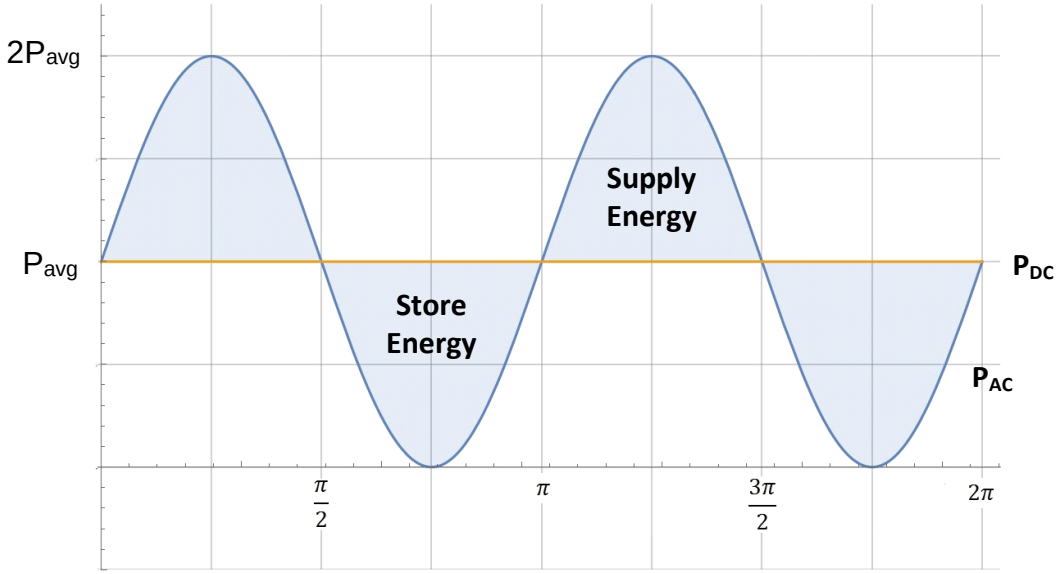


Figure 1-3: Instantaneous power mismatch between the DC and AC ports of a Single Phase Inverter and indication of where the energy storage device will store and supply energy.

Unfortunately, the whole process of absorbing and supplying power by the DC-bus capacitor creates a ripple on the DC-bus. This ripple is inversely proportional to the capacitance of the DC-bus capacitor, and directly proportional to the system power. The DC-bus ripple must also remain within strict limits in order to avoid damage to converter itself, the DC-bus capacitor and even the load or source it is connected to.

Electrolytic capacitors are commonly connected directly over DC-bus to solve this problem using passive filtering. Electrolytic capacitors are a popular, easy solution because of their very high energy density when compared to other capacitors and their simplicity compared to other complex converter solutions.

Unfortunately, electrolytic capacitors are generally unreliable. They contribute to significant amount of power electronic circuit failures, and are very susceptible to failure under thermal stress. The high equivalent series resistance value of most of the electrolytic capacitors make them heat up under loaded conditions which will in turn decrease the capacitor lifetime [8].

When electrolytic capacitors are compared to other capacitor technologies like film capacitors, the film capacitors have a much better life expectancy and much lower internal resistance, but also significantly lower energy density. This lower energy density results in approximately an order of magnitude larger volume, at the same capacitance, as an electrolytic capacitor [7], [9]. Even though a film capacitor would be a better option than an electrolytic capacitor in terms of the life of the converter, the enormous increase in volume makes the film capacitor option unviable in passive filtering.

In the case of passive filtering where the capacitor is connected directly to the DC-bus, the total amount of energy stored in the capacitor is much more than the amount of energy that is extracted and injected into the circuit in each period.

The figure below is an illustration of the utilised and unutilised energy in a DC-bus capacitor, indicating the instantaneous energy storage in the capacitor.

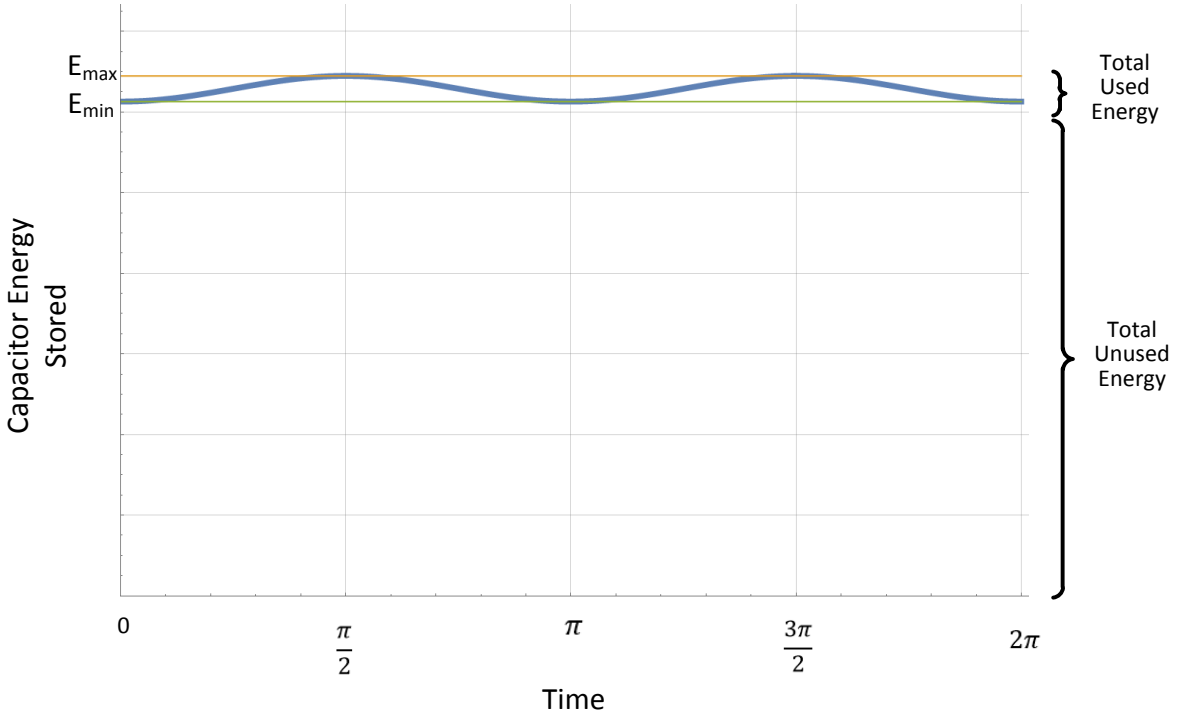


Figure 1-4: Energy waveforms of a capacitor directly connected to the DC-bus of a single phase inverter indicating which portion of the total stored energy is utilised.

If larger voltage variation of the capacitor is allowed, all this unused energy could be utilised. Unfortunately, a capacitor that is directly connected to the DC-bus cannot tolerate wide voltage variation, as this would mean that the DC-bus voltage is not constant anymore.

To overcome the constraint of small voltage variation of the energy storage capacitor, the capacitor can be decoupled from the DC-bus to allow a wider voltage variation without affecting the constant DC voltage of the bus. This allows a much smaller capacitor to be used for the same energy transfer, as a much larger part of the energy stored by the capacitor can then be utilised. This method is called active filtering, and unfortunately requires a much more complicated design, as a power electronic converter to regulate energy flow is now required as seen in Figure 1-5 below:

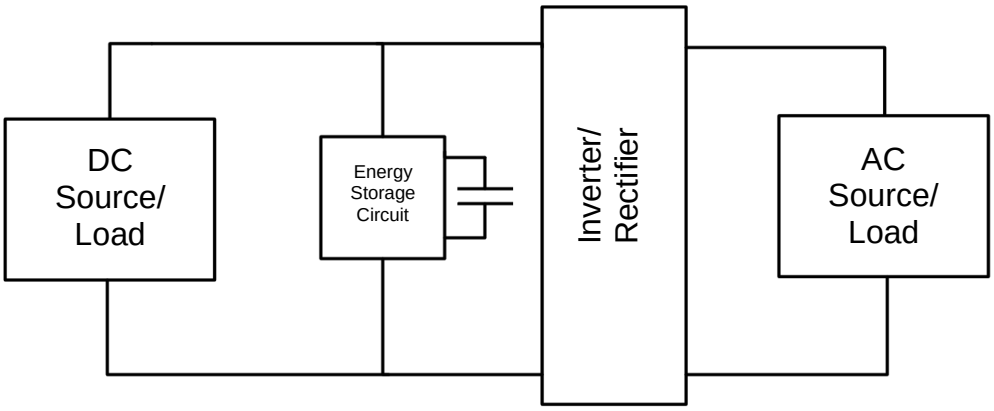


Figure 1-5: General Arrangement of an AC to DC or DC to AC converter with an energy storage circuit and energy storage device included.

This addition of a converter to regulate power flow so that the capacitor is decoupled from the DC-bus can be, but is not necessarily, counter intuitive to the total solution. A converter introduces additional complexities to the problem, like control, losses, cooling requirements and the possibility of an even larger total volume. But if these additional complexities are correctly addressed, an elegant, total solution can be implemented that has much more positive than negative side effects than a conventional electrolytic capacitor.

Several options exist to size the capacitor and optimise the energy flow of the converter. Therefore, a solution is required that incorporates both these factors, while ensuring a reliable and optimised design using other capacitor technologies like film capacitors, and still maintaining comparable volume to current solutions.

The concept of addressing the instantaneous power mismatch is applicable to most forms of power electronics that convert between AC and DC and not just in sinusoidal inverters. For the purposes of this study, only steady state sinusoidal inverters will be considered.

1.2 STRUCTURE OF DISSERTATION

This dissertation utilises a fundamental approach to ultimately propose a general solution addressing the instantaneous power mismatch in single phase inverters. A bi-directional converter is implemented to decouple the capacitor from the DC-bus. The proposed model allows the designer of the converter to accurately choose between

the associated trade-offs concerning the capacitor voltage, the converter losses and the energy storage capacitance.

Because of the fundamental approach and flexibility of the general solution, it is not only applicable to small household inverters, but also to energy mismatch problems at any high voltage systems where capacitor power is controlled by a converter.

The main contribution of this research is that it enables the designer to choose the minimum and maximum capacitor voltage, which in turn dictates the capacitance and converter losses. This capacitor voltage variation can be chosen larger by design to enable reduction of the capacitance enough to allow the possibility of the elimination of electrolytic capacitors, while limiting the converter losses so that the overall solution still has comparable volume with similar solutions that are currently being implemented worldwide.

The dissertation is organised as follows:

Chapter 1 (this chapter) introduces the problem that the research addresses as well as the research that has been done. It also gives an outline of the entire structure of the dissertation.

Chapter 2 is a review of the current available literature in the research scope. This includes a capacitor study and a study on previous work that has been done in this field.

Chapter 3 presents the general solution from a fundamental approach to allow the elimination of electrolytic capacitors. A control voltage waveform is derived from first principles to allow for DC bus ripple elimination, by controlling the capacitor power directly, instead of the DC-Bus voltage. A general solution is presented to allow the designer to use the design technique in a wide range of applications. This section also contains the contribution to the scientific community.

Chapter 4 presents a developed rudimentary loss model of the chosen bi-directional full bridge converter and discusses the attractiveness of incorporating a loss model into the general solution to allow for better informed design decisions.

Chapter 5 is an example of how the general solution in Chapter 3 can be followed to realise a working active filter. This section includes specific component selection and a comparison of the results that have been found when different solutions and points of operation are applied.

Chapter 6 concludes the dissertation. It provides a summary of what has been done, and also suggests how this research can be further developed in future projects.

2 LITERATURE REVIEW

The solution to the problem discussed in Chapter 1 is dependent on mainly two parts. These two parts are:

1. Capacitor technology
2. Capacitor energy flow management

Available literature on previous work that has been performed in these two fields of study are discussed in the sub chapters below.

2.1 CAPACITOR STUDY

2.1.1 *Introduction*

Capacitors and inductors are passive components that are used to temporarily store energy within a power electronic circuit. For a power electronic circuit to be used effectively, these components need to be optimised [10], [11].

The main focus of this dissertation is to optimise the energy flow to and from the capacitor. This can be done in one of two ways. Either by advancing the capacitor technology itself by improving properties of the materials and dielectric material it is made of, or by advancing the control techniques of the energy flow of the capacitor. This research will only consider existing capacitor technologies and will expand on the energy flow control techniques to solve the given problem.

An in depth study of the equations and physics that govern the working of a capacitor is required before the design process can start. Comprehensive studies into the basic workings of a capacitor are widely available, and the relevant details will be discussed in this chapter. The literature form this section has mainly been found in [9]–[11].

2.1.2 *Basic Capacitor Energy and Power*

Capacitors and inductors can be used for many applications in a power electronic circuits. These applications include filtering, regulation and buffering applications, but for this research, only capacitors used as an energy buffer will be discussed.

A capacitor can be used as an energy buffer interface between the DC and AC port of a single phase inverter, to accommodate the instantaneous power mismatch between the two ports.

In a buffering application, energy is periodically injected and extracted from the capacitor, usually at a far lower speed than the switching frequency of the circuit. The maximum energy that can be stored in a capacitor is given as:

$$E_{store,max} = \frac{1}{2} C V_{max}^2 \tag{3}$$

where C is the rated capacitance and V_{max} is the rated maximum voltage of the given capacitor. Because the voltage ripple is usually required to be small, the full value of $E_{store,max}$ cannot be extracted from the capacitor. To calculate the amount of energy that can be injected and extracted from the capacitor or buffer, we simply subtract the value of the energy stored at the minimum voltage of the allowable ripple from the energy stored at the maximum voltage of the ripple. This leads to:

$$\begin{aligned} E_{buff} &= E_{store,max} - E_{store,min} \\ E_{buff} &= \frac{1}{2} C V_{max}^2 - \frac{1}{2} C V_{min}^2 \end{aligned} \tag{4}$$

This equation can then be simplified to yield:

$$E_{buff} = \frac{1}{2} C (V_{max}^2 - V_{\min}^2) \tag{5}$$

In Equation (5), it can be seen how the buffered energy is dependent on the allowed voltage variation and not only the maximum voltage. Because V_{max} and $V_{\min}$ are squared, the same voltage variation at a higher voltage will be able to buffer a larger amount of energy.

The power processed by the capacitor takes the form:

$$P(t) = V_c(t) I_c(t) \tag{6}$$

where V_c is the voltage over the capacitor, and I_c is the current through the capacitor. It is also known that:

$$I_c(t) = C\frac{dV_c(t)}{dt} \tag{7}$$

where C is the capacitance. Combining these equations yields:

$$P_c(t) = V_c(t) \times C\frac{dV_c(t)}{dt} \tag{8}$$

From Equation (8) it can be seen that by controlling only the capacitor voltage, the power processed is also controlled.

Using the equations in this chapter as a basis are of great importance when designing a solution that will be able to address the problem of volume and control.

2.1.3 *Capacitor Technology Comparison*

Electrolytic capacitors are the most common capacitors used in energy buffering applications. This is mainly because of their large energy storage density when compared to film capacitors of the same volume. Unfortunately, the trade-off for higher energy storage density is also much higher equivalent series resistance, which limits the current due to overheating.

The rated RMS current of an electrolytic capacitor must be considered when designing with these type of capacitors, because they are generally lower than other types of capacitors. The thermal effect caused by the current is the main reason electrolytic capacitors are generally unreliable and prone to failure.

Electrolytic capacitors are also usually polarised, making them an attractive solution to DC-bus buffering applications, where a large capacitor is required, with no possibility of negative voltages.

Film capacitors on the other hand have much lower energy density when compared to electrolytic capacitors, but also much lower series resistance. As a result, this type of capacitor is much less susceptible to the thermal effect caused by the RMS current and, in turn, much less susceptible to general failure. The small capacitance and high current ratings make them popular when designing resonant tanks or snubber circuits.

In general, film capacitors are stable and maintain their stable performance over time and over a large temperature range, making them an attractive choice when circuit stability is crucial.

Several different types ceramic capacitors exist, based on the different types of dielectrics in the capacitor and therefore they cannot be easily classified as electrolytic or film capacitors can be. Some ceramic capacitors, like X7R capacitors, are comparable to electrolytic capacitors, as they have high energy densities, but also wide tolerances. These types of ceramic capacitors are also commonly used in buffering or filtering applications where precision is not required. NPO ceramic capacitors can be compared to film capacitors as they both have low energy densities, but high precision and stability.

A newer type of capacitor, called supercapacitors are becoming more popular in the electronic world. A supercapacitor is a very high energy density capacitor, storing ten to hundred times more energy than electrolytic capacitors of the same volume. The most significant drawbacks of a supercapacitor are very low voltage ratings and very high tolerances. They have been predicted to bridge the gap between capacitors and rechargeable batteries, having much larger energy density than capacitors, and much higher power densities that rechargeable batteries. They are most often used in applications requiring high energy and power charge and discharge cycles, rather than storing energy for long periods, like in electric vehicles.

a. Energy densities of Electrolytic Capacitors vs. Film Capacitors

A very comprehensive study of the commercially available capacitors has been done in dissertation which led to [7]. In this resource, the most applicable conclusions to this study are found in the section on highest energy storage density regions of the different capacitors.

The findings conclude that for electrolytic capacitors, the region up to 2 µF and 400 V to 500 V yields the highest energy density. This shows that electrolytic capacitors are best fitted for medium voltage applications that require high capacitance. This region for film capacitors can be found in the 400 V to 800 V and 600 µF to 1200 µF range, but still with approximately an order of magnitude lower peak energy density than electrolytic capacitors.

2.2 PREVIOUS WORK

The fundamentals of the instantaneous power mismatch and required energy buffering capabilities have been well established. The two main categories of the solutions that exist are active filters and passive filters [4], [5]. The fundamentals and working of each of these solutions are discussed below.

The problem that this research addresses has also been cited by Google and the Institute of Electrical and Electronics Engineers (IEEE) as one of the main challenges when designing an inverter in their competition. In this competition a very high energy density, 2 kW inverter had to be designed and built. Some of the methods and results from teams that entered this competition are also discussed, to account for current global research and assist in formulating a solution.

2.2.1 *Passive Filtering*

Passive filtering is the simplest method of solving the given problem. It entails a large capacitor that is connected over the DC-bus of the inverter, as seen in Figure 2-1. With an arbitrary large capacitance connected, the DC voltage and DC side current will become approximately constant. The challenge with passive filtering is that it requires a time varying voltage over the capacitor to allow energy flow, where the DC bus has to remain within certain predetermined limits [12], [13].

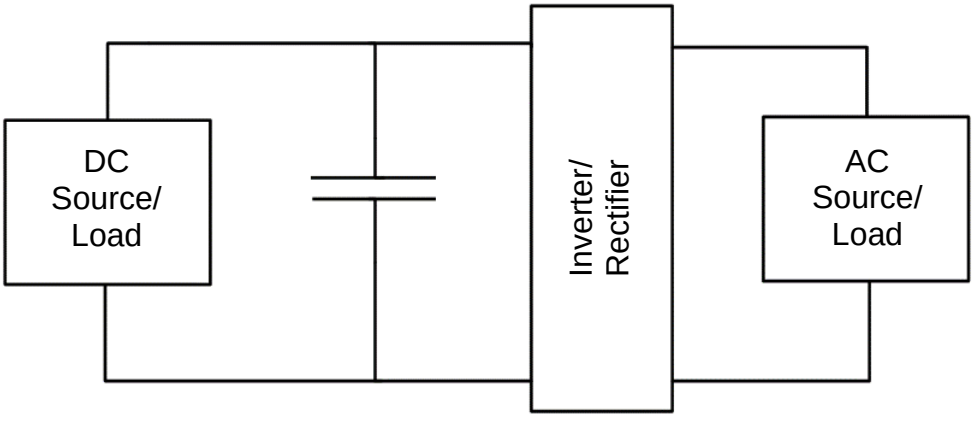


Figure 2-1: General arrangement of an inverter with a passive filter connected directly to the DC-bus.

The exact amount of energy that will have to be stored and supplied by the energy storage device can be calculated by integrating the power function for one half cycle as seen in Figure 1-3 by using Equation (9) below.

$$E_{Buff} = \int_0^{\pi} P_{AC}(t)\, dt \tag{9}$$

This equation can then be further reduced by performing the integration of the specified area in Figure 1-3 to yield:

$$E_{Buff} = \frac{P_{avg}}{\omega} \tag{10}$$

This calculated value of E_{Buff} is the energy that is injected and extracted by the passive components according to the laws of conservation of energy.

In this general arrangement of a passive filter seen in the figure above, the capacitance can be calculated to allow for a chosen voltage ripple. From [12] and [13] this equation has been found to be:

$$C = \frac{P_{avg}}{2\pi\, f\, V_{DC}\, \Delta V} \tag{11}$$

where C is the calculated required capacitance, f is the line frequency, V_{DC} is the average voltage of the DC-bus and ΔV is the allowable voltage ripple. This voltage ripple takes place at twice the line frequency. The biggest drawback in this method of filtering is that only a very small portion of the total stored energy is actually utilised, as seen in Figure 1-4.

This equation is utilised in Chapter 3 and Chapter 5 when comparisons between methods are made.

2.2.2 *Active Filtering*

As an alternative to passive filtering, researchers have turned to several different methods of active filtering to manage the double line frequency energy flow. In most of the active filter applications, the buffering capacitor is decoupled from the DC bus with a power electronic converter circuit, as seen in Figure 1-5 in Chapter 1.

In this figure, the capacitor is now decoupled from the DC bus, and therefore wide voltage variation of the capacitor can be achieved, while still maintaining very narrow voltage ripple on the DC bus. The figure displays an example of a shunt connected

capacitor reduction circuit, although several techniques exist where the circuit is series connected [6], [14].

In this configuration, a much larger part of the energy stored by the capacitor can be utilised by the circuit. This will in turn lead to a much smaller required capacitor for the same amount of energy transferred in a given cycle, and also to smaller volume of the storage capacitor.

The larger the variation of the capacitor voltage is allowed, the smaller the capacitance can be. It would be preferable to keep the capacitor voltage as close as possible to the DC bus voltage. When the conversion ratio between the input and output ports of the converter is kept as small as possible, the losses are generally kept low as the converter does not have to work as hard as when the conversion ratio is high.

When looking at the time varying term in Equation (2), namely: $P_{avg}\sin(2\omega t)$, the control of the active filter circuit must act to negate the influence of this time varying term to achieve ideal ripple cancelation. The active filter circuit can do this by processing the negative value of this term, namely: $-P_{avg}\sin(2\omega t)$, so that when summation of the powers at the DC-bus is calculated, only the constant DC power value remains.

Since the shunt connected capacitor reduction techniques are fundamentally similar to active power filters, the control techniques are also similar. The pulsating component of the current is extracted from and injected into the measured DC bus. In essence, the DC bus itself is controlled and monitored. This method may require several current and voltage measurements, and physical access to those points. Most of the active filter configurations use current injection on the DC bus [14].

In [14] and [15] a bi-directional converter has been successfully employed to address this problem by decoupling the energy storage capacitor from the DC-Bus. Current injection is used in these methods. Unfortunately, in these methods the efficiency of the system is sacrificed to maintain a low DC-bus ripple due to the losses in the converter. Other solutions in [14]–[16] incorporate the energy buffering

stage with the power conversion stage of the inverter to lower the total losses of the inverter system.

References [7] and [9] present a stacked switch capacitor energy buffer to address this problem. This method entails switching several smaller capacitors in series and parallel at different times to reduce the DC-Bus ripple. Even though this method successfully reduces the DC-bus ripple, the ripple is still relatively large and complicated control has to be incorporated to achieve the desired results.

A promising alternative active filter configuration is discussed in [4]–[6]. In this configuration, a third port, in addition to the DC and AC ports, is introduced to manage the ripple power of the inverter. The ripple power is controlled directly to achieve the desired double frequency power value and therefore the voltage variation of the capacitor can be large by design. The greatest advantage of this method is that the minimum possible capacitance for a given voltage can be selected as energy storage is addressed directly.

Integration of the graph of the mismatch between the DC and AC power in Figure 1-3 has been done in Equation (9) and Equation (10). This calculated value governs the requirements of the direct control of the capacitor power. In contrast to other active filters, direct control of the ripple power implies control over the capacitor current and voltage as opposed to current injection into the DC bus.

To calculate the new relationship between capacitance, voltage and output power, a fundamental approach was taken by [5]. This method of calculating the required capacitor voltage waveform to ensure the correct power waveform is discussed below, as it realises promising results. The capacitor voltage is given as:

$$v_C(t) = V_C \cos(\omega t + \theta) \tag{12}$$

where V_C is the capacitor peak voltage, θ is the phase angle with respect to the output voltage and ω is the radian frequency of the inverter output voltage. Since it is known that the capacitor current is equal to $C\,dv/dt$, the instantaneous power processed by the capacitor can be calculated as seen below:

$$P_C(t) = V_C \cos(\omega t + \theta) C \frac{d}{dt}[V_C \cos(\omega t + \theta)]$$

$$= -\omega C {V_C}^2 \cos(\omega t + \theta) \sin(\omega t + \theta) \quad (13)$$

$$= -\frac{\omega C {V_C}^2}{2} \sin(2\omega t + 2\theta)$$

The assumption is made that the capacitor voltage can be controlled so that the power flow in the capacitor cancels out the double frequency term in the output power so that:

$$-\frac{\omega C {V_C}^2}{2} \sin(2\omega t + 2\theta) = P_{avg} \cos(\omega t - \phi) \quad (14)$$

where ϕ is output current phase shift.

The magnitude of the inverter double frequency ripple power and the capacitor power will be the same if:

$$\frac{\omega C {V_C}^2}{2} = P_{avg} \quad (15)$$

Thus, the capacitance and the peak voltage can be selected so that the magnitude of the capacitor power equals the inverter double frequency output power. Since the ripple port is decoupled from both the DC and AC voltages, the value of the peak capacitor voltage can be chosen high, so that the value of the capacitance is very low for a given application. Even though the choice of the capacitor value can be made arbitrarily small, the energy stored is not arbitrary and is still governed by the minimum required energy in Equation (9).

In this method, only the maximum capacitor voltage can be selected. Even though this allows the minimum possible capacitance to be utilised, it also means that the minimum capacitor voltage is required to be zero volt. A very large amount of stress then has to be carried by the converter to achieve the very high conversion ratios

between the input and output voltage, increasing the converter losses and complicating the control.

This configuration also enables reactive power to be introduced into the system if desired and if the output bridge can support it.

The value of the capacitance calculated in Equation (15) is the value of the minimum capacitance that stores exactly the energy required to satisfy (9), but a smaller capacitance value could be chosen by the designer if ideal ripple cancelation is not required.

2.2.3 *IEEE Inverter Competition*

The Little Box Challenge was a competition hosted by Google and the IEEE Power Electronic Society in 2014, and the winners were announced in 2016. The goal of this competition was to build a 2 kW inverter, but about ten times smaller than the current leading technologies.

In this challenge, four main reasons why this goal was not currently possible is presented in the problem statement of the competition. One of the problems was the DC-bus filter as presented in the introduction. All of the teams that made it to the final had to present a short document of how they solved the problem. Even though they are not academic journals, it has been decided it would be very advantageous to see how the current world leading technology solved the problem, and to be able to compare the results of this research and the results of some of the top qualifying teams.

All of the teams used some form of active filter to solve this problem. It seems that most of the solutions incorporate very complicated control to manage the energy flow and the transition conditions.

Only vague descriptions of how the DC voltage ripple was cancelled can be found in most of the documentation, and where the capacitance has been stated, it was in the range of hundreds of microfarads.

To be able to view this capacitance in perspective, using Equation (11) results in a required capacitance of 1.326 mF to be able to keep the voltage ripple within allowable

margins when passive filtering is used. This results in an order of magnitude smaller capacitance in most of the methods used in the competition.

3 GENERAL DC FILTER CAPACITOR POWER MANAGEMENT

In the literature study, several different approaches were researched to solve the problem of instantaneous power mismatch. It is seen that all of these methods create the same capacitor power waveform for a given inverter power waveform, even if the voltage or current ripple varies. This is due to the law of conservation of energy, given as:

$$P_{in}(t) = P_{out}(t) \tag{16}$$

which must hold true under ideal conditions. It is important to note that the power that a capacitor processes is primarily governed by the laws of conservation of energy, and voltage and current ripple will in turn create the required power waveform.

This dissertation presents a fundamental approach to define the DC filter capacitor power waveform in power electronic devices, focussing on the case study of single phase inverters, while strictly adhering to the laws of conservation of energy.

3.1 FUNDAMENTAL APPROACH TO SOLVING CAPACITOR POWER

In an isolated system, the input and output power of the inverter will be equal. This explains why a large ripple will be created on the DC side of the inverter when no energy buffer is implemented, given that the output side has been defined to be AC. If the AC side of the inverter has a defined power waveform, the exact input power waveform can be defined to ensure that $P_{in}(t) = P_{out}(t)$.

For an inverter in the configuration of Figure 1-2, for $P_{in}(t)$ to be equal to $P_{out}(t)$, the equation:

$$P_{DC}(t) = P_{AC}(t) \tag{17}$$

must hold true, as well as the equations from Chapter 1 below, where $P_{DC}(t)$ is the power waveform on the DC side of the inverter and $P_{AC}(t)$ is the power waveform on the AC side of the inverter. It can also be shown that:

$$P_{DC}(t) = P_{avg} + P_C(t) \tag{18}$$

and:

$$P_{AC}(t) = P_{avg} + P_{avg}\sin(2\omega t - \varphi) \tag{19}$$

where P_{avg} is the average power of the inverter and P_C is the power processed by the capacitor. Substituting Equations (18) and (19) back into Equation (17) yields the waveform of the power processed by the capacitor as:

$$P_C(t) = P_{avg}\sin(2\omega t - \varphi) \tag{20}$$

It is important to note that Equation (20) must hold true under passive and active filtering conditions.

3.1.1 *Capacitor Power Evaluation*

The following section is an analysis of the power evaluation of a capacitor. A more fundamental approach than [4] is taken and a different result is yielded.

The basic power processed by a capacitor is given as:

$$P_C(t) = V_C(t) \times C\frac{d}{dt}[V_C(t)] \tag{21}$$

where $P_c(t)$ is the power processed by the capacitor, $V_c(\mathrm{t})$ is the time varying capacitor voltage and C is the capacitance. As stated above, $P_c(t)$ must take the following from to adhere to the laws of conservation of energy:

$$P_C(t) = P_{avg}\sin(2\omega t) \tag{22}$$

where P_{avg} is the average power of the inverter. This value is assumed to be constant in this study, as only a single point of operation of the inverter is evaluated.

Equation (5) can then be rearranged to determine the value of C to yield the equation:

$$C_{min} = \frac{E_{Buff}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)} \tag{23}$$

where C_{min} is the minimum required capacitance to buffer the value E_{Buff}. The values of V_{max} and V_{min} , can now be chosen by the designer, but this decision will be discussed later on.

From Equation (21), only the time varying term $V_c(t)$ still needs to be evaluated. This can be done by equating Equation (21) and (22) and then evaluating the value of $V_c(\mathrm{t})$ in the time domain to derive the required capacitor voltage waveform, to eliminate the ripple. This derivation and the resulting equation can then be seen below:

$$P_{avg}\sin(2\omega t) = V_c(\mathrm{t}) \times C\frac{d}{dt}[V_c(t)]$$

$$\int P_{avg}\sin(2\omega t)\,dt = \int V_c(\mathrm{t}) \times C\frac{d}{dt}[V_c(t)]dt$$

$$P_{avg}\int \sin(2\omega t)\,dt = C\int V_c(\mathrm{t})\;dV_c(t) \tag{24}$$

$$\frac{-P_{avg}}{2\omega}\cos(2\omega t) + E = C\frac{V_c(\mathrm{t})^2}{2} + F$$

$$V_c(\mathrm{t}) = \sqrt{\frac{-P_{avg}}{C\omega}\cos(2\omega t) + G}$$

Before the value of the constant G can be calculated, the influence of the chosen values of V_{min} and V_{max} has to be introduced into Equation (24). This can be done by incorporating Equation (10) into Equation (23) which yields:

$$C = \frac{\frac{P_{avg}}{\omega}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)} \tag{25}$$

which can be rearranged to yield:

$$\frac{P_{avg}}{C\omega} = \frac{{V_{max}}^2 - {V_{min}}^2}{2} \tag{26}$$

From Equation (26) it can be seen that the constant term in Equation (24) can be substituted to incorporate the chosen voltage values into the required capacitor voltage waveform. This is where the evaluation of the constant G, in Equation (24), can begin. It is suspected that the constant G will take a similar form to that of Equation (26), and through substitution and evaluation of a function where V_{min} is chosen as 0 V, G is calculated to take the form:

$$G = \frac{{V_{max}}^2 + {V_{min}}^2}{2} \tag{27}$$

Substituting Equation (27) back into Equation (24) and reducing to allow for the least number of variables leads to the following:

$$V_c(\mathrm{t}) = \sqrt{-\frac{{V_{max}}^2 - {V_{min}}^2}{2}\cos(2\omega t) + \frac{{V_{max}}^2 + {V_{min}}^2}{2}}$$

$$V_c(\mathrm{t}) = \sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)} \tag{28}$$

It can now be seen from Equation (25) and (28), that only P_{avg}, V_{max} and V_{min} have to be chosen to derive the required capacitor voltage waveform.

In Equation (15) from the literature study, the voltage that can be chosen is the maximum capacitor voltage to ensure the required power waveform, with the assumption of a minimum capacitor voltage of 0 V. Equation (28) now enables the designer to choose not only the maximum, but also the minimum capacitor voltage, while still ensuring the required power waveform.

The corresponding current can then be derived by inserting Equation (28) in Equation (7), yielding the following:

$$I_c(t) = C\frac{d}{dt}\sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)}$$

$$I_c(t) = \frac{C\omega\left({V_{max}}^2 - {V_{min}}^2\right)\sin(2\omega t)}{2\sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)}} \quad (29)$$

To ensure that the derived equations are correct, we can calculate the power processed by the capacitor when the above mentioned capacitor voltage and current are multiplied. The resulting equations are as follows:

$$P_C(t) = V_c(t)I_c(t)$$

$$P_C(t) = \sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)} \times \frac{C\omega\left({V_{max}}^2 - {V_{min}}^2\right)\sin(2\omega t)}{2\sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)}} \quad (30)$$

$$P_C(t) = \frac{1}{2}\left({V_{max}}^2 - {V_{min}}^2\right)C\omega\sin(2\omega t)$$

Substituting Equation (26) back into Equation (30) yields:

$$P_c(t) = P_{avg}\sin(2\omega t) \quad (31)$$

which is what is expected. This method of deriving the required capacitor voltage to create a predetermined capacitor power waveform, is not only applicable in cases where the capacitor power takes the form of a sine wave. Any predetermined capacitor power waveform can be substituted in and a required voltage waveform can be derived.

3.1.2 *Application to Passive Filtering*

The design of a passive filter to correspond to a chosen capacitor voltage range has been derived. Because the model above is based on fundamental equations, it must

be applicable to passive filtering, as well as active filtering where the capacitor is decoupled from the DC bus.

Equation (11) illustrates the required capacitance to limit the voltage to a chosen ripple, like Equation (25) does for the fundamental approach. When the values of V_{DC} and ΔV are re-evaluated to express them in terms of V_{min} and V_{max}, they are found to be:

$$V_{DC} = \frac{V_{max} + V_{min}}{2} \tag{32}$$

and:

$$\Delta V = V_{max} - V_{min} \tag{33}$$

Equation (32) and Equation (33) can then be substituted back into Equation (11) to yield:

$$C = \frac{P_{avg}}{2\pi f \left(\frac{V_{max} + V_{min}}{2}\right)(V_{max} - V_{min})} \tag{34}$$

and Equation (34) can be rearranged to yield:

$$C = \frac{\frac{P_{avg}}{\omega}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)} \tag{35}$$

which is the same as Equation (25). From this comparison it can be seen that the capacitance sizing for passive filtering and active filtering is fundamentally the same, just from different approaches. In passive filtering, the capacitor power will naturally take the form described in Equation (20).

To further ensure that the model is applicable to passive filtering, an example is shown below.

If ΔV is chosen to be 10% of V_{DC}, the following equations can be derived:

$$V_{max} = 1.05V_{DC} \tag{36}$$

$$V_{min} = 0.95V_{DC} \tag{37}$$

The equations above can then be substituted back into Equation (35) to calculate the capacitance in terms of V_{DC}, which yields:

$$C = \frac{10P_{avg}}{{V_{DC}}^2\omega} \tag{38}$$

If the DC bus capacitor of the single phase inverter is chosen as the value in Equation (38), then the values of Equation (36) and Equation (37) can also be substituted back into Equation (28) to yield:

$$V_c(\mathrm{t}) = \sqrt{-\frac{1}{2}((1.05V_{DC})^2 - (0.95V_{DC})^2)\cos(2\omega t) + \frac{1}{2}((1.05V_{DC})^2 + (0.95V_{DC})^2)} \tag{39}$$

$$V_c(\mathrm{t}) = \sqrt{-0.1{V_{DC}}^2\cos(2\omega t) + 0.1{V_{DC}}^2}$$

From Equation (39) the capacitor current and the power can also be calculated for validation purposes.

$$I_c(t) = C\frac{d}{dt}\sqrt{-0.1{V_{DC}}^2\cos(2\omega t) + 0.1{V_{DC}}^2}$$

$$I_c(t) = \frac{0.1C\omega\,{V_{DC}}^2\sin(2\omega t)}{\sqrt{-0.1{V_{DC}}^2\cos(2\omega t) + 0.1{V_{DC}}^2}} \tag{40}$$

$$P_C(t) = V_c(t)I_c(t)$$

$$P_C(t) = \sqrt{-0.1{V_{DC}}^2\cos(2\omega t) + 0.1{V_{DC}}^2} \times \frac{0.1C\omega\ {V_{DC}}^2\sin(2\omega t)}{\sqrt{-0.1{V_{DC}}^2\cos(2\omega t) + 0.1{V_{DC}}^2}} \tag{41}$$

$$P_C(t) = 0.1{V_{DC}}^2 C\omega\ \sin(2\omega t)$$

Substituting Equation (38) back into Equation (41), yields:

$$P_c(t) = P_{avg}\sin(2\omega t) \tag{42}$$

which is also expected. The corresponding voltage, current and power waveforms can be seen in Figure 3-1, Figure 3-2 and Figure 3-3 below:

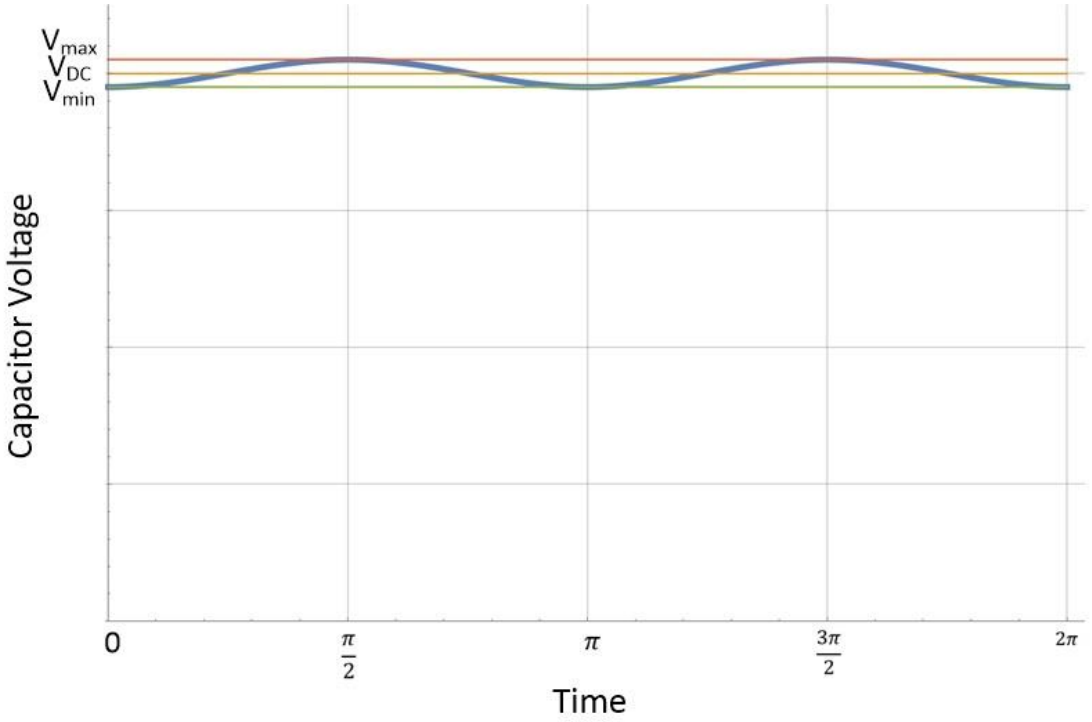


Figure 3-1: Passive filtering capacitor voltage waveform as a function of time.

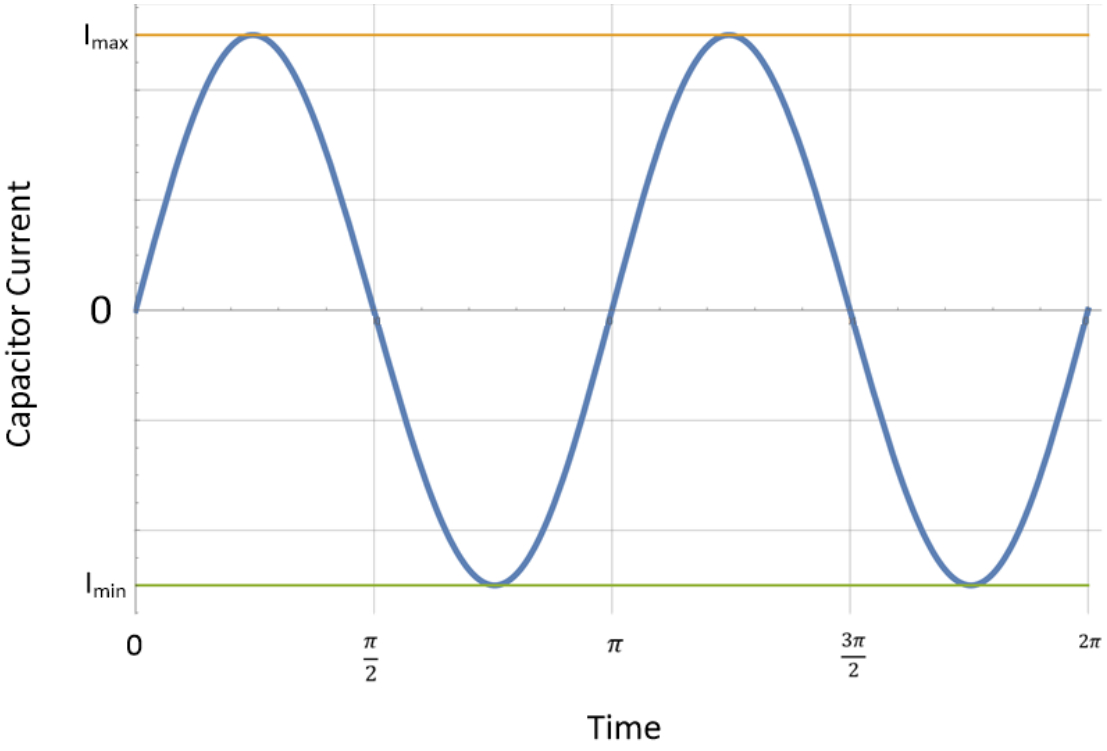


Figure 3-2: Passive filtering capacitor current waveform as a function of time.

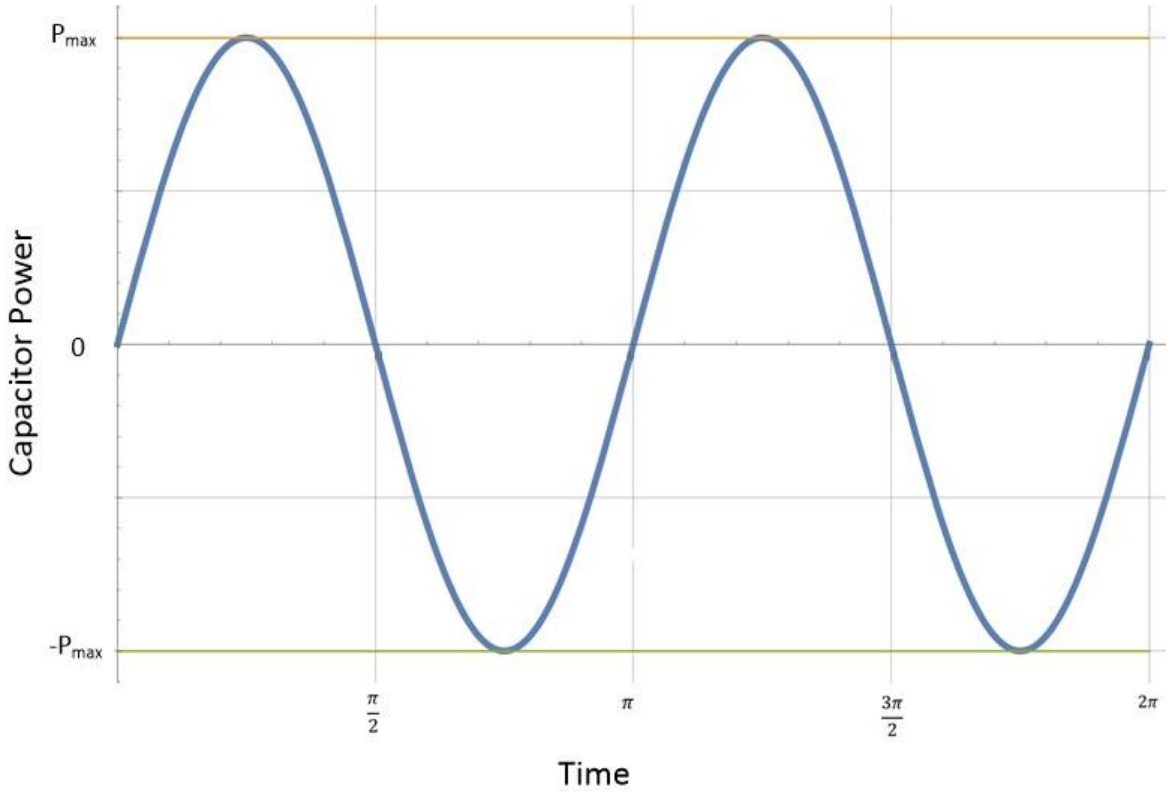


Figure 3-3: Passive filtering capacitor power waveform as a function of time.

The derived equations and waveforms above are the exact waveforms, not an estimation, which the capacitor will naturally create to ensure that the laws of conservation of energy holds.

The fundamental approach to calculating capacitor power has been validated in the case of passive filtering. It must be noted that even though the waves of the voltage and current look like they assume the form of a purely sine wave, from the equations it can be seen that this is not true. Using a Fast Fourier Transform (FFT) tool, the Total Harmonic Distortion (THD) of the voltage wave has been found to be 3%.

3.1.3 *Application to Active Filtering*

As stated above, all capacitor power waveforms must take the form of a sine wave if the output power has been defined as such as seen in the literature review. In essence, direct power control and active filtering are the same thing, although different parameters are controlled.

The concept of direct power control entails controlling the power processed by the capacitor directly, instead of injecting current into the DC bus to regulate the DC bus voltage and current, as in the most cases of active filtering. The greatest advantage of

this approach is that it enables the minimum possible capacitance to be used. The control system of direct capacitor power control will try to create the negative part of the time varying term in the AC power, as seen in Equation (2), to cancel the term and create ideal ripple cancelation in the DC bus.

This approach can be seen in [4], where a Ripple Port is implemented to create an almost ripple free DC bus and proves that this concept can be further explored. The proposed solution in [4] suggests that the power processed by the capacitor can be controlled by regulating only the capacitor voltage and the following equation was derived to relate the capacitor power to capacitor voltage, as seen in Chapter 2:

$$P_c(t) = -\frac{\omega C {V_c}^2}{2}\sin(2\omega t + 2\theta) \tag{43}$$

From this equation the maximum voltage of the capacitor can be chosen, where after the minimum capacitance can be calculated. Unfortunately, the findings of this approach conclude that the capacitor voltage must be brought down to 0 V, an infinite step-down ratio. In this method, it is very hard to achieve ideal ripple cancelation, as very high and unnecessary stress will be put on the converter in order to achieve the very high conversion ratios. This will in turn create very high losses in the converter and possibly damage components.

To ensure that the fundamental approach as seen in Chapter 3.1 is applicable to passive filters as well as active filters, the same approach is taken, but for a scenario where the capacitor is decoupled from the DC bus. Equation (28), Equation (29) and Equation (31) are used. The minimum and maximum voltage can also be chosen now, together with the voltage ripple.

In the following section, a comparison is made between when V_{min} is chosen as 0 V as in [4], and when V_{min} is chosen as $\frac{V_{max}}{2}$. This is done to demonstrate the influence the voltage choice has on the subsequent voltage, current and power waveforms and required calculated capacitance of the capacitor, for a constant value of P_{avg} and V_{max}.

In Figure 3-4, Figure 3-5 and Figure 3-6 below the associated waveforms can be seen.

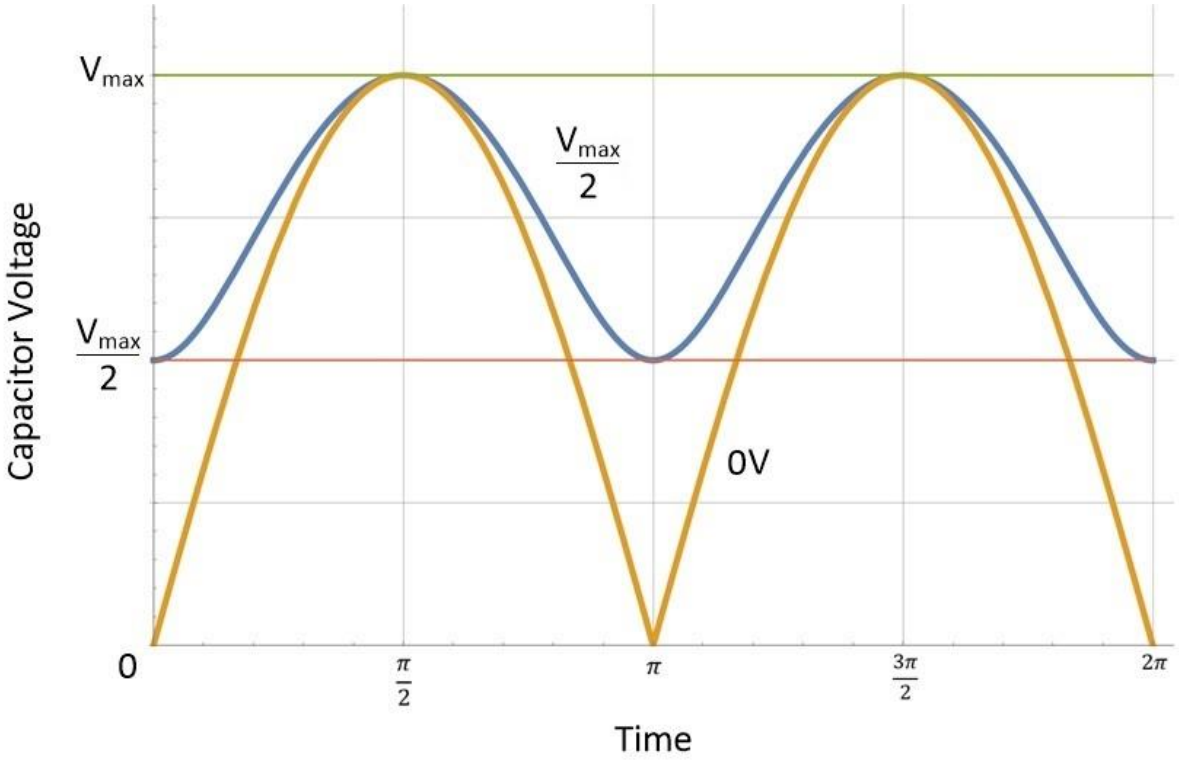


Figure 3-4: Active filtering capacitor voltage waveforms comparison between a minimum capacitor voltage of 0 V and $\frac{V_{max}}{2}$.

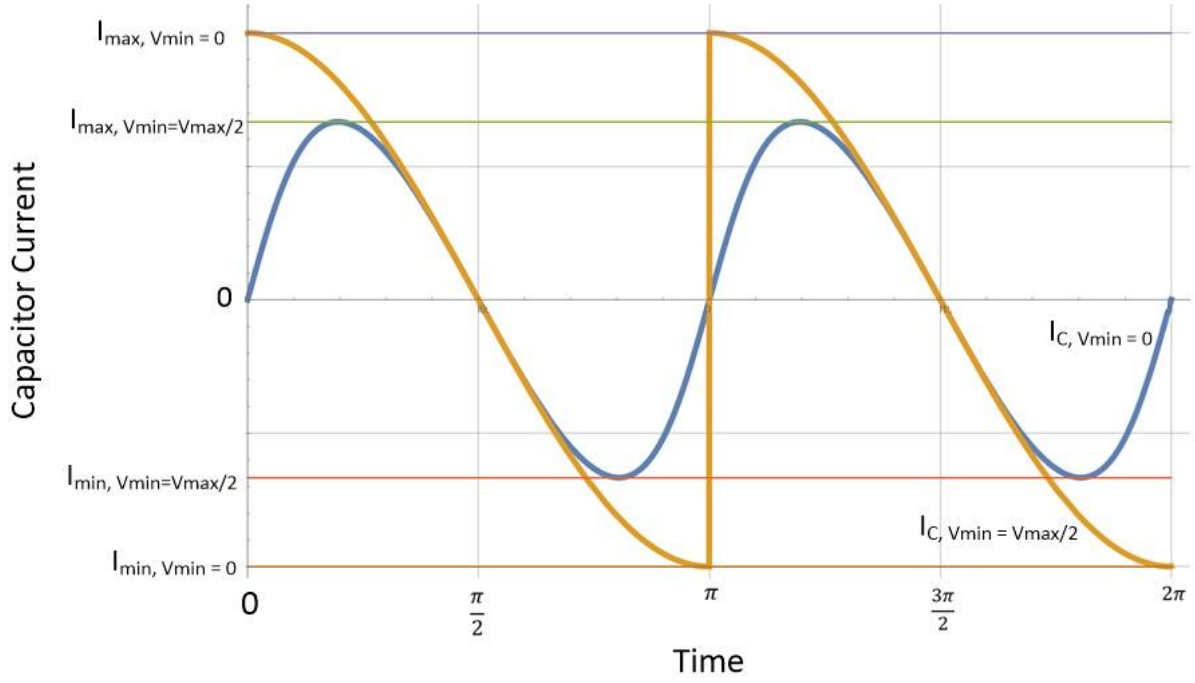


Figure 3-5: Active filter capacitor current waveforms comparison between a minimum capacitor voltage of 0 V and $\frac{V_{max}}{2}$**.**

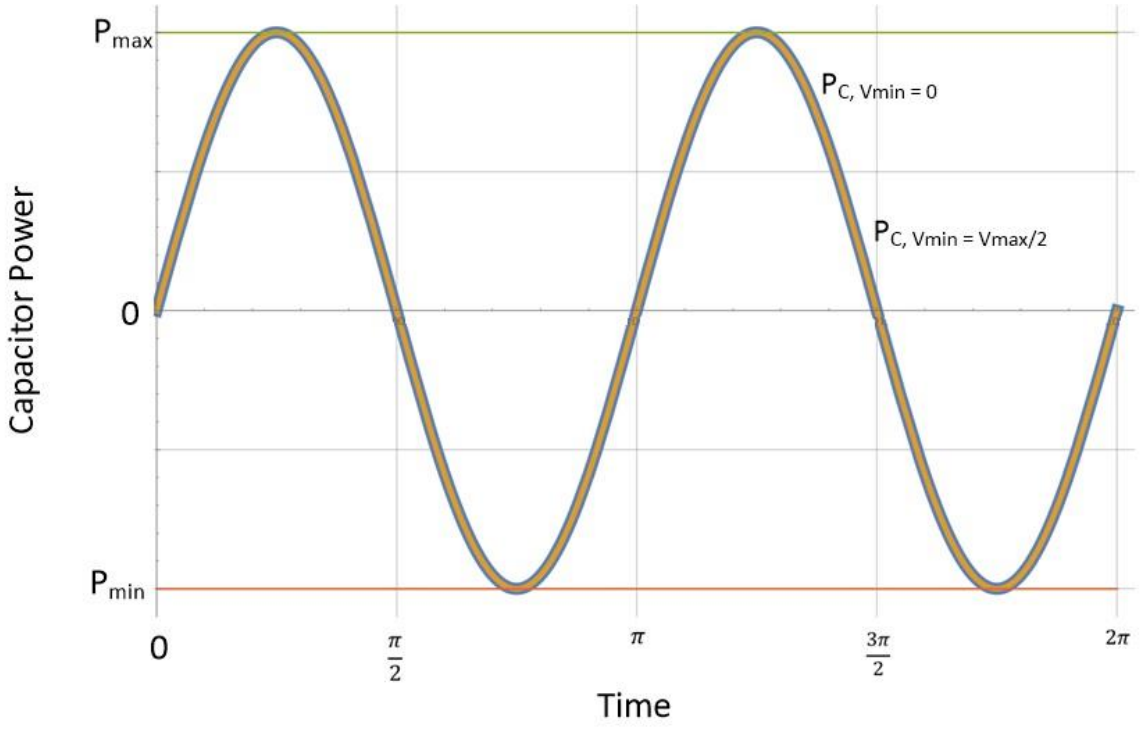


Figure 3-6: Active filtering capacitor power waveform comparison between a minimum capacitor voltage of 0 V and $\frac{V_{max}}{2}$.

The power processed by the capacitor takes the form of a perfect sine wave. This model is a validation of the mathematics that the minimum value of the capacitor does not have to be forced down to 0 V to achieve ideal ripple cancelation.

From these waveforms several advantages can be seen when the voltage is not forced down to zero. In the capacitor current waveforms, the peak current is approximately 0.7 times the peak value of the compared current, placing less strain on the components. Also, when minimum voltage is chosen as 0V, the current has to change direction instantaneously, which is not practically possible, due to the inductive components.

Generally, the waveforms of the method where the voltage is not forced down to zero are much easier to achieve practically, with the only drawback being a slightly larger capacitor. This trade-off is discussed in full later on in the report.

3.2 CHOICE OF VOLTAGE VARIATION

The preliminary results from Chapter 3.1.3 have been seen to be a very promising alternative method of addressing the problem of instantaneous power mismatch. With this method, the minimum and maximum capacitor voltages can be chosen more freely by the designer. Three important influences that the designer has to keep in mind when deciding on these voltages have been identified and are as follows:

1. Energy storage capacitance
2. Decoupling converter losses
3. Decoupling converter component ratings and stress

The three influences are discussed in the section below.

3.2.1 *Capacitance*

It is known that the higher the voltage variation over the energy storage capacitor, the smaller the capacitance will be in turn. Also, the same voltage variation at a higher voltage will yield a smaller capacitance compared to the same voltage variation at a lower voltage.

In Chapter 3.1.3 it was explained that not forcing the minimum voltage down to zero has several advantages. When the assumption is made that the maximum voltage is chosen as a constant V_{max}, an equation can be derived to show how the choice of the minimum voltage will influence the capacitance. In the derivation below, the assumption is also made that the required power processed by the capacitor remains constant.

This relationship can be calculated when we consider Equation (23) for a case where the minimum capacitor voltage is chosen as zero volt and compare it to a case where the minimum voltage is chosen as a variable V_{min} as seen in the equations below:

Let:

$$C_{min,V_{min}=0} = \frac{E_{Buff}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)}$$

$$C_{min,V_{min}=0} = \frac{2E_{Buff}}{{V_{max}}^2} \tag{44}$$

and let:

$$C_{min,V_{min}=V_{min}} = \frac{E_{Buff}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)} \tag{45}$$

In both these cases the value of E_{Buff} is the same because the required power to be processed by the capacitor remains the same.

When the minimum capacitor voltage is chosen as zero volt, the corresponding calculated capacitance will be the minimum possible capacitance to buffer the value of E_{Buff}. The relationship between the capacitance and minimum capacitor voltage can then be expressed as a factor of the minimum possible capacitance against the minimum capacitor voltage, as a factor of the maximum capacitor voltage. This derivation and resulting plot can be seen below:

$$\frac{C_{min,V_{min}=V_{min}}}{C_{min,V_{min}=0}} = \frac{\frac{E_{Buff}}{\left(\frac{1}{2}{V_{max}}^2\right) - \left(\frac{1}{2}{V_{min}}^2\right)}}{\frac{2E_{Buff}}{{V_{max}}^2}}$$

$$\frac{C_{min,V_{min}=V_{min}}}{C_{min,V_{min}=0}} = \frac{1}{2(\frac{1}{2} - \frac{{V_{min}}^2}{2})} \tag{46}$$

A plot of the above equation can be seen in Figure 3-7:

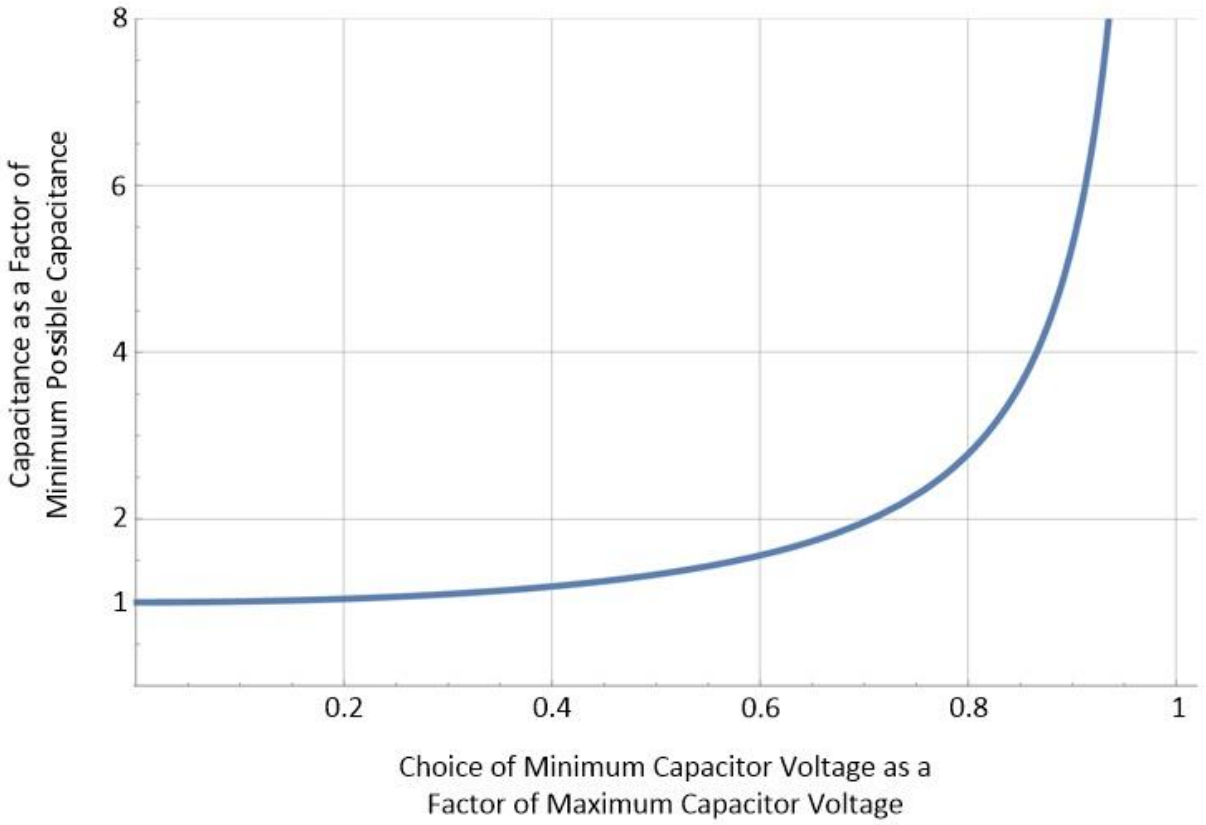


Figure 3-7: Trade-off illustration between the choice of minimum voltage as a factor of the maximum voltage and the capacitance as a factor of minimum possible capacitance.

From the equation and graph above the designer can now decide on the trade-off between the chosen minimum voltage or the larger capacitance. Equation (46) shows that when the minimum voltage is chosen as $\frac{V_{max}}{2}$, as in the example above, the capacitance will only be 1.333 times larger than that of the minimum possible capacitance, but with corresponding current and voltage waveforms that are much easier to practically achieve. The advantage of a much smaller capacitor when the capacitor is decoupled from the DC-bus, is mainly lost after 0.8 times the maximum voltage. It is at this point where the capacitance greatly increases for a very small difference in voltage variation.

It can also be seen that at the choice of minimum voltage approaching the maximum voltage, the limit of the function approaches infinity. This also shows that an infinitely

large capacitor is required to have a constant DC-bus voltage, when passive filtering is applied.

3.2.2 *Losses*

The control and design of power electronic devices depend heavily on the losses. This is an important consideration in this context, as it will greatly affect the efficiency and cooling requirements of the converter and, in turn, the overall volume.

Losses can occur in almost all of the components in a power electronic converter, although the biggest contributions are usually the energy storage components and the power electronic switching devices or transistors.

In general, converters with a very wide voltage or current conversion ratio, cannot operate efficiently across the entire operating range without complicated control. It is for this reason that it is good practice to limit the operating region of the converter to be able to limit the losses, even though the capacitance would be sacrificed in the process.

A loss model of the chosen converter will greatly simplify the choice that the designer has to make on the voltage variation. For this reason a rudimentary loss model has been incorporated in Chapter 4.

3.2.3 *Component Ratings and Stress*

An advantage of the mathematical model presented in Chapter 3.1 is that the voltage and current that will have to be accommodated by the chosen converter, is accurately defined before the converter design stage starts.

By knowing the extreme current and voltage values before the design process of the converter starts, the process can be greatly simplified.

With this model, the voltages can be chosen to keep the current below the maximum rating of the available components. This enables designers to not have to procure new components to accommodate the design, but rather enables the designer to design the solution to fit the components available.

3.3 PHASE COMPENSATION

It must be kept in mind that the phase of the capacitor power waveform is very important with regards to the output power. If the capacitor power is out of phase with the grid power, the resulting DC voltage ripple could become even larger than if no filter is installed. Equation (28) can be rearranged to accommodate a phase angle with regards to the line voltage to yield:

$$V_c(\mathrm{t}) = \sqrt{-\frac{1}{2}({V_{max}}^2 - {V_{min}}^2)\cos(2\omega t - \theta) + \frac{1}{2}({V_{max}}^2 + {V_{min}}^2)} \tag{47}$$

Phase compensation is however not required with passive filtering, as the capacitor voltage will naturally assume the correct phase for the DC ripple to be reduced. It is this phase compensation that will enable the device to be used on reactive loads as well, but for the purpose of this study, the assumption is made that the inverter load is only resistive.

Assuming a resistive inverter load, let the inverter output voltage be:

$$V_{AC}(t) = Vsin(\omega t) \tag{48}$$

and let

$$I_{AC}(t) = Isin(\omega t) \tag{49}$$

Equation (48) can then be plotted along with the corresponding power waveform that will be seen at the output terminals of the inverter. The filter capacitor voltage and power waveform is also plotted and can be seen in Figure 3-8 and Figure 3-9 below:

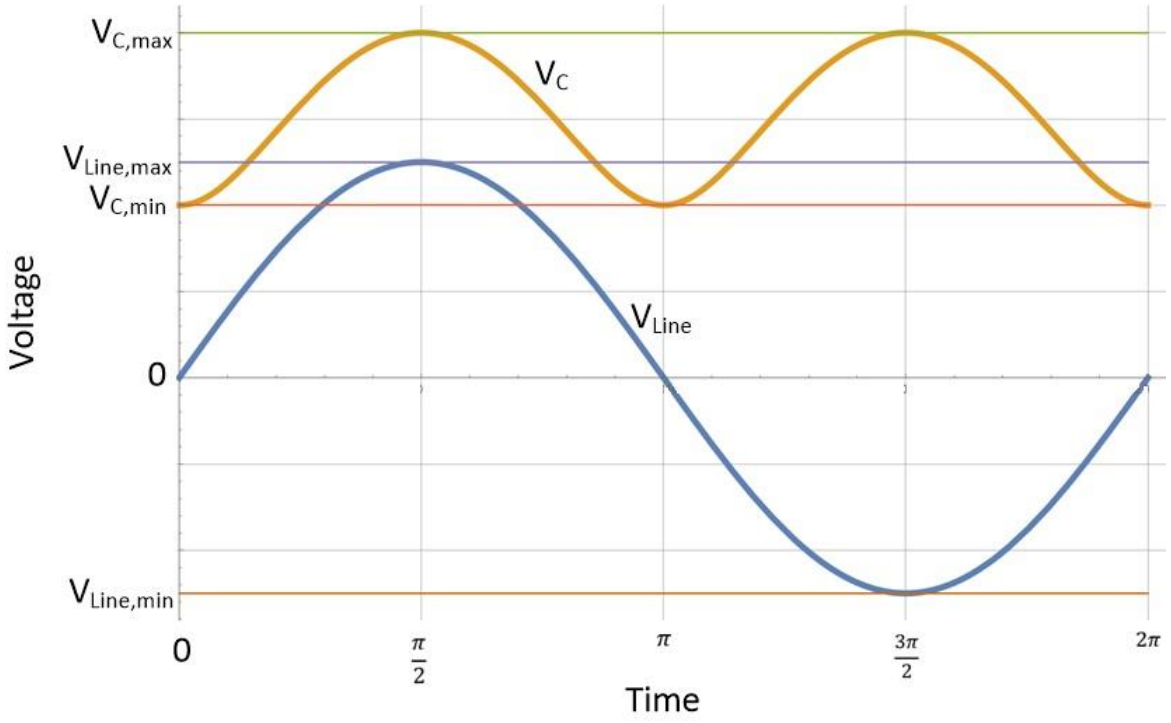


Figure 3-8: Inverter output voltage and active filter capacitor voltage waveforms without phase compensation.

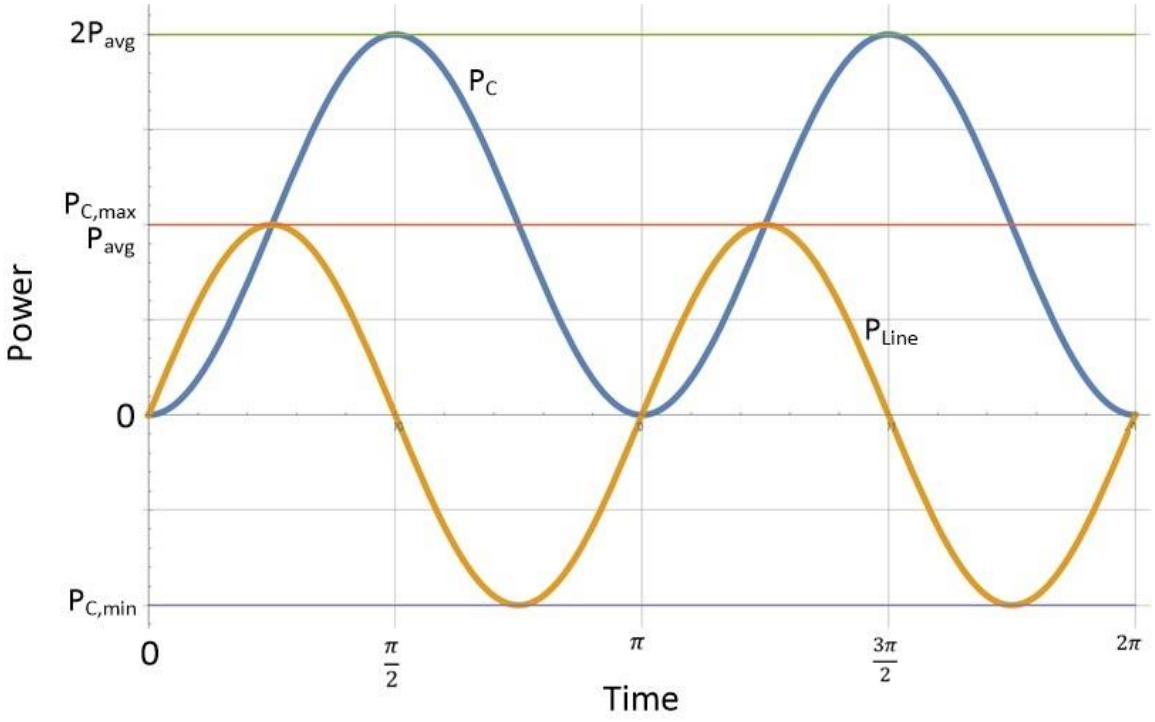


Figure 3-9: Inverter output power and active filter capacitor power waveforms without phase compensation.

The effect of the sum of the power waveforms in Figure 3-9, and the resulting system power waveform be seen in the Figure 3-10 below:

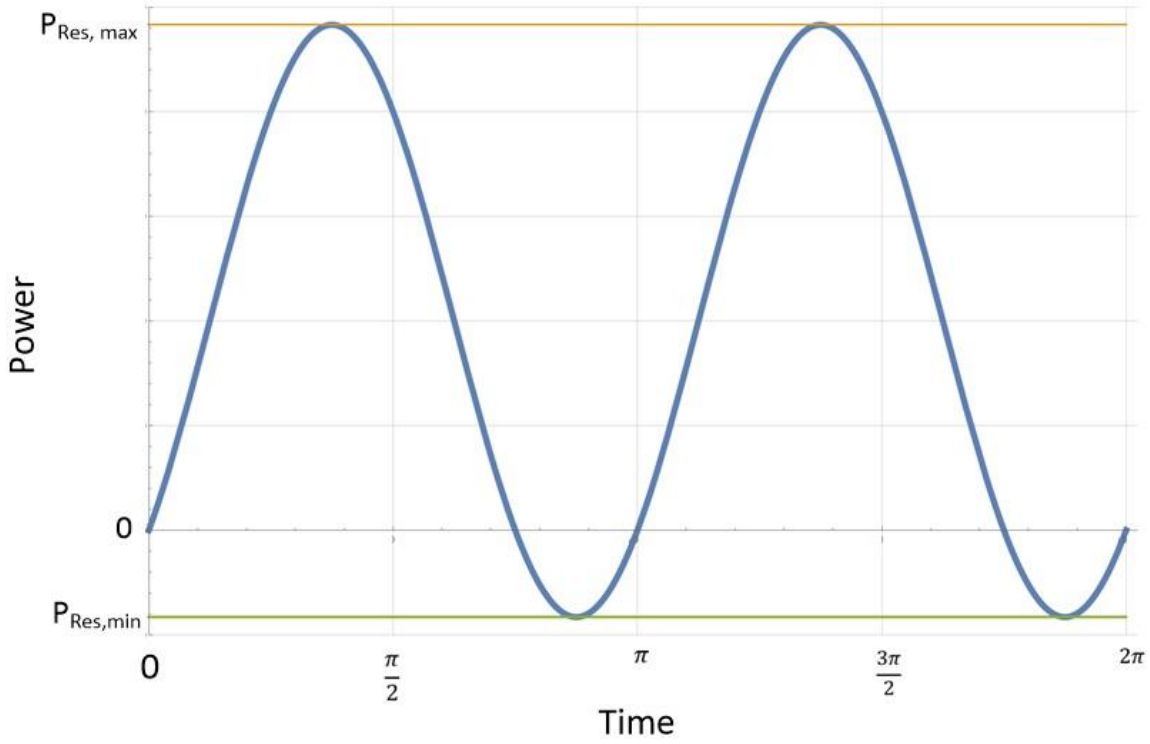


Figure 3-10: Resulting system power waveform without phase compensation.

It can be seen that even though the ripple is around the average power value, this would be a very undesirable effect, as the resulting DC-bus current and voltage ripple would be very large. This would, in turn, damage components and create very high inefficiencies due to increased losses.

As the voltage of the capacitor is controlled to control the power processed by the capacitor, the forced capacitor voltage waveform must be phase shifted, so that the capacitor power waveforms of the inverter AC side waveforms are π radians out of phase.

From Figure 3-9 it can be seen that the capacitor power waveform has to shift $\frac{\pi}{4}$ radians earlier in time, in order to be exactly out of phase with the inverter power. Keeping in mind that the capacitor voltage waveform is at twice the frequency of the line voltage and using trigonometry substitutions, it is found that if θ from Equation (47) is set as $-\frac{\pi}{2}$, the resulting capacitor voltage and current will shift in order to achieve Figure 3-11, Figure 3-12 and Figure 3-13 below:

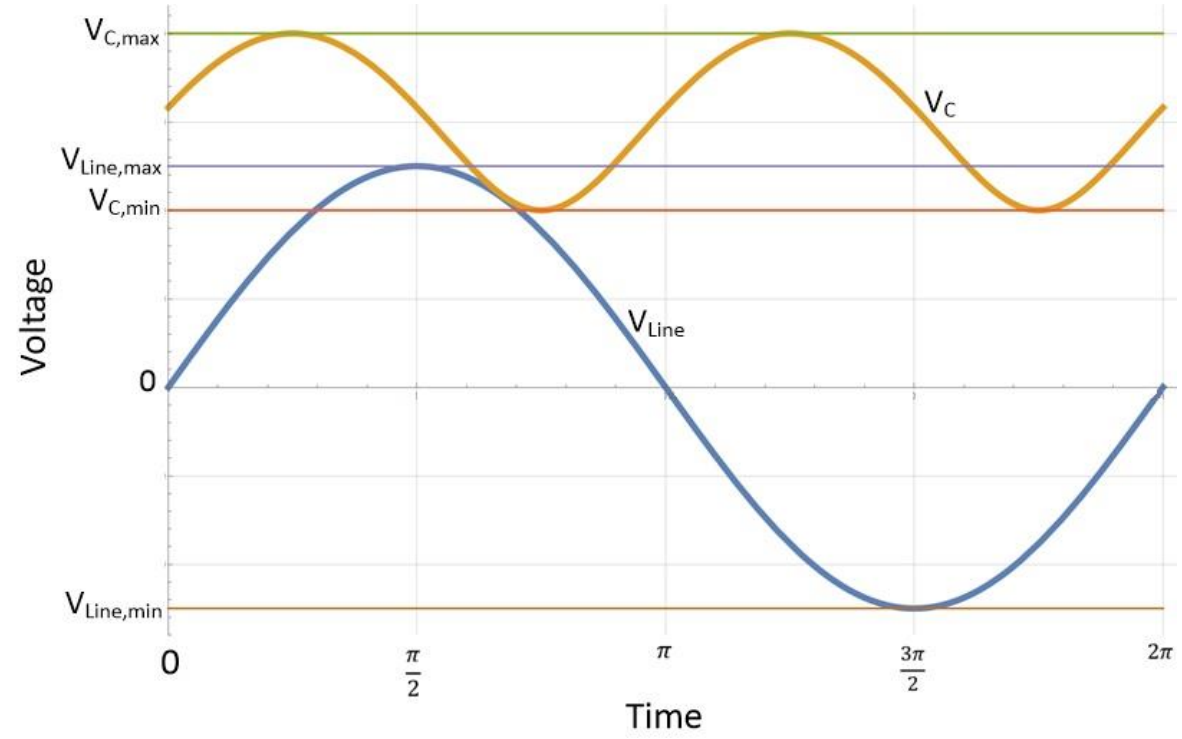


Figure 3-11: Inverter output voltage and active filter capacitor voltage waveforms with phase compensation

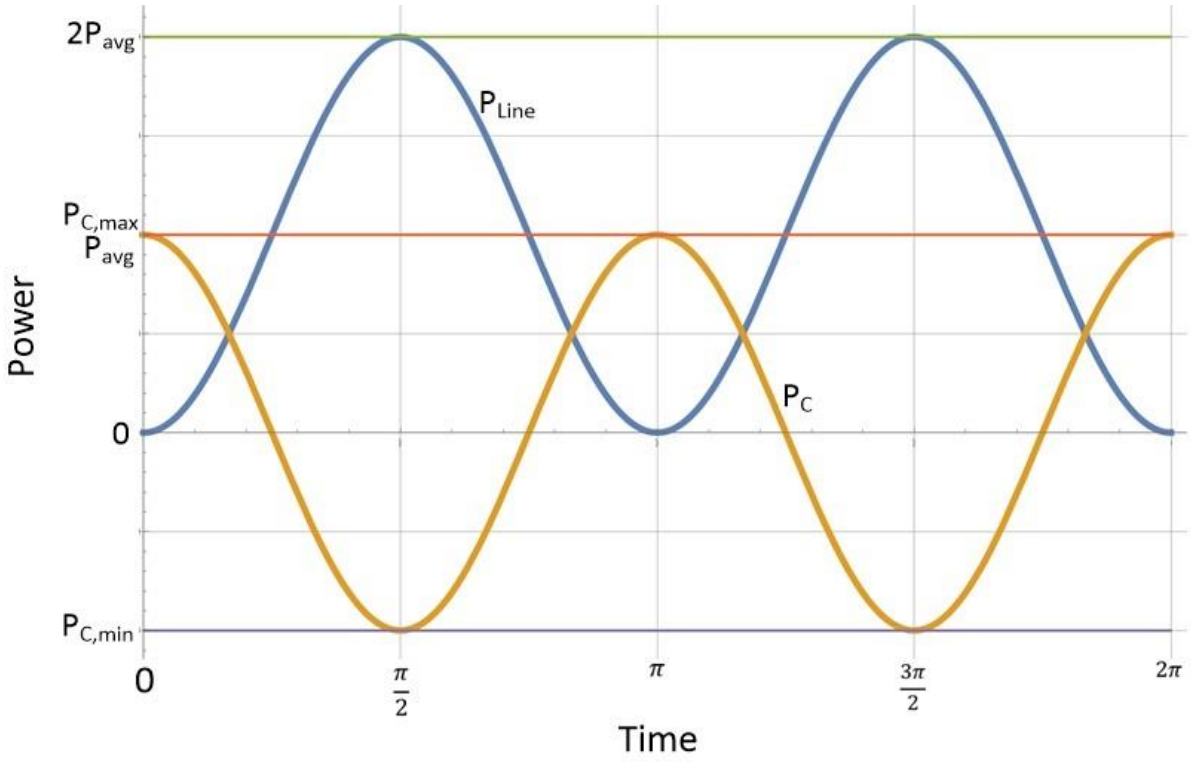


Figure 3-12: Inverter output power and active filter capacitor power waveforms with phase compensation.

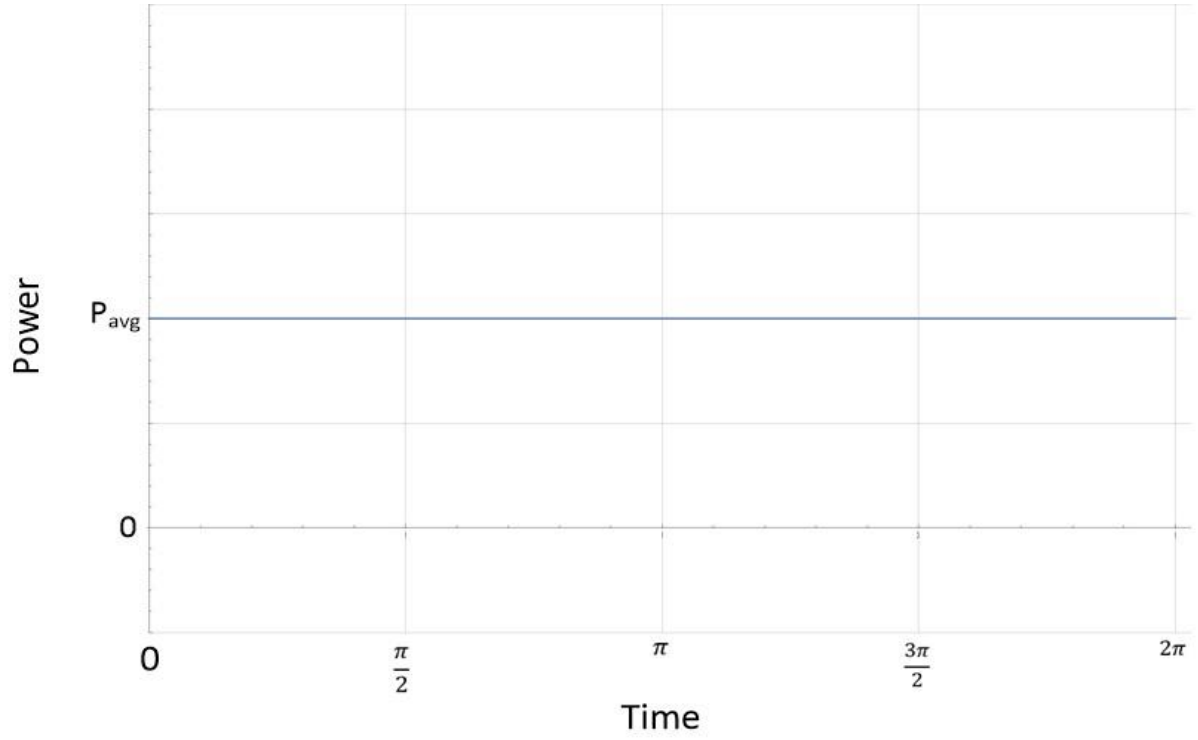


Figure 3-13: Resulting system power waveform with phase compensation.

In Figure 3-13 the ripple free DC bus power can be seen with phase compensation incorporated.

3.4 GENERAL SOLUTION DESIGN PROCEDURE

With all the building blocks now available, a general solution can be formulated. In this section, a step by step design procedure of how the approach described in this research can be implemented, to achieve the desired outcome, is presented. This section is applicable to any converter or any capacitor and enables designers to implement the converter or technology that they are most comfortable with.

The assumptions for the guide to be applicable are as follows:

- The inverter is single phase.
- The average power rating and line frequency of the inverter are available.
- The choice of direct capacitor power control has been made.
- The inverter is operating at a maximum point of operation.

The Flow Diagram and descriptions thereof can be seen in Figure 3-14 below:

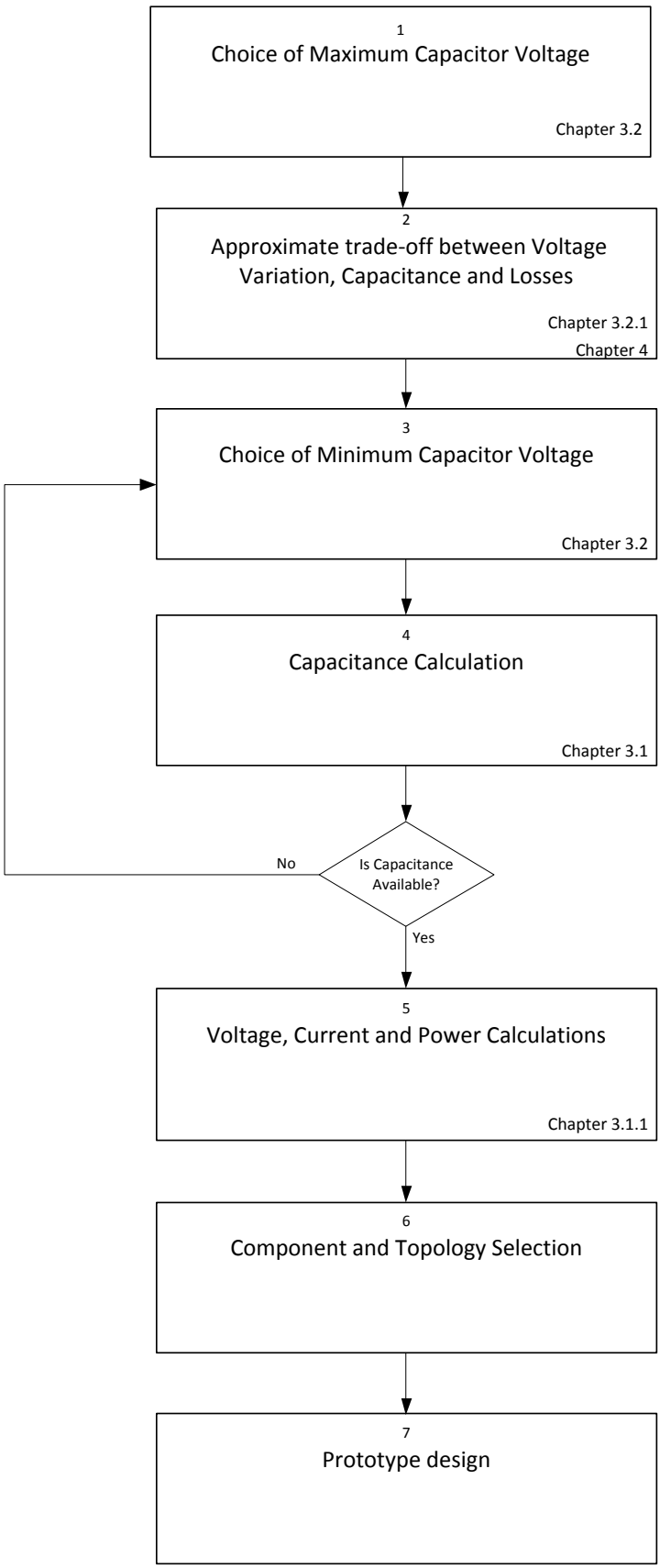


Figure 3-14: Flow diagram of general solution design procedure of the fundamental approach to capacitor power control.

Block 1 – Choice of maximum Capacitor Voltage:

The first step of this design procedure would be to decide on the maximum capacitor voltage. This value will typically depend on the ratings of components that are already available to the designer. It must be noted that, because the capacitor will be decoupled from the DC-bus, the chosen voltage value is of no relevance to the DC-bus voltage. It is advised to choose this value relatively close to the DC-bus voltage. This will avoid too much strain on the converter and avoid the need to design for high conversion ratios. Theoretically, the voltage can be any value chosen by the designer.

Block 2 – Approximate trade-off between Voltage Variation, Capacitance and Losses:

One can now move on to the trade-off between the voltage variation, capacitance and losses. This step, as in Block One, must be chosen with the converter design in mind. If the choice of the absolute minimum voltage is made, the converter will be subjected to very high stress and conversion ratios, which usually requires complicated control and unnecessary losses in the converter.

Figure 3-7 and Figure 4-6 visually illustrates this trade-off. It is advised that the choice is made in the indicated optimum region. This optimum region is discussed in the following chapter.

Block 3 – Choice of Minimum Capacitor Voltage:

After the approximate voltage variation has been decided on, the specific minimum capacitor voltage must be chosen, keeping in mind the comments of Block Two.

Block 4 – Capacitance Calculation:

Equation (25) must now be used to calculate the required capacitance for the chosen voltage variation. If this capacitance value is too high, the designer can

simply return to block one to change the chosen voltages and re-assess the choices.

Decision Block – Is Capacitance Available?:

The capacitance value calculated in Equation (25) will likely not be commercially available. It is then the designer's responsibility to compare the calculated result of the capacitance with an available capacitance and then select a new capacitance as close as possible to the calculated value. The designer must then return to the capacitance calculation and calculate a new value for the minimum or maximum voltage. This must be done to ensure that the power processed by the capacitor remains as predicted.

Block 5 – Voltage, Current and Power Calculations:

The new values of minimum and maximum voltage can then be substituted into Equation (28), Equation (29) and Equation (31) to calculate and plot the waveform of the voltage, current and power, respectively.

Block 6 – Component and Topology Selection:

From the results of Block Five, the component selection can now be made as all the maximum voltage and current values will be available. A choice of an appropriate converter can also be made, that will be able to deliver the waveforms calculated in Block Five.

Block 7 – Prototype Design:

All the design variables will now be available for the designer to create a device to solve the problem of instantaneous power mismatch with an active filter applying direct capacitor power control.

4 CONVERTER LOSS MODEL

As stated in the previous Chapter 3.2.2, to be able to use the model to its full potential, a loss model of the chosen converter is also required. It is not a necessity to incorporate a loss model into the general solution, but it will add the ability to accurately choose a set point voltage variation. The trade-off between voltage variation, capacitance and losses can be viewed on the same plot simultaneously and an informed decision can then be made.

For the purpose of this study, a simple full bridge converter is chosen as seen in Figure 4-1 below. As it is not the purpose of this research to optimise the converter design, a simple PWM modulation technique is assumed, along with hard switching of all the transistors across the entire operating range.

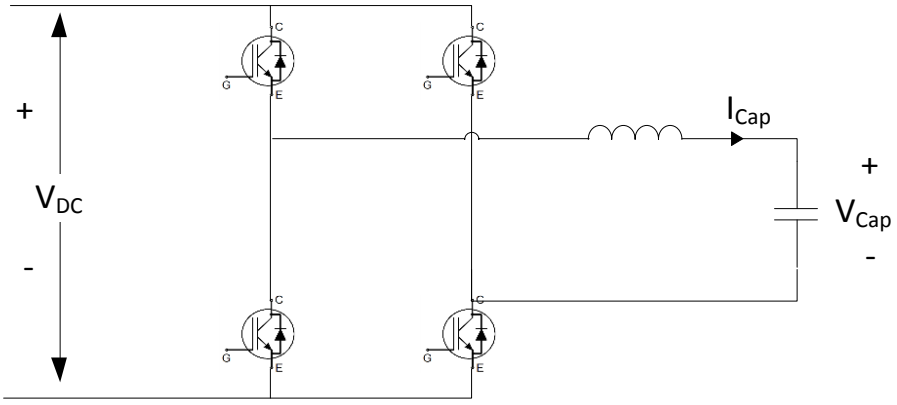


Figure 4-1: Bi-Directional Full Bridge converter configuration.

For the purpose of this rudimentary loss model, the assumption is made that only switching losses and conduction losses of the transistors will significantly contribute to the total converter losses. Other losses incurred from the circuit like the capacitor's series resistance are deemed to be insignificantly small, and will be ignored.

The argument of how the losses of this converter can be calculated has been established in [17]–[19]. These researches made use of the integral of continuous time functions to calculate the losses over a specific period. In this research these formulas were adapted to accommodate discrete time steps instead of continuous time functions.

The main goal of this loss model is not to establish a traditional model, where the losses are compared at different power outputs. The purpose is to be able to visually asses the losses at the same power output, but at different chosen voltage variations.

This would enable the designer to quickly and accurately assess the choice of voltage variation, capacitance and converter losses. All these factors can then be displayed on the same plot.

As there are several variables in the general solution that can change how the loss model will be presented, the following assumptions are made, as in the capacitance evaluation in Chapter 3.2.1 to be able to be compared:

1. The inverter output power is kept constant.
2. The choice of maximum capacitor voltage remains constant.
3. The choice of minimum capacitor voltage is chosen as a factor of the maximum capacitor voltage.

4.1 CHOSEN COMPONENTS

To be able to assess the losses of a transistor, the characteristics of the specific transistor needs to be known. Most of the important characteristics that are required to evaluate the transistor can typically be found in the manufacturer's datasheet of the device.

Depending on the required accuracy, researchers tend to test the transistors under laboratory conditions to be able to measure the desired characteristics with accurate measuring equipment. In this research, only the datasheet characteristics will be utilised.

It has been decided to use IGBT's in this model, even though any transistor with any bidirectional converter can be used. IGBT's have been chosen mainly because of the high power capabilities, as IGBT's perform better that MOSFET's at higher voltages and a higher voltage would equate to a smaller capacitance at the same power requirements.

To keep up with modern trends of increased switching frequency, the IGBT in the Infineon Trenchstop 5 range has been chosen. The relevant characteristics from the datasheet can be seen in the Table 1 below:

Table 1: Chosen Infineon IGBT characteristics

Parameter	Value
Part Number	IKP15N65F5
Collector - Emitter Breakdown Voltage	650 V
Collector Current	21 A
Operating Switching Frequency	30 kHz – 120 kHz

Additional characteristics of the IGBT will be discussed as they become relevant in the specific section.

It has to be kept in mind that the current through the transistor and the length of the "on" period of the transistor changes for one point of operation, as seen in Figure 3-5. This increases the complexity of the loss model.

Normally a single switching period can be evaluated to determine the losses of a single point of operation, but in this model a full cycle of the grid frequency current has to be evaluated to determine the losses at a single point of operation of the converter. The duration of this cycle will be equal to the period of twice the line frequency.

4.2 CONDUCTION LOSSES

The conduction losses in a transistor occur when the transistor is in full conduction. These losses are governed by the Collector – Emitter saturation voltage and the current that is flowing through the transistor at that time. The presence of voltage over the transistor and current through the transistor at the same time, equates to power being dissipated by the transistor in the form of heat.

To calculate the conduction losses of the above mentioned converter, a discrete Microsoft Excel model has been created. In this model, one full current cycle is evaluated with discrete time steps. In each of these time steps, the transistor state (on or off), voltage and current is evaluated, to determine the instantaneous power

dissipated in that specific time period. Equation (50), a generic equation of the calculation of power, is adapted to fit the discrete model.

$$P_{Conduct,avg} = \frac{1}{T}\int_0^T P_{conduct}(t)\,dt \tag{50}$$

The average power dissipated for the total period can then be calculated by adding all the discrete time step power values together, and then dividing the calculated sum by the number of time steps. An equation to illustrate this can be seen in Equation (51) below.

This process is then repeated on a range of values from zero to 0.975 times the value of the maximum capacitor value. This is done to be able to assess the operating range where values would possibly be chosen.

In the evaluation of this discrete model, it was found that the total power dissipated by the converter due to conduction losses cannot be calculated by calculating the losses of a single transistor and multiplying it by 4 for the number of transistors. This is due to the fact that the "On" and "Off" durations of transistors T1 and T4 vary greatly with transistor T2 and T3, as named in Figure 4-1. If the minimum capacitor voltage is chosen high, T1 and T4 will be in the "On" state for much longer periods than T2 and T3.

As stated above, the model is defined in terms of the choice of the minimum capacitor voltage, as a factor of the chosen maximum capacitor voltage. The method of calculating the conduction losses can be seen in the equation below:

$$P_{Conduct,V_{min}=xV_{max}} = 2 \times \frac{\sum_{i=1}^{n}(V_{CE,sat} \times I_{T1,T4}[i_x])}{n} + 2 \times \frac{\sum_{i=1}^{n}(V_{CE,sat} \times I_{T2,T3}[i_x])}{n} \tag{51}$$

Equation (51) is explained as follows:

- $P_{Conduct,V_{min}=xV_{max}}$ is the calculated conduction losses of when the minimum voltage is chosen as a factor, x, of the maximum voltage.

- x is defined as: {0; 0.1; 0.2; 0.3; 0.4; 0.5; 0.6; 0.7; 0.8; 0.9; 0.975}. x is never defined as 1, as that would imply that the minimum and maximum capacitor voltage is equal.
- The number two is for the two transistors in the converter that have the same losses.
- $V_{CE,sat}$ is the Collector – Emitter saturation voltage.
- $I_{T1,T4}[i_x]$ is the magnitude of the current through the transistors T1 and T4, at the time period defined as i, in the scenario where the minimum voltage is chosen as x times the maximum voltage.
- $I_{T2,T3}[i_x]$ is the magnitude of the current through the transistors T2 and T3, at the time period defined as i, in the scenario where the minimum voltage is chosen as x times the maximum voltage.
- n is the number of time steps.

A possible scenario that will be explained in more detail in the following chapter has been evaluated to be able to plot the loss model results. In this scenario, the average power value of the converter has been chosen as 2000 W and the maximum capacitor voltage and DC-bus voltage has been chosen as 400 V. The converter switching frequency has also been chosen as 100 kHz.

From the datasheet of the chosen IGBT, it is seen that the Collector-Emitter saturation voltage at 25˚ C is given as 1.6 V, and as 1.85 V at 150˚ C.

The results of the conduction losses part of the model can be seen in Figure 4-2 below:

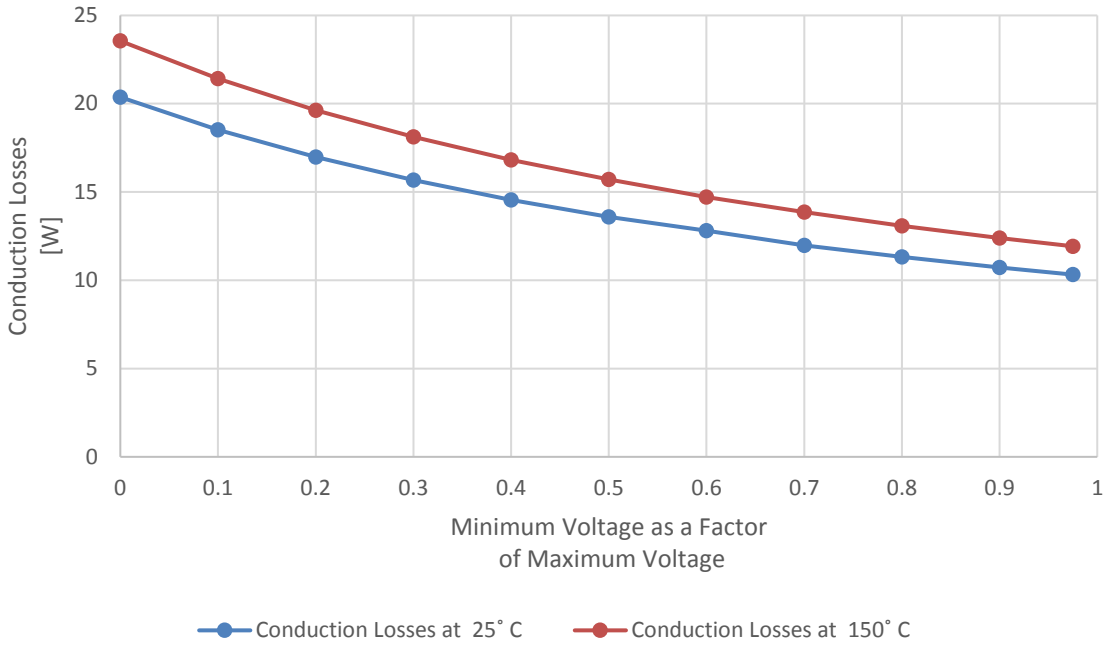


Figure 4-2: Calculated conduction losses of Full Bridge converter as a function of the selected minimum capacitor voltage.

From the preliminary results, it can already be seen that a smaller voltage variation has a very large impact on the associated conduction losses.

4.3 SWITCHING LOSSES

Switching losses occur in a transistor in the transition period when the device is either turning on or off. In this period, for a very short time, there will be significant current through and voltage over the transistor, which will result in power being dissipated in the transistor.

As stated previously in the chapter, for an accurate model, researchers usually measure these transitions to be able to predict the switching losses. For the purpose of this study, the datasheet of the specific transistor will be utilised.

In this datasheet, the energy dissipation values of the turn-on, turn-off and total energy dissipated per transition had been supplied. These values at different temperatures can be seen in Table 2 below:

Table 2: Switching Energy Losses of Chosen IGBT

IGBT Junction Temperature (˚ C)	Total Energy Dissipated (mJ)	
	I_C = 2 A	I_C = 7.5 A
At 25	0.06	0.17
At 150	0.08	0.24

The assumption is made that these given energy losses are accurate enough for the purpose of this loss model. The datasheet also states that these values include the tail of the IGBT turn-off transition and the diode reverse recovery energy.

From the datasheet it could also be seen that the switching losses increase linearly as the Collector current increases. The above mentioned information could then be extrapolated to create functions for the total energy losses, including turn-on and turn-off energy at the different current values. The functions and plots can be seen below:

$$E_{Total,\ 25^{\circ}C} = 0.00002 \times I_C + 0.00002 \tag{52}$$

$$E_{Total,\ 150^{\circ}C} = 0.00003 \times I_C + 0.000022 \tag{53}$$

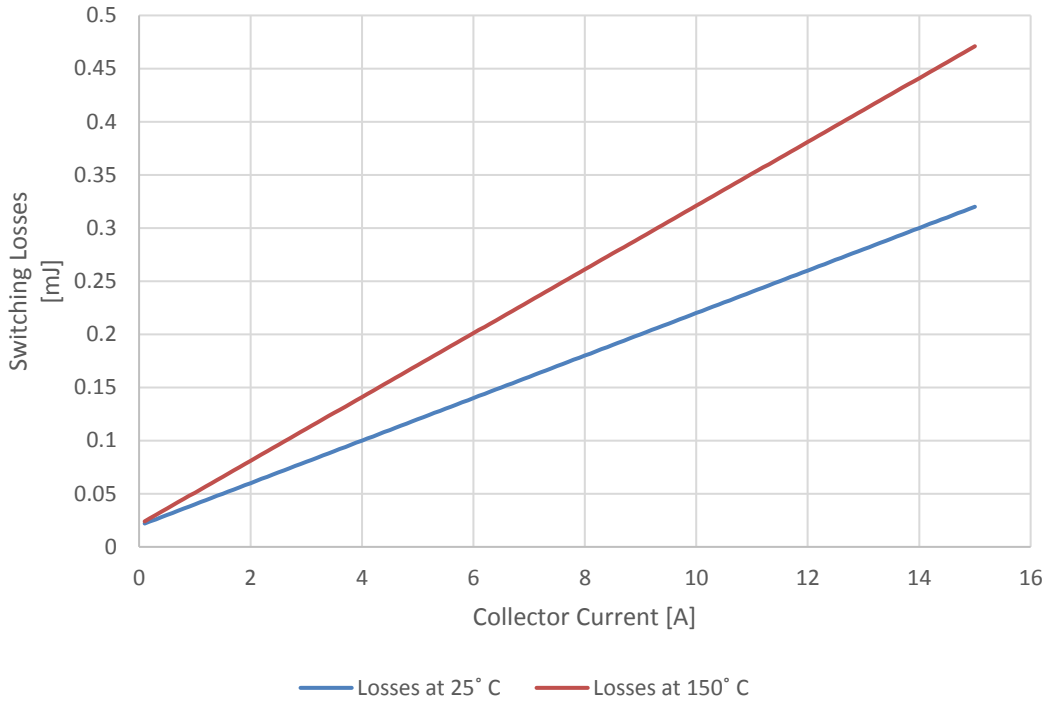


Figure 4-3: Total IGBT switching losses function per transition at 25 ˚C and 150 ˚C respectively.

The power dissipation of the IGBT due to switching losses could then be calculated with the equation below. The total amount of energy dissipated in one current cycle is added together and divided by the period, to convert energy to power.

It could be seen that the switching losses of all four of the transistors are equal over the total current period. This is because the amount of power and the switching transitions of all the transistors are very close at any given transition.

$$P_{Switching,V_{min}=xV_{max}} = 4 \times \frac{\sum_{i=1}^{n}(E[i_x])}{T} \quad (54)$$

Equation (54) is explained as follows:

- $P_{Switching,V_{min}=xV_{max}}$ is the calculated switching losses of when the minimum voltage is chosen as a factor, x, of the maximum voltage.
- x is defined as: {0; 0.1; 0.2; 0.3; 0.4; 0.5; 0.6; 0.7; 0.8; 0.9; 0.975}. x is never defined as 1, as that would imply that the minimum and maximum capacitor voltage is equal.
- The number four is for the four transistors in the converter.
- $E[i_x]$ is the magnitude of the energy dissipated, at the time period defined as i, in the scenario where the minimum voltage is chosen as x times the maximum voltage.
- n is the number of time steps.
- T is the period of one current cycle.

The same scenario as described in Chapter 4.2 was incorporated into the model, and the total switching losses of the converter can be seen in Figure 4-4 below:

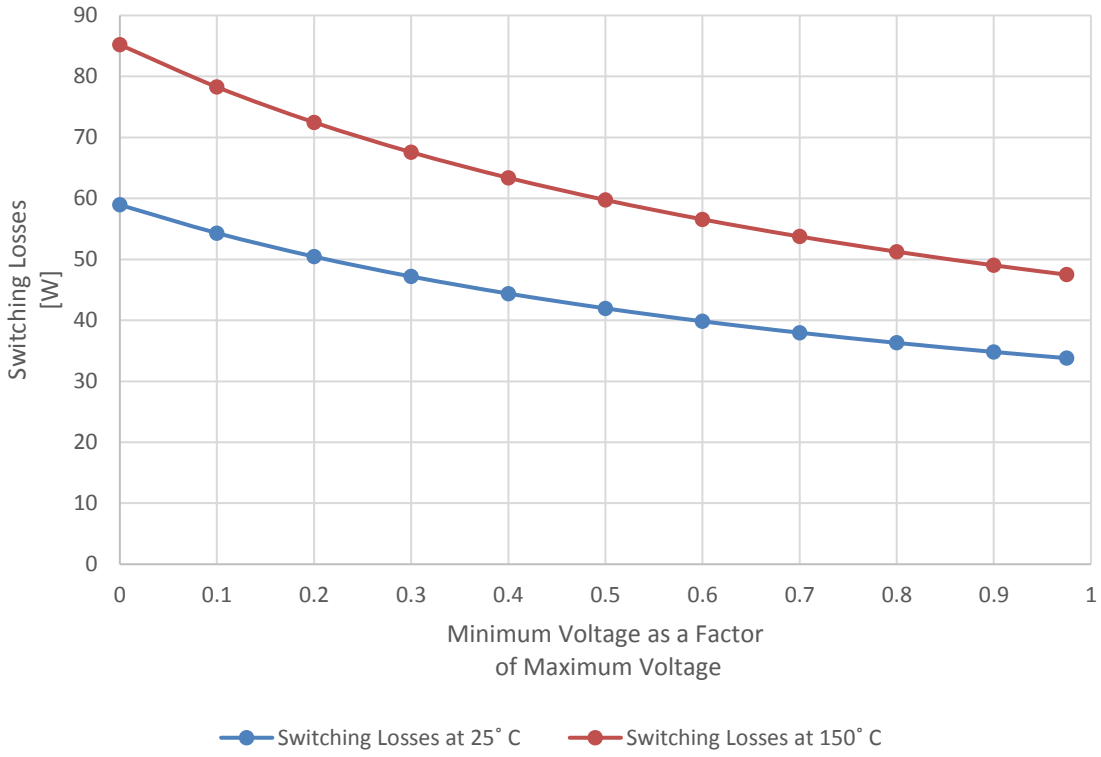


Figure 4-4: Predicted switching losses of converter.

4.4 DISCUSSION

4.4.1 *Total Converter Losses*

The total converter losses, including conduction and switching losses of the entire converter, can be seen in Figure 4-5 below:

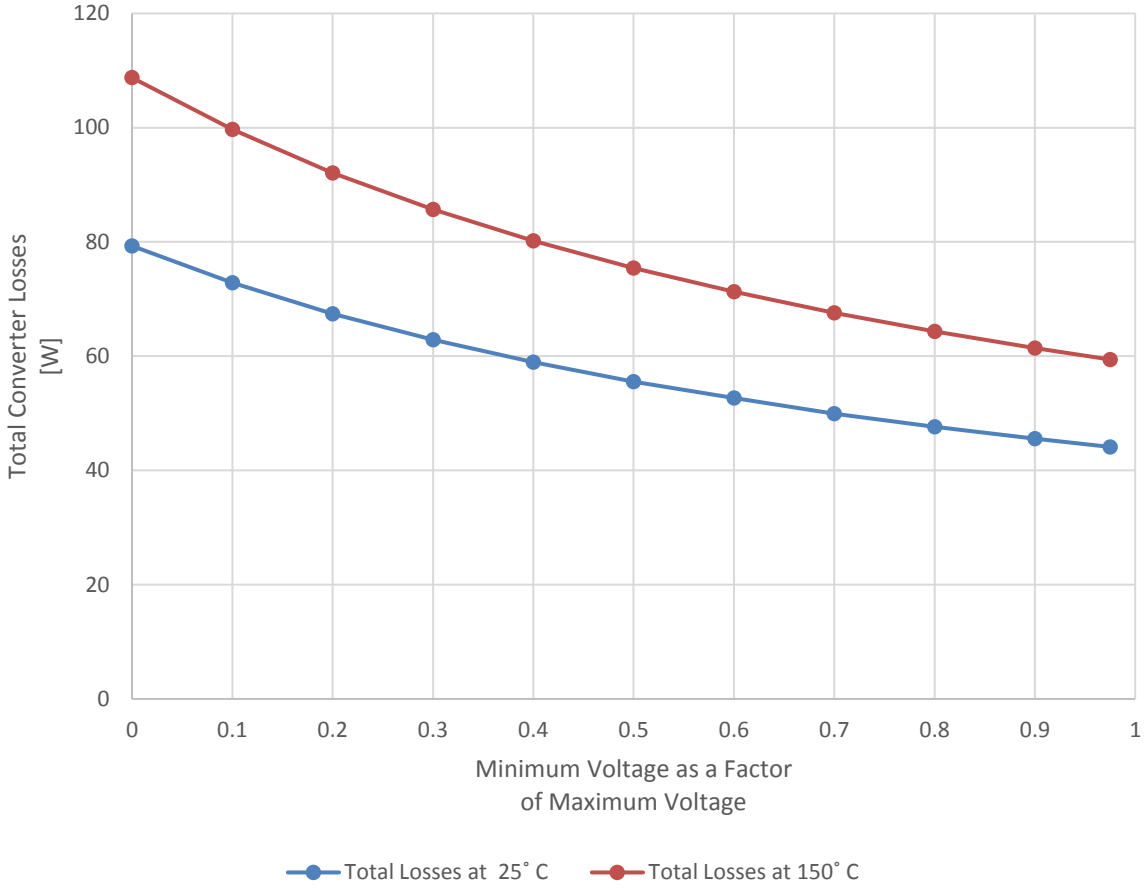


Figure 4-5: Total calculated losses of Full Bridge converter as a function of the selected minimum capacitor voltage.

From the figure above it can be seen that the choice of the minimum voltage has an impact on the total losses of the converter. At a temperature of 150 ˚C, the losses drop by a total of 46% in the entire range, but already drops 31% at the 0.5 mark. The plot of the losses at 25˚ C drops a total of 45% over the entire range, and 31% as well at the 0.5 mark.

It can also be seen that the slopes of both the loss graphs are at a maximum at the lowest choice of the minimum capacitor voltage and then evens out relatively later in the graph.

The above graphs supports the notion that there are several benefits to not driving the capacitor voltage all the way down to zero volt.

4.4.2 *Optimum Choice of Minimum Voltage*

In Chapter 3.2.1 the trade-off between capacitance and choice of minimum voltage could be seen, and in the chapter before, the trade-off between the converter losses and minimum choice of voltage could be seen. In the figure below both of these trade-offs can be seen on the same axis:

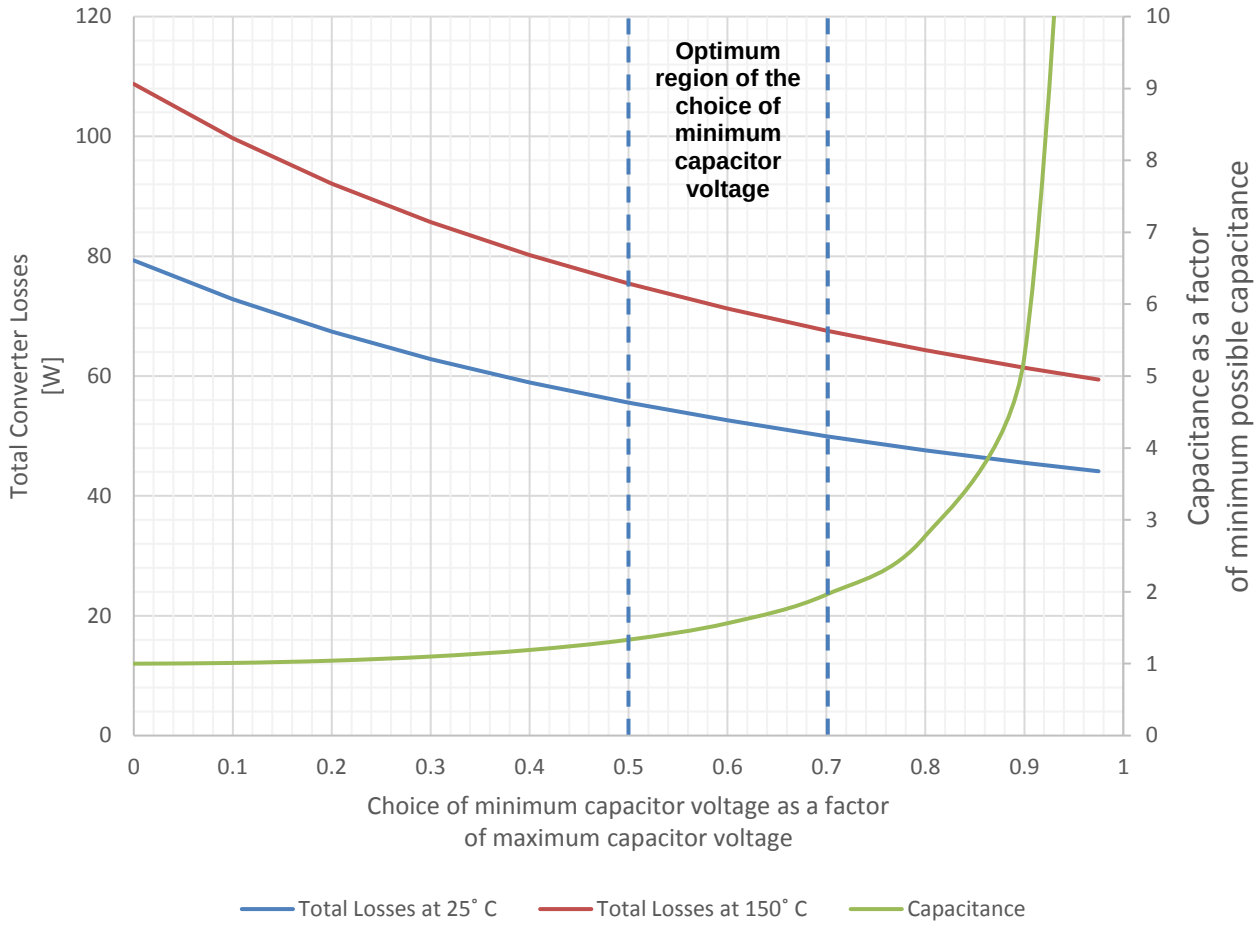


Figure 4-6: Trade-offs illustration between converter losses, capacitance and capacitor voltage, also indicating the suggested region of the optimum choice of minimum capacitor voltage.

From the figure, the optimum region between all of the trade-offs was chosen at a minimum capacitor voltage of 0.5 to 0.7 times the maximum voltage. These values have been chosen by visually inspecting the graph above and comparing possible outcomes. In this chosen region, the capacitance is still before the knee point, at a value of 1.33 to 2 times the minimum possible capacitance value, where the advantages of the small increase in capacitance are still captured.

The losses in this region is where the slope of the loss graph tends closer to 1. Approximately 31% at 0.5 to 38% at 0.7 less than the maximum losses will be incurred at 25˚ C.

When the choice of minimum capacitor voltage is chosen at a higher voltage than the prescribed region, the capacitance increases very fast, and the advantages of a smaller capacitor is quickly lost, without significantly decreasing the converter losses. The increase in the size of the capacitor will greatly outweigh the decrease of the cooling requirements.

On the other hand, when the minimum capacitor voltage is chosen at a lower voltage than the prescribed region, the losses increase greatly with a small decrease in capacitance. Even though the difference would not be as drastic as when the voltage is chosen higher than the indicated area, almost no reduction in capacitance would still cause a significant increase in cooling requirements.

It can be seen that the choice of minimum capacitor voltage in this chosen region captures the positive effects of both the reduction in capacitance and reduces the associated losses.

5 SINGLE PHASE INVERTER CASE STUDY APPLICATION

This section describes a chosen case study where the design procedure described in Chapter 3.4 is followed, including graphs, illustrations and specific components chosen for the circuit. The results will then be compared and discussed.

The concept of direct control of the capacitor power has been proven with experimental results in [4], so this research will only continue up to simulation results.

It must be kept in mind that even though the model is only applied to a single example, the general solution is still applicable to many other solutions with higher or lower voltage or power ratings.

The chosen scenario in Table 3 below is an extract of the requirements of the Little Box Challenge. Let:

Table 3: Little box Challenge Requirements

1)	Rated Average Inverter Power	2000 W
2)	DC Bus Voltage	400 V
3)	Maximum DC Bus Voltage Ripple	3 %

This challenge was rolled out in America, where the line frequency is 60 Hz. For the purpose of this study, a line frequency of 50 Hz has been chosen to conform to South African standards.

Three different solutions have been chosen and will be compared. They are as follows:

Solution One: Passive Filtering.

This approach will only entail connecting a large capacitor across the DC bus, calculated to allow the prescribed 3% voltage ripple.

Solution Two: Ripple Port Active Filtering

In this approach, the direct capacitor power control method is employed. The maximum capacitor voltage is chosen as 400V, and the minimum voltage chosen as zero volt as seen in the experiment done in [4].

Solution Three: Active Filtering

In this approach, the direct capacitor power control method is also employed. The main goal of this chapter is to compare the new application of the general solution to the solutions that already exist. So the maximum capacitor voltage is chosen as 400V, and the minimum voltage chosen as 0.6 times the value of the maximum capacitor voltage, in the centre of the predicted optimum region in Figure 4-6. So the minimum capacitor voltage is chosen as 240 V.

This design will only be applicable to a single point of operation, but the concept is applicable across all ranges.

5.1 DESIGN FROM GENERAL SOLUTION AND ASSOCIATED WAVEFORMS

5.1.1 *Passive Filtering*

For solution one, only a large capacitor will be placed over the DC-bus to limit the ripple within the allowed margins specified above.

For the model to be used, values are required for the maximum capacitor voltage, minimum capacitor voltage and rated inverter power.

For the capacitor voltage:

$$V_{max} = 1.015V_{DC}$$
$$V_{max} = 406\,V \tag{55}$$

$$V_{min} = 0.985V_{DC}$$
$$V_{min} = 394\,V \tag{56}$$

and the Value of P_{avg} is specified to be 2000 W.

The capacitance required for a 3% ripple can then be calculated by substituting the value back into Equation (25) which yields:

$$C = \frac{\frac{2000}{2\pi(50)}}{\left(\frac{1}{2}(406)^2\right) - \left(\frac{1}{2}(394)^2\right)} \tag{57}$$

$$C = 1.326\,mF$$

As set out in the design procedure, this exact capacitance is not commercially available, and an available value that is larger has to be chosen to keep the voltage within limit.

Three commercial capacitor manufacturers, namely: Kemet, Illinois Capacitor and TDK were consulted to select an appropriate capacitor. An electrolytic capacitor with a capacitance of 1.5 mF was chosen.

To calculate the voltage ripple, we can substitute this new capacitance back into Equation (11) and rearrange:

$$\Delta V = \frac{2000}{2\pi\ (50)\ (400)\ (1.5 \times 10^{-3})} \tag{58}$$

$$\Delta V = 10.6\,V$$

The new minimum and maximum capacitor voltages will then be:

$$V_{max} = 405.3\,V$$
$$V_{min} = 394.7\,V \tag{59}$$

The corresponding capacitor voltage, current and power waveforms can then be calculated from Equations (28), (29) and (31) which can be seen in Figure 5-1, Figure 5-2 and Figure 5-3 below. The results are shown for two periods of the line voltage.

$$V_c(\mathrm{t}) = \sqrt{-\frac{1}{2}(405.3^2 - 394.7^2)\cos(2\omega t) + \frac{1}{2}(405.3^2 + 394.7^2)} \tag{60}$$

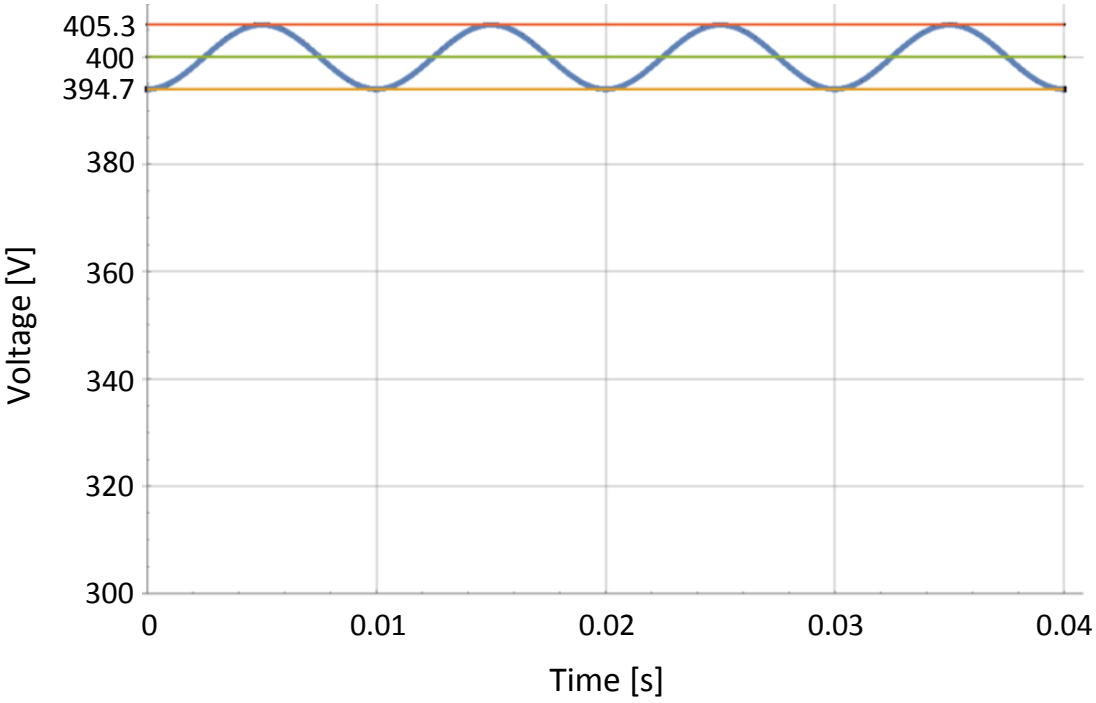


Figure 5-1: Solution One capacitor voltage with less than 3% capacitor voltage ripple.

$$I_c(t) = \frac{(1.5 \times 10^{-3})2\pi(50)\,(405.3^2 - 394.7^2)\sin(2(2\pi(50))t)}{2\sqrt{-\frac{1}{2}(405.3^2 - 394.7^2)\cos(2(2\pi(50)t) + \frac{1}{2}(405.3^2 + 394.7^2)}} \quad (61)$$

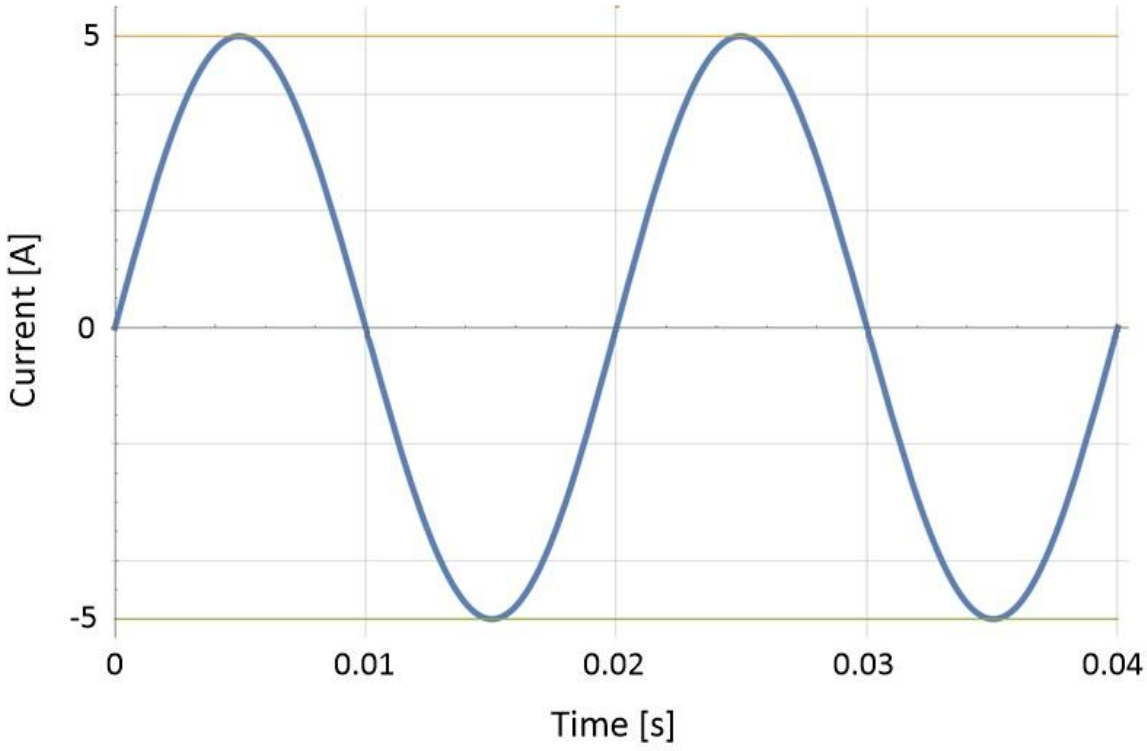


Figure 5-2: Solution One capacitor current.

$$P_c(t) = 2000\sin(2(2\pi(50))t) \quad (62)$$

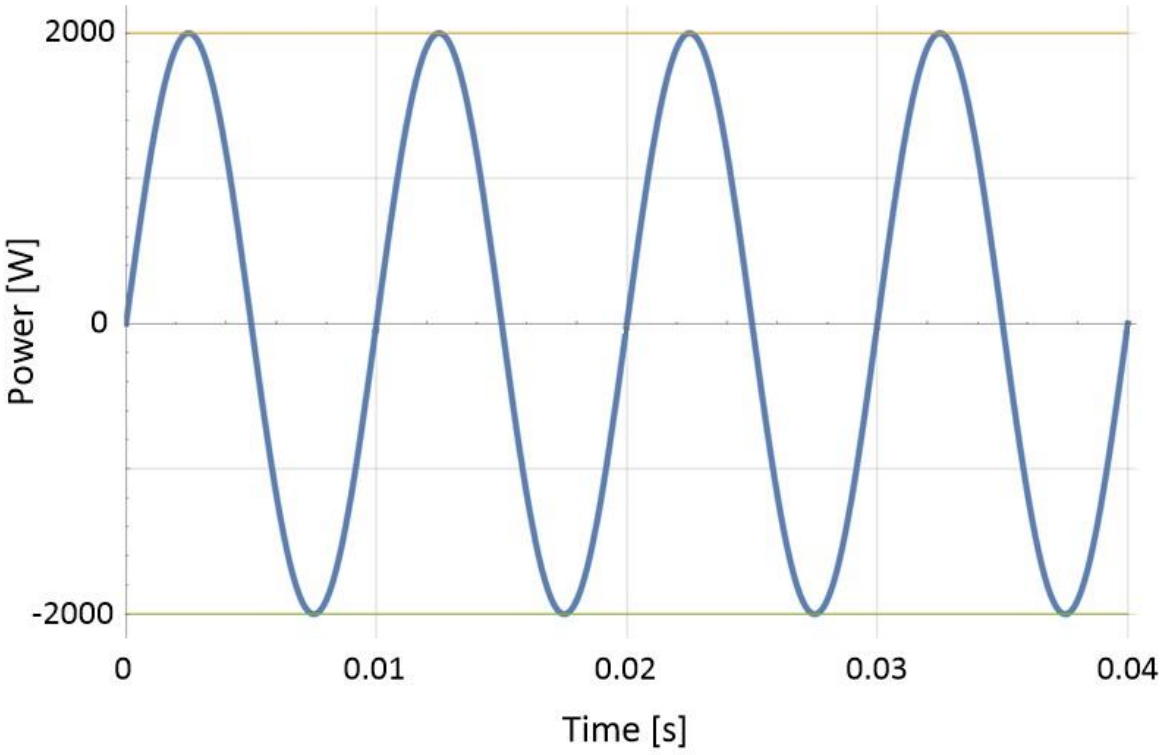


Figure 5-3: Solution One resulting capacitor power waveform

The most important information we can gather from this part of the study is the required capacitance to keep the DC-bus voltage within allowable limits. This will be compared to the results of active filtering solutions in the end of this chapter.

5.1.2 *Active Filtering*

In this section the general design procedure of Chapter 3.4 will be applied. Since step one to three has already been completed, we will start at step four, the capacitance calculation. For this, as in passive filtering, Equation (25) is used which yields:

For Solution Two:

$$C_{S2} = \frac{\frac{2000}{2\pi(50)}}{\left(\frac{1}{2}(400)^2\right) - \left(\frac{1}{2}(0)^2\right)} \tag{63}$$

$$C_{S2} = 79.5775\ \mu F$$

And for Solution Three:

$$C_{S3} = \frac{\frac{2000}{2\pi(50)}}{\left(\frac{1}{2}(400)^2\right) - \left(\frac{1}{2}(240)^2\right)} \tag{64}$$

$$C_{S3} = 124.34\ \mu F$$

As predicted in the General Design Procedure, these calculated values are not commercially available, so new commercially available capacitors are chosen. Note that the closest capacitance value, higher or lower, can be chosen as both will achieve the desired goal. This is unlike in passive filtering, where the larger capacitance must be chosen so that the ripple remains within the selected boundary.

For capacitance in Solution Two:

$$C_{S2} = 80\ \mu F \tag{65}$$

For capacitance in Solution Three:

$$C_{S3} = 120\ \mu F \tag{66}$$

The above mentioned capacitors are also chosen from commercial capacitor manufacturers and both could be found as film capacitors. A 120 µF capacitor with comparable parameters could not be found, so the chosen capacitor for Solution Three is chosen as exactly the same 80 µF capacitor as in Solution 2, and a 40 µF capacitor from the same range. These capacitors can then be installed in parallel. A more in depth comparison will be done later in the chapter.

As said in the decision block, the voltage waveform will have to be recalculated, to ensure that the eventual capacitor power waveform takes the correct sine wave form. For both solutions the minimum voltage was chosen to be recalculated, even though the maximum voltage could have been chosen as well.

Equation (25) can be rearranged to yield:

$$V_{min} = \sqrt{{V_{max}}^2 - \frac{2P_{avg}}{C\omega}} \tag{67}$$

For capacitor of Solution Two:

$$V_{min,S2} = \sqrt{400^2 - \frac{2(2000)}{(80 \times 10^{-6})2\pi(50)}} \tag{68}$$

$$V_{min,S2} = 29.0699\ V$$

For capacitor of Solution Three:

$$V_{min,S3} = \sqrt{400^2 - \frac{2(2000)}{(120 \times 10^{-6})2\pi(50)}} \tag{69}$$

$$V_{min,S3} = 232.157\ V$$

At this point, all the required variables have now been calculated. Block Five is now evaluated in which the plots of the voltage, current and power will be shown. As in passive filtering, Equations (28), (29) and (31) can be utilised to plot the voltage, current and power, as seen in Figure 5-4, Figure 5-5 and Figure 5-6, respectively.

$$V_{c,S2}\,(\mathrm{t}) = \sqrt{-\frac{1}{2}(400^2 - 29.0699^2)\cos(2\omega t) + \frac{1}{2}(400^2 + 29.0699^2)} \tag{70}$$

$$V_{c,S3}\,(\mathrm{t}) = \sqrt{-\frac{1}{2}(400^2 - 232.157^{\,2})\cos(2\omega t) + \frac{1}{2}(400^2 + 232.157^{\,2})} \tag{71}$$

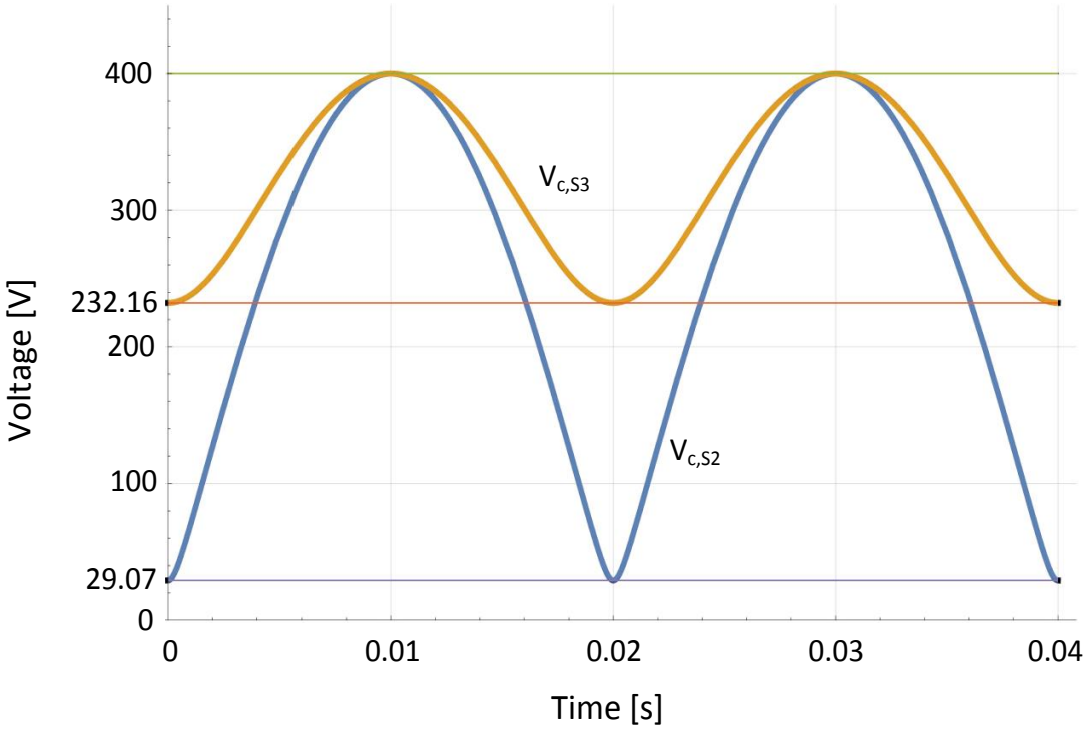


Figure 5-4: Solution Two and Solution Three capacitor voltage waveforms comparison.

$$I_{c,S2}(t) = \frac{(80 \times 10^{-3})2\pi(50)\,(400^2 - 29.0699^2)\sin(2(2\pi(50))t)}{2\sqrt{-\frac{1}{2}(400^2 - 29.0699^2)\cos(2(2\pi(50)t) + \frac{1}{2}(400^2 + 29.0699^2)}} \quad (72)$$

$$I_{c,S3}(t) = \frac{(100 \times 10^{-3})2\pi(50)\,(400^2 - 232.157^{\,2})\sin(2(2\pi(50))t)}{2\sqrt{-\frac{1}{2}(400^2 - 232.157^{\,2})\cos(2(2\pi(50)t) + \frac{1}{2}(400^2 + 232.157^{\,2})}} \quad (73)$$

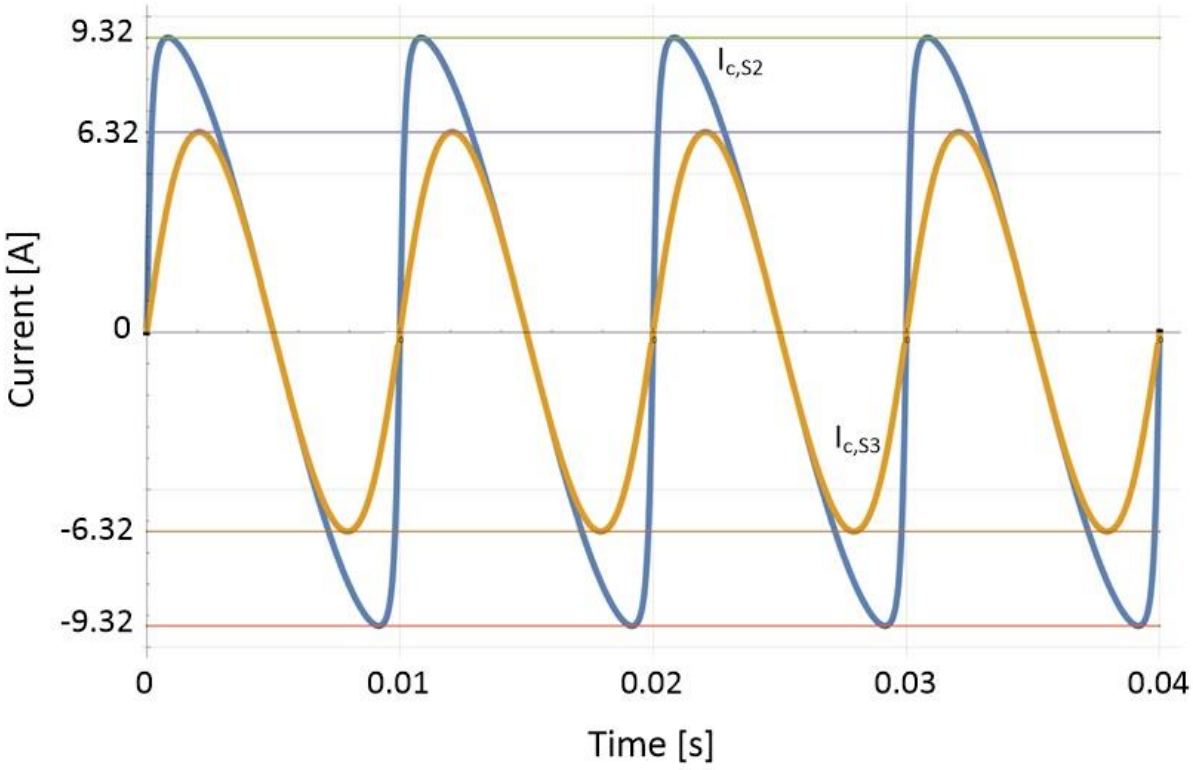


Figure 5-5: Solution Two and Solution Three capacitor current waveforms comparison.

$$P_{c,S2}(t) = 2000\sin(2(2\pi(50))t) \quad (74)$$

$$P_{c,S3}(t) = 2000\sin(2(2\pi(50))t) \quad (75)$$

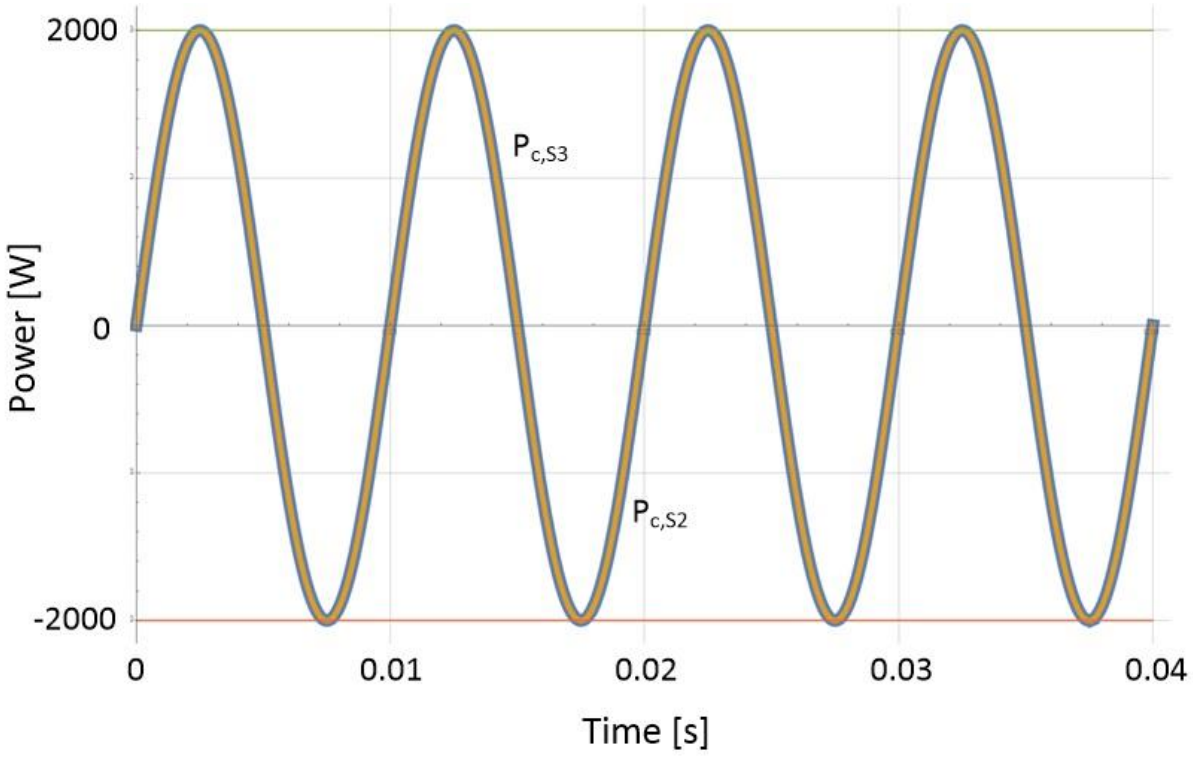


Figure 5-6: Solution Two and Solution Three resulting power wavefvefroms.

Block Six will be discussed in full in Chapter 5.2.

5.2 PROTOTYPE DESIGN

5.2.1 *Passive Filtering*

In this section the components and the converter topology must be selected. For the passive filtering example of Solution One, only a capacitor has to be selected.

This capacitor has been selected as an electrolytic capacitor with the following parameters:

Table 4: Passive Filter Capacitor

Parameter:	Value:
Capacitance	1.5 mF
Manufacturer	Kemet
Rated Voltage	550 VDC
Volume	393.4 cm^3

According to the Equation (11), this capacitor will be able to keep the required voltage under the allowable 3%.

5.2.2 *Active Filtering*

a. Topology Selection

For the topology selection any arbitrary bi-directional converter can be chosen that is able to processes the required power. For the argument presented, a Full Bridge converter has been chosen as seen in Chapter 4.

b. Component Selection

The most important component to select in terms of this research is the capacitor, as the converter and other components would be subject to the decision of the designer.

Research had been done to compile datasheets of film capacitors from Kemet, Illinois Capacitor and TDK and the appropriate film capacitors have been selected as seen in the table below:

Table 5: Active Filtering Component Selection

	Solution Two	Solution Three
Capacitance	80 µF	120 µF (80 µF + 40 µF)
Manufacturer	Illinois Capacitor	Illinois Capacitor
Rated Voltage	700 VDC	700 VDC
Volume	125.6 cm^3	203.3 cm^3

When the volume of the capacitors are compared, it is seen that for Solution Two the total capacitance is 33% less than the capacitance of Solution Three. It can also be seen that the volume of the capacitor of Solution Two is 38% less than the volume of Solution Three

c. Calculated Losses

As all the needed information to calculate the associated losses is now available, the predicted losses for Solution Two and Solution Three can now be calculated.

For conduction losses at 25˚ C we substitute back into Equation (51) to yield:

$$P_{Conduct,25^{\circ}\,\mathrm{C},S2} = 2 \times \frac{\sum_{i=1}^{100\,000}(1.6 \times I_{T1,T4}[i_{S2}])}{100\,000} + 2 \times \frac{\sum_{i=1}^{100\,000}(1.6 \times I_{T2,T3}[i_{S2}])}{100\,000} \tag{76}$$

$$P_{Conduct,25^{\circ}\,\mathrm{C},S2} = 18.99\,W$$

$$P_{Conduct,25^{\circ}\,\mathrm{C},S3} = 2 \times \frac{\sum_{i=1}^{100\,000}(1.6 \times I_{T1,T4}[i_{S3}])}{100\,000} + 2 \times \frac{\sum_{i=1}^{100\,000}(1.6 \times I_{T2,T3}[i_{S3}])}{100\,000} \tag{77}$$

$$P_{Conduct,25^{\circ}\,\mathrm{C},S3} = 12.89\,W$$

In the equations above, the 100 000 refers to the amount of time steps in the model and the 1.6 represents the Collector- Emitter saturation voltage of the chosen IGBT at 25˚ C.

For conduction losses at 150˚ C we substitute back into Equation (51) to yield:

$$P_{Conduct,150^{\circ}\,\mathrm{C},S2} = 2 \times \frac{\sum_{i=1}^{100\,000}(1.85 \times I_{T1,T4}[i_{S2}])}{100\,000} + 2 \times \frac{\sum_{i=1}^{100\,000}(1.85 \times I_{T2,T3}[i_{S2}])}{100\,000} \tag{78}$$

$$P_{Conduct,150^{\circ}\,\mathrm{C},S2} = 21.96\,W$$

$$P_{Conduct,150^{\circ}\,\mathrm{C},S3} = 2 \times \frac{\sum_{i=1}^{100\,000}(1.85 \times I_{T1,T4}[i_{S3}])}{100\,000} + 2 \times \frac{\sum_{i=1}^{100\,000}(1.85 \times I_{T2,T3}[i_{S3}])}{100\,000} \tag{79}$$

$$P_{Conduct,150^{\circ}\,\mathrm{C},S3} = 14.9\,W$$

In the equations above, the 100 000 refers to the amount of time steps in the model and the 1.85 represents the Collector- Emitter saturation voltage of the chosen IGBT at 150˚ C.

For switching losses at 25˚ C we substitute back into Equation (54) to yield:

$$P_{Switching,25^\circ C,S2} = 4 \times \frac{\sum_{i=1}^{1\,000}(E_{25^\circ C}[i_{S2}])}{0.01} \tag{80}$$

$$P_{Switching,25^\circ C,S2} = 55.58\,W$$

$$P_{Switching,25^\circ C,S3} = 4 \times \frac{\sum_{i=1}^{1\,000}(E_{25^\circ C}[i_{S3}])}{0.01} \tag{81}$$

$$P_{Switching,25^\circ C,S3} = 40.25\,W$$

For switching losses at 150˚ C we substitute back into Equation (54) to yield:

$$P_{Switching,150^\circ C,S2} = 4 \times \frac{\sum_{i=1}^{1\,000}(E_{150^\circ C}[i_{S2}])}{0.01} \tag{82}$$

$$P_{Switching,150^\circ C,S2} = 80.16$$

$$P_{Switching,150^\circ C,S3} = 4 \times \frac{\sum_{i=1}^{1\,000}(E_{150^\circ C}[i_{S3}])}{0.01} \tag{83}$$

$$P_{Switching,150^\circ C,S3} = 57.18\,W$$

In the equations above the 1 000 refers to the amount of times the IGBT will switch on and off in the 0.01 second period of the double line frequency.

The total losses at 25˚ C are then calculated to be:

$$P_{Losses,25^\circ C,S2} = 74.57\ W \tag{84}$$

$$P_{Losses,25^\circ C,S3} = 53.14\ W \tag{85}$$

And the total losses at 150˚ C are then calculated to be:

$$P_{Losses,150^\circ C,S2} = 102.12\ W \tag{86}$$

$$P_{Losses,150^\circ C,S3} = 72.08\ W \tag{87}$$

A full discussion of the losses results can then found in Chapter 5.4.

5.3 SIMULATION RESULTS

This chapter describes the simulation results of the above mentioned case study, but does not include the passive filtering case study. Both of the active filter solutions are presented, discussed and verified on a simulation level.

This case study is not presented on an experimental level, as the goal of this research is to present a general solution of capacitor power management and not a specific application solution.

The configuration of the active filter in conjunction with the full bridge single phase inverter can be seen below. Both of the active filter scenarios in the case study make use of exactly the same circuit, only with different capacitances. A triangular waveform of 100 000 kHz was used as the carrier waveform and the fundamental voltage waveform calculated in Chapter 5.1.2 was implemented using C code. All of the simulations were conducted in PSIM.

Phase compensation, as discussed in Chapter 3.3, had also been implemented in both of the simulation scenarios.

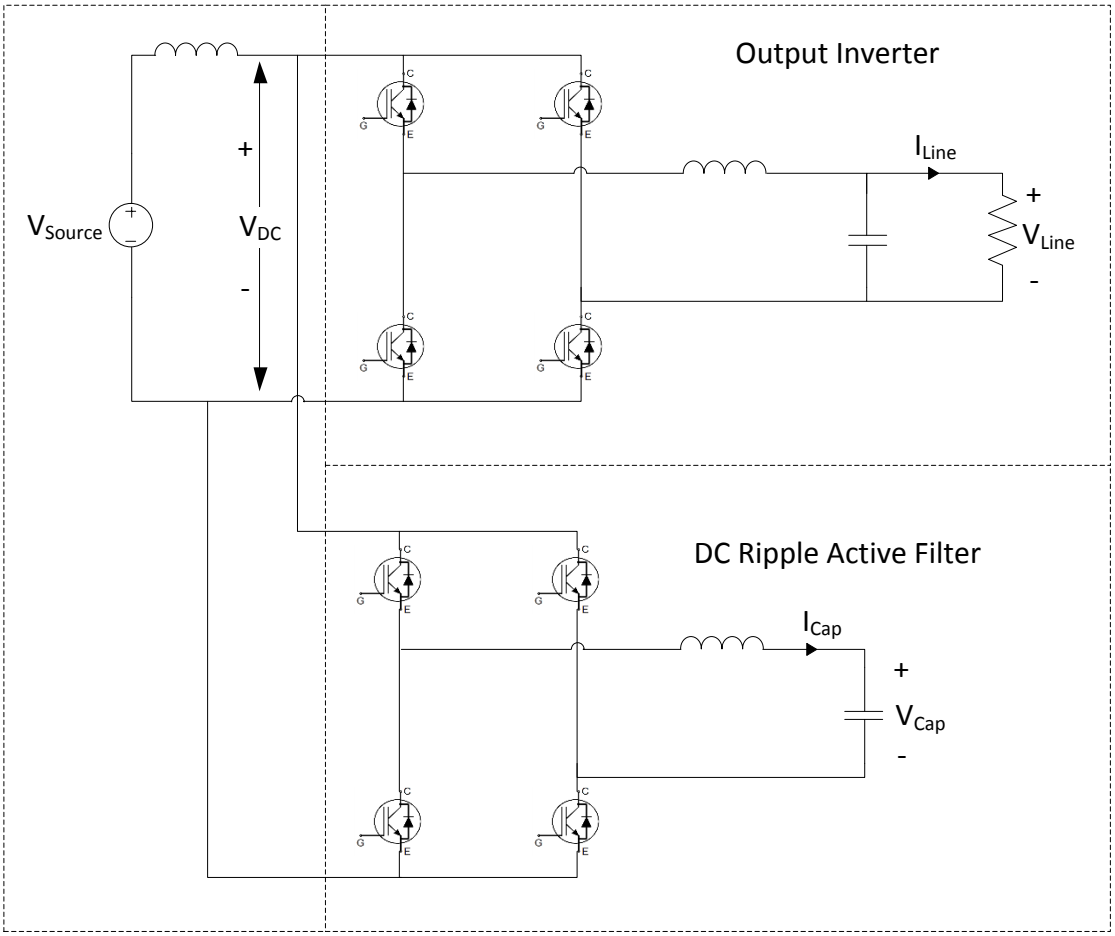


Figure 5-7: Topology and configuration of simulation setup.

As seen in the figure above, a small inductance has been placed in series with the voltage source. This has been done to weaken the ideal source so that the simulation results are closer to real-world application. An inductance value of 1 mH has been chosen as it is a real-world possible value that that can be found in DC sources.

In the plots below, the resulting power is calculated by adding the instantaneous values of the inverter power with the instantaneous value of the capacitor power.

5.3.1 *Simulation Results of Solution Two (80 µF Capacitor)*

In the simulation, the results and conclusions are based on the converter as a whole, including the inverter and the active filter. For this reason, the plots will illustrate both of the inverter and filter variables on the same axis, and then the net effect of those variables in the system thereafter.

The first simulation is done on the case study where the capacitance was calculated to be 80 µF and a minimum required voltage of 29.07 V. The relevant plots can be seen below.

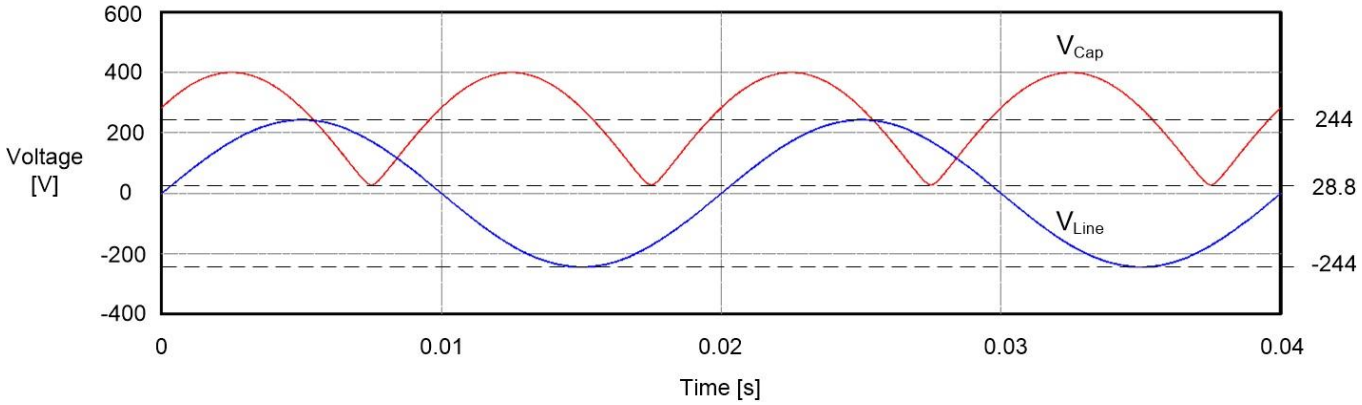


Figure 5-8: Solution Two comparison between the inverter output line voltage and the active filter capacitor voltage.

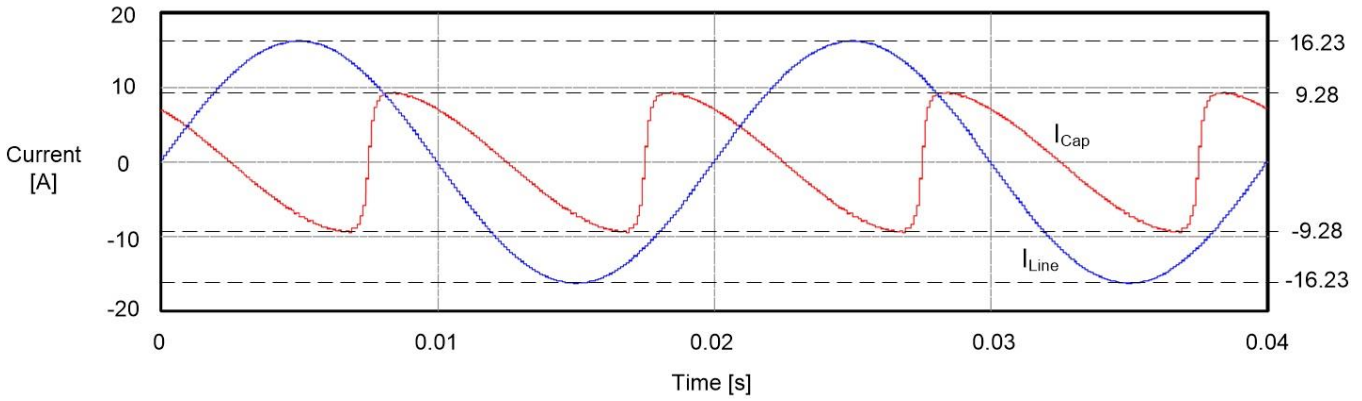


Figure 5-9: Solution Two current comparison between the inverter output line current and the active filter capacitor current.

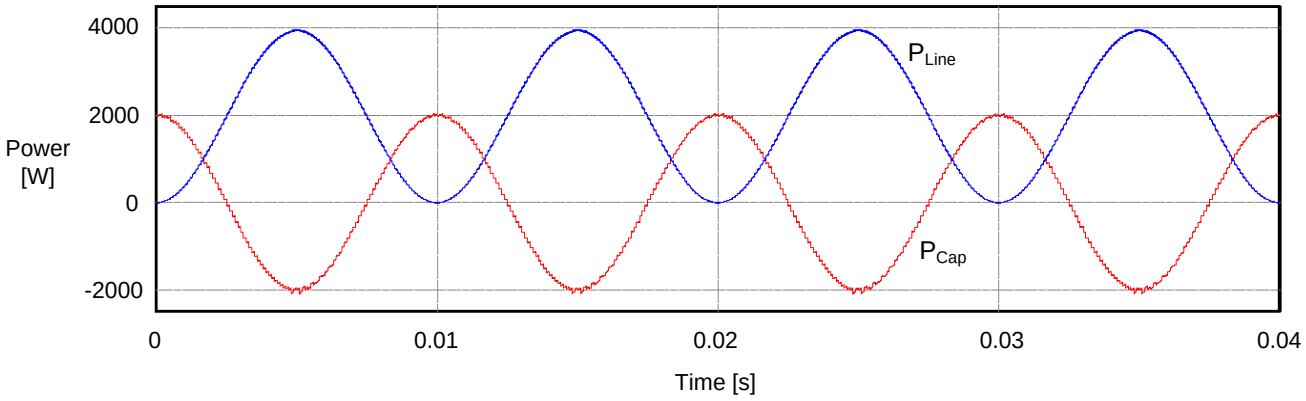


Figure 5-10: Solution Two power comparison between the inverter output line power and the active filter capacitor power.

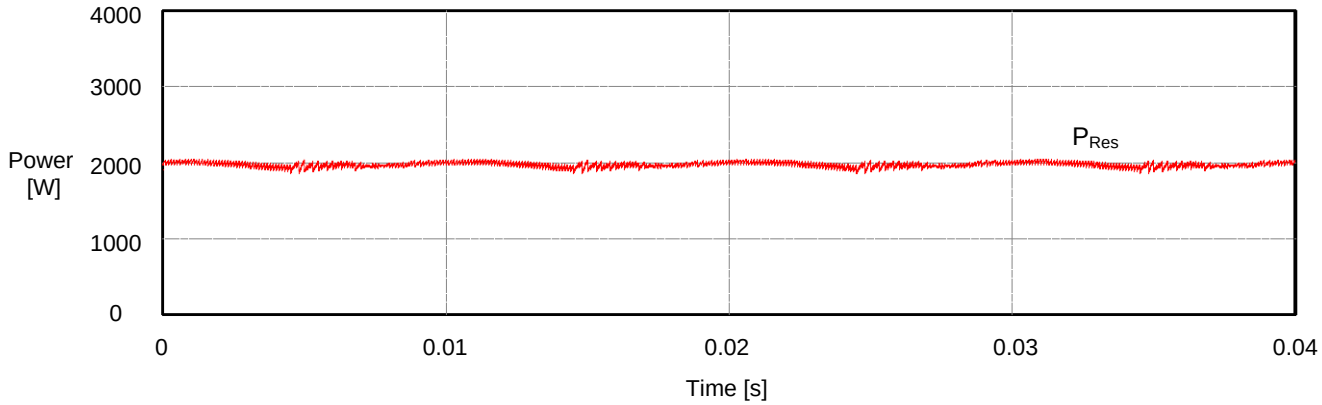


Figure 5-11: Solution Two resulting power.

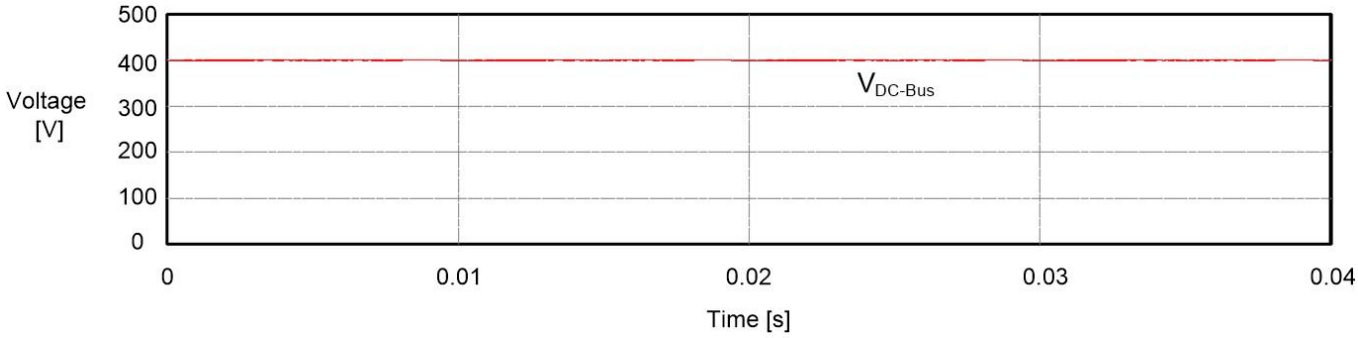


Figure 5-12: Solution Two resulting DC-Bus voltage.

From the plots above it can be seen that the results are as expected and predicted by the mathematical model.

5.3.2 *Simulation Results of Solution Three (120 µF Capacitor)*

The second simulation is done on the case study, where the capacitance was calculated to be 120 µF and a minimum required minimum voltage of 232.2V. The relevant plots can be seen below.

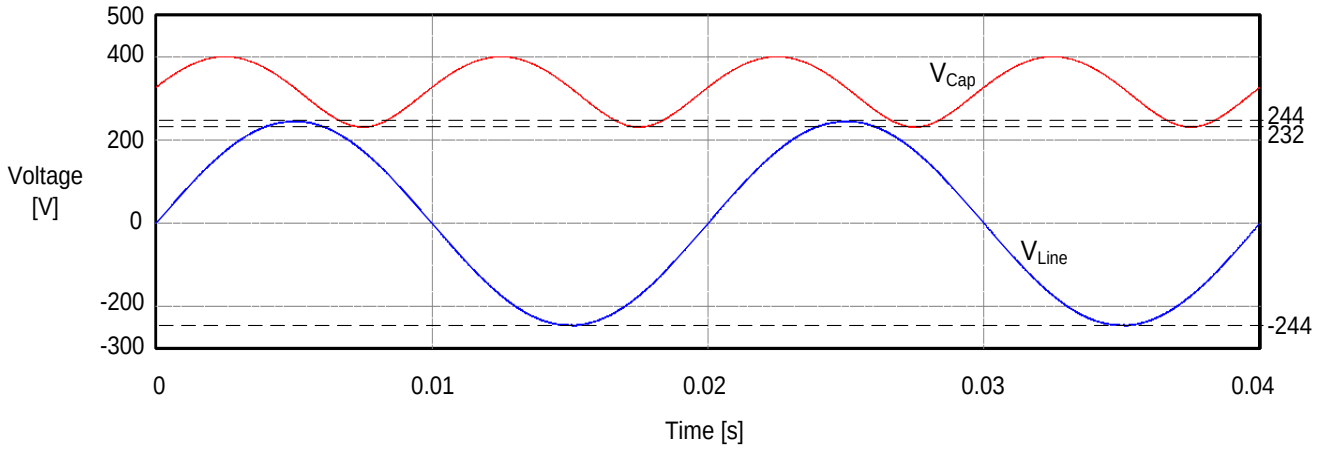


Figure 5-13: Solution Three voltage comparison between the inverter output line voltage and the active filter capacitor voltage.

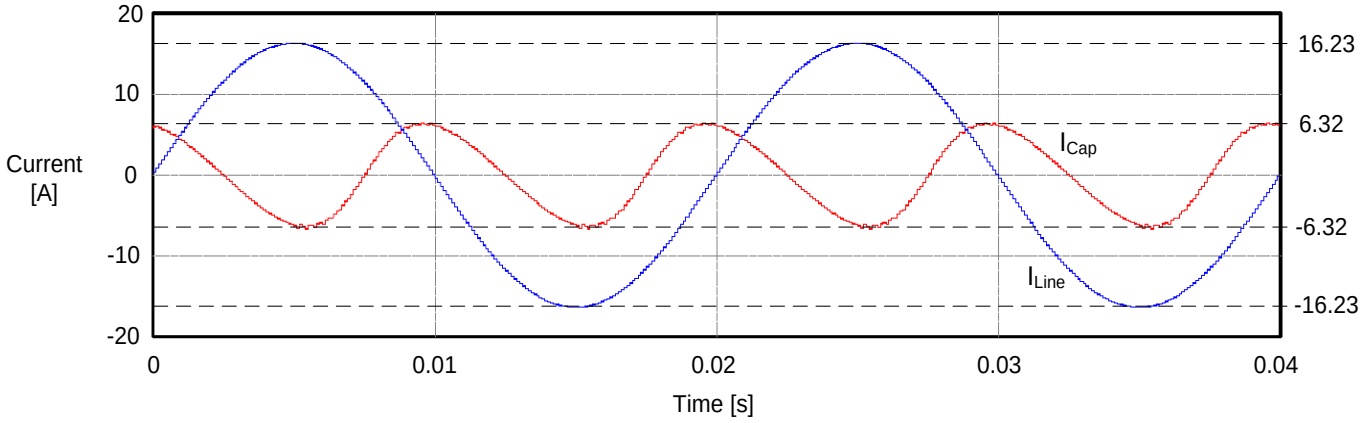


Figure 5-14: Solution Three current comparison between the inverter output line current and the active filter capacitor current.

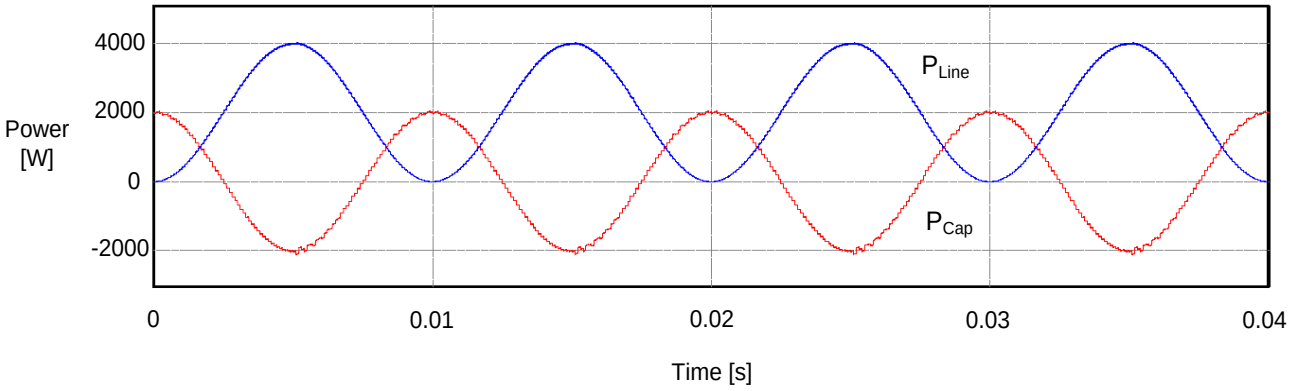


Figure 5-15: Solution Three power comparison between the inverter output line power and the active filter capacitor power.

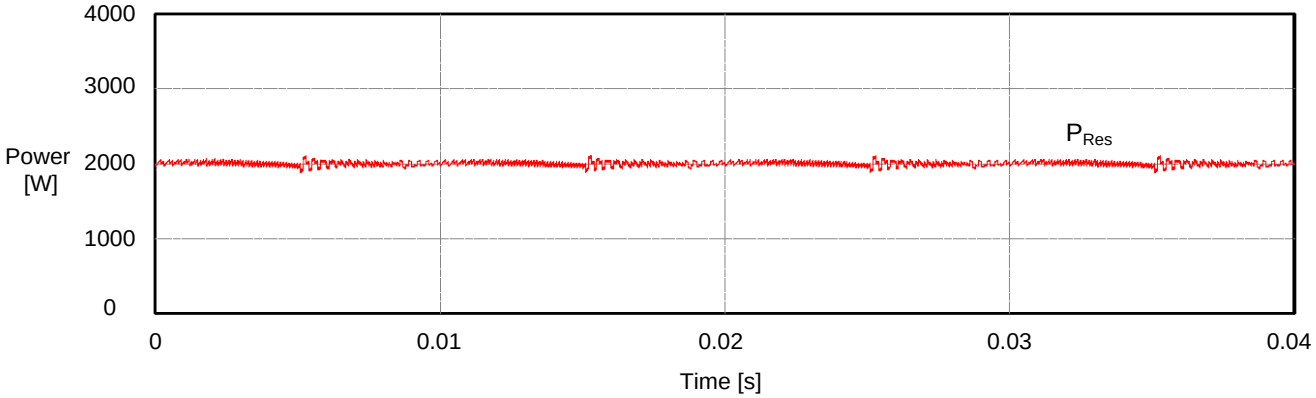


Figure 5-16: Solution Three resulting power.

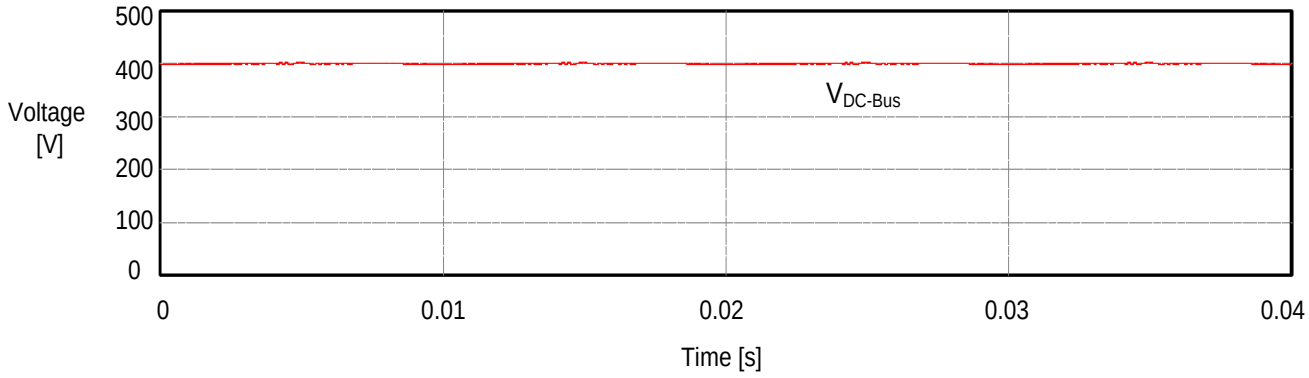


Figure 5-17: Solution Three DC-bus resulting voltage.

It can be seen that all of the results obtained from the simulation results are as expected from the general solution model.

5.4 COMPARISON AND RESULTS DISCUSSION

5.4.1 *Trade-off Comparison*

Chapter 3 and Chapter 4 describes and discusses the trade-offs between minimum capacitor voltage, capacitance and losses that a designer can choose when utilising the general solution presented. In Figure 5-18 below, these trade-offs of Solution two and Solution Three are illustrated and compared.

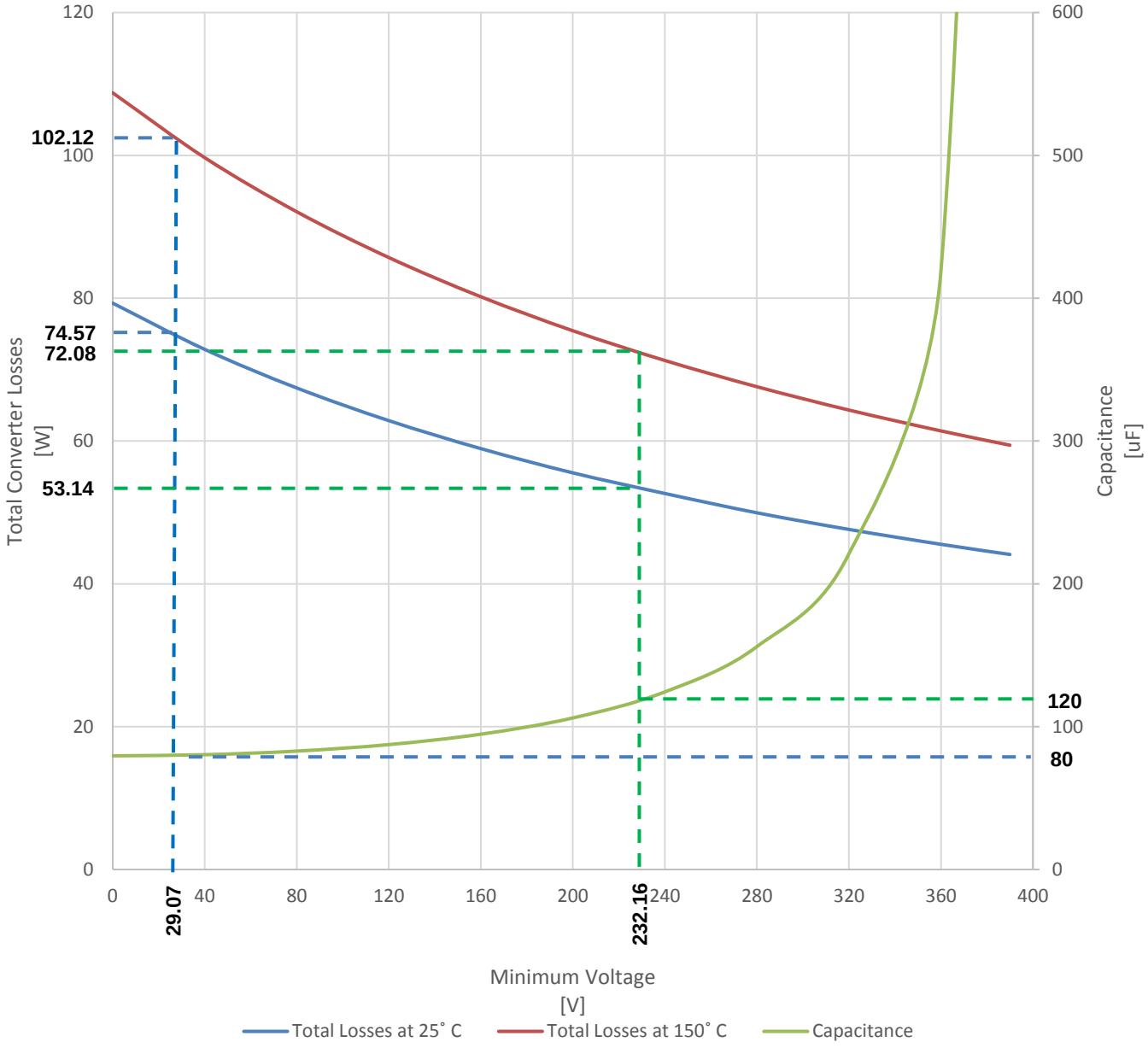


Figure 5-18: Trade-offs illustration between converter losses, capacitance and capacitor voltage of Solution Two and Solution Three

From the figure above the advantages and disadvantages can clearly be seen when the minimum capacitor voltage is chosen at the different indicated points. The figure above supports and verifies the statements made in Chapter 3 and Chapter 4 about the choice of voltage variation.

A noticeable conclusion seen in the figure is how a small increase in capacitor volume, can greatly decrease the losses of the converter, but only up to a point. Even

though only two set points on the graph is illustrated, the graph is applicable to the entire operating range with real life values included.

5.4.2 *Capacitor Comparison*

From the results above, it can be seen that it is possible to replace the electrolytic capacitor with a film capacitor using the general solution while still achieving the desired goals.

In Table 6 below is a full comparison of all of the chosen capacitors for the different solutions.

Table 6: Overall Capacitor Comparison

	Solution One	Solution Two	Solution Three
Filter Type	Passive	Active	Active
Capacitor Type	Electrolytic	Film	Film
Manufacturer	Kemet	Illinois Capacitor	Illinois Capacitor
Capacitance	1,5 mF	80 µF	120 µF
Rated Voltage	550 V	700 V	700 V
Voltage Variation	394.7 V to 405.3 V	29.07 V to 400 V	232.16 V to 400 V
Series Resistance	204 mΩ @ 100 Hz	2.6 mΩ @ 100 kHz	1.3 mΩ @ 100 kHz
Dimensions	66mm (D) × 115mm (H)	57.5mm (L) × 57.5mm (B) × 38mm (H)	57.5mm (L) × 57.5mm (B) × 38mm (H) + 57.5mm (L) × 45mm (B) × 30mm (H)
Volume	393.4 cm^3	125.6 cm^3	203.2 cm^3

Several interesting conclusions can be made from the capacitor comparison. The first is the large difference in the equivalent series resistance between the electrolytic capacitor and the film capacitors. The series resistance of the electrolytic capacitor is roughly 150 times larger than the film capacitors, as predicted from the capacitor study. It is mainly this resistance value that greatly reduces the reliability of the

electrolytic capacitor. The value of this resistance is also given at the correct approximate frequency at which the different capacitors are made to operate.

The capacitance of the film capacitors are 18.75 and 12.5 times less than that of the electrolytic capacitor, respectively, but the volume is only 3.13 and 1.94 times smaller. This is because of the very large difference in energy density between film capacitors and electrolytic capacitors.

The difference in volume between the capacitors from Solution One and Solution Two is 267.8 cm^3. It must be noted that the calculated volume does not include the volume of the converter and required cooling of the converter. The volume of the required heatsink would be subject to several design parameters to determine the effectiveness of the heatsink.

If old and ineffective cooling techniques are implemented to address the issue of cooling, the overall volume of the solution could overtake the volume of a simple passive filter, losing the benefit of volume reduction, but still keeping the benefit of the elimination of electrolytic capacitors. The matter of cooling requirements in this regard is subject to the designer and the choice of cooling method.

All of the capacitors have a chosen voltage safety factor, with the electrolytic capacitor having the smallest safety factor.

5.4.3 *Active Filtering Solutions Comparison*

The most notable difference in the capacitor voltage plot is the large difference in voltage variation, while the capacitance only differs by 33%. As previously stated, the voltage variation must be kept as small as possible to simplify the converter design and control. Even though in the example presented, the voltage in not driven all the way down to zero volt, the change from 400V down to 29 V is still a very large ratio between the input and output voltage.

From the current plots, the advantages of the smaller voltage variation can also be seen. The maximum current is significantly less in the choice of a higher minimum voltage, placing less stress on the converter components and directly translating to lower losses.

An interesting point noted is that when the voltage is driven down to zero, it would be very hard to implement and achieve ideal ripple cancelation. It is seen that a capacitance change of only 0.4225 µF caused the minimum voltage to change from 0 to 29 V. This equates to a 7.25% change in minimum voltage, but only a 0.53% change in capacitance. The conclusion made is that the absolute perfect capacitance will then have to be implemented for ideal ripple cancelation when a minimum capacitor voltage of 0V is chosen.

6 CONCLUSION

6.1 SUMMARY

To solve the problem of instantaneous power mismatch, a very large electrolytic capacitor is usually implemented because of its large energy density compared to other capacitors. It is known that these electrolytic capacitors traditionally have a short lifetime and are prone to failure. Film capacitors would be a good replacement, but unfortunately have low energy densities.

This research proposes a general solution from a fundamental approach of how the power processed by a capacitor can be better defined and then also better addressed, to solve the problem of instantaneous power mismatch in single phase inverters.

A general solution is derived from the laws of conservation of energy to lower the required capacitance enough so that electrolytic capacitors are no longer required and can be replaced by film capacitors. Because of the fundamental approach, this technique is applicable to all converters and methods that solve the problem of instantaneous power mismatch in single phase inverters.

A mathematical model is presented to validate that this approach is applicable to passive and active filters. The method is then applied to the direct capacitor power control of the ripple port and is optimised to enable the use of a capacitance that is very close to the minimum possible capacitance, but with smaller voltage variation and voltage and current waveforms that are much easier to achieve practically. A plot of the trade-off between capacitor voltage variation, capacitance and converter losses is also presented to enable the designer to choose an optimum point of operation.

A general design procedure is also introduced to visually illustrate how a designer can apply the model with an arbitrary converter and components and being able to define the capacitor voltage variation as the designer sees fit. The model is then applied to three different practical scenarios, which include passive and active filter examples.

6.2 CONCLUSION

The mathematics and simulations prove that the presented model is viable as an alternative approach to solve the problem of instantaneous power mismatch in single phase inverters. It is seen that the electrolytic capacitor can be eliminated using this method, whilst still maintaining comparable volume, even when the converter is included.

Film capacitors with a capacitance of 80 µF and 120 µF have been shown to solve the problem of instantaneous energy mismatch just as well as an electrolytic capacitor of 1.5 mF, with a volume that is 1.94 to 3.13 times smaller than the electrolytic capacitor, excluding the converter.

It is also seen that the presented graph, which illustrates the trade-offs between voltage variation, capacitance and converter losses, greatly simplifies the designer's choice of voltage variation. This illustrated graph is the main contribution to the scientific community and is a summary of all the presented work.

This research provides an alternative method of understanding the basics of power flow in capacitors and once it is better understood, the implemented solutions can be improved as well. This is seen in the waveforms as compared to the ripple port, where the voltage must be driven down to zero volt for ideal ripple cancelation. The main advantages found when the minimum voltage is not driven down to zero is:

a) Lower voltage variation
b) Lower maximum current
c) Less stress on the converter
d) Easier converter design and control
e) Lower losses

6.3 FUTURE WORK

A valuable contribution can be made to see where else the model can be put to effective use, as in the case of the decoupling of the capacitor in single phase

inverters. This whole model would apply to inductors as well, but instead of controlling the voltage to force a power waveform, one would control the current.

Future work on the fundamental model can also be done by adding experimental results, and the required control aspects under step changes.

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