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# A Review of the Experimental Performance of Turn-Off Methods in Wide Bandgap Semiconductors

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**ABSTRACT** Wide Bandgap devices are becoming more popular because of their higher switching performance. However, this higher performance comes at the cost of increased susceptibility to parasitic effects and leads to problems such as voltage overshoot and ringing of the switching node. Many strategies have been described in the literature that suppress these undesirable effects and enable faster switching. Generally, the literature describes the effectiveness of a new suppression method by experimentally comparing the outcomes when the strategy is used versus when it is not used. However there is no study that compares experimental results of the many different reported strategies with each other. This work is a meta-analysis of previously reported experimental results of WBG devices that compare the different reported strategies against one another. This shows which class of strategy holds the most promise for future development. The data presented also enables future strategies to be benchmarked against the current state-of-the-art.

**INDEX TERMS** Experimental comparison, fast-switching devices, oscillation suppression methods, wide bandgap (WBG) devices.

## I. INTRODUCTION

Silicon semiconductor technology has been the basis of the development of the field of power electronics almost since its inception. With the development of the Thyristor in the 1960s and subsequently BJTs, MOSFETs, and IGBTs, Silicon has enabled the advances. Unfortunately, Silicon semiconductor technology is now seen as mature and has reached its full potential [1], [2], [3], [4].

However, wide bandgap (WBG) semiconductor devices (SiC and GaN) have taken over as the semiconductor material of choice for new technology. WBG devices have become more prevalent in state-of-the-art research because of the numerous advantages of their physical properties compared to their silicon predecessors [1], [5]. A comparison of these physical properties can be seen in Fig. 1.

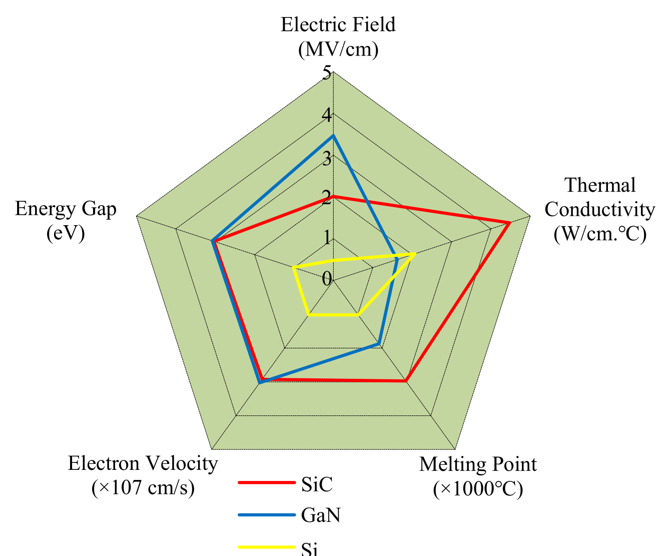


**FIGURE 1.** Summary of semiconductor material properties [1], [5].

The figure shows that WBG devices have a higher energy gap, electric field, and electron velocity than silicon devices. The main consequences of these physical improvements are that WBG devices are able to switch much faster than Si devices, at higher voltages, and operate at higher temperatures. The increased switching speed, represented by a higher *dv/dt*

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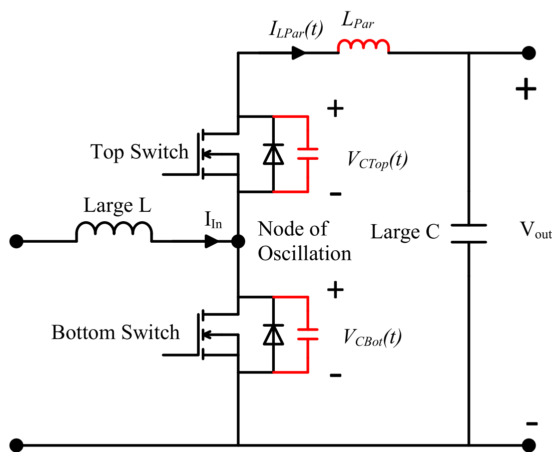


**FIGURE 2.** Representation of a commutation cell in power electronics.

or *di/dt*, enables several attractive advantages that have led to their popularity.

The main advantages of increasing switching speed are increased efficiency, increased switching frequency and increased energy density [6], [7], [8], [9].

Unfortunately, the increase in switching speed also increases several unwanted oscillations in the circuit [5], [10], of which the overshoot and ringing of the switching node are the most prominent that is caused by resonance between the parasitic components during the switching event.

To better understand this overshoot, an example of a phase arm or commutation cell can be seen in Fig. 2, with the circuit parasitic components illustrated in red. This circuit represents one of the most common functions in power electronics, where current in one semiconductor device is turned off and commutates to another device. The parasitic components may scale in size with different technologies but are a characteristic of the underlying physics. The impact of the parasitic components depends on the relative magnitudes of the switching speed of the semiconductor devices and the resonant frequencies of the parasitic components.

Many different non-ideal switching effects can arise from the presence of parasitic components. When the phase arm equivalent circuit of Fig. 2 is operating as a boost converter with power flowing from the left to the right, it is specifically the turn-off of the bottom switch and turn-on of the top switch that would cause an overvoltage and ringing across the bottom switch. When the turn-off of the bottom switch is slow, the overvoltage is small, and when the turn-off is fast, the overvoltage is large, as seen in Fig. 3.

It is important to note this problem is not a consequence of WBG devices but rather of the intrinsic parasitic components of a circuit in combination with the faster switching speed that WBG can offer. Fig. 2 could contain either SiC or GaN devices. The size of the parasitic components and the slope of the turn-off current in Fig. 3 could be different depending on the devices.

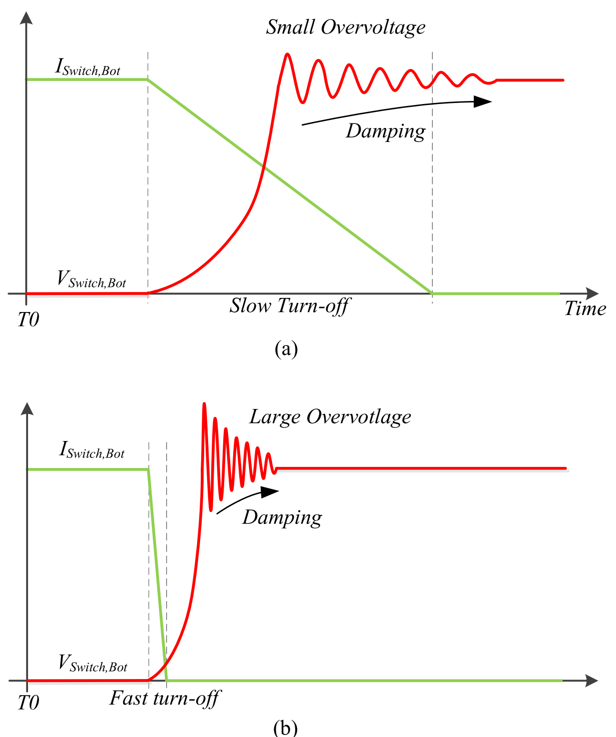


**FIGURE 3.** Comparison of the voltage overshoot of the switching node when switching (a) slow and (b) fast.

**TABLE 1.** Typical Structure of Oscillation Suppression Methods Article

| Section | Content of Section |
|---|---|
| 1 | Introduction |
| 2 | Analysis of some new oscillation suppression methods. |
| 3 | Simulation results |
| 4 | Experimental results |
| 5 | Comparison of experimental results with and without suppression method. |
| 6 | The conclusion was that the suppression method implementation was successful as the overshoot decreased from experimental results without the suppression method to the results with a suppression method. |

This overvoltage is a long-standing problem, and much research has gone into almost all aspects of it. A general structure of a typical overvoltage and oscillation suppression methods article in the literature has developed over a long time, but unfortunately, the final step of this could lead to irrelevant results. This article structure generally follows the outline in Table 1

In this standard presentation of results, the conclusion in such an article is generally made that the research is successful as the experimental results with the suppression method have a lower overshoot than the results without the suppression method. However, these results are never directly or indirectly compared to other experimental results. As such, the actual relevance of the results is unknown, as they are not placed in

the context of other experimental results in the field. At best, some individual factors like inductance may be compared to a single other reference.

As there is no comparison with other reported results, it is difficult to decide whether to continue to develop and refine a specific method or if some other method offers better performance.

The work reported in this paper attempts to provide a framework to compare different overvoltage and oscillation suppression methods articles. It does so by extracting the relevant comparable information from previously reported experimental results. These experimental results are then compiled in a database from which the data can be interpreted from several different viewpoints.

This database can also be used by other researchers to easily compare their new experimental results with multiple previous experimental results.

The layout of this paper is as follows:

Section II is a summarised review of the overvoltage and oscillation suppression methods reported in the literature. Only papers on WBG devices have been used.

Section III provides the methodology for the extraction of the relevant information from the experimental results presented in the literature. An example of the information extraction process is provided.

Section IV introduces the table of the database of experimental results that is found in the Appendix, and discusses some considerations of the table.

Section V presents several different scatter plots of the comparisons of the experimental results, with a discussion of the observations.

Section VI provides the conclusion of the paper.

## II. EXISTING OSCILLATION SUPPRESSION METHODS

All of the existing oscillation suppression methods are, in essence, different approaches to solving the same problem, and the approaches can vary significantly. Generally, all the methods reported in the literature have successfully solved the problem of overshoot and ringing for the switching speed investigated.

It must be noted that these methods indirectly change the efficiency of the converter by directly influencing the power waveforms. The two most prominent influences of these methods on the efficiency of the converter are 1) slowing the switching speed, which increases the switching losses, and 2) introducing additional circuit components like controllers in Active Gate Drivers and components in snubbers. The ideal implementation of a method when concerning efficiency would be not to reduce the switching speed while incorporating as few additional components as possible.

A summary of the existing oscillation suppression methods can be found in Table 2. In this table, a short discussion of the implementation, as well as the advantages and disadvantages, can be seen, together with the references that discuss the method. It is not the intention of this paper to critique the different approaches or to discuss them in any great detail. A good review of the methods themselves has been carried out in [5].

## III. EXPERIMENTAL RESULTS EXTRACTION METHODOLOGY

An article that describes an overvoltage and oscillation suppression method will normally show the waveforms of the switching devices both before and after the implementation of the method. These experimental results contain the information of interest. However, the results are normally only presented as oscillograms in the papers, and there is no other access to the waveform data. The relevant information presented in the various waveforms needs to be extracted, and the methodology used to process the published oscillograms is discussed in this section

### *A. RESEARCH ARTICLES INCLUDED IN THIS STUDY*

The articles included in this study were any and all that could be found that presented an overvoltage and oscillation suppression method, focusing on the past five years. Only well-cited papers older than five years were also included, and only WBG articles fitting this description were used.

Of these articles mentioned above, the main requirement for a paper to be included was that the turn-off voltage waveform had to be presented explicitly to extract the data. This means that the actual turn-off voltage waveform, zoomed in to show only one turn-off event and with division sizes, had to be presented. During this investigation, it was found that several of the oscillation suppression methods articles presented in Section II do not present the experimental results in this manner.

### *B. EXTRACTED DATA POINTS*

When the turn-off switching transition of a switch is considered, several characteristics can be extracted, and to ensure fairness and consistency in the comparison, all the results have been extracted in the same way.

The main data relevant to this study that could be extracted and subsequently compared from the experimental results waveform are:

1) Voltage Overshoot Percentage [%] - This is the percentage of how much larger the maximum voltage is over settling DC voltage after the oscillation has subsided.
2) Voltage switching speed or slew rate [V/ns] – this is the average rate at which the voltage over the switch progresses from 10% to 90% of the full voltage range.
3) Power loop inductance – this is the experimental power loop parasitic inductance measured indirectly from the switching oscillation frequency.

The voltage overshoot percentage is used instead of the actual overshoot to compensate for the differences in DC voltage, and the average switching speed from 10% to 90% is used for the same reason. These three datapoints are then compared to each other at the same time to be able to make a conclusion on the effectiveness of a specific result. Weighting factors could be added in this comparison step, but, at the

**TABLE 2. Oscillation Suppression Methods Summary**

| Oscillation Suppression Method | Implementation | Advantages | Disadvantages | References |
|---|---|---|---|---|
| Minimisation of parasitic inductance | • Reduction of power loop inductance by:<br>○ Power loop layout optimisation<br>○ Packaging optimisation<br>○ Component selection | • Very Effective<br>• Easy to understand<br>• Component selection is simple to implement | • Layout optimisation can become very complicated<br>• The parasitic inductance can never be reduced to zero. | [10], [11], [12], [13], [14], [15], [16], [17], [18] |
| Slower switching | • A resistor on the gate terminal or a slower slew rate of the gate driver | • Simple to implement | • Not very effective in reducing oscillations<br>• Increase in switching losses | [14], [19] |
| Ferrite Beads | • Adding a high-frequency dependent resistor | • Simple to implement<br>• cost-effective<br>• passive | • Much better at decreasing oscillation duration than a reduction of maximum voltage<br>• Slightly increased losses | [14], [19], [20] |
| Active Gate Driver | • Control voltage, current or impedance of the gate terminal of the semiconductor device | • Several papers have been very effective<br>• Very flexible solution | • Potentially highly complex<br>• Higher cost of more components | [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36] |
| RC Snubbers | • Adding circuit components to create a critically damped system at the ringing frequency | • Simple to implement<br>• cost-effective<br>• passive<br>• High order can be very effective | • Lower order has minimal oscillation suppression<br>• Slightly increased losses<br>• Higher order can be complicated to calculate and design | [20], [37], [38], [39], [40], [41], [42], [43], [44], [45] |
| Zero Overvoltage Switching | • Increase switching speed and inductance according to an optimisation condition. | • The only method that becomes more effective when switching faster | • A very narrow window of operation<br>• A small change in current or voltage creates a large overshoot<br>• This is only possible at very high switching speeds | [46], [47], [48] |
| RC Clamping | • Similar to RC Snubber, but with more components<br>• Symmetrical structure | • Reduced Switching losses compared to RC Snubber<br>• Effective reduction of overshoot<br>• Passive | • Effective implementation can be complicated and difficult | [49], [50] |
| External RLC Resonator | • Magnetic coupling through an external resonator in parallel to the main circuit bus bar. | • Effective suppression<br>• No Components are inserted in the switching circuit, so reliability is ensured. | • Complicated implementation based on non-Hermitian parity-time (PT) symmetry | [51], [52] |

moment, it is thought that weighting factors could cloud the raw results, and to argue for a fair application of weighting factors would be difficult but could be done in future research.

This data cannot be simply read from the plots provided in the papers, and the published oscillograms needed to be digitised before the values could be calculated. Additionally, the experimental results, both with and without a suppression method, were processed where possible.

### *C. DATA EXTRACTION EXAMPLE*

The example of the step-by-step methodology is discussed below using [19] where a simple gate resistor is implemented to switch slower and thereby suppress the overshoot and oscillation. Even though the example is presented for a SiC semiconductor, precisely the same process is relevant to GaN devices as well.

*Step 1:* Digitise the waveform from a high-definition IEEE Xplore image

In this step, the voltage waveform, presented in as high-definition as possible, is converted to a digital waveform by plotting data points on the graph. Online software that can convert multiple points to x and y coordinate values was used to assist in this process. The image of how the experimental results are presented in [19] can be seen in Fig. 4 before digitisation, and the image after digitisation can be seen in Fig. 5.

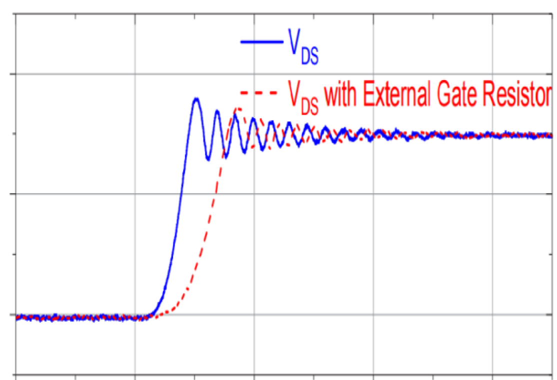


**FIGURE 4. Example of an image voltage turn-off waveform that could be converted to a data point before digitisation [19].**

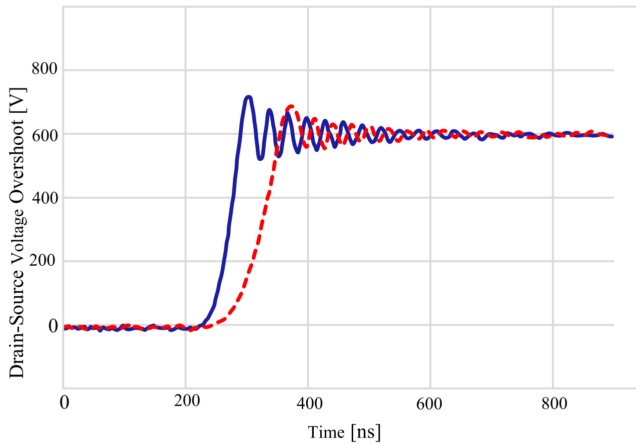


FIGURE 5. Example of an image voltage turn-off waveform that could be converted to a data point after digitisation [19].

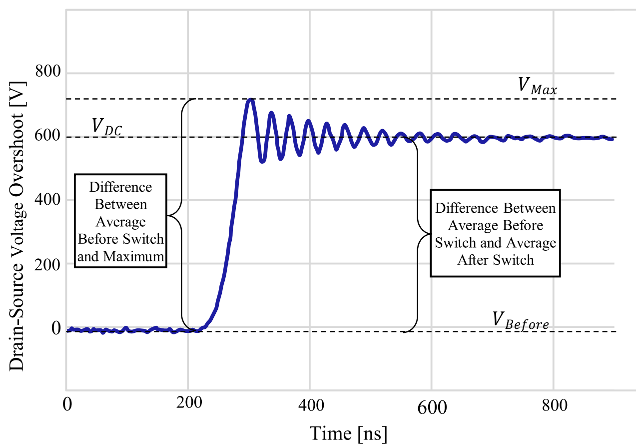


FIGURE 6. Example of the extraction of relevant parameters to calculate the percentage voltage overshoot (only shown for results without suppression method).

A manual data sample check is also performed in this step to verify the integrity of the data. For clarity, only the result without the suppression method will be discussed further.

*Step 2:* Voltage overshoot percentage calculation

For this step, three new values are defined to be able to calculate the percentage voltage overshoot, and they are as follows:

1) Average Voltage Before Switch - $V_{Before}$
2) Average DC settling Voltage after Switch - $V_{DC}$
3) Maximum Voltage - $V_{\text{Max}}$

These values can be seen in Fig. 6 and are then used to calculate the percentage voltage overshoot in the equation below:

$$\%OS = \frac{V_{\text{Max}} - V_{Before}}{V_{DC} - V_{Before}} \times 100 \quad (1)$$

In this equation, the difference between $V_{Before}$ and $V_{DC}$ has to be used to determine the DC voltage instead of simply using

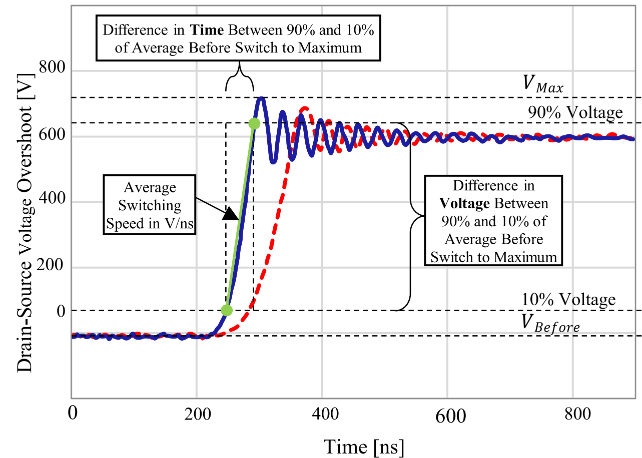


FIGURE 7. Example of the extraction of relevant parameters to calculate the switching speed.

$V_{DC}$.This is because several articles present the voltage plot without the 0 V indication directly from an oscilloscope and only with division markers, so the plot has to be compensated for a revised 0 V indication.

*Step 3:* Average switching speed (average slew rate)

After the overshoot has been calculated, the average switching speed or slew rate can be calculated. This is performed from 10% to 90% of the $V_{Before}$ to $V_{\text{Max}}$, and is done to calculate the speed of the entire range of the switching event. If the 10% to 90% of $V_{Before}$ to $V_{DC}$ was chosen to calculate the average switching speed, switching events with large overshoots would have seemed to perform better as the slow part of the switch was not included in the assessment area. This step can be seen in Fig. 7.

Firstly, voltage values of 10% and 90% need to be calculated. As the calculated voltage would fall between two data points of the digitisation process, the assumption is made that the voltage progresses linearly between these two points as they are close enough together. The slope between the points can be used to calculate the corresponding voltage and time stamp for the 10% and 90% values for both the results with and without a suppression method.

*Step 4:* Power loop inductance

The power loop inductance can be calculated from the ringing frequency of the voltage waveform if the circuit capacitance is known. For this step, the ringing period is found. This is done by extracting the period from the first trough to the second trough of the voltage waveform, as seen in Fig. 8.

It was found that using the first and second troughs leads to the most reliable indication of the ringing frequency. Thereafter, the capacitance of the power loop is required. This is output capacitance ($C_{OSS}$) of the $C_{Switch}$ value seen in Fig. 2, which is part of the resonant circuit. This value can be read from the datasheet of the device used in the experiment. In this case, the SiC MOSFET SCT3040KL is used, and using the settling voltage, the capacitance can be read from the

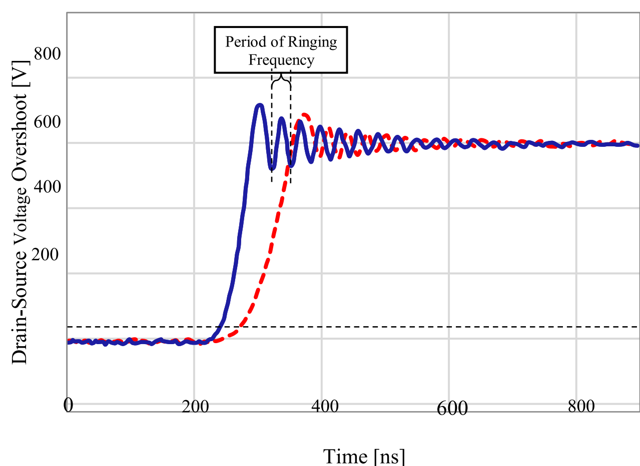


**FIGURE 8.** An example is ringing period extraction to calculate parasitic inductance.

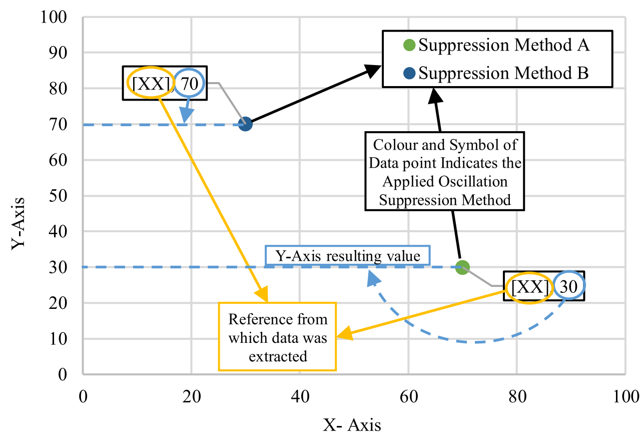


**FIGURE 9.** Example of the presentation of the experimental results scatter plots in Section V.

manufacturer's datasheet. For the purposes of extracting the power loop inductance, the device capacitance was considered linear. Other contributing factors to the overall capacitance were neglected, as it was assumed that the device capacitance dominated.

Using the method and equation from [53], the inductance can be calculated with the equation below:

$$L_{Loop} = \frac{{T_{Ring}}^2}{4\pi^2 \times C_{OSS}} \tag{2}$$

## IV. EXPERIMENTAL RESULTS TABLE PRESENTATION

Using the method described in Section III all the articles that met the requirements were processed for both the before and after suppression method implementation. The data points are recorded in Table 3 in the Appendix.

Additional Notes on this table include:

1) Where only results with a suppression method were presented in the research paper, the results without a suppression method section are left blank.
2) In comparison plots in Section V, only results with the suppression method are presented.
3) Where the inductance is measured in the results without a suppression method, it is not repeated in results with a suppression method.
4) Several references present more than one oscillation suppression method result, so more than one data point could be extracted.
5) In [53], no oscillation suppression method is implemented, as this paper only presents a method to calculate and confirm parasitic inductance. However, this article does present an additional data point.

## V. EXPERIMENTAL RESULTS INVESTIGATION

This section analyses the data in Table 3 from several different points of view. The experimental data from each paper has been extracted and reduced to several numbers in the table. It would not be fair to compare the numbers in the table directly with each other. The data in the table were extracted from measurements of converter circuits that were normally designed with a specific application in mind. In this sense, the switching data is secondary to the actual application. Each of the papers describes a different application with different operating conditions and is implemented with different levels of engineering rigour. The data in Table 3 needs careful interpretation. However, viewing a sufficient number of data points gives insight into the trend of progress in the field.

The data are analysed in three ways: Firstly, to show the effectiveness of different suppression methods on the overshoot and device switching speed. Then the influence of the operational characteristics such as the switching voltage and parasitic inductance and then the trend towards faster switching speeds over the past decade.

For each of the data points plotted in this section, the colour and symbol show the suppression method. Each data point is labelled with the reference from which it was extracted and the Y-axis variable. No distinction is made between GaN and SiC results. A simplified key to reading the scatter plots can be seen in Fig. 9

### A. COMPARISON OF OSCILLATION SUPPRESSION METHODS

#### 1) PERCENTAGE OVERSHOOT VS SWITCHING SPEED

The first section is the direct comparison of the voltage overshoot percentage and the switching speed in V/ns. This comparison allows the results of a single article to be compared with all the other articles. This is shown in Fig. 10.

It is generally accepted that fast switching speeds lead to large overshoots. Therefore, a fast switching speed with a low overshoot is seen as a more successful implementation of a suppression method. This is seen in the outlier of [18] in Fig. 10. Conversely, the outlier of [41] shows a less effective suppression method as the switching speed is relatively slower and the overshoot is substantial.

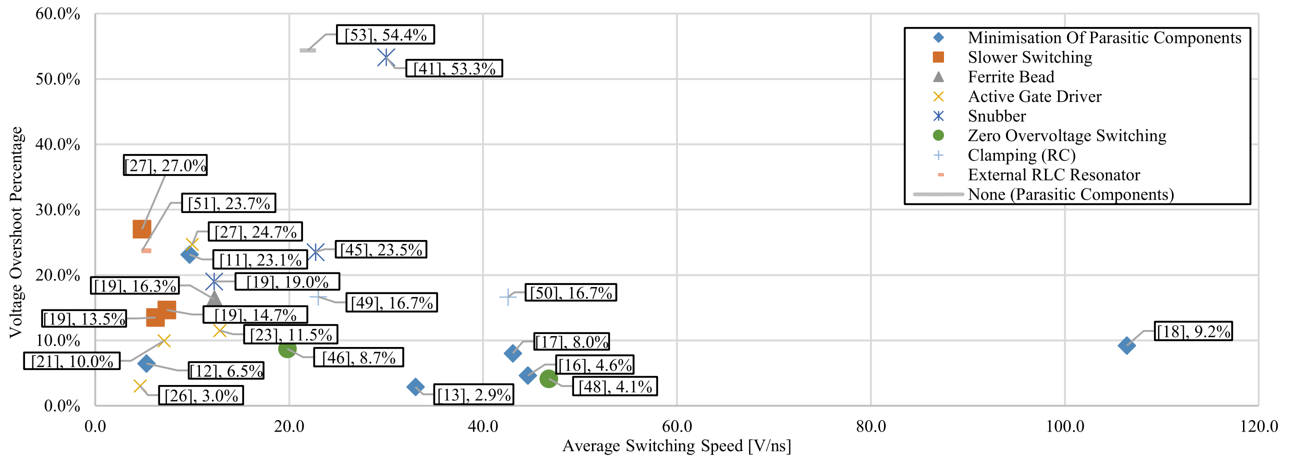


FIGURE 10. Scatter plot of voltage overshoot percentage versus average switching speed.

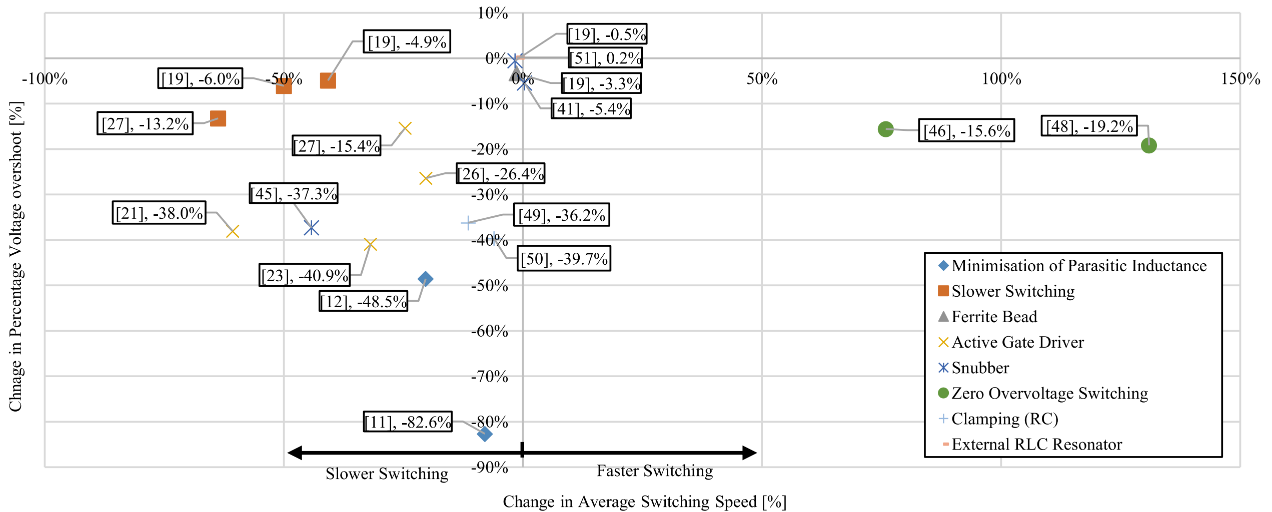


FIGURE 11. Scatter plot of change in percentage voltage overshoot versus change in switching speed from results without suppression method to results with a suppression method.

It can be seen that some of the suppression methods cluster together. For example, the active gate driver [21], [23], [26], [27] and the slower switch of [19], [27] and the parasitic reduction methods of [13], [16], [17]. While there is no definitive pattern emerging, the parasitic reduction methods show good performance in this view of the results. In particular, the apparent exceptional performance of [18] bears closer scrutiny. However, it is not within the scope of the current paper to delve into possible reasons for this high performance.

The data presented in Fig. 10 allows new suppression methods to be compared to the existing ones. In this way new results can be more readily interpreted as to their effectiveness.

### 2) CHANGE IN OVERSHOOT VS CHANGE IN SWITCHING SPEED

In many articles, the implementation of a suppression method is contrasted against the same circuit without the suppression method present. In all cases the suppression method is shown to increase the performance of the circuit. To capture this type of result, the percentage change in overshoot is plotted against the percentage change in switching speed, shown in Fig. 11. To interpret this plot, consider first the three orange (square) clustered points of [19] and [27], representing the suppression method of slower switching. As is known, slower switching speeds lead to lower overshoots. As almost all suppression methods sacrifice switching speed to reduce the overshoot, the other method's results can be compared to the slower switching method to determine their relative success.

However it can be seen that the Zero Overvoltage Switching method has the characteristic that it increases the switching speed and reduces the overshoot, against conventional expectations. This indicates that this method might be well suited to handle future fast-switching devices.

One of the main findings of the comparison plots of Figs. 10 and 11 shows that scoring well in the change measurement (Fig. 11) does not automatically imply that the result

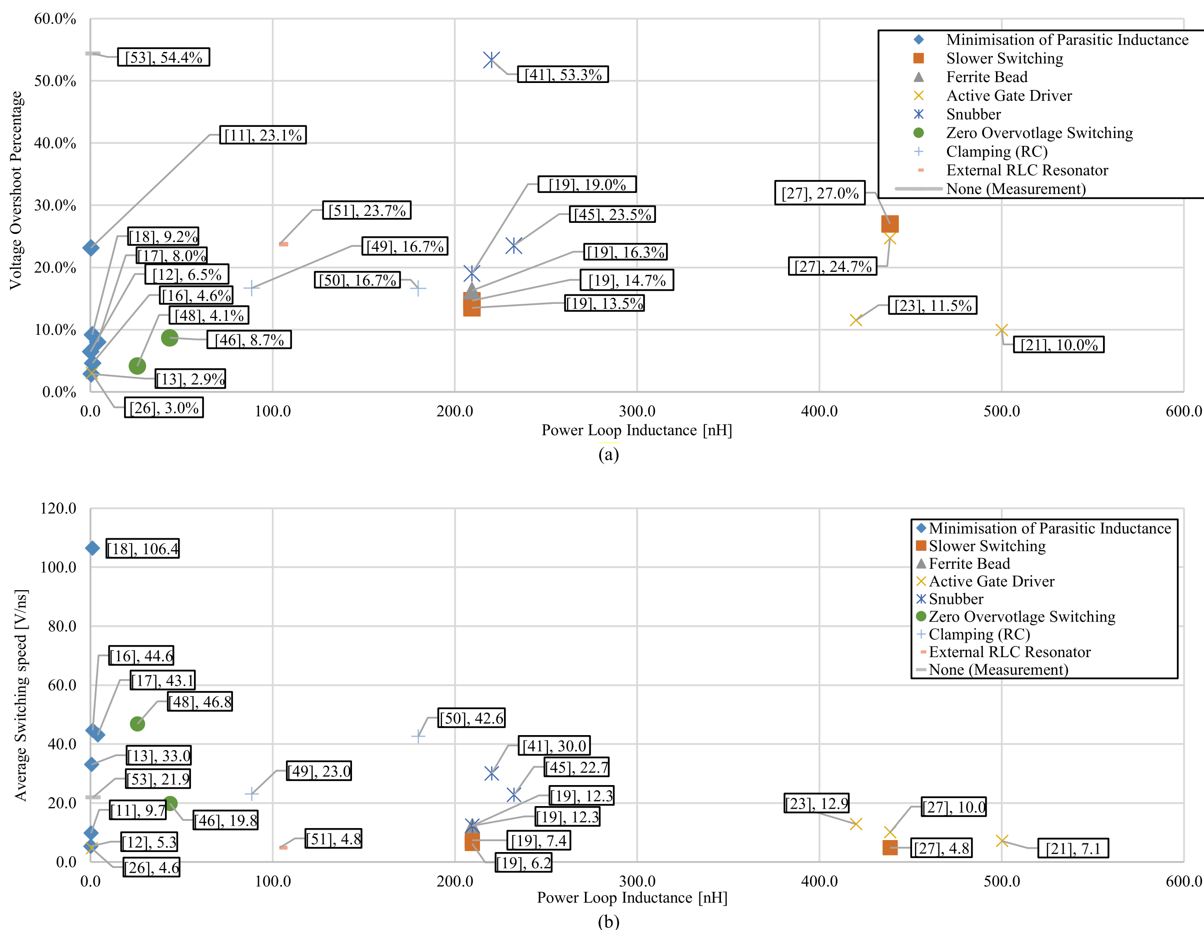


**FIGURE 12.** Scatter plot of the investigation of the influence of loop inductance on (a) voltage overshoot percentage and (b) average switching speed.

compares well overall, as was discussed in Section I. Even though a given experimental setup might benefit greatly from a suppression method, the overall result still might not compare well with other methods.

An example of this can be seen in [11], where the inductance is minimised. In this result in Fig. 11, an overshoot reduction of 82.6% is achieved, and only 8% switching speed is sacrificed, which could be considered a very good result. However, when this result is seen in Fig. 10, compared to other results, it has a relatively slow switching speed and a relatively large overshoot. Conversely, if a result like [18], can be improved only marginally, the improvement itself would be unimpressive, but the actual result would be exceptional.

### B. INFLUENCE OF CIRCUIT PARAMETERS

#### 1) INFLUENCE OF INDUCTANCE ON OVERSHOOT AND SWITCHING SPEED

It is well known that the parasitic inductance in the power loop has a major influence on the voltage overshoot and, therefore, the allowable switching speed.

This has logically led to the suppression method, which minimises parasitic inductance to decrease the overshoot.

To verify this concept, the percentage voltage overshoot is plotted against the parasitic inductance in Fig. 12(a) and the switching speed against the parasitic inductance in Fig. 12(b).

When Fig. 12(a) is considered, it is expected that the data points should lean heavily to the right-hand side of the plot to represent a higher percentage overshoot when the inductance is higher. However this is seen not to be the case. It appears that there are several data points where the inductance is very low, but the overshoot is still very high, and there are cases where the parasitic inductance is very high, but the overshoot is not. Therefore, even though lowering parasitic inductance for a given circuit will reduce the overshoot, low parasitic inductance in isolation does not predict a high or a low overshoot. In Fig. 12(b), it can be seen that data points with high inductance tend to switch slower, and data points with lower inductance seem to switch faster, in general.

#### 2) INFLUENCE OF VOLTAGE AND POWER ON THE OVERSHOOT

In this section, the view that the overshoot would generally be higher in converters that have a higher DC voltage or power is investigated. This section tests this view by first plotting

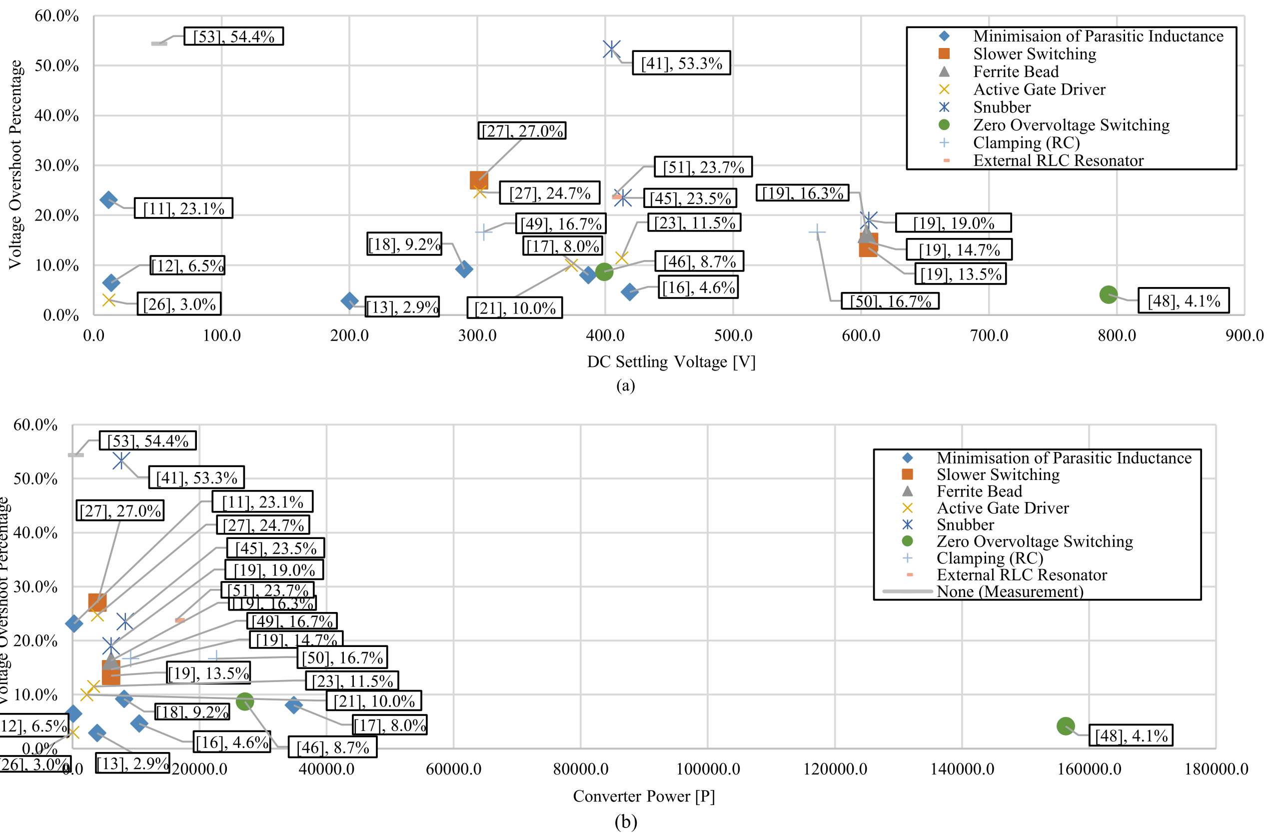


**FIGURE 13.** Scatter plot of the investigation of the correlation of (a) DC settling voltage and (b) converter power on the voltage overshoot percentage.

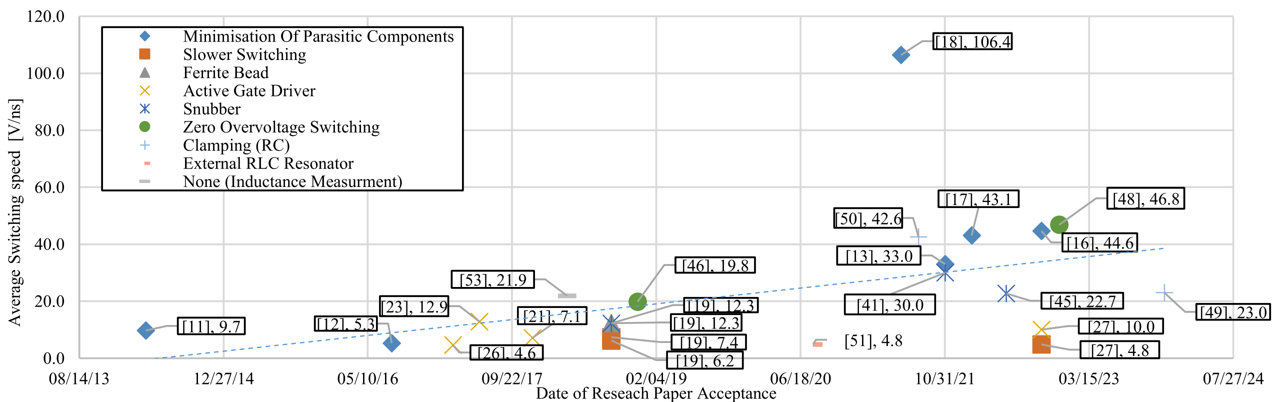


**FIGURE 14.** Scatter plot of average switching speed versus the date the article was accepted for publishing.

the voltage overshoot against the settling voltage in Fig. 13(a) and then plotting the voltage overshoot percentage against the converter's power in Fig. 13(b).

In these plots, it can be seen that there are several low DC voltage data points with high and low overshoots, as well as several high power data points with high and low overshoots.

This indicates that there is a very weak correlation between the overshoot and the voltage or power of a converter, and the general expectation that higher DC voltages or higher power could cause higher overvoltages does not seem to be true in general.

### C. FUTURE DIRECTION OF HIGH-SPEED POWER ELECTRONICS

The switching speed is plotted versus the date the research was accepted for publication in Fig. 14. It is easy to see that the

general trend over the past decade has been towards technology that enables higher switching speed. This is already well known. However, most of the articles used to extract the data from this work were based on real applications. Therefore, the trend shown in Fig. 14 is not only an idealised version of the pure devices but includes the complexities of the actual circuit.

Fig. 14 includes a trendline that shows an increase in switching speed of approximately 4 V/ns per year. This implies that if the trend continues, switching speeds may increase to between 50 V/ns and 100 V/ns over the next decade. Such a prediction is fraught with uncertainties, and the continuous increase in switch speeds may very well be countered by the associated increase in EMI. It may be that the switching speed plateaus over the next decade.

However, if the trend does continue to increase, it is questionable whether or not the currently used suppression methods would still be appropriate. From the graph of Fig. 12(a), the only suppression method amenable to increasing switching frequency is the Zero Overvoltage Switching method of [46], [48]. However, this method is still in its infancy, and much work is needed to demonstrate its full potential both theoretically [54] and practically.

### D. GAN VERSUS SIC DISCUSSION

Even though this research does not focus on the differences between SiC and GaN, the raw results in the appendix could be used for an in-depth future comparison.

However, it can be seen that the average switching speed of SiC devices is 16.7 V/ns versus 37.7 V/ns of GaN, and the average DC voltage of SiC is 444.5 V versus 196.1 V of GaN. These results are as expected as GaN can switch faster than SiC and is generally used at higher voltage.

When the average overshoot is considered, it is seen that the SiC devices have an average overshoot of 18%, and GaN has an overshoot of 14%, which is considered too small a difference to be statistically relevant.

These two materials generally have different areas of application, but both suffer from overvoltage problems due to fast switching. From the data, there is no indication that a certain type of overvoltage suppression method is more favourable for either GaN or SiC.

The semiconductor material does not directly influence the overshoot other than possibly introducing a change in the parasitic switch inductance and capacitance. The overshoot is a consequence of the electromagnetic environment around the switch coupled with its fast speed. Therefore, it is not expected that the material will influence the overshoot or the suppression methods. Indeed, while this paper did not focus on older Si devices, it is expected that similar clustering of suppression methods could be expected.

The generality of the suppression methods implies that a given method could equally well be implemented on either GaN or SiC materials and, by extension, also on other materials.

## VI. DISCUSSION AND RECOMMENDATIONS

From the results, it can be seen that the minimisation of parasitic inductance yields the best results by far at the moment. This result makes sense as it directly addresses the root cause of the problem, but as mentioned, the main drawback of this method is that it will reach a natural limit.

The Active Gate Driver method also has promising results, as the overshoot could be lowered substantially without sacrificing too much of the switching speed. This method has been described as a “research hotspot” and is expected to remain a heavily researched area.

It is anticipated that that any significant progress can be divided into a medium term future and a long-term future. For the medium term future of five to ten years, it is expected that significant progress will lie in the hybrid application of minimisation of parasitic inductance with other methods, like Active Gate Driver. This will enable step-wise progression, but the parasitic inductance will still remain the major hurdle.

It is expected that the long-term future (more than ten years) will be in the application of a method where parasitic inductance is not the main obstacle. The only known method at the moment where parasitic inductance is not the main hurdle is Zero Overvoltage Switching. Methods like this will also enable the full potential of future faster-switching devices like ultra-wide bandgap devices.

## VII. CONCLUSION

This research reviews and compares the experimental results of several methods used to suppress the overvoltage and ringing of the switching node in WBG devices. A method to extract the relevant information from images of the turn-off voltage transition is presented and applied to all the resources that meet the requirements. A database of the results is included so that new methods can compare themselves against existing performance. The results in the database were plotted against each other, and the observations are summarised below:

1) Research articles that do not compare their experimental results to other experimental results in the field run the risk of not actually being as relevant as they expect. The single comparison of a waveform with and without a suppression method could be misleading as there is no common baseline between different methods.
2) Even though in a given switching circuit, when the parasitic inductance is lowered, the overshoot generally decreases, the parasitic inductance in isolation does not point to higher or lower overshoots.
3) Generally, the voltage and power of a converter, on their own, do not correlate with a higher overshoot.
4) If the achieved switching speed is used as a metric for the progress of power electronics, it can be seen that the field has progressed very well in the past ten years.

## APPENDIX

See Table 3

**TABLE 3. Oscillation Suppression Methods Comparison**

| Paper Title | Publication Acceptance Date | Method of suppression | Transistor material | Switch model | Results **Without** Oscillation Suppression Method | | | | | Results **With** Oscillation Suppression Method | | | | | Change in voltage overshoot percentage | Change in switching speed percentage |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Settling voltage [V] | Voltage overshoot % | Power [W] | Switching speed [V/ns] | Inductance [nH] | Settling voltage [V] | Voltage overshoot % | Power [W] | Switching speed [V/ns] | Inductance [nH] | | |
| [16] | 10/01/22 | Minimisation of Parasitic Inductance (Packaging ) | GaN | GS-065-060 | - | - | - | - | - | 419.2 | 4.6% | 10479.8 | 44.6 | 1.2 | - | - |
| [17] | 02/01/22 | Minimisation of Parasitic Inductance (Packaging) | GaN | GS-065-150-1-D | - | - | - | - | - | 386.8 | 8.0% | 34814.6 | 43.1 | 4.0 | - | - |
| [18] | 06/01/21 | Minimisation of Parasitic Inductance (Packaging) | GaN | S66508D | - | - | - | - | - | 289.8 | 9.2% | 8113.1 | 106.4 | 1.0 | - | - |
| [11] | 04/01/14 | Minimisation of Parasitic Inductance (PCB Layout Optimisation) | GaN | EPC2015 | 11.4 | 105.8% | 228.9 | 10.6 | 1.5 | 11.7 | 23.1% | 234.8 | 9.7 | 0.3 | -82.6% | -8.0% |
| [12] | 08/01/16 | Minimisation of Parasitic Inductance (PCB Layout Optimisation) | GaN | EPC2015 | 13.6 | 55.0% | 108.9 | 6.6 | 1.0 | 13.7 | 6.5% | 109.3 | 5.3 | 0.1 | -48.5% | -20.3% |
| [13] | 11/01/21 | Minimisation of Parasitic Inductance (PCB Layout Optimisation) | GaN | GS66508T | - | - | - | - | - | 200.0 | 2.9% | 3880.3 | 33.0 | 0.6 | - | - |
| [19] | 09/01/18 | Slower Switching (Driver) | SiC | SCT3040KL | 603.6 | 19.6% | 6035.8 | 12.5 | 209.4 | 605.7 | 13.5% | 6056.9 | 6.2 | - | -6.0% | -50.0% |
| [19] | 09/01/18 | Slower Switching (Gate Resistor) | SiC | SCT3040KL | 603.6 | 19.6% | 6035.8 | 12.5 | 209.4 | 606.4 | 14.7% | 6064.0 | 7.4 | - | -4.9% | -40.8% |
| [27] | 10/01/22 | Slower Switching (Gate Resistor) | SiC | C2M0080120D | 299.1 | 40.2% | 3888.3 | 13.3 | 438.7 | 301.3 | 27.0% | 3916.4 | 4.8 | - | -13.2% | -63.7% |
| [19] | 09/01/18 | Ferrite Bead | SiC | SCT3040KL | 603.6 | 19.6% | 6035.8 | 12.5 | 209.4 | 604.4 | 16.3% | 6044.2 | 12.3 | - | -3.3% | -1.4% |
| [21] | 12/01/17 | Active Gate Driver | SiC | SCH2080KE | 373.3 | 48.0% | 2240.1 | 18.1 | 500.1 | 373.6 | 10.0% | 2241.6 | 7.1 | - | -38.0% | -60.7% |
| [26] | 01/03/17 | Active Gate Driver | GaN | EPC2015 | 11.7 | 29.4% | 58.6% | 5.8 | 0.7 | 11.9 | 3.0% | 59.6 | 4.6 | - | -26.4 | -20.3 |
| [23] | 06/01/17 | Active Gate Driver | SiC | SCT2080KE | 414.7 | 52.4% | 3317.6 | 18.9 | 420.0 | 412.9 | 11.5% | 3303.6 | 12.9 | - | -40.9% | -31.9% |
| [27] | 10/01/22 | Active Gate Driver | SiC | C2M0080120D | 300.2 | 40.1% | 3902.2 | 13.3 | 438.7 | 302.1 | 24.7% | 3927.5 | 10.0 | - | -15.4% | -24.7% |
| [19] | 09/01/18 | Snubber (RC) | SiC | SCT3040KL | 603.6 | 19.6% | 6035.8 | 12.5 | 209.4 | 605.9 | 19.0% | 6059.5 | 12.3 | - | -0.5% | -1.6% |
| [41] | 11/01/21 | Snubber (RC) | SiC | C2M0080120D | 406.9 | 58.8% | 7730.7 | 29.9 | 220.2 | 405.1 | 53.3% | 7696.0 | 30.0 | - | -5.4% | 0.3% |
| [45] | 06/01/22 | Snubber (CRC) | SiC | C2M0025120D | 415.1 | 60.8% | 8302.7 | 40.7 | 232.4 | 413.9 | 23.5% | 8278.0 | 22.7 | - | -37.3% | -44.2% |
| [46] | 12/01/18 | Zero Overvoltage Switching | SiC | C2M0025120D | 401.7 | 24.3% | 19283.8 | 11.3 | 43.6 | 399.2 | 8.7% | 27144.9 | 19.8 | - | -15.6% | 75.9% |
| [48] | 12/01/22 | Zero Overvoltage Switching | SiC | FS03MR12A6MA 1B | 801.9 | 23.3% | 157969.8 | 20.3 | 25.8 | 793.5 | 4.1% | 156328.2 | 46.8 | - | -19.2% | 130.9% |
| [49] | 12/01/23 | Clamping (RC) | SiC | C2M0080120D | 306.3 | 52.9% | 9188.6 | 26.0 | 88.5 | 304.9 | 16.7% | 9147.6 | 23.0 | - | -36.2% | -11.4% |
| [50] | 08/01/21 | Clamping (RC) | SiC | IMW120R045M1 | 572.4 | 56.3% | 22896.6 | 45.3 | 179.9 | 565.8 | 16.7% | 22630.0 | 42.6 | - | -39.7% | -6.1% |
| [51] | 08/01/20 | External RLC Resonator (RC) | SiC | CAS120M12BM2 | 404.8 | 23.5% | 16193.7 | 4.9 | 103.8 | 405.8 | 23.7% | 16230.6 | 4.8 | - | 0.2% | -1.3% |
| [53] | 04/01/18 | None - Determination of Parasitic components | GaN | EPC2010C | - | - | - | - | - | 51.2 | 54.4% | 512.5 | 21.9 | 1.4 | - | - |

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