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The system design of a radar track-while-scan facility utilizing modern digital techniques

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the video is gated through to the display.

During the sweep the range rings also need to be generated and displayed. A cyclic counter is used to generate the range rings. When the flip-flop Q output from the range counter is set the range ring counter is loaded with DD Hex and the count is enabled. When the counters overflow, i.e. after 34 counts, the ring counter is loaded with DD Hex once again and the process is repeated. The carry is a pulse occuring every 2040m out to a range of 14280m. This pulse is one count wide i.e. 400 nsec.

The symbol video information is generated by the symbol generating circuitry. This signal is also a TTL voltage level.

When all three signals are available they are passed to a voltage summing network. This voltage summer consists of an op-amp connected in a non-inverting mode.

Each signal is input via a potentiometer, the function of these potentiometers being to control the output voltage of the particular signal being adjusted. Thus individual intensity controls for symbol brightness, range ring brightness and video brightness are available. The output of the summer is taken through a variable potentiometer to ground. The function of this potentiometer is to allow the setting of the overall display intensity. The centre tap of the potentiometer is passed through a 50 ohm line driver and output to form the

Z-modulation signal.

For the particular display used the signal was required to be inverted, in that OV on the Z-modulation input line caused no dot to be illuminated and a signal less than -1.2 volt caused the dot to start being illuminated. Maximum illumination was obtained with a voltage of -5volt.

Figure 6.4 details an oscilloscope plot of the X and Y deflection voltages and the Z-modulation waveform containing only the output from the range ring counter.

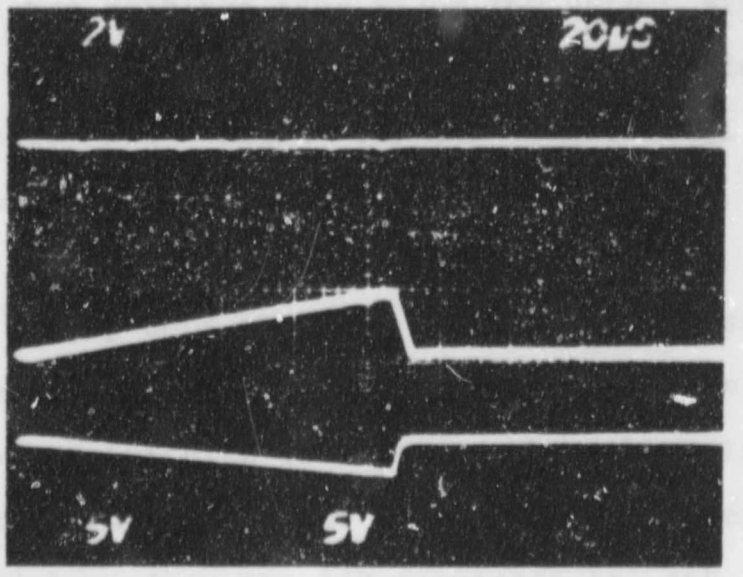


Figure 6.4 The Analog Sweep Voltages with the Z Modulation Signal

6.2 The Joystick Interface

Figure 6.5 illustrates the block diagram of the joystick position input device.

The joystick consists of two orthogonal potentiometers. Opposite polarity voltages are applied to either lead of the potentiomer. The centre-tap is then passed through an op-amp operating in the inverting mode. This op-amp has a variable potentiometer in the feedback loop to control the voltage level of the signal emerging from the op-amp. A potentiometer is connected to the non-inverting terminal of the op-amp to provide a means of adjusting the offset voltage of the output signal. These two settings thus allow the output signals of each of the two axis of the joystick to be varied for various full scale voltages and offset values. More will be said of these adjustment points in the following section.

From the op-amps the two signals are passed to 10 bit A/D converters. The start-of-conversion pulses are derived from the symbol positioning circuitry. When the pulse arrives it signals to the A/D to commence a conversion. After the conversion time the DR line from the A/D converter is set high. This signal becomes the clock signal to the latches and the digitised values are clocked into the latches. These two 10 bit words are passed in parallel format to the symbol positioning circuits to provide the position input for the designation marker.

Figure 6.5 Block Diagram of the Joystick Position Input Device

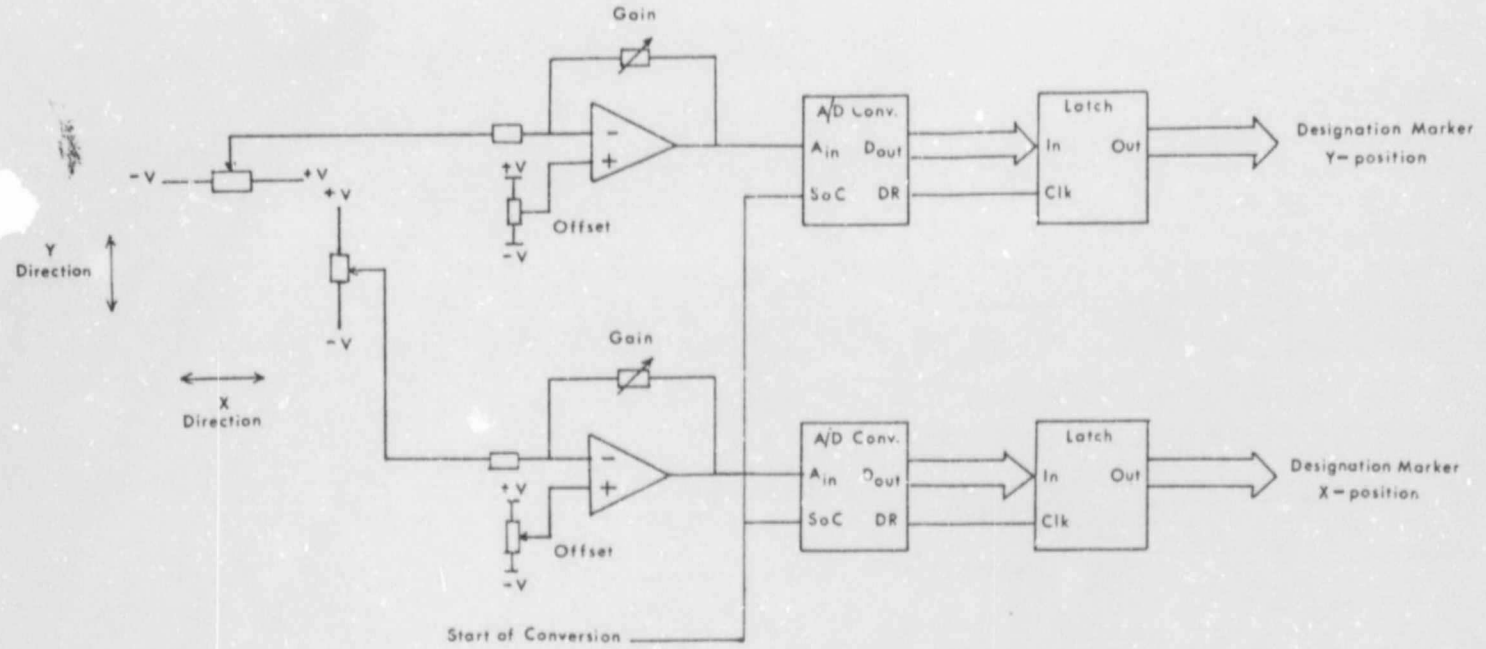


Figure 6.5 Block Diagram of the Joystick Position Input Device

6.3 The Symbol Generating And Positioning Circuitry

Provision must be made for the displaying of a designation marker symbol and three tracking symbols.

The HP 1310A display operates by drawing vectors on the screen. In order to output the symbol it was decided to draw the symbol on a raster-scan grid. The size of the symbol would then determine the size of this grid and thus the total time required to output all four symbols.

The grid is essentially overlaid on the PPI display. The range counter maximum count is 255 and this occurs at either edge of the screen. There are thus 512 counts from the extreme left to the extreme right or from the top to the bottom of the display. The 512 discrete steps require a 9 bit D/A or A/D converter as required, not a very standard value. A 10-bit D/A and A/D converter was thus requested for the symbol postioning circuitry.

Figure 6.6 illustrates the grid superimposed on the PPI display.

The display size is 9 inch x 9 inch (228x228mm). Through experimentation it was found that the designation marker size should be about 6-8mm square for accurate positioning over the target. This area required a grid of between 27 and 35 bits. To facilitate easy implementation a grid of 32x32 bits was chosen.

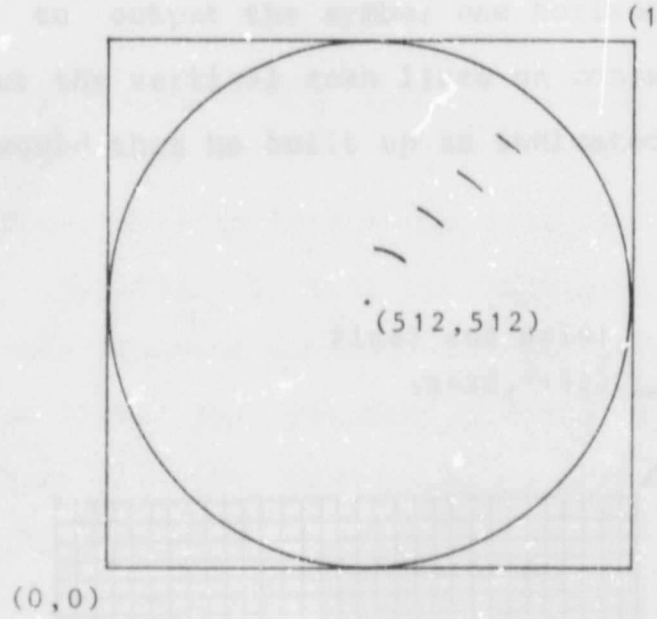


Figure 6.6 The PPI Display and the Overlay Grid

As was mentioned in section 6.1.1 the dead time between the end of one sweep and the commencement of the following sweep is 298 usec. In order to write out a complete symbol of 32x32 bits at the clock rate would require 410 μsec. It is therefore evident that some scheme had to be adopted whereby the symbols were sequentially built up on the display over successive intervals.

Another factor is the settling time of the display in response to a step input. For this particular display the settling time for a full screen deflection voltage step is 10 μsec. Thus, once the sweep is finished and the position of the symbol is output to the display a delay must be introduced in the symbol Z-modulation information to allow the trace to settle.

In order to simplify the grid generating circuitry it was decided to output the symbol one horizontal scan at a time and to output the vertical scan lines on consecutive intervals. The symbol would thus be built up as indicated in figure 6.7.

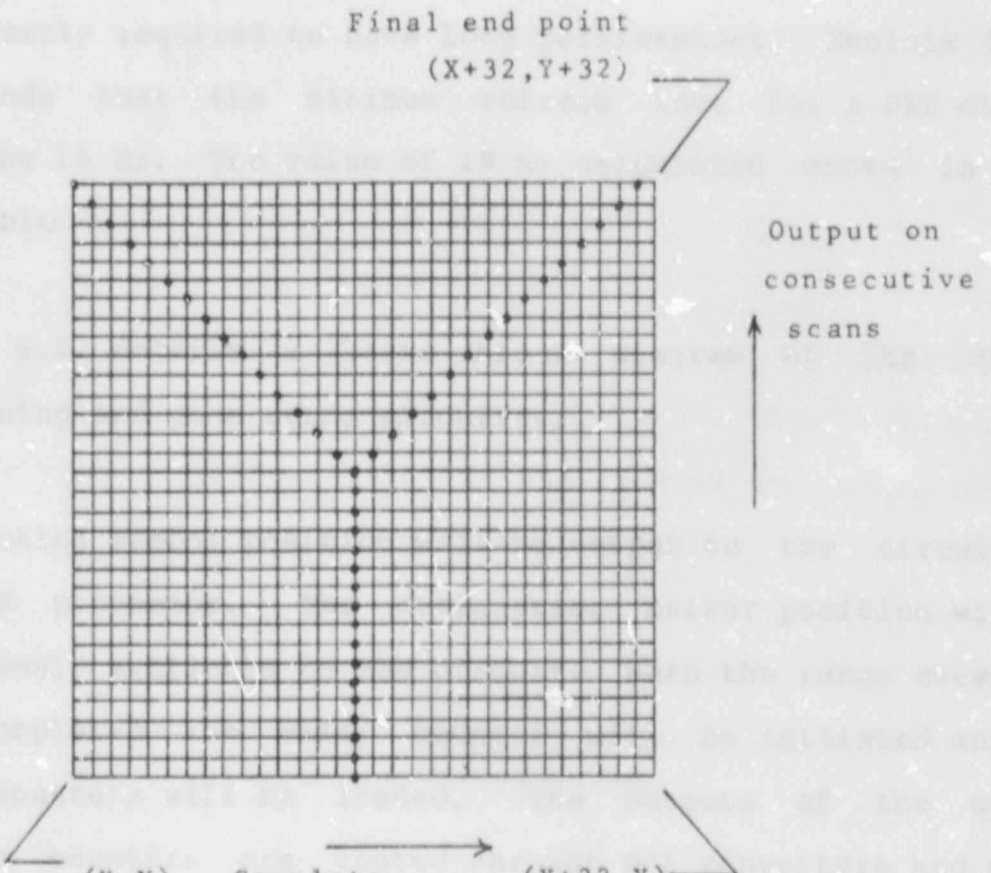


Figure 6.7 How the Symbol is Built Up

Once a symbol is completely output, the next symbol would be output and so on. When all four symbols have been output the process would start again.

The time to output the four symbols would then be calculated as follows:

4 x 32 Y-scans x 400 μsec = 51.2 msec.

One would assume that this would give rise to flicker on the display. However, it must be remembered that PPI displays are by necessity required to have long persistences. Skolnik (1970) recommends that the minimum refresh rate for a PPI display should be 15 Hz. The value of 19 Hz calculated above is thus acceptable.

Figure 6.8 details a basic block diagram of the symbol positioning and generating circuitry.

The tracking symbol position will be output to the circuit by the TWS processor. The designation marker position will be continuously avaliable to the circuit. When the range sweep has been completed the delay counter will be initiated and the symbol counters will be loaded. The outputs of the symbol position counters are routed through D/A converters and on to the display. This will thus allow the display to settle on the starting point of the symbol. After 10 μsec the delay counter will start the symbol grid counters. The symbol grid X-counter counts off 32 clock pulses and then halts. The position counter similarly counts off 32 pulses, so the output of the X-position counter will be a value that starts at the initial X value and rises to a value of initial X value plus 32. When passed through the D/A converter the result will be a ramp voltage.

Figure 6.8 Basic Block Diagram of the Symbol Positioning and Generating Circuitry

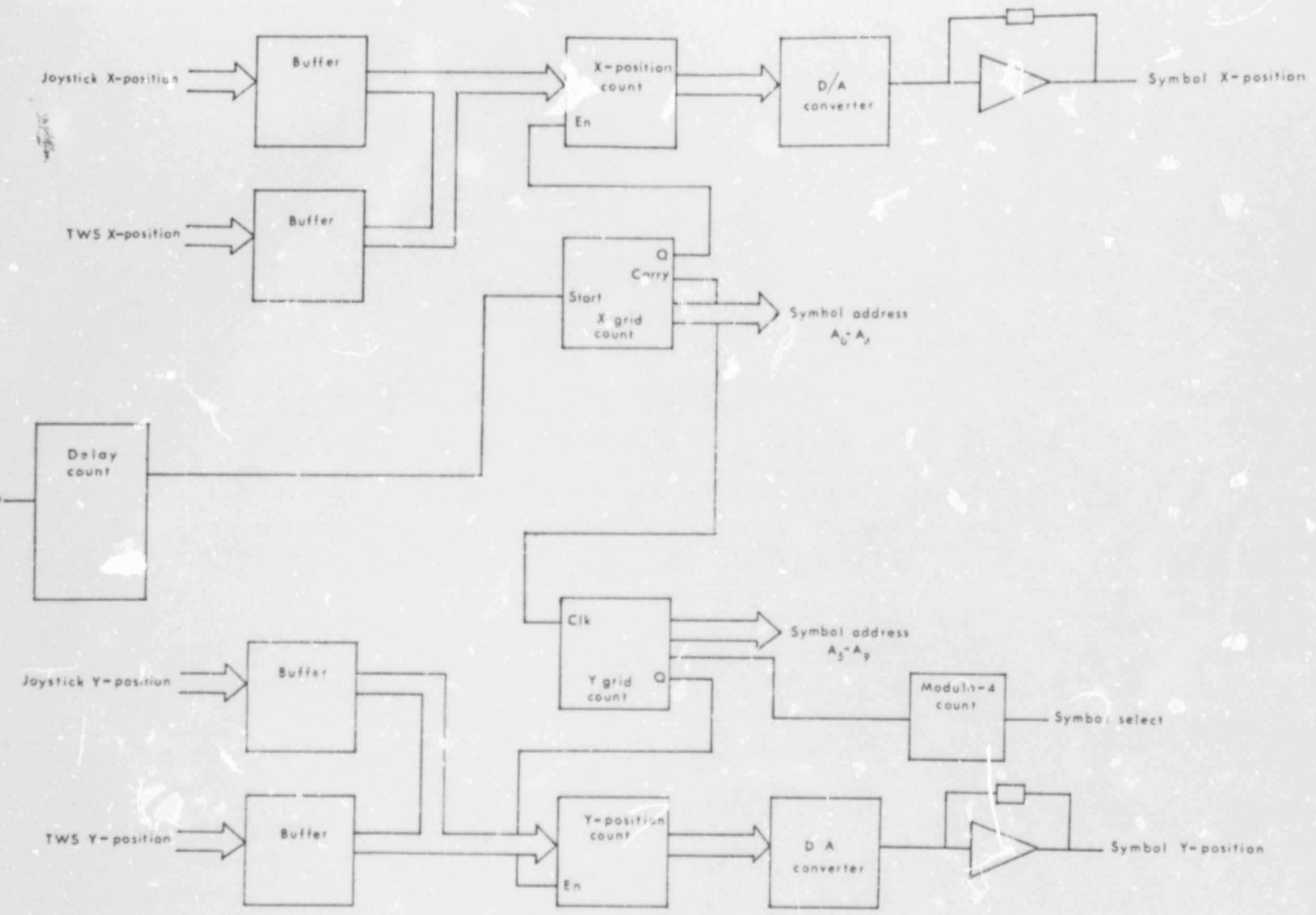


Figure 6.8 Basic Block Diagram of the Symbol Positioning and Generating Circuitry

The output of the Y-position counter is constant for the whole period. When the grid X-counter has reached 32 it clocks the grid Y-counter to increment by 1. After 32 sweeps the grid Y-counter resets and the whole process is repeated.

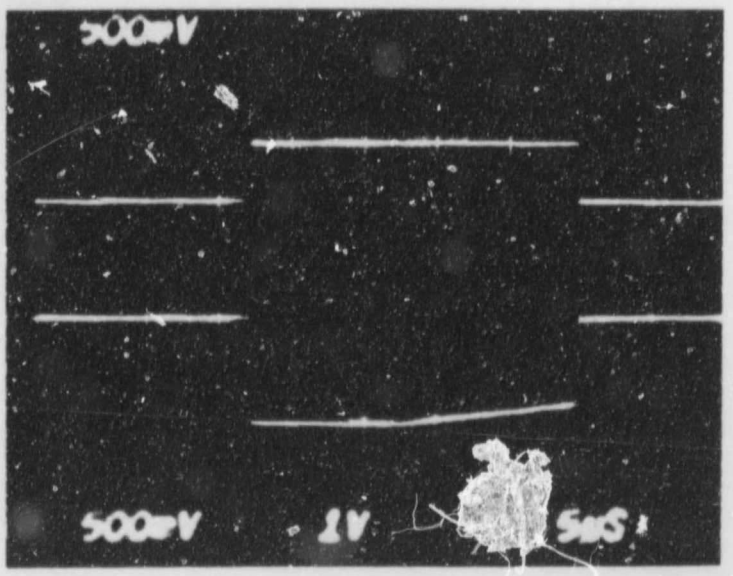
A Modulo-4 cyclic counter is used to control the selection of the particular symbol to be output. This counter is clocked by the grid Y counter resetting. The resetting also forms the Start-of-Conversion pulse for the joystick input device.

The output from the grid X and Y counters forms the address bus for the symbol Z-modulation circuit. The Y counter outputs form the five most significant bits of the address and the X counter outputs form the five least significant bits.

Appendix F contains a detailed description of the operation of the symbol positioning and generating circuit.

The reason for the variable potentiometers being included in the output stages of the joystick input devices may now be explained. The maximum analog output voltage from the potentiometers is adjusted so that the symbol positioning circuits do not output a count that may cause the designation tracker symbol to move off the edge of the screen.

Figure 6.9 details an oscilloscope plot of the actual voltage waveform obtained from the circuit.



Y Voltage

X Voltage

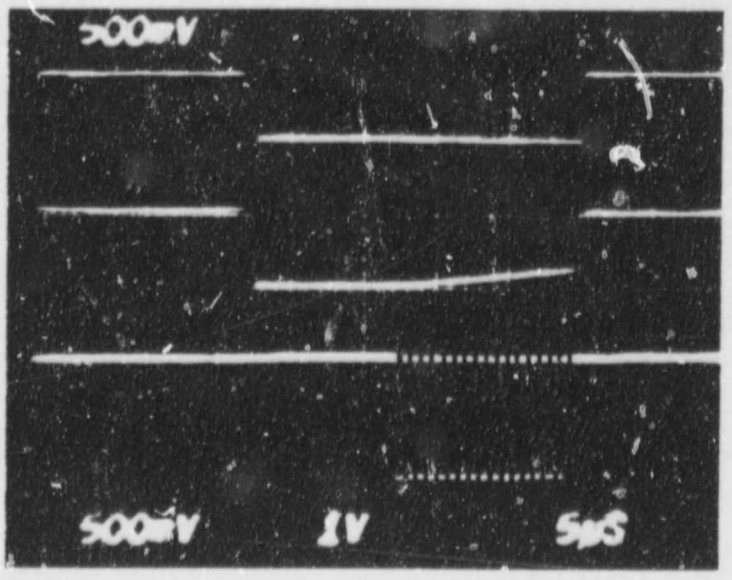
Figure 6.9 The Analog Symbol Voltages

While the deflection voltages are being generated it is also necessary to generate the Z-modulation signal. Remembering that the symbol is built up on a 32x32 grid, it is possible to implement many symbols shapes. The design procedure was to use a 2Kx8 EPROM in which to store the shape of the symbols. Each symbol's Z-modulation information for a particular point X,Y on the grid is 1 bit, the four lower bits of the EPROM data bus are thus used to store the four symbol shapes. The address for the EPROM is generated by the grid X-position and Y-position counters, the five most-significant bits of the address coming from the Y-position grid counter. The Modulo-4 ring counter, in addition to selecting the particular symbol initial position

also selects the correct symbol data to be output as the Z-modulation signal. This signal is added to the Z-modulation signal from the sweep to form the composite Z-modulation waveform.

Figure 6.10 details the block diagram of the Z-modulation generating circuitry.

Figure 6.11 details an oscilloscope plot of the actual deflection voltages with the Z-modulation signal superimposed.



Y Voltage

X Voltage

Z Modulation

Figure 6.11 The Analog Symbol Voltages with the Z Modulation Signal

The designation marker symbol shape is a square, the TWS symbols

Figure 6.10 Block Diagram of the Symbol
Z-modulation Generating Circuitry

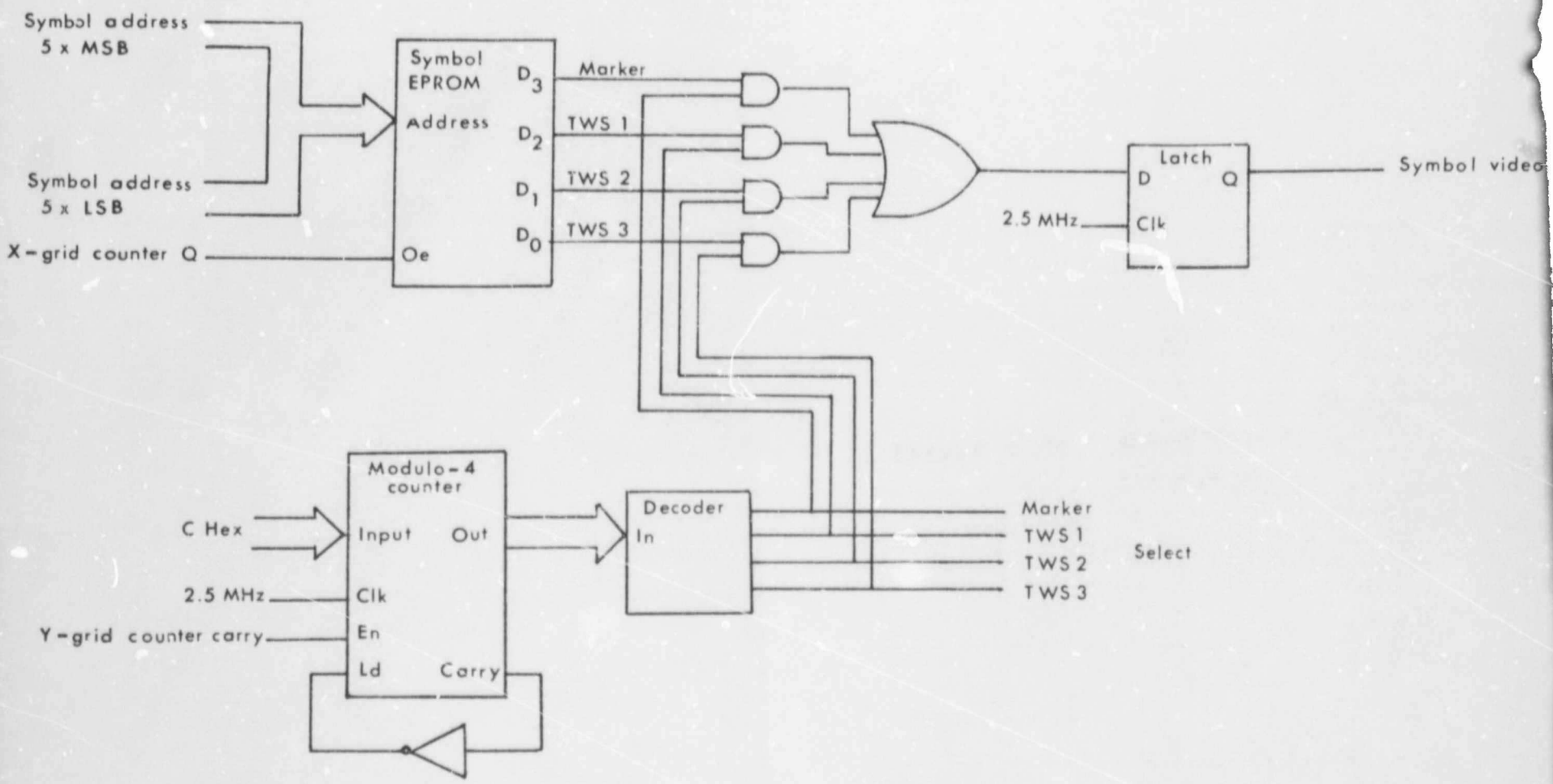


Figure 6.10 Block Diagram of the Symbol Z-modulation Generating Circuitry

have three shapes: Y,X, +

Once the symbol deflection voltages have been generated they are mixed into the sweep deflection voltage waveforms.

Figure 6.12 details an oscilloscope plot of the composite X and Y deflection voltages with the Z-modulation waveform included.

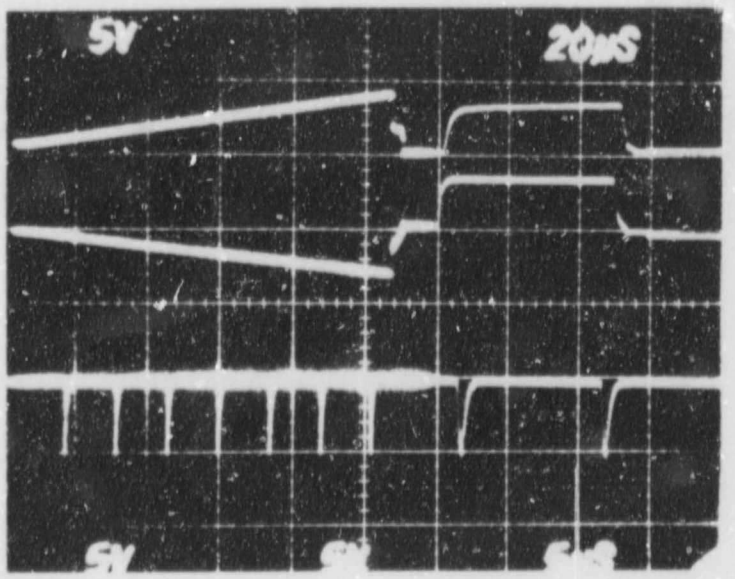


Figure 6.12 The Composite X,Y Deflection Voltages with the Z Modulation Signal

The portion dealing with the symbol generating voltages is shown magnified for clarity.

6.4 The Track-While-Scan-Processor

The Track-while-Scan processor is discussed under three sections

1. The window generator
2. The Memory function
3. The tracking algorithm

6.4.1 The Window Generator

The window generator card is constructed on a special wire-wrap card capable of being plugged into one of the IBM PC expansion slots. It thus has direct access to the system data bus, address bus and control lines.

The main function of the window generator is to set up the window within which all echoes may be gated through to the memory card.

Figure 6.13 illustrates the manner in which the window is implemented.

The window start azimuth value, azimuth extent, start range value and range extent are output to the window generator by the TWS processor.

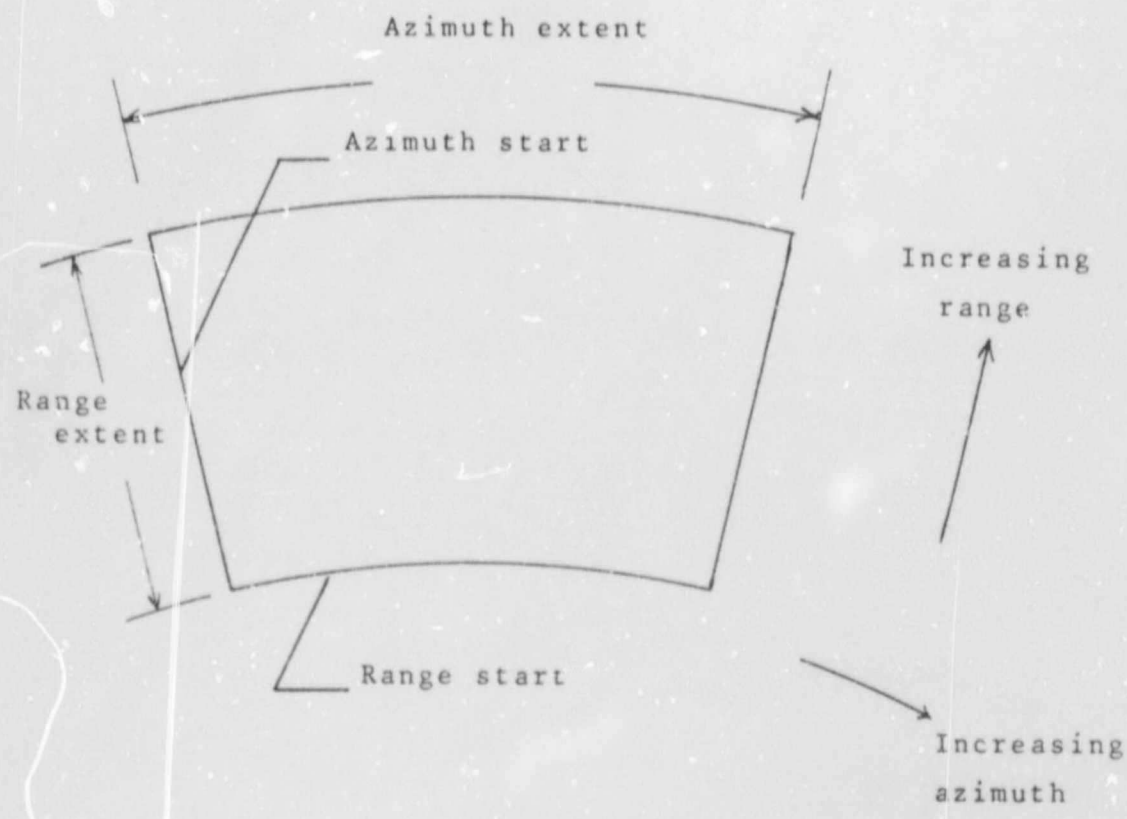


Figure 6.13 How the Window is Constructed

Figure 6.14 details a basic block diagram of the window generating circuit.

The start azimuth value, azimuth extent, start range value and range extent are output from the IBM PC data bus via Programmable Interface Adapters (PIA's). The output of the range PIA is two 8 bit words. The start range is an 8 bit word that is presented to the inputs of a comparator. The range extent is an 8 bit word that is output to the range extent counter. When the range count equals the value stored in the comparator the range extent counter is initiated. When the

Figure 6.14 Basic Block Diagram of the Window Generating Circuitry

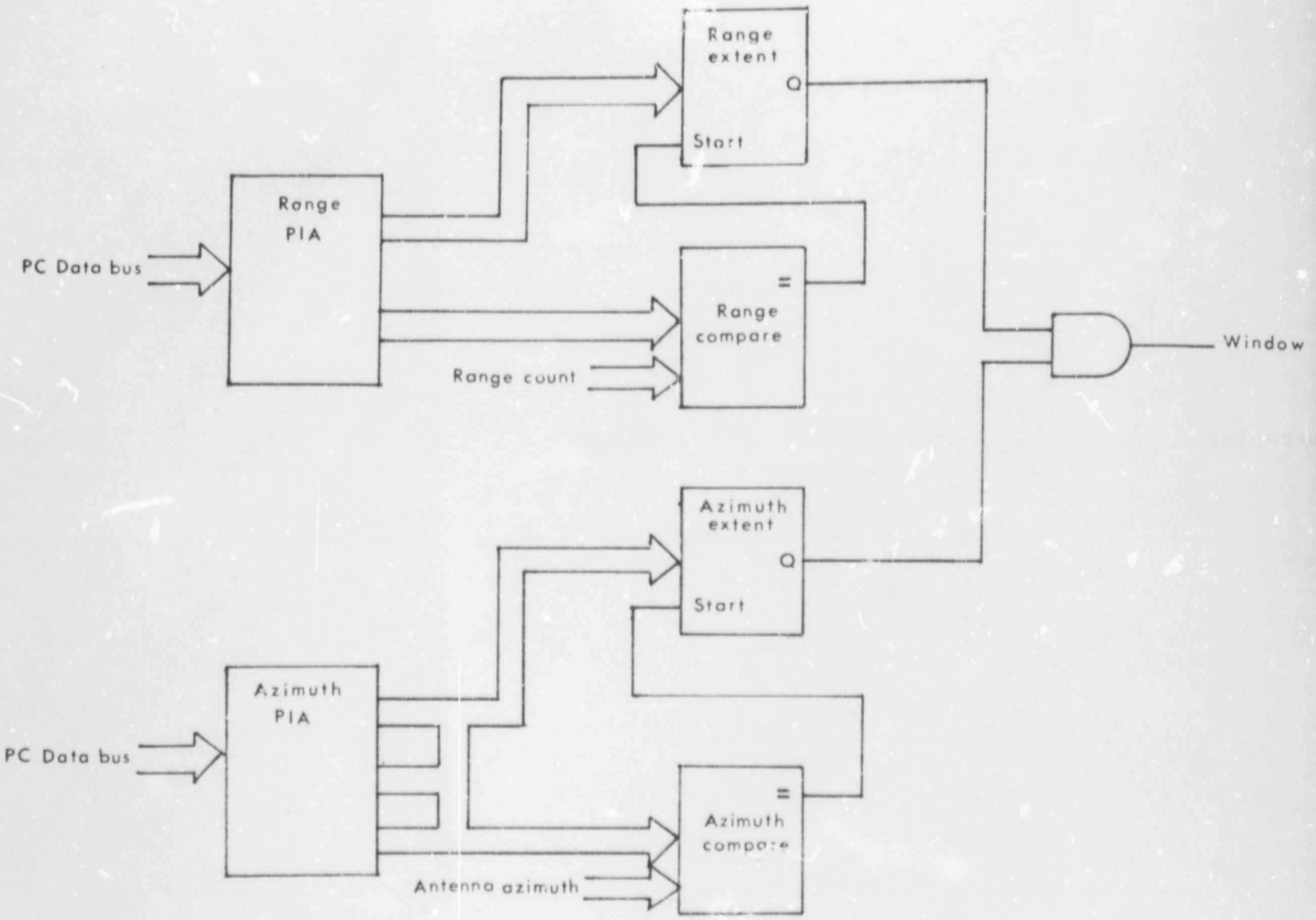


Figure 6.14 Basic Block Diagram of the Window Generating Circuitry

range extent has been reached the counter is disabled. The output from the window range generator is thus a pulse that is high for the period in which the range count lies within the window.

The start azimuth value is presented to the azimuth comparator and the azimuth extent is loaded into the azimuth extent counter. As the antenna scans round, the antenna position is continuously compared to the value stored in the comparator. When the two values are equal the azimuth extent counter is initiated. When the azimuth extent has been reached the counter is disabled. The output from the window azimuth counter is thus a pulse that is high for the period in which the antenna lies within the window.

These two outputs are then ANDed to form the gating pulse for the one-bit video.

Appendix G contains a detailed description of the operation of the window generating circuit.

6.4.1.1 The Memory Card

The function of the memory card is to store the range and azimuth values of each and every echo received within the window. Figure 6.15 details the basic block diagram of the

memory card.

While the radar is operating within the window the echo counter will be enabled, the address bus for the memories will originate from the echo counter and the range and azimuth values from the radar will be routed to the memory data bus. For each echo then the range and and azimuth will be recorded at a particular memory location. When the antenna scans past the window the echo counter is disabled, the IBM PC address bus is routed to the memories and the memory data bus is allowed access to the processor. The memories on the memory card then essentially form part of the processor memory map. The tracking algorithms then have access to all the information stored while the radar was operating within the window.

Two further operations are required. One PIA is necessary to input the designation marker position. The X and Y positions of the marker are 10 bit words. The words are thus split up into three 8 bit words. The lower 8 bits of the X and Y positions are input as is, the upper two bits of each word being combined into a single word. The algorithm must then decode the data back to the correct values. The other operation is the output of the tracking symbol position. Again a PIA is used for this function. The processor outputs the 8 bit data and the PIA is wired in such a manner that the relevant bits form the correct words.

Appendix H contains a detailed description of the operation of the memory card.

Figure 6.15 Basic Block Diagram of the Memory Card

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