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Lowan, Akani Henley

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Development of a Coupled Inductor SEPIC Using a Planar Integrated Structure for LED Lighting Applications

Akani Henley Lowan

A dissertation submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, Johannesburg, in fulfillment of the requirements for the degree Master of Science in Engineering.

Johannesburg, 2013

Declaration

I declare that this dissertation is my own unaided work. It is being submitted for the degree of Master of Science in Engineering at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree nor examination at any other university.

Signed on _____ day of _____ 2013

_____

Akani Henley Lowan

Abstract

The growing interest and use of LED lighting sources has resulted in a lot of effort being focused on developing LED driving circuits. In this dissertation the coupled inductor SEPIC is considered. The significance of the circuit in this work is that it is constructed from a new technology. The novelty in the construction is that all the passive components in the circuit are integrated in a planar structure. It is envisaged that the technology will eventually lead to cost reductions, improved reliability and an easier manufacturing process for the converter. In order to formulate some of the design specifications for the converter, namely the relative inductor sizes and coupling coefficient an analysis of the ripple in the converter for various coupling configurations is done. The analysis is facilitated by derived equations which describe the operation of the circuit in the time domain for steady state conditions. In order to be able to integrate the converter it is necessary to understand the operation and building elements of the planar structure. So a two conductor integrated passive is reviewed. A two conductor integrated passive essentially consists of two conductors which sandwich a dielectric, and all of which are enclosed by a magnetic core. The review entails a study of the various terminal uses of the structure and resulting equivalent circuits that can be obtained. The equivalent circuits are regarded as building blocks to constructing more complex circuits and examples of this are shown. The example circuits that are integrated include a custom network, a boost converter, and a flyback converter. Finally the complete design approach for developing a coupled inductor SEPIC using a planar structure is presented. From the design two different integrated assemblies are proposed. To validate the design, a 5W prototype for each assembly was built and tested. The prototypes' impedances were compared to the impedances of ideal conventional circuits in which agreement was observed into the high frequencies. Voltage waveforms during voltage conversion operation were also compared to that of built conventional circuits and general agreement was observed in all the waveforms. The efficiency was also measured where an average efficiency of 85.6% for the one prototype and 86.3% for the other prototype was observed for a 5W load.

Acknowledgments

I would like to thank my supervisor, Professor Ivan Hofsajer, for his guidance and patience throughout the duration of the study.

I would also like to extend my gratitude to my family and friends for their support and understanding during the course of the study.

Lastly but not least, I would like to thank Dr Richard Reeves and Mr Gareth Sessel for reviewing sections of this work.

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List of Symbols

A	effective area of capacitor plates
A_1	coefficient in the assumed solution to a 2nd order differential equation
A_2	coefficient in the assumed solution to a 2nd order differential equation
A_{cap}	effective area of capacitor plates
A_{core}	area of centre leg on a magnetic core
$\hat{B}$	magnetic field flux density
C_x	required capacitance
d	separation distance between two plates
D	duty cycle
d_x	separation distance between two plates
δ_{cu}	skin depth
Δi_{L1}	current ripple through inductor 1
Δi_{L2}	current ripple through inductor 2
Δv_{Cs}	voltage ripple across the series coupling capacitor
ϵ_0	permittivity of free space
ϵ_r	relative permittivity of material
ϵ_x	relative permittivity of material
η	efficiency
f	operating frequency
f_s	switching frequency
$\hat{H}$	magnetic field intensity
I	operating current
$i_{L1}(t)$	current through inductor 1 as a function of time

$i_{L1-OFF}(t)$	current through inductor 1 during the off interval as a function of time
$i_{L1-ON}(t)$	current through inductor 1 during the on interval as a function of time
I_{L1-0}	initial current through inductor 1
$I_{L1-average}$	average current through inductor 1
$I_{L1-peak}$	peak current through inductor 1
$i_{L2}(t)$	current through inductor 2 as a function of time
$i_{L2-OFF}(t)$	current through inductor 2 during the off interval as a function of time
$i_{L2-ON}(t)$	current through inductor 2 during the on interval as a function of time
I_{L2-0}	initial current through inductor 2
$I_{L2-average}$	average current through inductor 2
$I_{L2-peak}$	peak current through inductor 2
I_{peak}	peak current due to inductors in circuit
j	imaginary unit
J_{cu}	current density
k	coupling coefficient
l_{core}	length of centre leg on a magnetic core
l_g	length of air gap
l_{mean}	mean length of conductor layer
l_{path}	length of magnetic path
M	mutual inductance
μ_0	permeability of free space
μ_r	relative permeability of the core
n	switching cycle
N	number of inductor turns
ω	angular frequency
$P_{in(DC)}$	input DC power
$P_{out(DC)}$	output DC power
ρ	resistivity

s_1	time constant in the assumed solution to a 2nd order differential equation
s_2	time constant in the assumed solution to a 2nd order differential equation
t	time
τ	arbitrary integration variable
T_s	switching period
$v_{Cs}(t)$	voltage across the series coupling capacitor as a function of time
$v_{Cs-OFF}(t)$	voltage across the series coupling capacitor during the off interval as a function of time
$v_{Cs-ON}(t)$	voltage across the series coupling capacitor during the on interval as a function of time
V_{Cs-0}	initial voltage across the series coupling capacitor
$V_{Cs-average}$	average voltage across the series coupling capacitor
w_c	conductor width
w_{core}	width of centre leg on a magnetic core
$\hat{W_e}$	electrical energy
$\hat{W_m}$	magnetic energy

Chapter 1

Introduction

Over the years, attention has been given into developing lighting technologies that are efficient and that have little harm on the general environment. The light emitting diode (LED) has received growing interest over the years as a lighting source that will ultimately replace other traditional lighting sources such as incandescent lighting and fluorescent lighting.

Incandescent lighting is known to be inefficient and to have a low luminous efficacy, making it an unsuitable lighting option. Fluorescent lighting makes use of mercury vapour in its lighting mechanism and at the end of its operating life the fluorescent tube becomes a hazardous waste item to the environment due to the toxic mercury compound. LEDs have the advantage of being durable, energy efficient, have a high luminous efficacy, a long operating life and contain no toxins which can harm the environment [1, 2]. The growing interest and use of LED lighting sources has resulted in a lot of effort being focused on developing LED driving circuits.

1.1 Circuit Topologies

Circuit drivers for LED loads are necessary as it is common that a load may require a different voltage level to the voltage level of the available power source. Considering figure 1.1, for simple low power applications a series resistor may be a simple solution to limiting the power delivered to the LED load. However this method is generally very inefficient due to the energy that is lost through the resistor and is unacceptable for high power operation. Another approach to adjust the voltage or current delivered may be through the use of a linear regulator, which is also an inefficient device.

In order to convert the dc voltage level of an input source to a different output voltage level in an efficient manner, dc-dc converters are employed. They generally comprise of reactive components and semiconductor devices which are typically used as switches. Dc-dc converters do have power loss but not as large as that of a resistive network that would perform the same function and as such much higher efficiencies are achieved.

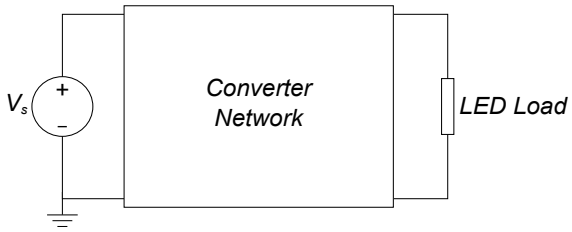


Figure 1.1: Source and load with power converter network.

Various dc-dc converter topologies have been employed before to drive LED loads such as a buck, boost, buck-boost, flyback, Cuk and a single ended primary inductor converter (SEPIC). Variations of these classic topologies are also employed to drive LED loads. An appreciable review of the various classic LED driving circuits has been presented [3]. In this work interest is given to a converter on merit of versatility such as the ability to obtain a constant output voltage for a wide input voltage range and also having a topology that requires a minimum number of components. A buck-boost, Cuk, flyback and SEPIC all meet this criteria but focus is given to a SEPIC. The SEPIC has robust power factor correction capabilities [3, 4] which make it a worthwhile topology to investigate as circuits with good power factor correction are highly applicable in domestic and industrial applications. A variation of the standard SEPIC in which the inductors are magnetically coupled also exists, and is referred to as a coupled inductor SEPIC. Although coupling inductors on single magnetic core may increase the demand on the design of the magnetic component, it can have various performance benefits as well as reduce the required space for the circuit. A coupled inductor SEPIC has been regarded to have some performance benefits over a standard SEPIC such as lower current ripples [5, 6], high frequency noise reduction [7] and lower AC current losses [8]. A coupled inductor SEPIC has also been demonstrated to be more efficient and have less component stress than a flyback converter [9]. The mentioned advantages make the coupled inductor SEPIC worthy of being studied and it is therefore a focus in this work.

1.2 Converter Requirements

The design of an LED driver typically involves efficiency considerations, thermal considerations as well as electromagnetic interference and compatibility considerations [3]. In addition there are other requirements such as low cost, reliability and ease of manufacture that the converter should meet. In general research effort towards improving these aspects exists. Barriers dominating some of these aspects have been identified as system packaging, parasitics, control, thermal management and system integration issues [10]. In this dissertation attention is given to system integration, as it is envisaged it will eventually lead to reduced costs, improved reliability and easier manufacturing for the converter.

1.3 Converter Construction

The physical construction of power converters has traditionally involved the use of discrete components, however it has been indicated that the manufacturing process of a power converter using discrete components can be labour and cost intensive [10]. Thus recent years in the power electronics industry have seen advances towards modularisation and integration of power electronics in an effort to reduce assembly requirements and cost as well as improve aspects of the system performance [10]. One of the goals in power electronic system modularisation and integration is to achieve a construction and manufacturing technique that may ultimately only require a single production line with a high level of automation, thus reducing the manufacturing labour and cost. Integration and modularisation schemes may be for the active devices in a converter or for the passive components in a converter. This work is focused on the integration of the passive components. Integration of passive components involves having the capacitive and inductive components integrated into one electromagnetic component. The primary focus in this dissertation is the integration of the passive components in a coupled inductor SEPIC (as indicated in figure 1.2), using a planar structure.

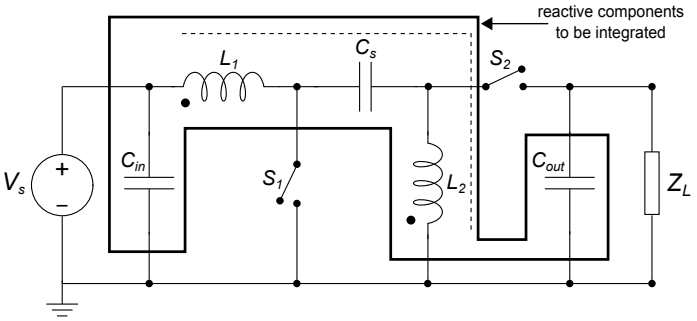


Figure 1.2: Topology of a coupled inductor SEPIC with reactive components to be integrated.

1.4 Integrated Electromagnetic Components

Historically structures to integrate capacitive and inductive components were initially based on barrel type windings such as in figure 1.3. The first integrated passive component is cited to have been patented in 1949 [11] and since then other barrel type integrated passives were created [12–15].

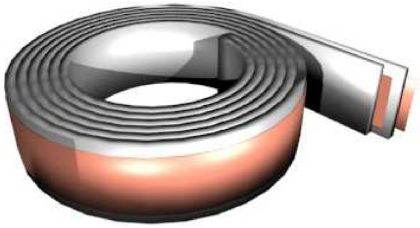


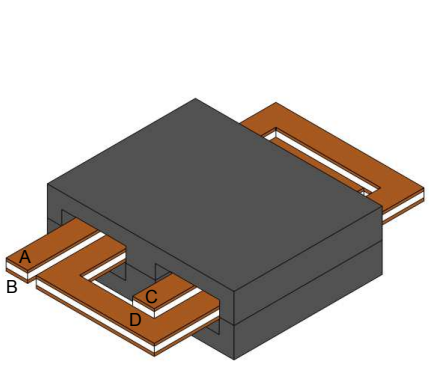
Figure 1.3: Barrel wound structure [16].

Barrel type structures had limitations in the materials and capacitance values that could be achieved which led to the development of planar structures [17]. The advantages of integrating the reactive components in a planar structure are:

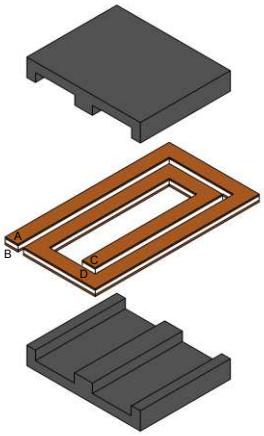
- Ease of manufacture. Prefabricated conductive, dielectric and magnetic sheets can easily be stacked on top of each other.
- Reduced cost due to the easier manufacturing process.
- An increased surface-to-volume ratio which has thermal management benefits.
- Increased power densities.
- Possibility of using alternate capacitive materials other than electrolytic which results in improved reliability.

Another modern technique to construct integrated passives using multi-cells has been proposed [18] but in this dissertation the planar spiral winding structure is employed.

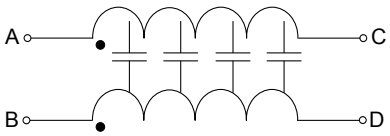
An example of a planar integrated passive is given in figure 1.4. It constitutes of two conducting sheets sandwiching a high permittivity dielectric layer and all of which are enclosed by the magnetic core. The general circuit impression is given in figure 1.4(c) which indicates the configuration of the reactive components. The schematic also aims to communicate that the capacitance in the structure is of a distributed nature.



(a) General structure.



(b) Exploded view.



(c) General circuit impression.

Figure 1.4: Planar integrated passive structure.

The most significant aspect to appreciate however is that from a terminal perspective the integrated passive structure of figure 1.4 can behave like a simple lumped component or network of lumped components. This depends on the terminals used and is for a certain range of frequencies. The concept forms the fundamental basis from which a network of planar integrated passive components can be realised.

Various circuit models for the structure of figure 1.4 have been proposed and can be classified as lumped parameter models and distributed parameter models. Lumped parameter models have been demonstrated to predict the performance of the integrated passive structure for low frequencies. Whereas distributed models can describe the behaviour of the integrated electromagnetic structure up to high frequencies. The significance of the various models is regarded to be application specific, and details of this are reviewed further in chapter 3. In this dissertation, a lumped parameter model is employed and demonstrated to be sufficient for general design purposes.

The approach to planar integration of passive components has also been application specific whereby to date the technology has only been applied to a few classic topologies. The ease in which the technology is applied has also been dependent on the designer's experience. A review of some of the previous work on integrated planar structures has been conducted [19]. Other examples include integration of LCT components [20], integration of LCCT components [21], integration of LLCT components [22], and integration of the passive components in a flyback converter [23]. Planar integration of the passive components in a coupled inductor SEPIC has not been attempted and is thus a key contribution of this dissertation.

1.5 Study Objectives

In order to successfully develop a coupled inductor SEPIC using a planar integrated structure, some key aspects in the approach have to be highlighted. These constitute the study objectives which are:

- An analysis of the operation of the coupled inductor SEPIC. From the analysis, some of the design specifications can be formulated.
- Review a two conductor planar integrated passive. This structure is a building block in constructing the planar integrated coupled inductor SEPIC.
- Design and construct a coupled inductor SEPIC using planar integrated passives. This objective also includes an evaluation of the performance of the circuit.

1.6 Outline

The content in the remainder of the dissertation is as follows:

- Chapter 2 is dedicated to analysing the ideal operation of the coupled inductor SEPIC. A qualitative description of the operation is given followed by a time domain analysis of the circuit response at steady state. From the derived time domain equations, the effect of inductor coupling on the converter ripple is assessed. The chapter concludes with a description of an appropriate inductor coupling configuration for the study.
- Chapter 3 discusses a two conductor planar integrated structure. Modelling approaches are considered as well as the various terminal uses of the structure. Aspects pertaining to the combination of multiple modules are also discussed.
- Chapter 4 details the design process for developing a coupled inductor SEPIC using planar integrated passive components. Two different integrated assemblies are proposed and discussed throughout the chapter. The chapter also details the experimental evaluation of the integrated assemblies. The experiments include impedance measurements, measured waveforms during voltage conversion operation, and efficiency measurements.
- Chapter 5 summarises the presented work and highlights the conclusions. Some recommendations for future work are also made.

Chapter 2

Coupled Inductor SEPIC

This chapter aims to describe the operation of a coupled inductor SEPIC and to study the effects of inductor coupling on the circuit. The operation is described qualitatively and then followed by a piecewise linear analysis of the circuit for ideal steady state operation in continuous conduction mode. The study on inductor coupling leads to a partial formulation of the circuit design specifications for this dissertation. The design specification considered is the ratio of the two inductors as well as the inductor coupling coefficient.

2.1 Fundamental Operation

The coupled inductor SEPIC is depicted in figure 2.1. The input current to the circuit is through inductor L_1 which also ensures that the input current is continuous. The capacitor C_{in} minimises the line voltage ripple as well as unwanted impedance interactions. The coupling capacitor C_s isolates the input from the output. It also provides some protection against a short circuited load. The output capacitor C_{out} is meant to provide continuity of the output voltage and is thus sized to have a low voltage ripple. The circuit also contains switches S_1 and S_2 which are typically realised using a transistor and diode, respectively. The transistor is usually driven by a pulse width modulated signal.

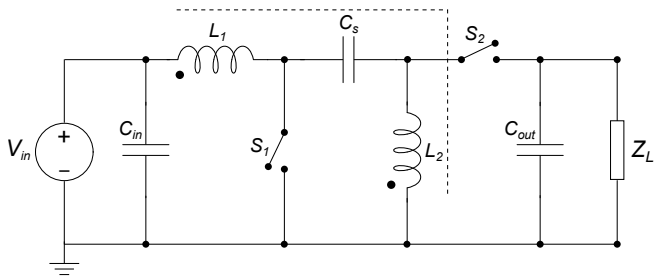
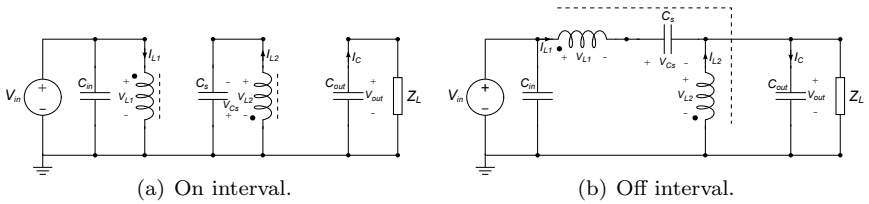
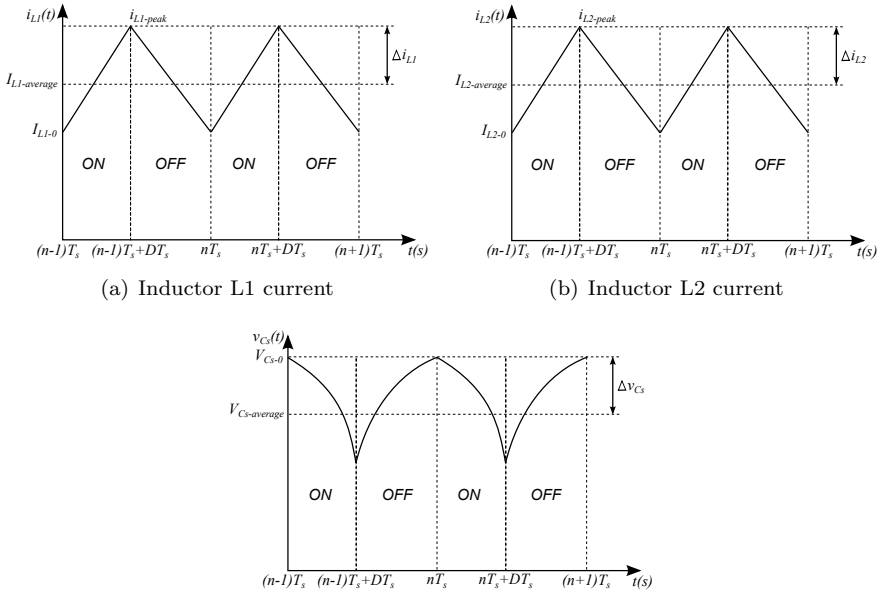


Figure 2.1: Coupled inductor SEPIC topology.



(a) On interval. (b) Off interval.

Figure 2.2: Coupled inductor SEPIC voltage and current definitions during a switching cycle.



(a) Inductor L1 current (b) Inductor L2 current

(c) Capacitor Cs voltage

Figure 2.3: Coupled inductor SEPIC voltage and current waveforms during a switching cycle.

Figure 2.2 shows the configurations of the circuit during a switching cycle. The analysis is simplified by first considering the quantities that will not change instantaneously when the circuit switches between the various states, namely the capacitor voltages and the inductor currents. Figure 2.3 illustrates the typical inductor current waveforms and the coupling capacitor voltage waveform during steady state operation of the coupled inductor SEPIC. The analysis in the chapter only considers these three components given the assumptions about the other two capacitors which are: that the source is regarded as ideal meaning the effect of C_{in} can be ignored, and that the output capacitor C_{out} is assumed to be large and thus to be a constant voltage source at steady state.

In general the operation of the circuit in the two intervals of a switching cycle is described as follows

On interval [(n-1)T_s, (n-1)T_s+DT_s]: When switch S_1 is closed, switch S_2 which is usually realised using a diode is reverse biased and thus open circuited with the configuration as in figure 2.2(a). During this interval the source supplies energy to inductor L_1 leading to a current increase. Similarly capacitor C_s supplies energy to inductor L_2 leading to a current increase. The output capacitor supplies energy to the load during this interval.

Off interval [(n-1)T_s+DT_s, nT_s]: Switch S_1 is opened while switch S_2 which is usually realised using a diode is forward biased resulting in the circuit of figure 2.2(b). During this interval inductor L_1 and inductor L_2 supply energy to the circuit. Capacitor C_s is charged through the input inductor. The output capacitor C_{out} is also charged during this interval.

The mathematics associated with the waveforms of figure 2.3 which also indicates the operation of the converter in the time domain can be summarised as

$$i_{L1}(t) = \begin{cases} i_{L1-ON}(t-(n-1)T_s) & \text{when } (n-1)T_s \leq t < DT_s + (n-1)T_s \\ i_{L1-OFF}(t-DT_s-(n-1)T_s) & \text{when } DT_s + (n-1)T_s \leq t < nT_s \end{cases}$$

$$i_{L2}(t) = \begin{cases} i_{L2-ON}(t-(n-1)T_s) & \text{when } (n-1)T_s \leq t < DT_s + (n-1)T_s \\ i_{L2-OFF}(t-DT_s-(n-1)T_s) & \text{when } DT_s + (n-1)T_s \leq t < nT_s \end{cases}$$

$$v_{Cs}(t) = \begin{cases} v_{Cs-ON}(t-(n-1)T_s) & \text{when } (n-1)T_s \leq t < DT_s + (n-1)T_s \\ v_{Cs-OFF}(t-DT_s-(n-1)T_s) & \text{when } DT_s + (n-1)T_s \leq t < nT_s \end{cases}$$

where n is the switching interval for $n \in \mathbb{N}$ and $n > 0$. The subscript *ON* refers to the on interval and similarly the subscript *OFF* refers to the off interval. The complete equations are derived in the section that follows however still maintaining the assumptions for C_{in} and C_{out}. The assumptions limit the direct applicability of the equations such as, the change in the average current with a changing load cannot be clearly ascertained. Nonetheless the equations are useful in illustrating the operation at a fundamental level. The equations also allow for various aspects of the circuit not possible with a circuit simulator to be assessed.

2.2 Piecewise Linear Analysis

In order to derive the equations that describe the waveforms in figure 2.3, the interaction between the various circuit elements is first considered. The on interval is analysed by considering the circuit in figure 2.2(a). Noting that the current enters the dotted terminals in both inductors, the circuit operation with the quantities of interest can be described by equations 2.1a to 2.1c.

$$V_{in} = L_1 \frac{di_{L1}(t)}{dt} + M \frac{di_{L2}(t)}{dt} \tag{2.1a}$$

$$v_{Cs}(t) = L_2 \frac{di_{L2}(t)}{dt} + M \frac{di_{L1}(t)}{dt} \tag{2.1b}$$

$$i_{L2}(t) = -C_s \frac{dv_{Cs}(t)}{dt} \tag{2.1c}$$

During the off interval as in figure 2.2(b), with the switch S_1 open and switch S_2 closed the circuit operation with the quantities of interest can be described by equations 2.2a to 2.2c.

$$V_{in} = L_1 \frac{di_{L1}(t)}{dt} + M \frac{di_{L2}(t)}{dt} + v_{Cs}(t) + V_{out} \tag{2.2a}$$

$$V_{out} = -L_2 \frac{di_{L2}(t)}{dt} - M \frac{di_{L1}(t)}{dt} \tag{2.2b}$$

$$i_{L1}(t) = C_s \frac{dv_{Cs}(t)}{dt} \tag{2.2c}$$

From the two sets of equations the solution to each quantity can now be obtained. Given the interdependency amongst the terms, it may in general be more convenient to solve for some quantities before others. The solutions to these equations are however presented in an unordered manner and hence may occasionally make reference to other equations derived in later subsections.

2.2.1 Inductor L1 Dynamics

On interval

The current through inductor L_1 for the on interval is obtained by using equations 2.1a and 2.1b. $\frac{di_{L2}}{dt}$ is made to be the subject of the formula in equation 2.1b and substituted in equation 2.1a, which can be rewritten as equation 2.3.

$$\frac{di_{L1}(t)}{dt} = \frac{V_{in}}{L_1 - \frac{M^2}{L_2}} - \frac{M}{L_2} \frac{v_{Cs}(t)}{L_1 - \frac{M^2}{L_2}} \tag{2.3}$$

Equation 2.3 is solved using integration which can be set up as

$$i_{L1-ON}(t) - i_{L1-ON}(0) = \int_0^t \frac{V_{in}}{L_1 - \frac{M^2}{L_2}} - \frac{M}{L_2} \frac{v_{Cs-ON}(\tau)}{L_1 - \frac{M^2}{L_2}} \, d\tau$$

Solving the integral requires knowledge of the voltage across the capacitor C_s during the on interval, which is given by equation 2.11. After manipulation the current through inductor L_1 during the on interval for a coupled inductor SEPIC is found to be given by equation 2.4.

$$\begin{aligned} i_{L1-ON}(t) = I_{L1-0} + \frac{M}{L_1} I_{L2-0} + \frac{V_{in}}{L_1 - \frac{M^2}{L_2}} \, t - \frac{M^2}{L_1^2} \frac{V_{in}}{L_2 - \frac{M^2}{L_1}} \, t \\ - \frac{M}{L_1} \sqrt{\frac{C_s}{L_2 - \frac{M^2}{L_1}}} \left(V_{Cs-0} - \frac{M}{L_1} V_{in} \right) sin \left(\frac{t}{\sqrt{C_s (L_2 - \frac{M^2}{L_1})}} \right) \\ - \frac{M}{L_1} I_{L2-0} cos \left(\frac{t}{\sqrt{C_s (L_2 - \frac{M^2}{L_1})}} \right) \end{aligned} \tag{2.4}$$

Off interval

The current through inductor L_1 in the off interval is obtained using equations 2.2a, 2.2b and 2.2c. By making $\frac{di_{L2}}{dt}$ the subject of the formula in equation 2.2b and considering the capacitor voltage in equation 2.2c, after substitution equation 2.2a can be rewritten as equation 2.5.

$$V_{in} = L_1\frac{di_{L1}(t)}{dt} + M\left(-\frac{M}{L_2}\frac{di_{L1}(t)}{dt} - \frac{V_{out}}{L_2}\right) + \frac{1}{C_s}\int i_{L1}(t)dt + v_{Cs-ON}(DT_s) + V_{out} \quad (2.5)$$

After differentiating with respect to time equation 2.5 gives rise to a homogeneous differential equation (DE)

$$\frac{d^2 i_{L1}(t)}{dt^2} + \frac{1}{C_s(L_1 - \frac{M^2}{L_2})}i_{L1}(t) = 0$$

An assumed solution of the standard form as in equation 2.6 is used to solve the DE, where $x(t)$ is the function of interest. A review of solving the DE is given in [24].

$$x(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \quad (2.6)$$

From inspection it can be shown that

$$s_1, s_2 = \pm j\frac{1}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}$$

Given the initial conditions and their relation to the coefficients

$$\begin{aligned} i_{L1-OFF}(0) =& i_{L1-ON}(DT_s) = A_1 + A_2 \\ \frac{di_{L1-OFF}(0)}{dt} =& \left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right)\frac{1}{L_1 - \frac{M^2}{L_2}} \\ =& A_1 j\frac{1}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}} - A_2 j\frac{1}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}} \end{aligned}$$

A_1 and A_2 are found to be

$$A_1 = \frac{i_{L1-ON}(DT_s)}{2} - \frac{j}{2}\sqrt{\frac{C_s}{L_1 - \frac{M^2}{L_2}}}\left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right)$$

$$A_2 = \frac{i_{L1-ON}(DT_s)}{2} + \frac{j}{2}\sqrt{\frac{C_s}{L_1 - \frac{M^2}{L_2}}}\left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right)$$

Substituting everything into the standard form of equation 2.6 and manipulating the expression, the current through inductor L_1 in the off interval for a coupled inductor SEPIC is found to be given by equation 2.7.

$$i_{L1-OFF}(t) = i_{L1-ON}(DT_s)cos\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right) + \tag{2.7}$$

$$\sqrt{\frac{C_s}{L_1 - \frac{M^2}{L_2}}}\left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right) sin\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right)$$

2.2.2 Inductor L2 Dynamics

On interval

The current through inductor L_2 during the on interval is found using equations 2.1a and 2.1b as well as equation 2.1c in integral form. $\frac{di_{L1}}{dt}$ is made to be the subject of the formula in equation 2.1a and substituted in equation 2.1b, which can be rewritten as equation 2.8.

$$-\frac{1}{C_s}\int i_{L2}(t)dt + V_{Cs-0} = L_2\frac{di_{L2}(t)}{dt} + \frac{M}{L_1}V_{in} - \frac{M^2}{L_1}\frac{di_{L2}(t)}{dt} \tag{2.8}$$

After differentiation with respect to time, equation 2.8 gives rise to the homogeneous DE

$$\frac{d^2i_{L2}(t)}{dt^2} + \frac{1}{C_s(L_2 - \frac{M^2}{L_1})}i_{L2}(t) = 0$$

An assumed solution of the standard form as in equation 2.6 is used to solve the DE. Given the initial conditions and their relation to the coefficients

$$i_{L2-ON}(0) = I_{L2-0} = A_1 + A_2$$

$$\begin{aligned}\frac{di_{L2-ON}(0)}{dt} &= \frac{V_{Cs-0}}{L_2 - \frac{M^2}{L_1}} - \frac{\frac{M}{L_1}V_{in}}{L_2 - \frac{M^2}{L_1}} \\ &= A_1 j\frac{1}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}} - A_2 j\frac{1}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\end{aligned}$$

A_1 and A_2 are found to be

$$A_1 = \frac{I_{L2-0}}{2} - \frac{j}{2}\sqrt{\frac{C_s}{L_2 - \frac{M^2}{L_1}}}\left(V_{Cs-0} - \frac{M}{L_1}V_{in}\right)$$

$$A_2 = \frac{I_{L2-0}}{2} + \frac{j}{2}\sqrt{\frac{C_s}{L_2 - \frac{M^2}{L_1}}}\left(V_{Cs-0} - \frac{M}{L_1}V_{in}\right)$$

Substituting everything into the standard form of equation 2.6 and manipulating the expression, the current through inductor L_2 during the on interval for a coupled inductor SEPIC is found to given by equation 2.9.

$$i_{L2-ON}(t) = I_{L2-0} cos\left(\frac{t}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right) + \sqrt{\frac{C_s}{L_2 - \frac{M^2}{L_1}}}\left(V_{Cs-0} - \frac{M}{L_1}V_{in}\right) sin\left(\frac{t}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right) \tag{2.9}$$

Off interval

For the off interval the current through inductor L_2 is obtained using equation 2.2a, the derived capacitor voltage of equation 2.12 and by making $\frac{di_{L1}}{dt}$ the subject of the formula in equation 2.2b to give rise to

$$\frac{di_{L2}(t)}{dt} = \frac{1}{M - \frac{L_1 L_2}{M}}\left(V_{in} + V_{out}\left(\frac{L_1}{M} - 1\right) - v_{Cs}(t)\right)$$

which is solved by integration in the form

$$i_{L2-OFF}(t) - i_{L2-OFF}(0) = \frac{1}{M - \frac{L_1 L_2}{M}} \int_0^t V_{in} + V_{out}\left(\frac{L_1}{M} - 1\right) - v_{Cs-OFF}(\tau)\, d\tau$$

yielding the solution as in equation 2.10.

$$\begin{aligned} i_{L2-OFF}(t) = & \frac{1}{M - \frac{L_1 L_2}{M}}\left[\left(\frac{L_1}{M} - \frac{M}{L_2}\right) V_{out}\, t + \right. \\ & \left(L_1 - \frac{M^2}{L_2}\right) i_{L1-ON}(DT_s)\left(cos\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right) - 1\right) + \\ & \left.\sqrt{C_s(L_1 - \frac{M^2}{L_2})}\left(V_{in} + V_{out}\left(\frac{M}{L_2} - 1\right) - v_{Cs-ON}(DT_s)\right) sin\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right)\right] \\ & + i_{L2-ON}(DT_s) \end{aligned} \tag{2.10}$$

2.2.3 Capacitor Cs Dynamics

On interval

The voltage across capacitor C_s during the on interval is solved from considering equation 2.1c and rewriting the equation in a general integral form as

$$v_{Cs}(t) = -\frac{1}{C_s}\int_0^t i_{L2}(\tau) d\tau + V_{Cs-0}$$

Substituting the derived inductor current in the on interval as in equation 2.9, the integral is written as

$$v_{Cs-ON}(t) = -\frac{1}{C_s}\int_0^t I_{L2-0} cos\left(\frac{\tau}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right)$$

$$+\sqrt{\frac{C_s}{L_2 - \frac{M^2}{L_1}}}\left(V_{Cs-0} - \frac{M}{L_1}V_{in}\right) sin\left(\frac{\tau}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right) d\tau + V_{Cs-0}$$

After some manipulation the voltage across capacitor C_s during the on interval in the coupled inductor SEPIC is then found to be given by equation 2.11.

$$v_{Cs-ON}(t) = \left(V_{Cs-0} - \frac{M}{L_1}V_{in}\right) cos\left(\frac{t}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right) \tag{2.11}$$

$$-\sqrt{\frac{L_2 - \frac{M^2}{L_1}}{C_s}} I_{L2-0} sin\left(\frac{t}{\sqrt{C_s(L_2 - \frac{M^2}{L_1})}}\right) + \frac{M}{L_1}V_{in}$$

Off interval

The voltage across capacitor C_s during the off interval is obtained from considering equation 2.2c and rewriting the equation in a general integral form as

$$v_{Cs}(t) = \frac{1}{C_s}\int_0^t i_{L1}(\tau)d\tau + v_{Cs-ON}(DT_s)$$

Substituting the derived inductor current in the off interval as in equation 2.7, the integral is written as

$$v_{Cs-OFF}(t) = \frac{1}{C_s}\int_0^t i_{L1-ON}(DT_s) cos\left(\frac{\tau}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right) +$$

$$\sqrt{\frac{C_s}{L_1 - \frac{M^2}{L_2}}}\left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right) sin\left(\frac{\tau}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right) d\tau$$

$$+ v_{Cs-ON}(DT_s)$$

After some manipulation the voltage across capacitor C_s during the off interval in the coupled inductor SEPIC is then found to be given by equation 2.12.

$$v_{Cs-OFF}(t) = \sqrt{\frac{L_1 - \frac{M^2}{L_2}}{C_s}} i_{L1-ON}(DT_s) sin\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right) - \tag{2.12}$$

$$\left(V_{in} + \frac{M}{L_2}V_{out} - V_{out} - v_{Cs-ON}(DT_s)\right) cos\left(\frac{t}{\sqrt{C_s(L_1 - \frac{M^2}{L_2})}}\right)$$

$$+ V_{in} + \frac{M}{L_2}V_{out} - V_{out}$$

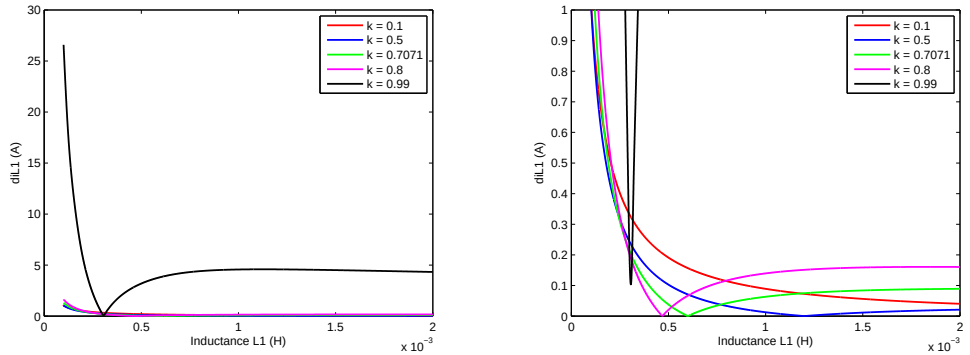
The correctness of the equations was established through a comparison to simulated waveforms from which agreement was observed. These waveforms can be seen in appendix A.

As mentioned earlier the equations allow for various aspects of the circuit not possible with a circuit simulator to be assessed. This includes a sensitivity analysis as well as things like the effect of inductor coupling on the converter's ripple. Understanding the effect of inductor coupling on the converter's ripple helps in finding the optimum operating point. From this some of the design specifications can be formulated.

2.3 Converter Ripple Analysis

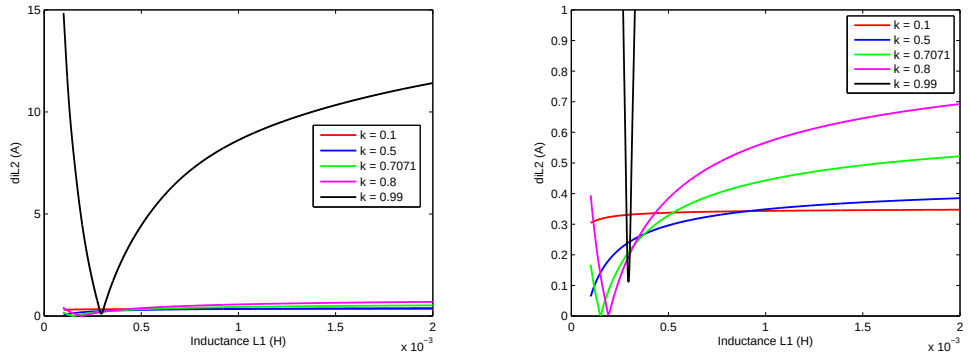
In this section the derived equations are applied in assessing the ripple of the converter for a varying inductance at different coupling values. The ripple magnitude (Δx) associated with a component is defined in figure 2.3 as the difference between the peak value and the average value of a quantity of that component. The ripple magnitude in a converter is of significance as it is used in specifying the sizes of the reactive components.

The average ripple magnitudes for a coupled inductor SEPIC are presented in figure 2.4. The ripple magnitudes in figure 2.4(a) are generated using equations 2.4 and 2.7 from which the average ripple magnitude over successive time intervals is obtained. Similarly the ripple magnitudes in figure 2.4(c) are generated using equations 2.9 and 2.10 from which the average ripple magnitude over successive time intervals is obtained. Lastly the ripple magnitudes in figure 2.4(e) are generated using equations 2.11 and 2.12 from which the average ripple magnitude over successive time intervals is obtained. An arbitrary operating condition but for the converter in continuous conduction mode is selected to study the effect inductor coupling on the ripple. The component values are obtained using a circuit level design which is reviewed in appendix B. The converter is operated at $50kHz$ with $D = 43\%$, $V_{in} = 24V$, $L_2 = 300\mu H$ and $C_s = 22\mu F$. L_1 is varied from $100\mu H$ to $2mH$ for each different value of the coupling coefficient k.



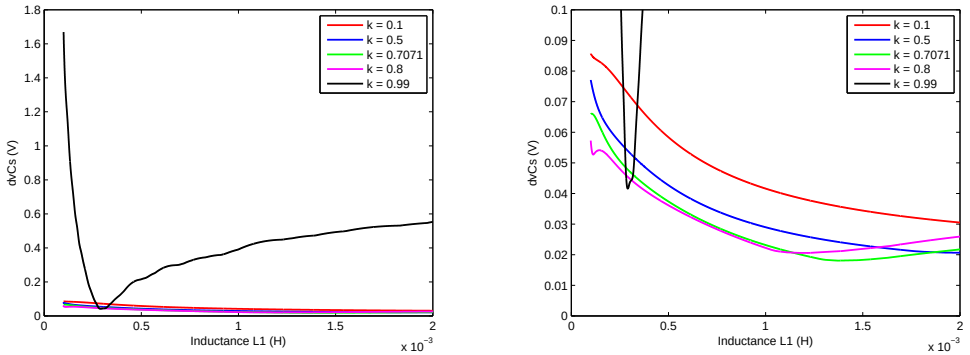
(a) Inductor L1 current ripple

(b) Inductor L1 current ripple (magnified)



(c) Inductor L2 current ripple

(d) Inductor L2 current ripple (magnified)



(e) Capacitor Cs voltage ripple

(f) Capacitor Cs voltage ripple (magnified)

Figure 2.4: Coupled inductor SEPIC ripple magnitudes for a varying inductance L1.

Inspection of figure 2.4(b) and figure 2.4(d) indicates two interesting operating regions. The first region involves a case when the current ripple in *both* inductors is lowest for a specific value of k and this occurs when $k = 0.99$ (that is for increased coupling) and when $L_1 = L_2 = 300\mu H$. At this point the magnitude of current ripple in both inductors is $128mA$, which is almost half than when the inductor coupling is poor.

The second region worth noting is when the current ripple in either inductor is zero. Investigation of these points indicates that the coupling coefficient and ratio of inductor values have a specific relation which has been noted to result in 'zero' ripple operation [6].

In the work [6] it is demonstrated that for the condition of equation 2.13 a ripple free current through inductor L_1 can be obtained.

$$k = \sqrt{\frac{L_2}{L_1}} \tag{2.13}$$

And for the condition of equation 2.14 a ripple free current through inductor L_2 can be obtained.

$$k = \sqrt{\frac{L_1}{L_2}} \tag{2.14}$$

In practice complete elimination of the ripple is not possible but the proposed condition does result in a very small ripple. A trade-off associated with the 'zero' ripple technique is that the other inductor will have a significantly larger ripple. Furthermore the capacitor voltage ripple is not necessarily superior to other operating regions. In general the ripple magnitudes for the converter in figure 2.4 are similar when inductor L_1 is kept constant and inductor L_2 varied, with the main difference being that the curves for L_1 and L_2 are swapped.

2.4 Magnetic Component Specifications

The preceding section raises the question as to which inductor size and coupling configuration is more suited. Besides being able to obtain an almost zero inductor current ripple, there has been another indication of a benefit associated with having some leakage inductance in a coupled inductor SEPIC. It has been shown that loose coupling can reduce AC current losses resulting in efficiency improvements of 1% [8]. Also a low input current ripple achieved from having some leakage inductance is said to be associated with good EMI performance [8] however the mechanism is not well established. On the other hand, tight coupling between the inductors also has some benefits. For equal inductor values their magnitude can be halved when compared to an uncoupled case, as established in the preceding section. Tight coupling to minimise any leakage inductance has also been demonstrated to reduce the high voltage spikes and ringing that occurs at the MOSFET drain source voltage during the turning off instant [7]. This is associated with less noise.

The design and construction of tightly coupled inductors appears to be relatively simpler than the design and construction of coupled inductors with a specific amount of leakage inductance. The suggested efficiency benefits of a coupled inductor structure with some leakage appear to be marginal for this application. Also such a design is associated with more ringing during the switching instances. Hence for purposes of this study the magnetic components will be:

- $L_1 = L_2$
- $k \approx 1$

This configuration implies a reduced physical size and cost of the magnetic component in the circuit compared to an uncoupled case. This is due to the inductor values being half of the uncoupled case and the single magnetic core that is used. Other configurations such as the 'zero' current ripple technique discussed earlier may be suitable for other applications.

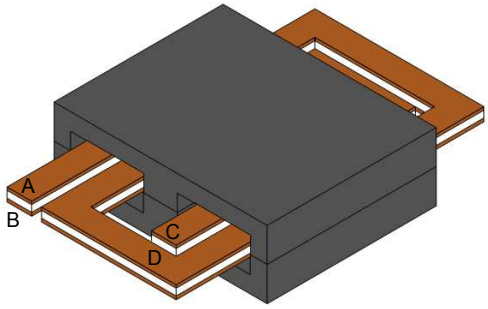
Chapter 3

The Two Conductor Planar Integrated Passive

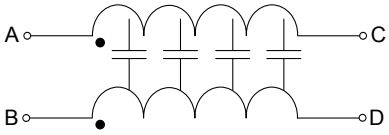
In order to realise a coupled inductor SEPIC or any other circuit using planar integrated passive components it is necessary to have a fundamental understanding of the integrated component structure and resulting behaviour. So in this chapter a two conductor planar integrated passive is reviewed. A working model for the planar integrated passive component is firstly established. Then the various terminal uses of the two conductor structure are evaluated from which various circuit functions are established. The established circuit functions are also considered in a context in which they are building blocks towards constructing more complex assemblies. The chapter concludes with considerations necessary when combining multiple integrated passive modules.

3.1 Modelling Approaches

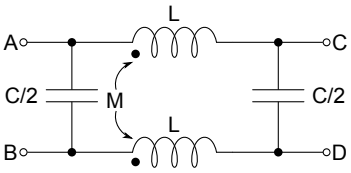
A modern two conductor integrated passive structure is again presented in figure 3.1 and consists of two conductors sandwiching a dielectric layer, all of which are enclosed by a magnetic material. Maintaining the same terminal labels, the circuit level impression is as in figure 3.1(b). It indicates the inductors realised by the top and bottom conductors as well as the capacitance distributed along the structure. A simple lumped parameter model of the structure which will be referred to as the split-c model is given in figure 3.1(c). The model has in some work been incorrectly referred to as Reeves' model [25]. This has occurred where the work in [12] has been cited with reference to the model even though the work makes no mention of the model. The model is similar to some representations of transformers that have their inter-winding capacitance included [26]. It is also similar to a pi model in a lumped approximation of a transmission line [27], that is if the loss components are ignored. The two inductors on the split-c model represent the self-inductance of the two conductors. The magnetic coupling that arises from the structure being enclosed in a



(a) General structure.



(b) General circuit impression.



(c) Split-c model.

Figure 3.1: Typical planar integrated structure.

magnetic core is represented by a mutual inductance M. The total capacitance formed by the two conducting plates and dielectric is represented as two split capacitances at the ends. The structure of figure 3.1(a) has been described by various other lumped parameter models as well as distributed parameter models. In this dissertation focus is given to the split-c model as it is intuitive and useful for general design purposes. The model does however have limitations which are discussed later in the chapter. The relevance of other modelling work and the challenges associated with their use is first considered.

Motivation for the need of distributed models is because integrated passive components typically exhibit high frequency characteristics which cannot be predicted by the existing lumped parameter models. These high frequencies characteristics can contribute to increased EMI effects [28]. They may also be in the form of high frequency resonances which can be of significance in the design of resonant sensitive applications. Even though distributed models can predict these high frequency artifacts they still only enjoy limited application. One such example is of a proposed generalised transmission structure to model integrated passive components [29]. It is an extension of the classic transmission line model for a two conductor structure and it aims to account for unbalanced currents that occur on the structure. The model was demonstrated to describe characteristics of the integrated structure well into the high frequencies but has been regarded to be complicated and unsuitable for general design purposes [28]. A similar model has been discussed but considers the two conductors as two separate transmission lines with an electric coupling to a ground plane as well as electric and magnetic coupling to each other [30]. Similarly the model has also been found to be complicated and unsuitable for general design purposes. Another unpopular distributed model for integrated passive components has also been proposed [31], and its issue is asso-

ciated with the limited detail on parameter calculation that is provided. Furthermore the model was later described as complex, difficult to analyse and simulate [11]. Other efforts on distributed models have been focused on two terminal devices which also happen to have other geometrical differences [14, 32] when compared to the indicated planar structure of figure 3.1 and as such cannot be directly applied. Apart from the inherent complexities, the application of some of the distributed models is also hindered by more work which is still required in developing specialised simulation tools [33, 34].

In general for cases where the physical length of an integrated structure is significantly smaller than the wavelength of the signals in a circuit, lumped parameter models suffice and may also be preferable as they are easier to apply. Lumped parameter models have been regarded as useful for quick design and verification purposes [28, 35]. The existing lumped parameter models can be loosely classified as ones which consider:

- Principal components as well as loss and reactive parasitics.
- Principal components and loss parasitics only.
- Principal components only.

Some examples of each are considered. The first model to note is an extension of the split-c model however for a series resonator which contains both reactive parasitcs and loss parasitics [36]. The most significant contribution of the work related to the model is in the computation of the intra-winding capacitance of each inductor. The presence of various loss components are only acknowledged as their origin and general effect on the frequency response of the circuit is not well substantiated. Besides this model a transformer based lumped parameter model has also been suggested [35], which includes details of loss parasitics and reactive parasitics. The determination of some of the parasitics is glossed over but nonetheless the model does give a good indication of the parasitic aspects to consider which could impact the performance of the circuit. A lumped parameter model [37] that aimed to describe an inductor-capacitor hybrid [12] has also been suggested in an effort to indicate the practical limitations that the conductor resistance has on the operation of the structure. Apart from the principal components, this model only considers the winding resistance. Other lumped parameter models have also been proposed but are limited in application because the work only focused on a two terminal device [15]. The split-c model only considers the principal components. It is imagined that the suitability of each lumped parameter model class would be determined by the application in question.

In the next section the split-c model is applied in a study of the terminal uses of a two conductor integrated passive structure. The study will provide insight into the behaviour of a practical two conductor integrated passive module and also provide insight on the use

of the split-c model. Other work towards evaluating the operation for different terminal connections on an integrated passive component has been done [38]. The evaluation was for a three-layered structure (a structure composing of three conductors separated by two high permittivity dielectrics all enclosed in a magnetic core). The work employed a different model and involved characterising the terminal response of the three-layered structure for all possible configurations which were established through an exhaustive search. The work also highlighted key structural behaviour associated with certain interconnections and layer manipulation.

3.2 Terminal Uses

For a two conductor integrated LC module such as in figure 3.1 it is possible to derive a parallel resonant circuit, a series resonant circuit, a low-pass filter, and a high-pass filter all of which can also be used just as an inductor and capacitor. In this section the indicated circuit functions are analysed in detail using the split-c model as a starting basis and compared with experimental results. For the experiment, a structure with a single turn is employed by which some parasitics can be neglected. A photograph of the structure is presented in figure 3.2. Again the structure is composed of two conductors sandwiching a dielectric layer which are all enclosed in a magnetic core. The self-inductance of the conductors is determined using equation 3.1.

$$L = A_{core} \frac{\mu_0}{l_{path} \frac{1}{\mu_r} + l_g} \tag{3.1}$$

In equation 3.1 A_{core} is the area of the centre leg of the magnetic core, μ_0 is the permeability of free space, μ_r is the relative permeability of the core, l_{path} is the length of the magnetic path, and l_g is the length of the air gap.

The capacitance realised by the two conducting plates and dieletric is determined using equation 3.2.

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{3.2}$$

In equation 3.2 A is the effective area of the plates, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the material, and d is the separation distance between the plates. For the structure in figure 3.2 the self inductance of the conductors is $37\mu H$ and the total capacitance of the structure is $117nF$ at low frequencies, which are obtained using equation 3.1 and equation 3.2 respectively. The material used for the two conductor module is C-ply made by 3M and the magnetic core is composed of five E64 and five PLT64 ferrite cores. The dimensions of the structure are $27.3 \times 7.6 \times 1.7$ $(L \times W \times H)$ cm^3. Close to unity coupling exists between the two inductors.

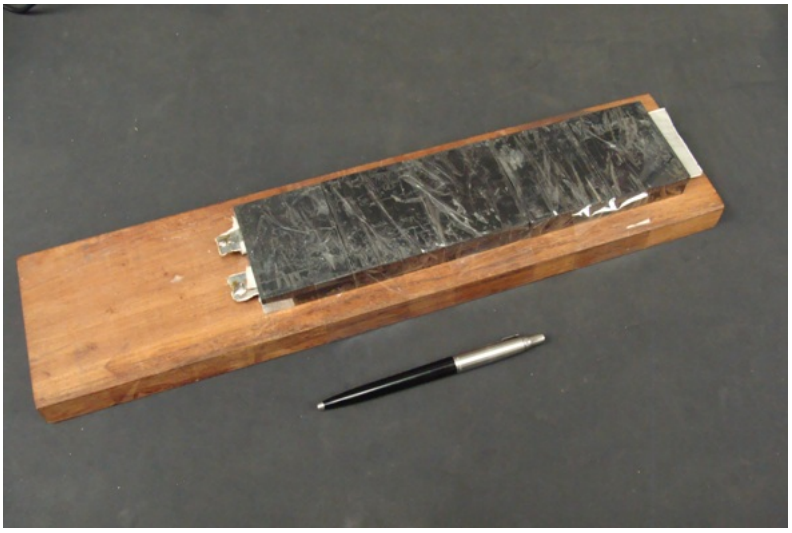
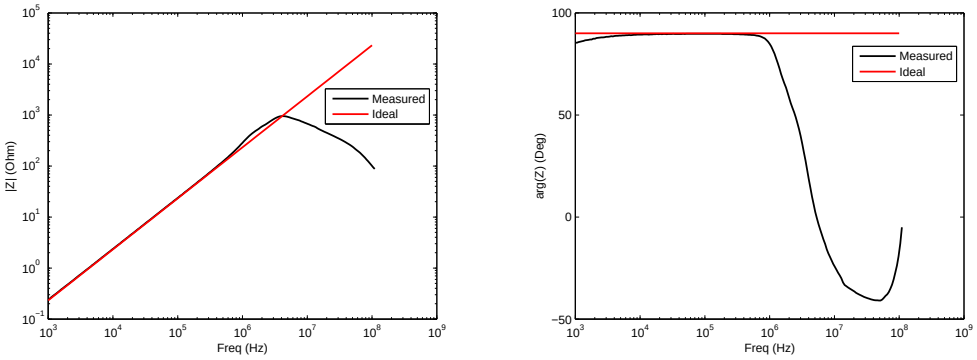


Figure 3.2: Photograph of experimental prototype.

In the rest of the section where the split-c model is used the self inductance and the total capacitance are set to equal the values of the physical structure. On the impedance plots the ideal plot refers to the analytic result of the split-c model and the measured plot refers to the actual measurement of the prototype. All the impedance measurements are small signal measurements. Also on all the measurements copper strips were used as the leads, each having the dimensions $8.3 \times 1.8 \times 0.05$ $(L \times W \times H)$ cm^3. The various terminal uses will now be considered and to begin with, the terminal usage for an inductor function will be discussed.

3.2.1 Inductor Function

An inductor only function is obtained by using a conducting sheet only, that is with no electric field perpendicular to the current flow. The general objective however is to integrate an inductor function with other functions as much as possible. Although not economical, a predominately inductive function can be obtained on the integrated structure of figure 3.1 by using terminals at opposite ends of a conductor such as A and C. The impedance of an ideal inductor is compared to a measured impedance of the structure in figure 3.2 at terminals A and C. The comparison is illustrated in figure 3.3. On the plots agreement between the ideal and measured value is observed until 794.3kHz. At higher frequencies the measured value is dominated by a stray capacitance and losses. The losses are a combination of core losses and conductor related losses due to the skin effect which becomes significant at high frequencies.



(a) Magnitude of impedance.

(b) Phase of impedance.

Figure 3.3: Frequency response of inductor function on the integrated structure.

3.2.2 Capacitor Function

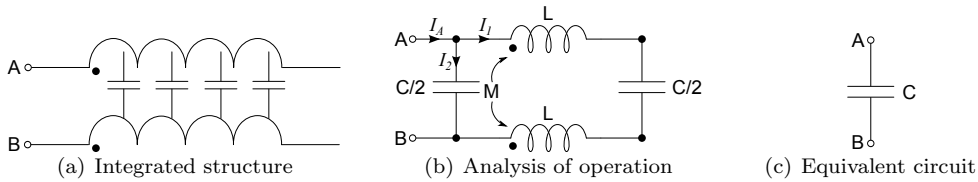
A capacitor function can be obtained through the use of the same side terminals such as A and B (or C and D) as shown in figure 3.4(a), with the equivalent circuit as in figure 3.4(c), where C is the total capacitance between the conducting plates. The equivalent circuit can be obtained from a consideration of the split-c model as in figure 3.4(b) and by determining the effective impedance across terminals A and B. The impedance across terminals A and B is defined by equation 3.3.

$$Z_{AB} = \frac{V_{AB}(\omega)}{I_A(\omega)} = \frac{V_{AB}(\omega)}{I_1(\omega) + I_2(\omega)} \tag{3.3}$$

After manipulation the resulting impedance is given by equation 3.4 and is simplified to describe a capacitor as in equation 3.5 for $L = M$. The impedance of an ideal capacitor and the measured impedance across terminals A and B are compared in figure 3.5. On the plots agreement between the ideal and measured value is noted until 712.65kHz where the measured value starts to deviate. At higher frequencies the measured value is dominated by the lead inductance.

$$Z_{AB} = \frac{j\omega(L-M) + \frac{1}{j\omega C}}{1 - \frac{\omega^2 C(L-M)}{2}} \tag{3.4}$$

$$Z_{AB} = \frac{1}{j\omega C} \tag{3.5}$$

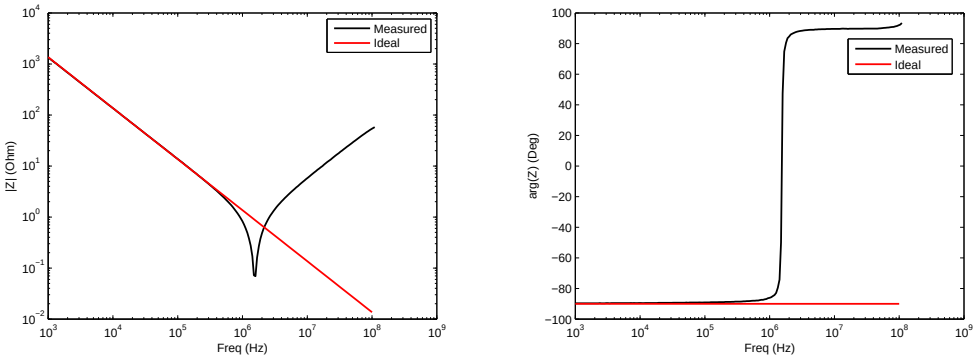


(a) Integrated structure

(b) Analysis of operation

(c) Equivalent circuit

Figure 3.4: Capacitor function on the integrated structure.



(a) Magnitude of impedance.

(b) Phase of impedance.

Figure 3.5: Frequency response of capacitor function on the integrated structure.

3.2.3 Series Resonator Function

For a two conductor integrated structure a series resonator is obtainable through the use of the terminals at diagonally opposite ends such as in figure 3.6(a) with the equivalent circuit as in figure 3.6(c). The equivalent circuit can be obtained from a consideration of the split-c model as in figure 3.6(b) and by determining the effective impedance across terminals A and D. The impedance across terminals A and D is defined by equation 3.6.

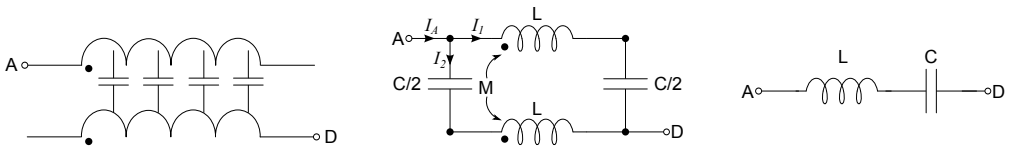
$$Z_{AD} = \frac{V_{AD}(\omega)}{I_A(\omega)} = \frac{V_{AD}(\omega)}{I_1(\omega) + I_2(\omega)} \tag{3.6}$$

After manipulation the resulting impedance is given by equation 3.7 and is simplified as in equation 3.8. For $L = M$ equation 3.9 is obtained which describes a circuit with an inductor and a capacitor in series as shown in figure 3.6(c). L is the self inductance of one conductor and C is total capacitance established by the two conductors and dielectric. The ideal impedance and measured impedance of a series resonant function are compared in figure 3.7. The ideal and measured value match until 897.15kHz. At higher frequencies the parasitics present in the inductor function also dominate the series resonator function.

$$Z_{AD} = \frac{V_{AD}(\omega)}{\frac{V_{AD}(\omega)}{j\omega(L+M)+\frac{1}{j\omega\frac{C}{2}}} + \frac{V_{AD}(\omega)}{j\omega(L+M)+\frac{1}{j\omega\frac{C}{2}}}} \tag{3.7}$$

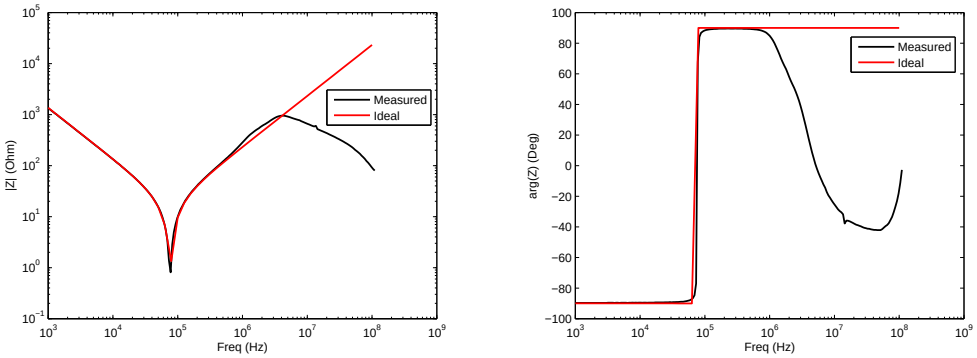
$$Z_{AD} = j\omega\frac{(L+M)}{2} + \frac{1}{j\omega C} \tag{3.8}$$

$$Z_{AD} = j\omega L + \frac{1}{j\omega C} \tag{3.9}$$



(a) Integrated structure (b) Analysis of operation (c) Equivalent circuit

Figure 3.6: Series resonator function on the integrated structure.



(a) Magnitude of impedance. (b) Phase of impedance.

Figure 3.7: Frequency response of series resonator function on the integrated structure.

3.2.4 Parallel Resonator Function

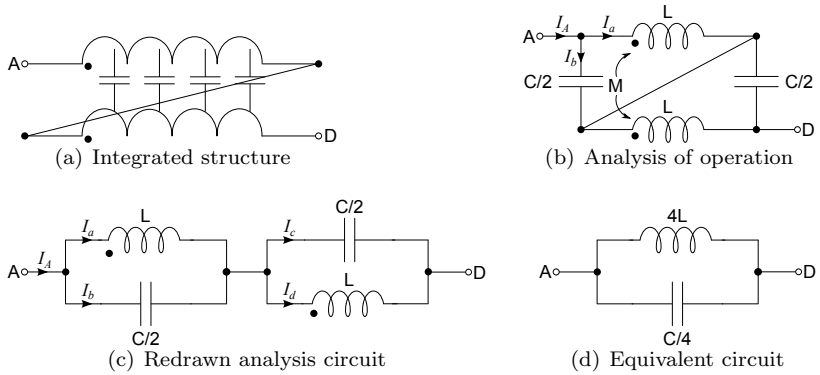
A parallel resonator is obtainable through the use of the terminals at diagonally opposite ends while the other diagonally opposite terminals are short circuited such as in figure 3.8(a). The equivalent circuit is as in figure 3.8(d). Again the equivalent circuit is obtained from a consideration of the split-c model as in figures 3.8(b) and 3.8(c) and by determining the effective impedance across terminals A and D. The impedance across terminals A and D is defined by equation 3.10.

$$Z_{AD} = \frac{V_{AD}(\omega)}{I_A(\omega)} = \frac{V_{AD}(\omega)}{I_a(\omega) + I_b(\omega)} \tag{3.10}$$

After manipulation the resulting impedance is given by equation 3.11. For $L = M$ the equation reduces to equation 3.12 which describes a parallel configuration of an inductor and a capacitor where $C^{'} = \frac{C}{4}$ and $L^{'} = 4L$. In other words the effective capacitance is a quarter of the total capacitance of the structure and the effective inductance is four times that of the original self inductance. The ideal impedance and measured impedance of a parallel resonator function are compared in figure 3.9. There is agreement between the ideal and measured value until 1.023MHz. At higher frequencies the measured value is dominated by the same parasitic elements which dominate the capacitor function.

$$Z_{AD} = \frac{V_{AD}(\omega)}{\frac{1}{j\omega 2(L+M)}V_{AD}(\omega) + j\omega\frac{C}{4}V_{AD}(\omega)} = \frac{1}{\frac{1}{Z_L{}'} + \frac{1}{Z_c{}'}} \tag{3.11}$$

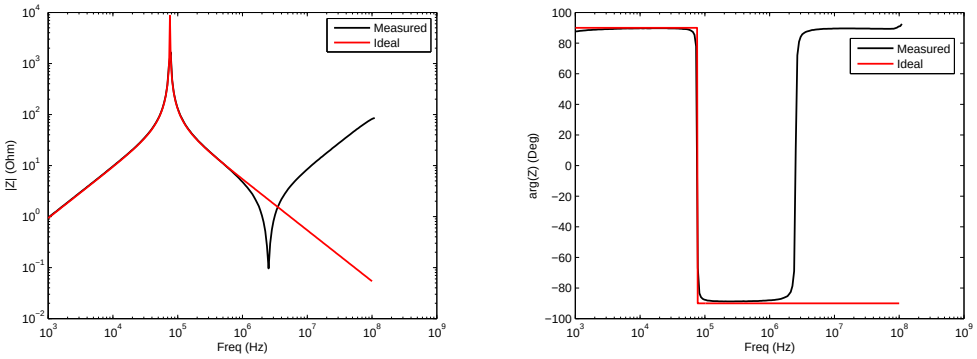
$$Z_{AD} = \frac{j\omega L' \frac{1}{j\omega C'}}{j\omega L' + \frac{1}{j\omega C'}} \tag{3.12}$$



(a) Integrated structure (b) Analysis of operation

(c) Redrawn analysis circuit (d) Equivalent circuit

Figure 3.8: Parallel resonator function on the integrated structure.



(a) Magnitude of impedance. (b) Phase of impedance.

Figure 3.9: Frequency response of parallel resonator function on the integrated structure.

3.2.5 Low Pass Filter Function

A low pass filter function is obtainable through the use of the terminals as in figure 3.10(a) with the equivalent circuit as in figure 3.10(c). The equivalent circuit is derived from consideration of the input impedance, together with an arbitrary load Z_L connected at terminals C and D as in figure 3.10(b). The input impedance is defined by equation 3.13. The currents are found as in equation 3.14 and equation 3.15.

$$Z_{AD} = \frac{V_{AD}(\omega)}{I_A(\omega)} = \frac{V_{AD}(\omega)}{I_1(\omega) + I_2(\omega)} \tag{3.13}$$

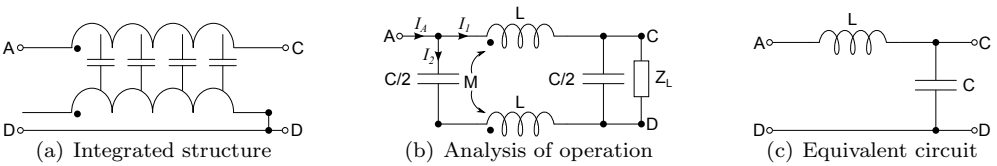
$$I_1 = V_{AD}\frac{1-\frac{j\omega M}{j\omega L+\frac{1}{j\omega C/2}}}{j\omega L+\frac{1}{j\omega C/2+\frac{1}{Z_L}}-\frac{(j\omega M)^2}{j\omega L+\frac{1}{j\omega C/2}}} \tag{3.14}$$

$$I_2 = \frac{V_{AD}}{j\omega M}\left(1-\frac{\left(j\omega L+\frac{1}{j\omega C/2+\frac{1}{Z_L}}\right)\left(1-\frac{j\omega M}{j\omega L+\frac{1}{j\omega C/2}}\right)}{j\omega L+\frac{1}{j\omega C/2+\frac{1}{Z_L}}-\frac{(j\omega M)^2}{j\omega L+\frac{1}{j\omega C/2}}}\right) \tag{3.15}$$

After algebraic manipulation, the resulting impedance is given by equation 3.16. For $L = M$ equation 3.16 simplifies to equation 3.17 which describes an inductor in series with a parallel network of a capacitor and the given impedance Z_L. The ideal impedance of equation 3.17 is compared to the measured impedance of the integrated structure as in figure 3.11. On the plots a match between the ideal and measured value is noted until 1.018MHz. At higher frequencies the measured value is dominated by the same parasitics that dominate the inductor function. In the analysis, a load value of $Z_L = \sqrt{L/C}$ was chosen as it provides a sharp corner frequency.

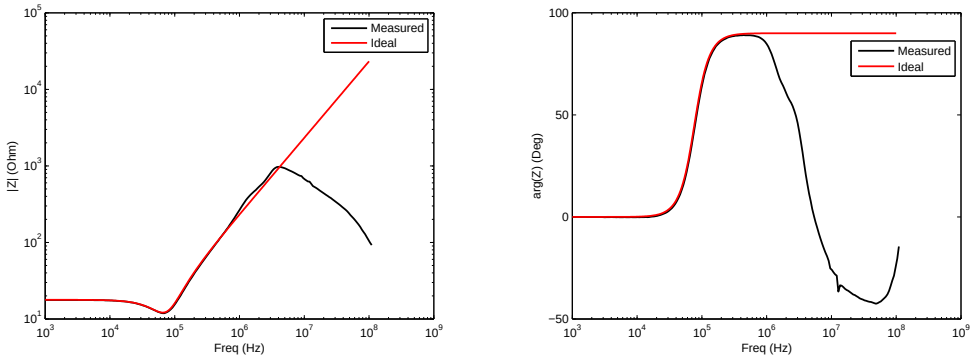
$$Z_{AD} = \frac{(j\omega L)^2-(j\omega M)^2+\frac{j\omega L}{j\omega C/2}+\frac{j\omega L+\frac{1}{j\omega C/2}}{j\omega C/2+\frac{1}{Z_L}}}{j\omega 2(L-M)+\frac{1}{j\omega C/2}+\frac{1}{j\omega C/2+\frac{1}{Z_L}}} \tag{3.16}$$

$$Z_{AD} = j\omega L+\frac{1}{j\omega C+\frac{1}{Z_L}} \tag{3.17}$$



(a) Integrated structure (b) Analysis of operation (c) Equivalent circuit

Figure 3.10: Low pass filter function on the integrated structure.



(a) Magnitude of impedance. (b) Phase of impedance.

Figure 3.11: Input impedance of low pass filter function on the integrated structure.

3.2.6 High Pass Filter Function

A high pass filter function is obtainable through the use of the terminals as in figure 3.12(a) with the equivalent circuit as in figure 3.12(c). The equivalent circuit is derived from consideration of the input impedance, together with an arbitrary load Z_L connected at terminals B and D as in figure 3.12(b). The input impedance is defined by equation 3.18. The currents are found as in equations 3.19 and 3.20.

$$Z_{AD} = \frac{V_{AD}(\omega)}{I_A(\omega)} = \frac{V_{AD}(\omega)}{I_1(\omega) + I_2(\omega)} \tag{3.18}$$

$$I_1 = V_{AD} \frac{\left(\frac{Z_L}{j\omega L + Z_L}\right)(j\omega M - j\omega L) - \frac{1}{j\omega\frac{C}{2}}}{\left(\frac{Z_L}{j\omega L + Z_L}\right)((j\omega M)^2 - (j\omega L)^2) - \frac{1}{j\omega\frac{C}{2}}X} \tag{3.19}$$

where,

$$X = \left[j\omega L + \frac{1}{j\omega\frac{C}{2}} + \frac{j\omega L Z_L}{j\omega L + Z_L} - \frac{(j\omega M)^2}{j\omega L + Z_L} \right]$$

$$I_2 = V_{AD} \frac{\frac{Z_L}{j\omega L + Z_L}\left[(j\omega M)^2 - (j\omega L)^2 - (j\omega M - j\omega L)\left(j\omega M - \frac{j\omega L j\omega M}{j\omega L + Z_L}\right)\right] - \frac{1}{j\omega\frac{C}{2}}A}{\left(\frac{j\omega L Z_L}{j\omega L + Z_L} + \frac{1}{j\omega\frac{C}{2}}\right)\left[\frac{Z_L}{j\omega L + Z_L}((j\omega M)^2 - (j\omega L)^2) - \frac{1}{j\omega\frac{C}{2}}B\right]} \tag{3.20}$$

where,

$$A = \frac{1}{j\omega\frac{C}{2}} + \frac{j\omega L Z_L}{j\omega L + Z_L} + (j\omega L - j\omega M)\left(1 + \frac{j\omega M}{j\omega L + Z_L}\right)$$

$$B = j\omega L + \frac{1}{j\omega\frac{C}{2}} + \frac{j\omega L Z_L}{j\omega L + Z_L} - \frac{(j\omega M)^2}{j\omega L + Z_L}$$

$$Z_{AD} = \frac{\left(\frac{1}{j\omega\frac{C}{2}} + \frac{j\omega L Z_L}{j\omega L + Z_L}\right)\left[\frac{Z_L}{j\omega L + Z_L}((j\omega M)^2 - (j\omega L)^2) - \frac{1}{j\omega\frac{C}{2}}P\right]}{\frac{Z_L}{j\omega L + Z_L}\left[(j\omega M)^2 - (j\omega L)^2 - (j\omega M - j\omega L)Q\right] - \frac{1}{j\omega\frac{C}{2}}R} \tag{3.21}$$

where,

$$P = j\omega L + \frac{1}{j\omega\frac{C}{2}} + \frac{j\omega L Z_L}{j\omega L + Z_L} - \frac{(j\omega M)^2}{j\omega L + Z_L}$$

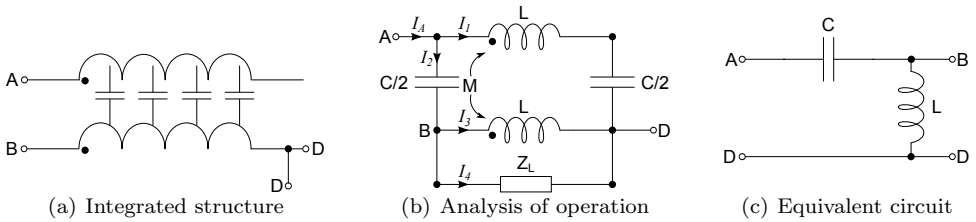
$$Q = j\omega M - \frac{j\omega L j\omega M}{j\omega L + Z_L} - \frac{j\omega L Z_L}{j\omega L + Z_L} - \frac{1}{j\omega\frac{C}{2}}$$

$$R = 2\frac{1}{j\omega\frac{C}{2}} + 2\frac{j\omega L Z_L}{j\omega L + Z_L} + (j\omega L - j\omega M)\left(1 + \frac{j\omega M}{j\omega L + Z_L}\right)$$

After algebraic manipulation, the resulting impedance is given by equation 3.21. For $L = M$ equation 3.21 simplifies to equation 3.22 which describes a capacitor in series with a parallel

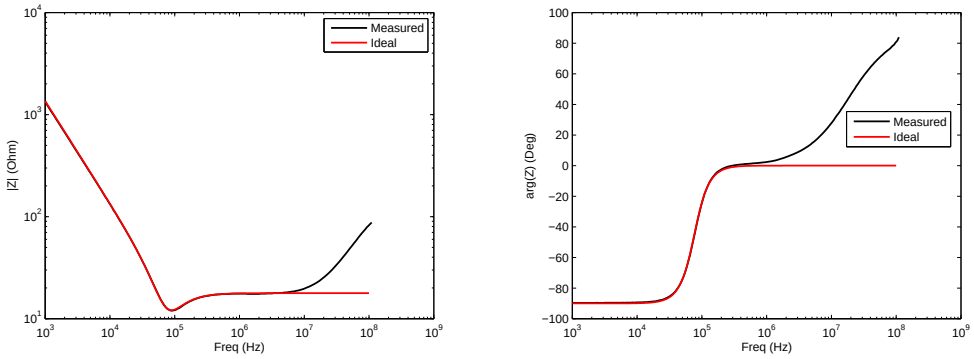
network of an inductor and the given impedance Z_L. The ideal impedance of equation 3.22 is compared to the measured impedance of the integrated structure as in figure 3.13. There is agreement between the ideal and measured values until 955kHz. At high frequencies the measured value is dominated by the same parasitics as the capacitor function. For the analysis, a load value of $Z_L = \sqrt{L/C}$ was chosen for a sharper corner frequency.

$$Z_{AD} = \frac{1}{j\omega C} + \frac{j\omega L Z_L}{j\omega L + Z_L} \tag{3.22}$$



(a) Integrated structure (b) Analysis of operation (c) Equivalent circuit

Figure 3.12: High pass filter function on the integrated structure.



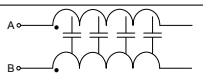
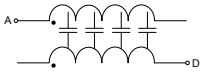
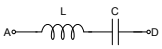
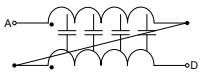
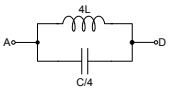
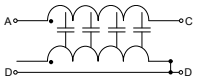
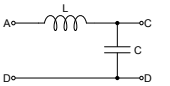
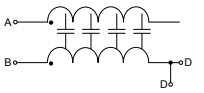
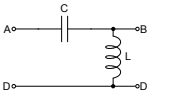
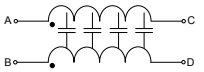
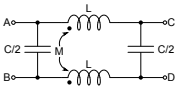
(a) Magnitude of impedance. (b) Phase of impedance.

Figure 3.13: Input impedance of high pass filter function on the integrated structure.

3.2.7 Four Terminal Function

Besides the terminal functions described all four terminals on the two conductor structure may also be used. One known use involves an EMI filter. The split-c model as it is represents a building block typically used in EMI filters. In a barrel equivalent of the planar integrated two conductor structure the four terminals have been used for a source and a load [12]. On the mentioned structure the connections for the source are diagonally opposite and similarly for the load.

Table 3.1: Summary of Circuit Functions.

Circuit Function	Terminal Connections	Equivalent Circuit
Capacitor		
Series resonator		
Parallel resonator		
Low pass filter		
High pass filter		
Four terminal		

3.2.8 Discussion

This section has shown the circuit functions which can be obtained from a two conductor structure. The circuit functions are summarised in table 3.1. In each circuit function the split-c model is in agreement with the measured impedance of a physical two conductor structure till at least 712.65kHz. This demonstrates that the split-c model can be used to model integrated passive structures for low frequencies and possibly up to a lower limit of medium frequencies.

The analysis has largely dealt with cases for $L = M$. The model has not been assessed for cases where $L \neq M$. However it is still expected to be valid even when the coupling is reduced.

3.3 Circuit Functions as Building Blocks

The established circuit functions in the preceding section can also be regarded as building blocks for constructing more complicated integrated passive networks. The equivalent circuits from the split-c model form a useful basis in understanding the lumped parameter representation. When constructing an integrated circuit, an isolated capacitor in a conventional circuit can be realised by the capacitor function and similarly for an inductor where it exists. Where an inductor and capacitor are connected, the other circuit functions may be used to realise the inductance and capacitance. As an example the high pass filter or low pass filter function would be used where access to all three terminals is required. For a parallel LC network the parallel resonator function would be used.

In this idea a building block or a module is two conductors sandwiching a dielectric. The enclosing magnetic core is not regarded as part of the module even though it forms part of the physical structure. If the circuit to be integrated had uncoupled inductors, the definition of a module would have to be revised to consider the magnetic components. In this dissertation, only integrated circuits with all conductors magnetically coupled are considered. The conventional circuits that can be integrated in a structure where all conductors are magnetically coupled, are ones with either a single inductor and those with intended inductor coupling. The rest would require a magnetic structure with shunts to decouple inductances. For integrated circuits where all conductors are magnetically coupled, the design of the enclosing magnetic core is usually considered after the configuration with the building blocks has been established. The idea of using the circuit functions as building blocks is demonstrated through some examples that follow. In the examples, the derivation of complex assemblies is shown and the impedance of each assembly analysed. Before these examples are demonstrated it is worthwhile to note the physical details of the example integrated circuits.

3.3.1 Physical Details of Integrated Circuits

For the integrated circuits that follow in the rest of the chapter, all are the same form as the structure presented in figure 3.2. They all have the dimensions of $27.3 \times 7.6 \times 1.7$ $(L \times W \times H)$ cm^3. Where a module with two conductors sandwiching a dielectric appears, it is constructed from C-ply which is made by 3M. C-ply has a copper thickness of $35\mu m$ and a dielectric thickness of $14\mu m$. The dielectric has a relative permittivity of 16. The magnetic core of the integrated circuits is constructed from an E-PLT ferrite combination which consists of five E64 cores and five PLT64 cores.

The size of the passive components or a single two conductor module is the same as that of the two conductor integrated passive studied in the preceding section. The same size passive components are used as the interest in the study in this section is not on unique operating points but rather the ability to replicate the topologies using integrated passives.

The integration of the various circuits will now be considered.

3.3.2 Integration of Passives in a Custom Network

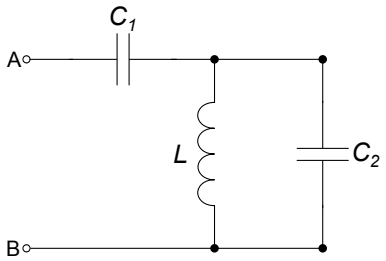
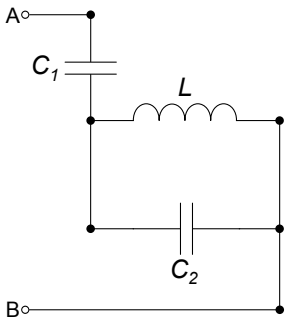


Figure 3.14: Network of passive components.

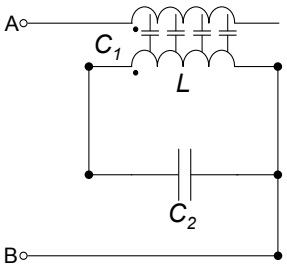
The first network that is integrated using the building blocks is given in figure 3.14. Several methods to integrate it may be used leading to different configurations however with the same functionality. Three different examples are considered.

Integration Using a High Pass Filter Function and a Capacitor Function

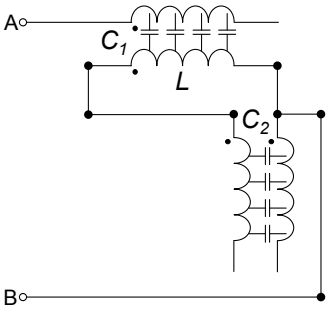
The first set of building blocks that can be used are the high pass filter function and capacitor function as seen in figure 3.15. The high pass filter configuration is used as a general LC. To begin with the network can firstly be redrawn as in figure 3.15(a). C_1 and L are then integrated using a high pass filter function as in figure 3.15(b). Following C_2 is realised by the capacitor function as in figure 3.15(c). The network is then arranged into a vertical stack as in figure 3.15(d) by rotating the C_2 module 90° anti-clockwise and shifting it into place. The vertical stack gives a one dimensional representation of the structure as it appears physically.



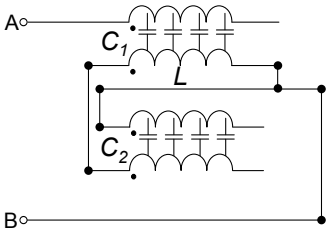
(a) Redrawn network.



(b) Intergration of C_1 and L.



(c) Intergration of C_2.



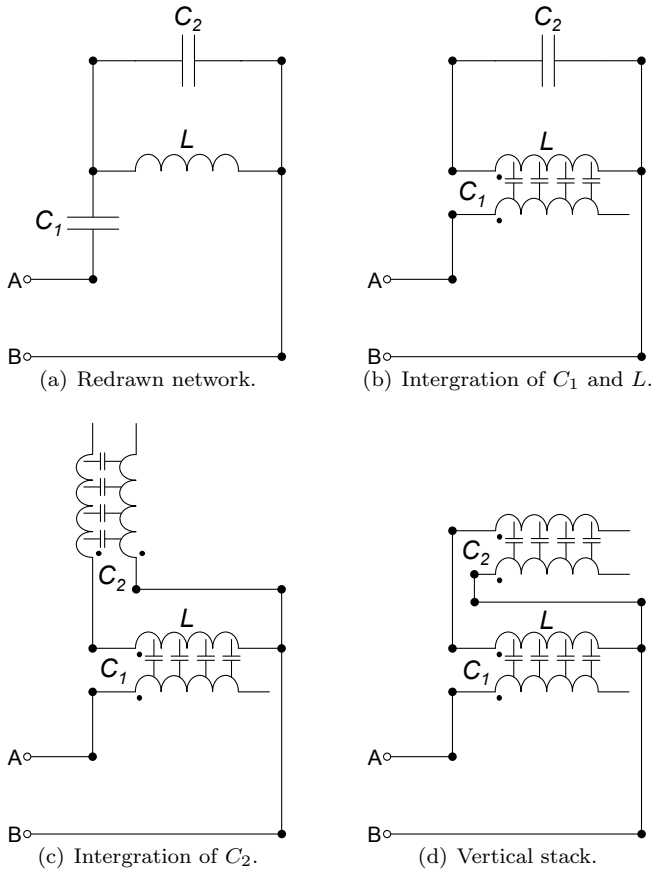
(d) Vertical stack.

Figure 3.15: Integration of components using a high pass filter function and a capacitor function.

Integration Using a Low Pass Filter Function and a Capacitor Function

A low pass filter function and capacitor function can also be used to realise the passive network of figure 3.14. Firstly the circuit is redrawn as in figure 3.16(a). Then C_1 and L are realised by a low pass filter configuration as in figure 3.16(b). Following C_2 is realised by the capacitor function as in figure 3.16(c). The network is finally arranged into a vertical stack as in figure 3.16(d) by rotating the C_2 module 90° clockwise.

It can be shown that the structure of figure 3.15(d) and 3.16(d) are the same physically. This implies that the integrated configuration can be derived in two ways. This however is only applicable to the passive network of figure 3.14.

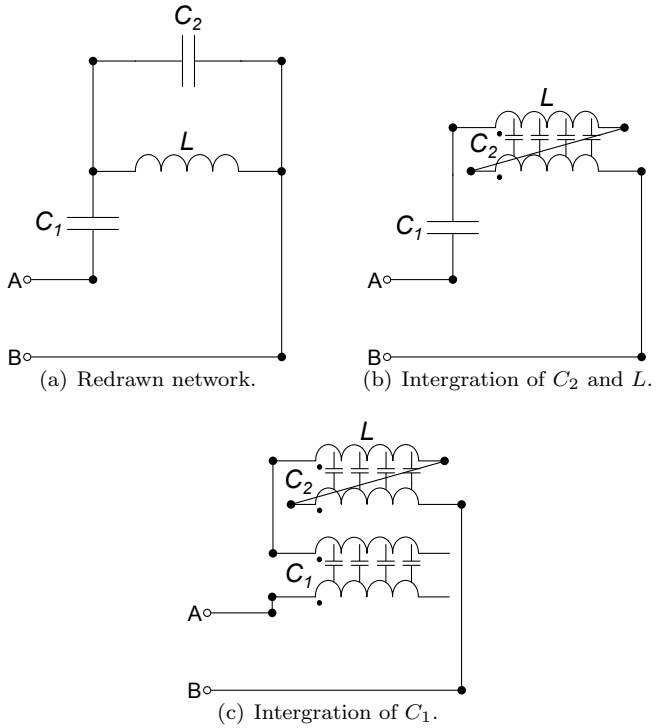


(a) Redrawn network. (b) Intergration of C_1 and L. (c) Intergration of C_2. (d) Vertical stack.

Figure 3.16: Integration of components using a low pass filter function and a capacitor function.

Integration Using a Parallel Resonator Function and a Capacitor Function

Another method of realising the passive network in figure 3.14 involves the use of a parallel resonator function and a capacitor function as seen in figure 3.17. To begin with the original network is redrawn as in figure 3.17(a). C_2 and L are then integrated as in figure 3.17(b) using the parallel resonator function. C_1 is then integrated as in figure 3.17(c), in which the network is already arranged into a vertical stack.



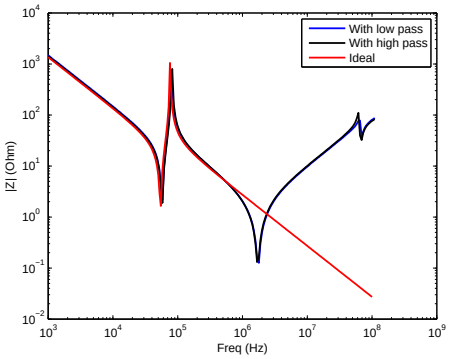
(a) Redrawn network.
(b) Intergration of C_2 and L.
(c) Intergration of C_1.

Figure 3.17: Integration of components using a parallel resonator function and a capacitor function.

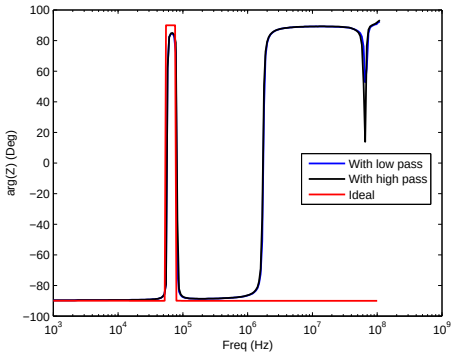
Impedance Analysis

The validity of the structures is established through an impedance analysis. A prototype for each assembly was constructed in which $C_1 = C_2 = 117nF$ and $L = 37\mu H$ for the first two assemblies. For the assembly created using a parallel resonator function $C_1 = 117nF$, $C_2 = 29.25nF$ and $L = 148\mu H$. For all the assemblies small signal measurements of the impedance were recorded and are compared to the ideal impedance of the structures at terminals A and B as in figures 3.18 and 3.19.

Firstly looking at figure 3.18 agreement between the measured and ideal values is observed in the low frequency region. This indicates that the assemblies are identical to the circuit of figure 3.14 for low frequencies. Furthermore there is agreement in the impedance of the two physical structures for the entire frequency range confirming that structures are the same. For the structure that is integrated using a parallel resonator function and a capacitor function agreement between the measured and ideal values is observed for low frequencies as seen in figure 3.19. This again shows that the structure is identical to the ideal conventional circuit for low frequencies. The impedances of all the assemblies have the same shape which demonstrates that it is possible to use various building blocks to realise the passive network. The measured impedances of all the assemblies are dominated by the lead inductance at high frequencies. There are also resonances at very high frequencies which are associated with the distributed nature of the structure.

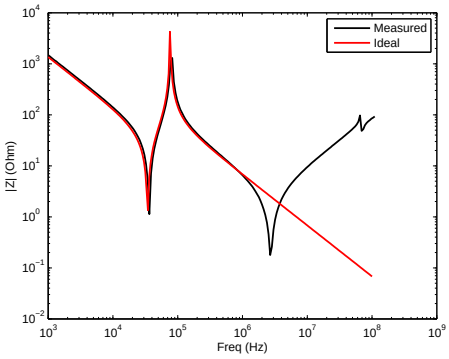


(a) Impedance magnitude.

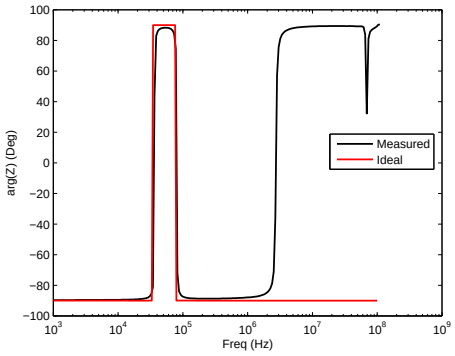


(b) Impedance phase.

Figure 3.18: Impedance of custom network. Integrated structures are realised using a high pass filter function or a low pass filter function as well as a capacitor function. The ideal impedance is that of an ideal conventional (discrete) circuit.



(a) Impedance magnitude.



(b) Impedance phase.

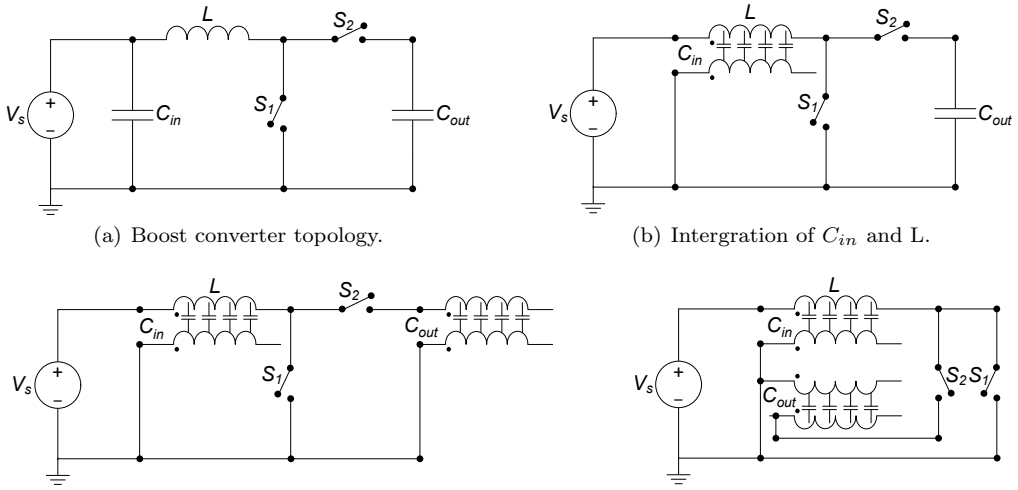
Figure 3.19: Impedance of custom network. Integrated structure is realised using a parallel resonantor function and a capacitor function. The ideal impedance is that of an ideal conventional (discrete) circuit.

3.3.3 Integration of Passives in a Boost Converter

The passive components of the boost converter in figure 3.20(a) can also be integrated using the established circuit functions as building blocks. The first two components considered are C_{in} and L which can be integrated using the low pass filter function as in figure 3.20(b). The output capacitor is then integrated using the capacitor function as in figure 3.20(c). The two modules are then arranged into a vertical stack as in figure 3.20(d) by vertically flipping the output capacitor function and shifting it into place. The vertical stack gives a one dimensional representation of the structure as it appears physically.

A prototype of the integrated boost converter was constructed from which the impedance could be analysed. The components on the prototype are $C_{in} = C_{out} = 117nF$ and $L = 37\mu H$. The impedance of the physical structure was compared to an ideal conventional (discrete) circuit as in figure 3.21. The measured impedance of the boost converter is a small signal measurement taken at the switch terminals when the alternate switch's terminals are shorted. Also the source terminals were open circuited for the measurements. In figure 3.21

agreement is seen between all the measured and ideal values in the low frequency region. This indicates that the integrated structure is identical to the conventional circuit for low frequencies. At higher frequencies the measurement is dominated by the lead inductance. The integration of the passive components in the boost converter is also another contribution of this dissertation.



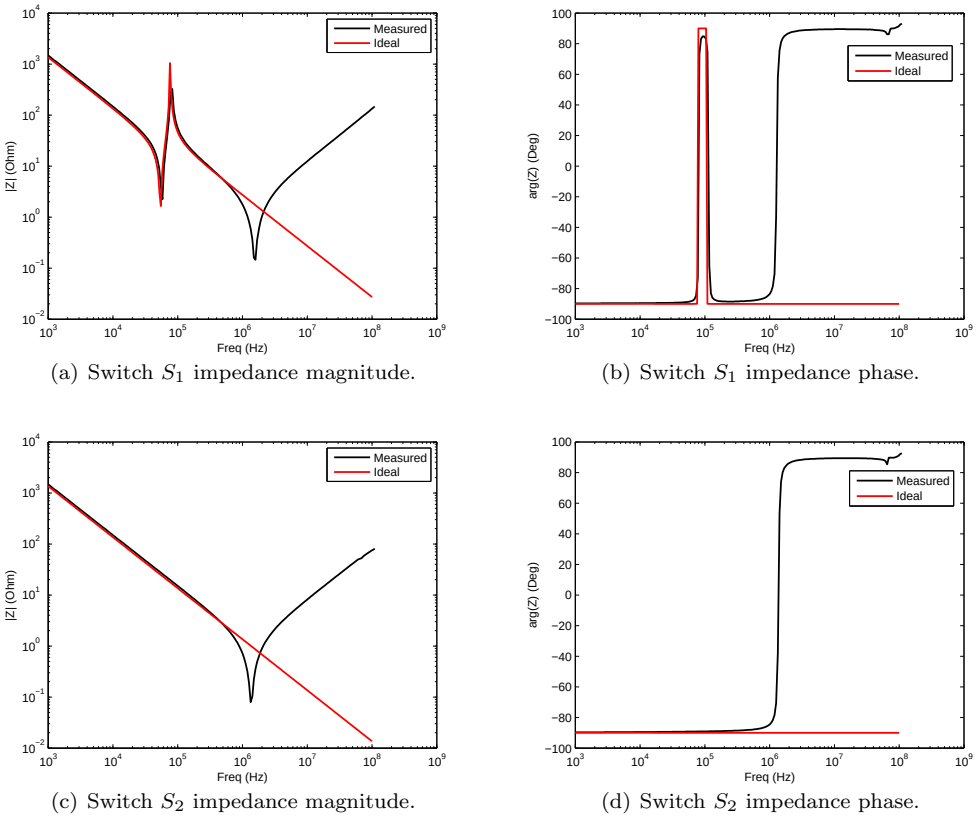
(a) Boost converter topology.

(b) Intergration of C_{in} and L.

(c) Intergration of C_{out}.

(d) Vertical stack.

Figure 3.20: Integration of components on a boost converter.



(a) Switch S_1 impedance magnitude.

(b) Switch S_1 impedance phase.

(c) Switch S_2 impedance magnitude.

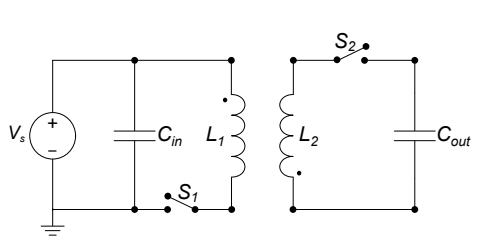
(d) Switch S_2 impedance phase.

Figure 3.21: Impedance at the switches' terminals of the boost converter. The ideal impedance is that of an ideal conventional (discrete) circuit.

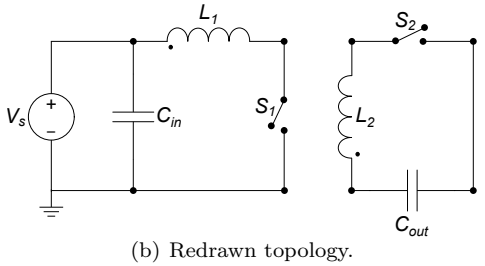
3.3.4 Integration of Passives in a Flyback Converter

The passive components in the flyback converter of figure 3.22(a) can also be integrated using the established circuit functions as building blocks. The converter has previously been integrated [23]. The contribution of this work is on the actual integration steps. Firstly the topology is redrawn as in figure 3.22(b). Then C_{in} and L_1 are integrated using the low pass filter configuration as in figure 3.22(c). C_{out} and L_2 are similarly integrated using the low pass filter function as in figure 3.22(d). The modules are then arranged into a vertical stack by rotating the C_{out} and L_2 module 90° anti-clockwise as in figure 3.22(e).

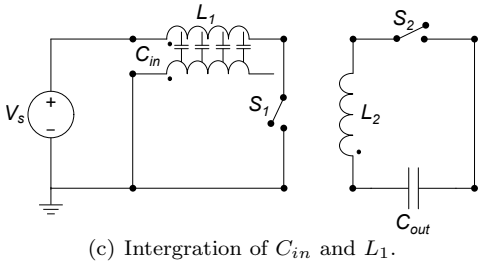
The impedance of a constructed integrated flyback is compared to the impedance of an ideal conventional (discrete) circuit in figure 3.23. The components on the prototype are $C_{in} = C_{out} = 117nF$ and $L_1 = L_2 = 37\mu H$. The measured impedance is a small signal measurement taken at the switch terminals when the alternate switch's terminals are short circuited. The source connection was also open circuited for the measurements. In figure 3.23 agreement between the measured and ideal impedance is observed for low frequencies. This again demonstrates that the integrated structure is identical to the conventional circuit for low frequencies. At higher frequencies the impedance is dominated by the lead inductance.



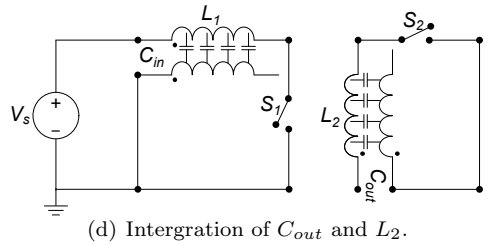
(a) Flyback converter topology.



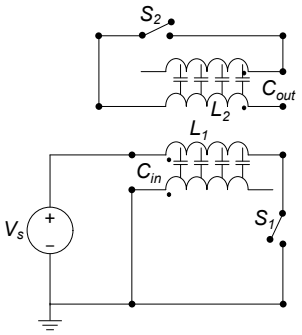
(b) Redrawn topology.



(c) Intergration of C_{in} and L_1.

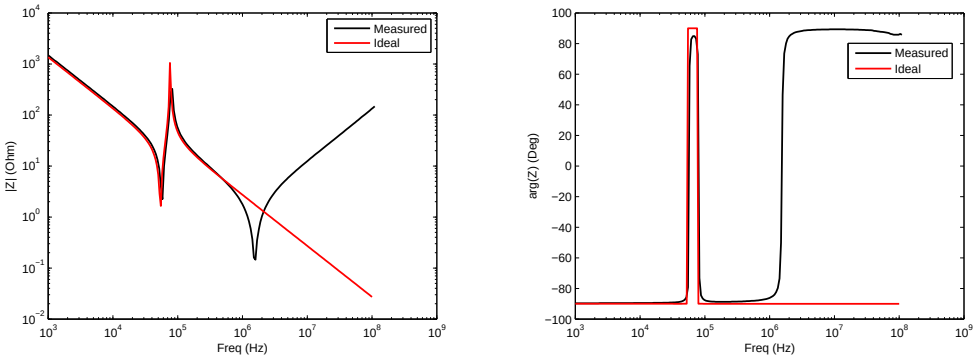


(d) Intergration of C_{out} and L_2.



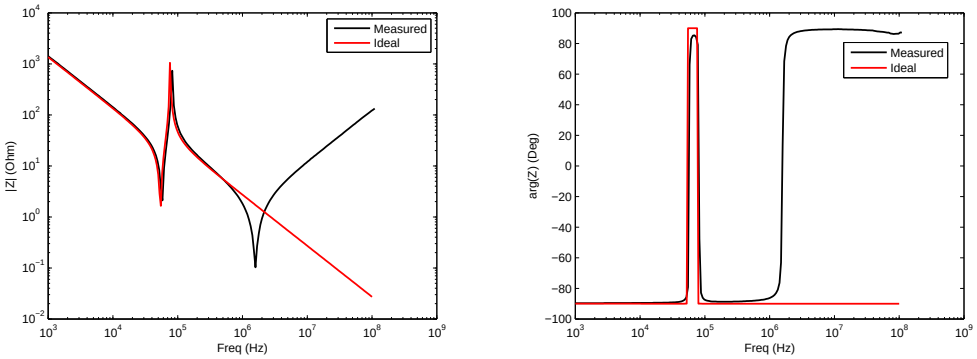
(e) Vertical stack.

Figure 3.22: Integration of components on a flyback converter.



(a) Switch S_1 impedance magnitude.

(b) Switch S_1 impedance phase.



(c) Switch S_2 impedance magnitude.

(d) Switch S_2 impedance phase.

Figure 3.23: Impedance at the switches' terminals of the flyback converter. The ideal impedance is that of an ideal conventional (discrete) circuit.

3.3.5 Discussion

This section has shown how a two conductor integrated passive can be used as a building block to integrate complex passive networks. A two conductor structure could be more suited as a building block than a three conductor structure or higher. This is because elementary circuit functions are easier to obtain and because the aggregate structure would be easier to decompose and analyse.

The successful integration of passive components in the various circuits suggests that passive modules can be combined into a single magnetic core with no adverse effects. Some considerations are however necessary and these are discussed in the next section.

3.4 Considerations for Multiple Modules

When combining multiple modules there exists capacitive coupling, inductive coupling and other features that the designer should be aware of. Some of these aspects need to be mitigated where possible.

3.4.1 Capacitive Coupling

When combining two or more modules, the large surface area between the modules may give rise to capacitive coupling. This coupling may compromise the operation of the circuit at high frequencies. If capacitive coupling exists between two modules, it can be reduced by increasing the seperation distance between the two modules. There is however a tradeoff in increasing this separation distance and keeping the height of winding within that of the winding window.

In some configurations there is no voltage difference along two conductors and this creates a field free region allowing the space to be collapsed and the conductors to be amalgamated. The current in the new conductor is then a sum of the currents in the previous two conductors.

3.4.2 Inductive Coupling

Conductors that are within the same magnetic core share a magnetic flux and are coupled by this flux. The inductive coupling generally does not compromise the performance of the circuit but does create offsets on floating nodes. This will be clearly seen in section 4.3 where the voltage profiles for an integrated structure are shown. Inductor coupling does become a concern when saturation effects are involved and when for example terminals on a conductor are forced to the same potential. If one conductor has both terminals forced to the same potential, a zero voltage gradient would also exist across the other conductors in the system. This would result in a dysfunctional circuit.

3.4.3 Other Considerations

Other things to consider when integrating circuits are differential mode and common mode currents. Common mode currents are currents in the conductors which are in the same direction and contribute to magnetising the core. Currents that are in different directions in the conductors contribute less to magnetising the core because the flux cancels each other. Poorly managed or unaccounted common mode currents can lead to saturation of the magnetic core and hence a dysfunctional circuit. The issue of the common mode currents is usually addressed in the design of the magnetic core. An example of this can be seen with the design of the planar integrated coupled inductor SEPIC.

Chapter 4

Passive Component Integration in a Coupled Inductor SEPIC

The design of a coupled inductor SEPIC using planar integrated passives is presented in this chapter. Two new integrated assemblies are proposed and discussed throughout the chapter. The chapter also details the experimental verification of the integrated assemblies and concludes with a discussion on the advantages that the integrated structures have in LED lighting.

4.1 Design Approach

The design approach adopted in this work for a coupled inductor SEPIC constructed from planar integrated passives consists of three stages namely an assembly design, a circuit level design, and a structural design. These can be described as follows:

- The assembly design is concerned with establishing which building blocks presented in the preceding chapter will be used and in what configuration to realise the various passive components in the circuit. Limits associated with material properties and size are ignored in this design stage and are given attention in the structural design.
- The circuit level design involves specifying the component sizes that will satisfy given operating requirements. This stage is also applicable to the design of a conventional circuit and is therefore not exclusive to the planar integrated structure.
- The structural design builds upon the established assembly and circuit level design to size the structure. This stage also considers the operating requirements as well as the material technology.

4.2 Assembly Design

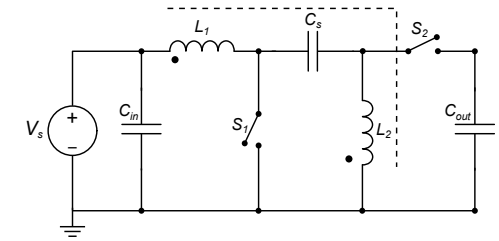
The assembly design entails deriving a planar component configuration that is in effect equivalent to the topology of the original circuit. The building blocks established in the previous chapter are used as the modules to realise the various components in the circuit. For this work each module is a two conductor single turn structure sandwiching a dielectric, that is if the enclosing magnetic structure is ignored. A module can also consist of multiple turns. Two new assemblies are proposed in this section but from an evaluation of the building blocks it is easy to imagine that many other configurations are possible.

4.2.1 Assembly A

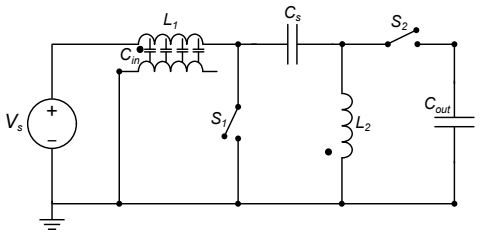
The first assembly is derived using a low pass filter function and a capacitor function of an integrated passive module given in table 3.1 as building blocks. The low pass filter configuration is used as a general LC circuit.

The topology of a classic coupled inductor SEPIC is presented in figure 4.1(a). To begin with, inductor L_1 and capacitor C_{in} are integrated using the low pass filter configuration of an integrated passive module as in figure 4.1(b). Similarly inductor L_2 and capacitor C_s are also integrated using the low pass filter configuration of an integrated passive module as in figure 4.1(c). And lastly the output capacitor is realised using the capacitor function of an integrated passive module as in figure 4.1(d). The diagram only explicitly indicates coupling between inductors L_1 and L_2 however it is worth noting that each conductor enclosed in the magnetic structure has a mutual inductance with every other conductor.

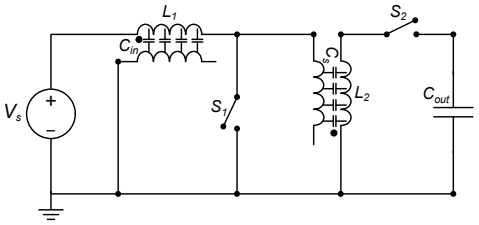
With the components of the circuit as indicated, the only requirement would be to rearrange them into a vertical stack which gives a better impression of the structure as it appears physically. Firstly the module with inductor L_2 and capacitor C_s is flipped vertically and rotated 90° anti-clockwise which results in the arrangement of figure 4.1(e). The module used to realise C_{out} is then rotated 90° clockwise resulting in the arrangement of figure 4.1(f). As an additional refinement, the two empty regions $cdef$ and $ghij$ between the modules can be collapsed and the conductors in the collapsed regions amalgamated. The refinement arises from an analysis of the voltage distribution which indicates that there is no voltage difference between the two conductors of each region along the structure. The current in the amalgamated conductor becomes a vector sum of the individual currents in the two plates. If the region could not be collapsed it would require an insulation layer, and the thickness would be a compromise between keeping the height of the winding window low and keeping the capacitance of the region low. In this work however three of the two layered modules are used due to material availability resulting in the structure of figure 4.2.



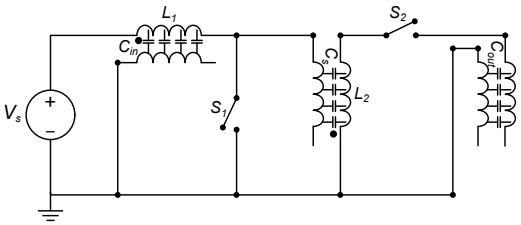
(a) Coupled inductor SEPIC topology.



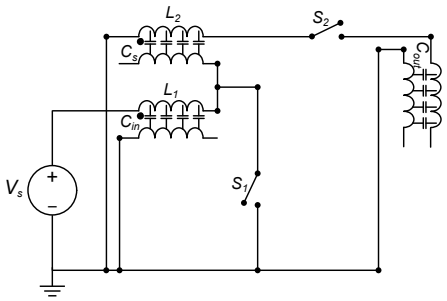
(b) Integration of L_1 and C_{in}.



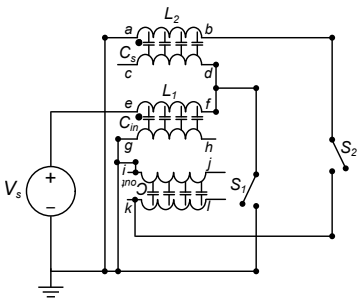
(c) Integration of L_2 and C_s.



(d) Integration of output capacitor.

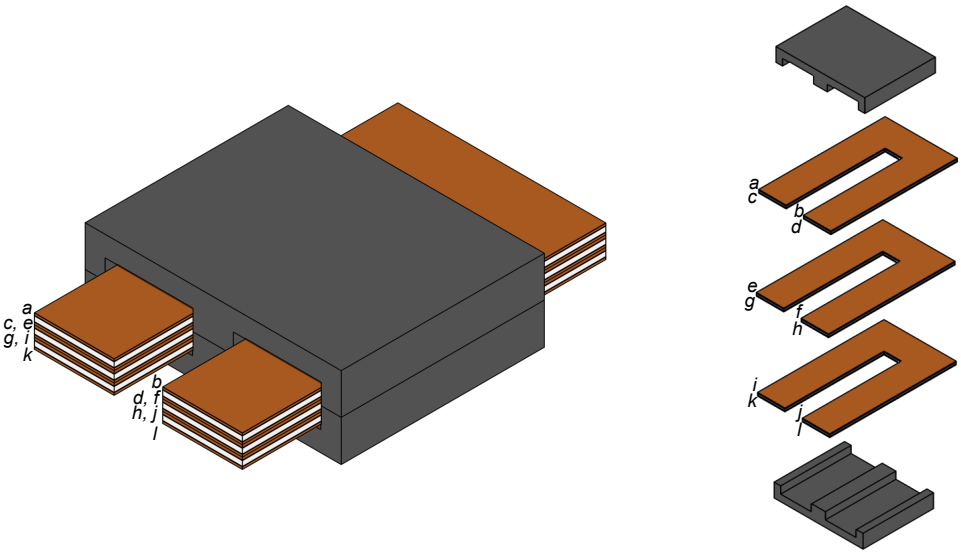


(e) Rearrangement of LC modules.



(f) Rearrangement of LC modules.

Figure 4.1: Integration of passive components.



(a) General structure.

(b) Exploded view.

Figure 4.2: Three dimensional impression of physical structure.

4.2.2 Assembly B

The second assembly of the planar integrated coupled inductor SEPIC is rather interesting in that a significant part of the converter's electromagnetic function can be realised with one LC module. To illustrate the idea, the classic coupled inductor SEPIC in figure 4.1(a) is redrawn as in figure 4.3(a). Inductor L_1 is then rotated 90° clockwise and inductor L_2 is flipped vertically resulting in the representation of figure 4.3(b). Capacitor C_{in} is then rotated 90° anti-clockwise and shifted into place as in figure 4.3(c). Upon inspection it is noted that the configuration of L_1, L_2, C_{in} and C_s in figure 4.3(c) is similar to the split-c model of an integrated LC structure. There is no established constraint on the ratio of C_{in} and C_s, only that they should each be greater or equal to the required (design) size. Hence one integrated LC module can be used to realise the function of four passive components in a coupled inductor SEPIC. The output capacitor function is also realised using an integrated passive structure as in figure 4.3(d).

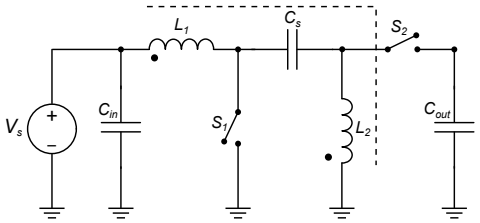
The complete structure is then arranged into a vertical stack by first flipping the L_1, L_2, C_{in} and C_s module vertically and rotating it by 90° clockwise. The output capacitor is also rotated 90° in a clockwise direction resulting in the structure of figure 4.3(e). As an additional refinement, the empty region $cdef$ between the two modules can be collapsed and the two conductors amalgamated into one. The refinement arises from an analysis of the voltage distribution which indicates that there is no voltage difference between the two conductors in the region along the structure. The current in the amalgamated conductor becomes a vector sum of the individual currents in the two plates. In this work however two of the two layered modules are used due to material availability resulting in the structure of figure 4.4.

4.2.3 Discussion

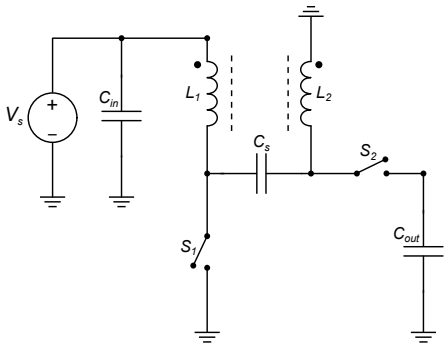
In chapter 2 it was established that the inductances should be equal and that the coupling coefficient should be unity. The derived assemblies are based on these specifications. If the inductor sizes were different or the desired coupling coefficient was not unity, assembly B would no longer be viable. If the desired coupling coefficient was not unity a leakage layer would have to be introduced between the inductors in assembly A.

Other differences between the two assemblies also exist. Assembly A has the advantage in that each component can be precisely designed whereas for assembly B the capacitors C_{in} and C_s have to be equal. Assembly B uses less material than assembly A which may be a more cost effective solution in some applications. The differences between the two assemblies suggest that each assembly may be suited for different applications.

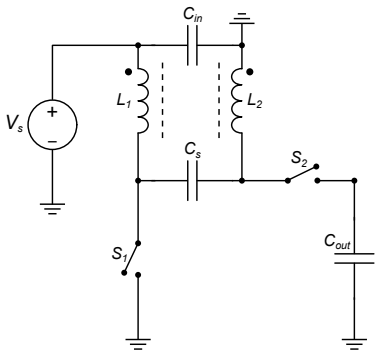
Given a particular assembly it is useful to also consider how it'll operate generally. The spatial voltage and current distributions for each assembly are therefore considered next.



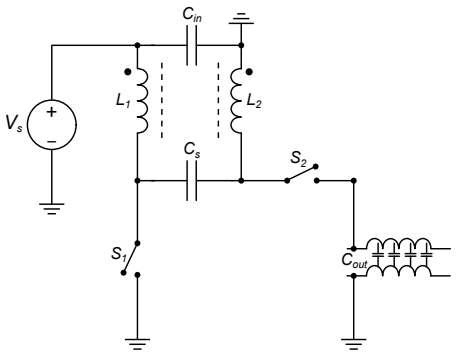
(a) Redrawn coupled inductor SEPIC.



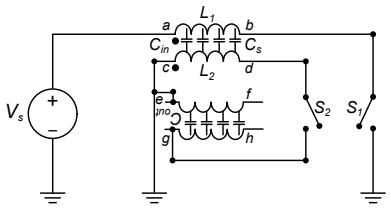
(b) Inductors L_1 and L_2 redrawn.



(c) Adjustment of capacitor C_{in}.

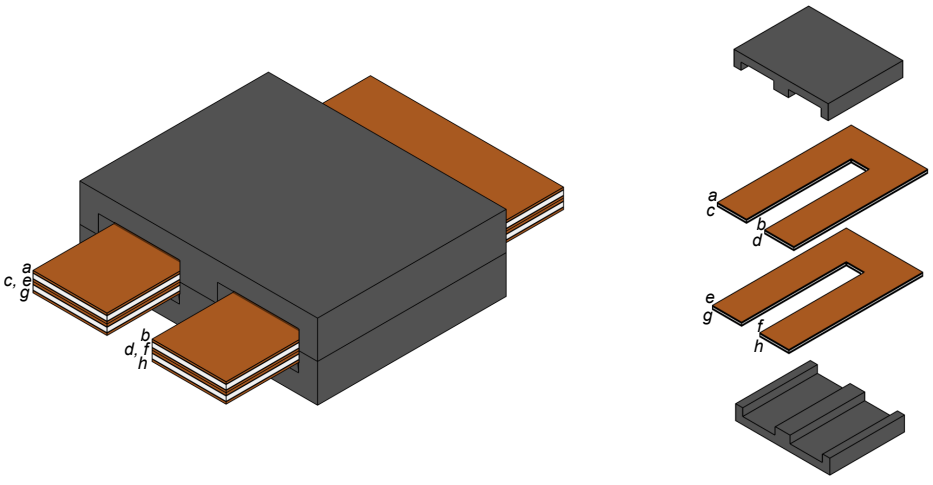


(d) Integration of output capacitor.



(e) Rearrangement of LC modules.

Figure 4.3: Integration of passive components.



(a) General structure.

(b) Exploded view.

Figure 4.4: Three dimensional impression of physical structure.

4.3 Spatial Voltage and Current Distributions

This section will describe the spatial voltage and current distributions of the planar integrated coupled inductor SEPIC during steady state operation in continuous conduction mode. The distributions are however for a particular moment in time.

Assembly A

Assuming linear distributions the spatial voltage and current distributions for assembly A are as in figure 4.6. The voltage and current definitions on the conventional circuit are shown in figure 4.5 and can be used as a reference. Linear distributions are valid for a structural size that is significantly less than a wavelength of the operating frequency, and also for non-resonant operation. These two aspects are both applicable in this work.

The voltages across the conductors are governed by Faraday's law of induction. Given the common magnetic flux and each conductor being a single turn, all the conductors have the same voltage gradient across them even though the node voltages may vary as indicated in figures 4.6(a) and 4.6(b).

The current distributions are easier to describe if the structure is first decomposed into its two layer modules as in figures 4.6(c) and 4.6(d). The current distributions in the amalgamated conductors of figures 4.6(e) and 4.6(f) are then a vector sum of the currents in the formerly separate conductors. The on interval in figure 4.6(c) is described as follows:

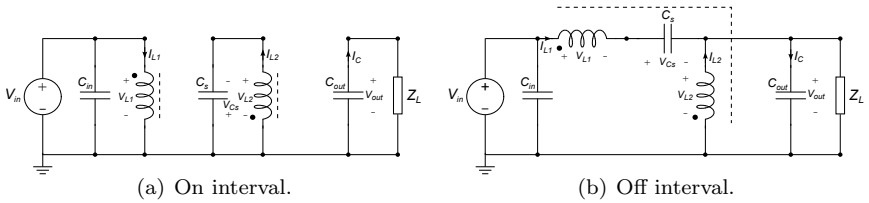
- For the module making up inductor L_1 and capacitor C_{in} a terminal is connected to ground forcing V_{in} across inductor L_1. Some current is drawn by C_{in} and decreases along L_1.
- On the module making up inductor L_2 and capacitor C_s a terminal is also connected to ground. The dielectric forming capacitor C_s then discharges through the ground path contributing to the current through inductor L_2 via the ground path. The mechanism entails a small amount of charge being discharged for each infinitesimal segment along the dielectric, adding to the total current on the conductor towards the ground connection.
- The output capacitor C_{out} has a current drawn to supply the load in small amounts along the structure accumulating towards the load terminals. The current on the plate of C_{out} connected to ground is a return current.

The off interval in figure 4.6(d) is described as follows:

- For the module making up inductor L_1 and capacitor C_{in} the second ground connection is disconnected. The rest of the circuit draws more current during this interval and

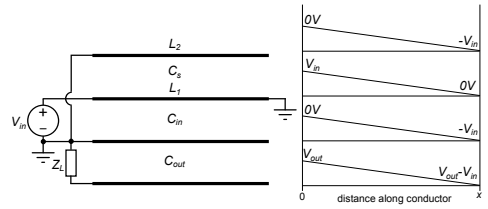
C_{in} discharges increasing the current along L_1. The current from inductor L_1 charges the dielectric making up C_s.

- On the module making up inductor L_2 and capacitor C_s the second ground connection is also disconnected. Another terminal on the module is connected to a terminal on the output module. Charge accumulates along L_2 and ultimately forms the current that goes to the load and output capacitor.

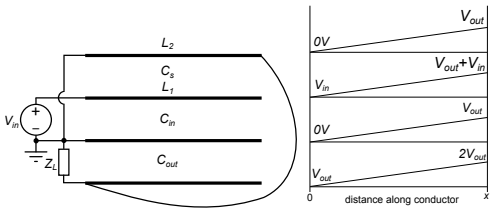


(a) On interval. (b) Off interval.

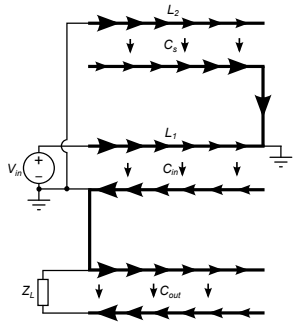
Figure 4.5: Voltage and current definitions on the conventional circuit.



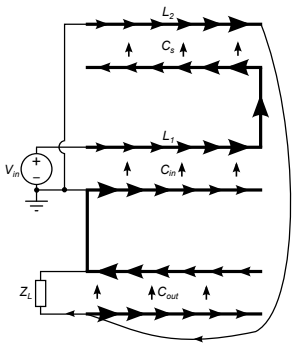
(a) Voltage during on interval.



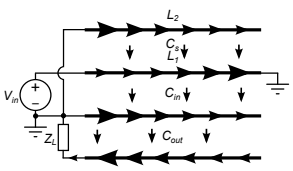
(b) Voltage during off interval.



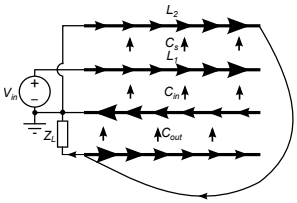
(c) Current during on interval.



(d) Current during off interval.



(e) Current during on interval.



(f) Current during off interval.

Figure 4.6: Spatial voltage and current distributions during the on and off states.

Assembly B

Assuming a linear distribution the spatial voltage and current distributions for assembly B are as in figure 4.8. The voltage and current definitions on the conventional circuit are shown again for convenience in figure 4.7 and can be used as a reference.

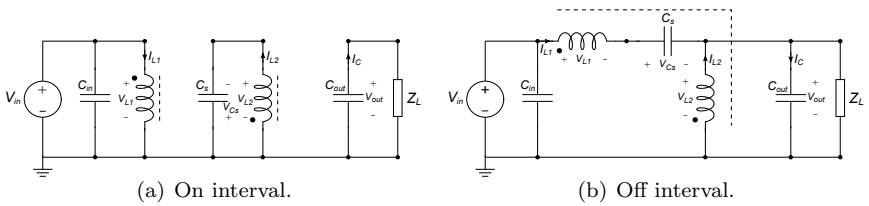
The voltages across the conductors are governed by Faraday's law of induction. Just as in assembly A the common magnetic flux and each conductor being a single turn results in all the conductors having the same voltage gradient across them even though the node voltages may vary as indicated in figures 4.8(a) and 4.8(b).

The current distributions are easier to describe if the structure is first decomposed into its two layer modules as in figures 4.8(c) and 4.8(d). The current distributions in the amalgamated conductors of figures 4.8(e) and 4.8(f) are then a vector sum of the currents in the formerly separate conductors. The on interval in figure 4.8(c) is described as follows:

- For the module making up L_1, L_2, C_{in} and C_s a terminal is connected to ground. Closer to C_s the dielectric discharges along the conductor towards ground, increasing the current along the conductor. The current through the ground path contributes to the current in inductor L_2.
- On the module making the output capacitor C_{out} a current is drawn to supply the load in small amounts along the structure accumulating towards the load terminals.

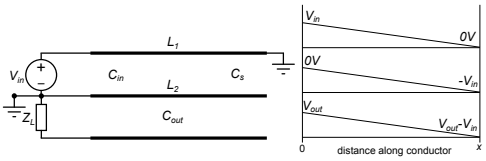
The off interval in figure 4.8(d) is described as follows:

- For the module making up L_1, L_2, C_{in} and C_s the second ground connection is disconnected. A connection is made from the terminal of L_2 and C_s to the output terminal. Capacitor C_s is charged through inductor L_1 where current reduces along the plate till the edge. Meanwhile current accumulates along inductor L_2 and forms the current that goes to the load and output capacitor.
- The module making up the output capacitor is charged during this interval and current to the load is supplied by the rest of the circuit.

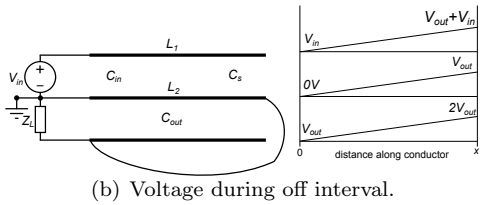


(a) On interval. (b) Off interval.

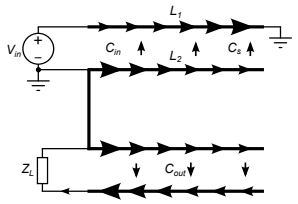
Figure 4.7: Voltage and current definitions on the conventional circuit.



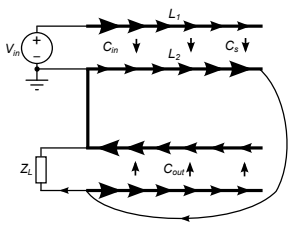
(a) Voltage during on interval.



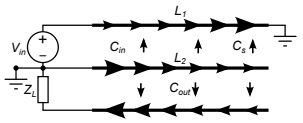
(b) Voltage during off interval.



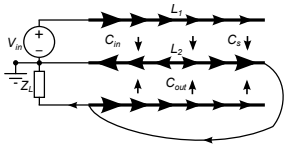
(c) Current during on interval.



(d) Current during off interval.



(e) Current during on interval.



(f) Current during off interval.

Figure 4.8: Spatial voltage and current distributions during the on and off states.

Significant similarities between the spatial voltage and current distributions of the two assemblies exist. Firstly it should be noted that the node voltages and the voltage gradient of a particular plate common in both assemblies is the same. Additionally the current distribution on a plate common in both assemblies is the same except for the plate that makes up L_1. The subtle difference in the current distribution on this plate is due to capacitors C_{in} and C_s being formed by a single dielectric in the one assembly and being formed by two dielectrics in the other assembly. Nonetheless given the similarities the two assemblies are expected to operate identically.

This section has been concerned with describing the operation of the planar integrated structures. In order to develop a planar integrated coupled inductor SEPIC, a circuit level design must also be considered.

4.4 Circuit Level Design

The circuit level design involves specifying the passive component values and is technology independent. The design is also applicable to a conventional circuit and is therefore not exclusive to the planar integrated circuit. Also this stage may happen before the assembly design. The design process has been presented in [5] and is reviewed in appendix B. A summary of the input and output parameters from the design process are given in this section. The input design parameters are:

- Input voltage range $V_{in(min)}$ and $V_{in(max)}$.
- Output voltage range $V_{out(min)}$ and $V_{out(max)}$.
- Switching frequency f_s.
- Operating power level, from which the current range is also determined.
- Inductor coupling coefficient.

The input parameters are then used in a set of design equations to obtain the circuit specifications or the output parameters which are:

- Input capacitance C_{in}.
- Series coupling capacitance C_s.
- Output capacitance C_{out}.
- Inductance L_1 and L_2.
- Applicable switching devices (MOSFET and diode).

The power characteristics would typically be informed by the LED lighting application. However in this dissertation the power characteristics are a soft constraint due to the available construction material.

In cases where the component sizes are a hard constraint, the design approach becomes iterative in nature and it may become necessary to adjust some or all of the input parameters to achieve a functional design.

After the component sizes have been specified an additional design step is required to specify the requirements and technology of the physical components. Physical materials have varying loss dynamics which must be minimised. They also have frequency limitations and limitations associated with the operating voltages and currents. This additional design step is regarded as the structural design and in this work focus is only given to the planar integrated circuits. The structural design for a conventional circuit largely involves specifying the material technology and energy ratings for the passive components.

4.5 Structural Design

The structural design for a planar integrated circuit makes use of an established assembly and the parameters from the circuit level design to size the structure. In sizing the structure, the operating requirements and material technology are also considered. In this section attention is given to the structural design of the two derived assemblies. The main steps in the structural design are the design of the inductors and the design of the capacitors.

4.5.1 Inductor Design

The design of the inductors is the first aspect that is considered in the structural design of a planar integrated coupled inductor SEPIC. To begin with the core size and technology to satisfy the inductances L_1 and L_2 is specified. The approach to determining the core size and technology for assembly A and B is the same.

In assembly A the average current in both plates of the low pass filter function is equivalent to the average current that would pass through the one inductor in a discrete sense. The current on the plates of the purely capacitive function is in a differential mode and thus does not contribute to the magnetising current. Also the displacement current in the capacitive components of the structure does not contribute to the magnetising current. The magnetising current of the structure is then simply due to the two inductors as they are positioned in such a way that their flux is additive.

Similarly, assembly B has the two inductances which magnetise the core and the output capacitance module which does not contribute to the magnetisation of the core. The use of the two inductors in selecting the core size and technology is therefore suitable.

The configuration of the magnetic core may either be an E-E combination or an E-PLT combination. The selection of the magnetic material is informed by the operating requirements and frequency. The specification of the core size is based on the required inductance which is expressed as in equation 4.1 where l_{path} is the length of the magnetic path, A_{core} is the area of the centre leg of the magnetic core, N is the number of turns, μ_0 is the permeability of free space, and μ_r is the relative permeability of the material. The structural parameters are as indicated in figure 4.9.

$$\frac{l_{path}}{A_{core}} = \frac{N^2 \mu_0 \mu_r}{L} \tag{4.1}$$

The number of turns N for the work in this dissertation are set to one. This is so that the parasitic elements associated with a multi-turn structure can be ignored.

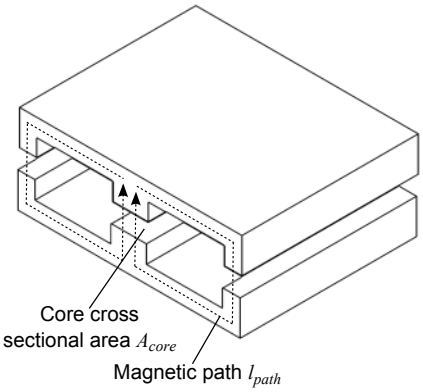


Figure 4.9: Magnetic core with parameter definitions.

As indicated by equation 4.1 the use of an air gap has been avoided with the aim of achieving a higher inductance with a single turn. The omission of an air gap is relevant to the work in this dissertation for the reason given. Generally an air gap can be included if required. The design of an inductor with an air gap would include an additional term in equation 4.1. The feasibility of the design as it stands is verified through energy considerations. The electrical energy defined by equation 4.2 is supposed to be less than the magnetic energy defined by equation 4.3 for the design to be realisable without an air gap. The current specified in equation 4.2 is a sum of the two inductor currents.

$$\hat{W_e} = \frac{1}{2} L I_{peak}^2 \tag{4.2}$$

$$\hat{W_m} = \frac{1}{2} \hat{B} \hat{H} A_{core} l_{path} \tag{4.3}$$

After verifying the feasibility of the energy storage, the conductor width can be considered. To obtain the required conductor width the conductor thickness is first determined. The usefulness of the conductor is limited by the skin effect and as such the conductor thickness is set to a skin depth at the operating frequency given by equation 4.4. In equation 4.4 ρ is the resistivity of the material and f is the operating frequency. The width of the conductor is then determined by equation 4.5 where I is the operating current and J_{cu} is the desired current density.

$$\delta_{cu} = \sqrt{\frac{\rho}{\pi f \mu_0}} \tag{4.4}$$

$$w_c = \frac{I}{J_{cu} \delta_{cu}} \tag{4.5}$$

The conductor thickness and width can be larger than what is defined by the equations, however the equations are useful in determining optimum sizes. In general the width of the

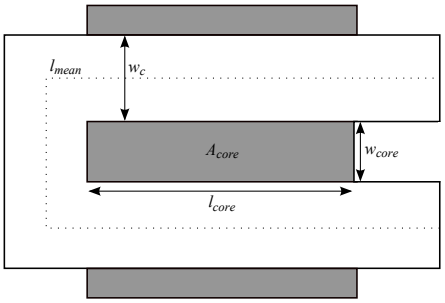


Figure 4.10: Top view of planar integrated coupled inductor SEPIC, with top magnetic core removed.

winding window has to be larger than the conductor width or the width of a group of turns in a multi turn structure. If for a single turn the winding window width is much larger than the computed conductor width, the conductor width may be set to almost that of winding window width in order to achieve a higher capacitor area. This is the approach adopted for the derived assemblies.

In general the winding window height also has to be greater than the height of the material stack which can only be determined after determining the required dielectric thicknesses.

4.5.2 Capacitor Design

The capacitor design is the second aspect that is considered in the structural design of a planar integrated coupled inductor SEPIC. In order to design for the capacitances, the area created by the inductor winding is considered and can be visualised as in figure 4.10.

To obtain the area, the mean length of the layer is first determined as in equation 4.6.

$$\begin{aligned} l_{mean} &= 2(l_{core} + w_c) + w_{core} + w_c + w_c \\ &= 2l_{core} + 4w_c + w_{core} \end{aligned} \tag{4.6}$$

The capacitor area is then determined as in equation 4.7.

$$A_{cap} = w_c l_{mean} \tag{4.7}$$

Given the capacitor area, the capacitances C_{in}, C_s and C_{out} can then also be designed using equation 4.8 where C_x represents each individual capacitance, ϵ_x is the relative permittivity of the dielectric, ϵ_0 is the permittivity of free space and d_x is the dielectric thickness.

$$\frac{\epsilon_x}{d_x} = \frac{C_x}{A_{cap}\epsilon_0} \tag{4.8}$$

The capacitor design is achieved by selection of the appropriate dielectric constant and dielectric thickness given that the other parameters are fixed. The dielectric material is

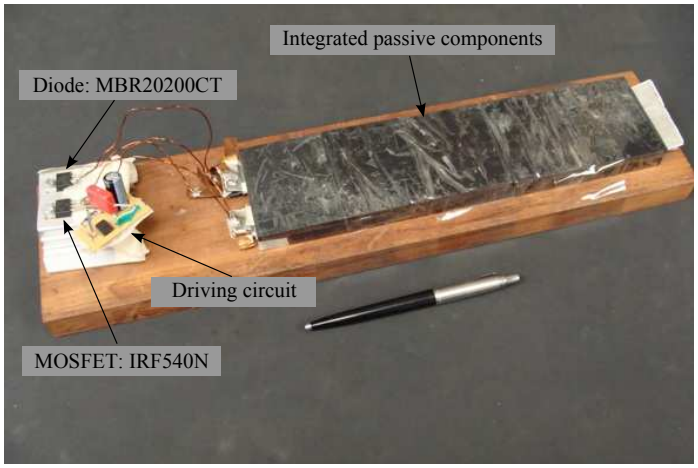
selected to have a bandwidth beyond that of the switching frequency and the dielectric thickness is selected to be thicker than required for the electric breakdown strength.

For assembly B the capacitors C_{in} and C_s share a dielectric and are of equal magnitude. This implies that the capacitance in equation 4.8 considers the total capacitance of the two.

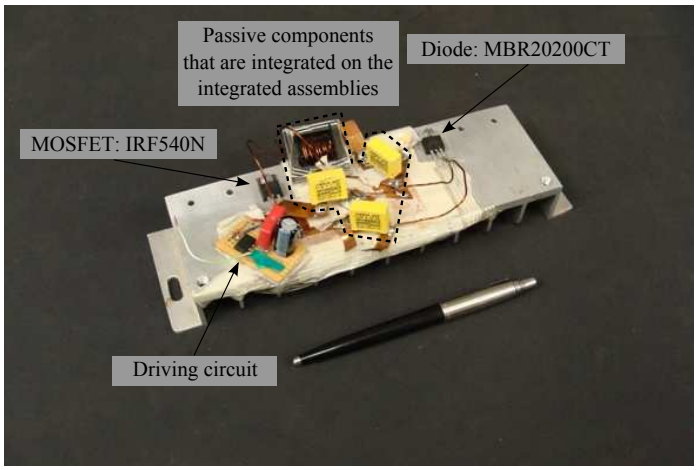
In general the entire structural design process may be iterative depending on what materials are available or what can be practically built.

4.6 Experimental Verification

In order to verify the validity of the proposed planar circuits, a 5W prototype for each assembly was constructed. Only 5W prototypes could be achieved due to the available material. Two conventional circuits similar to each prototype were also constructed in order to compare the operation. The constructed prototype for assembly A is shown in figure 4.11(a) and its associated conventional circuit is shown in figure 4.11(b).



(a) Assembly A prototype.



(b) Conventional circuit.

Figure 4.11: Photographs of experimental prototypes.

The integrated circuit is constructed from an E-PLT ferrite combination which consists of five E64 cores and five PLT64 cores. Added to the cores it is also constructed from three 3M C-ply units which make up the inductor and capacitor modules. A unit of the 3M C-ply material consists of two conductors which sandwich a dielectric material. The prototype for assembly B is similar to assembly A with the only difference being that is has two 3M C-ply units instead of three. The conventional circuit associated with assembly B is similar to the conventional circuit associated with assembly A with the only difference being the different valued capacitors C_{in} and C_s. The specifications for the constructed prototypes are as in table 4.1 and table 4.2. For assembly B the capacitors C_s and C_{in} were each $58.5nF$ and for the associated conventional circuit $55nF$ each. The size of the integrated prototype is $43.8 \times 7.6 \times 2.9$ $(L \times W \times H)$ cm^3. The height is dominated by the heat sink which can be reduced. The significant height is that of the magnetic structure which is 1.7cm.

The experimental work entails an impedance analysis of the integrated circuits, an assessment of the voltage conversion operation as well as the efficiency of the circuits. Since the work was mainly focused on construction aspects of the converter, a purely resistive load was employed in testing the operation of the circuit.

Table 4.1: Components and parameter values on the integrated prototype

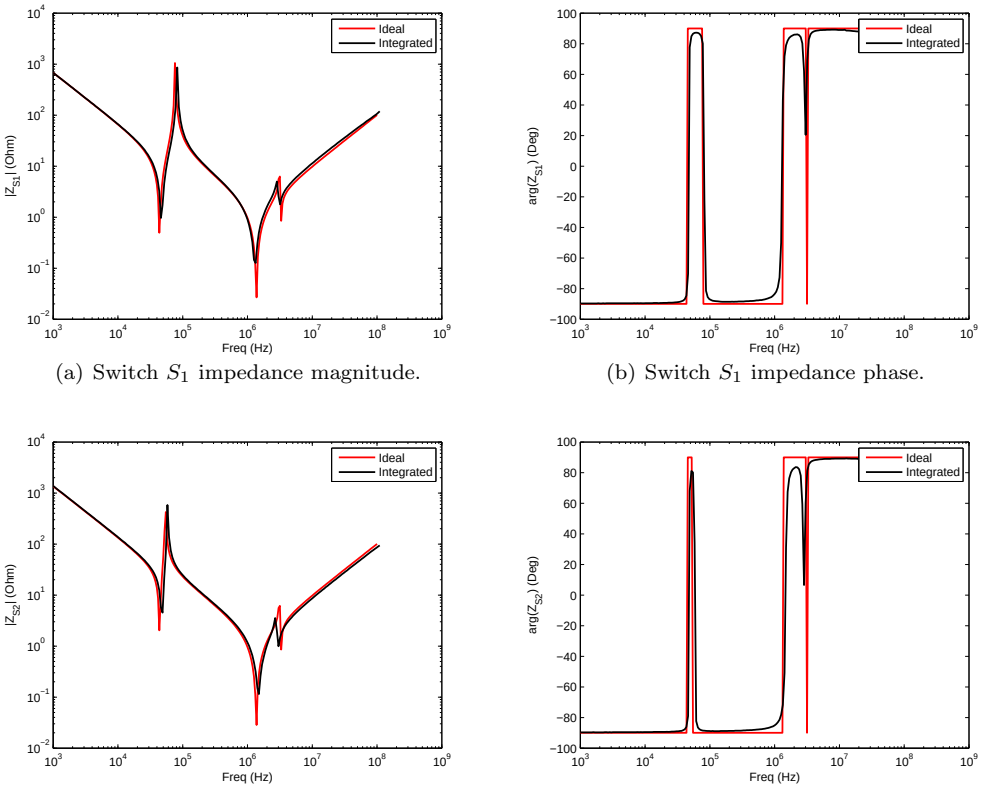
Component	Value	Description
L_1, L_2	$37\mu H$	35 micron conductor (3M C-ply)
C_s, C_{in}, C_{out}	$117nF$	100V ceramic (3M C-ply)
S_1	IRF540N	100V/33A MOSFET
S_2	MBR20200CT	200V/10A Schottky diode

Table 4.2: Components and parameter values on the conventional prototype

Component	Value	Description
L_1, L_2	$37\mu H$	0.8mm conductor
C_s, C_{in}, C_{out}	$120nF$	275V polypropylene capacitor
S_1	IRF540N	100V/33A MOSFET
S_2	MBR20200CT	200V/10A Schottky diode

4.6.1 Impedance Analysis

Assembly A



(a) Switch S_1 impedance magnitude.

(b) Switch S_1 impedance phase.

(c) Switch S_2 impedance magnitude.

(d) Switch S_2 impedance phase.

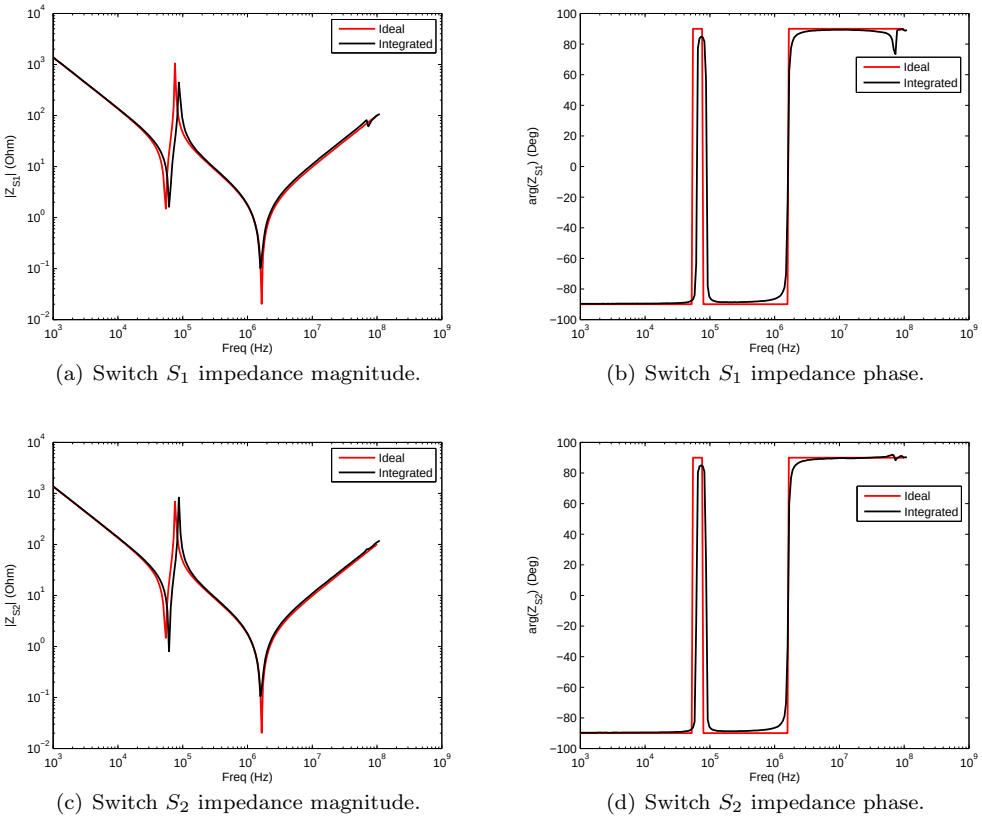
Figure 4.12: Impedance at the switches' terminals of the coupled inductor SEPIC. The impedance of the integrated circuit is a small signal measurement. The ideal impedance is that of an ideal conventional (discrete) circuit.

The measured impedance of assembly A along with the ideal impedance is depicted in figure 4.12. The impedance is analysed at terminals that enable the effect of all components to be observed. For this work the impedance at the switches' terminals is analysed for when the alternate switch's terminals are short circuited. This emulates the configuration of the circuit during a switching interval. Figures 4.12(a) and 4.12(b) are the impedance magnitude and phase as seen at the terminals of switch S_1 which are labelled as terminals *df* and *gi* on figure 4.1(f), however with the source open circuited so the effect of C_{in} can be observed. Figures 4.12(c) and 4.12(d) are the impedance magnitude and phase as seen at the terminals of switch S_2 which are labelled as terminals *b* and *k* on figure 4.1(f), again with the source open circuited.

From the various plots it is noted that the discrete circuit is able to predict the same number of resonant points observed on the small signal measurement of the integrated structure. This does suggest that structurally the integrated circuit is identical to the discrete circuit.

Two resonant points in the 2.5-4MHz region are observed and are due to leakage inductance effects. Less than unity coupling was present on the structure that was measured as the structure had a large space between region $cdef$ in figure 4.1(f) due to an insulation layer. As seen in figure 4.1(f) this space also happens to be between inductor L_1 and L_2. The insulation layer was present before the structure was refined and region $cdef$ collapsed. The coupling coefficient between inductor L_1 and L_2 on the ideal discrete circuit is set to $k = 0.9994$. The effect of the lead inductance has also been included and modelled as a series inductor.

Assembly B



(a) Switch S_1 impedance magnitude.

(b) Switch S_1 impedance phase.

(c) Switch S_2 impedance magnitude.

(d) Switch S_2 impedance phase.

Figure 4.13: Impedance at the switches' terminals of the coupled inductor SEPIC. The impedance of the integrated circuit is a small signal measurement. The ideal impedance is that of an ideal conventional (discrete) circuit.

The measured impedance of assembly B along with the ideal impedance is depicted in figure 4.13. The analysis is at the switches' terminals for when each alternate switch's terminals are shorted. Figures 4.13(a) and 4.13(b) are the impedance magnitude and phase as seen at the terminals of switch S_1 which are labelled as terminals b and ce on figure 4.3(e), however with the source open circuited. Figures 4.13(c) and 4.13(d) are the impedance magnitude and phase as seen at the terminals of switch S_2 which are labelled as terminals d and g on

figure 4.3(e), again with the source open circuited.

From the plots it is observed that the discrete circuit is able to predict the artifacts on the measurement of the integrated circuit up to about 69.1MHz. That is with the effect of the lead inductance included. The measurements suggest that the integrated structure appears identical to the discrete circuit for low frequencies and medium frequencies. The two resonant points observed in assembly A in the 2.5-4MHz region are not present in this assembly. This is possibly due to the fact that the leakage inductance effects are less pronounced in assembly B as the space between inductors L_1 and L_2 is less. The coupling coefficient between inductor L_1 and L_2 on the ideal discrete circuit is set to unity. On the impedance measurement of the integrated circuit, resonance is observed in the 69.1MHz region. It cannot be predicted by the discrete circuit and would therefore require a more elaborate model of the structure.

4.6.2 Voltage Conversion Operation

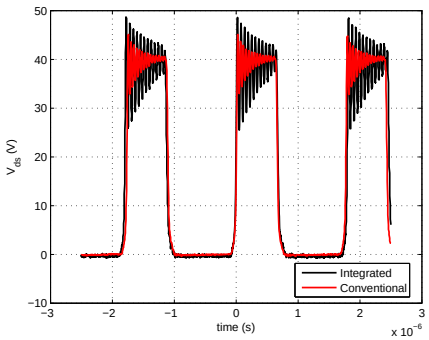
The prototypes were also assessed for voltage step up operation and voltage step down operation with the waveforms as in figure 4.14 to figure 4.17. For step up operation, the input voltage was approximately 15V DC and the expected output voltage was an average of 23V for a duty cycle of 61%. Measurements were recorded for a 5W load. For step down operation, the input voltage was approximately 20V DC and the expected output voltage was an average of 14V for a duty cycle of 42%. Measurements were also recorded for a 5W load. For both step up and step down operation the switching frequency was set to 560kHz. The given input voltages make the circuits suited for battery related applications. The inductor current of the integrated prototypes was difficult to measure due to the integrated nature of each module, nonetheless the terminal voltage was measured.

The measured waveforms of the integrated circuits and conventional circuits as seen in figure 4.14 to figure 4.17 generally follow each other closely. Some cases exist where the swing or voltage shape is slightly different. Different ringing characteristics are also observed. The variation in voltage that is observed in the swing or shape is due to slight differences in the circuit component values. These differences are seen on all the series capacitor voltages and on the inductor voltages of assembly B.

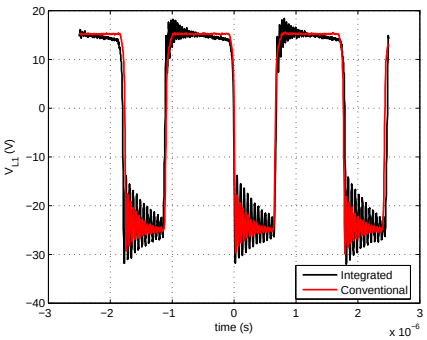
Two distinguishable characteristics associated with the ringing are observed on the waveforms. Firstly the ringing frequency of the integrated circuits is lower than that of the conventional circuits. During a switching event the junction capacitance of the diode or the drain source capacitor of the MOSFET resonate with the surrounding circuit components including the parasitic elements. Present on the integrated circuit is a higher parasitic inductance on the leads of the semiconductor devices which can be seen on figure 4.11(a). The higher inductance contributes to a lower ringing frequency. Secondly besides the differ-

ent ringing frequency, the integrated circuits have less damping associated with the ringing than the conventional circuits. The difference in the damping is due to the conventional circuits being more lossy than the integrated circuits. Two mechanisms by which the loss is increased in the conventional circuits are through the proximity effect and the skin effect. The conventional circuits are built from round conductors which perform poorly at high frequencies due to the skin effect. Also the several wound layers of the round wire lead to a pronounced proximity effect. The integrated circuit is built using flat, thin conductors which are more suited for high frequency operation.

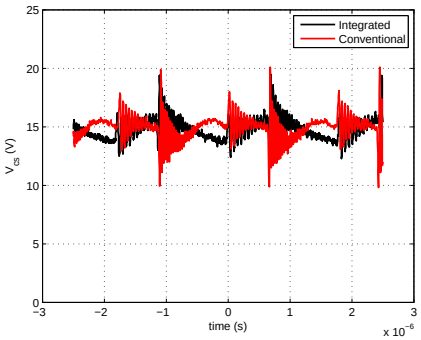
In general the measurements of the integrated prototypes are in agreement with the conventional circuits. The slight variations in the measurements are due to differences in the construction and slight differences in the circuit component values. An inspection of the series capacitor voltages together with the output capacitor voltages indicates that the voltage conversion operation is as expected. This all further demonstrates the validity of integrating the passive components in a coupled inductor SEPIC.



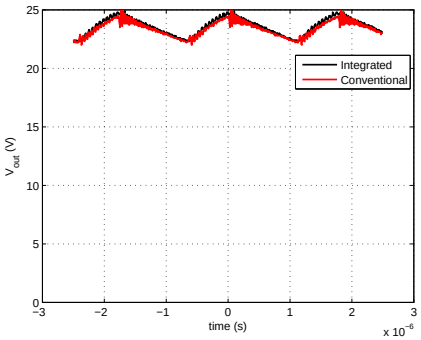
(a) Drain source voltage.



(b) Inductor L1 voltage.

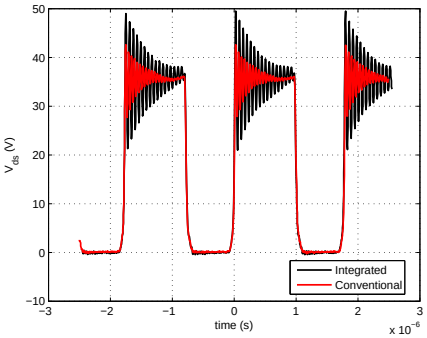


(c) Capacitor Cs voltage.

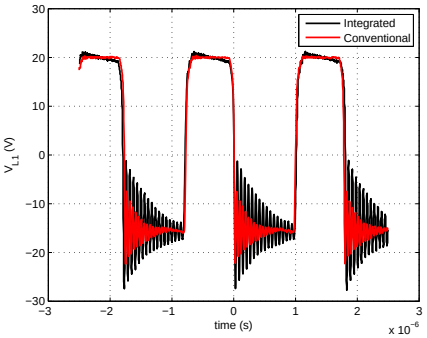


(d) Output voltage.

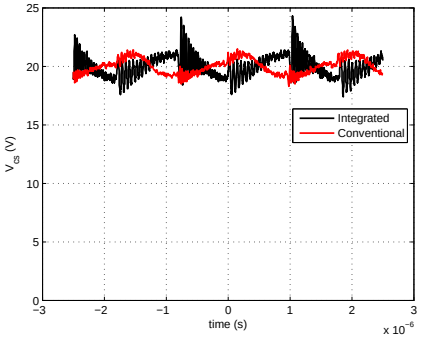
Figure 4.14: Voltages during step up operation in assembly A.



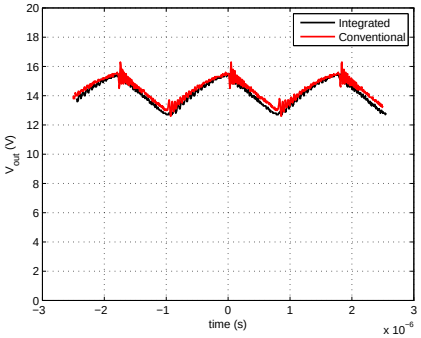
(a) Drain source voltage.



(b) Inductor L1 voltage.

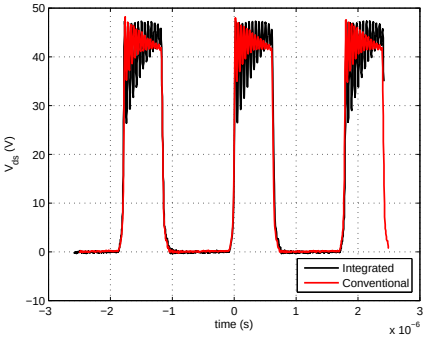


(c) Capacitor Cs voltage.

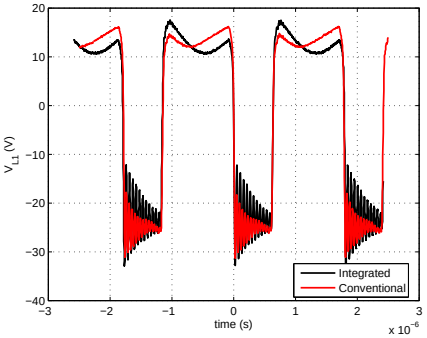


(d) Output voltage.

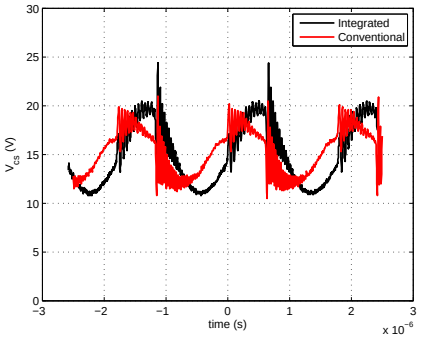
Figure 4.15: Voltages during step down operation in assembly A.



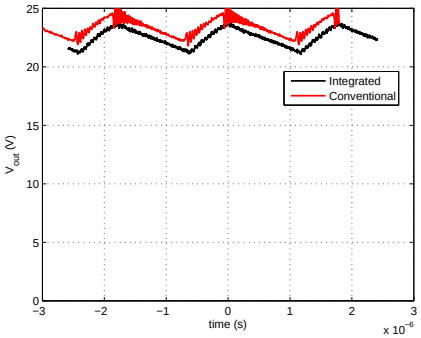
(a) Drain source voltage.



(b) Inductor L1 voltage.

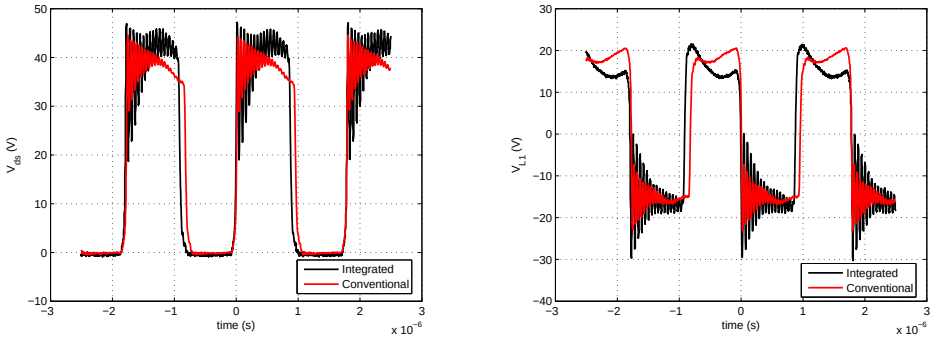


(c) Capacitor Cs voltage.



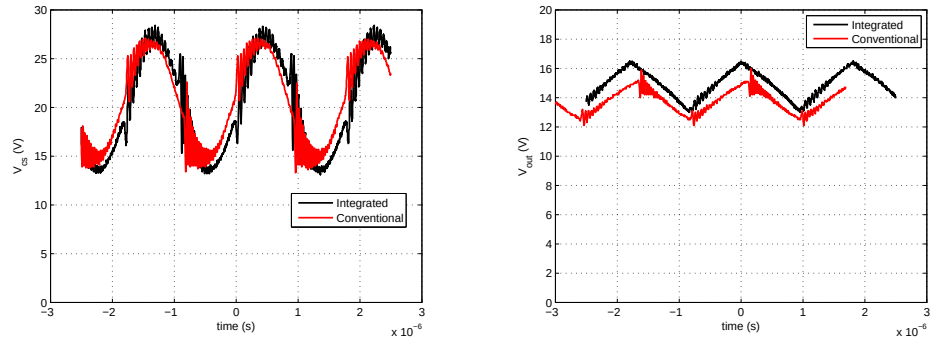
(d) Output voltage.

Figure 4.16: Voltages during step up operation in assembly B.



(a) Drain source voltage.

(b) Inductor L1 voltage.



(c) Capacitor Cs voltage.

(d) Output voltage.

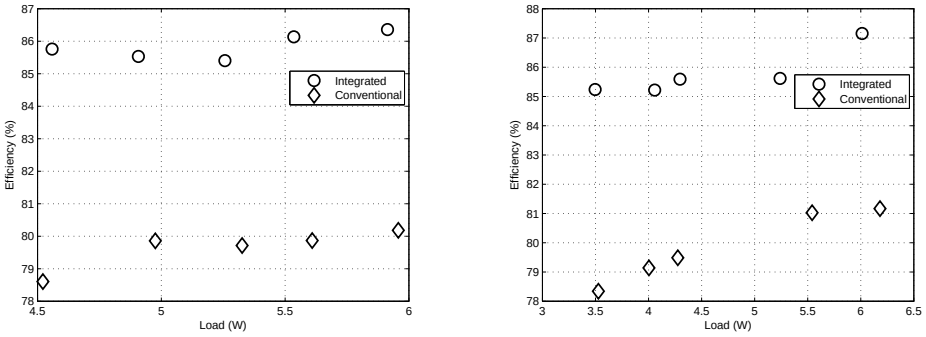
Figure 4.17: Voltages during step down operation in assembly B.

4.6.3 Efficiency

The efficiency of the two integrated prototypes along with their associated conventional circuits for different output power conditions is depicted in figures 4.18 and 4.19. The efficiency of the circuits was calculated using equation 4.9.

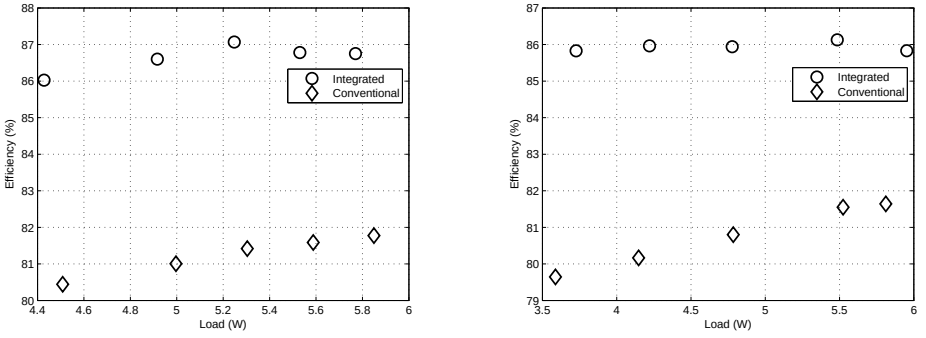
$$\eta = \frac{P_{out(DC)}}{P_{in(DC)}} \tag{4.9}$$

During step up operation for assembly A the measured efficiency ranges from 85.4% to 86.3% and from 78.6% to 80.2% for the conventional circuit. During step down operation for assembly A the measured efficiency ranges from 85.2% to 87.2% and from 78.3% to 81.1% for the conventional circuit. For assembly B during step up operation, the measured efficiency ranges from 86.0% to 87.1% and from 80.4% to 81.7% for the conventional circuit. During step down operation for assembly B the measured efficiency ranges from 85.8% to 86.1% and from 79.7% to 81.6% for the conventional circuit. In all the modes of operation the integrated circuits are more efficient than the conventional circuits. The increased efficiency can firstly be attributed to the differences in the magnetic component. The integrated circuits have a larger magnetic core which is more efficient than the smaller core found on the conventional circuits. The integrated circuits also have a construction well suited for



(a) Step up operation. (b) Step down operation.

Figure 4.18: Efficiency measurements for assembly A.



(a) Step up operation. (b) Step down operation.

Figure 4.19: Efficiency measurements for assembly B.

high frequency operation resulting in increased efficiency. The efficiency of the integrated circuits does demonstrate one aspect in the viability of developing a coupled inductor SEPIC using planar integrated components.

4.7 Assembly Footprint Reduction

The footprint of the proposed prototypes is rather large and would generally not be attractive in many applications. The size of the footprint can be reduced by constructing the inductors using multiple turns instead of a single turn, however some considerations are necessary.

The multiple inductor turns may be in the form of a spiral on one layer which does give rise to an unwanted intra-winding capacitance. A method to compute this capacitance has been previously described [36] and would be useful in predicting the resonant frequency of the structure. The inductor turns may also span across multiple layers which does give rise to an unwanted inter-layer capacitance. Mitigating this capacitance entails increasing the insulation thickness between the various conducting layers however this is ultimately constrained by the winding window height. The significance of these parasitic capacitances on the performance of the circuit was not assessed in this work and would therefore be suitable for future work.

4.8 Suitability to Application

The experimental results demonstrate similarities in the performance of the conventional circuits and the planar integrated circuits. There are however other aspects which make the planar integrated coupled inductor SEPIC more suited for LED lighting applications:

- The planar integrated circuit would typically have a broad footprint although significantly smaller than that of the constructed prototypes. The broad footprint would result in a good thermal performance which is of significance in LED lighting applications as the circuit would typically run for extended hours.
- It is envisaged that the planar structure would be easier to manufacture, possibly in a highly automated process which would result in reduced costs. Reduced costs in a new lighting technology such as LED lighting would help increase its widespread acceptance.
- Besides the material used in the construction of the prototypes, the integrated circuits can be built with other high permittivity dielectrics. Alternate materials to the electrolytic capacitors which are common in the conventional circuit would promise a more reliable circuit.
- The reduced interconnections between the circuit components would also improve the reliability and robustness of the structure.

Chapter 5

Conclusion

The study as presented consists of the three sections. The first section entailed a mathematical analysis of the coupled inductor SEPIC and an assessment of the effect of inductor coupling on a SEPIC. Following was a review of a two conductor planar integrated passive. The last section was the planar component integration in a coupled inductor SEPIC. In this chapter each section is summarised and the conclusions from each section are highlighted. Some suggestions for future work are also made.

5.1 Coupled Inductor SEPIC Analysis

A piecewise linear analysis of the coupled inductor SEPIC is presented for ideal steady state operation in continuous conduction mode. The analysis is limited to consideration of the dynamics associated with three passive components instead of four, the fourth being the output capacitor. An implication of this is that aspects such as a change in the average output current cannot be observed. The derived equations are nonetheless able to describe the operation of the circuit at a fundamental level. The equations also allow for a sensitivity analysis to be performed for some of the component dynamics. In this work the derived equations are applied in studying inductor coupling and the effects it has on the current and voltage ripple. From the study it is noted that for tight coupling, low current ripple and low voltage ripple are achieved when the inductances are equal. It is also noted that weaker coupling is more suited for the 'zero' current ripple technique. A configuration where the inductances are equal and where the coupling coefficient is unity was chosen for this dissertation.

Future work in the piecewise linear analysis could entail derivation of the equations that take the output capacitor into account. This of course would increase the order of the differential equations but would yield a more complete mathematical description of the coupled inductor SEPIC in the time domain.

5.2 The Two Conductor Planar Integrated Passive

The two conductor planar integrated passive is reviewed. The review entails a study of the various terminal uses of the structure as well as the use of the structure in constructing more complex integrated assemblies. The study of the various terminal uses entailed the use of a practical structure as well as the split-c model. The split-c model was included in the study with the secondary objective of gaining insight into its use for modelling integrated passives. For each of the terminal uses, a measured frequency response was compared to an ideal response and agreement was observed for low frequencies. This indicates that the split-c model can be used for modelling a two conductor planar integrated passive at low frequencies.

A study of the terminal uses showed some of the equivalent circuit functions that can be obtained from the integrated passive. The different equivalent circuits are regarded as building blocks for developing more complex integrated assemblies. This aspect is demonstrated through case studies in which multiple modules are combined to create functional circuits. The work suggests that multiple modules can be combined into a single core without any adverse effects. This is also demonstrated in the development of the planar integrated coupled inductor SEPIC.

5.3 Passive Component Integration in a Coupled Inductor SEPIC

The approach to integrating the passive components in a coupled inductor SEPIC is described as a three part design process consisting of an assembly design, a circuit level design, and a structural design. From the design process, two integrated assemblies of the coupled inductor SEPIC were proposed. A prototype for each planar integrated coupled inductor SEPIC assembly was also built and experimentally verified. The experimental work entailed impedance measurements, waveform measurements during voltage conversion operation, as well as efficiency measurements. The experimental results were generally in agreement with what was expected. This demonstrates the validity of integrating the passive components in a coupled inductor SEPIC.

The ability to integrate the passive components in a coupled inductor SEPIC poses a new way of thinking about constructing the circuit. It is imagined this may have benefits in several applications. The planar integrated coupled inductor SEPIC is suited in LED lighting applications because the construction is associated with several potential benefits. These include an improved thermal performance, ease of manufacture resulting in reduced costs, and improved robustness and reliability.

The constructed planar integrated circuits have a large footprint which can be reduced by constructing the inductance using multi-turns instead of a single turn. However this could not be investigated in this work as multi-turn structures have inherent parasitic capacitances which can compromise the operation of the circuit. Future work could then involve constructing the integrated circuits using multi-turns instead of single turns. The work should also entail the use of alternative materials so that higher powers are achieved. This is because many LED drivers such as those found in buildings typically operate at higher power levels than that achieved in this work. Once a structure is of a reasonable size and power has been obtained, the circuit could be designed so that it meets electromagnetic interference and electromagnetic compatibility standards. Another aspect to consider in future work is a thermal design which would help in increasing the power density of each circuit.

References

[1] M. Ali, M. Orabi, M. E. Ahmed, and A. El-Aroudi. "Design consideration of modified SEPIC converter for LED lamp driver." In *IEEE PEDG 2010: The 2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems*, pp. 394 –399. June 2010.

[2] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, and S.-C. Mou. "A High-Efficiency Dimmable LED Driver for Low-Power Lighting Applications." *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 735 –743, February 2010.

[3] S. Winder. *Power Supplies for LED Driving*. Elsevier, USA, first ed., 2008.

[4] Z. Ye, F. Greenfeld, and Z. Liang. "A topology study of single-phase offline AC/DC converters for high brightness white LED lighting with power factor pre-regulation and brightness dimmable." In *34th Annual Conference of IEEE Industrial Electronics Society (IECON 2008)*, pp. 1961 –1967. November 2008.

[5] W. Gu and D. Zhang. *Designing a SEPIC Converter*. Appication Note, National Semiconductor Corporation, 2008.

[6] J. Kolar, H. Sree, N. Mohan, and F. Zach. "Novel aspects of an application of 'zero'-ripple techniques to basic converter topologies." In *28th Annual IEEE Power Electronics Specialists Conference*, vol. 1, pp. 796 –803. June 1997.

[7] D. WeiHua, Z. Bo, D. GuiPing, and H. ZongBo. "Coupled inductor design with small voltage spike of SEPIC converter." In *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition*, vol. 3, pp. 1922 –1926. March 2005.

[8] J. Betten. "SEPIC converter benefits from leakage inductance.", PowerPulse.Net Design Features [Online], May 2010. `http://www.powerpulse.net/techPaper.php?paperID=153`; accessed 18 July 2011.

[9] J. Betten and R. Kollman. "SEPIC outperforms the flyback.", Texas Instruments, Jan 2006. `http://www.eetimes.com/design/power-management-design/4009613/No-need-to-fear-SEPIC-outperforms-the-flyback`; accessed 25 September 2011.

[10] F. Lee, J. van Wyk, D. Boroyevich, G.-Q. Lu, Z. Liang, and P. Barbosa. "Technology trends toward a system-in-a-module in power electronics." *IEEE Circuits and Systems Magazine*, vol. 2, no. 4, pp. 4 – 22, 2002.

[11] M. Smit, J. Ferreira, and J. Van Wyk. "Application of transmission line principles to high frequency power converters." In *23rd Annual IEEE Power Electronics Specialists Conference*, vol. 2, pp. 1423 –1430. June 1992.

[12] R. Reeves. "Inductor-capacitor hybrid." *Proceedings of the Institution of Electrical Engineers*, vol. 122, no. 11, pp. 1323 –1326, November 1975.

[13] R. Reeves. "Choke - capacitor hybrid as a fluorescent-lamp ballast." *Proceedings of the Institution of Electrical Engineers*, vol. 122, no. 10, pp. 1151 –1152, October 1975.

[14] R. Kemp, P. Murgatroyd, and N. Walker. "Self resonance in foil inductors." *Electronics Letters*, vol. 11, no. 15, pp. 337 –338, July 1975.

[15] O. Stielau, J. van Wyk, M. Ehsani, and I. Pitel. "Integrated reactive components in power electronic circuits." In *21st Annual IEEE Power Electronics Specialists Conference*, pp. 831 –838. 1990.

[16] G. McMullin. *Frequency and Time Domain Modelling of Integrated Passives*. MSc Dissertation, University of Johannesburg, June 2006.

[17] J. van Wyk and J. Ferreira. "Some present and future trends in power electronic converters." In *Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation. Power Electronics and Motion Control.*, vol. 1, pp. 9 –18. November 1992.

[18] L. Zhao, J. Strydom, and J. van Wyk. "A planar multicell structure for advanced integrated reactive power modules." *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1656 – 1664, November 2003.

[19] I. Hofsajer, J. Ferreira, and J. Van Wyk. "A comparative study of some electromagnetically integrated structures in hybrid technology." In *29th Annual IEEE Power Electronics Specialists Conference*, vol. 2, pp. 1957 –1963. May 1998.

[20] I. Hofsajer, J. Ferreira, and D. van Wyk. "Design and analysis of planar integrated L-C-T components for converters." *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1221 –1227, November 2000.

[21] M. Gerber, I. Hofsajer, and W. Cronje. "Construction and modelling of a planar multilayer electromagnetically integrated LCCT component." In *Conference Record of the 2000 IEEE Industry Applications Conference*, vol. 5, pp. 3044 –3050. 2000.

[22] Y. Liang, W. Liu, B. Lu, and J. Van Wyk. "Design of integrated passive component for a 1 MHz 1 kW half-bridge LLC resonant converter." In *Conference Record of the 2005 IEEE Industry Applications Conference. Fourtieth IAS Annual Meeting.*, vol. 3, pp. 2223 – 2228. October 2005.

[23] J. Claassens, I. Hofsajer, and K. de Jager. "Passive component integration in a ZVS flyback converter." In *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 539 – 544. March 2006.

[24] J. Stewart. *Calculus: Concepts & Contexts*. Cengage Learning, USA, fourth ed., 2009.

[25] R. Reeves. Personal Communication, 15 June 2012.

[26] C. W. T. McLyman. *Designing Magnetic Components for High Frequency DC-DC Converters*. KgMagnetics Inc., California, first ed., 1993.

[27] C. R. Paul. *Introduction to Electromagnetic Compatibility*. John Wiley& Sons, Inc., New Jersey, second ed., 2006.

[28] L. Zhao. *Generalized Frequency Plane Model of Integrated Electromagnetic Power Passives*. PhD Thesis, Virginia Polytechnic Institute and State University, May 2004.

[29] L. Zhao and J. van Wyk. "Frequency-domain modeling of integrated electromagnetic power passives by a generalized two-conductor transmission structure." *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 11, pp. 2325 – 2337, November 2004.

[30] R. Chen. *Integrated EMI Filters for Switch Mode Power Supplies*. PhD Thesis, Virginia Polytechnic Institute and State University, November 2004.

[31] M. Smit, J. Ferreira, J. Van Wyk, and M. Ehsani. "A new ultrasonic series resonant converter with integrated L-C-T." In *21st Annual IEEE Power Electronics Specialists Conference*, pp. 729 –733. 1990.

[32] P. Murgatroyd. "Field and circuit models for the wound foil inductor." *Gordon and Breach Science Publishers Ltd*, vol. 3, pp. 92 –102, May 1976.

[33] G. S. McMullin and I. W. Hofsajer. "A Simulation Tool for Integrated Passive Structures in Power Electronic Circuits." *2006 4th International Conference on Integrated Power Systems (CIPS)*, pp. 1 –6, June 2006.

[34] C. Oberholzer and I. Hofsajer. "Modelling and Simulation Techniques for Multilayer Integrated Passive Structures in the Time Domain." In *IEEE 38th Annual Power Electronics Specialists Conference*, pp. 2248 –2253. June 2007.

[35] M. Ehsani, P. Le Polles, M. Arefeen, I. Pitel, and J. Van Wyk. "Computer-aided design and application of integrated LC filters." *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 182 –190, January 1996.

[36] L. Zhao, J. Strydom, and J. van Wyk. "Wide band modeling of integrated power passive structures: the series resonator." In *2002 IEEE 33rd Annual Power Electronics Specialists Conference*, vol. 3, pp. 1283 – 1288. June 2002.

[37] P. Murgatroyd and N. Walker. "Lumped-circuit model for inductor-capacitor hybrid." *Electronics Letters*, vol. 12, no. 1, pp. 2 –3, August 1976.

[38] K. de Jager and I. W. Hofsajer. "Development of Design Guidelines for the Synthesis of Networks with Planar Integrated LC Structures." *2006 4th International Conference on Integrated Power Systems (CIPS)*, pp. 1 –8, June 2006.

Appendix A

Verification of Analytic Expressions

The correctness of the derived equations in chapter 2 for the coupled inductor SEPIC is well demonstrated through a comparison with a simulated response. The circuit used in the analysis and in the simulation is as in figure A.1. The components and operation details were: $L_1 = L_2 = 240\mu H$, $k = 0.9$, $C_s = 22\mu H$, $D = 0.43$, $f_s = 50kHz$ and $V_s = 24V$. The analytic response and the simulated response are presented in figure A.2. The analytic response in figure A.2(a) uses equations 2.4 and 2.7 which are plotted for successive time intervals. Similarly the analytic response in figure A.2(b) uses equations 2.9 and 2.10 which are plotted for successive time intervals. Lastly the analytic response in figure A.2(c) uses equations 2.11 and 2.12 which are also plotted for successive time intervals. On the plots, there is only a slight deviation in the coupling capacitor voltage illustrated in figure A.2(c) where the analytic response is slightly higher in magnitude than the simulated response. Nonetheless as observed in figures A.2(a) and A.2(b), the analytic response and simulated response are almost indistinguishable. This confirms the correctness of the derived equations. The plots also indicate minor oscillations at the natural frequency of the system.

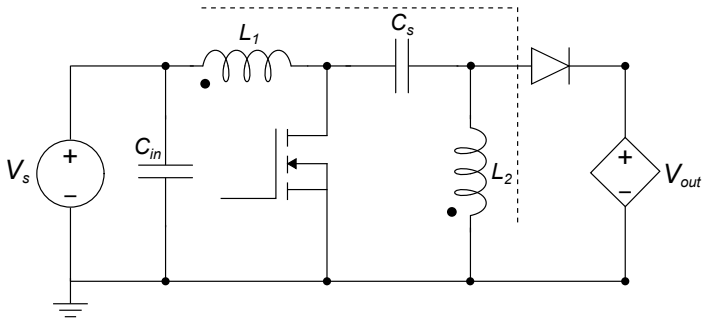
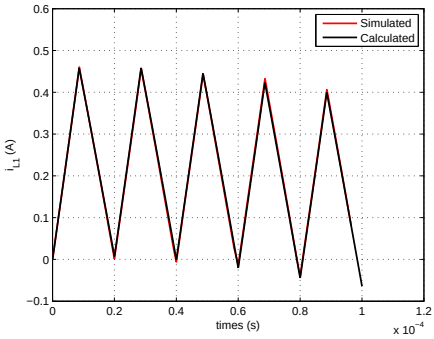
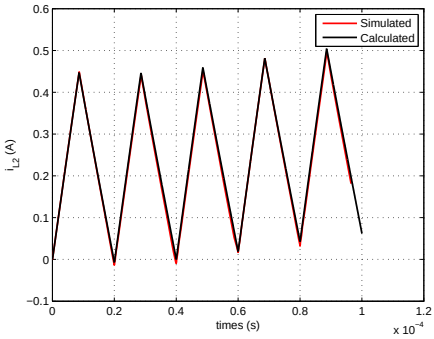


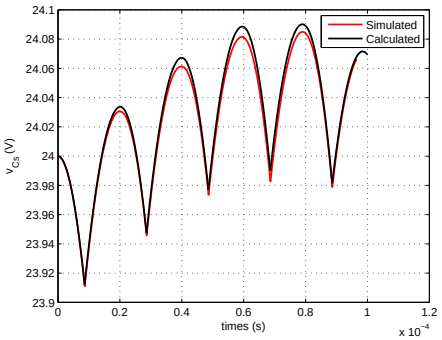
Figure A.1: Effective coupled inductor SEPIC used in the analysis.



(a) Inductor L1 current



(b) Inductor L2 current



(c) Coupling capacitor Cs voltage

Figure A.2: Analytic and simulated, voltage and current waveforms during a switching cycle.

Appendix B

Circuit Level Design of a Coupled Inductor SEPIC

This appendix will discuss the circuit level design of a coupled inductor SEPIC. The design process has been presented in [5] and is briefly reviewed here. The circuit level design entails sizing the passive components of the circuit based on some input parameters. For completeness this chapter will also discuss considerations for specifying the switching devices.

B.1 Design Requirements

The coupled inductor SEPIC is shown in figure B.1. The circuit level design process has input parameters which are:

- Input voltage range $V_{in(min)}$ and $V_{in(max)}$.
- Output voltage range $V_{out(min)}$ and $V_{out(max)}$.
- Switching frequency f_s.
- Operating power level, from which the current range is also determined.
- Inductor coupling coefficient.

As will be shown in the following section these input design parameters are used in mathematical equations to obtain the passive component sizes in the circuit. The indicated input design parameters are also used in specifying the ratings of the switching devices.

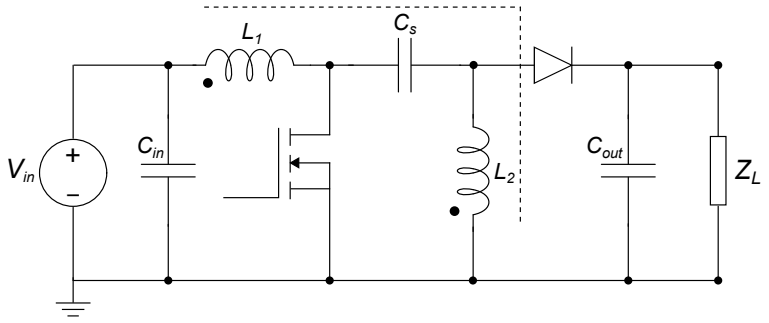


Figure B.1: Coupled Inductor SEPIC Topology.

B.2 Passive Component Selection

The sizing of the passive components is based on the consideration of an acceptable amount of voltage or current ripple for a given time interval. There are typical voltage or current ripple percentages which are usually selected that result in predictable operation. In cases where the component size forms part of the constraints the design approach may become iterative. The typical voltage or current ripple percentages that are selected for predictable operation may also have to be adjusted.

The design approach is now considered and to begin with, duty cycle aspects are discussed.

B.2.1 Duty Cycle

The duty cycle is also used when specifying the passive component sizes as well as some of the semiconductor performance requirements as will be seen shortly. In general, the duty cycle for a coupled inductor SEPIC operating in continuous conduction mode is given by

$$D = \frac{V_{out} + V_D}{V_{in} + V_{out} + V_D}$$

For an instance where the input and output voltage is specified as a range instead of a fixed value, the maximum duty cycle is given by equation B.1.

$$D_{max} = \frac{V_{out(max)} + V_D}{V_{in(min)} + V_{out(max)} + V_D} \tag{B.1}$$

Similarly for an instance where the input and output voltage is a range, the minimum duty cycle is given by equation B.2.

$$D_{min} = \frac{V_{out(min)} + V_D}{V_{in(max)} + V_{out(min)} + V_D} \tag{B.2}$$

B.2.2 Inductor Selection

The inductors are sized based on an acceptable amount of current change (or ripple) through the inductor for a given time interval in steady state operation. The requirement arises from the ideal voltage and current relationship of an inductor given by

$$v_L = L\frac{di}{dt}$$

For coupled inductors in a SEPIC the approach to determining the required inductor sizes is different compared to a single uncoupled inductor. For unity coupling, the required inductor sizes can be determined by first considering the voltage definition across an inductor. For instance considering the voltage across inductor L_1 during a switching interval given by

$$v_{L1} = L_1\frac{di_1}{dt} + M\frac{di_2}{dt}$$

where i_1 is the current in inductor L_1 and i_2 is the current in inductor L_2. If L_1 is chosen to equal L_2 then $L_1 \approx M$ for almost unity coupling. Requiring the current ripple to be the same in both inductors, that is $\Delta i_1 = \Delta i_2 = \Delta i$ then

$$v_{L1} \approx 2L_1\frac{\Delta i}{\Delta t}$$

Typically the peak to peak current ripple (Δi) is limited to 40% of the largest expected average current. For the coupled inductor SEPIC, the largest average current is obtained at $V_{out(max)}$ and $V_{in(min)}$ at maximum output power. Hence

$$\Delta i = 0.4I_{in} = 0.4I_{out}\frac{V_{out(max)} + V_D}{V_{in(min)}}$$

The required inductor sizes are then given by equation B.3.

$$L_1 = L_2 = \frac{V_{in(min)}D_{max}T_s}{2\Delta i} \tag{B.3}$$

In constructing or purchasing an inductor, often the peak current is required in order to establish saturation limits. The peak inductor currents are given by

$$I_{L1(peak)} = I_{out}\frac{V_{out(max)} + V_D}{V_{in(min)}}\left(1 + \frac{40\%}{2}\right)$$

$$I_{L2(peak)} = I_{out}\left(1 + \frac{40\%}{2}\right)$$

B.2.3 Series Capacitor Selection

Similar to the inductors the capacitors are sized based on an acceptable voltage change for a given time interval as is in the ideal operation of a capacitor.

$$i = C\frac{dv}{dt}$$

Design guides are varied on the typical requirements of voltage ripple for the series coupling capacitor. A peak to peak voltage ripple (Δv_{Cs}) of 5% of the average capacitor voltage has been found to result in predictable operation. The capacitor size is obtained using equation B.4.

$$C_s = \frac{I_{out} D_{max} T_s}{\Delta v_{Cs}} \tag{B.4}$$

Besides the voltage ripple, the series coupling capacitor must also meet an RMS current rating for the maximum output power level. The capacitor must have a current rating that exceeds

$$I_{Cs(RMS)} = I_{out}\sqrt{\frac{V_{out(max)} + V_D}{V_{in(min)}}}$$

B.2.4 Output Capacitor Selection

The output capacitor is also sized based on an acceptable amount of voltage change for a given time interval. The ripple requirements for the output capacitor are however more stringent than the series coupling capacitor so the capacitor's equivalent series resistance (ESR) is also considered.

A reasonable approach that has been used is to assume the ESR contributes to half of the ripple and that the capacitance contributes the other half [5]. The capacitor size would then be specified by equation B.5.

$$C_{out} \geq \frac{I_{out} D_{max} T_s}{0.5\Delta v_{Cout}} \tag{B.5}$$

The ESR of the capacitor would have to be

$$ESR \leq \frac{I_{out} D_{max} T_s}{0.5\Delta v_{Cout}}$$

The capacitor also needs to have a current rating higher than the RMS current requirement given by

$$I_{Cout(RMS)} = I_{out}\sqrt{\frac{V_{out(max)} + V_D}{V_{in(min)}}}$$

B.2.5 Input Capacitor Selection

An input capacitor is not entirely critical on the coupled inductor SEPIC as inductor L_1 ensures the input current is continuous. It may however be included to mitigate impedance interactions for certain applications [5].

B.3 Selection of Switching Devices

B.3.1 MOSFET Selection

The primary requirements for the MOSFET involve considering the maximum continuous forward current as well as the maximum allowable drain-source voltage, which is significant when the MOSFET is not conducting. Sometimes it may be necessary to also consider the peak forward current. A measure of the continuous forward current is given by the RMS current value as in equation B.6.

$$I_{DS(RMS)} = I_{out}\sqrt{\frac{(V_{out(max)} + V_{in(min)} + V_D) \times (V_{out(max)} + V_D)}{V_{in(min)}^2}} \tag{B.6}$$

The peak current is given by

$$I_{DS(peak)} = I_{L1(peak)} + I_{L2(peak)}$$

Usually the MOSFET's datasheet will specify this value with an associated time interval which must be evaluated carefully for the application in question.

The transistor should also be able to handle the drain source voltage given by equation B.7.

$$V_{DS} = V_{in(max)} + V_{out(max)} \tag{B.7}$$

B.3.2 Diode Selection

Similar to the MOSFET, the primary requirements for a diode are that it must be able to handle the maximum continuous forward current and a peak reverse voltage, that is applied when the diode is not conducting. The diode must also handle a peak forward current for a specified time interval. The maximum continuous forward current the diode should handle is equal to the output current. The peak reverse voltage applied to the diode when it's not conducting is given by equation B.8.

$$V_{RD} = V_{in(max)} + V_{out(max)} \tag{B.8}$$

The peak forward current is given by

$$I_{D(peak)} = I_{L1(peak)} + I_{L2(peak)}$$