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A NOVEL TEST METHOD FOR MINIMISING ENERGY COSTS IN IGBT POWER CYCLING STUDIES

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A thesis submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, in fulfillment of the requirements for the degree of Doctor of Philosophy.

Johannesburg, 2006

DECLARATION

I declare that this thesis is my own, unaided work. It is being submitted for the degree of Doctor of Philosophy in the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination in any other University.

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_____ day of _____ 2006

ABSTRACT

Insulated Gate Bipolar Transistors (IGBTs) are popular power electronic switching devices with several advantages. However, they have been known to fail in the field when subjected to significant variations in power dissipation – known as power cycling. In the work presented here, a novel alternating-current (AC) power cycling test method for IGBTs together with their free-wheeling diodes is proposed and verified.

A review of previous work revealed that the parameter that most affects IGBT lifetime under power cycling conditions is the variation in its junction-case temperature difference (ΔT_{jc}). Through simulation, the behaviour of a conventional single phase inverter (H-bridge) using simple pulse width modulation (PWM) control was quantified, and the effect of switching frequency and load power factor was studied.

Results of the simulations and literature review were used to develop design criteria for a new AC test circuit. The new AC test circuit (a modified version of the conventional H-bridge) was then designed and its performance compared to the criteria and to the simulation results of the conventional circuit. The circuit was then built and its performance was validated. The circuit complied with the performance criteria, in particular the desired variation in ΔT_{jc}, to an adequate degree of accuracy.

The proposed test circuit is novel for several reasons. The stresses on devices used in a conventional H-bridge using a high power factor inductive load are reproduced using a low power factor inductive load, considerably reducing the energy cost of running such a test. IGBT switching losses are not actively reduced, as is normal practice, but instead are actively increased to generate the required losses. Free-wheeling diodes are also tested, but do not have significant

switching losses, as the nature of the test circuit dictates that these be transferred to the IGBTs.

The main drawback of the proposed test circuit is that a larger number of devices are needed; however, this tradeoff is necessary to obtain the energy cost savings provided by this circuit.

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	Alternating current
Al	Aluminium
Al_2O_3	Aluminium Oxide
AlN	Aluminium Nitride
AlSiC	Aluminium Silicon Carbide
BeO	Beryllium Oxide
BIL	Basic insulation level
BJT	Bipolar junction transistor
CAL	Controlled Axial Lifetime
C_{snub}	Snubber capacitor
CSP	Chip-scale packaging
CTE	Coefficient of thermal expansion
Cu	Copper
D^2BGA	Die dimensional ball grid array
DBC	Direct bonded copper
DC	Direct current
DUT	Device under test
E_{cond}	Conduction energy loss
EMI	Electromagnetic interference
E_{off}	Turn-off energy
$E_{off(tail)}$	Tail current during IGBT turn-off
E_{on}	Turn-on energy
$E_{on(norm)}$	Normalised turn-on energy
FCOF	Flip-chip on flex
FEM	Finite Element Method
GTO	Gate turn-off transistor
I_1	Current at the end of IGBT turn-on
I_2	Current at the start of IGBT turn-off
I_C	IGBT collector current
$I_{C(max)}$	Maximum rated IGBT collector current
$I_{C(rated)}$	Rated IGBT collector current
I_{cal}	Calibration current used to measure ΔT_{jc}
IEC	International Electrotechnical Commission
I_G	IGBT gate current
$I_{G(sat)}$	IGBT gate leakage current
IGBT	Insulated gate bipolar transistor
IGT	Insulated gate transistor
I_{load}	IGBT or diode load current (collector current, I_C, in the case of an IGBT and anode current, I_A, in the case of a diode)
I_{off}	IGBT or diode load current during the off period, t_{off}, of a power cycling test
I_{on}	IGBT or diode load current during the conduction period, t_{on}, of a power cycling test
IR	Infra-Red
I_{snub}	Snubber current
I_{tail}	Current at start of tail during IGBT turn-off
L_{CE}	IGBT collector-emitter inductance
L_G	IGBT gate inductance

L_S	Stray inductance
Mo	Molybdenum
Mo	Molybdenum
MOSFET	Metal oxide semiconductor field-effect transistor
MOV	Metal oxide varistor
MPIPPS	Metal-posts interconnected parallel-plate structure
N_f	Number of power cycles to failure of an IGBT or diode
Ni	Nickel
NPT	Non punch through
$P_{cond(ave)}$	Average conduction loss
P_{loss}	Total power losses
P_{off}	Turn-off power loss
P_{on}	Turn-on power loss
PT	Punch through
PWM	Pulse width modulation
Q_{rr}	Diode reverse recovery charge
Q_{rr}	Diode reverse recovery charge
R_G	IGBT gate resistor (discrete resistance added externally)
R_{snub}	Snubber resistor
R_{thjc}	Thermal resistance, an alternative term for Z_{thjcss}
SAD	Silicon avalanche diode
SCR	Silicon controlled rectifier (also called “thyristor”)
Si	Silicon
SOA	Safe operating area
T	Switching period
t_1	IGBT turn-on time
t_2	IGBT turn-off time
T_{amb}	Ambient temperature
T_{case}	Temperature on the case of an IGBT module
$T_{case(max)}$	Maximum case temperature
$T_{case(min)}$	Minimum case temperature
t_{cond}	Time period during which a device conducts current
t_f	90%-10% IGBT turn-off current fall time
T_H	Temperature on the surface of a heatsink
Ti	Titanium
T_j	Absolute IGBT or diode junction temperature
t_{off}	Time period during which an IGBT or diode does not conduct current
t_{on}	Time period during which an IGBT or diode conducts current
t_r	10%-90% IGBT turn-on current rise time
TSEP	Temperature sensitive electrical parameter
tstep	Simulation time step
t_{tail}	Duration of tail current during IGBT turn-off
TTL	Transistor-transistor logic
V_1	Voltage at the start of IGBT turn-on
V_2	Voltage at the end of IGBT turn-off
V_3	IGBT collector-emitter voltage when IGBT tail current reaches zero
V_{CC}	DC bus voltage
$V_{CC(ref)}$	Reference DC bus voltage
V_{CE}	IGBT collector-emitter voltage
$V_{CE(max)}$	Maximum rated IGBT collector-emitter voltage
$V_{CE(sat)}$	IGBT forward conduction voltage drop
V_{CE0}	Zero-crossing of IGBT output characteristic
V_{CEN}	IGBT collector-emitter voltage drop at $I_{C(rated)}$

V_F	Diode on-state voltage drop
V_G	Voltage source applied to IGBT gate terminal
V_{GE}	IGBT gate-emitter voltage
$V_{GE(th)}$	IGBT threshold gate-emitter voltage
VSD	Variable speed drive
V_{source}	An applied power source voltage
Z_{thjc}	Junction-case thermal impedance
Z_{thjcss}	Steady-state junction-case thermal impedance
f	PWM switching frequency
ΔT_{jc}	Difference in temperature between the junction and case of an IGBT or diode
$\Delta T_{jccond(ave)}$	Average increase in ΔT_{jc} due to conduction losses
ΔT_{jcmax}	Maximum value of ΔT_{jc} during a power cycling test
ΔT_{jcmin}	Minimum value of ΔT_{jc} during a power cycling test
$\Delta T_{jcsw(ave)}$	Average increase in ΔT_{jc} due to switching losses
τ	Time constant

1. INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) is a power electronic switching device gaining popularity because of its comparatively low switching losses [1] and high switching frequency [2].

A typical IGBT module consists of single or multiple silicon chips on a direct bonded copper (DBC) substrate. Several chips are required for high current modules; these chips are placed in parallel and are connected to one another by aluminium bonding wires. The above setup is mounted on a mounting plate, and housed in plastic packaging which is then filled with silicon gel [3], as shown in Figure 1.1.

IGBTs are used in many applications: static power conversion, uninterruptible power supplies, slip energy recovery systems, power amplifiers and traction (motor drives for trains, trams etc.). The last application, among others, requires repetitive low frequency cycling (of the order of minutes) between periods of low current conduction and high current conduction – this is called “power cycling”. This corresponds, for example, to a train stopping in a station (low current) and traveling between stations (high current), as illustrated for the case of a direct

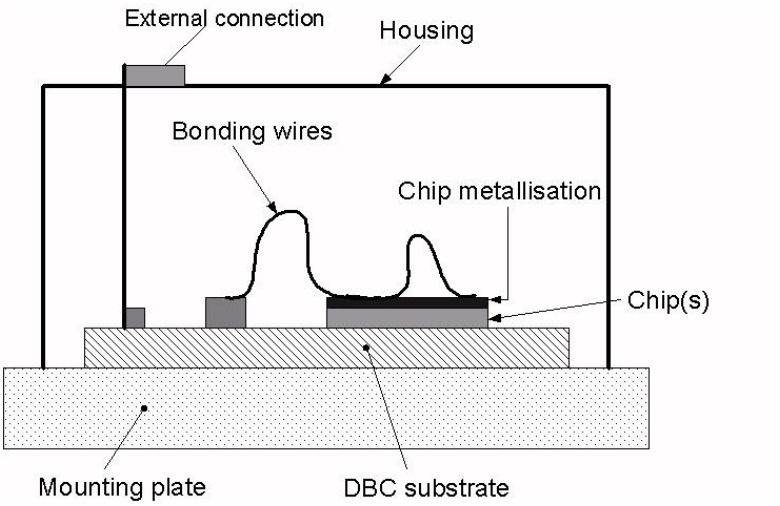


Figure 1.1 Simplified IGBT module structure [3]

current (DC) load in Figure 1.2. IGBTs are required to conduct and survive several million such power cycles in the field [3].

Figure 1.2 also shows the variation in the difference in temperature between the IGBT junction and case, ΔT_{jc}, with power cycling. This variation (ΔT_{jcmax}-ΔT_{jcmin}) will be shown to be an important parameter for power cycling characterisation of IGBTs.

The problem with power cycling is that it has been known to cause failure of IGBTs in the field. This is due to thermo-mechanical effects inside the module. The main cause of failure is the thermal expansion coefficient mismatch between the aluminium bonding wires and the silicon chips, eventually leading to lift-off of the bonding wires due to the repetitive thermal stress. The greater ΔT_{jcmax} and the variation in ΔT_{jc}, the greater the thermal stress and the shorter the module lifetime [3], [4].

There are several other issues causing IGBT module degradation with the number of cycles conducted. First, fatigue of the solder used to bond the chips to the DBC substrate also occurs relatively frequently [4]. Second, extrusion of aluminium grains in the chip metallisation causes an increase in onstate resistance, and hence in forward conduction voltage drop ($V_{CE(sat)}$) and conduction losses [3]. Thirdly, it has been suggested that the bonding wires do not lift off, but break at some

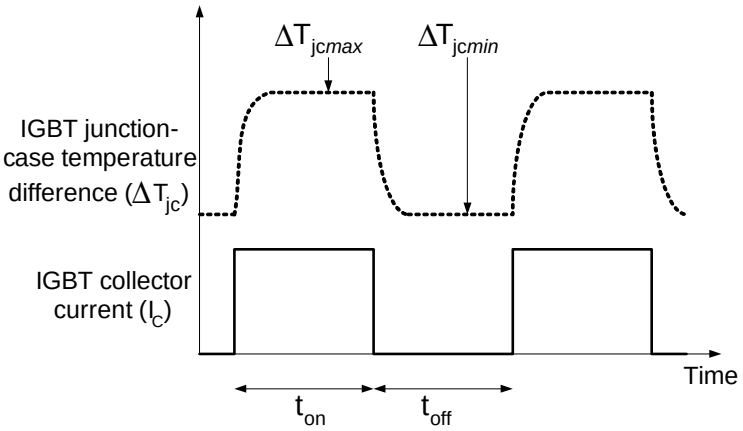


Figure 1.2 Typical power cycling waveforms

distance from the Al-Si interface [2]. Other causes of failure can be an increase in thermal resistance due to the migration of the contact grease between the heatsink and the module [5], and the failure of internal IGBT gate insulation [6].

The majority of the above work was performed on DC loads, often without switching. However, alternating current (AC) loads are also common in traction [7]. It is therefore important to study the effect of switching losses due to pulse width modulation (PWM) control on the stresses on both IGBTs and their free-wheeling diodes. The aim of this study is to propose and evaluate a novel test method for AC power cycling.

The methodology involved the following:

1. Previous work was studied and summarized
2. The stresses that devices used in a conventional single phase inverter (H-bridge) are subjected to were quantified by simulation
3. Based on the above, a list of criteria that an AC test circuit must meet was made
4. A novel test circuit was needed to meet most of these criteria. This was designed and its performance was compared to the above criteria and to the conventional circuit by simulation
5. The test circuit was built and its performance was compared to the simulations

The test circuit is novel for the following reasons:

1. The stresses on IGBTs and free-wheeling diodes used in a conventional H-bridge driving a high power factor inductive load are reproduced with the modified circuit using a low power factor inductive load to an adequate degree of accuracy, significantly reducing the energy costs of running such a test
2. IGBT switching losses are not actively reduced, as is normal practice, but instead are increased and controlled to produce the desired IGBT losses

3. Diodes are also tested, but do not have any significant switching losses, as total diode losses need to be reduced to achieve the required stresses under conventional conditions

This document is structured as follows. A description of IGBT characteristics, structure and packaging is given in Chapter 2, and a summary of previous work undertaken on DC IGBT power cycling is in Chapter 3. In Chapter 4 previous AC power cycling work is summarized and in Chapter 5 the investigation strategy is stated, based on the preceding chapters, and the criteria that the new circuit must meet are listed. In Chapter 6 the conventional H-bridge is simulated. The modified H-bridge is described and simulated in Chapter 7, and implemented in Chapter 8. The results are compared to the criteria of Chapter 5 and to the conventional circuit, validating the design and its model, and several implementation issues are discussed.

2. THE IGBT

2.1 General characteristics

2.1.1 History and operation

The electrical symbol most commonly used for the IGBT is shown in Figure 2.1. This symbol is used throughout this document.

The IGBT was first introduced as the “insulated gate transistor (IGT)” [8] and it became commercially available in 1988 [5]. The structure and equivalent circuit of the original IGT are shown in Figure 2.2.

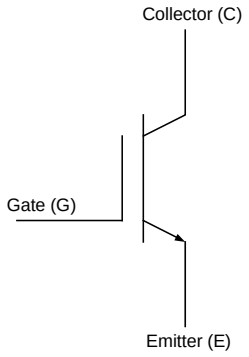


Figure 2.1 IGBT symbol

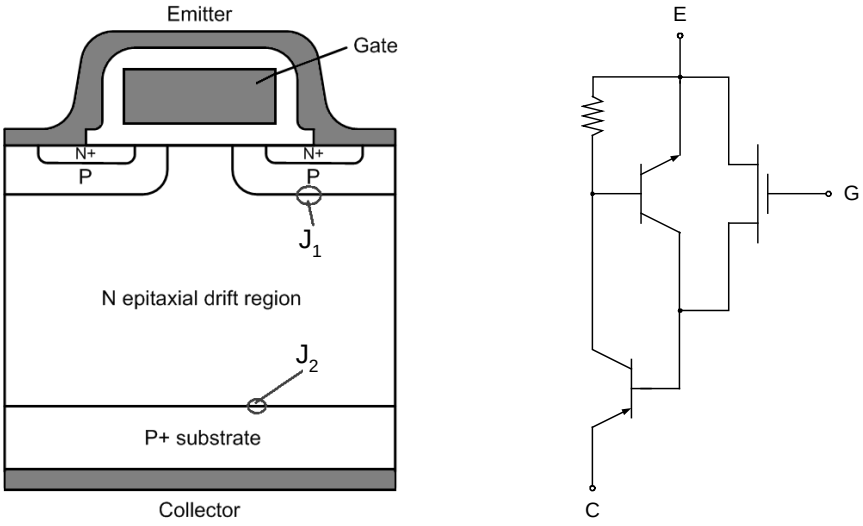


Figure 2.2 Structure and equivalent circuit of the IGT [8]

The advantage of the IGT over existing power switching devices like MOSFETs, BJTs and GTOs was that it had the high input impedance of the MOSFET (making it a voltage-controlled device and hence easy to control and with comparatively low gate energy consumption), while at the same time having the high current carrying capacity, high switching speed and low switching losses of the BJT. IGBT ratings were, however, much lower than those of the GTO, and the IGBT has only recently started to catch up. The properties of the IGBT and other common power electronic switching devices are shown in Table 2.1. The differences in their voltage and current ratings are shown in Figure 2.3.

The properties and operation of the IGBT are as follows [8]. If the collector becomes negative with respect to the emitter, junction J_2 in Figure 2.2 becomes reverse biased and current flow is blocked. This is called the "reverse blocking state". If the collector becomes positive with respect to the emitter (with the gate at the same voltage as the emitter), then junction J_2 becomes forward biased but J_1 becomes reverse biased and current flow is again blocked. This is called the "forward blocking state". If a sufficiently large voltage is now applied to the gate with respect to the emitter, the device becomes forward biased and it behaves similarly to a forward biased diode.

The IGBT is a voltage-controlled device: applying a positive voltage between gate

Table 2.1 Comparison of power electronic device characteristics [9]

	Current density	Switching losses	Driver complexity	Type of driver	SOA	Voltage limits
Power MOSFET	Low	Very low	Low	Voltage	Wide	Low
IGBT	High	Low to medium	Low	Voltage	Wide	High
BJT	Medium	Medium to high	High currents required	Current	Narrow	Medium
Darlington	Low	High	Medium	Current	Narrow	Medium
MCT	Very high	High	Low	Voltage	Narrow	Medium
GTO	Very high	High	High	Current	Narrow	Very high
SITH	High	High	High	Current	Narrow	Medium

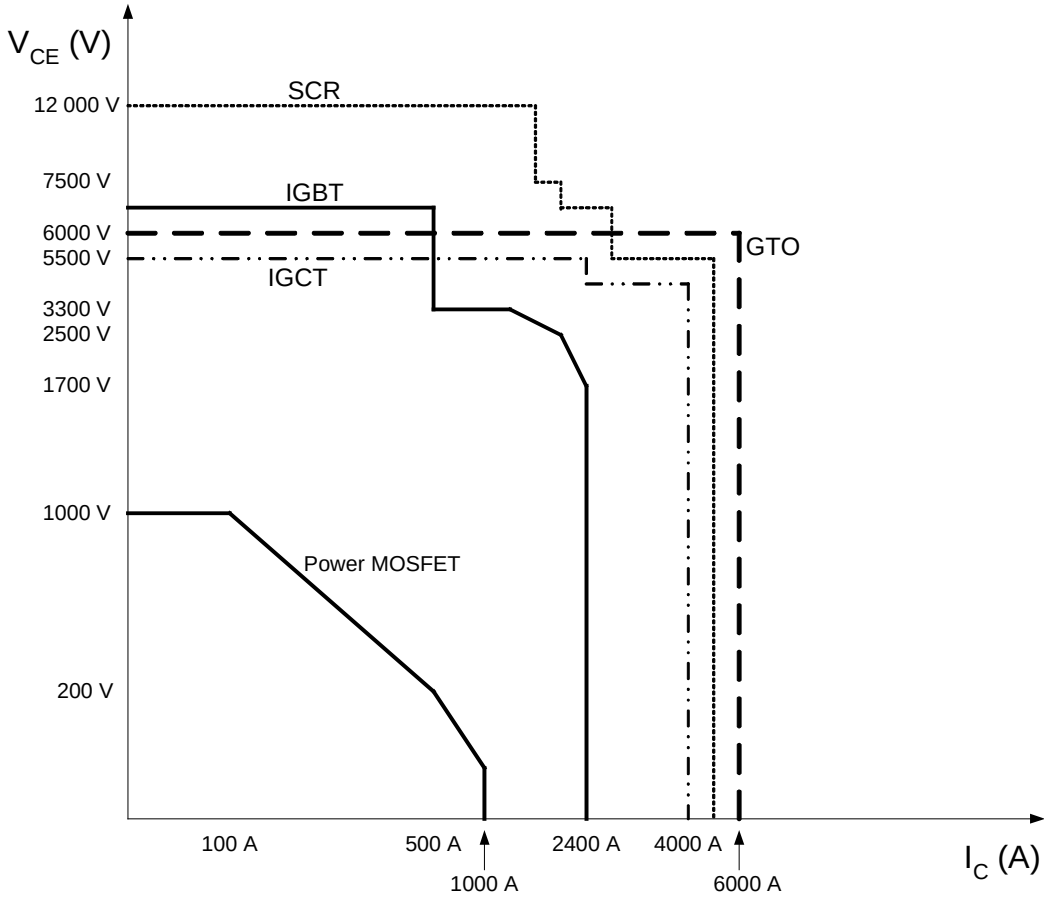


Figure 2.3 Power range of commercially available power electronic devices [7]

and emitter turns the device on and applying a negative voltage turns it off. Typical values of V_{GE} are +15 V (turn-on) and –15 V (turn-off), although absolute maximum ratings are usually +/- 20 V [10]. Typical switching waveforms are shown in Figure 2.4.

2.1.2 Power losses and junction temperature

There are four types of power losses in IGBTs [8]:

- Conduction losses are a function of the collector current during conduction (I_C) and the on-state voltage drop during that time ($V_{CE(sat)}$). The required load current can generally not be changed, but IGBTs with lower $V_{CE(sat)}$ values have lower conduction losses.
- Switching losses are a function of the collector current being switched (I_C), the blocking voltage when the IGBT is off (V_{CE}) and the gate resistance

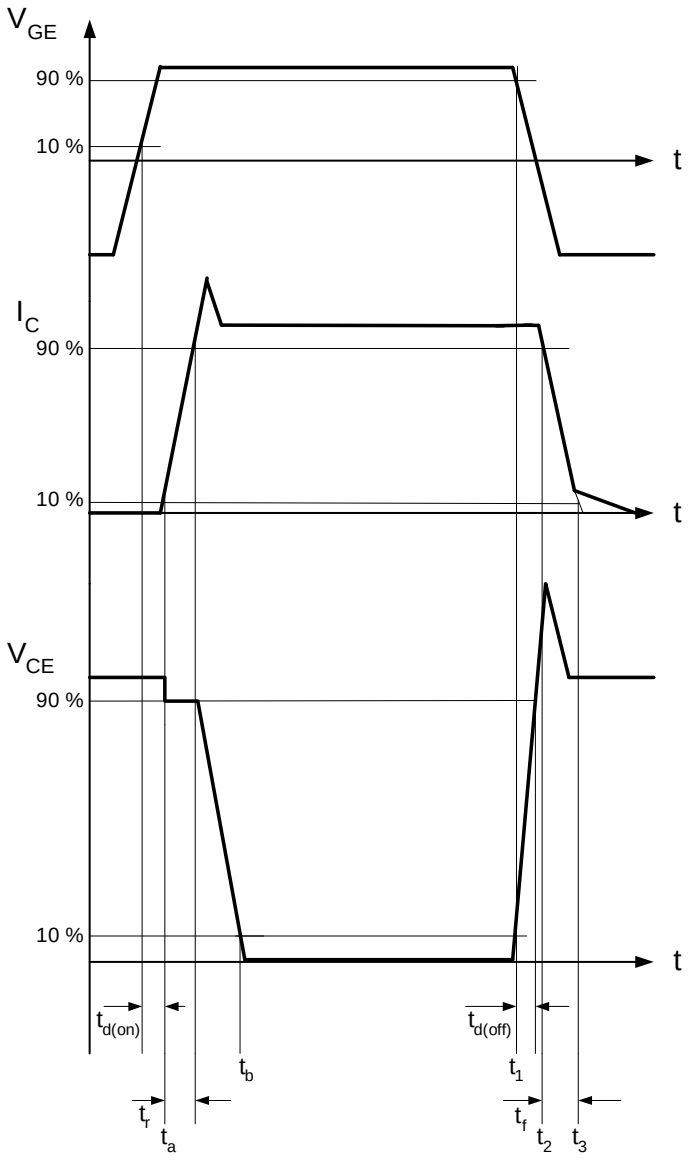


Figure 2.4 Typical IGBT switching waveforms [9]

(R_G). IGBTs usually dissipate significant losses during turn-on and turn-off.

- Off-state losses occur when the IGBT is in the blocking state. IGBTs conduct small leakage currents when they are blocking. These currents, and hence the losses, are usually negligible.
- Gate drive losses are the losses of the gate driver circuit, and hence do not contribute to the device losses. They are also small compared to the device power losses due to the very small gate current drawn by IGBTs.

IGBT power losses are directly related to junction temperature by thermal impedance. This is as follows [10]:

$$T_j = T_{case} + Z_{thjc} \cdot P_{loss} \quad \text{..... (2.1)}$$

where T_j = Absolute IGBT junction temperature (°C or K).

T_{case} = temperature on the IGBT module case (°C or K).

Z_{thjc} = IGBT junction-case thermal impedance (K/W).

P_{loss} = Total power lost by the IGBT (W).

The total power losses are the sum of the above four loss types. Each of these four power losses can be calculated as average, maximum or instantaneous losses, giving rise to average, maximum or instantaneous junction temperature. As mentioned previously, it is the maximum junction temperature, ΔT_{jcmax}, that is most significant in power cycling studies. ΔT_{jcmin} is the same as T_{case} if sufficient time is given for the IGBT to cool off during the off-cycle. The variation in ΔT_{jc} is then given by the difference between ΔT_{jcmax} and ΔT_{jcmin}.

The thermal impedance of an IGBT is usually given in manufacturers' data sheets as a function of pulse duration and duty cycle. A typical format is shown in Figure 2.5. The steady-state value of Z_{thjc} is termed Z_{thjcss} or R_{thjc}.

Any free-wheeling diodes included in the module also have conduction, switching and off-state losses and hence they also exhibit similar junction temperature properties as the IGBT. They are also, therefore, exposed to power cycling stresses. This is discussed in Section 2.2.

2.1.3 NPT and PT structures

There are two types of IGBT structures used today: "non punch through" (NPT) and "punch through" (PT). The structure of two typical examples is shown in Figure 2.6.

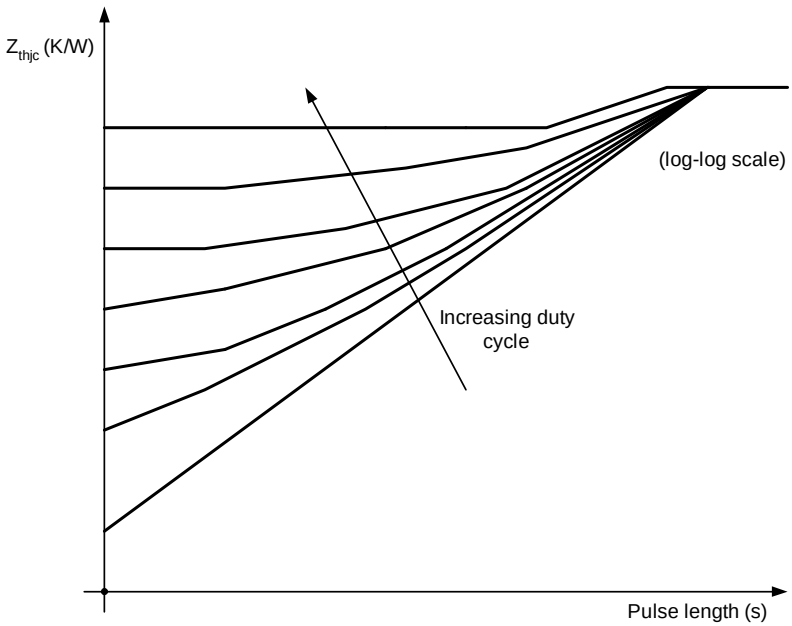
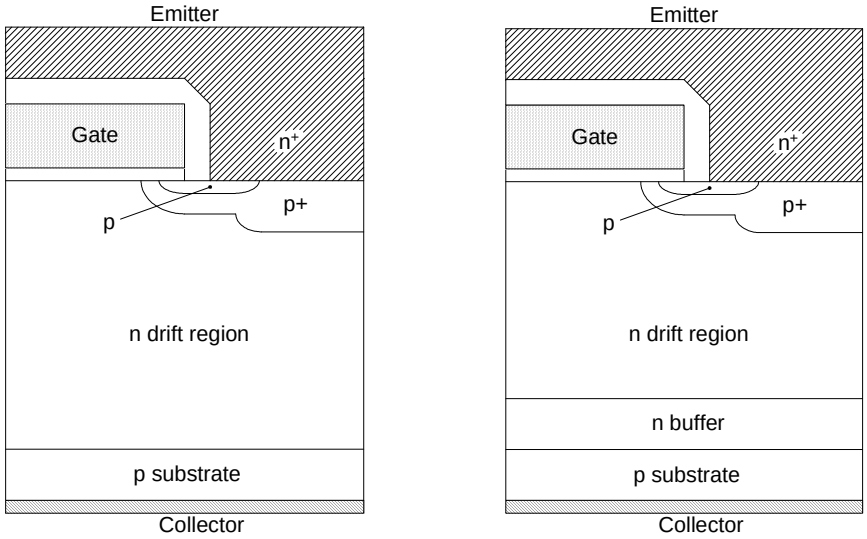


Figure 2.5 Typical IGBT thermal impedance curves



a) *b)*

Figure 2.6 Structure of two typical IGBTs: a) 1200 V, 100 A non punch through IGBT; b) 1200 V, 50 A punch through IGBT [11]

The IGBT used in this study is the SKM 100 GB 123 D, manufactured by Semikron [12]. The module contains one leg of an inverter, i.e. it has two series IGBTs, each with a free-wheeling diode, as shown in Figure 2.7. A photograph of the module is also shown. The manufacturer's data sheet is shown in Appendix A.

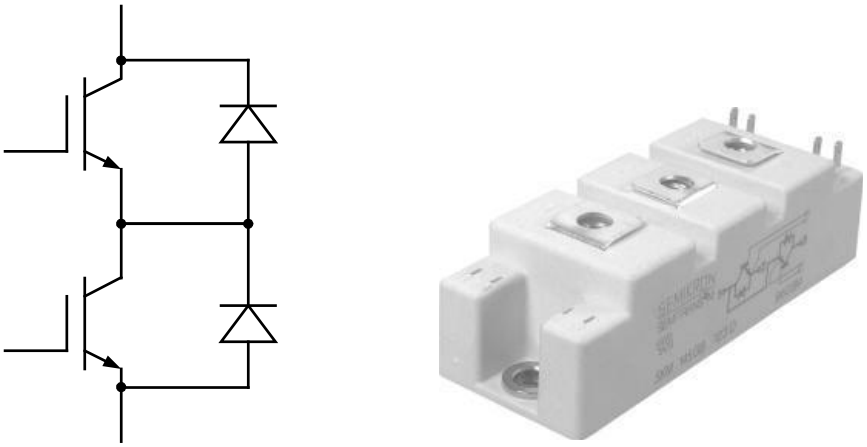


Figure 2.7 Schematic and photograph of the SKM 100 GB 123 D module

The SKM 100 GB 123 D IGBT has a similar structure to the original IGT. This is an example of an NPT type IGBT. The advantages of NPT IGBTs are higher blocking voltage capability ($V_{CE(max)}$), greater immunity to latch-up during short-circuit switch-off, a rectangular safe operating area (SOA), greater short-circuit capability [13] and a positive temperature coefficient $V_{CE(sat)}$ [10]. NPT IGBTs also have better short-circuit withstand capability and are generally influenced less by self-heating effects [11], [14]. It is also easier to parallel NPT devices (due to the positive temperature coefficient of $V_{CE(sat)}$ and they are cheaper to manufacture [7].

However, NPT devices have higher $V_{CE(sat)}$ values and hence higher conduction losses, as well as higher turn-on losses, but have lower overall switching losses, making them better suited to high switching frequencies [15]. Another disadvantage of NPT IGBTs is the high off-state loss at high switching frequency [16].

The main advantage of PT IGBTs is lower conduction loss, making them better suited for high current applications [15]. The disadvantages of PT IGBTs are a non-rectangular SOA (so that rated V_{CE} cannot be applied at rated I_C), relatively high and temperature-dependent tail current during switch-off, leading to higher turn-off losses and higher total switching losses, as well as a negative temperature

coefficient of $V_{CE(sat)}$ [10]. However, the negative temperature coefficient only occurs at higher currents [11]. PT devices are also generally more temperature-dependent [15].

NPT devices are the more popular of the two in industry [7].

2.1.4 Gate drivers

A gate driver circuit is generally placed between the IGBTs and the control circuit. The function of the gate driver is to isolate the low voltage control circuitry from the power circuit. The gate driver circuit also usually converts between 0-5 V digital or 0-15 V TTL control voltage levels and the +/- 15 V required by IGBTs. Short circuit protection in the form of V_{CE} monitoring is also usually provided. The gate drivers require a separate low voltage power supply.

2.1.5 Ratings

There are several different properties that determine which IGBT is chosen for a particular application. The most important are:

1. Collector-emitter voltage (V_{CE}) rating. This is usually chosen to be at least twice the expected continuous service voltage.
2. Collector (load) current rating, I_C. This is usually chosen to be at least twice the expected peak instantaneous service load current.
3. The characteristics of the free-wheeling diodes. These are usually specially designed for use with IGBTs (refer to Section 2.2 for further details).
4. Conduction and switching losses. For low switching frequencies a device with lower conduction losses is preferable, while for high switching frequencies one with lower switching losses should be used.
5. Thermal impedance, Z_{thjc}. For applications where high losses are expected, a lower Z_{thjc} will give lower junction temperatures, resulting in lower stresses on the IGBTs and less chance of exceeding device ratings.

Table 2.1 and Figure 2.3 show that IGBTs have relatively high voltage ratings when compared to other power switching devices. A survey of commercially available IGBTs yielded the ratings of Tables 2.2 and 2.3. These tables are by no means exhaustive.

The IGBTs in the high voltage range (Table 2.2) are packaged in two different ways: all devices except the Toshiba device are similar to the device used in this study (refer to Figure 1.1 for a schematic and Figure 2.7 for a photograph): a baseplate is provided which is mounted onto a heatsink and the electrical connections are made onto the other side via screw terminals. The Toshiba device is a press-pack type device, which is similar to the conventional arrangement often used for SCRs and diodes. The devices in the ≤1700 V range (Table 2.3) also have two different types of packaging. The discrete devices are similar to the standard voltage regulator (the TO-247 type arrangement), whereas those packages containing one or more inverter leg are similar to the device used in this study.

It is important to note that the devices mentioned above are all commercially available. Other devices with high ratings have been proposed, but are not to the author's knowledge available commercially, such as press-pack designs proposed by Fuji Electric [25, 26]. These papers proposed a device of similar structure to the Toshiba press-pack device. Details of the Toshiba device were first published in 1995 [27] and are commercially available (refer to Table 2.3). The Fuji device is to the author's knowledge not yet commercially available.

IGBT module structure is discussed in more detail in Section 2.3.

Table 2.2 Largest commercially available IGBTs ($V_{CE(max)}$>1700 V)

	Dynex[1]	eupec[2]	ABB[3]	Toshiba[4]
V_{CE} (max)	3300 V	6500 V	3300 V	2500 V
$V_{CE(sat)}$ (typical)	3.0 V	3.8 V	3.1 V	5.5 V
$I_{C(max)}$ (T_{amb} = 25°C)	1200 A (90°C)	1200 A	1200 A	1000 A
Z_{thjcss} (typical)	0.008 °C /W	0.011 °C /W	0.009 °C /W	0.018 °C /W

[1] Part number: DIM1200ESM33-F000 [17]. It is a 3-leg inverter module (3 phase inverter without DC chopper but with free-wheeling diodes), similar in physical structure to the Semikron SKM 100 GB 123 D used in this study. Dynex was formerly GEC-Plessey.

[2] Part number: FZ 600 R 65 KF1 [18]. It is a 3-leg inverter module (3 phase inverter without DC chopper but with free-wheeling diodes), similar in physical structure to the Semikron SKM 100 GB 123 D used in this study.

[3] Part number: 5SNA 1200E330100 [19]. It is a 3-leg inverter module (3 phase inverter without DC chopper but with free-wheeling diodes), similar in physical structure to the Semikron SKM 100 GB 123 D used in this study.

[4] Part number: ST1000EX21 [20]. It is a discrete IGBT with free-wheeling diode housed in a press-pack housing (a hockey puck type arrangement similar to that often used for SCRs).

Table 2.3 Largest commercially available IGBTs ($V_{CE(max)}$≤1700 V)

	Semikron[1]	International Rectifier[2]	Fuji[3]	Renesas[4]
V_{CE} (max)	1700 V	1200 V	1700 V	900 V
$V_{CE(sat)}$ (typical)	2.2 V	2.5 V	2.5 V	2.1 V
$I_{C(max)}$ (T_{amb} = 25°C)	2400 A	105 A	600 A	60 A
Z_{thjcss} (typical)	0.013 °C /W	0.20 °C /W	0.06 °C /W	0.69 °C /W

[1] Part number: SkiiP 2403GB172-4DW [21]. It is a 4-leg inverter module (3 phase inverter with DC chopper and free-wheeling diodes). It is heatsink-mounted.

[2] Part number: IRGPS60B120KD [22]. It is a discrete IGBT with free-wheeling diode housed in a TO-247 package.

[3] Part number: 6MBI450U-170 [23]. It is a 3-leg inverter module (3 phase inverter without DC chopper but with free-wheeling diodes), similar in physical structure to the Semikron SKM 100 GB 123 D used in this study.

[4] Part number: CT60AM-18F [24]. It is a discrete IGBT with free-wheeling diode housed in a TO-3PL package. Renesas was formerly the semiconductor division of Mitsubishi Electric.

2.1.6 Protection

Like all power electronic switches, IGBTs usually require some type of protection. The main dangers are overvoltage, high dv/dt and short circuit.

Overvoltages are harmful as the IGBT voltage ratings may be exceeded. This is usually dealt with by choosing a sufficient safety margin between the device rating and the expected peak voltage, or by placing a snubber capacitor across the DC bus directly at the device terminals. In special cases overvoltage protection devices are used for this. The metal oxide varistor (MOV) is the most common device as it is cheap and sufficient for the vast majority of cases. Under special conditions, silicon avalanche diodes (SADs) may be used. These offer better protection in the form of a lower clamping voltage and slower aging, but have lower energy ratings and are more expensive [28].

High dv/dt can cause an IGBT to go into latchup (it switches permanently on and can no longer be switched off by the gate). Placing a series RC snubber across the collector and emitter, as shown in Figure 2.8a, has the effect of slowing down high dv/dt across the IGBT. The use of larger external gate resistance, R_G, as shown in Figure 2.8b, can have a similar effect [29]. Increasing R_G increases the switching times and decreases di/dt during switching and hence reduces voltage transients during switching:

$$V = L_S \cdot di/dt \quad \text{(2.2)}$$

where L_S is stray inductance in the circuit.

However, this also leads to larger switching losses as well as slower turn-off during short circuit conditions and hence greater danger of damage. This resistance is usually included on the gate drive.

Short circuit protection is provided primarily by the gate driver. Its function is to turn off the IGBT when a short circuit is detected. Turn-off must be controlled.

Switching the IGBT off too fast could cause damaging voltages due to high di/dt according to Equation 2.2.

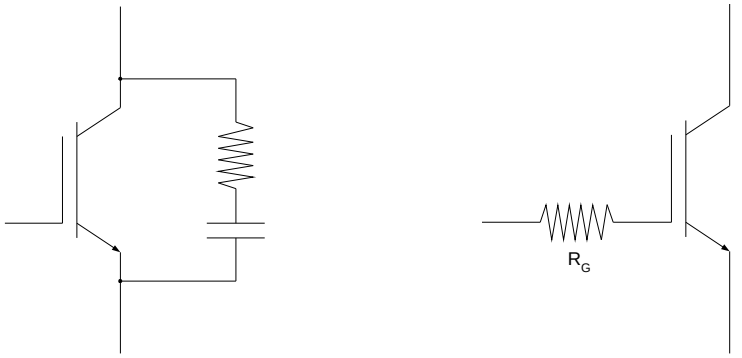


Figure 2.8 Two methods of dv/dt protection of IGBTs: a) Series RC snubber, b) External gate resistance, R_G

2.2 Free-wheeling diodes

The IGBT is a uni-directional device and hence it requires free-wheeling diodes to conduct reverse current for most applications. Therefore, most commercially available IGBTs have free-wheeling diodes built in.

Mounting the diodes in the same package as the IGBTs reduces stray inductance of both the power side of the module (the collector-emitter inductance, L_{CE}) as well as on the control side (the gate inductance, L_G). However, the diodes are generally manufactured as separate chips due to the special characteristics which they need to possess [10, 30].

The IGBT collector current waveform of Figure 2.4 shows a current spike when the IGBT turns on. This is due to the reverse recovery current of the free-wheeling diode [10]. If commercially available discrete diodes were used, this peak reverse recovery current could become as high as twice the diode on-state current [30]. This current needs to be safely conducted by the IGBT, and hence affects the peak current and switching loss rating of the IGBT.

The diodes therefore need to have “soft” recovery characteristics, i.e. the reverse recovery current and the reverse recovery time must be as low as possible, but must not be too “snappy” when they turn off, as this produces large voltage transients. To accomplish this gold, platinum or helium doping or electron radiation may be used [10, 30]. However, this causes an increase in on-state voltage drop and a corresponding increase in conduction losses [30]. A compromise therefore needs to be made.

Diodes in general only have significant turn-off losses, with turn-on losses negligible for most cases. This is reflected in the data sheet of the device used in this study, where only turn-off losses are given for the free-wheeling diodes [12].

In the vast majority of industrial cases, the load of an inverter is inductive, as opposed to capacitive, in nature, i.e. it has a lagging power factor [31]. However, it is hardly ever purely inductive as most loads dissipate power and hence have non-negligible resistance. The usual power factor is in the region of 0.8 or higher [32,33]. In such a case the IGBTs in a conventional single-phase or three-phase inverter conduct a greater portion of the current than the diodes (this is shown in Chapter 6). Therefore, the diodes generally have a slightly lower current rating than the IGBTs. For example, the diodes used in this study are rated at 95 A at 25°C and at 65 A at 80°C, whereas the IGBTs are rated at 100 A and 90 A respectively [12].

The free-wheeling diodes in the SKM 100 GB 123 D use a technology called “Controlled Axial Lifetime” (CAL) to achieve the soft recovery characteristics. This involves, among other processes, the implantation of He++ ions. The manufacturer claims that this technology gives improved soft recovery characteristics, reducing IGBT turn-on losses and thereby increasing the maximum allowed switching frequency, while at the same time maintaining a low diode on-state voltage drop, V_F [10, 12].

2.3 IGBT packaging

Power semiconductor packaging must have five characteristics [34]:

1. There must be electrical isolation between the semiconductor and the heatsink. This is so that all devices in one circuit can be mounted on the same heatsink, as well as for safety purposes.
2. Heat generated by the semiconductor device must be effectively dissipated so that the temperature on the surface of the chips is as low as possible. Therefore, Z_{thjc} should be as low as possible.
3. It must exhibit good electrical performance, e.g. the internal parasitic inductance must be kept to a minimum. This inductance causes increased switching losses, as well as high-frequency ringing. Also, its geometry must be such that a low-inductance bus can be connected to it. Also, capacitive coupling between devices should be minimized as this is a major cause of EMI.
4. It must have high reliability. The main cause of premature failure is due to power cycling, as discussed in this document. The main cause of this failure is the difference in coefficient of thermal expansion (CTE) between the different materials used. Therefore, this difference should be kept as small as possible. Chemical degradation can also shorten module life.
5. It must be cheap and easy to manufacture. Costs include material, machining and labour. Devices that require difficult forming or many parts should be avoided, even if the material costs are relatively low.

The most common IGBT module packaging is the wire-bond structure. This is the technology used in the device used in this study [12]. This type of product was chosen because its structure has the problem of reliability under power cycling conditions. These problems will be discussed in detail in Chapter 3. The wire-bond structure is discussed in Section 2.3.1.

In recent years, pressure-pack devices have become commercially available. The manufacturers of these devices claim improved reliability over wire-bond

packaging. These devices are double-sided and hence offer double-sided cooling. However, to the author's knowledge only two such devices are currently on the market. These structures are discussed in Section 2.3.2.

Finally, in Sections 2.3.3 and 2.3.4 other device structures are discussed. These structures are the TO-247 type arrangement often used for lower-power discrete devices as well as several other high-power designs that have been proposed for IGBTs but are not as yet commercially produced.

2.3.1 Wire-bond structure

A simplified diagram of a typical wire-bond IGBT module was shown in Figure 1.1. A more detailed diagram is shown in Figure 2.9. The mechanical and thermal properties of the different parts of this module are shown in Table 2.4. The housing is made of plastic and the module may be filled with hard epoxy resin and/or silicon gel for humidity protection [3].

Several silicon chips, limited to an area of approximately 4.6 mm^2 in size, are usually used in parallel to achieve the required current rating and are soldered onto the DBC substrate. The DBC is made up of three layers: two copper layers and a central ceramic layer. The ceramic layer provides electrical isolation and good heat transfer characteristics. Of the two materials used for this, AlN has the better thermal conductivity but is more expensive. BeO was used on older modules but is no longer used due to its toxicity [3,7,35].

The bonding wires are ultrasonically soldered onto the chips. Each chip requires 8-12 such wires to connect it. Consequently, there may be as many as 450 bonding wires in a single module. The number of solder joints is twice the number of bonding wires, and may be protected by a polyimide coating. In addition to the chip metallisation, a Mo strain buffer may be added to improve the reliability of the wire-chip bonds. The wires themselves may also be coated [4,5,6,36].

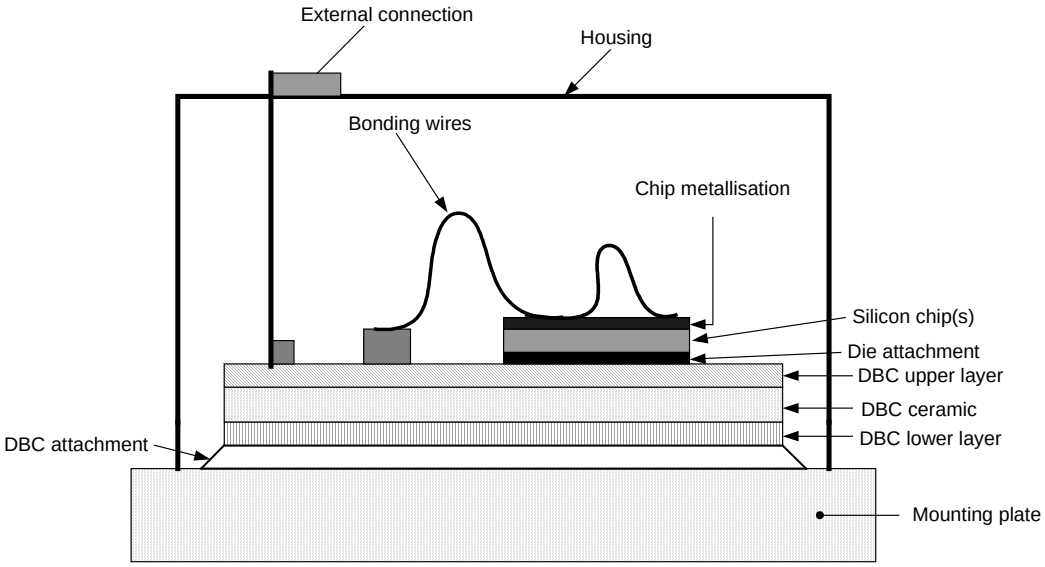


Figure 2.9 Schematic diagram of a typical wire-bond IGBT module [3,6,35]

Table 2.4 Mechanical properties of wire-bond IGBT materials [3]

Layer	Material	Thickness (μm)	CTE (10^{-6}/K)
Bonding wires	Al(1)	300	24
Chip metallisation	Al(2)	3	
Chips	Si	300	3
Die attachment	Solder	50	
DBC upper layer	Cu	600	
DBC ceramic	AlN or Al_2O_3	700	4
			7
DBC lower layer	Cu	300	16.8
DBC attachment	Solder	100	25
Mounting plate	Cu	3000	

(1) The bonding wires are 99.99% or 99.999% Al with the rest taken up by Cu, Ni or Ti.
(2) The chip metallization is made up of 99% Al with the other 1% made up of either Si or Ti.

The use of AlSiC baseplates has also been proposed due to its lower CTE and lower weight [7].

The advantages of wire-bond technology are electrical isolation between the power circuit and the heatsink, simple cooling and relatively low packaging costs [36].

There are several disadvantages of wire-bond technology. Firstly, the lack of reliability due to power cycling has long been a concern (refer to Chapter 3). Secondly, several manufacturing problems have been noted, such as air gaps appearing in the solder layers. Thirdly, IGBT failure modes cannot always be defined. Fourthly, wire-bond modules have been known to fail explosively [35, 36].

2.3.2 Press-pack structure

There are currently two press-pack type IGBT modules on the market, that manufactured by Toshiba mentioned previously (refer to Table 2.2) and one manufactured by ABB. Both devices are single IGBTs with free-wheeling diodes. A third module has been proposed by Fuji, but is not to the author's knowledge commercially available.

2.3.2.1 Toshiba [20,27]

A simplified schematic diagram of the Toshiba device is shown in Figure 2.10 and a cross-section is shown in Figure 2.11.

The chip structure is similar to that used in the wire-bond modules. The package structure is similar to the hockey-puck type structure used for discrete devices with high power ratings such as SCRs, GTOs and diodes. The collector and emitter electrodes are made of copper, with molybdenum pads to compensate for the different thickness of the IGBT and diode chips.

The advantages of the Toshiba press-pack package are that no soldering or bonding wires are required. The manufacturers claim that this improves reliability as these were found to be the most vulnerable parts of the wire-bond package.

Also, the press-pack package prevents module explosion. Another advantage is the compactness of the design, reducing stray inductance and $V_{CE(sat)}$. Also, due to the double-sided cooling, Z_{thjc} is expected to be lower. However, the value of Z_{thjc} given in the manufacturer's data sheet is not significantly lower than that of conventional wire-bond devices (refer to Table 2.3).

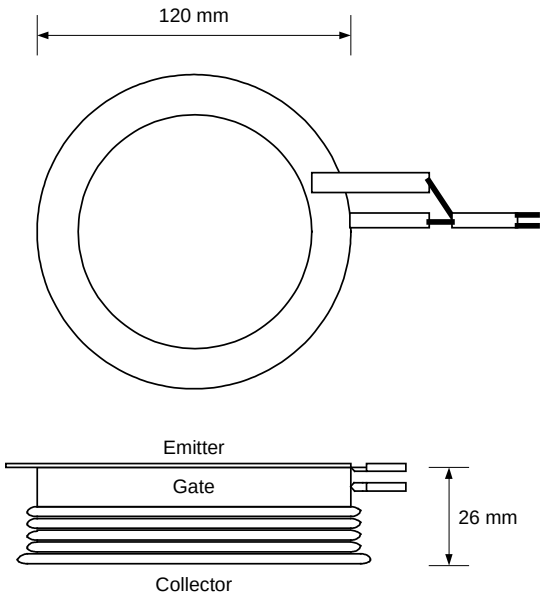


Figure 2.10 Simplified schematic diagram of the Toshiba ST1000EX21 [20]

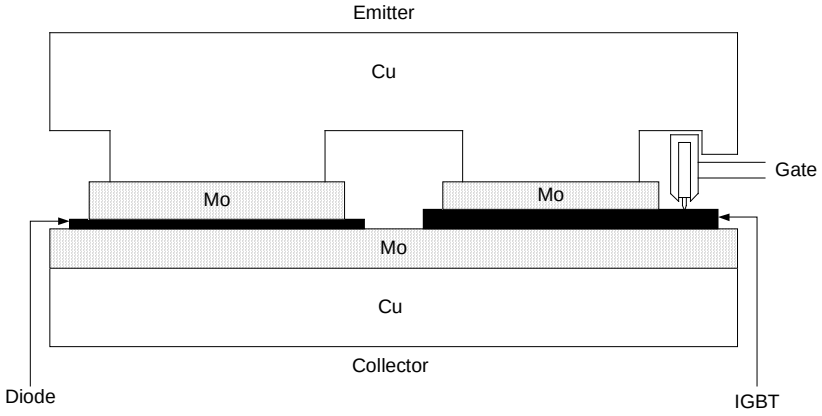


Figure 2.11 Cross-section of the ST1000EX21 [27]

A disadvantage of the Toshiba IGBT, and of all press-pack devices, is the lack of electrical isolation between the chips and the heatsink, which may be a safety

concern. However, this method allows the heatsink to be used as electrical connection, in the same way as for other devices with the same structure. Another disadvantage is that there is only one device per package.

2.3.2.2 ABB [38]

A photograph of the ABB module is shown in Figure 2.12. It has an area of 236 x 150 mm^2 and a height of 26 mm. There is less detailed information available on this device than on the Toshiba and Fuji equivalents. It can be assumed that they have similar characteristics as the packaging appears similar.

This device has a much larger area than the other press-pack devices. This is a disadvantage as more heatsink is required. However, it has the positive effect of a substantially lower Z_{thjc} value.

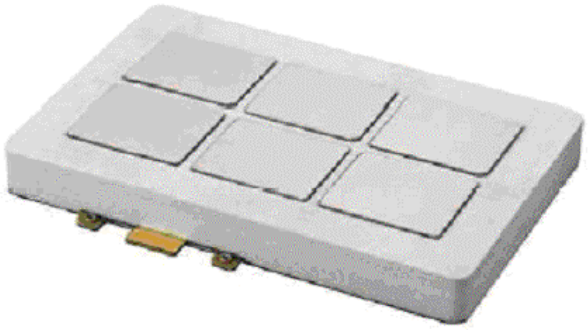


Figure 2.12 The 5SNR 20H2500 manufactured by ABB [38]

2.3.2.3 Fuji [25,26]

The Fuji device is rectangular with a surface area of 133 x 110 mm^2 and a thickness of 20 mm. The chips are all of uniform height and molybdenum is again used for the chip contacts.

An advantage of the Fuji device is its rectangular shape, which the manufacturer claims reduces the amount of unused space. Also, the claimed $V_{CE(sat)}$ is lower than that of the Toshiba device. Another advantage is the “gate source repair

technique" in which the chips are broken up into separate independent IGBT or diode "units", all mounted in parallel. The total current rating is over-rated by 20%, and any "unit" that fails is automatically removed from the circuit and its gate and emitter is short-circuited. This improves module reliability.

The disadvantage of this module seems to be its complexity. Also, as with the Toshiba product, the value of Z_{thjc} is not significantly lower than conventional packages, despite the double-sided cooling.

2.3.3 Other commercially available packages

The only other commercially available package is the standard TO-247 type structure usually used for voltage regulators, transistors and low power SCRs and IGBTs. Sometimes discrete high-power IGBTs also use this package. An example of this is the IRGPS60B120KD manufactured by International Rectifier [22]. Its characteristics are summarized in Table 2.3. Its external dimensions are shown in Figure 2.13.

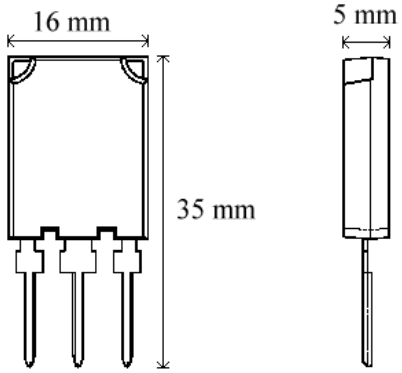


Figure 2.13 Arrangement of a typical TO-247 type IGBT [22]

The advantage of this packaging technology is its small physical size. However, this limits the power rating.

2.3.4 Other proposed packages

Several other packaging technologies have been proposed to overcome some of the problems mentioned above. These new methods have to the author's knowledge not yet been commercially used with IGBTs, even though they may have already been successfully used in other applications. They are included to illustrate the state-of-the-art in IGBT packaging research.

Chip-scale packaging (CSP) has been used successfully for electronic devices. A type of CSP is "die dimensional ball grid array" (D^2BGA), or "flip-chip on flex" (FCOF). It is similar to the wire-bond structure in that the chips are mounted on a DBC substrate, but wire bonds are replaced with large solder balls. Its inventors claim that it offers short connections distances, large contact areas and the potential for double-sided cooling, resulting in relatively low stray effects, lower $V_{CE(sat)}$ and better heat transfer [39, 40].

Another new technology is "Metal-posts interconnected parallel-plate structure" (MPIPPS) [37,41]. Its structure is similar to the D^2BGA design, but the chips are connected by conducting posts instead of solder balls. The advantages of this method are similar to those of the D^2BGA.

A third proposed packaging method replaces the copper base plate with water-cooled microchannel heat sinks. This arrangement is repeated on the wire-bond side of the module to give double-sided cooling. This necessitates replacement of the wire-bonds with the same flip-chip solder bumps described above. This method results in improved heat transfer [42].

2.4 Conclusion

This chapter has shown that the IGBT has several important advantages, most notably low on-state voltage drop, relatively high power ratings and a low power and easily controlled gate. Its characteristics were described, as well as its packaging. The main drawback of IGBTs is the reliability of their packaging.

3. DC POWER CYCLING

It was shown in the previous chapter that the IGBT has many advantages. However, there are several issues that may cause problems with IGBTs in the field. These problems are related to the packaging of the devices. One of the biggest problems is that of reliability of wire-bond modules when subjected to power cycling. This phenomenon has been studied in detail by many authors. The purpose of this chapter is to summarize this work and to highlight the important outcomes.

Power cycling arises from the repetitive cycling of power drawn by a load. This power causes heat dissipation in that load as well as in the power electronics controlling that load. Hence, surrounding areas may also be heated up. If materials with different thermal properties are in close proximity to this heat source and to one another, they will heat up and expand at different rates and to a greater and lesser degree. If the heat source is then removed, the materials will cool down and contract, and this again occurs at different rates and to different extents. Each time these different materials heat up and cool down, mechanical forces will occur between them. If the heat source is applied and removed a large number of times, allowing all of the materials sufficient time to heat up and cool down each time, the repeated forces could cause fatigue of the materials to occur. This in time could result in the materials becoming detached from one another. This phenomenon has been found to occur in wire-bond IGBT modules.

The first section of this chapter explains how power cycling comes about. In the following section the different observed failure mechanisms are presented. The third section gives various test methods that have been proposed and used in the past. As mentioned before, the vast majority of this work has been carried out for the case of the DC load. The reasons for this are given. Because such test methods are subjective in many ways, the failure criteria differ enormously between different researchers. These failure criteria are given in the fourth section and the

test results in the fifth section. In the sixth section the results of FEM simulations are presented. Finally, several practical applications of the different laboratory power cycling tests are summarized. These applications involve the studying of the behaviour of IGBTs in the field.

3.1 Power cycling

Reliability is a major issue in traction applications such as trains, trams, subways and even lifts (elevators) and electric cars. In these applications there is a large amount of traveling and stopping. For example, a tram or a short-distance train travels for only a few minutes between stops. This train or tram must be able to operate for about 30 years in the field. This corresponds to a lifetime of 100 000-135 000 hours and 5 to 10 million travel-stop cycles [3,6,43-46].

During the time the train travels between stops, it draws power from the supply and hence the IGBTs and free-wheeling diodes in the VSDs in the locomotive conduct current and hence their junction temperature rises. When the train stops, the locomotive no longer draws current and hence the devices in the VSDs cool down again, as illustrated previously in Figure 1.2. For a short-distance tram the on- and off-periods (t_{on} and t_{off}[1]) can be as short as 30 seconds each [3,6,44-46].

Power cycling is therefore defined as the variation in ΔT_{jc} of the power devices (IGBTs, diodes and other switching devices) caused by periodic cycling in the power they are required to conduct. The characteristics of the power cycling phenomenon are determined by three broad factors:

1. The characteristics of the load – locomotive motors in the most common case.
2. The characteristics of the power devices – the electrical parameters such as $V_{CE(sat)}$ and losses as well as mechanical properties such as the packaging and Z_{thjc}.

[1] Refer to Figure 1.2 for definition of t_{on} and t_{off}.

3. The characteristics of the route – travel-stop time (the longer the time between stops the fewer cycles there are) and geographic factors such as the presence of steep inclines (the more inclines the more power the load draws and hence the greater the variation in ΔT_{jc} of the devices is). The variation in ΔT_{jc} is claimed to be less than 40°C in most traction cases [2].

There are also other cyclic factors that may affect the reliability of a VSD in traction applications. These are seasonal influences (higher ambient temperatures in summer and lower temperatures in winter) and daily influences (higher ambient temperatures during the day than during the night) [3]. These effects are usually ignored in power cycling studies. Taking all of these factors into account, there is a large range of possible load profiles. A typical profile is shown in Figure 3.1. The figure shows the number of times different variations in ΔT_{jc} may occur in a train VSD on a specific route in the Swiss Alps over a lifetime of 30 years. This profile was determined theoretically and is specific to that route as the three factors listed above will vary from route to route.

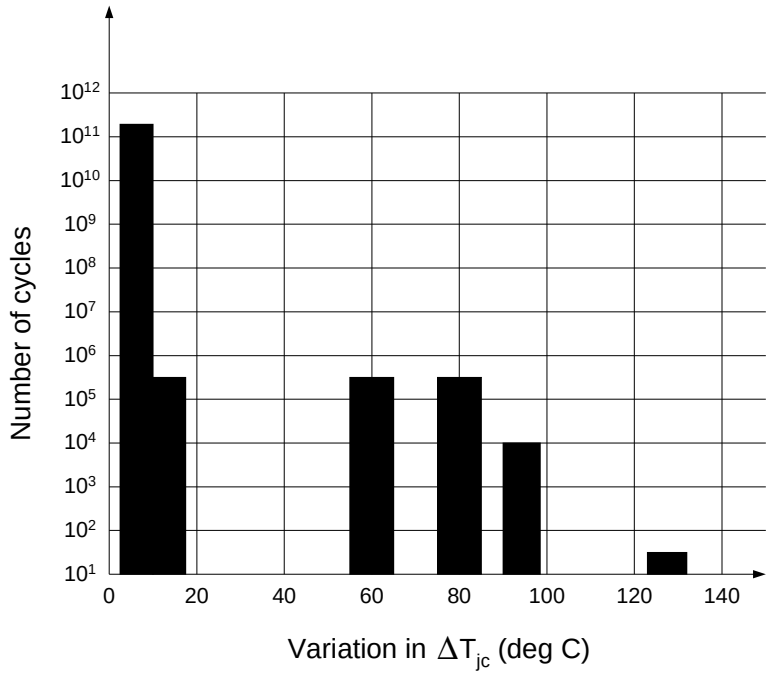


Figure 3.1 Load profile estimated for a route in the Swiss Alps, for 30 years service at 360 days a year and 26 trips a day [47]

An experimentally determined load profile is shown in Figure 3.2. This is for a single journey on a route with ten stops in France. The average variation of four IGBT junction temperature measurements are given. This figure shows that there are many tens of thousand such cycles in a single trip, many orders of magnitude greater than the number of stops. This is due to the many traction-braking cycles, which do not necessarily all occur at stations. However, most of the cycles are below 25 °C. It has been suggested that IGBT modules should be sufficiently reliable for variations in ΔT_{jc} of less than 40 °C [2]. Therefore in the case of Figure 3.2, the modules are expected to perform reliably, but there may be a concern in the case of Figure 3.1.

The above shows that it is impossible to create a single test that is representative of all situations in the field, and so many different accelerated test methods have been proposed and used in the past (discussed in Sections 3.3-3.5), each with its advantages and disadvantages. However, measurement of variations in ΔT_{jc} in service has many merits, despite the obvious difficulties associated with this.

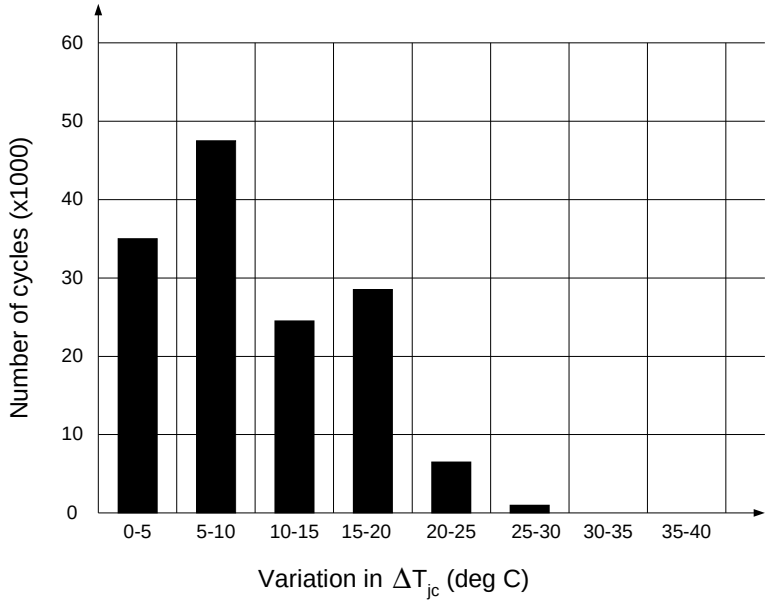


Figure 3.2 Simplified load profile determined in the field for a single journey on the Lille-Valenciennes route in France [48]

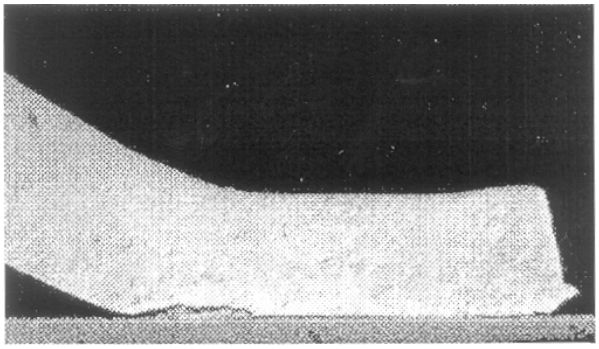
3.2 Observed failure modes

The two most common failure mechanisms that have been observed in wire-bond IGBT modules due to power cycling are disconnection of the aluminium bonding wires from the silicon chips and an increase in module Z_{thjc}. The former was found to be the dominant failure mode above a variation in ΔT_{jc} of about 100 °C and for shorter cycle periods ($t_{on} + t_{off}$), while the latter was found to be dominant below a variation in ΔT_{jc} of about 80 °C and for longer cycle periods [4,43,48,49]. These two and other less common failure mechanisms are presented in this section, as well as a summary of all factors affecting module lifetime.

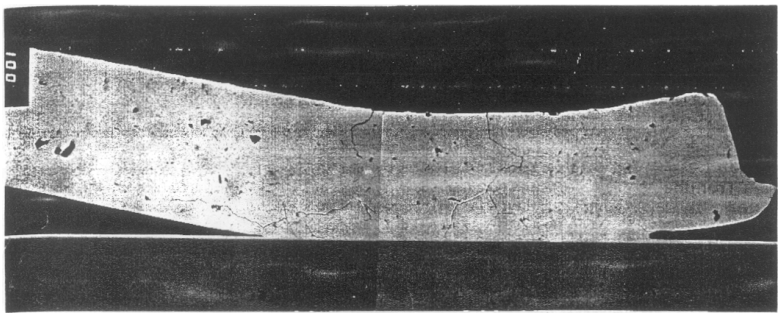
3.2.1 Bond-wire lift-off

The aluminium bond-wires become disconnected from the silicon chips due to the continued cycling of ΔT_{jc}. This is commonly called “bond-wire lift-off” and is often quoted as being the main failure mode. It is caused by the mechanical stresses due to the coefficient of thermal expansion (CTE) mismatch of the two materials concerned (silicon and aluminium) as they are in close proximity to the heat source and are in contact with one another, as described above. Cracks form between coarse and fine Al grains in the bond-wire. These cracks start at the heel and toe of the bond-wire close to the Al-Si boundary. When a crack reaches the centre of the bond, the disconnection process is complete. Fatigue of the Al-Si solder may also occur, also leading to lift-off of the bond-wires [1,3,4,6,36,46]. Typical examples are shown in Figures 3.3 and 3.4.

The process leading to crack formation and propagation in the bonding wires is shown in Figure 3.5. During the heating period (t_{on}) the wire experiences compressive stress at the heel and toe of the Al-Si connection and during the cooling period (t_{off}) it experiences tensile stress in the same regions. This means that crack propagation occurs only during the cooling period. The greater the variation in ΔT_{jc}, the greater the compressive and tensile stress, the faster the cracks propagate and hence the faster the disconnection occurs [2].



a)



b)

Figure 3.3 Examples of cracks in bonding wires due to power cycling:
a) Horizontal crack at the Al-Si interface [3], b) Cracks throughout the bonding wire [50]

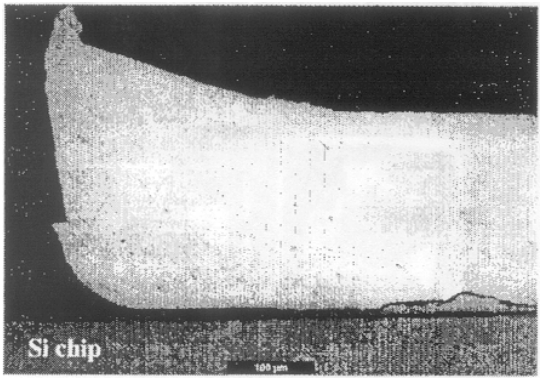


Figure 3.4 Example of complete bond-wire lift-off [36]

Every chip has several bond-wires connected to it (refer to Section 2.3.1). The lift-off of a single such wire starts the “domino effect”: each remaining bond-wire is required to conduct a higher current than before, leading to higher local and average temperatures. This increased stress on the remaining wires causes their aging to be accelerated and causes a second wire to lift-off prematurely, further

increasing the stress on the remaining wires and joints and hence they also age faster and hence they fail sooner than expected [1,3]. If the temperature levels are high enough, the bond wires may become disconnected by melting instead of by crack formation [49].

A related, though less common, failure mode is the extrusion of the aluminium grains in the chip metallization, known as “reconstruction”. This causes an increase in the resistance of the metallization and hence an increase in power dissipation, an increase in temperature, greater stresses on the Al-Si bond and faster time to failure. In severe cases reconstruction can also cause chip disconnection, although the bond-wires are still connected to the chip [3,46,49].

Both bond-wire lift-off and reconstruction cause an increase in $V_{CE(sat)}$ and can hence be detected by monitoring $V_{CE(sat)}$ [3,4,6,36,46,48,51]. Solder degradation leads to a small, gradual increase in $V_{CE(sat)}$, whereas when a bond-wire lifts off the increase in $V_{CE(sat)}$ is almost in the form of a step [1]. This is discussed in more detail in Sections 3.5 and 3.7.

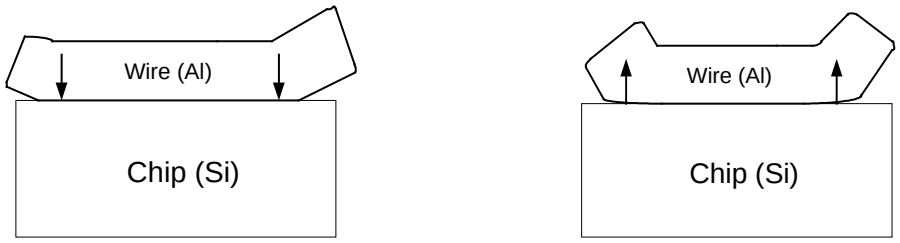


Figure 3.5 Stresses acting on the Al bonding wire at Al-Si interface during power cycling: a) Compressive stress during heating, b) Tensile stress during cooling [2]

3.2.2 Increase in Z_{thjc}

The thermal contact grease between the module and the heatsink has been found to migrate due to power cycling. Also, the solder contact between the DBC

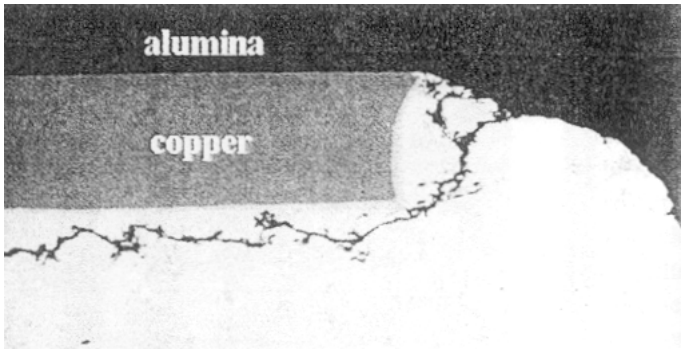
substrate and the copper baseplate can age, with voids and cracks forming. In extreme cases the chips or the base plate may even crack. Both of these factors cause uneven thermal contacts with the cooling system, hence leading to an increase in Z_{thjc}. However, some solder problems may be the result of poor manufacturing [1,5,6,43,46,49]. Cracked solder joints are shown in Figure 3.6. The increase in Z_{thjc} is a strong function of the length of the cracks. Z_{thjc} does not increase significantly until the cracks are of a certain length. This occurs at about 5 mm [43].

To detect this failure method, Z_{thjc} must be measured. Rewriting Equation 2.1 gives Equation 3.1. This shows that in order to determine Z_{thjc}, T_{case} and T_j must be measured. There are several methods of accomplishing these measurements: Infra-Red (IR) methods, thermocouples, optical fibres and indirect methods.

$$Z_{thjc} = \frac{T_j - T_{case}}{P_{loss}} \quad \text{……..…….. (3.1)}$$



a)



b)

Figure 3.6 Two examples of cracked baseplate solder joints caused by power cycling: a) From Morozumi et al. [4], b) From Thébaud et al [52]

IR methods are useful because they are fast and do not require contact with the surface being investigated. However, they are intrusive as the module needs to be opened and this may affect the aging processes as the environment of the chips is altered [44].

Thermocouples require surface contact, but can be as small as 0.25 mm in diameter. They have a response time of about 10 ms, but bad thermal contacts can significantly affect their performance. Despite this, thermocouples are the most popular of the direct techniques [44].

Optical fibres with phosphor sensors have response times of down to 25 ms and can take measurements through the silicon gel, leaving the chip environment virtually unaltered [44,46,48].

Using the indirect method T_j is calculated from a temperature sensitive electrical parameter (TSEP). The method is based on the fact that $V_{CE(sat)}$ is a function of T_j. It involves measurement of $V_{CE(sat)}$ at a small collector current (<1 A for 400 A modules) to avoid self-heating effects. This measured $V_{CE(sat)}$ is then compared to an initially obtained curve of $V_{CE(sat)}$ as a function of T_j at the same small collector current. The relationship between T_j and $V_{CE(sat)}$ is usually linear [3,6,44].

The measurement of Z_{thjc} is usually achieved by measuring its steady-state value (Z_{thjcss} or R_{thjc}).

3.2.3 Other failure modes

Other less common failure mechanisms have also been recorded. One such mode is similar to bond-wire lift-off, but where the cracks in the alumimium were found at some distance from the interface with the silicon. However, the end result was the same as wires became disconnected and the remaining wires and their bonds became more and more stressed. This can also be detected by an increase in $V_{CE(sat)}$ [2,5].

Another uncommon failure mechanism is the failure of an internal copper paralleling connection, which is sometimes used. This is detected by a much sharper increase in $V_{CE(sat)}$ than is observed for bond-wire lift-off [6].

A high gate leakage current has also been reported and is probably caused by failure of the gate oxide insulation layer [6, 46].

3.2.4 Factors affecting module lifetime

The following factors were found to affect IGBT module lifetime when subjected to power cycling [1,4,6,43,49,53]:

- The variation in ΔT_{jc}
- $\Delta T_{jc(max)}$
- Bond-wire diameter and current density
- Composition of the Al-Si and substrate-baseplate solders
- Al-Si bonding area
- Uniformity of substrate-baseplate solder layer
- Quality of the manufacturing process

3.3 Test methods

As mentioned previously, due to the almost infinite number of possible permutations in the field, many different test methods have been proposed and used in the past. Each has served to add to the understanding of the mechanisms involved. The vast majority of these tests have been DC in nature, i.e. during the conduction cycle (t_{on}) the load current is a constant DC value (refer to Figure 1.2) instead of a sinusoidally varying AC wave. The reasons for this are not given in the literature. However, the following reasons are presumed:

1. DC loads are easier to reproduce in the laboratory, as the device under test (DUT) only needs to be switched onto a resistive load during t_{on} and switched off again during t_{off}.

2. High values of variation in ΔT_{jc} can be achieved.

However, the following are disadvantages of this method:

1. The on-state current levels used to achieve the high values of variation in ΔT_{jc} are often unrealistically high when compared to the stresses the devices are typically subjected to in the field. For example, if a device conducts rated current its junction temperature will be high, but in the field the device will conduct much lower currents.
2. Switching losses are ignored.
3. Any effects due to a sinusoidally varying current are excluded.
4. Operating costs are high due to the large power dissipated in the load.

There are two main types of test: *thermal cycling* and *power cycling.* In the former the DUT is un-powered and is heated and cooled by an external heat source, e.g. an oven, to produce the variation in ΔT_{jc}. In the latter the variation in ΔT_{jc} is achieved by periodically loading the module so that the IGBT itself produces the heat [3].

Thermal cycling tests attempt to mimic the real world in a simplified manner. During such a test the entire assembly heats up and cools down together; this means that the mismatch in thermal properties between the different materials is the only aging factor. In addition to this, power cycling also causes a temperature gradient between different materials, producing effects not reproducible by thermal cycling [54]. Power cycling is therefore more representative of real world conditions. However, thermal cycling tests have the advantage that several devices can easily be tested at the same time. Thermal cycling tests are described in Section 3.3.1 and power cycling tests in the following section. The international standard method is also given.

3.3.1 Thermal cycling tests

Because thermal cycling tests are not as realistic as power cycling tests, only a few have been proposed. Two such tests are discussed here.

3.3.1.1 Liu et al [40]

IGBT modules were cycled between 0°C (ΔT_{jcmin}) and 100°C (ΔT_{jcmax}). The period for each cycle ($t_{on} + t_{off}$) was 30 minutes. After every 200 cycles the IGBTs were electrically tested to determine $V_{CE(sat)}$.

A few comments can be made about this test method:

1. The minimum temperature of 0°C is not representative of the field as heatsinks are usually operated at higher temperatures.
2. The cycling time is very long and hence it is expected that the dominant failure mode would be by an increase in Z_{thjc} (refer to Section 3.2). Complete test results were not supplied, so this cannot be confirmed.
3. Only $V_{CE(sat)}$ was measured and not Z_{thjc}.
4. The long cycle time means that the test takes long to complete.

3.3.1.2 Wu et al [49]

A thermal cycle chamber was used to cycle the DUT between 20°C and 150°C, each temperature being maintained for 15 minutes, with a 12 minute transition time. It can be expected that this test would take long to complete. However, with the particular devices tested, only 500 to 1000 cycles were required for clear voids and cracks in the solder layers to be formed. These effects were detected by opening the IGBT modules, and preparing cross-sectional samples containing the Si chips by cutting the module into four parts by using a diamond saw. No electrical parameters were measured in this test.

3.3.2 Power cycling tests

3.3.2.1 Held et al [3]

This test is representative of the most common test that has been used in the past. The test circuit of Figure 3.7 was used.

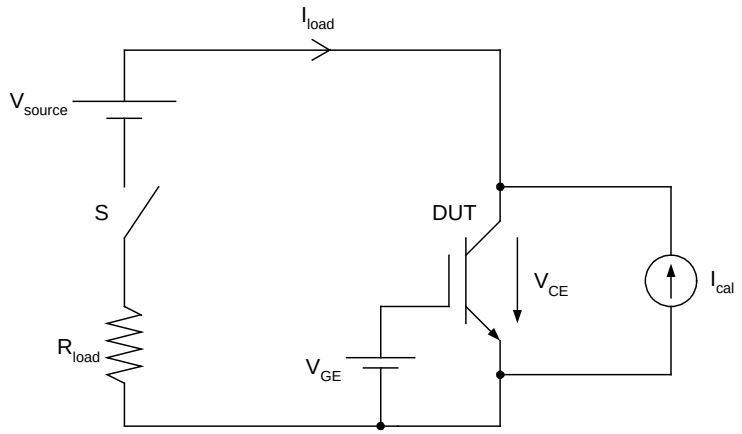


Figure 3.7 Typical power cycling test circuit [3]

The DUT was mounted on a heatsink, which was water-cooled so that the DUT cooled down faster during t_{off}, allowing for shorter cycle times and hence a faster total duration of the test. The water-cooled heatsink also minimized the variation in the ambient temperature (T_{amb}) and T_{case}. A periodic load current, I_{load}, was applied by switching a resistive load in and out of the circuit. When the switch, S, of Figure 3.7 was closed the DUT conducted a certain load current, I_{on}, and when it was open the DUT conducted an off-state current, I_{off}. The DUT was held permanently on by the application of a positive voltage gate-emitter voltage, V_{GE}.

ΔT_{jc} was determined by the indirect method (refer to Section 3.2.2). The main test parameters were $\Delta T_{jc(max)}$ and $\Delta T_{jc(min)}$. These values were set by adjusting the values of I_{on}, I_{off}, t_{on} and t_{off} – these were set before the test and were not further controlled during the test. $V_{CE(sat)}$ was measured during the test. ΔT_{jc} was also measured during the test by applying a small load current, I_{cal}, to the DUT during t_{off}. This current was 100 mA, much smaller than I_{on}, and was applied by a separate source to that supplying I_{load}. I_{off} was therefore not zero, but was small

enough so as not to cause significant heating in the DUT. $V_{CE(sat)}$ was measured for this small current and ΔT_{jc} was determined from this measurement. $V_{CE(sat)}$ was therefore the temperature sensitive electrical parameter (TSEP) in this case.

The test was carried out using ambient temperatures, T_{amb}, of 60°C, 80°C and 100°C and a variation in ΔT_{jc} of between 30°C and 80°C. I_{on} was set at between 240 A and 300 A for a 300 A device (80% to 100% of rated current). The cycling period was short: t_{on} varied from 0.6 s to 4.8 s and t_{off} from 0.4 to 5 s. It is therefore expected that the Al-Si bonds would be stressed the greatest. V_{GE} was permanently set at 15 V to allow equal current distribution through all parallel chips in the DUT. It is clear that the test was performed several times so that the effect of the entire range of parameters listed above could be studied.

3.3.2.2 Hamidi et al [36]

This test is similar to the previous test. I_{on} was set at 249 A and I_{off} at 0 A, and a water-cooled heatsink was once again used, for the same reasons as above. The cycle time was also very short: t_{on} was 0.9 s and t_{off} was 1.3 s. The variation in ΔT_{jc} was set at 60°C and $\Delta T_{jc(max)}$ varied between 105°C and 115°C. The authors were specifically attempting to stress only the Al-Si interface and not the baseplate assembly. Despite this, a swing in T_{case} of 16°C was measured with $T_{case(max)}$ varying from 65°C to 75°C. The following quantities were measured during the test: T_{case}, cooling water temperature, $V_{CE(sat)}$, I_{load}, chip temperature at the centre of each chip. Z_{thjc} was calculated using these measurements.

3.3.2.3 Morozumi et al [4]

A longer cycle period was used: t_{on} was 2 s and t_{off} was 18 s. Once again, $\Delta T_{jc(max)}$ and $\Delta T_{jc(min)}$ were set, by adjusting I_{load} and the supply voltage, to give ΔT_{jc} values ranging from 55°C to 125°C. The DUT was rated at 75 A and 1200 V. ΔT_{jc} was measured using the IR method and Z_{thjc}, $V_{CE(sat)}$ and I_{load} were monitored throughout the test.

3.3.2.4 Coquery et al [6,44]

An in-depth study was undertaken of 36 different 1200 V/400 A IGBT modules using four different technologies. The test method employed was similar to those discussed above, with just the individual parameters varying. The cycle period was longer still than the previous test: t_{on} was 20 s and t_{off} was 40 s. Water-cooling was again used, but only during the second half of t_{off}, i.e. for 20 s. The same indirect ΔT_{jc} measurement method as Section 3.3.2.1 was used. The accuracy of this method was verified by an IR camera and a contact sensor. Two different variations in ΔT_{jc} were used: 55°C and 90°C. Also, two different values of I_{on} were used: 55% and 99% of $I_{C(max)}$. The following parameters were monitored throughout the test: I_{load}, $V_{CE(sat)}$, ΔT_{jc}, T_{case}, V_{GE}, I_G and water flow rate and temperature.

3.3.2.5 Hamidi, Coquery, Lallemand [46]

This test method is similar to that described in the previous section. Devices with two different ratings were tested: 1200 V/400 A and 1600 V/1200 A. The same test parameters were used and the same measurements were made during the test.

A second faster test was also proposed. The cycle time was 10 s ($t_{on} = t_{off} = 5$ s), I_{on} was 95% of $I_{C(max)}$, $\Delta T_{jc(max)}$ was 100°C and $\Delta T_{jc(min)}$ was 43°C.

3.3.2.6 De Lambilly et al [1]

The test is similar to previous tests in that the test parameters were set in order to cycle the DUT between two preset temperatures. However, in this case it was $T_{case(max)}$ and $T_{case(min)}$ that were used, and $\Delta T_{jc(max)}$ and $\Delta T_{jc(min)}$. This cycling was attained in the same way as before: the flow of I_{on} to cause the heating and the flow of I_{off} (0 A in this case) to cool it down again. The cycle time was not predetermined, but was governed by the DUT itself: t_{on} for each cycle was set by the time it took T_{case} to reach the preset maximum, and t_{off} by the time it took T_{case}

to decrease to the preset minimum. Fans were used during t_{off} to aid in the cooling process. The value of I_{on} was preset at 66% of the DUT rating.

The following parameters were monitored during the test: $V_{CE(sat)}$, I_{load}, ΔT_{jc}, t_{on} and t_{off}. ΔT_{jc} and T_{case} were measured directly using thermocouples. The cycle times, t_{on} and t_{off}, were at least 30 s each. This and the fact that T_{case}, rather than ΔT_{jc}, was the controlled temperature means that all solder layers in the DUT would be stressed.

The IGBT modules tested had $V_{CE(max)}$ ratings of 1000-1200 V and $I_{C(max)}$ ratings of 200-400 A, and came from a number of different manufacturers.

3.3.2.7 Wu et al [49]

Over 40 different devices, rated at 1200 V and 300-400 A and from different manufacturers, were tested. IGBTs and free-wheeling diodes were tested separately using a test circuit similar to that of Figure 3.7. The DUT was mounted on a heatsink which was continuously water-cooled, not intermittently as in the previous cases. I_{on} was set at 85% of $I_{C(max)}$ of the DUT, while t_{on} was set at 20 s and t_{off} at 30 s. The chip surface temperature of one module was directly measured using a thermocouple. This gave values of 118°C for $\Delta T_{jc(max)}$ and 16°C for $\Delta T_{jc(min)}$. Therefore the variation in ΔT_{jc} was about 100°C. ΔT_{jc} was measured indirectly for the remaining modules and was found to be between 90°C and 115°C. I_{load}, $V_{CE(sat)}$, V_{GE}, I_G and Z_{thjc} were measured during the test.

3.3.2.8 Auerbach et al [51]

The authors of this paper proposed a novel method of testing more than one IGBT simultaneously. The test circuit is shown in Figure 3.8. A constant DC current is applied to a number of IGBTs connected in series. After a predetermined time, that current is removed and is applied to a different set of IGBTs, connected in series in the same way. This means that t_{on} and t_{off} must be the same. ΔT_{jc}, $V_{CE(sat)}$

and Z_{thjc} of each IGBT module are monitored throughout the test. ΔT_{jc} is measured indirectly in the same way as described in Section 3.3.2.1.

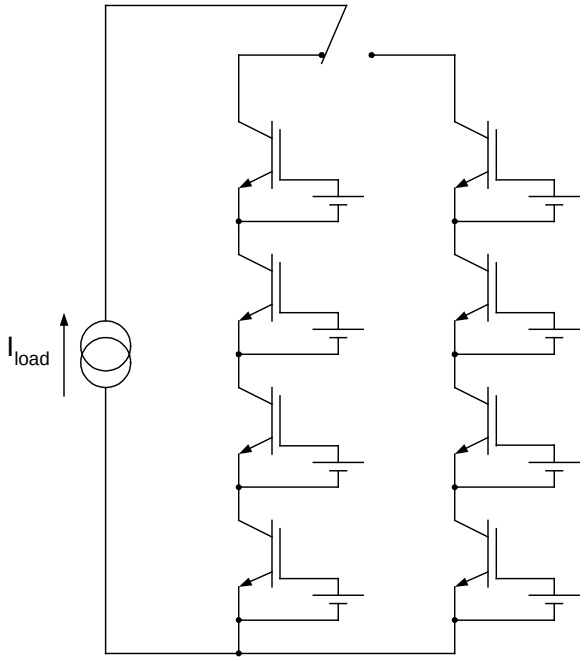


Figure 3.8 Setup for power cycling test of several IGBTs simultaneously [51]

3.3.2.9 Dupont et al [55]

This test method was developed to stress the DBC solder layer. Hence, the main parameter monitored during the test is Z_{thjc}. The solder layer was also acoustically scanned to detect the formation of any voids, which would increase Z_{thjc} and hence reduce the lifetime of the DUT. In order to only stress the DBC solder, a very low value of I_{on} (2 A for a 25 A device) was used. The test circuit is similar to that of Figure 3.8, but with only one device per leg. A cycle period of 20 s (t_{on} = t_{off} = 10 s) was used. The test parameters were chosen to give a total power dissipation of 75 W and 90 W. Baseplate temperature was fixed at a value between 30°C and 100°C and was kept constant to within 3°C. For a baseplate temperature of 90°C T_j rose to a maximum value of 153°C, giving a $\Delta T_{jc(max)}$ of 63°C.

3.3.2.10 Thébaud et al [52]

Again, mainly the baseplate solder layer was stressed. A higher power than previously is dissipated in each pulse (200 W for a 50 A/1200 V device) and the cycle period was 1 minute. Three different variations in ΔT_{jc} were used: $\Delta T_{jc(min)}$ = -55°C and $\Delta T_{jc(max)}$ = +125°C; $\Delta T_{jc(min)}$ = -15°C and $\Delta T_{jc(max)}$ = +125°C; $\Delta T_{jc(min)}$ = +25°C and $\Delta T_{jc(max)}$ = +125°C. These give variations in ΔT_{jc} of 180°C, 140°C and 100°C. These are therefore large temperature variations when compared to several of the test methods mentioned previously. The main criterion was to investigate the change in Z_{thjc} with the number of cycles.

3.3.3 Standard IEC test

A power cycling test is broadly specified in 8.2.6 of IEC 60747-9 (2001) [56]. It is termed the "Intermittent operating life test" and is a power cycling test. A method similar to most of the power cycling tests discussed above is proposed. The test circuit is shown in Figure 3.9. The following conditions must be specified by the tester: I_{on}, I_{off}, t_{on}, t_{off}, T_{case} and the variation in ΔT_{jc}. The gate voltage, V_G, must be kept constant at 15 V (ensuring that the IGBT is fully on) and the cycling is achieved by opening and closing the switch, S. V_G is the only value that is specified.

Two different test methods are specified:

Method 1: T_{case} is kept constant. This method is intended to mainly stress the Al-Si bond-wire connections.

Method 2: T_{case} is allowed to vary with T_j. This method is intended to mainly stress the baseplate soldering.

It can be seen that most of the power cycling tests devised in the past meet the requirements of the IEC test. However, most of these tests did not achieve cycling by turning the DUT on and off, but by switching the load on and off. The difference between the two methods is that there are switching losses included in the DUT during the IEC test. These switching losses would not be present in tests

where the DUT is held permanently on. This is not expected to significantly affect the test results as the additional switching losses would only occur twice during every cycle period: once during turn-on and once during turn-off.

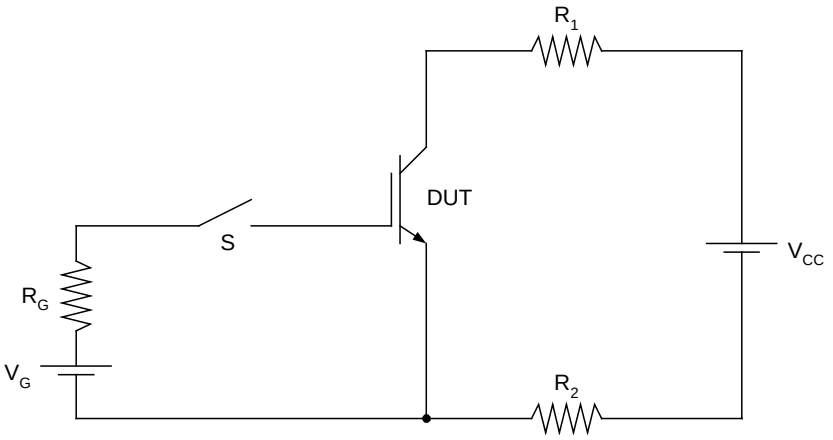


Figure 3.9 Intermittent operating life test circuit [56]

3.4 Failure criteria

The different test methods all specified different DUT parameters that were monitored during the tests. These parameters were monitored to detect any change in them that would indicate aging of the DUT. It is common practice to end the test once a pre-determined change has occurred in one or more of the monitored parameters. Power or thermal cycling tests are usually not run until complete failure.

Several reasons for this are presumed:

1. IGBTs have been known to fail explosively [35, 36]
2. It may require a long time for a module to completely fail
3. The onset of aging would indicate that a device has started to deteriorate, which in most cases is enough to warrant replacement of the device
4. Even relatively small changes in device parameters could cause problems in the field
5. The performance of different packaging technologies can be easily compared

The failure criteria that have been defined are summarized in Table 3.1. Several authors do not mention the failure criteria, and these are therefore not included in the table.

Table 3.1 Power and thermal cycling test failure criteria

Ref.	Failure criteria expressed as a percentage increase in monitored DUT parameters					
	$V_{CE(sat)}$	Z_{thjc}	I_{on}	$V_{GE(th)}$	$I_{G(sat)}$	Other
[3]	5%	-	-	-	-	-
[4]	-	20%	-	-	-	-
[36]	5%	20%	-	-	-	High leakage current, gate-emitter short circuit
[40]	20%	-	-	-	-	-
[48]	5%	20%		-	-	-
[49]	20%	20%	20%	20%	20%	-

3.5 Test results

The test methods and failure criteria have been presented. Now the test results are given. These are grouped as follows. First, the number of power cycles until failure, N_f, is given. This is the final outcome of all power or thermal cycling tests. These results are dependent on the failure criteria chosen and on the accuracy of the measurement of the different parameters in the test circuit that are used to determine whether these failure criteria have been reached. This gives rise to graphs showing the change in a particular parameter with the number of cycles conducted, and hence allowing failure to be detected. The two most commonly measured parameters are $V_{CE(sat)}$, which is an indication of aging of the Al-Si bonds, and Z_{thjc}, which is an indication of the baseplate solder quality. Their change with the number of cycles are given in Sections 3.5.2 and 3.5.3.

3.5.1 Number of cycles to failure (N_f)

The specified result of the IEC method described in Section 3.3.3 is a graph of the form shown in Figure 3.10. This graph shows N_f as a function of the variation in ΔT_{jc}. This is usually in the form of a straight line with a negative slope, as shown,

showing that the greater the variation in ΔT_{jc} per power cycle, the fewer cycles the DUT will survive. However, no failure criteria are specified. It is clear that several devices of the same type must be tested to obtain such a graph. Also, all conditions must be the same for all devices tested, with only the variation in ΔT_{jc} varying between the different tests.

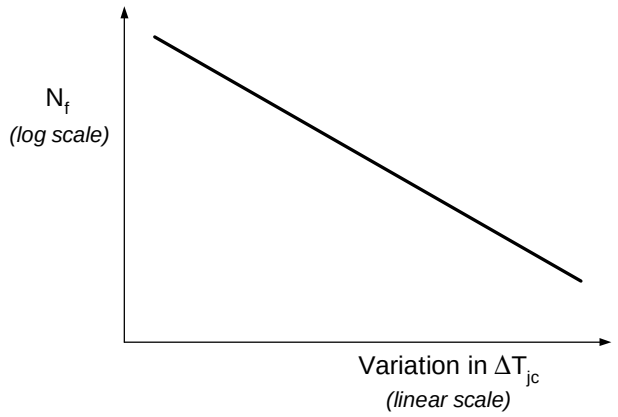


Figure 3.10 Outcome of the test of IEC 60747-9 (2001) [56]

Several authors have obtained such graphs. Two graphs are shown in Figures 3.11 and 3.12. These are some results of the tests described in Sections 3.3.2.1 and 3.3.2.8 respectively.

The following points may be made about the two graphs:

1. The graphs are similar in form to one another and to the specified IEC graph of Figure 3.10.
2. The effect of ambient temperature (T_{amb}) is significant. This reinforces the notion that all ambient conditions must be the same between different tests.
3. Both references used values of T_{amb} of 60°C, 80°C and 100°C. The test results agree very well with one another. This could be because the test methods are similar, despite the different test circuits (the only difference is in the number of devices tested at the same time – the circuit of Section 3.3.2.8 allows more than one device to be tested simultaneously, while that of Section 3.3.2.1 tests only one device at a time). Also, the packaging technologies of the two devices tested are expected to be similar. The

authors of [3] tested a 1200 V/300 A device, while the authors of [51] did not provide the DUT ratings. Also, the failure criteria should be similar. Reference [3] gives a failure criterion of a 5% increase in $V_{CE(sat)}$, while [51] gives no specific failure criterion.

4. The devices failed after 500-700 000 cycles for T_{amb} = 100°C, 1.5 million cycles for T_{amb} = 80°C and 9 million cycles for T_{amb} = 60°C at a variation in ΔT_{jc} of 40°C. This is the threshold variation below which IGBTs are stated to be sufficiently reliable (refer to Section 3.1). These tests show that this is the case if T_{amb} is maintained below about 60°C.

A similar graph is shown in Figure 3.13. A variation in ΔT_{jc} of 40°C gives 3 million cycles before 10% of the modules fail and 10 million cycles before 50% of the modules fail. This shows that the particular modules tested are probably sufficiently reliable. However, the failure criterion used for these tests was not given.

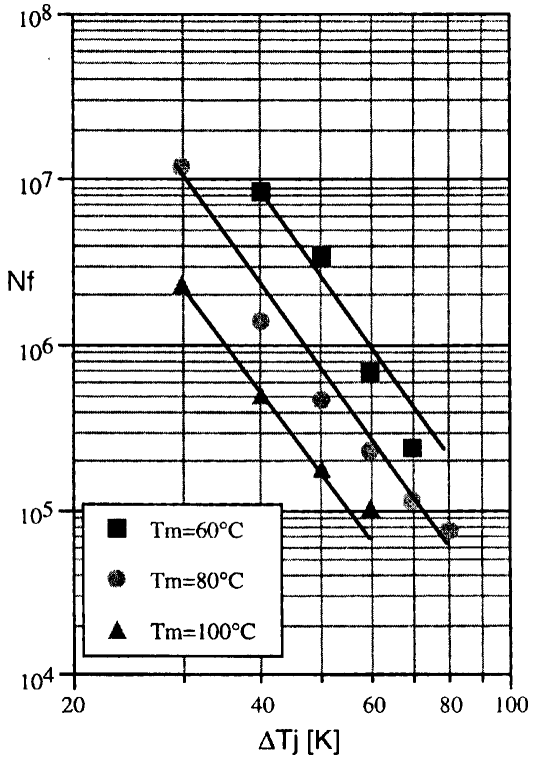


Figure 3.11 Experimentally obtained graphs of N_f as a function of the variation in ΔT_{jc} for three different ambient temperatures (T_{amb} – Tm in this figure) [3]

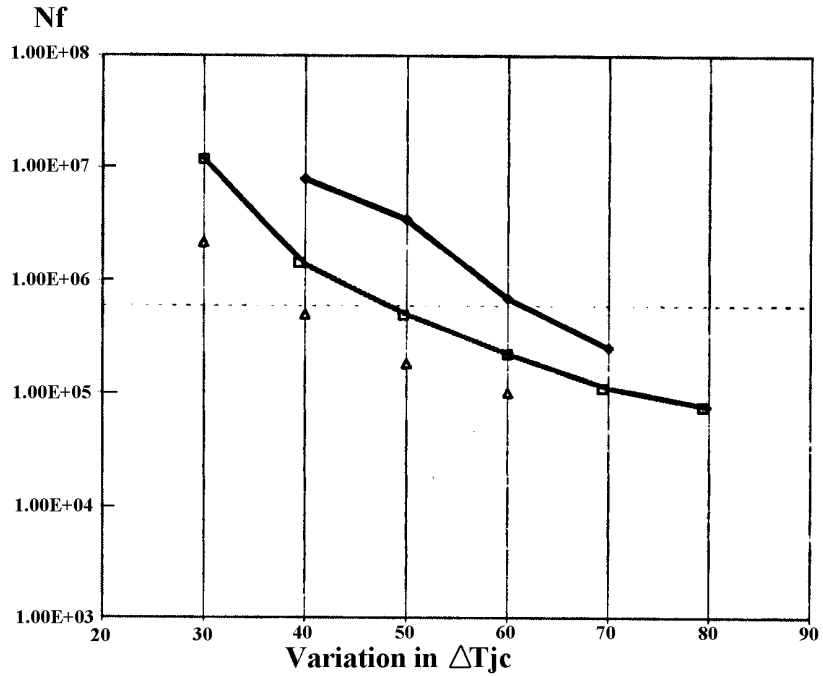


Figure 3.12 Experimentally obtained graphs of N_f as a function of the variation in ΔT_{jc} for T_{amb} of 60°C, 80°C and 100°C (from top to bottom) [51]

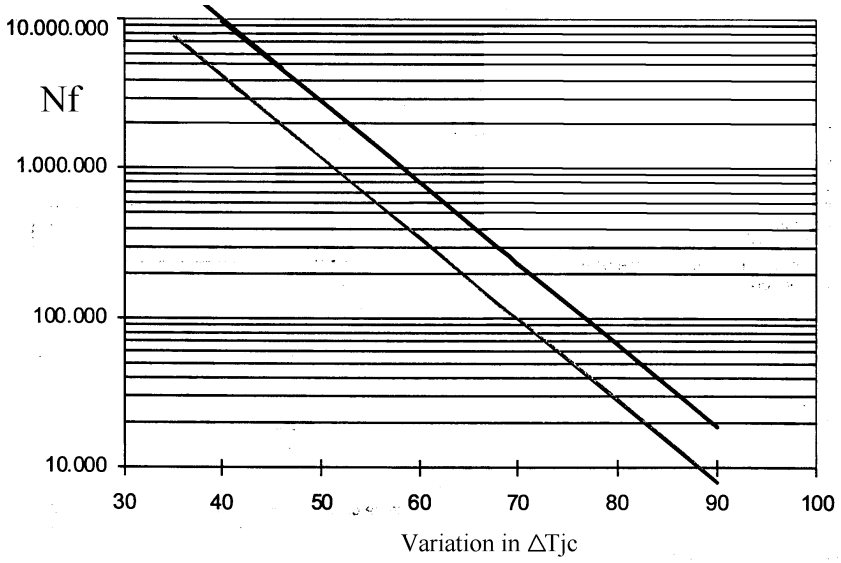


Figure 3.13 Experimentally obtained graphs of N_f as a function of the variation in ΔT_{jc} for a 3300 V/1200 A IGBT. The upper line is for a 50% failure rate and the lower line for a 10% failure rate [50]

Other similar experimentally determined curves of N_f as a function of the variation in ΔT_{jc} are given in [4], [6] and [44].

3.5.2 Change in $V_{CE(sat)}$ with the number of cycles

Typical graphs of the change in $V_{CE(sat)}$ as a function of the number of power cycles are shown for IGBTs in Figures 3.14 to 3.17.

These figures show that $V_{CE(sat)}$ increases with the number of power cycles applied. Increasing $V_{CE(sat)}$ causes increasing conduction losses, in turn causing higher variation in ΔT_{jc}, and hence accelerated failure. Most of the above figures show a gradual increase in $V_{CE(sat)}$. This is due to a gradual degradation of the Al-Si solder connection. Figures 3.16 and 3.17 also show distinct step increases in $V_{CE(sat)}$. These steps sometimes occur when a bonding wire becomes disconnected [57]. The almost vertical increase in $V_{CE(sat)}$ shown on the left of Figure 3.14 occurs when all bonding wires have been completely disconnected.

Other similar graphs of $V_{CE(sat)}$ as a function of number of cycles can be found in [3] and [46].

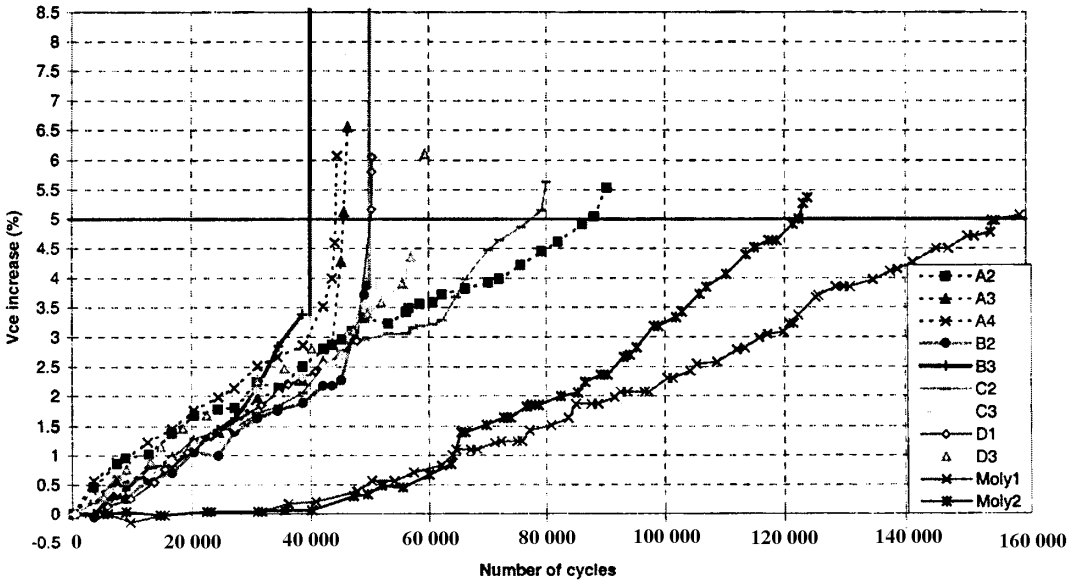


Figure 3.14 Experimentally determined graphs of the percentage increase in $V_{CE(sat)}$ with the number of power cycles for eleven different IGBTs [36]

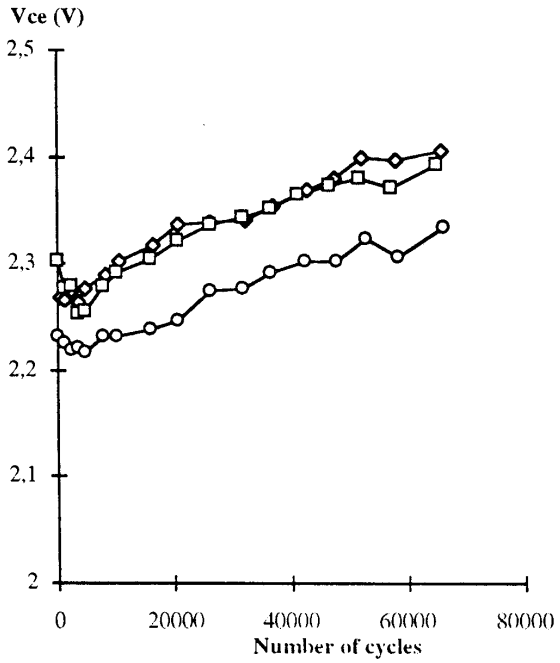


Figure 3.15 Experimentally determined graphs of $V_{CE(sat)}$ as a function of the number of power cycles for three different IGBTs [6]

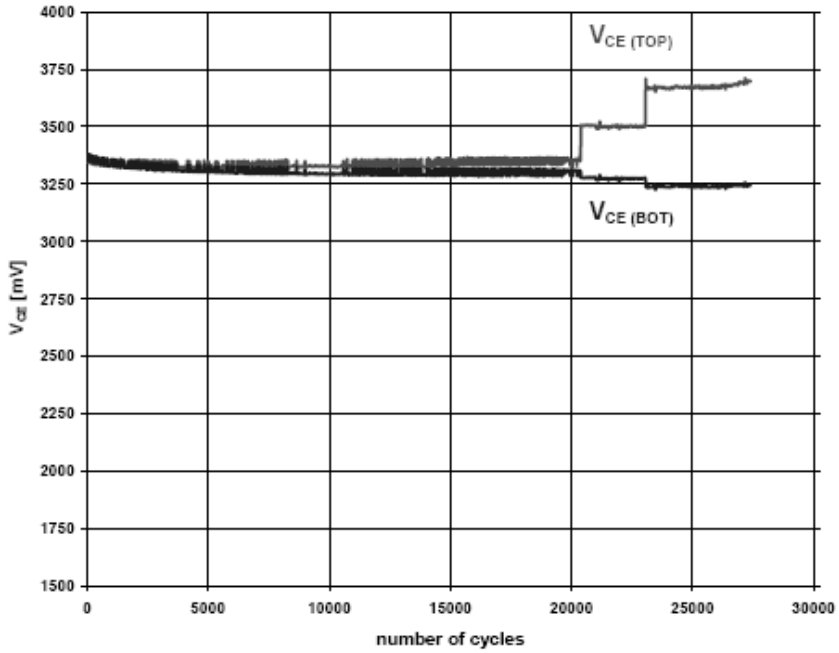


Figure 3.16 Experimentally determined graphs of $V_{CE(sat)}$ as a function of the number of power cycles for an inverter leg [57]

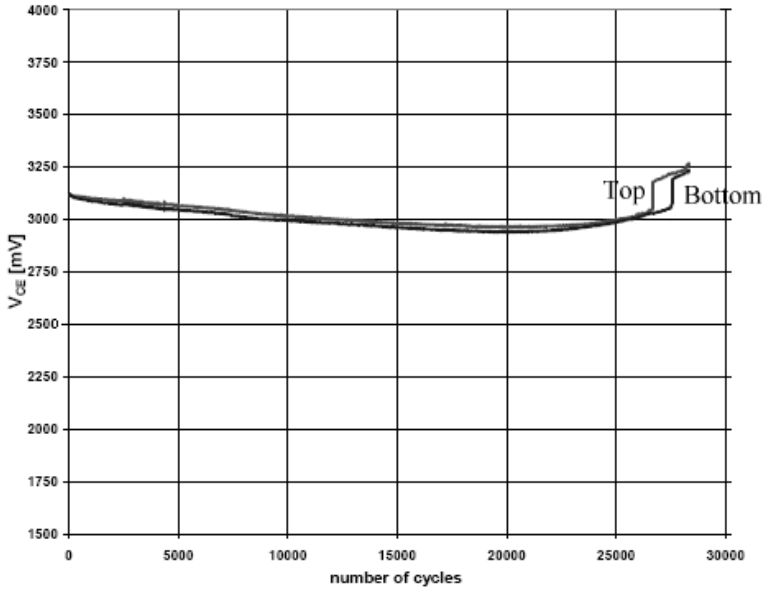


Figure 3.17 Experimentally determined graphs of $V_{CE(sat)}$ as a function of the number of power cycles for an inverter leg [57]

3.5.3 Change in Z_{thjc} with the number of cycles

Z_{thjc} (or usually its steady-state value, R_{thjc}) increases with the number of conducted cycles in a similar way to $V_{CE(sat)}$. Some typical examples of this are shown in Figures 3.18 and 3.19. A case where R_{thjc} does not change with the number of power cycles is shown in Figure 3.20. The latter was obtained using the test method outlined in Section 3.3.2.9. The reason for a negligible increase in R_{thjc} is that the only void that appeared in the baseplate solder layer occurred relatively close to the outside of the module and not directly underneath the chips and may also not have been large enough to significantly increase R_{thjc} (refer to Section 3.2.2). Other similar graphs of R_{thjc} as a function of number of cycles can be found in [4].

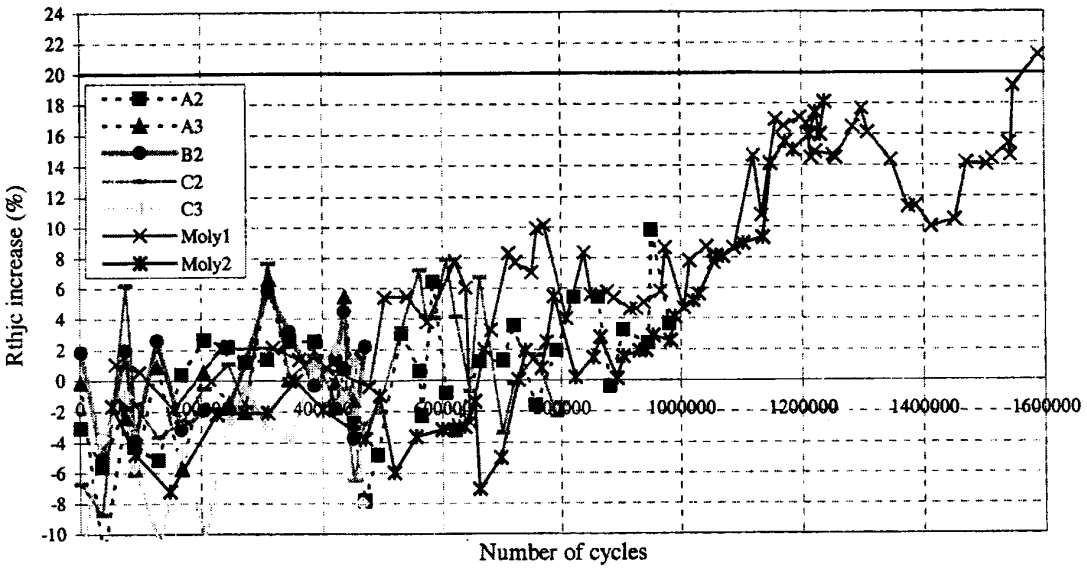


Figure 3.18 Percentage increase in R_{thjc} with the number of power cycles conducted of seven IGBTs [36]

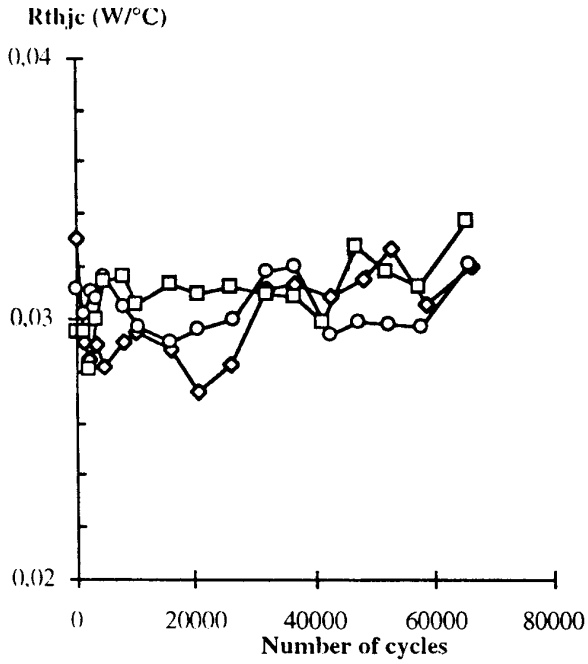


Figure 3.19 Increase in R_{thjc} with the number of power cycles conducted for three different IGBTs [6]

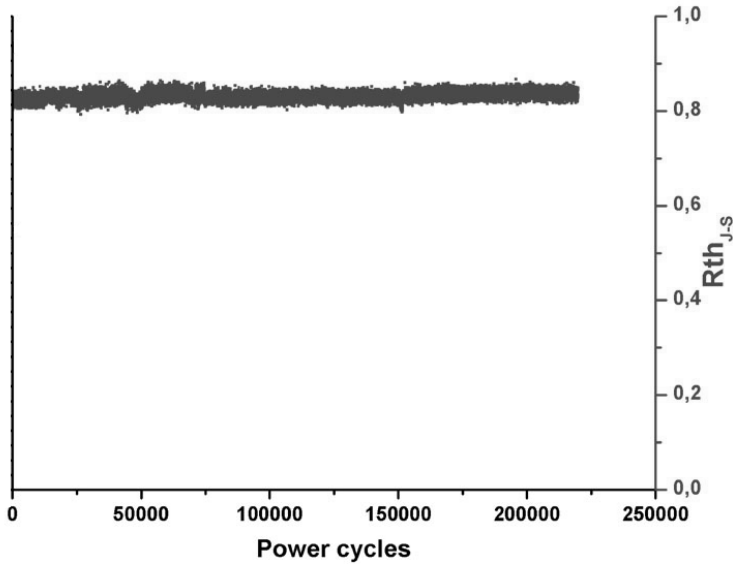


Figure 3.20 A case where the graph of R_{thjc} remains relatively constant with the number of cycles conducted [55]

3.6 Simulations

Several authors have attempted to explain or predict the behaviour of wire-bond IGBTs under power cycling conditions by thermo-mechanical modeling using finite element methods (FEMs). This work is summarized in this section.

3.6.1 Shammas et al [43]

An IGBT module rated at 1800 V/800 A was modeled. To achieve this, the module dimensions, as well as the mechanical and thermal properties of the different materials were required. These properties included thermal conductivity, thermal capacity and density. Only the baseplate solder layer was investigated and its fatigue was modeled by adding a very thin (1 μm thick) air gap to simulate a crack in this solder layer. The IGBT was modeled in its on state by applying a power source corresponding to 100 A of conducted current to the chips. The cycling period was 1 minute (t_{on} = t_{off} = 30 s). Several assumptions were made: only heat conduction was considered, the thermal conductivity was independent of

temperature for all materials except silicon and the temperature on the underside of the baseplate was kept constant at 25°C.

Static and dynamic simulations were performed. The outcome of the static simulations was R_{thjc}, the distribution of temperature and heat flux and the effect of degradation of the baseplate solder layer on the module thermal behaviour. The outcome of the dynamic simulations was the strain per cycle, and from this the expected value of N_f as a function of the variation in ΔT_{jc}. The model was verified experimentally.

The simulation results clearly show the effect of baseplate solder degradation: the difference between R_{thjc} with and without the crack present in the solder is about 16%. The presence of cracks was found to cause hotspots in the chips directly above such cracks. As mentioned previously, this paper also shows that a crack has little effect on IGBT thermal performance until it reaches a length of about 5 mm. This is illustrated in Figure 3.21.

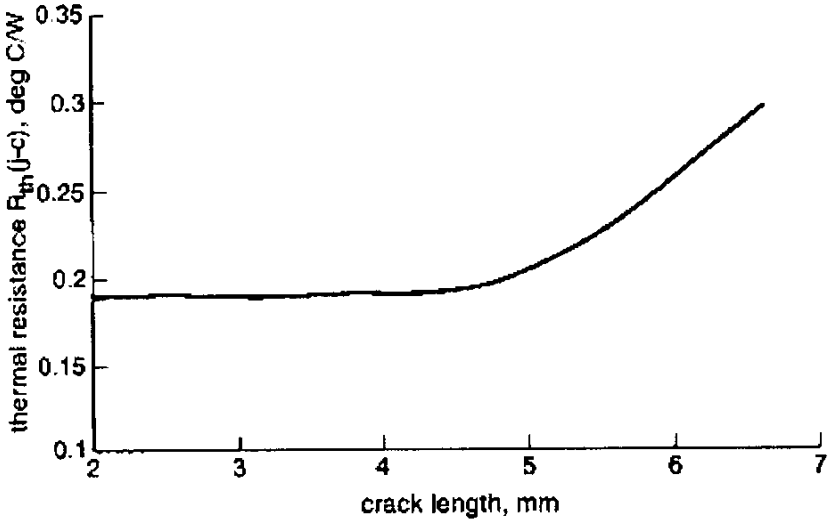


Figure 3.21 Simulation output showing the effect of baseplate solder crack length on R_{thjc} of an 1800 V/800 A IGBT module [43]

3.6.2 Hamidi et al [45]

Another set of experimentally verified simulations was carried out. The purpose was to determine the temperature distribution inside an IGBT module as it is very difficult to measure temperature inside such a module in the field. A 3300 V/ 1200 A device was modeled. As before, the dimensions and thermo-mechanical properties of all materials were entered into the model. Also, the required power was dissipated from the chips and the temperature on the underside of the module was kept constant at 38.5°C throughout. Two outputs of the simulations are shown in Figure 3.22.

Figure 3.22 raises two points. Firstly, the simulations are acceptably accurate. Second, there is a large temperature distribution over a typical IGBT chip. The junction temperature, T_j, is therefore an average representation of the actual chip temperature. Instantaneous measurement of the temperature over the entire surface of the chip would be extremely difficult to achieve.

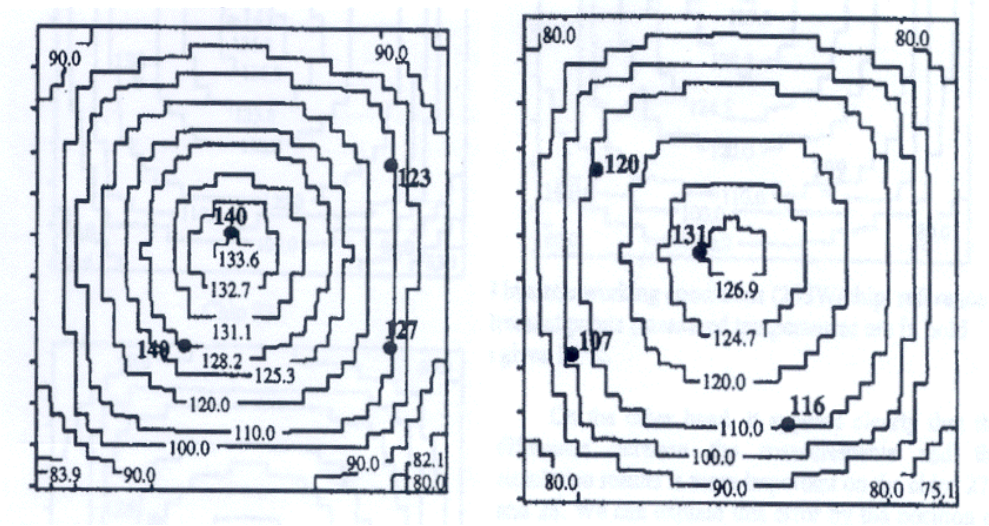


Figure 3.22 Simulated temperature distribution of two IGBT chips. Bold values are measurements for comparison [45]

3.6.3 Dupont et al [55]

Another purpose of FEM simulations in power cycling studies is to aid in the determination of the thermal time constant of a test assembly so that the minimum allowable cycling period can be determined. A similar methodology as before was used and the outcome was the response of the different parts of the test assembly to the application of a step power pulse. The typical simulated response of such an assembly is shown in Figure 3.23. The minimum cycle time can easily be determined from this figure.

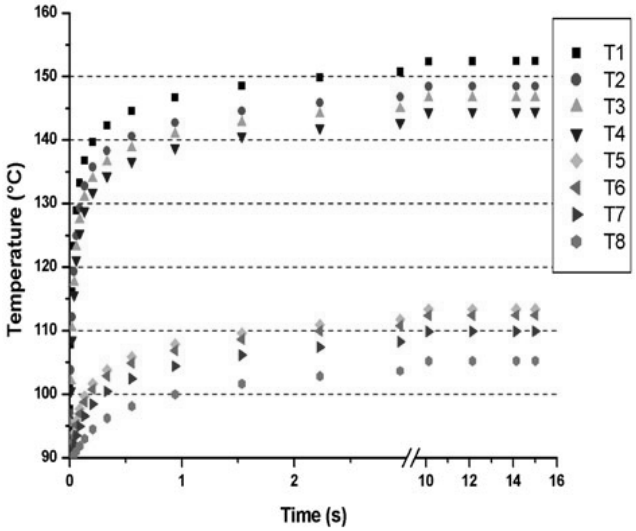


Figure 3.23 Simulated thermal response of the different layers of a power cycling test assembly [55]

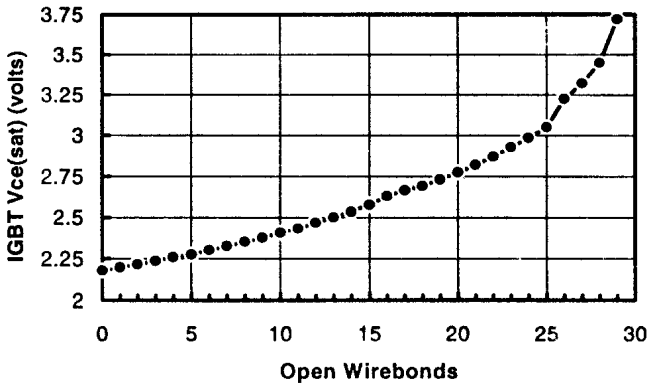
3.7 In-service monitoring of IGBTs

There are several practical outcomes of the work described above, the purpose of which is to give information on the degradation of IGBT modules in service. Three such studies are summarized here.

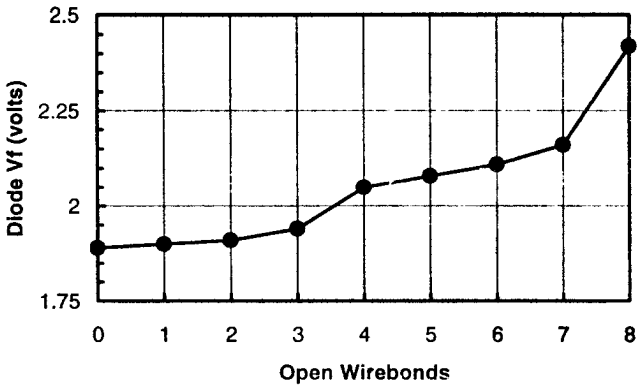
3.7.1 Sankaran et al [58]

It was shown in Section 3.5.2 that $V_{CE(sat)}$ increases as the Al-Si bonds age and the bond-wires become disconnected. A calibration was performed on an opened

IGBT module, rated at 600 V/400 A, to determine $V_{CE(sat)}$ as a function of the number of disconnected wire-bonds. The calibration was performed on the IGBT and on the free-wheeling diode and the results are shown in Figure 3.24. In-service IGBT modules can then be tested or monitored, and the results compared to these figures to determine whether any wire-bonds have become disconnected.



a)



b)

Figure 3.24 Calibration curves of $V_{CE(sat)}$ as a function of open wire-bonds for a current of 400 A: a) IGBT, b) Free-wheeling diode [58]

3.7.2 Lehmann et al [57]

This paper uses the principle outlined in the previous section, but carries it further in that an approach for detecting bond-wire lift-off of IGBT modules while they are in service is presented. This allows for an early warning that lift-off has occurred and that total failure may occur soon. It is based on the sudden increases

in $V_{CE(sat)}$ shown in Figures 3.16 and 3.17. These jumps occur when a bond-wire becomes disconnected or when all of the bond-wires of one parallel chip become disconnected and that chip therefore ceases to be part of the circuit. If bond-wire lift-off is detected, an error signal is sent to the gate driver, which switches off the module.

This method was implemented in commercially available modules by building the sensor, monitoring and control circuitry into the modules. The method can be used in devices using single or multiple IGBT chips.

3.7.3 Coquery et al [48]

A long term study to determine the extent and characteristics of IGBT stresses in railway applications was commissioned. A typical suburban railway system was monitored under normal working conditions, and the observed device stresses were compared to accelerated laboratory tests. This will take several years to complete.

The train chosen was a double-deck regional train consisting of one locomotive and one coach, used in France. The traction inverter consisted of four IGBT packs, rated at 3300 V/1200 A. The main measured parameter was temperature, and so the IGBT modules were equipped with thermocouples. This allowed the real thermal stresses, i.e. the variation in ΔT_{jc}, to be monitored. The effect of seasons and time of day can then also be studied. An example of data recorded from this train is shown in Figure 3.25. The temperature curves were recorded at several different points on the IGBT baseplate. It can be seen how the temperature follows the speed of the train, and that the cycle time is typically a few minutes.

The other part of this investigation is the measurement of $V_{CE(sat)}$ and R_{thjc} in the workshop at predetermined intervals (every 6 months to one year). The purpose is to detect any aging in the field, as these two parameters have been shown to be the significant aging factors.

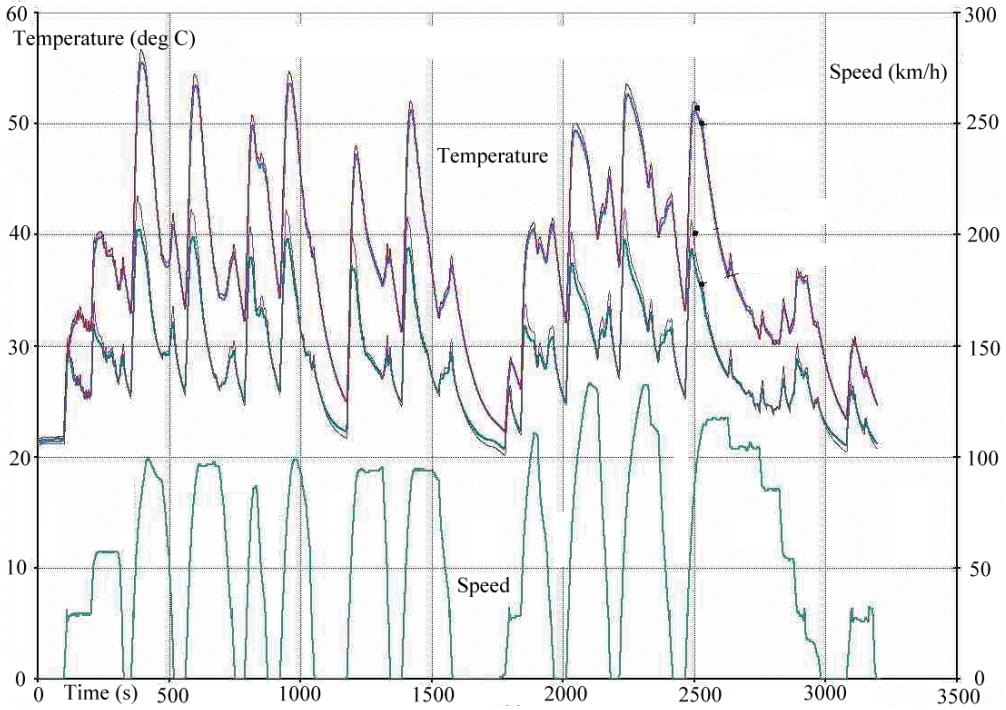


Figure 3.25 Train speed and IGBT module temperature, T_j, measured during a single journey on the Lille-Valenciennes route in France [48]

3.8 Conclusion

This chapter has summarized the previous work undertaken to study the factors that lead to power cycling. The different failure modes were analyzed and the various test methods were described. The most common failure modes are bond-wire lift-off and baseplate solder fatigue. The former can be detected by an increase in $V_{CE(sat)}$ while the latter leads to an increase in Z_{thjc}. Different factors causing this aging were identified. The most important of these factors are the variation in ΔT_{jc} and $\Delta T_{jc(max)}$. The vast majority of test methods, including that specified in the relevant IEC standard, are DC test methods, i.e. the load current is DC during the conduction period. The failure criteria used for these tests as well as the test results were also given. The results of several FEM modeling studies were also presented, as well as studies to investigate the behaviour of IGBT modules under real working conditions.

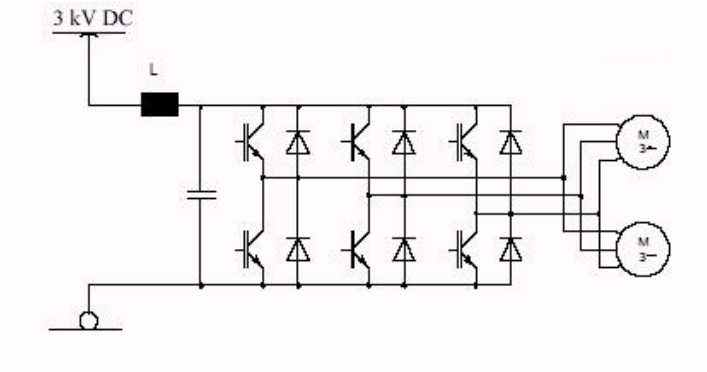
4. AC POWER CYCLING

This chapter is the last of the background chapters and its purpose is to present the issues surrounding AC power cycling. The first section discusses the differences between AC and DC traction. The second section looks at the effect of switching losses on the overall losses. Finally, previous AC test methods are presented.

4.1 AC and DC traction

Both AC and DC power supplies are commonly used for traction systems. Typical European supply voltages are 750 V, 1.5 kV and 3 kV DC, and 15 kV, 16⅔ Hz and 25 kV, 50 Hz [7, 59-62], whereas in North America 50 kV, 60 Hz is common [63]. Examples of typical AC traction motor drives employing IGBTs are shown in Figure 4.1. Each of these circuits contains a number of inverter legs. They are usually three-phase inverters, but controlled rectifiers are also used.

The induction motor is the motor of choice in all traction applications (from subways up to electric and diesel-electric locomotives) as it offers several advantages over the DC motor, the most important being reliability, ruggedness and a high ratio of power to weight. This means that induction motors are smaller than DC motors of the same output power, which is important due to the often limited space in locomotives. Induction motors and associated AC drives have been in service in Europe since the late 1980's.



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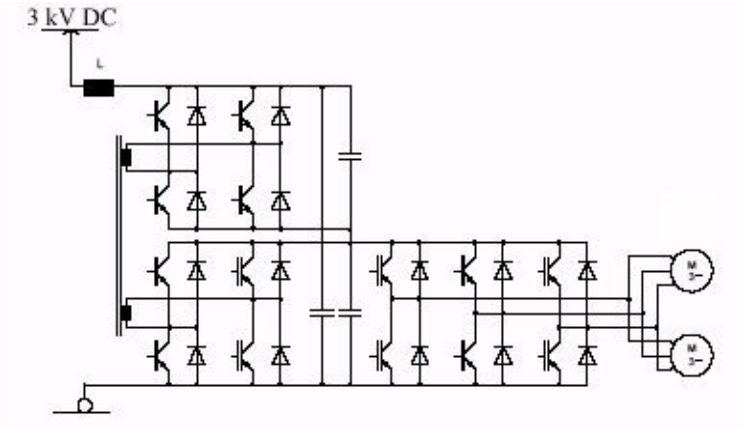

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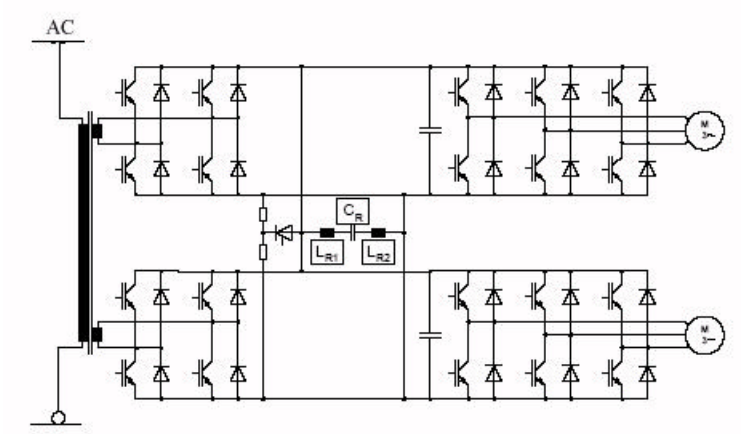

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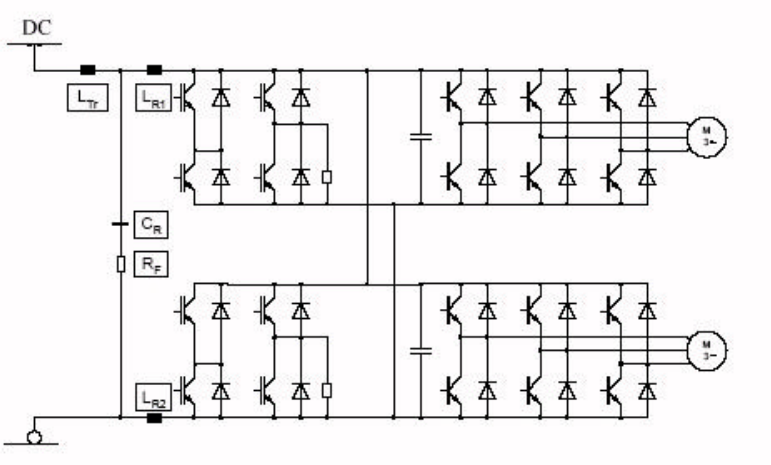


d)

Figure 4.1 Simplified schematic diagrams of typical AC traction motor drives employing IGBTs: a) and b) are fed off a DC power supply, c) and d) are the same drive configured to be able to operate an AC or DC power supplies [59]

DC motors have several disadvantages: the need for brush maintenance, the need for contactors for direction reversal and their susceptibility to pollutants such as coal dust and salt mist [62, 64, 65].

Traction motor drives originally employed mainly SCRs. During the 1980's SCRs were largely replaced by GTOs. IGBTs have several advantages over GTOs and SCRs (refer to Section 2.1.1) but they have only recently become viable in traction applications with devices of sufficient voltage rating becoming commercially available. The use of IGBTs also results in a reduction in the number of individual components used as well as in the overall size of traction motor drives [62, 63].

4.2 Switching and conduction losses

As mentioned in Section 2.1.2, there are four types of IGBT power losses: conduction losses, switching losses, off-state losses and gate driver losses. By far the most significant of these are conduction and switching losses and most authors ignore off-state and gate driver losses because they are sufficiently small [15].

In the DC power cycling test methods discussed in Chapter 3, switching losses are also small enough to play no significant part in the overall DUT losses. However, it was shown in the previous section that many traction loads are AC, meaning that switching losses are not small enough to ignore and should be included in power cycling studies. The lack of switching losses in DC power cycling tests is compensated for by increasing conduction losses by the use of larger currents than would normally be the case in practice, but this is not representative of the real situation. The purpose of this study is to include switching losses in power cycling studies in a way that is as representative of field conditions as possible.

Several authors have studied the effect of switching losses in PWM inverters, showing that switching losses can greatly increase the overall device losses. Two examples of these are shown in Figure 4.2.

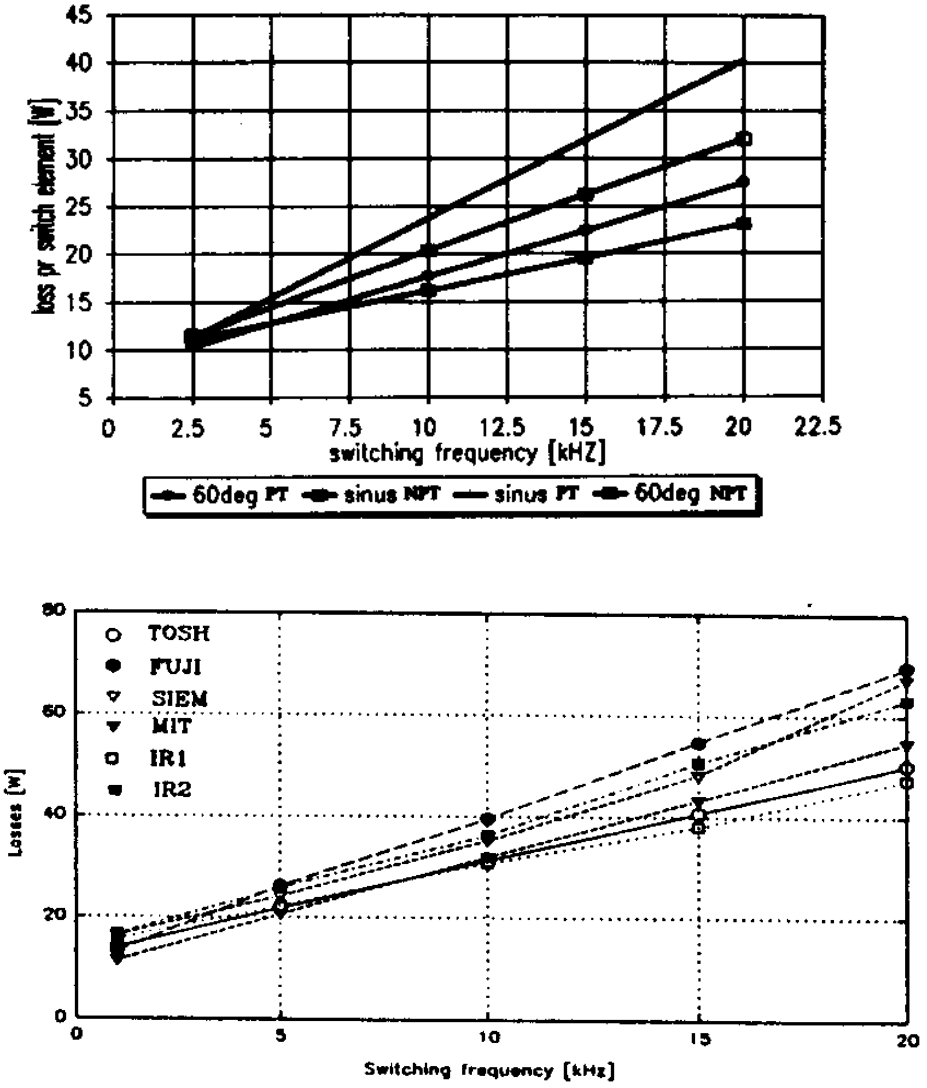


Figure 4.2 Effect of switching frequency on IGBT losses in a typical inverter: device losses for NPT and PT devices using two different PWM strategies (top) [15]; total inverter losses using IGBTs from different manufacturers (bottom) [66]

Figure 4.2 shows that the increase in losses with switching frequency occurs for all PWM modulation strategies and for the devices of all manufacturers. The increase is greater for PT devices than for NPT devices at higher switching frequencies. At lower switching frequencies PT devices have lower overall losses than NPT devices due to their lower conduction losses. A particular switching frequency at which total PT device losses exceed total NPT device losses can

therefore be determined [15]. This is for a particular load current, DC bus voltage and PWM strategy. Two examples are shown in Figure 4.3.

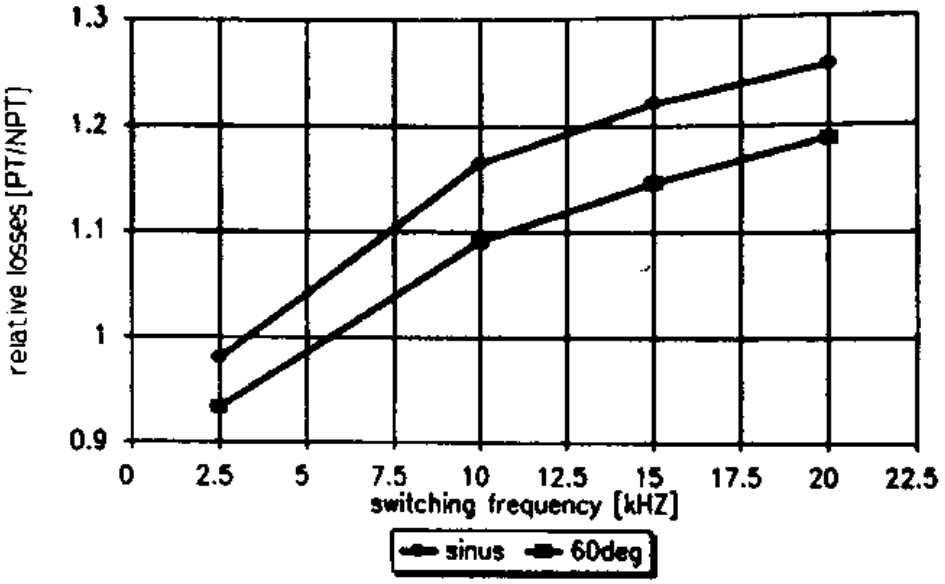


Figure 4.3 Relative losses for two different PWM strategies and for constant load current and DC bus voltage [15]

4.3 Previous AC power cycling tests

Despite the fact that the overwhelming majority of power cycling tests have been DC tests, two AC power cycling tests have also been documented.

4.3.1 Scheuermann et al [67]

This test involved the repeated application of the load temperature cycle of Figure 4.4. Each cycle consisted of two power pulses, each of 3 s duration and separated by a 1 s interval, followed by 8 s of no current. The average and maximum ΔT_{jc} curves of a 3.3 kV/1200 A IGBT module during this cycle are also shown. T_{amb} was kept constant at 20°C and T_{case} was found to be almost constant.

The corresponding IGBT collector current was not shown and the origin of this load profile was not cited. The peak in the maximum ΔT_{jc} waveform at the end of

the second pulse was purposefully included in the test to simulate a braking condition. Instantaneous ΔT_{jc} waveforms were not included. A dynamic switching frequency of 18 kHz and a static switching frequency of 8 kHz were quoted. The meaning of these is unclear. The test results are shown in Figure 4.5. The curve has a similar form to DC test results. However, significantly more cycles were withstood by the modules. There are several possible reasons for this, but insufficient information was provided by the authors to come to adequate conclusions.

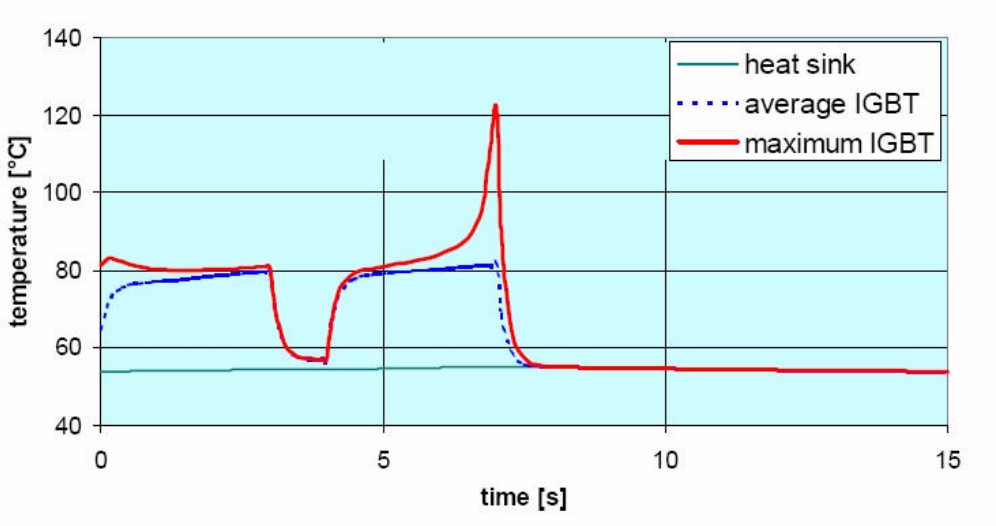


Figure 4.4 Load profile for the Scheuermann AC power cycling test [67]

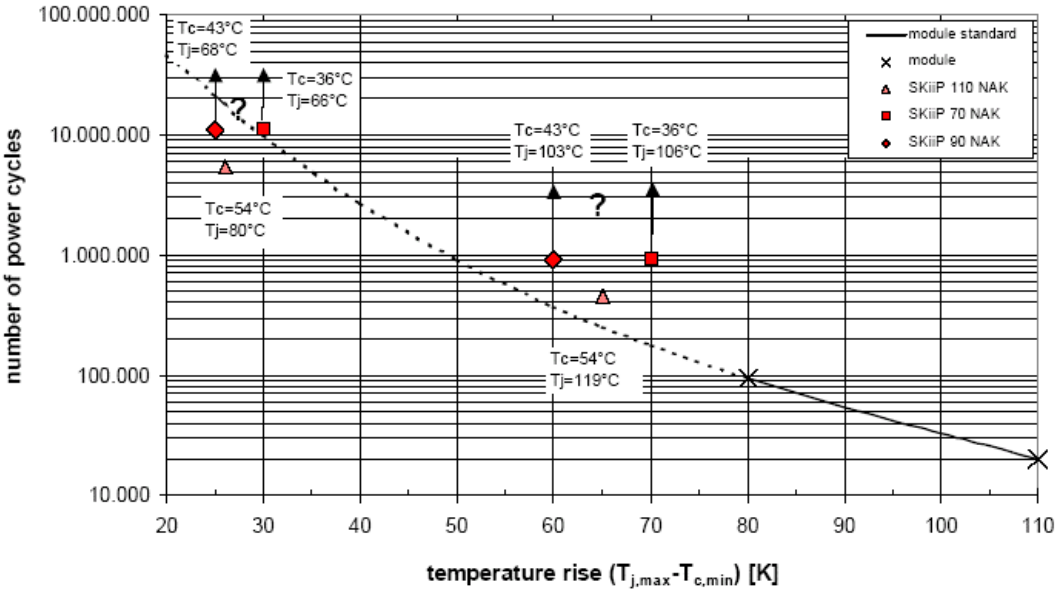


Figure 4.5 Test results of the Scheuermann AC power cycling test [67]

4.3.2 Sankaran et al [58]

This test involved the application of the load profile shown in Figure 4.6. This test involved the application of a load current pulse of approximately 10 s duration (t_{on}) followed by 30 s of no current (t_{off}). The value of I_{on} was rated current of the DUT (the curve shown is for a 600 V/400 A device). This current was not a DC current as shown, but had a 2 kHz PWM waveform. The duty cycle of the PWM waveform was adjusted to achieve the desired variation in ΔT_{jc}. Figure 4.6 shows that large variations in ΔT_{jc} are possible using this method. The heatsink temperature varied only slightly, as in the previous test.

The test conditions for the various tests performed are shown in Table 4.1, the number of cycles to failure are shown in Table 4.2 and the change in $V_{CE(sat)}$ with the number of cycles is shown in Figure 4.7. Four different IGBT packaging technologies were used: X1 to X4, where X1 was the earliest technology and X4 the latest. Five different IGBTs and two diodes were subjected to each test.

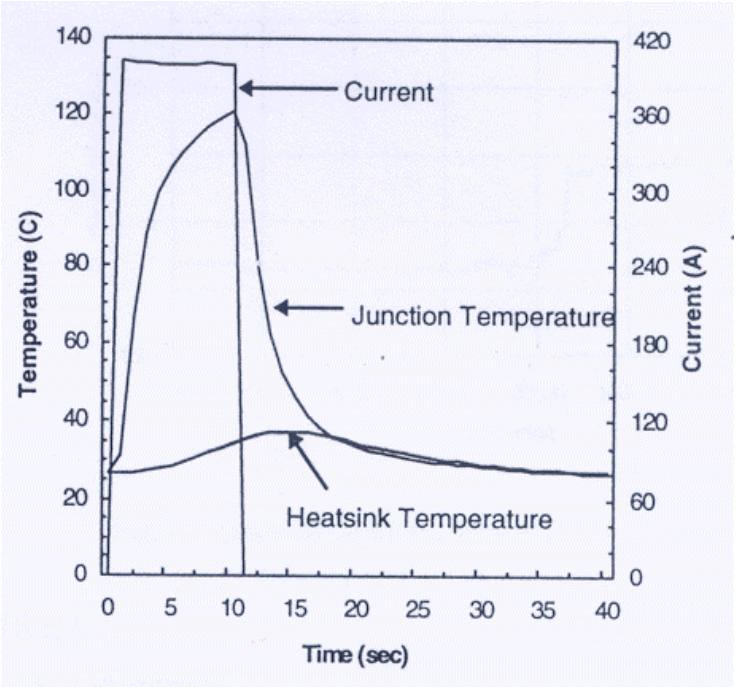


Figure 4.6 Load profile for the Sankaran AC power cycling test [58]

Table 4.2 shows that the newer IGBTs survived substantially more cycles than the older versions. The diodes were found to be more susceptible to failure than the IGBTs. This stresses the importance of also testing the diodes, especially as the diodes generally have lower ratings than the IGBTs (refer to Section 2.2).

Figure 4.7 shows a similar trend as was found for the DC tests – refer to Section 3.5.2 – where $V_{CE(sat)}$ increased gradually with the number of cycles conducted, but with a few steps where wire-bonds are suspected to have completely broken.

The advantages of this method are that switching losses were included in the test in a controlled manner and that the free-wheeling diodes were also tested. The disadvantage is that the magnitude and waveform of the test current were not representative of real operating conditions, giving rise to unrealistically large variations in ΔT_{jc}, in a similar manner to the DC test methods.

Table 4.1 Test conditions for the Sankaran AC power cycling test [58]

Test number	T_H (°C)	Variation in ΔT_{jc} (°C)	$\Delta T_{jc(max)}$ (°C)	IGBT packaging
IGBT1	30	90	120	X1
IGBT2	50	60	110	X2
IGBT3	50	45	95	X3
IGBT4	50	45	95	X4
IGBT5	60	60	120	X3
Diode 1	60	60	120	X4
Diode 2	30	90	120	X4

Table 4.2 Sankaran AC power cycling test results: no. of cycles to failure [58]

Test number	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
IGBT1	12 470	28 450	41 670	34 150	42 770
IGBT2	203 780	88 080	161 930	190 680	129 370
IGBT3	No failures recorded at 600 000 cycles – tests terminated				
IGBT4	No failures recorded at 500 000 cycles – tests terminated				
IGBT5	762 180	773 460	841 980	575 000	532 480
Diode 1	176 870	127 540	142 880	126 460	99 880
Diode 2	47 220	41 720	57 730	43 430	55 600

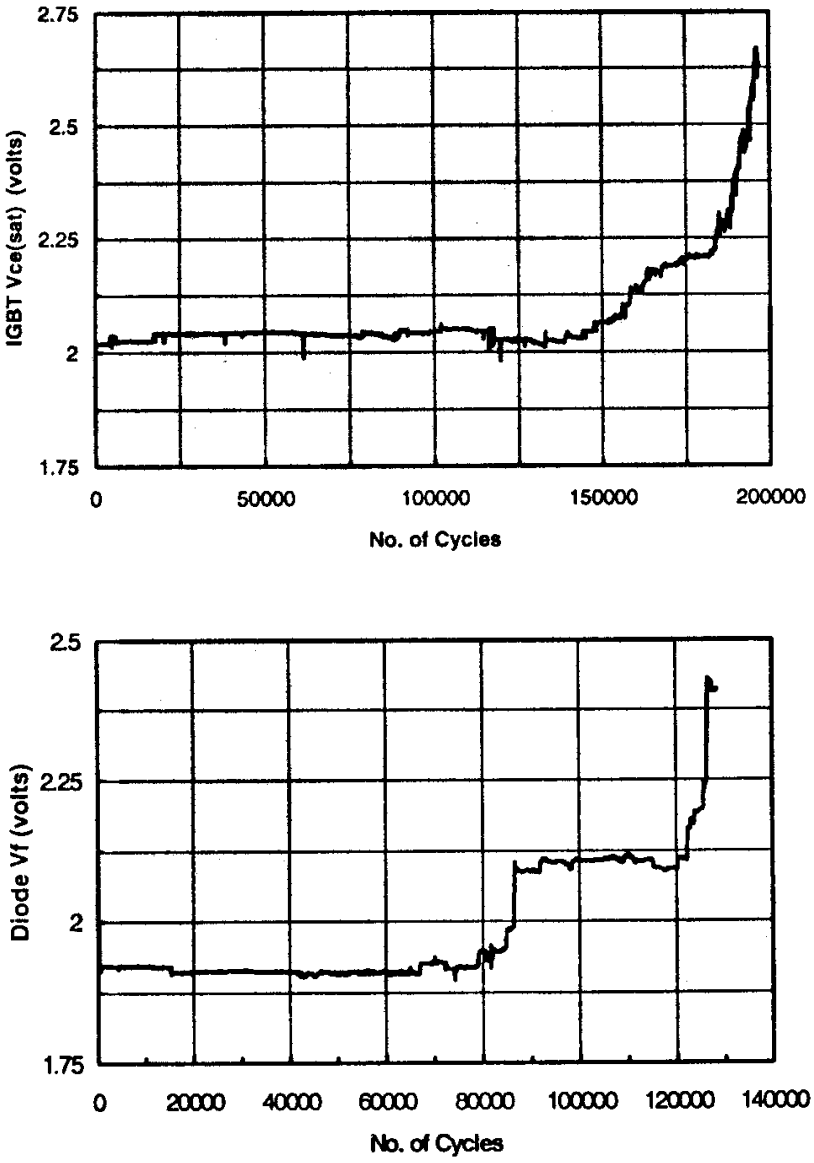


Figure 4.7 Change in $V_{CE(sat)}$ with the number of cycles for an IGBT and a diode during the Sankaran AC power cycling test [58]

4.4 Conclusions

This chapter has presented typical traction converters and AC and DC traction has been compared. It was found that the induction motor is the most common traction motor and hence that AC power cycling tests are important tools. The effect of switching losses on IGBTs in typical inverters was also shown. Finally,

two published AC power cycling tests were presented and several short-comings were noted.

5. INVESTIGATION STRATEGY

The purpose of this chapter is to review the published literature and from that to state and justify the direction of this study. The first section summarizes the state-of-the-art in power cycling tests by drawing from the preceding two chapters. In the second section the strategy adopted for this study is described, based on the first section. The chapters following this one describe the implementation of the strategy.

5.1 Power cycling tests: state-of-the-art

5.1.1 Assessment criteria for evaluating power cycling test methods

The state of the art of IGBT power cycling tests was assessed using the following criteria:

1. Accuracy with which service conditions are reflected
2. Amount and quality of information gained from the results
3. Complexity of the test apparatus
4. Cost of running a test
5. Total duration of a test

Firstly, all laboratory tests, whatever their nature, must be as representative of actual service conditions as possible. However, totally realistic tests are hardly ever possible for a variety of reasons, most notably the difficulty of exactly reproducing all field conditions and the long testing times. Therefore, the limitations of a laboratory test must be known and the effect of these limitations on the outcome must be understood. For example, typical traction load profiles such as those of Figures 3.1 and 3.2 are difficult to reproduce in the laboratory. Also, there are an almost unlimited number of different possibilities of load profiles in the field, and therefore it is impossible to cover all eventualities.

However, laboratory tests are still valuable tools and the information gained from such tests is still very useful, as the tests can give a comparison between the performance of different module designs. The effect of specific factors can also be studied in a controlled environment.

The complexity of a test covers aspects such as the ability to easily change and control different variables. Also, the complexity of the auxiliary equipment such as the controller, cooling and measurement systems is important as this affects the reliability of the test setup.

The monetary cost involved with the test setup involves a number of factors. Firstly, the fewer the number of power devices and the less auxiliary equipment needed, the cheaper the setup. Secondly, the amount of electrical power needed to run a test is important as most of the devices tested are rated for high currents and voltages and the tests can take a long time. Hence, energy costs can be large.

Lastly, another advantage of laboratory testing is that the tests can be accelerated. This means that useful results can be obtained much faster than if in situ tests were performed. Shortening of cycle periods (t_{on} and t_{off}) can often be achieved due to the relatively short thermal time constants of the devices being tested. However, the effect of the acceleration on the test results must be fully understood.

5.1.2 Comparison of AC and DC test methods

The available AC and DC power cycling test methods are now compared using the above criteria. DC test methods are summarized in Table 5.1 and AC methods are summarized in Table 5.2. The tables show that both methods have their advantages and disadvantages. DC test methods are obviously more realistic when DC loads are modeled, while AC test methods are more realistic when switching losses need to be included. DC test setups are less complex and less expensive than AC setups and are also easier to control.

Table 5.1 Summary of DC test methods

Criteria	Advantages	Disadvantages
Accuracy	• Can accurately reproduce DC loads • Can model extreme field conditions – large continuous DC currents give large values of ΔT_{jc}	• Cannot accurately model AC loads • Several test methods used higher than normal currents, resulting in very high variations in ΔT_{jc} • Switching losses are generally excluded
Quality of output data	• Good comparison between the performance of different technologies • The effect of varying different parameters can be clearly seen	• Can be difficult to relate test results to real operating conditions
Complexity	• Usually simple to set up and control	• Some tests require water-cooling systems
Cost	• Test circuit costs are small	• High energy costs due to the use of resistive loads and high test currents
Duration	• Short if time constant of DUT is short	• Needs long cycle periods if baseplate solder layer is to be stressed

Table 5.2 Summary of AC test methods

Criteria	Advantages	Disadvantages
Accuracy	• Can accurately reproduce AC loads • Switching losses are included	• Cannot accurately model DC loads • Several test methods used higher than normal currents, resulting in very high variations in ΔT_{jc} • Lack of detailed information available on present methods
Quality of output data	• Shows the effect of switching losses	• Can be difficult to relate test results to real operating conditions
Complexity	• None	• More complex than DC tests (controllers etc)
Cost	• None	• High energy costs due to the use of resistive loads and high test currents • Increased costs due to increased complexity
Duration	• Short if time constant of DUT is short	• Both methods used long cycle periods • Needs long cycle periods if baseplate solder layer is to be stressed

There are several short-comings with both AC and DC methods. These are the use of often unrealistically high currents, which produce unrealistically high variations in ΔT_{jc}, high energy costs due to these high currents and the use of resistive loads and the fact that most methods are not easily related to service conditions. Also, the effect of the large instantaneous power loss due to switching under normal operating conditions is not always accurately modeled, as switching may influence IGBT aging. The aim of this study is to present a method that attempts to overcome the above short-comings.

5.2 Proposed new method

The purpose of the present study is to develop a novel power cycling test method with the following characteristics:

1. It must include switching losses associated with the generation of inverter waveforms
2. Both IGBTs and free-wheeling diodes must be tested
3. The test setup must be kept as simple as possible
4. Equipment and energy costs must be kept to a minimum
5. The test duration must be as short as possible
6. Load current magnitude and waveform and the variation in ΔT_{jc} must be as representative as possible of service conditions

In an attempt to achieve the above objectives, a novel test circuit is proposed. It is a modified form of the single-phase inverter. Its purpose is to accurately reproduce the variation in ΔT_{jc} of a medium-sized (20-100 kW) inverter driving a high power factor inductive load, by using a low power factor inductive load. The process used to achieve this is described in the following chapters. First, the conventional inverter is analyzed. Then the proposed test circuit is introduced and its performance is compared to the conventional circuit and to the above criteria by simulation. Finally, the test circuit is built and its performance compared to the predictions.

6. THE CONVENTIONAL H-BRIDGE

In this chapter the conventional H-bridge (single-phase inverter) is simulated. First, the simulation methodology is described and its accuracy is verified. Next, the circuit and the results are presented. The simulation tool used was Matlab® [68]. The electric circuit was first modeled in Simulink using the Power System Toolbox. The current waveforms were then imported into the Matlab Workspace where calculations were performed to determine the waveforms of the power loss and ΔT_{jc}. This was performed for IGBTs and free-wheeling diodes. Next, the effect of load power factor and switching frequency are shown. Finally, the results are compared to previous work. The device used was the Semikron SKM 100 GB 123 D (see Section 2.1.3).

6.1 Description of simulation methods

6.1.1 IGBT

The Matlab code is shown in Appendix B.1. A method of superposition was used and the calculations were based on the method recommended by the manufacturer [10], with a more accurate estimation of $V_{CE(sat)}$ taken from Casanellas [69]. The first step involved approximating the current waveforms by very short current pulses, as shown in Figure 6.1.

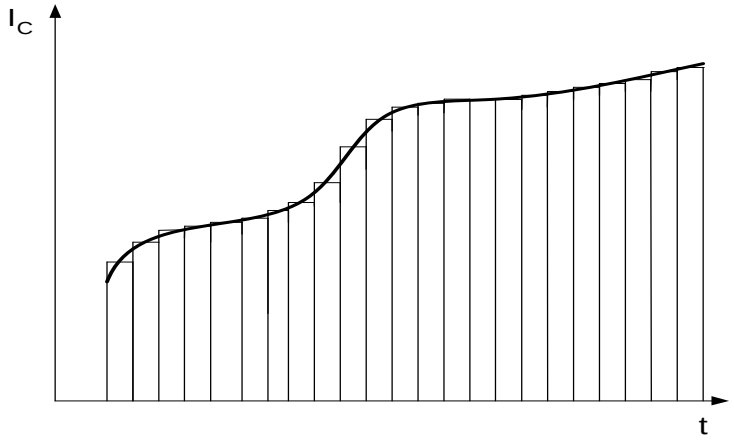


Figure 6.1 Sampling of an IGBT collector current waveform

The conduction power loss was computed for each pulse by multiplying the current for that pulse by the on-state voltage drop ($V_{CE(sat)}$), as calculated from the manufacturer's data, giving rise to waveforms such as those shown by the second graph of Figure 6.2. The IGBT output characteristic provided by the manufacturer was approximated by a straight line (refer to Figure 6.3). $V_{CE(sat)}$ was then calculated using the conventional equation of a straight line [69]:

$$V_{CE(sat)} = \frac{V_{CEN} - V_{CE0}}{I_{C(rated)}} \cdot I_C + V_{CE0} \quad \text{..... (6.1)}$$

where V_{CEN} and V_{CE0} are determined as shown in Figure 6.3 (V)

$I_{C(rated)}$ = Rated IGBT collector current (A)

I_C = Actual on-state IGBT collector current (A)

The switching energy for each switching operation was obtained from the device data sheet for the specific turn-on current, which gave the normalized energy. Actual switching energy was calculated using Equation 6.2:

$$E_{on} = E_{on(norm)} \cdot \frac{V_{CC}}{V_{CC(ref)}} \quad \text{..... (6.2)}$$

where E_{on} = Actual turn-on energy (J)

$E_{on(norm)}$ = Normalized turn-on energy at V_{CC} (J)

V_{CC} = Actual DC bus voltage – set in Part 1 (V)

$V_{CC(ref)}$ = Reference DC bus voltage – set by manufacturer (V)

Turn-off energy was calculated in the same way. Switching power losses were determined by dividing the energies by the simulation time step, as shown by the third graph of Figure 6.2. The switching losses were then substituted for the conduction losses at the relevant time steps, giving the total losses of the fourth graph of Figure 6.2.

The instantaneous value of ΔT_{jc} at each time step was determined by multiplying the total power at each point by the corresponding value of the IGBT junction-

case thermal impedance (Z_{thjc}), as given in the device data sheet. This was achieved by using the principle of superposition similar to that used in Section 3.4.2 of [70] and illustrated in Figure 6.4. Each power pulse resulted in a first order exponential rise in ΔT_{jc} at the start of the pulse and in a first order exponential fall in ΔT_{jc} of the same magnitude at the end of the pulse. The rise in ΔT_{jc} at each time step due to each power pulse was computed, and the sum of all these values gave the total rise in ΔT_{jc}, as shown by the dark curve in Figure 6.4. This method can be extremely intensive of computing power if significant accuracy is required, as the number of computations increases exponentially with the number of time steps, as illustrated in Figure 6.4. The time step would be considerably less than the device thermal time constant.

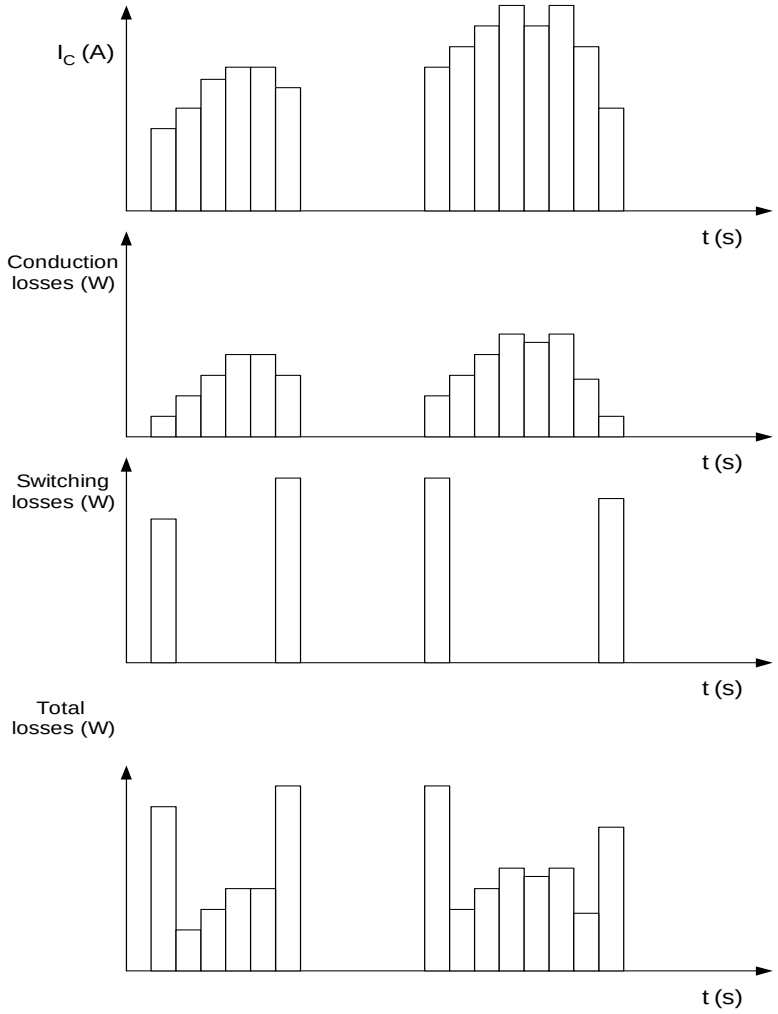


Figure 6.2 IGBT power loss waveforms as calculated from a sampled collector current waveform

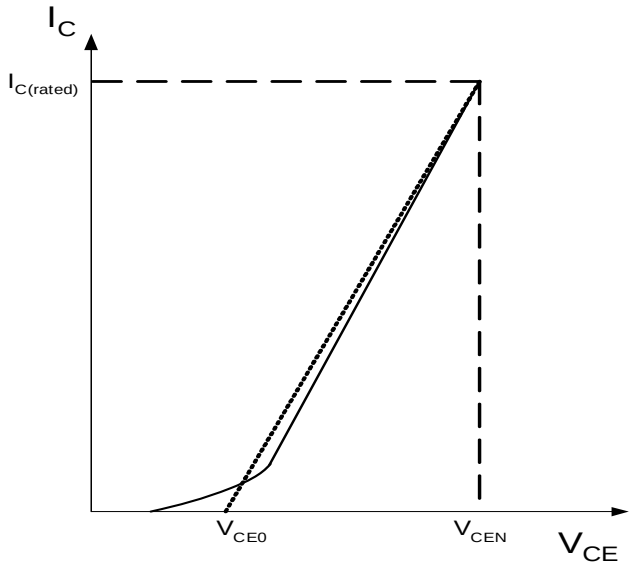


Figure 6.3 Approximation of an IGBT output characteristic by a straight line [69]

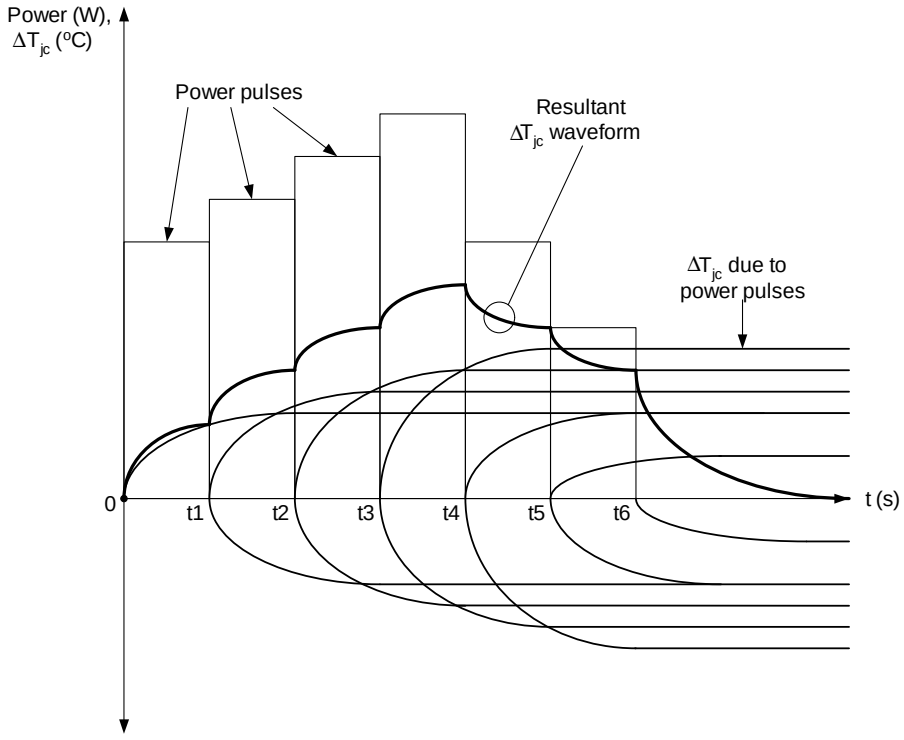


Figure 6.4 Determination of the IGBT ΔT_{jc} waveform from the power dissipation waveform

6.1.2 Diode

The Matlab code for free-wheeling diodes is shown in Appendix B.2. The method for free-wheeling diodes was very similar to that for IGBTs, with only the following changes:

1. IGBTs dissipate significant energy during both turn-on and turn-off, whereas this only occurs during turn-off for diodes. Therefore, only turn-off losses are given by the manufacturer [12] and turn-on losses were not calculated.
2. The turn-off losses were calculated from the reverse recovery charge as given by the manufacturer as a function of R_G and the diode current (refer to Appendix A). R_G was taken as 15 Ω, as recommended by the manufacturer [71]. The turn-off energy was then determined from Equation 6.3:

$$E_{off} = \int V_{CC} \cdot I_A \cdot dt = V_{CC} \cdot \int I_A \cdot dt = V_{CC} \cdot Q_{rr} \quad \text{.....} \quad (6.3)$$

where Q_{rr} is the reverse recovery charge of the diode

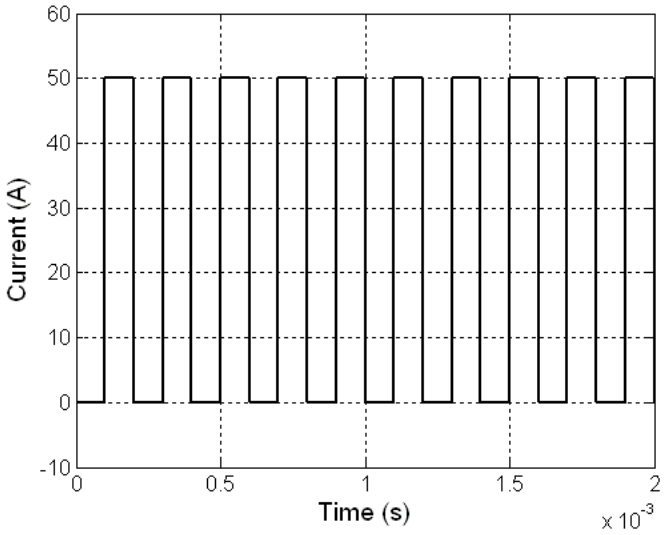
3. Different constants were used for the on-state characteristic.
4. A different curve was used for Z_{thjc}.

6.2 Verification of simulation methods

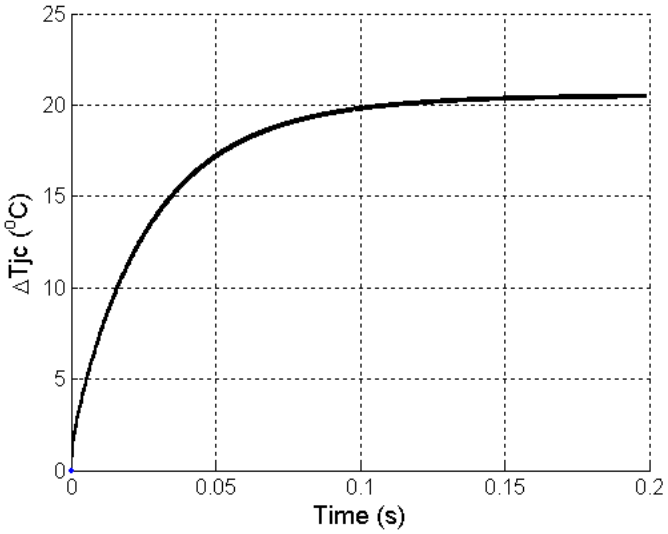
The method described in the previous sections was verified to show that the results are acceptably accurate. This was achieved by running the simulation for a simple IGBT collector current waveform and then comparing the results to those obtained by arithmetic calculation. The diode simulation was verified in the same way.

6.2.1 IGBT

A case of an IGBT conducting a repetitive 50 A peak rectangular collector current with a frequency of 5 kHz, as shown in Figure 6.5a, was chosen. The resultant waveform of ΔT_{jc} for a time period of 200 ms is shown in Figure 6.5b. Note that the time scale of Figure 6.5a is smaller than that of Figure 6.5b.



a)



b)

Figure 6.5 Verification of the calculation method: a) Continuous IGBT collector current waveform; b) Calculated ΔT_{jc} waveform for this current waveform

Using simple arithmetic calculations, the average steady-state increase in ΔT_{jc} due to conduction losses only was determined using Equation 6.4:

$$\Delta T_{jccond(ave)} = P_{cond(ave)} \cdot Z_{thjcss} = E_{cond} \cdot \frac{t_{cond}}{T} \cdot Z_{thjcss} = I_c \cdot V_{CE(sat)} \cdot \frac{t_{cond}}{T} \cdot Z_{thjcss} \quad \text{... (6.4)}$$

where $P_{cond(ave)}$ = Average conduction loss (W)

Z_{thjcss} = Steady-state junction-case thermal impedance (K/W)

E_{cond} = Conduction energy loss per conduction period (J)

t_{cond} = Period of conduction during each 5 kHz period (0.1 ms)

T = Switching period = $1/f$ (s)

f = Switching frequency (5 kHz)

I_c = Collector current during conduction (50 A)

$V_{CE(sat)}$ = Calculated using Equation 6.1 (V)

The average steady-state switching power loss was obtained from the data:

$$P_{sw(ave)} = (E_{on} + E_{off}) \cdot f \quad \text{..... (6.5)}$$

where E_{on} and E_{off} are the switching energy loss values obtained from the data sheet.

Multiplying this result by Z_{thjcss}, gives the average steady-state increase in ΔT_{jc} due to switching, $\Delta T_{jcsw(ave)}$. The total average steady-state increase in ΔT_{jc}, $\Delta T_{jc(ave)}$, is the sum of the conduction and switching temperature rises:

$$\Delta T_{jc(ave)} = \Delta T_{jccond(ave)} + \Delta T_{jcsw(ave)} = 20.6°C \quad \text{.....} \quad \text{(6.6)}$$

The value obtained from the simulation was 20.5 °C (as shown in Figure 6.5b). Therefore, it can be seen that the simulation method is acceptably accurate.

6.2.2 Diode

The same current waveform as above was chosen as the diode anode current waveform. Once again, the average steady-state increase in ΔT_{jc} was calculated, and the result was compared to the value obtained from the simulation. This was again determined from the sum of the temperature rises due to the conduction and switching losses separately. The conduction component was obtained using Equation 6.4 and substituting diode data. The switching component was calculated using Equation 6.5, setting E_{on} to be zero and substituting diode data for E_{off}. Summing these two components gave the following:

$$\Delta T_{jc(ave)} = \Delta T_{jccond(ave)} + \Delta T_{jcsw(ave)} = 29.6°C \quad \text{..... (6.7)}$$

The results of the simulation are shown in Figure 6.6. The value of $\Delta T_{jc(ave)}$ obtained from the simulation is 30.5°C. Therefore, the calculation method for diodes is also acceptably accurate.

The effect of simulation time step was found to be negligible for both devices.

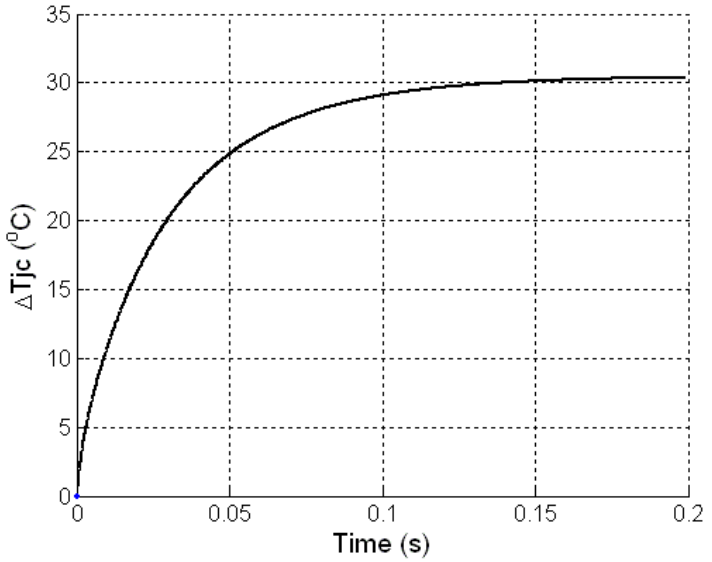


Figure 6.6 Verification of the calculation method: calculated diode ΔT_{jc} waveform for the anode current waveform of Figure 6.5a

6.3 The circuit and its operation

The above method was applied to a conventional single phase H-bridge. This circuit is widely used for variable speed drives (VSDs). A schematic diagram of the circuit is shown in Figure 6.7. A DC voltage source was applied to two IGBT legs, each consisting of two series IGBTs and two free-wheeling diodes, mounted either side of the load. The SKM 100 GB 123 D was again used.

The IGBTs were controlled in such a way as to obtain the desired current through the load, I_{load}. This current was a 50 Hz sinusoidal waveform, and was achieved by controlling the IGBTs using simple pulse width modulation (PWM), i.e. by comparing a reference sinusoidal waveform of 50 Hz with a triangular wave of the desired switching frequency. The IGBTs were switched in pairs: IGBTs 1 and 4 were switched together and IGBTs 2 and 3 were switched inversely to the first pair. The IGBTs in a phase leg (1 and 3 or 2 and 4) may never be on simultaneously as the DC bus would be short circuited. The control method is illustrated in Figure 6.8.

An alternative method, where only the upper IGBTs (1 and 2) are controlled by PWM and the lower IGBTs (3 and 4) are permanently on during the half cycle in which their corresponding IGBTs conduct, is shown in [72]. The method of Figure 6.8 was chosen as significant switching losses are included in all devices and all devices of the same type are stressed equally.

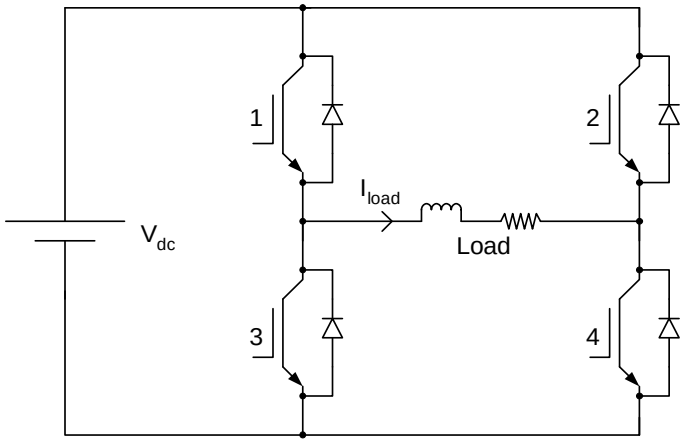


Figure 6.7 Single phase H-bridge circuit

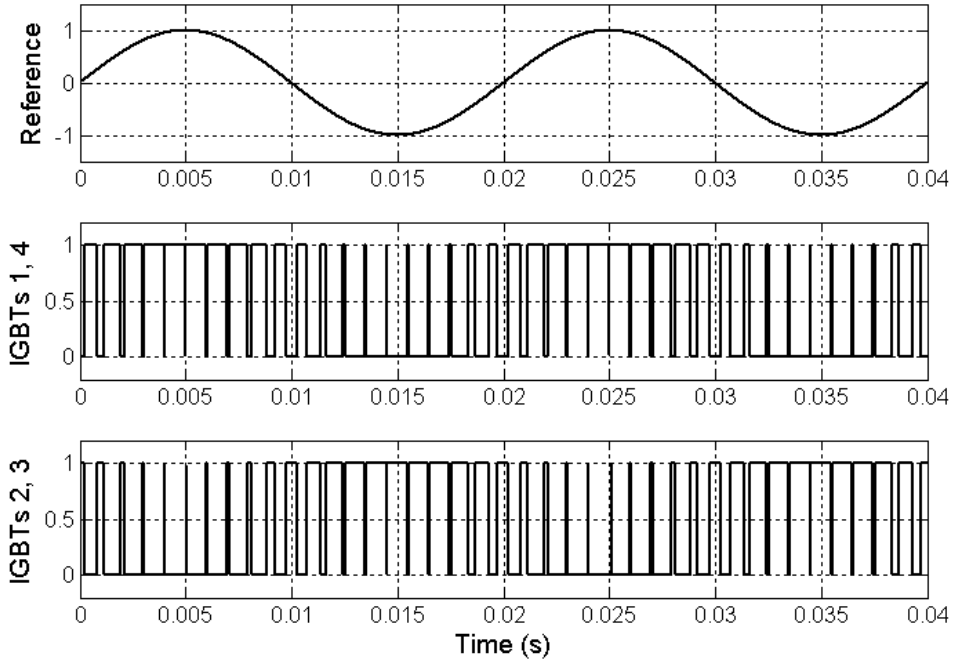
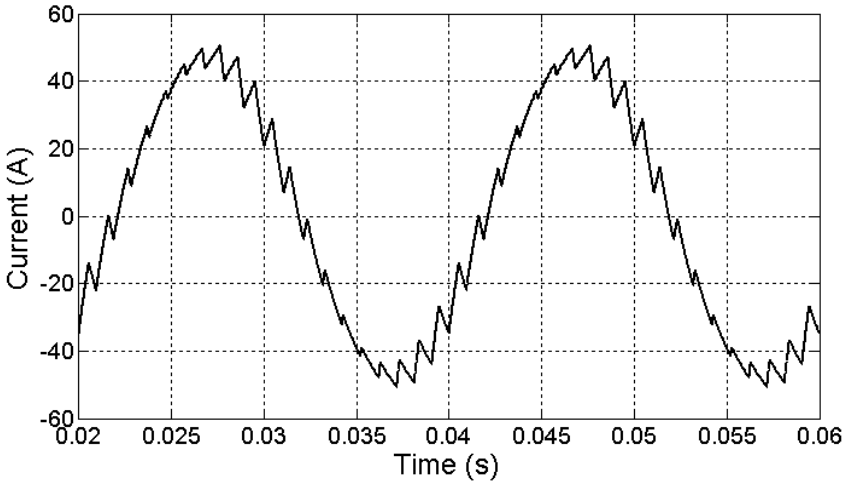


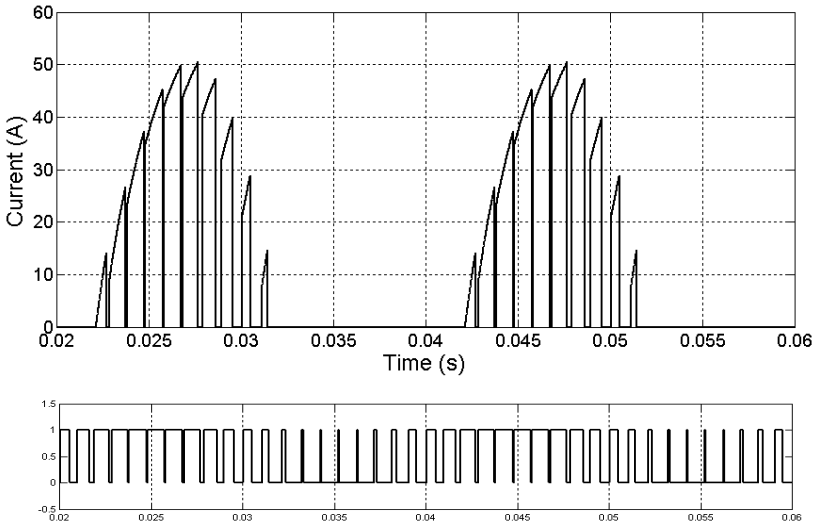
Figure 6.8 PWM control method used in this study

The operation of the circuit is illustrated by the device current waveforms of Figure 6.9. These waveforms were obtained by modeling the circuit using Simulink [68]. The following parameters were used:

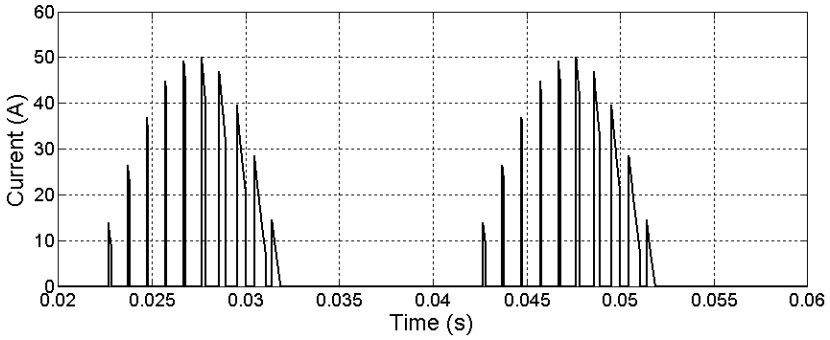
1. The load power factor was 0.8, as justified in Section 2.2.
2. The peak current was 50 A, half the device rating.
3. The DC bus voltage was 537 V, which is the voltage that would appear if a standard AC supply voltage of 380 V were used.
4. The load was modeled as a series RL branch. The resistor and inductor values were calculated from the voltage, current and power factor criteria above.
5. The switching frequency was 1 kHz, to give clarity to the waveforms.
6. All IGBTs were modeled as an ideal switch in series with an ideal diode. Both devices were assigned an on-state resistance of 10 mΩ.
7. A snubber capacitance of 2 μF was placed across the DC bus.



Load

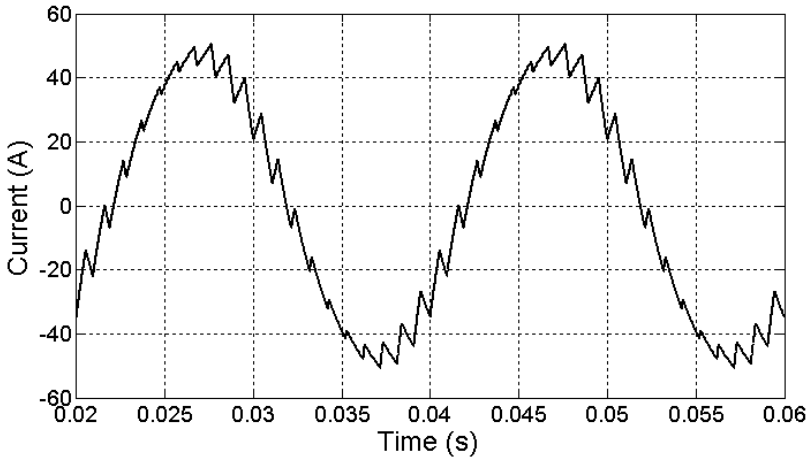


IGBTs 1 and 4

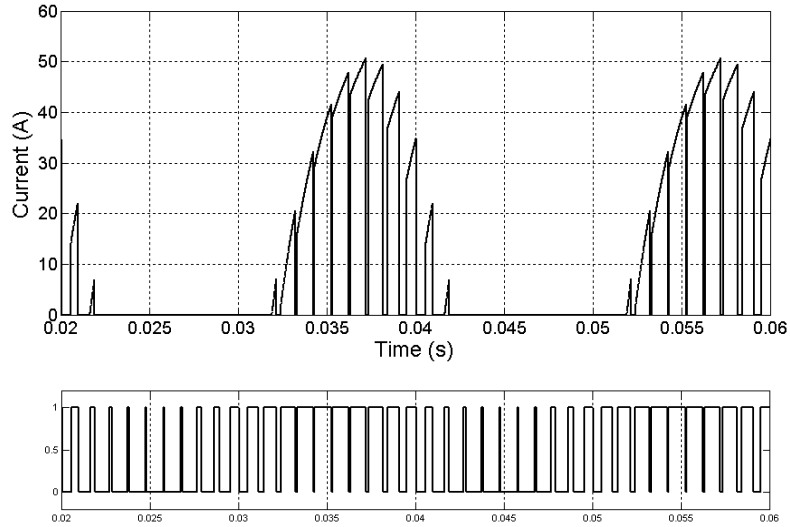


Diodes 2 and 3

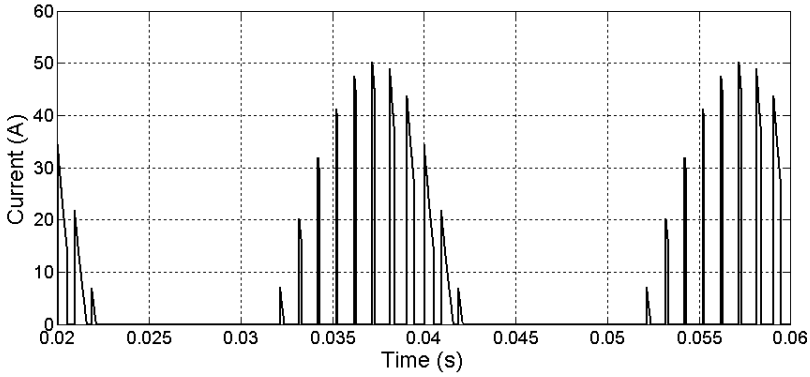
Figure 6.9a Current waveforms of load, IGBTs 1 and 4 and diodes 2 and 3



Load



IGBTs 2 and 3



Diodes 1 and 4

Figure 6.9b Current waveforms of load, IGBTs 2 and 3 and diodes 1 and 4

The following may be noted from Figure 6.9:

1. IGBTs 1 and 4 and diodes 2 and 3 conduct current during the positive half cycle of the load current waveform, and IGBTs 2 and 3 and diodes 1 and 4 conduct during the negative half cycle of the load current waveform.
2. When the IGBTs conduct current, the load current increases because the source supplies power to the load. When the diodes conduct, the load current decreases as power is being returned to the source.
3. The high power factor means that the IGBTs conduct current for significantly longer duration than the diodes.
4. The low switching frequency (1 kHz) means that the load current waveform is not of high quality. Increasing the switching frequency makes the load current waveform more sinusoidal, but increases device switching losses.
5. All IGBT current waveforms are identical. Likewise, all diode waveforms are identical. Therefore, only one set of calculations needs to be performed for IGBTs and one for diodes.
6. The waveforms are similar to those in the literature [70, 72]. A comparison can be found in Section 6.9.

6.4 Thermal calculation results

Next, the instantaneous power dissipation and ΔT_{jc} waveforms were calculated for the above current waveforms. The results are shown in Figure 6.10 for IGBTs and 6.11 for diodes. These figures show the following:

1. The ΔT_{jc} waveforms closely follow the current waveforms: when there is current flow ΔT_{jc} increases, and when there is no current flow ΔT_{jc} decreases.
2. Conduction losses are illustrated by the “envelope” of the instantaneous power waveforms. This envelope has a similar shape to the current waveform.
3. Switching losses are illustrated by the additional points above the conduction losses. These occur at both turn-on and turn-off for IGBTs, but

only at turn-off for diodes. The overall effect of the switching losses is small because of the low switching frequency.

4. The high load power factor causes the IGBT current pulses to be longer than the diode pulses at higher current levels, i.e. near the peak of the load current waveform. The IGBT ΔT_{jc} waveform then rises faster than that of the diode because it conducts current for a longer duration per 20 ms cycle.
5. Both waveforms do not end at zero after one 20 ms cycle and will therefore continue rising with the number of cycles conducted. However, steady-state is expected to be reached after a certain number of 20 ms cycles.

The ΔT_{jc} waveforms for a number of cycles are shown in Figure 6.12. These waveforms are for an application of 240 ms (12 cycles) of the above load current waveform and then 240 ms of no current. These figures show that both ΔT_{jc} waveforms reach steady-state after approximately eight cycles. An envelope may be drawn around each waveform. These envelopes have the same time constant and shape as that of the thermal impedance curve of each device, as expected.

The variation in ΔT_{jc} is labeled in Figure 6.12. It is defined as the difference between the maximum instantaneous value of ΔT_{jc} during the conduction period (t_{on}) and the steady-state value of ΔT_{jc} during the off cycle (t_{off}). This constitutes one power cycle. Extending t_{on} or t_{off} would not affect the variation in ΔT_{jc}. Therefore, the minimum allowable cycling period is approximately 480 ms (t_{on} = t_{off} = 240 ms), if only the bond wire-chip interface is to be stressed. This is significantly shorter than the periods used in previous tests (refer to Sections 3.3 and 4.3).

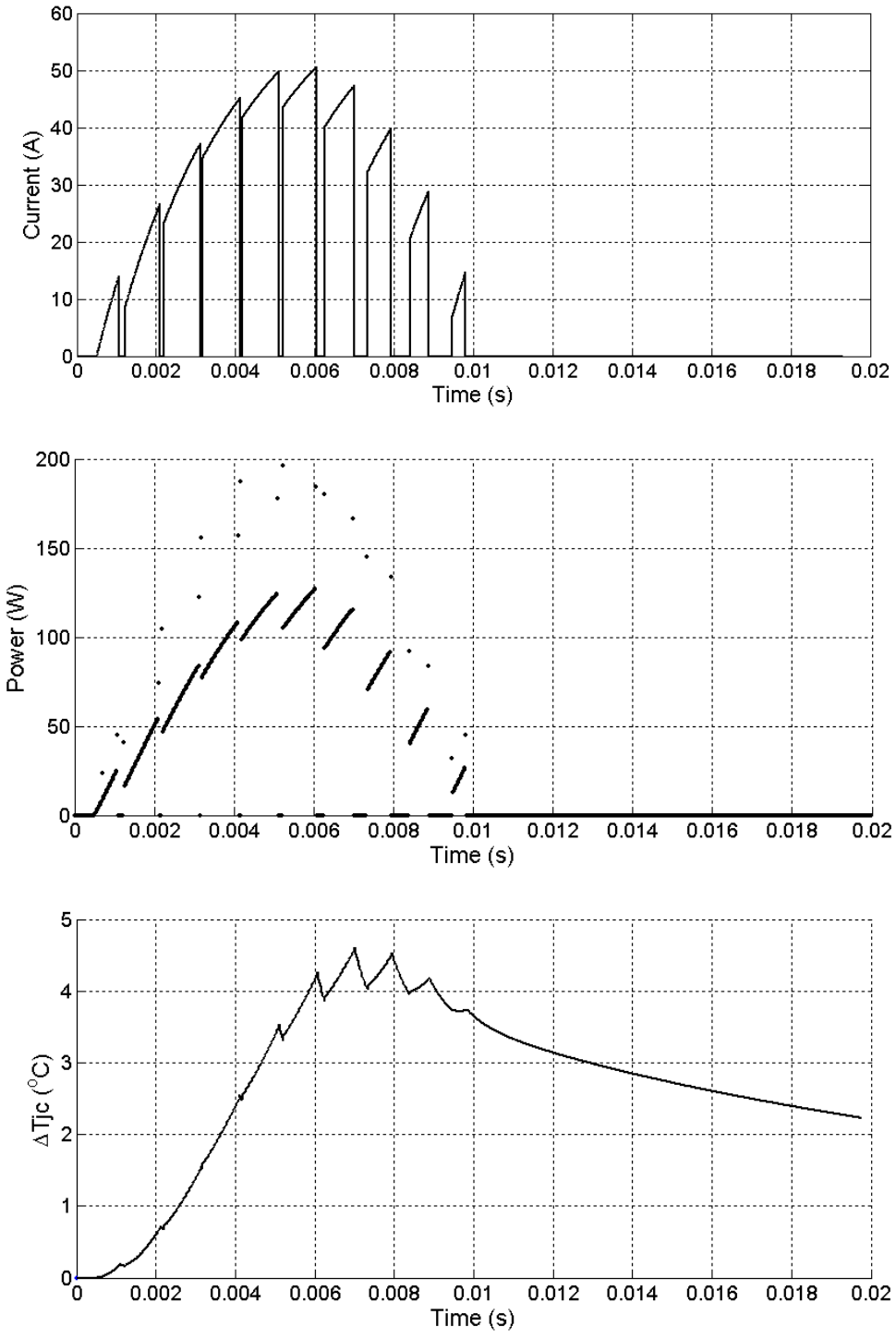


Figure 6.10 IGBT collector current, instantaneous power and ΔT_{jc} waveforms

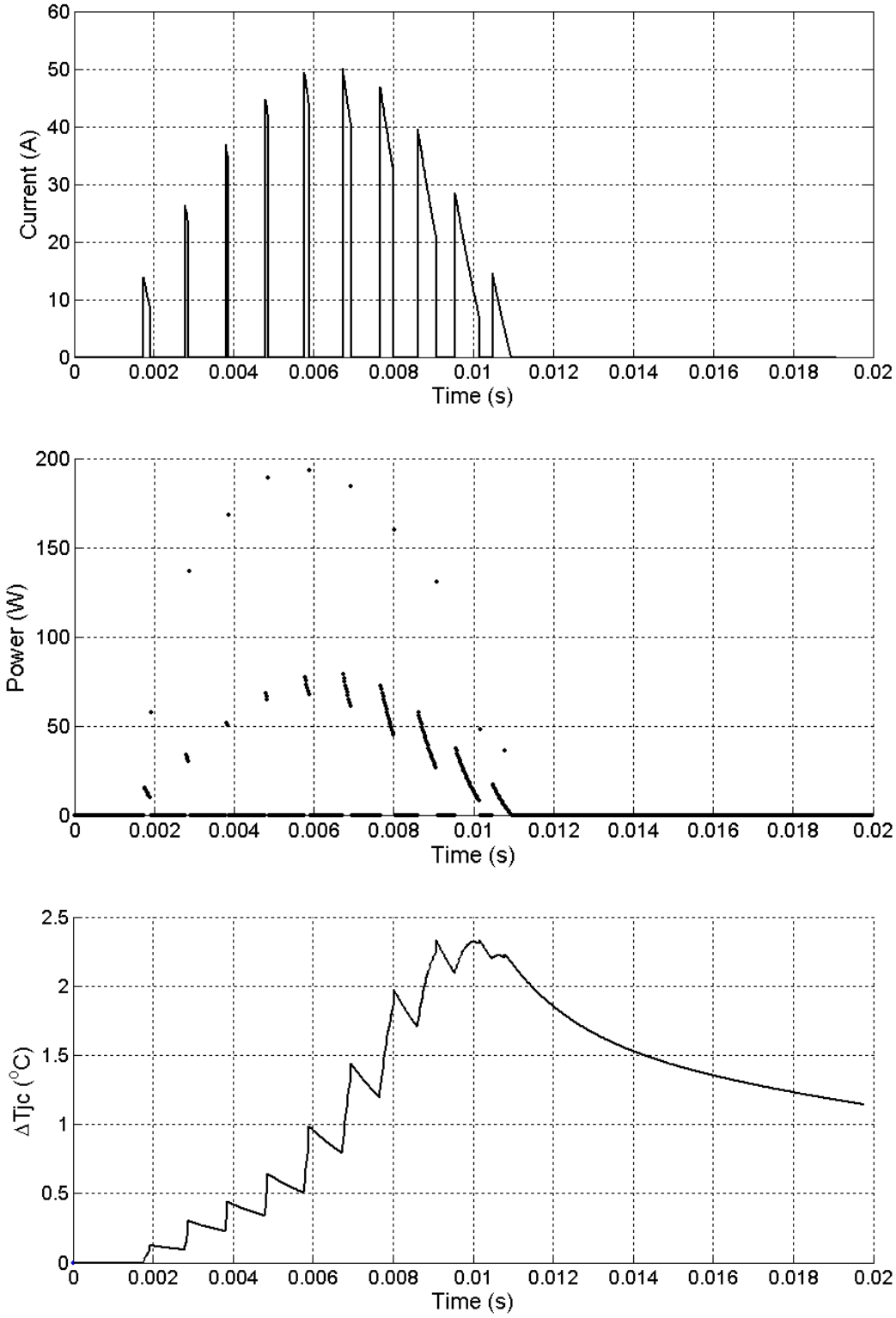
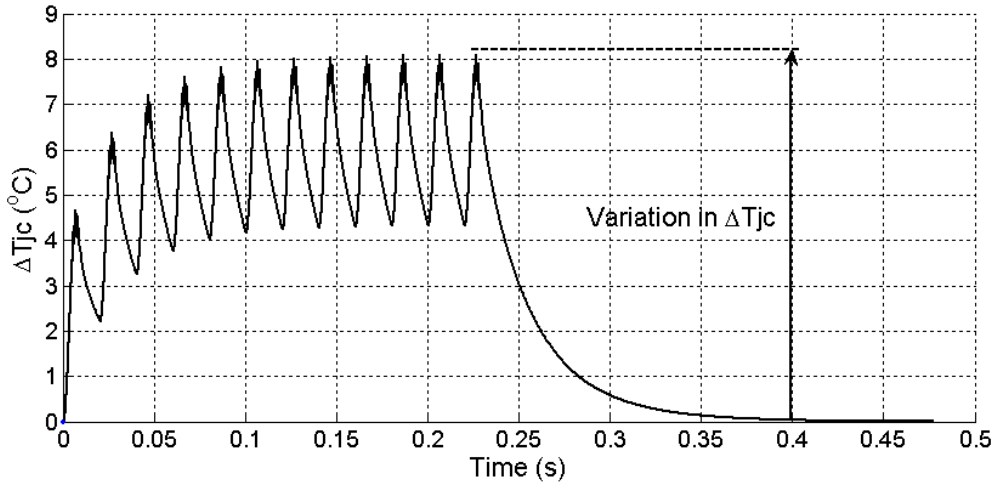
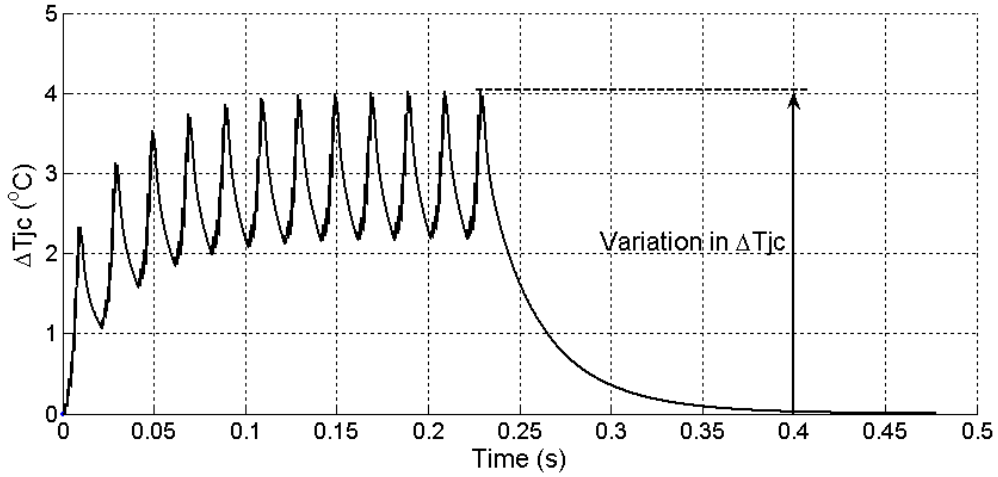


Figure 6.11 Diode anode current, instantaneous power and ΔT_{jc} waveforms



a)



b)

Figure 6.12 ΔT_{jc} waveforms for 240 ms of load current, followed by 240 ms of zero load current: a) IGBT, b) Diode

6.5 The effect of load power factor

It is well known that the load power factor affects the duration of current that the IGBTs conduct relative to the diodes. The larger the power factor, the greater the portion of the load current that is conducted by the IGBTs, and the smaller the portion that is carried by the diodes. Conversely, for lower power factors, the

diodes conduct more current and the IGBTs less. This also means that the variation in ΔT_{jc} for IGBTs is greater at larger load power factors, while that for diodes is smaller. This is illustrated for one mains cycle in Figures 6.13 and 6.14 and for one complete power cycle in Figure 6.15. A load power factor of 0.05 was used. The peak current value was kept constant at 50 A for all simulations presented in this chapter.

These figures show that the variation in ΔT_{jc} at the lower power factor is smaller for IGBTs and greater for diodes, as predicted. This mechanism may be explained as follows: the greater the power factor, the greater the load resistance and the smaller the load inductance. Therefore, more power is transferred into mechanical power or heat in the load and less is transferred back to the supply. This is illustrated by the fact that the IGBTs conduct the rising portion of the load current, i.e. the portion that is transferred to the load, and that the diodes the falling portion of the load current, i.e. the portion that is returned from the load back to the power supply. Consequently, IGBT and diode current pulses are of similar width near the peak of the load current waveform.

In contrast, switching losses are relatively unaffected by power factor. This is illustrated by the fact that there is very little difference in magnitude of the switching loss pulses of the two power factors (the simulation time step remained the same).

The variation in ΔT_{jc} after one 20 ms cycle (refer to figures 6.10, 6.11, 6.13 and 6.14) is used for all comparisons, as calculation of this figure is significantly less computation-intensive than the steady-state value.

The single-cycle variation in ΔT_{jc} for the range of load power factors from 0.05 to 0.95 and a switching frequency of 1 kHz is plotted in Figure 6.16 for IGBTs and diodes. This figure clearly shows the increase in the variation in ΔT_{jc} of the IGBTs and the decrease for diodes. This effect is approximately linear for both devices and is more pronounced for diodes.

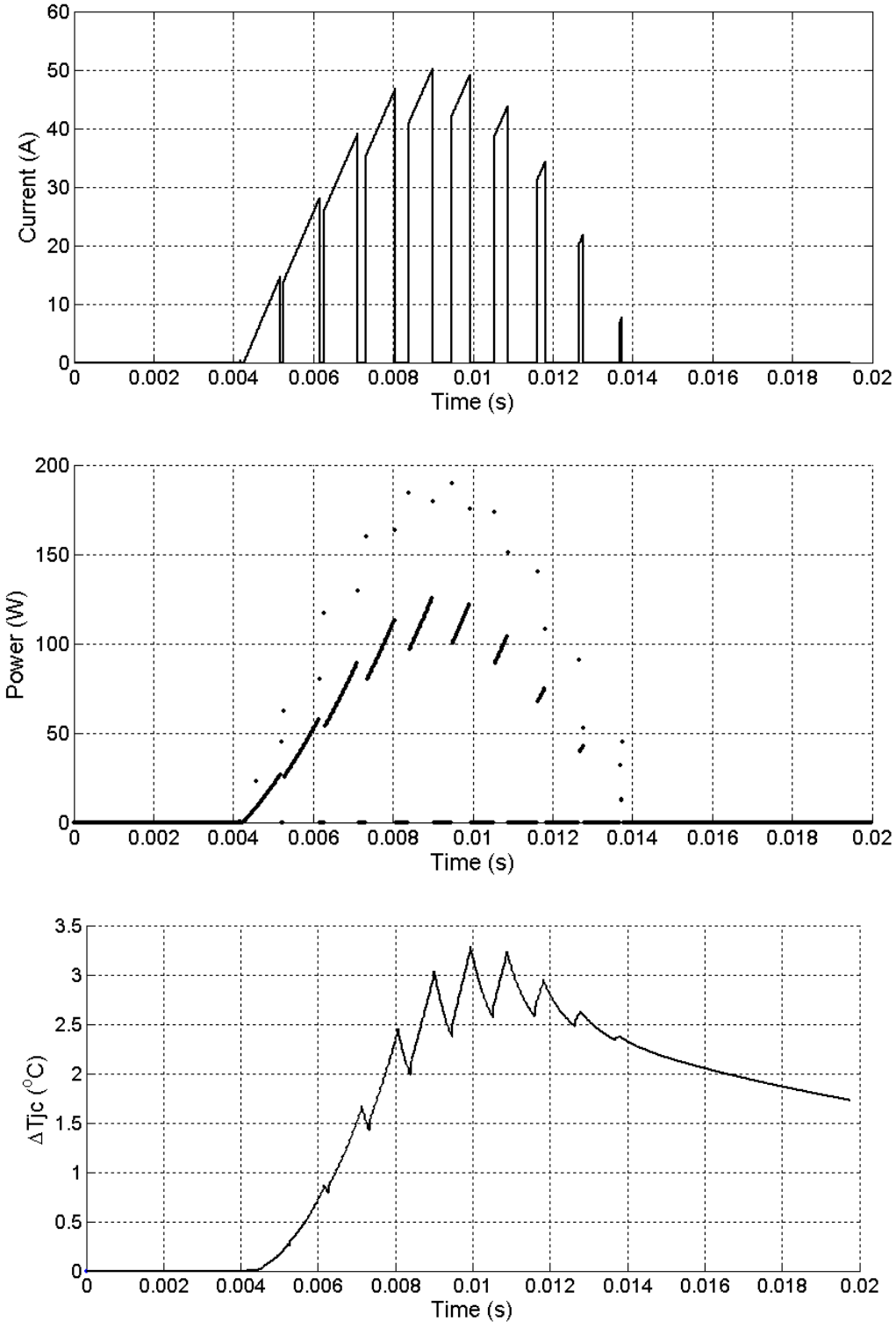


Figure 6.13 IGBT collector current, instantaneous power and ΔT_{jc} waveforms for a load power factor of 0.05

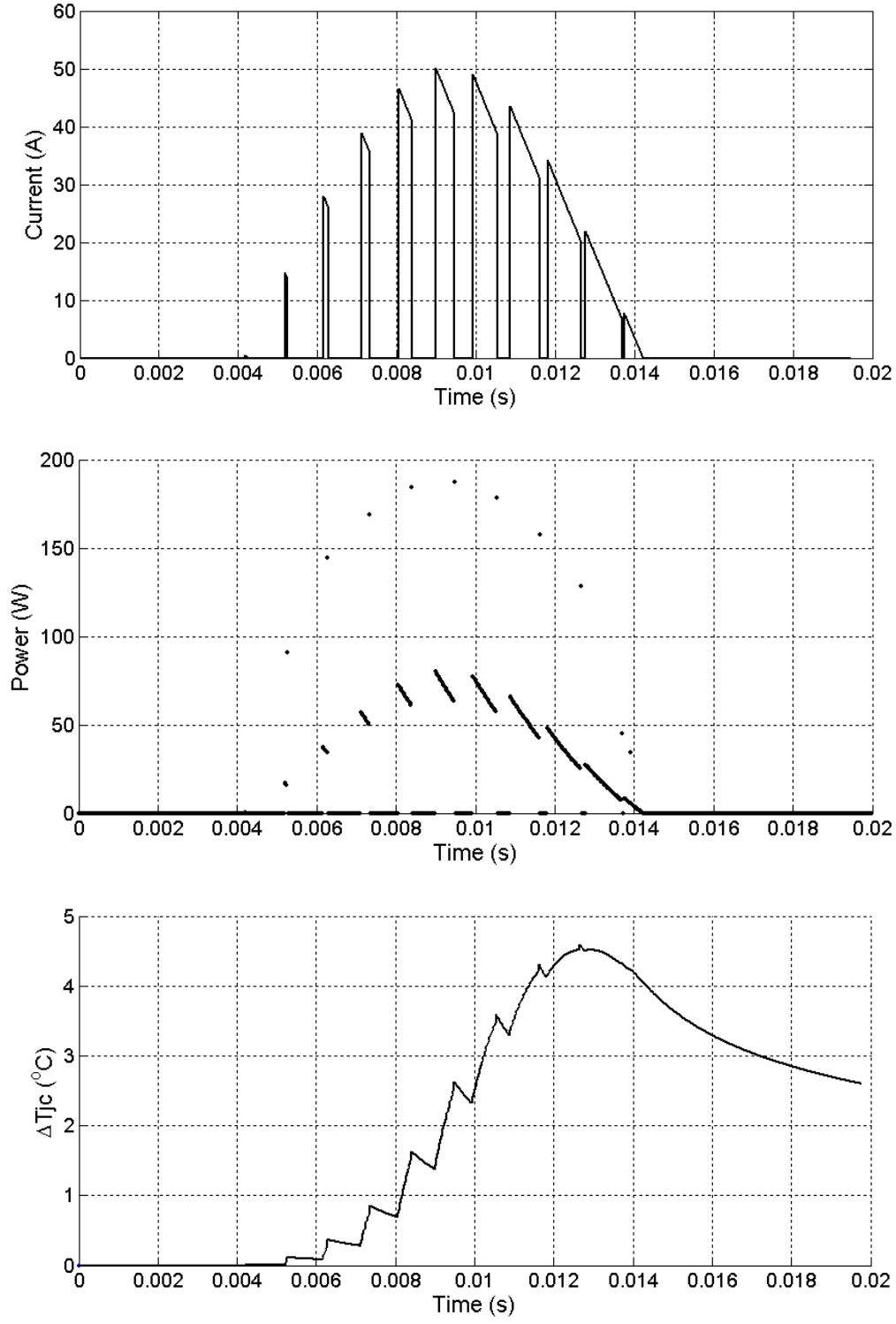


Figure 6.14 Diode anode current, instantaneous power and ΔT_{jc} waveforms for a load power factor of 0.05

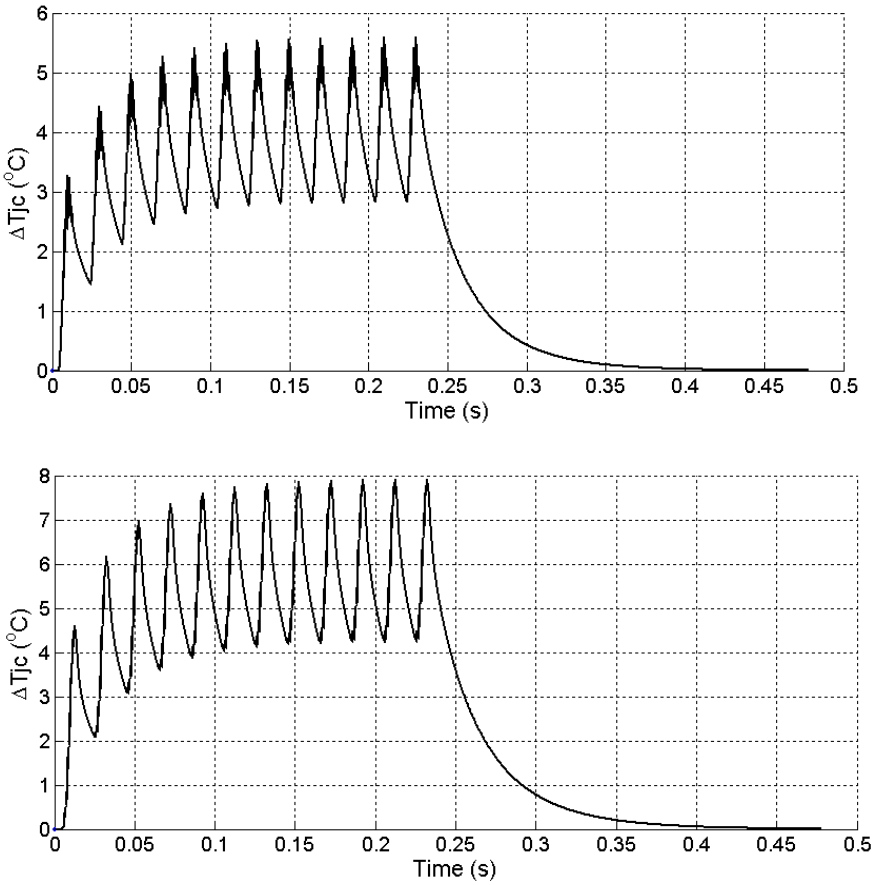


Figure 6.15 ΔT_{jc} waveforms for $t_{on} = t_{off} = 240$ ms for a load power factor of 0.05: IGBT (top) and diode (bottom)

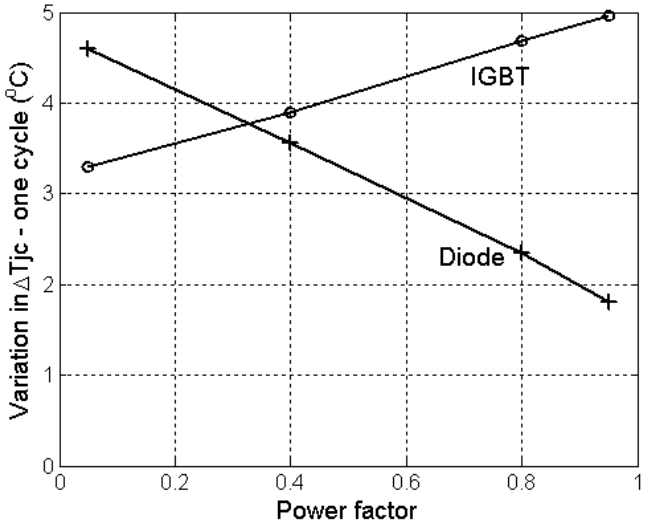


Figure 6.16 Variation in ΔT_{jc} after one 20 ms cycle as a function of load power factor for a switching frequency of 1 kHz

6.6 The effect of switching frequency

Inverters in the 20-100 kW range generally operate at switching frequencies of 2-4 kHz. Therefore, the variation in ΔT_{jc} for PWM switching frequencies in a similar range was determined. To illustrate the effect of switching frequency, instantaneous current, power loss and ΔT_{jc} waveforms for a load power factor of 0.8 and a switching frequency of 5 kHz are shown in Figure 6.17 for IGBTs and in Figure 6.18 for diodes.

The higher switching frequency means that switching occurs more frequently, resulting in a load current waveform that is more sinusoidal. There are also more frequent switching loss pulses – the highest envelope in Figure 6.17 is turn-on loss, the second is turn-off losses and the lowest is conduction loss. The magnitude of the conduction loss pulses is unchanged from 1 kHz, whereas the switching loss pulses are larger. The latter is due to a shorter simulation time step at 5 kHz (refer to Section 6.1.2), due to the greater resolution required at the higher switching frequency. The ΔT_{jc} waveforms also increase faster and are smoother due to the more frequent switching operations.

The effect of switching frequency on the variation in ΔT_{jc} is shown in Figure 6.19 for a load power factor of 0.8. Switching frequency has a significant effect, this effect is linear.

6.7 Complete characterization of the circuit

The effect of both switching frequency and power factor on the variation in ΔT_{jc} is shown in Figure 6.20. Both single-cycle and steady-state values are plotted. The following observations may be made from these figures:

1. For both devices the variation in ΔT_{jc} increases linearly with switching frequency, irrespective of the load power factor.
2. The increase in the single-cycle variation in ΔT_{jc} from 1 kHz to 5 kHz falls between 27% and 43% for IGBTs, and between 47% and 120% for diodes. In both cases the larger increases are for the lower curves, i.e. at lower

power factors for IGBTs and at higher power factors for diodes. This is because the conduction losses are lower and hence the increase in switching losses has a greater effect on the total losses.

3. Switching frequency has a significantly greater effect for diodes because they have significantly lower conduction losses.
4. There is a slightly greater separation between diode curves than between IGBT curves. This is because power factor has a slightly greater effect on the diode temperature rise, as shown in Figure 6.16.
5. The magnitude of the steady-state variation in ΔT_{jc} of both IGBTs and diodes is significantly less than the 40°C stated in the literature as the limit below which aging due to power cycling is insignificant for DC power cycling (refer to Section 3.1). Increasing the load current magnitude would increase the variation in ΔT_{jc}. However, this would result in the devices being operated outside their normal limits. Also, using devices with higher switching losses would increase the variation in ΔT_{jc}.

Average power loss components and average current are shown in Figure 6.21 for IGBTs and Figure 6.22 for diodes. The following observations can be made from these figures:

1. The first graphs show that average total losses of both devices have the same form as the variation in ΔT_{jc}, as expected.
2. The second graphs show that the switching losses of both devices are independent of load power factor.
3. The third graphs show that the conduction losses of both devices are relatively independent of switching frequency. This is because the average current (the final graphs) has the same form.

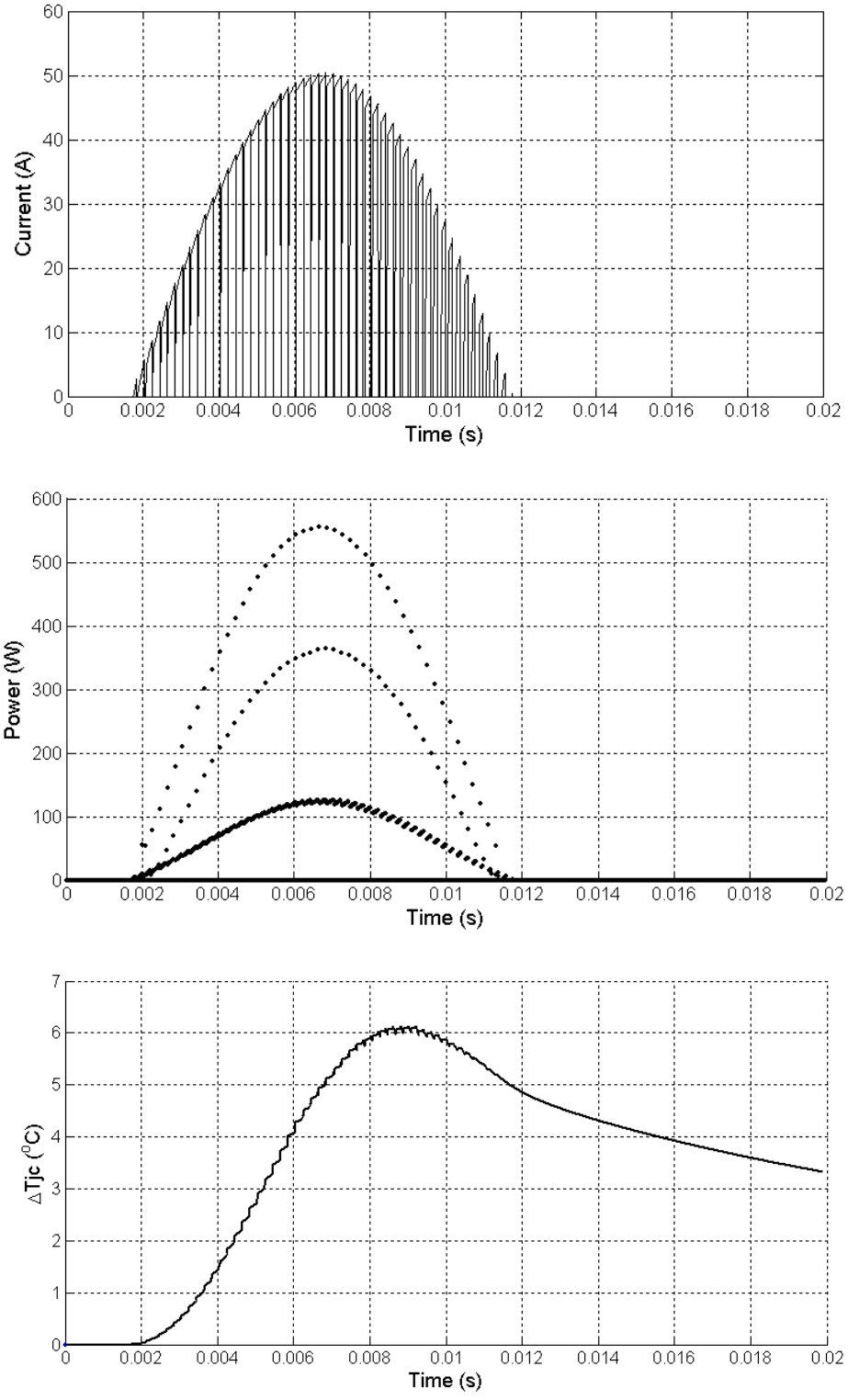


Figure 6.17 IGBT collector current, instantaneous power and ΔT_{jc} waveforms for a load power factor of 0.8 and a switching frequency of 5 kHz

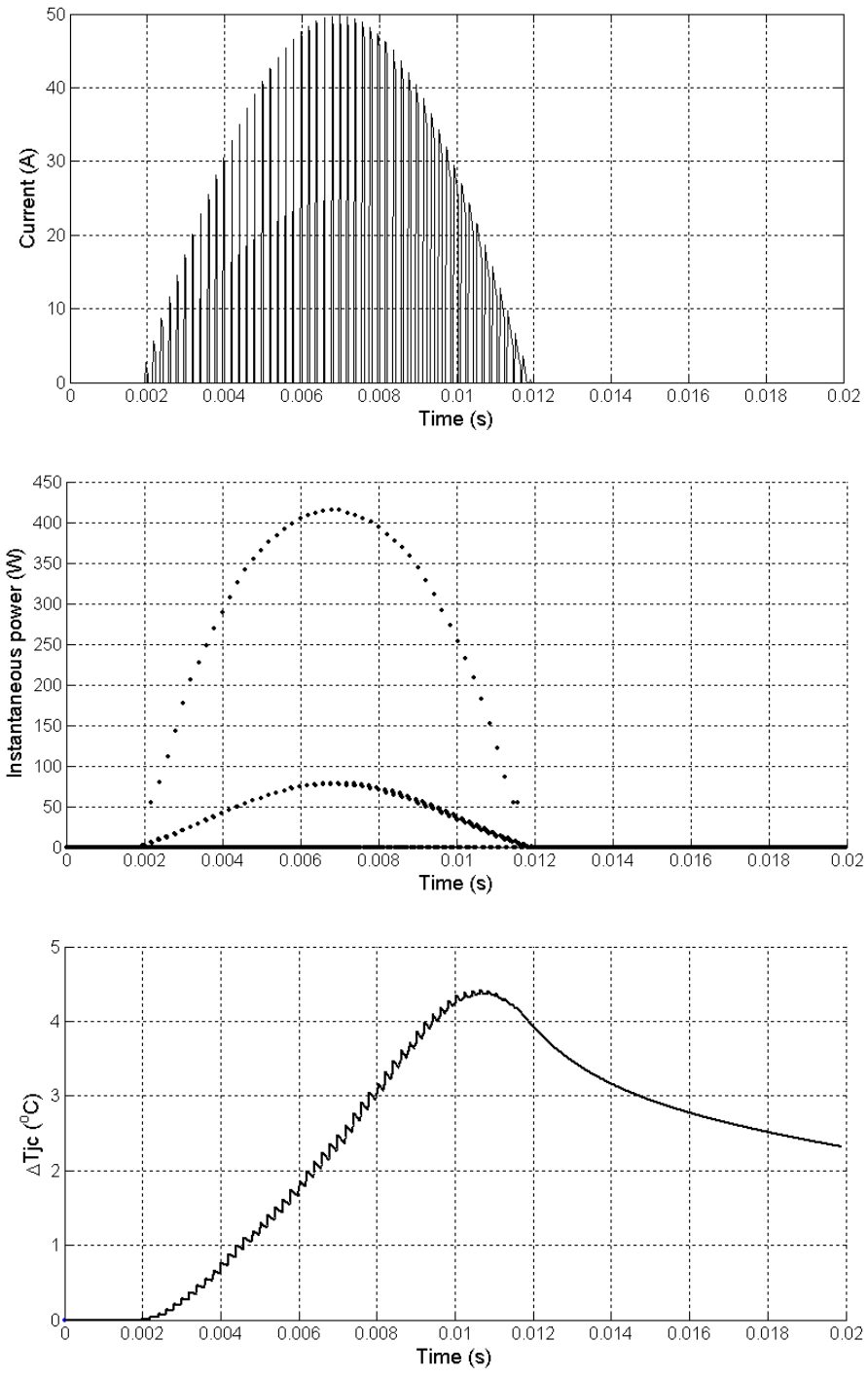


Figure 6.18 Diode anode current, instantaneous power and ΔT_{jc} waveforms for a load power factor of 0.8 and a switching frequency of 5 kHz

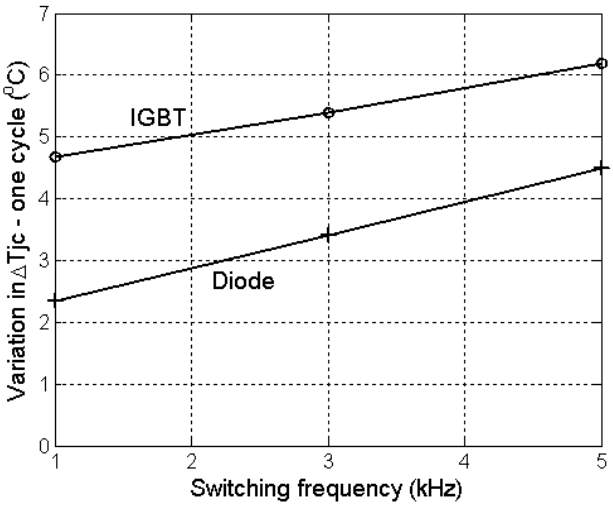
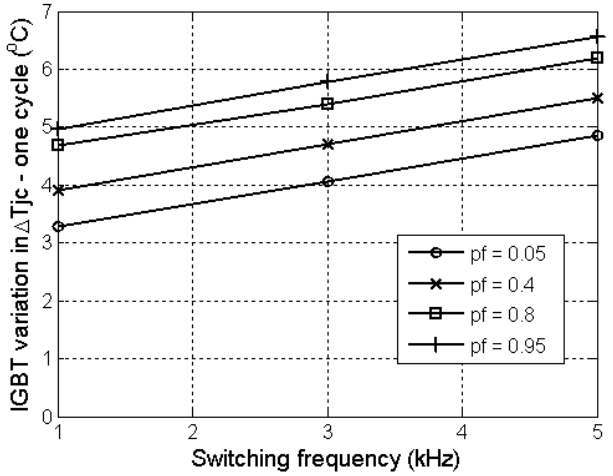
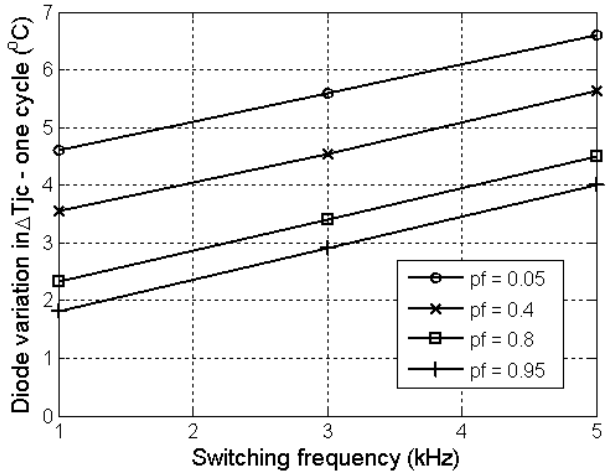


Figure 6.19 Variation in ΔT_{jc} as a function of switching frequency (0.8 power factor)





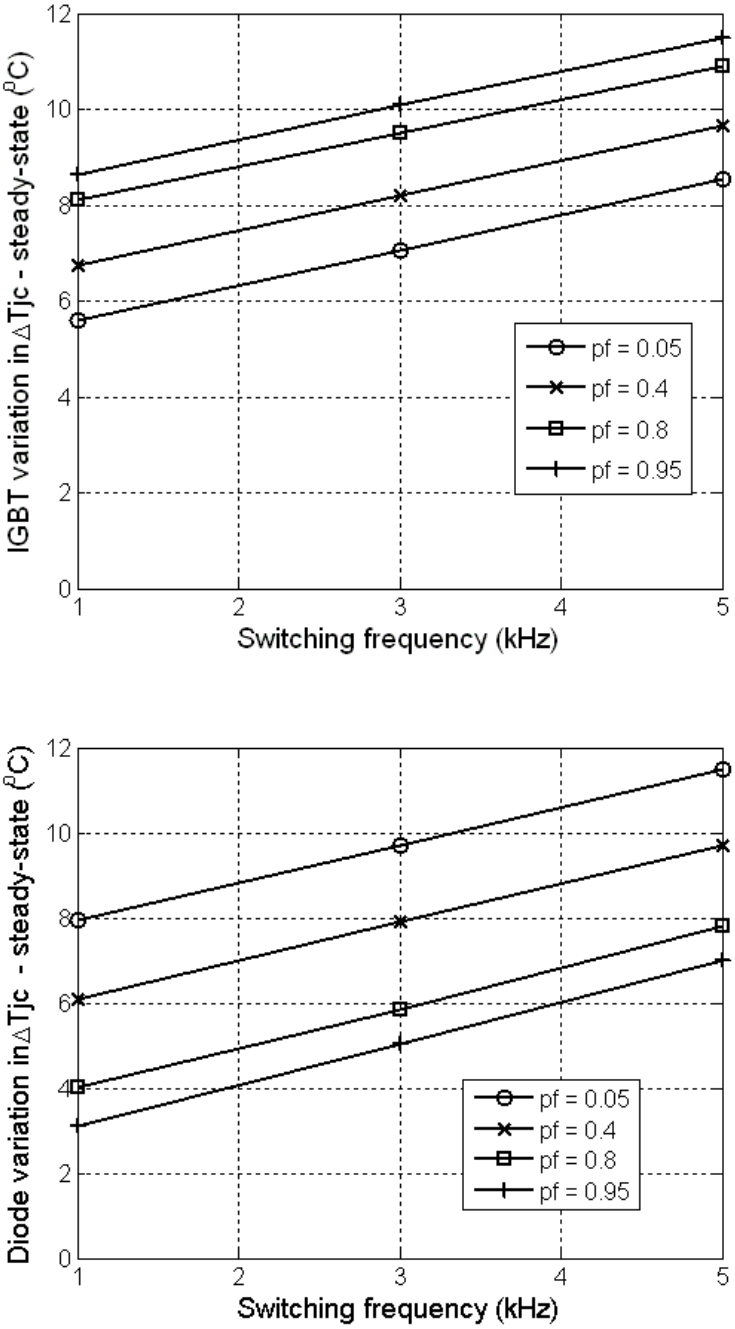
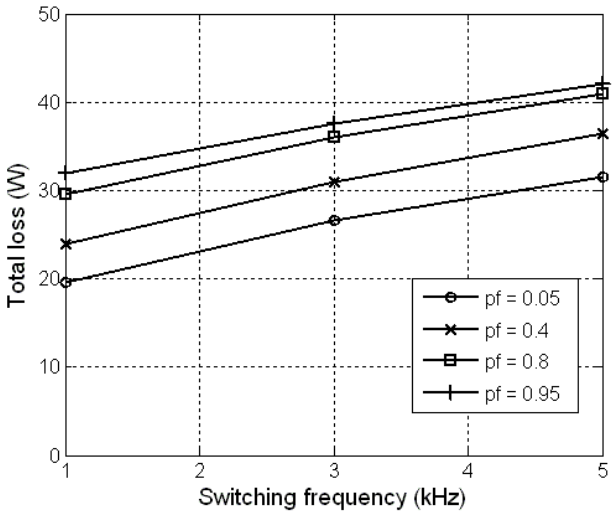
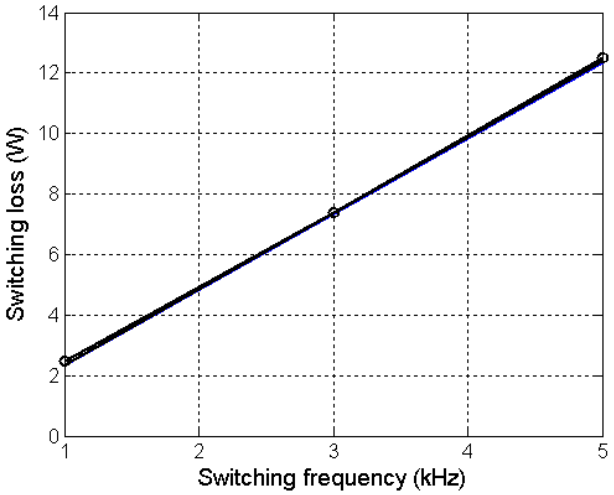
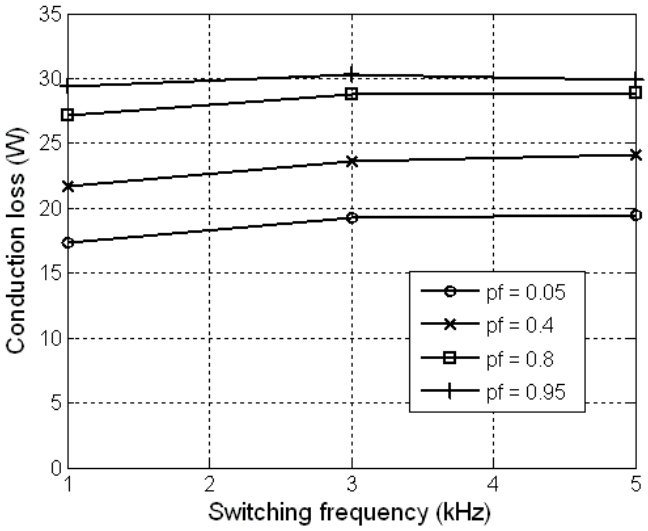


Figure 6.20 Variation in ΔT_{jc} as a function of load power factor and switching frequency for IGBTs and diodes: one cycle (top) and steady-state (bottom)


Total loss (W)
Switching frequency (kHz)
pf = 0.05
pf = 0.4
pf = 0.8
pf = 0.95


Switching loss (W)
Switching frequency (kHz)


Conduction loss (W)
Switching frequency (kHz)
pf = 0.05
pf = 0.4
pf = 0.8
pf = 0.95

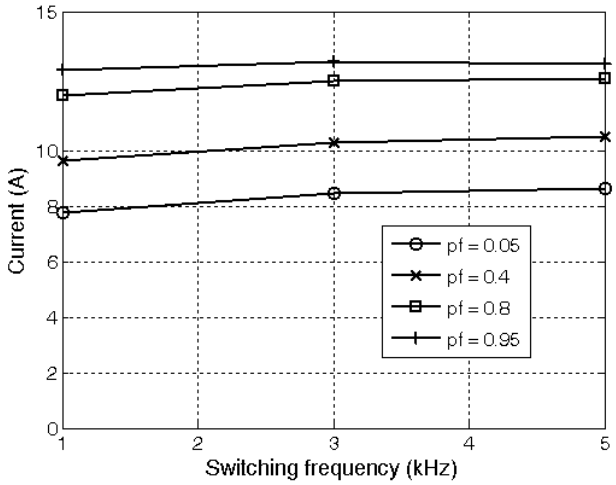
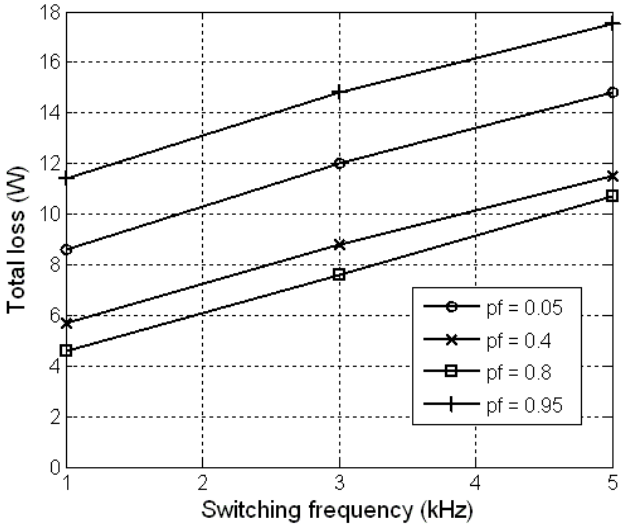
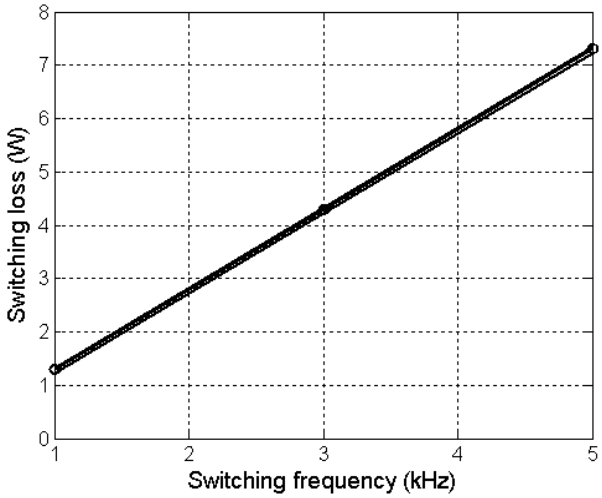


Figure 6.21 Average loss components and average current for IGBTs





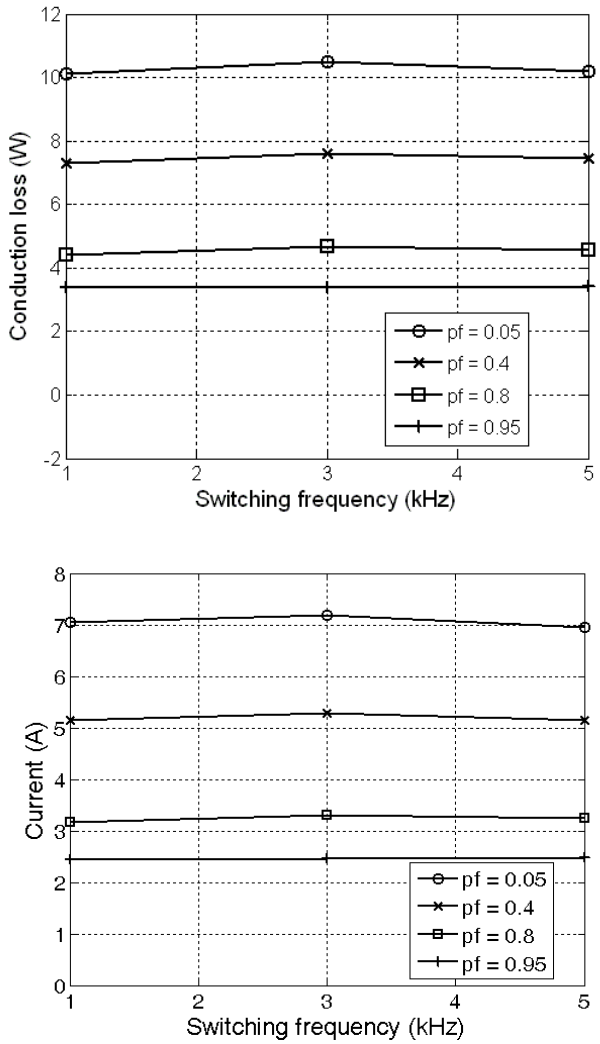


Figure 6.22 Average loss components and average current for diodes

6.8 Comparison with previous studies

Two relevant studies have been performed previously. Although these studies do not duplicate the simulations performed above, comparison with the methods and results of these studies serves to validate the results obtained here.

6.8.1 Yun [70]

In Section 3.4.2 of [70], Yun studied the effect of pulsed power dissipation in an IGBT. The power dissipation and ΔT_{jc} were calculated for IGBTs and diodes used

in a PWM inverter. The calculation method was similar to that used here. However, the loss at each point was calculated by multiplying the voltage and current at that point – the conduction and switching losses were not calculated separately. The *SOLIDIS* software package [73] was used.

A typical IGBT ΔT_{jc} waveform for three mains cycles (60 ms) is shown in Figure 6.23. The shape of the waveform is similar to those obtained here, for a higher switching frequency, e.g. that of Figure 6.17. The author does not state the value of the switching frequency or the load power factor used.

The advantage of Yun's calculation method is that it is simple because the voltage and current values at each point are simply multiplied together to obtain the total power loss. This does, however, mean that the model of the IGBT or diode used to obtain the voltage and current waveforms must be of good quality and the time step must be very small, increasing computation time.

Conversely, the advantage of the method used in this study is that the current waveform only is needed and this can be easily obtained without the need for an accurate IGBT or diode model. The device conduction voltage drop and switching loss are determined from the manufacturer's data. This means that the manufacturer's data needs to be accurate.

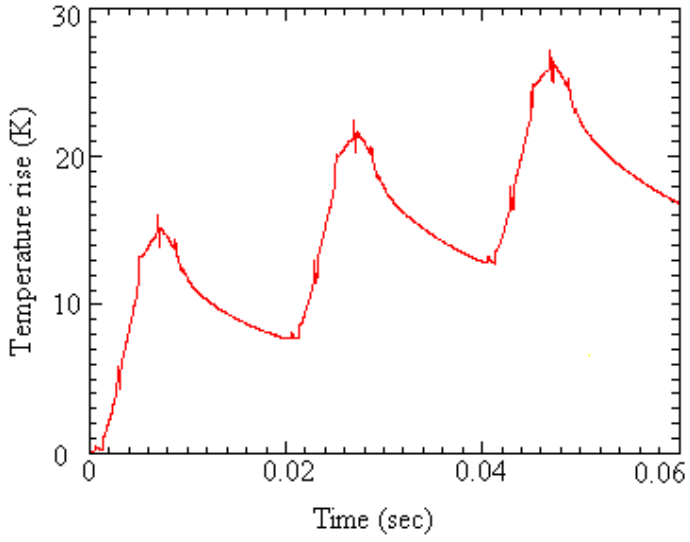


Figure 6.23 Typical simulated IGBT ΔT_{jc} waveform obtained by Yun [70]

6.8.2 Mantooth et al [72]

A typical H-bridge was simulated using the *Saber* software package [74]. *Saber* is an integrated electro-thermal package with a physics based electrical IGBT model and built-in thermal models of typical packages. The IGBTs were housed in a TO-247 package (refer to Section 2.3.4), but their ratings were not given. The load had a power factor of 0.998 and the peak current was approximately 18 A. The DC link voltage was 300 V.

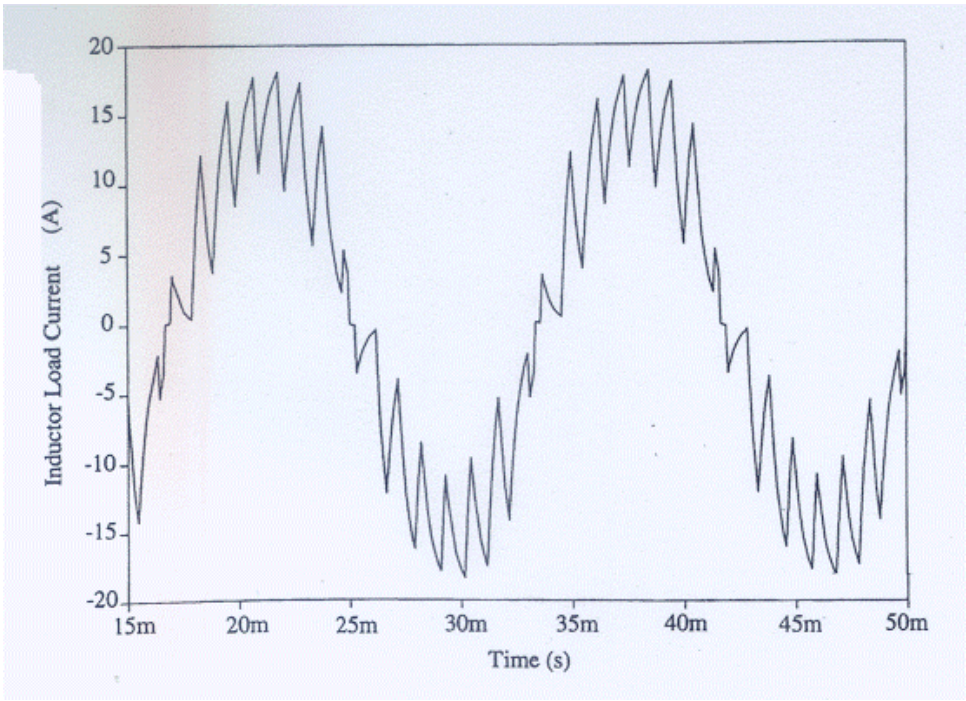
The load and IGBT current waveforms for a switching frequency of 900 Hz are shown in Figure 6.24. These are similar to the waveforms obtained here for a load power factor of 0.8 and a switching frequency of 1 kHz (refer to Figure 6.9). The differences can be attributed to the difference in load power factor and control strategy, as well as differences in the device models.

The IGBT ΔT_{jc} waveform obtained for a switching frequency of 20 kHz is shown in Figure 6.25. This is a steady-state waveform, therefore the envelope is not rising with each mains cycle. There are substantial temperature transients, which were not obtained in this study. This could be due to the differing transient thermal impedance (magnitude and time constant) of the smaller package. Operating the device at its maximum current rating (c.f. 50% used here) could also contribute to this effect. No device ratings were given by the authors.

6.9 Conclusions

A typical single phase H-bridge has been completely characterized. The load, IGBT and free-wheeling diode current waveforms were presented. The power loss and ΔT_{jc} waveforms were then calculated. These calculations were performed for the entire range of load power factors, and for switching frequencies up to 5 kHz.

The variation in ΔT_{jc} was previously identified as the most important parameter for power cycling reliability. The performance of the new test circuit will be compared with these results, with particular emphasis on the variation in ΔT_{jc}.



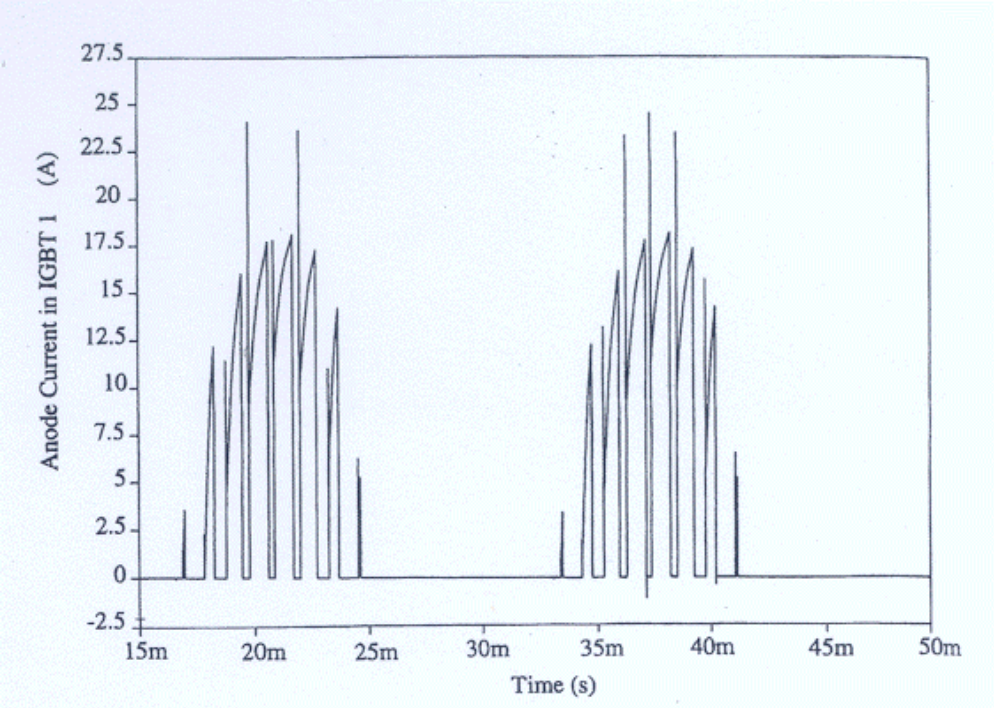


Figure 6.24 Load and IGBT current waveforms obtained by Mantooth et al [72]

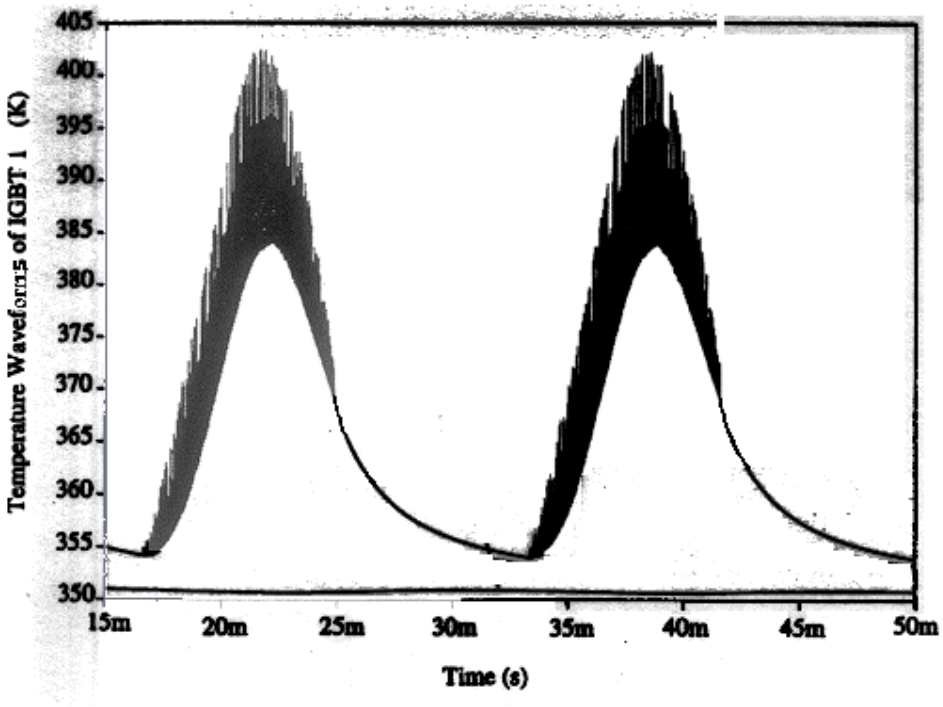


Figure 6.25 IGBT ΔT_{jc} waveform obtained by Mantooth et al [72]

7. THE MODIFIED H-BRIDGE

This chapter presents the test circuit and the reasons for choosing it. Its operation is explained by simulation and its performance is compared to the conventional circuit.

7.1 The circuit and its operation

7.1.1 Circuit requirements

The suitability of a test circuit must be compared to the criteria of Section 5.2. The conventional H-bridge with a high power factor load (0.8 to 0.95 [32, 33, 75]), replicates the stresses of a typical single or three phase inverter. Therefore, the first three criteria are met as switching losses are included, both IGBTs and diodes are tested and the setup is as simple as possible. If only connections to the chips are to be tested – as is most often the case (see Section 3.2) – then cycling time can be as short as the time constant of Z_{thjc} allows. This time constant is about 30 ms for both IGBTs and diodes, resulting in the Z_{thjc} curves of both devices reaching steady-state in about 240 ms (Figures 6.12 and 6.15). The minimum value of t_{on} and t_{off} is therefore 240 ms. Maximum values are not set, they can be as large as needed by other parameters. Also, they are not necessarily equal. The shortest cycling time possible with the conventional circuit is therefore 480 ms – the shortest possible – meeting the fifth criterion. The final criterion is also met as the current magnitude and waveform, and hence the variation in ΔT_{jc}, are representative of field conditions.

However, the high power factor load would result in large power losses in the load and hence in large operating costs, resulting in the fourth criterion not being met. To reduce these losses, a mainly inductive load was to be used. However, device stresses would then be different to the high power factor load case (see Figure 6.20). Several other changes were therefore needed to the circuit. These are explained below, followed by the simulation method and results.

The most important parameter in comparing the conventional and modified circuits is the variation in ΔT_{jc}, as shown in Chapters 3 and 4. The target values of this parameter are those that would be obtained for a conventional 20-100 kW inverter. A typical switching frequency is 2 to 4 kHz. From Figure 6.20, the single-cycle variation in ΔT_{jc} for a 0.8 to 0.95 power factor load is therefore 5.1 to 6.1 °C for IGBTs and 2.3 to 3.9 °C for diodes.

7.1.2 Description of the circuit

The conventional single-phase inverter of Figure 6.7 was modified to give the circuit of Figure 7.1. The original IGBTs (e1, e2, g1 and g2 in Figure 7.1) and free-wheeling diodes (a2, b2, c2 and d2) were kept. The same IGBTs as the conventional case were used (Semikron SKM 100 GB 123D). The free-wheeling diodes of the same IGBT module were used for their soft reverse-recovery characteristics. Additional IGBTs (f1, f2, h1 and h2) were placed in series with the free-wheeling diodes. This is so that these IGBTs may also be significantly stressed, because the inductive load means that reverse-connected devices are stressed more than at higher power factors (as shown in the previous chapter).

Implementation of this circuit would result in all IGBTs having extra anti-parallel diodes in the circuit – those of smaller size in Figure 7.1. This was not envisaged to be a problem for the reverse-connected IGBTs (f1, f2, h1 and h2) as their series diodes (a2, b2, c2 and d2) would prevent current flow through the extra diodes. However, no diodes were present in series with the forward-connected IGBTs (e1, e2, g1 and g2). These therefore had to be added (diodes a1, b1, c1 and d1).

The circuit was therefore divided into modules as shown. This meant that the diodes had extra anti-parallel IGBTs – those of smaller size in the figure. These would be permanently turned off in practice and were hence ignored in the simulations.

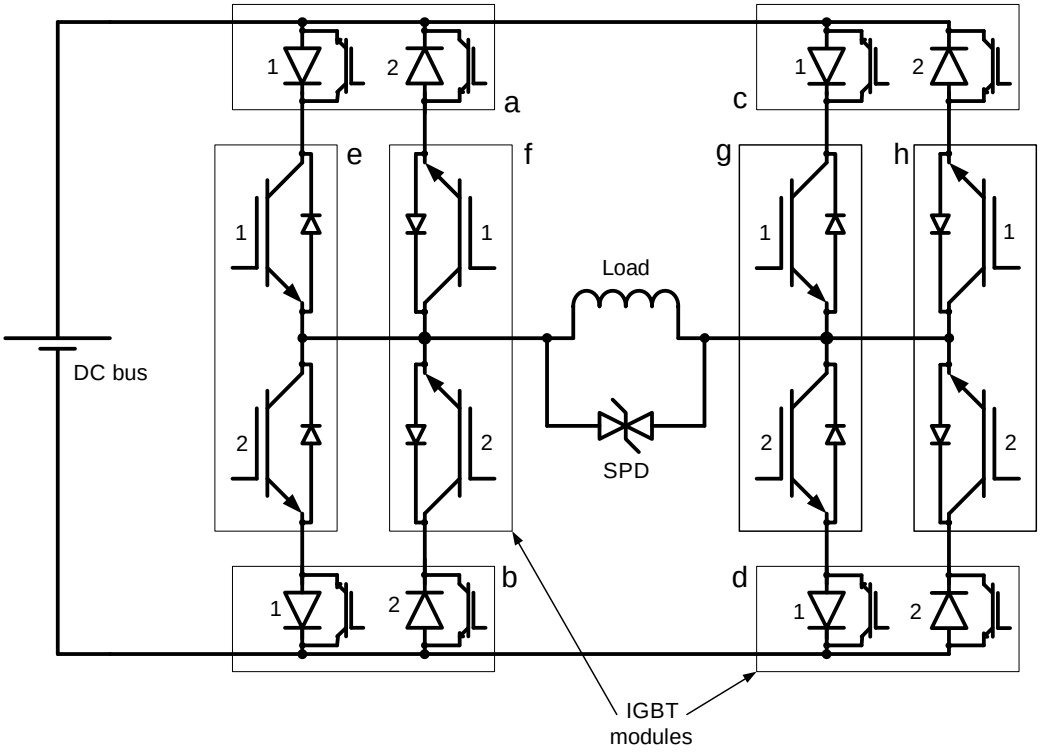


Figure 7.1 Test circuit

7.1.3 Simulation method

The circuit was modeled in Simulink. All IGBTs and diodes were modeled in the same way as in the previous chapter. Several other modifications were made to the circuit because when implemented, it would have significantly larger physical size than a conventional inverter, which was expected to result in sizeable transient switching voltages. Protection was to be provided in two forms: series RC snubbers placed in parallel with all devices (not shown in Figure 7.1 for clarity); and a surge protective device (SPD) mounted in parallel with the load.

The snubber values were 10 Ω and 100 nF. The resistor value was chosen to be as low as possible to provide as much dv/dt protection for the devices as possible, but not too low to prevent excessive snubber capacitor discharge current from flowing through the devices during turn-on [29]. The snubber capacitor value is recommended by the manufacturer as a DC bus snubber in conventional circuits.

The purpose of the load SPD is to clamp any voltage transients above a certain level. It consisted of three 275 V, 10 kA silicon avalanche diodes (SADs) in series. Three SAD samples of this rating were chosen because each sample has a clamping voltage of approximately 420 V at low current levels. Therefore, three samples have a clamping voltage of about 1.3 kV. Since there are always at least two blocking devices in series, this would prevent overstressing the individual devices. The SADs were modeled as a single metal oxide surge arrester with a clamping voltage of 1.3 kV.

SADs were chosen over more conventional metal oxide varistors (MOVs) for the following reasons [28]:

1. They limit surge voltage to a lower level.
2. The clamping voltage is more consistent between different samples.
3. SADs do not age significantly if their ratings are not exceeded, while MOVs are known to age with each transient conducted. The large number of voltage transients expected – at each PWM switching operation – therefore made SADs more suitable for this application.

Other simulation settings were:

- The load was modeled as a pure inductance of 10 mH. This value was readily obtainable in the laboratory.
- The DC bus voltage was set at 160 V to give a peak load current of 50 A.
- A 9 mF smoothing capacitor was placed across the DC bus.
- A dead time was included, due to the relatively slow turn-off expected to be caused by stray inductance when the circuit is implemented. The largest value possible with the gate driver to be used (Semikron SKHI 23/12 [71]) – 10 μs – was chosen.
- IGBT turn-on and turn-off times were controlled to meet the values of the data sheet (approximately 70 ns for both). This was achieved by controlling the time taken for the resistance to change from a state of high resistance to low resistance for turn-on, and vice versa for turn-off.

7.1.4 Simulation results

Load voltage and current for a switching frequency of 1 kHz are shown in Figure 7.2. The current waveform is similar to the conventional case (Figure 6.9). However, it is smoother, due to the lower power factor (as shown by the device waveforms of Figures 6.13 and 6.14). The voltage waveform is also similar to the conventional case, with the exception of the large switching transients. These are limited by the SAD to about 1.3 kV.

Waveforms for individual devices are shown for IGBTs in Figure 7.3 and for diodes in Figure 7.4. Forward-conducting devices are IGBTs e1, e2, g1 and g2 and diodes a1, b1, c1 and d1. Reverse-conducting devices are IGBTs f1, f2, h1 and h2 and diodes a2, b2, c2 and d2. The device current waveforms are similar to the conventional case (Figures 6.13 and 6.14), with the exception of the large transients during turn-on. The voltage waveforms are similar to the load voltage waveform, with the exception of the large transients during switching and that their magnitude is significantly larger than the DC bus voltage.

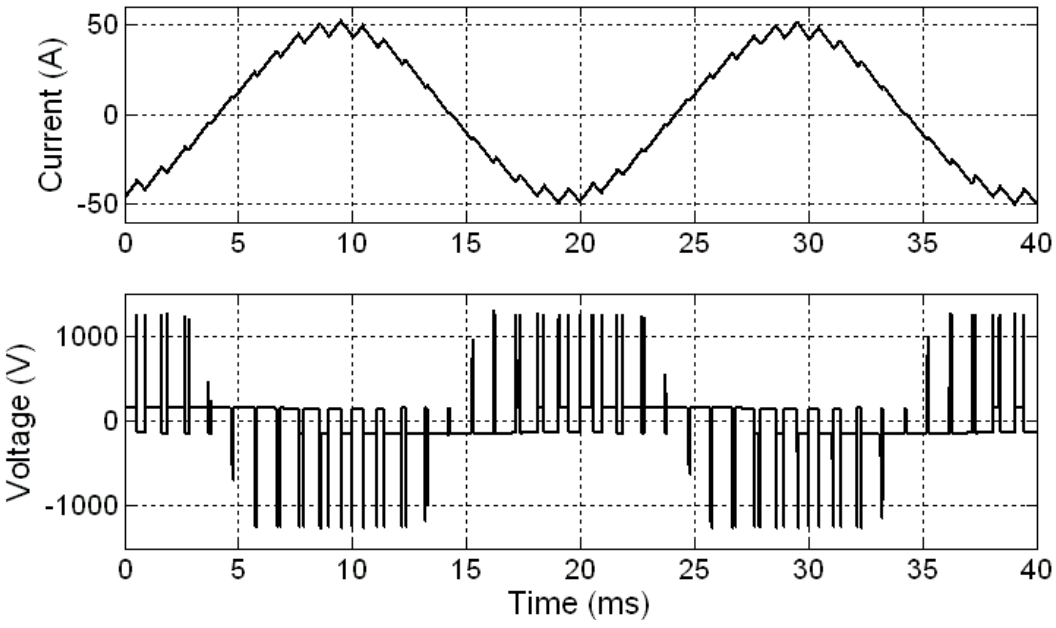


Figure 7.2 Simulated load current (top) and voltage (bottom) waveforms

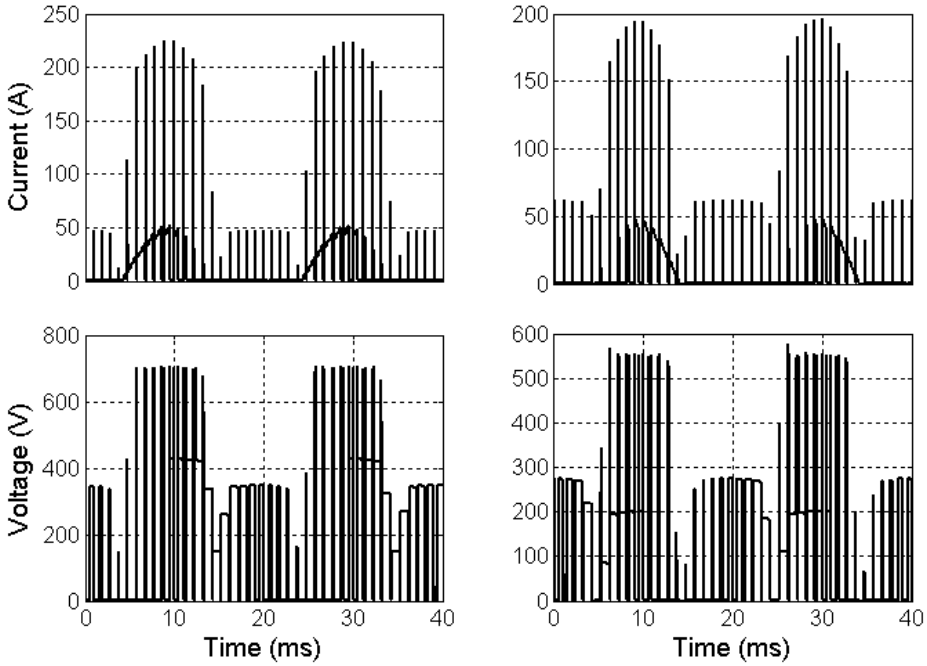


Figure 7.3 IGBT voltage and current waveforms: forward-conducting (left) and reverse-conducting (right)

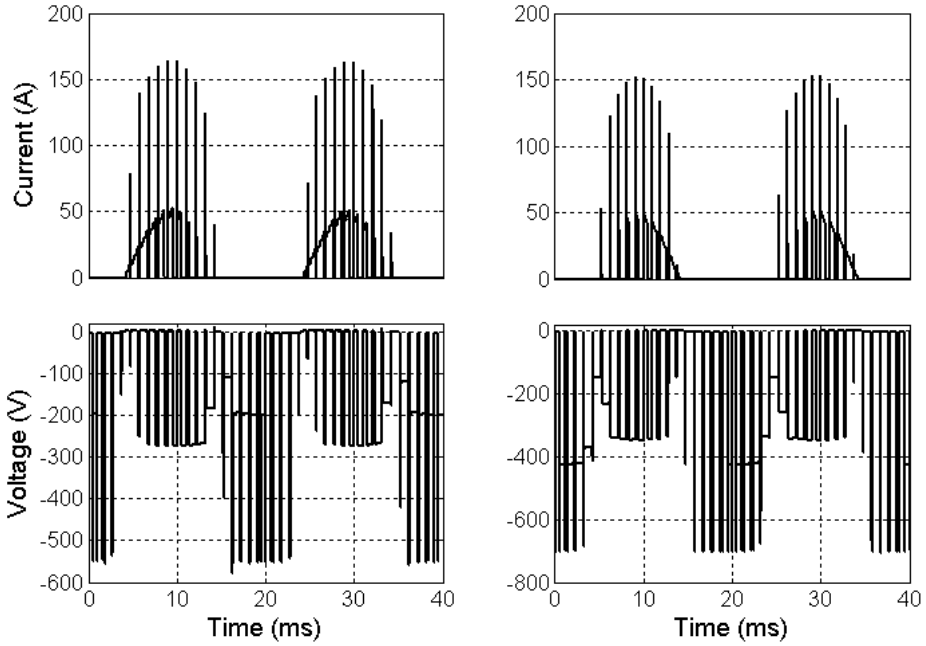


Figure 7.4 Diode voltage and current waveforms: forward-conducting (left) and reverse-conducting (right)

The origin of the transients is explained by studying the switching waveforms. First, turn-on is considered, as shown in Figure 7.5. The principle is the same for forward and reverse-conducting devices, therefore only forward-conducting devices will be looked at.

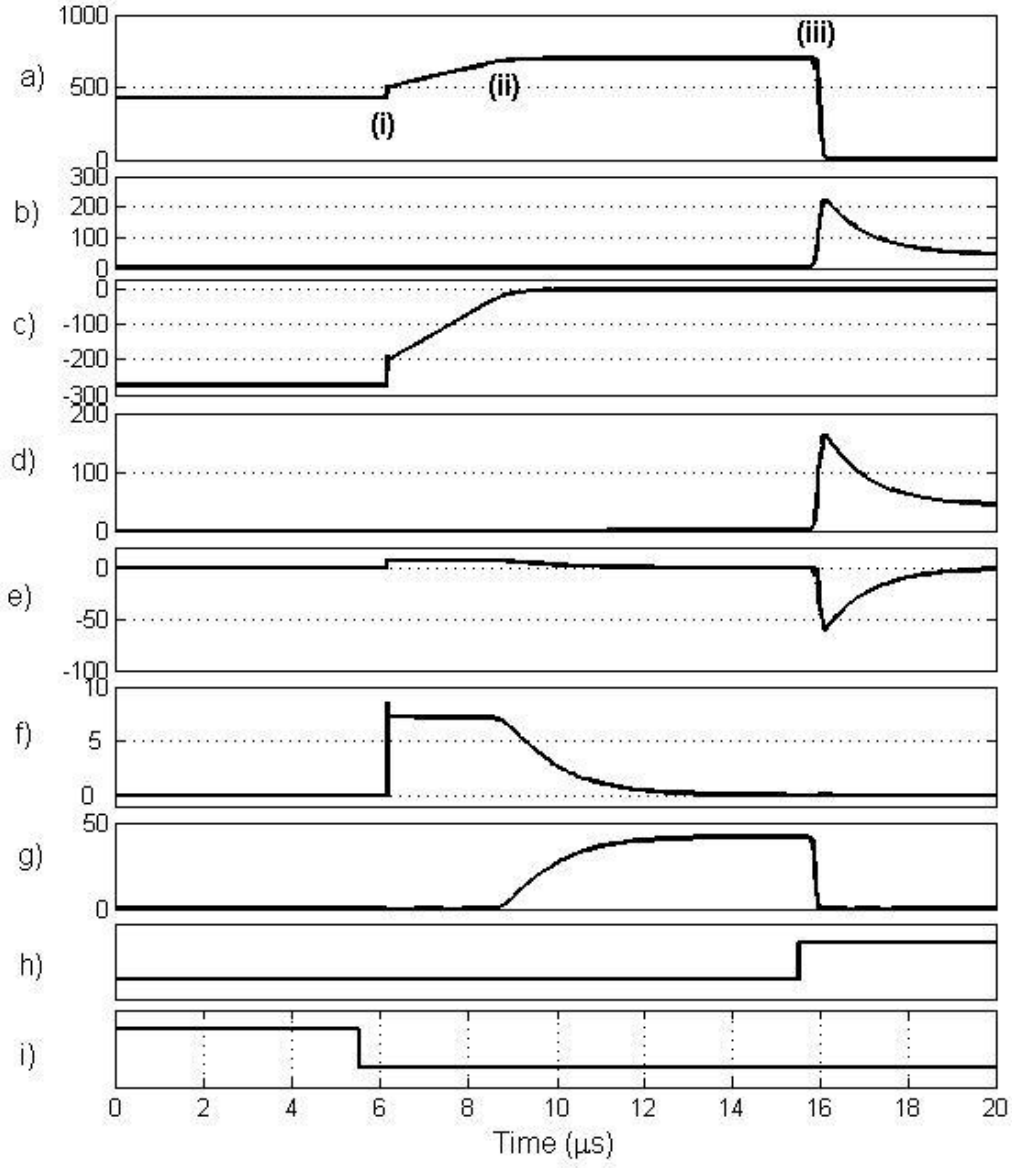


Figure 7.5 Forward-conducting device waveforms during turn-on: a) IGBT voltage, b) IGBT current, c) series diode voltage, d) series diode current, e) IGBT snubber current, f) series diode snubber current, g) SAD current, h) IGBT gate signal, i) turning off IGBT gate signal

The operation is as follows:

- In the off state the IGBT and series diode snubber capacitors are charged, the device currents are zero and the complimentary devices are conducting current.
- At (i) in Figure 7.5 the complimentary devices are turned off, as shown in part i. At this point the diode snubber capacitor discharges, as seen in part c (diode voltage) and part f (diode snubber current). This causes the IGBT snubber to charge further (parts a and e). The steps in IGBT and diode voltage at (i) are due to the voltage drop across the snubber resistors.
- At (ii), the load voltage reaches the turn-on voltage of the SAD. It therefore clamps the load voltage, and hence the IGBT voltage, and the IGBT voltage flattens. The SAD conducts current when it clamps (part g), and in so doing take over the snubber currents.
- At (iii), the stipulated dead time of 10 μs after (i), the IGBT is turned on (part h). The IGBT voltage therefore decreases to $V_{CE(sat)}$ and it starts to conduct current. There is an IGBT turn-on current transient caused by its snubber capacitor discharging through the device (part e). However, there is already a transient present, as shown by the diode current (part d).
- This transient is caused by the charging and discharging of the snubber capacitors of other devices, as shown in Figure 7.6 for the case of IGBT e1 and diode a1. The steady-state conduction current of diode a1, i.e. after the transient, is about 50 A. The peak transient current through this diode is about 180 A, a difference of 120 A. This difference is provided by the other three current paths on that side of the load: those containing IGBTs e2, f1 and f2. IGBTs e2 and f1 provide the greatest portion in almost equal parts. These are the small transients during the 10 ms off period of the mains cycle in Figure 7.3. The transients are caused by discharge of the snubber capacitors of the series diodes of IGBTs f1 and e2 (diodes a2 and b1 – Figure 7.6 parts d and e). These currents do not flow through the diodes themselves, as shown by the fact that there is zero diode current during the 10 ms off period in Figure 7.4, because they are reverse biased, but through the snubbers. The fourth branch, IGBT f2 and diode b2,

provides only a small part of the transient. This current does not flow through the devices as the IGBT is off and the diode is reverse biased; instead it flows through their snubbers.

- IGBT turn-on current rise time, t_r, is listed as 70 to 140 ns by the manufacturer (see Appendix A). This is defined as being from 10% to 90% of the steady-state current (see Figure 2.4). The rise time was set to obtain a value in this range (about 90 ns). The total rise time, including the transient, is 660 ns.
- The stepped form of the current during turn-on is due to the rise time being achieved by switching discrete resistances. Simulink was found unable to provide controlled turn-on of a switch.

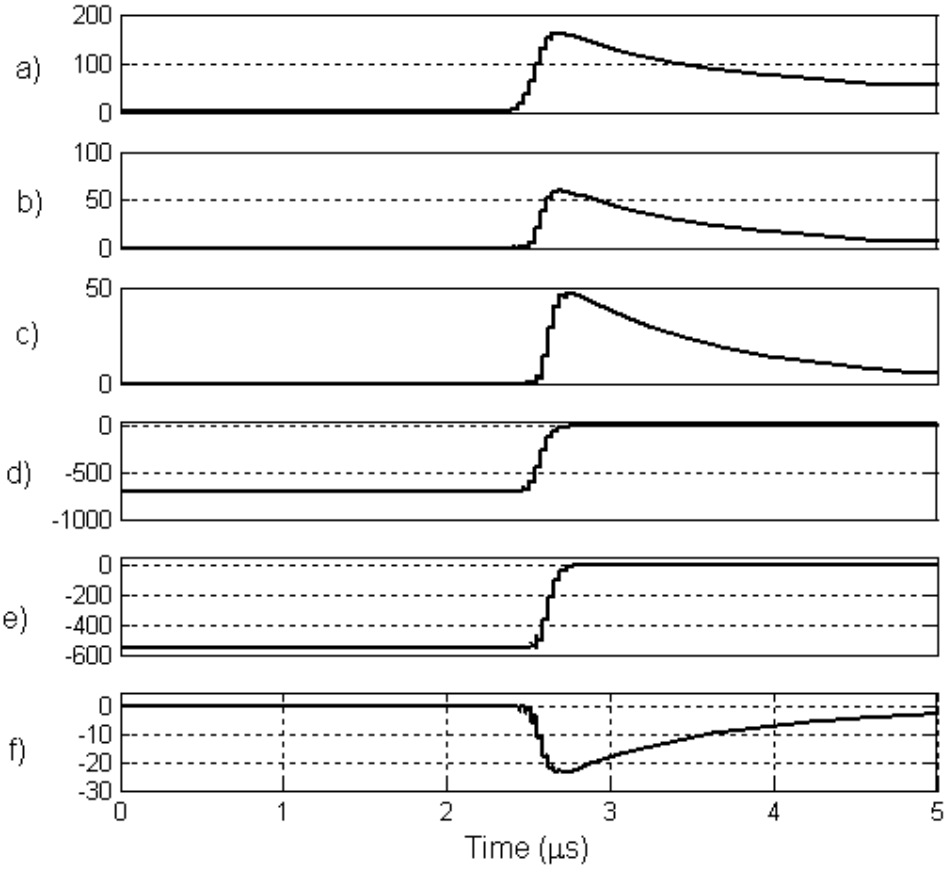


Figure 7.6 Forward-conducting device waveforms during turn-on: a) Diode a1 current, b) IGBT f1 current, c) IGBT e2 current, d) Diode a2 voltage, e) Diode b1 voltage, f) IGBT f2 snubber current

Waveforms during turn-off are shown in Figure 7.7. These are described as follows:

- At the beginning the IGBT and series diode are conducting load current (parts b and d).

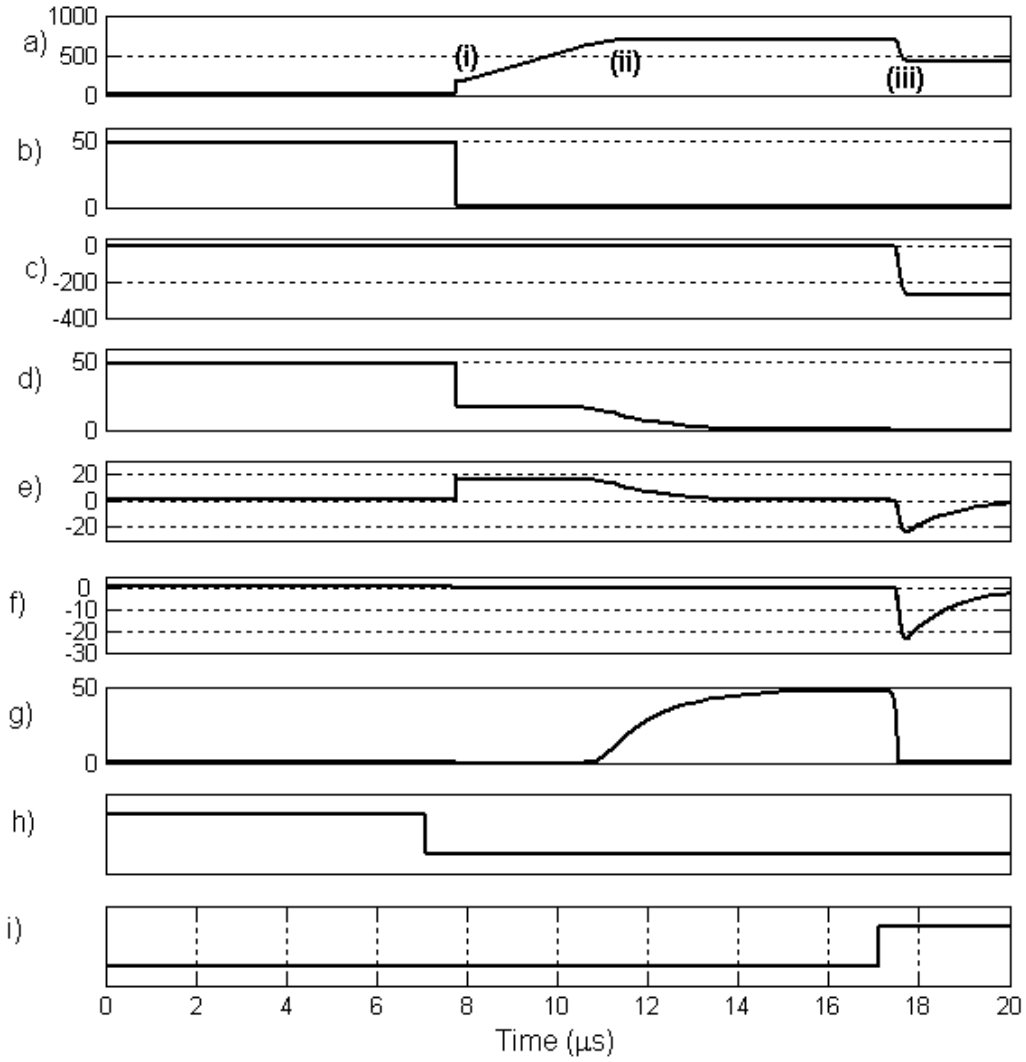


Figure 7.7 Forward-conducting device waveforms during turn-off: a) IGBT voltage, b) IGBT current, c) series diode voltage, d) series diode current, e) IGBT snubber current, f) series diode snubber current, g) SAD current, h) IGBT gate signal, i) turning on IGBT gate signal

- At (i) the IGBT turns off and its current drops to zero. This appears to happen instantaneously as the 90%-10% fall time, t_f, of 70 ns is short in comparison with the time scale. The diode current (part d) does not drop to zero, but carries the small current drawn by the IGBT snubber as it charges up (part e).
- At (ii) the IGBT snubber capacitor voltage flattens out (part a) as it is once again clamped by the SAD (shown by the fact that it conducts current – part g). The IGBT snubber current, and hence the diode current, drops to zero as the SAD takes over conduction.
- At (iii), the 10 μs deadtime after (i), the complimentary devices are turned on. This causes the diode snubber capacitor to charge (part c), resulting in its snubber conducting a current transient (part f). This current cannot flow through the diode because it is reverse biased or through the IGBT because it is off. It therefore flows through the IGBT snubber (part e), resulting in the IGBT snubber capacitor partly discharging (part a).

The following observations can be made from the above waveforms:

1. The voltage and current transients are caused by charge redistribution during the deadtime of 10 μs during both turn-on and turn-off
2. IGBT turn-on losses are expected to be large due to the high voltage and current values and the relatively long turn-on time
3. The high currents are above the 1 ms device rating of 150 A for the 100 A device. However, due to the comparatively short duration of this current, the IGBTs are expected to survive the transients, provided that adequate cooling is provided [76].
4. IGBT turn-off losses are comparatively small, due to the low current (there is no transient present), low voltage (this is only the small step voltage due to the snubber resistor) and short duration (about 70 ns instead of 660 ns).
5. IGBT turn-on losses can be accurately controlled by controlling the clamping voltage of the SADs. Increasing the clamping voltage increases the voltage transients, and hence the current transients and transient duration. Turn-off losses cannot be controlled in such a way.

6. Diodes have negligible switching losses: during turn-on the voltage returns to zero before the device starts conducting, and during turn-off the current returns to zero before the snubber capacitor starts charging.
7. High, but controllable, IGBT switching losses are useful in this application because total IGBT losses, and hence ΔT_{jc}, need to be increased. Similarly, lower than normal, or no, diode switching losses are desirable because total diode losses need to be reduced. Refer to Section 7.1.1.

7.2 Thermal calculations

The voltage and current waveforms were used to compute the power loss waveforms and hence the ΔT_{jc} waveforms, as was done for the conventional circuit. The calculation method is given first, followed by the results.

7.2.1 Calculation method

Four sets of calculations were performed for each case: one each for forward and reverse conducting IGBTs and diodes. The calculation method is similar to that used for the conventional circuit. Again, conduction losses were calculated for IGBTs and diodes by determining $V_{CE(sat)}$ at each step and multiplying by the current. For diodes, this was sufficient as there were no switching losses. The diode ΔT_{jc} waveforms were then calculated from the conduction losses only, in the same manner as for the conventional case. For IGBTs, the switching losses were also computed. This is illustrated in Figure 7.8. Both turn-on and turn-off losses were calculated by using simple geometry from Figure 7.8:

$$P_{on} = \frac{1}{6 \cdot t_{step}} \cdot V_1 \cdot I_1 \cdot t_1 \quad \text{……..…….……} \quad (7.1)$$

where P_{on} = turn-on loss per pulse

V_1, I_1 = voltage and current per pulse, defined in Figure 7.8

t_1 = total turn-on time = 660 ns

t_{step} = simulation time step

$$P_{off} = \frac{1}{6 \cdot t_{step}} \cdot V_2 \cdot I_2 \cdot t_2 \quad \text{..... (7.2)}$$

where P_{off} = turn-off loss per pulse

V_2, I_2 = voltage and current per pulse, defined in Figure 7.8

t_2 = total turn-off time = 70 ns

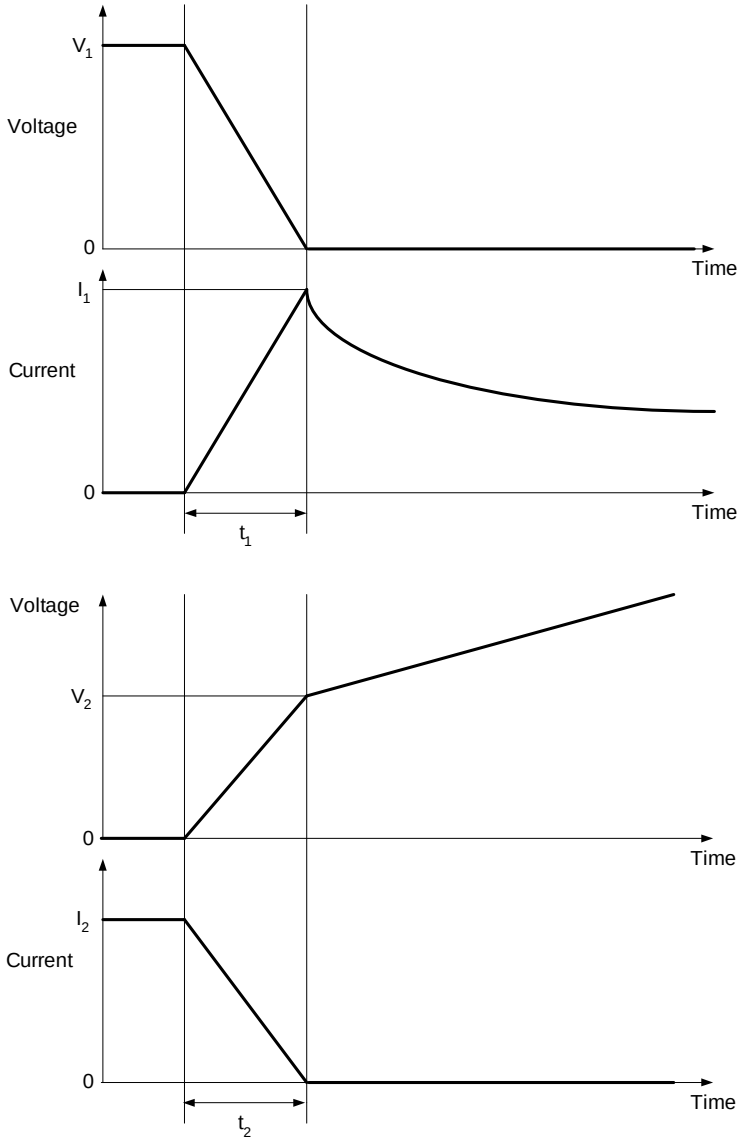


Figure 7.8 Calculation of IGBT turn-on losses (top) and turn-off losses (bottom)

IGBT switching losses were substituted for conduction losses in the same way as for the conventional circuit. Total power loss and ΔT_{jc} waveforms were then calculated, as before.

7.2.2 Results

The thermal calculation results are shown in Figures 7.9-7.12, with the voltage and current waveforms for comparison. Only the 10 ms conduction periods are shown for clarity, as there is no diode current flow during the other 10 ms and IGBT current flow was shown to contribute negligible losses (the contribution to the variation in ΔT_{jc} was less than 2%).

The following observations can be made from these results:

1. IGBT turn-on losses are much larger than turn-off and conduction losses, as shown by the large power pulses at turn-on and the resultant increases in ΔT_{jc}.
2. In the proposed circuit, the waveforms result in IGBT turn-off losses being less than 1% of turn-on losses.
3. Due to the lack of diode switching losses, the total diode power loss waveforms closely resemble the diode current waveforms, as the power at each time step is simply the product of the current and $V_{CE(sat)}$. This results in smoother ΔT_{jc} waveforms than for the IGBTs, that are similar to the conventional case.

7.3 Comparison with conventional circuit

The above was repeated for switching frequencies of 2 kHz and 3 kHz, and the results were compared to the conventional case. The variation in ΔT_{jc} for these frequencies is shown in Figure 7.13, with the conventional circuit results for comparison. The following observations can be made from these results:

1. ΔT_{jc} for forward-conducting IGBTs is substantially greater for the modified circuit due to the larger switching and conduction losses
2. ΔT_{jc} for reverse-conducting IGBTs is slightly smaller, as the larger switching losses are cancelled out by lower conduction losses
3. For reverse-conducting diodes ΔT_{jc} is substantially lower for the modified circuit due to lower conduction losses and the absence of switching losses

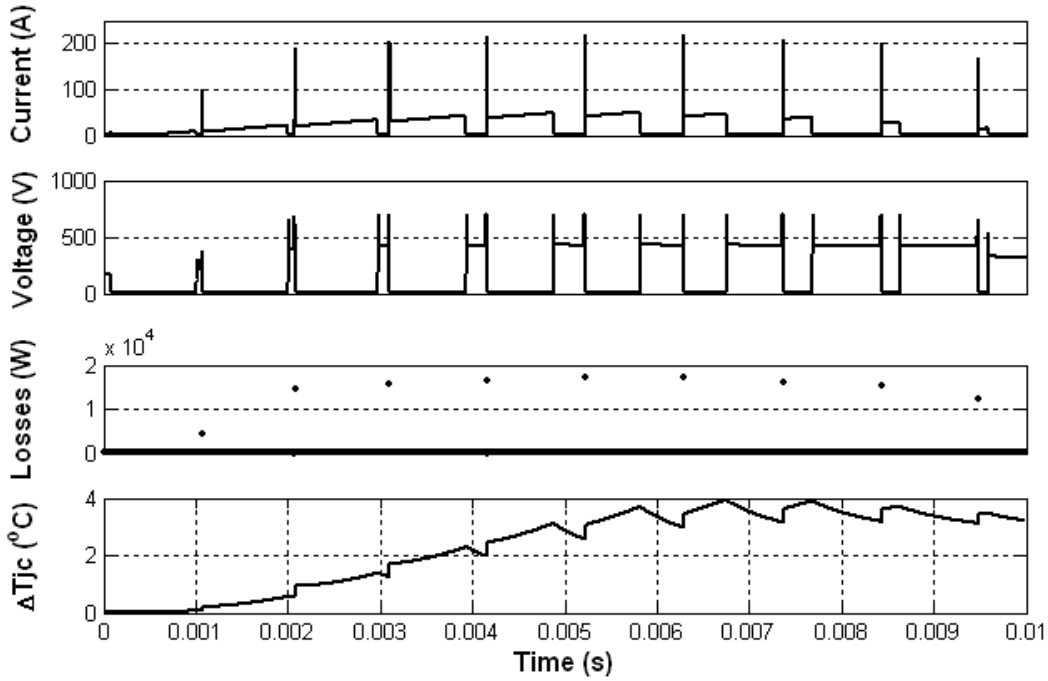


Figure 7.9 Simulation results for forward-conducting IGBTs

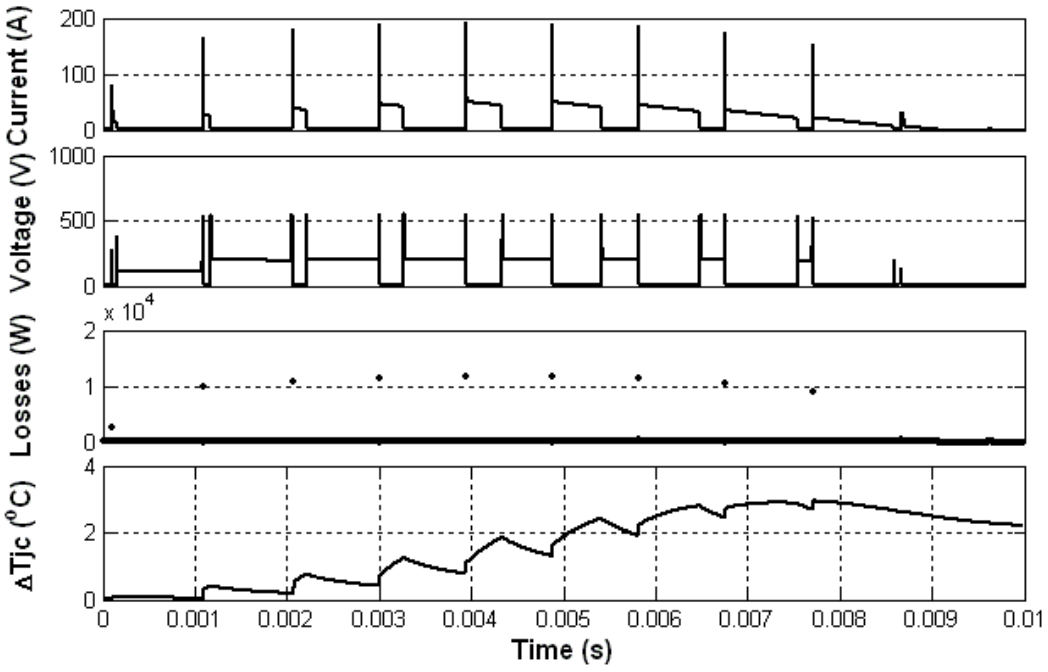


Figure 7.10 Simulation results for reverse-conducting IGBTs

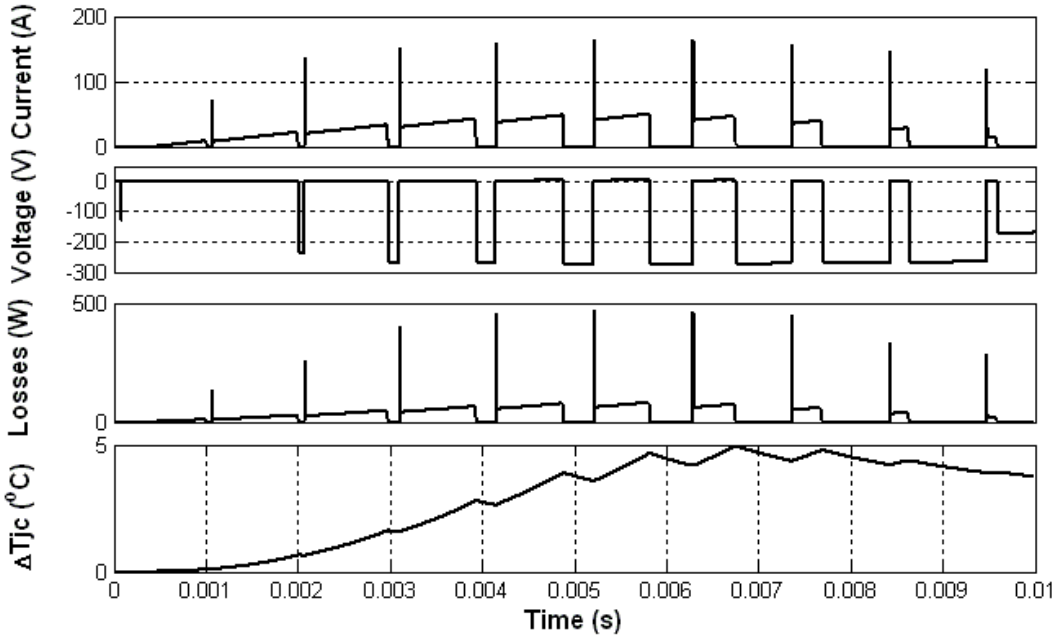


Figure 7.11 Simulation results for forward-conducting diodes

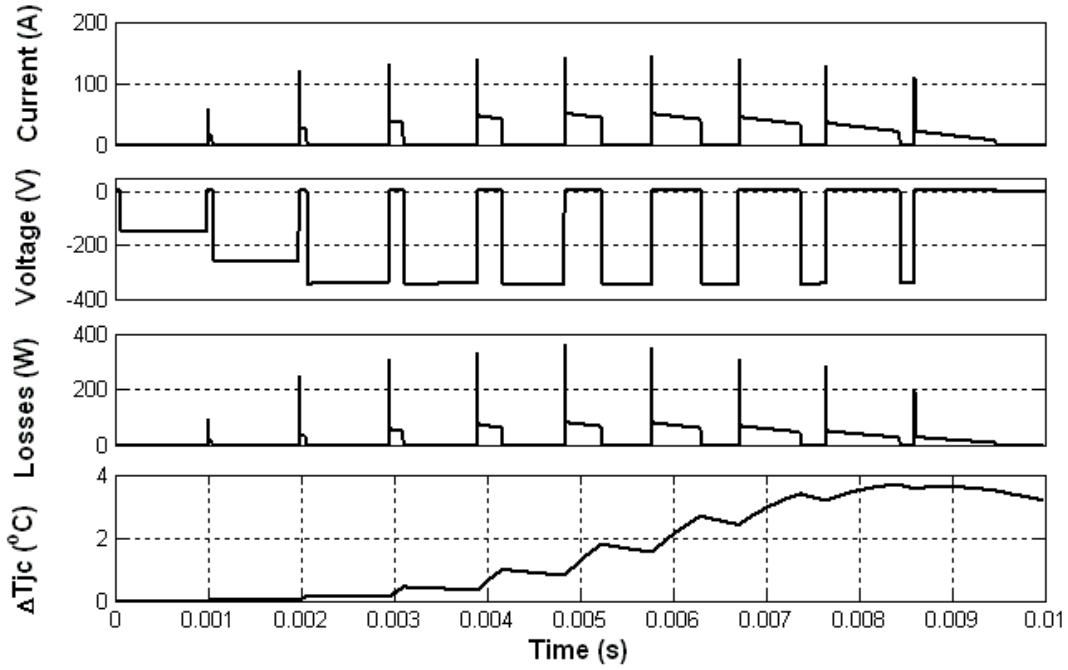


Figure 7.12 Simulation results for reverse-conducting diodes

4. For forward-conducting diodes ΔT_{jc} is similar due to the absence of switching losses being offset by larger conduction losses
5. The horizontal dotted lines are the targets defined in Section 7.1.1. The variation in ΔT_{jc} for the modified circuit can be compared as follows:
    - At 3 kHz the variation in ΔT_{jc} for forward-conducting IGBTs is within 10% of the upper limit (6.1°C), and for reverse-conducting IGBTs it is within 30% of the lower limit (5.1°C). The former is adequate, while the measured variation in ΔT_{jc} for reverse-conducting IGBTs is expected to be larger due to larger switching losses, reducing the difference
    - At 3 kHz the variation in ΔT_{jc} for reverse-conducting diodes is within the required limits, while for forward-conducting diodes it is substantially greater. Using the reported logarithmic variation of power cycling performance of IGBTs and diodes reported in the literature (Section 3.5), forward-conducting diode performance at the upper limit can be easily determined.
    - Increasing the switching frequency above 3 kHz would result in stresses on the reverse-conducting IGBTs that are closer to the required, but would result in the forward-conducting IGBTs being stressed far in excess of the upper limit. Diode stresses would be relatively unaffected at a higher switching frequency. 3 kHz is therefore an acceptable switching frequency.

The behaviour of the circuit can be further explained by studying the losses, as was done previously for the conventional circuit. IGBT losses are shown in Figure 7.14 and diode losses in Figure 7.15. Average current is compared in Figure 7.16. These figures raise the following points:

1. The variation in ΔT_{jc} has the same form as the average total power for IGBTs and diodes, as expected.
2. IGBT switching losses are greater for forward-conducting devices because of higher voltage and current during turn-on.

3. Average current, and hence conduction losses, are greater for forward-conducting devices than for reverse-conducting devices. This effect increases with switching frequency due to the higher power dissipated in the load SADs and device snubber resistors. This can be seen in Figures 7.5 and 7.7, which show that power is dissipated in these devices at each switching operation.

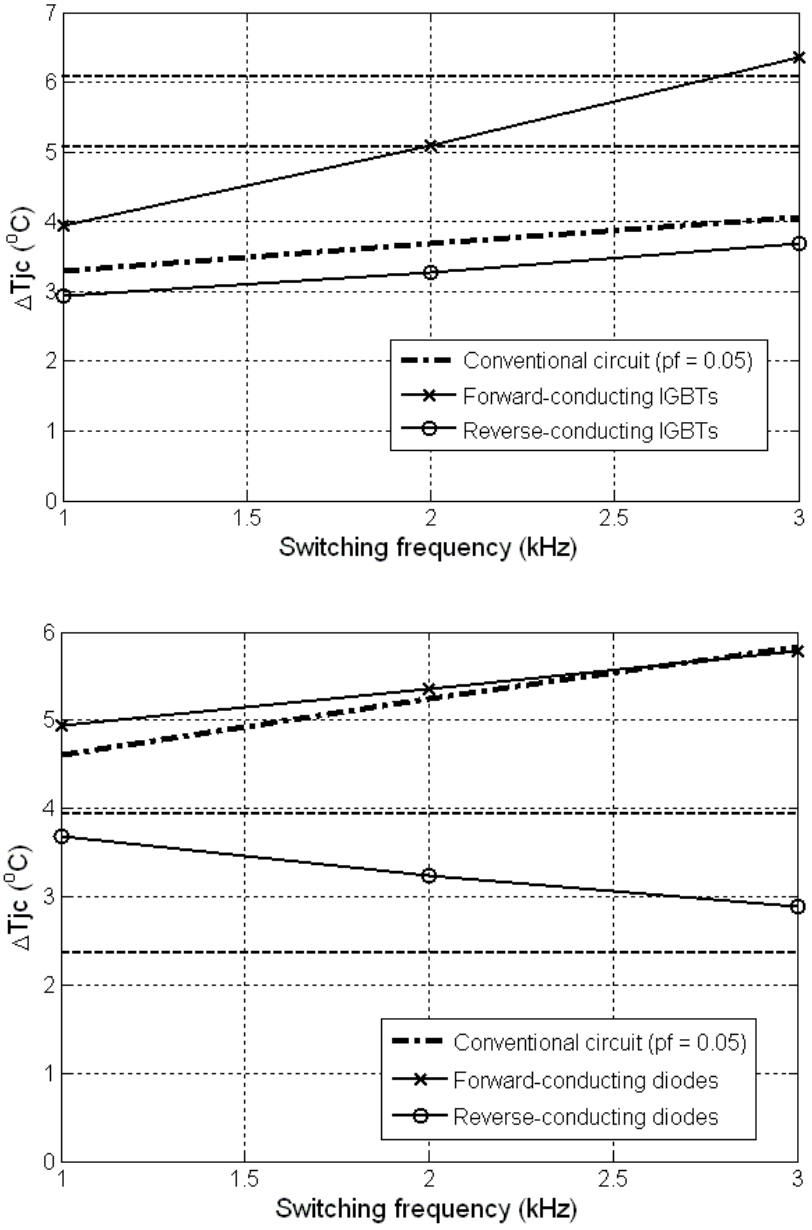
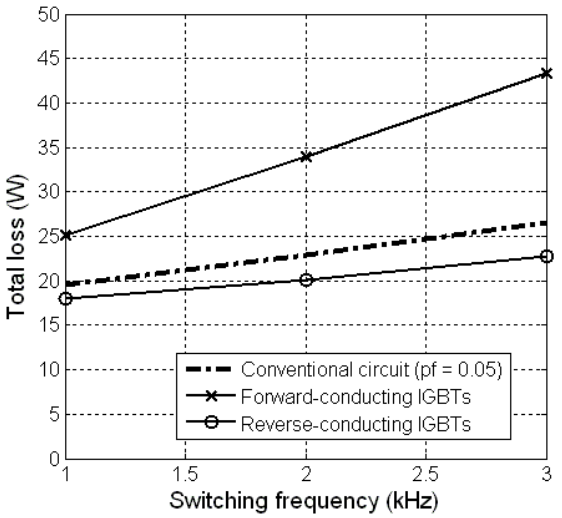
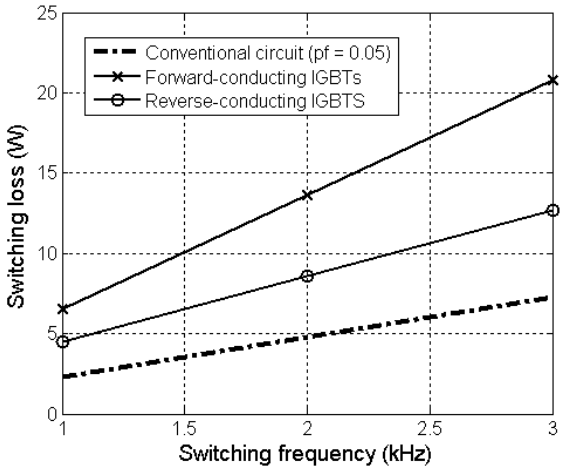


Figure 7.13 Comparison of variation in ΔT_{jc} obtained for conventional and modified circuits: IGBTs (top) and diodes (bottom)





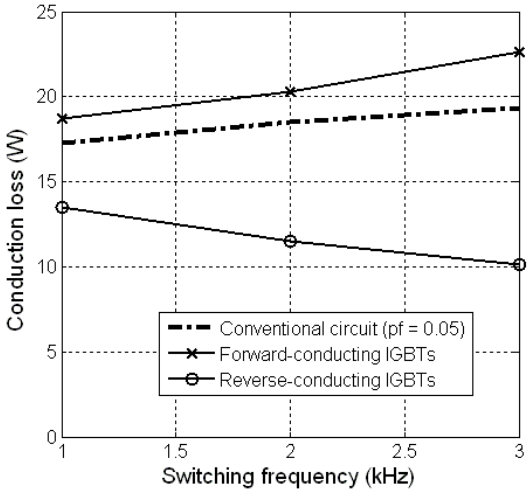


Figure 7.14 Comparison of average IGBT losses obtained for conventional and modified circuits

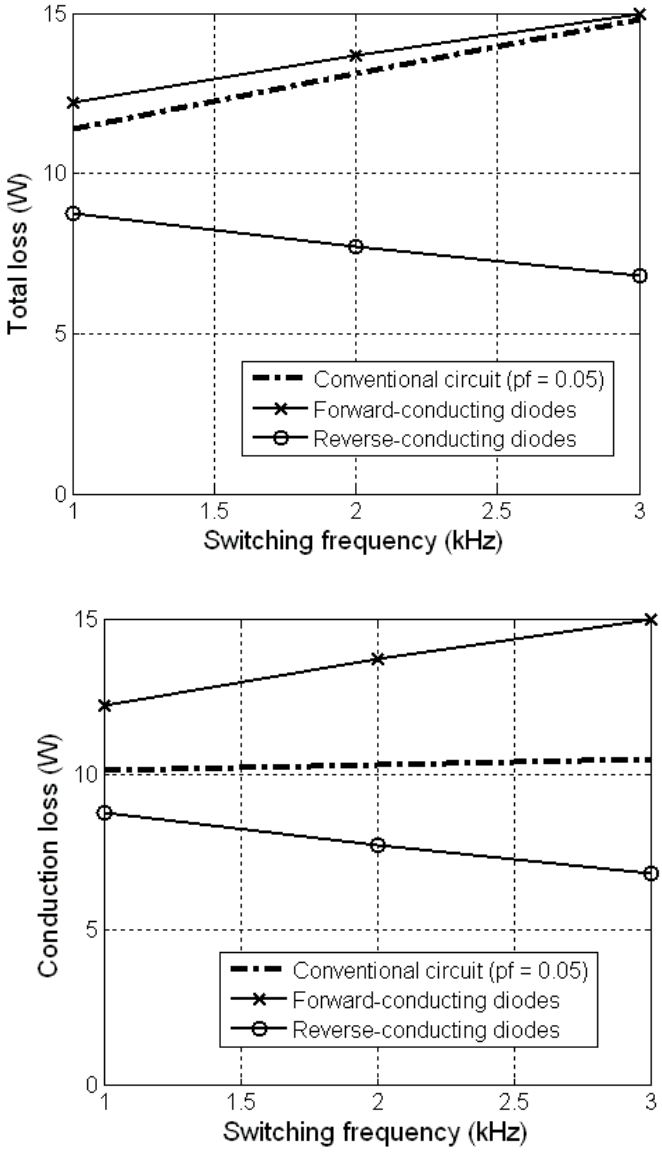


Figure 7.15 Comparison of average diode losses obtained for conventional and modified circuits

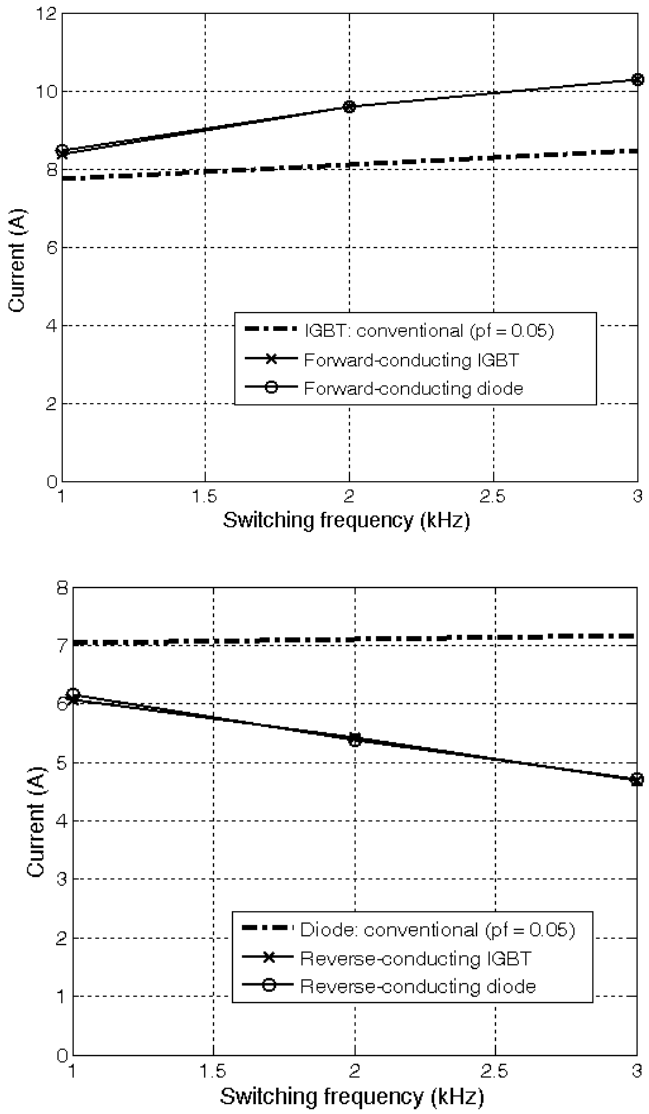


Figure 7.16 Comparison of average current: forward-conducting devices (top), reverse-conducting devices (bottom)

7.4 Conclusion

The modified H-bridge has been presented. The reasons for choosing it, the simulation methodology and results have been shown. The circuit and the simulation results compare to the criteria of Section 5.2 as follows:

1. Switching losses are included in IGBTs, but not in diodes. The latter is an advantage as diode losses need to be decreased because of the low load power factor.

2. When using a switching frequency of 3 kHz, forward-conducting IGBTs and reverse-conducting diodes are stressed to within 10% of the required limits in variation in ΔT_{jc}. Reverse-conducting IGBT stresses are relatively low, but higher switching losses in practice are expected to reduce this difference. Forward-conducting diodes are stressed higher than required, but power cycling performance at the required level can easily be calculated from the measurements.
3. The test circuit uses twice as many devices as a conventional H-bridge and is therefore more complex. However, this allows twice as many devices to be tested simultaneously.
4. Equipment costs are higher due to the greater number of devices tested, but this is offset by the significantly lower operating costs due to the low power factor load.
5. The test duration can be made as short as is needed – approximately 400 ms per cycle is recommended
6. Load current magnitudes and waveforms are similar to the conventional case, with exception of the switching transients. However, these transients are beneficial as they increase IGBT losses, but do not significantly affect diode losses.

The above shows that this circuit is capable of accurately reproducing the stresses that IGBTs and diodes would face in the field when a high load power factor is used, by using a low load power factor to keep operating costs to a minimum.

8. IMPLEMENTING THE MODIFIED H-BRIDGE

In the first section the implementation of the circuit in the laboratory is described. Next, voltage and current measurements are given, followed by the thermal calculation method and results. The results are compared to the simulations of the previous chapter. Finally, several implementation issues are discussed.

8.1 Implementation

The circuit of Figure 7.1 described in the previous chapter was implemented. The anti-parallel IGBTs of the diodes – those of smaller size in the figure – were permanently turned off using 9 V batteries, and hence played no part in the circuit.

The IGBT gate drivers recommended by the manufacturer (Semikron SKHI 23/12 [71]) were used. The gate resistance was the recommended value (15 Ω). The gate drivers were controlled by a Motorola MC68HC908JL3 microprocessor [77].

The DC supply voltage was fed from a variable 50 Hz three-phase supply and rectified with a suitably rated three-phase rectifier. A 9 mF smoothing capacitor network was placed across the output of the rectifier. The load comprised four commercial iron-core inductors mounted in series. The total inductance was approximately 10 mH.

A photograph of the test setup is shown in Figure 8.1. In the following sections the fabrication of each part of the setup is explained in detail.

8.1.1 Power supply and DC bus

The circuit diagram of the power supply circuit is shown in Figure 8.2. Detailed circuit diagrams of the rectifier and DC bus smoothing capacitor network are shown in Figures 8.3 and 8.4.

The rectifier consisted of three individual bridge arms, as shown in Figure 8.1. These arms were the SKKD 100/16 [78]. The DC bus capacitor network was recommended and supplied by the IGBT manufacturer. All capacitors are 4.7 mF and all resistors 22 kΩ. The variac was used to adjust the DC bus voltage fed to the inverter. The control circuitry was fed from a separate constant single phase 220 V, 50 Hz supply.

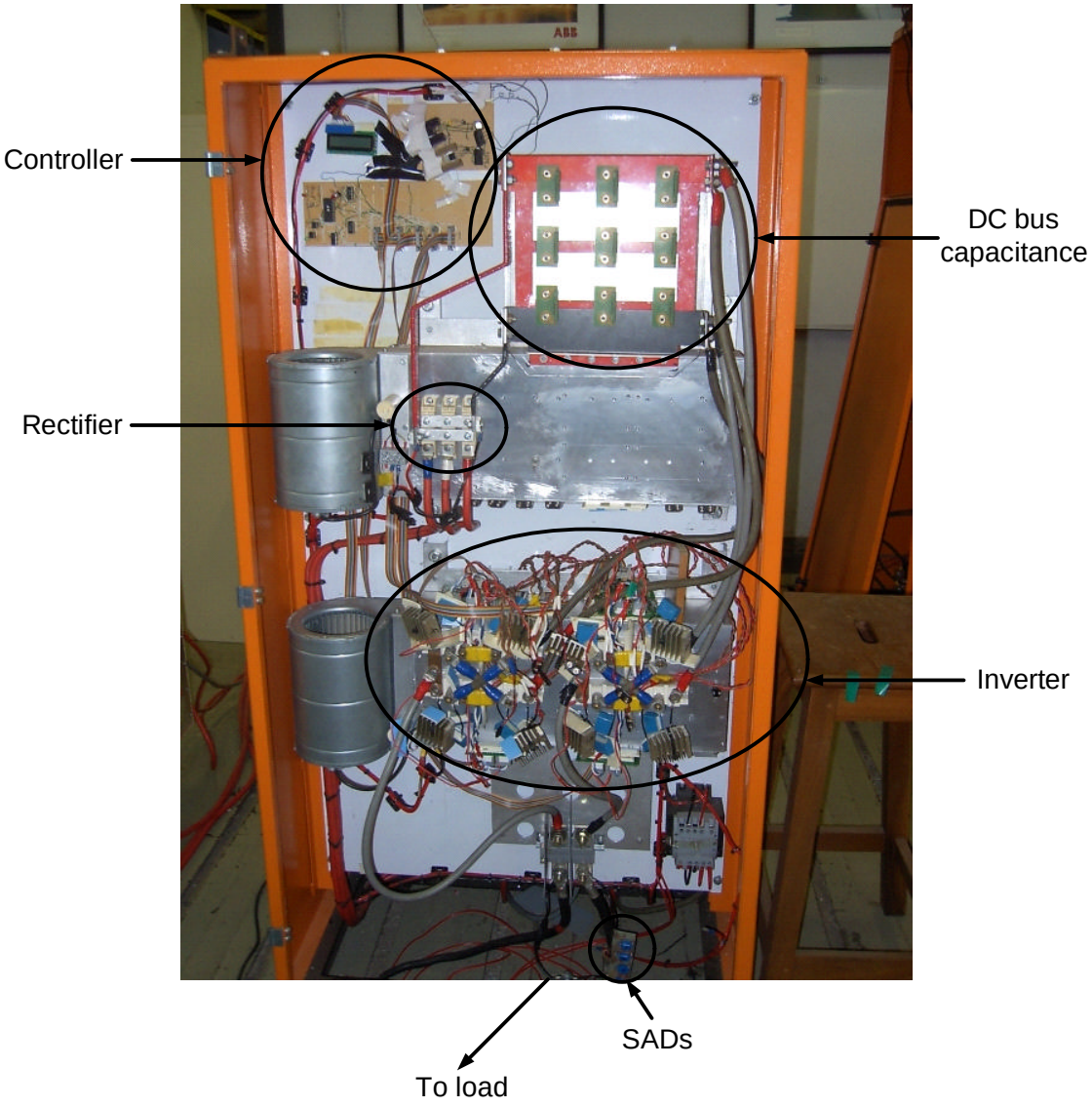


Figure 8.1 Photograph of the test setup (the inverter is hidden behind the snubbers included to reduce stray inductances)

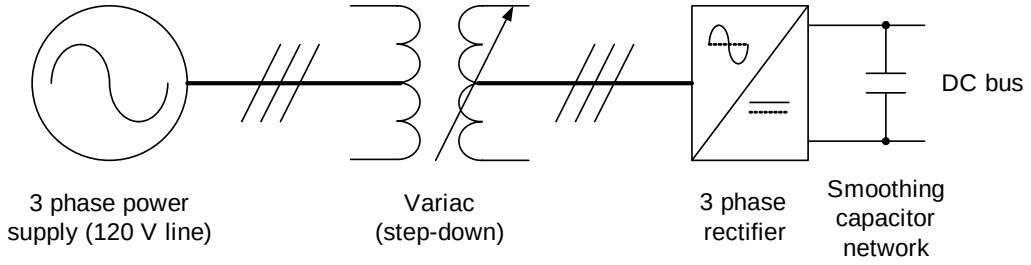


Figure 8.2 Circuit diagram of the power supply circuit

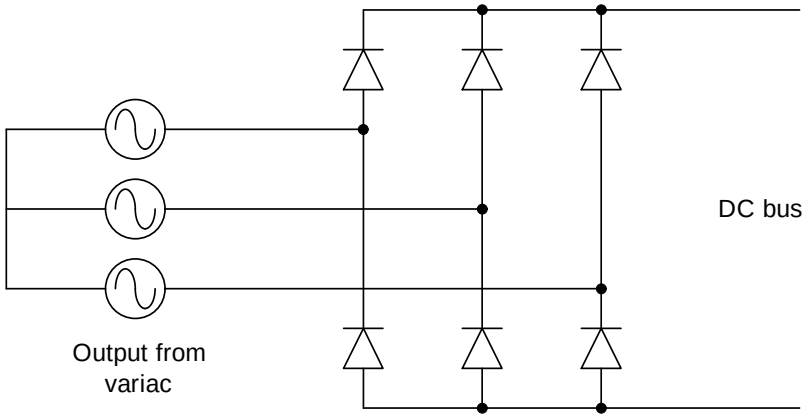


Figure 8.3 Detailed circuit diagram of rectifier

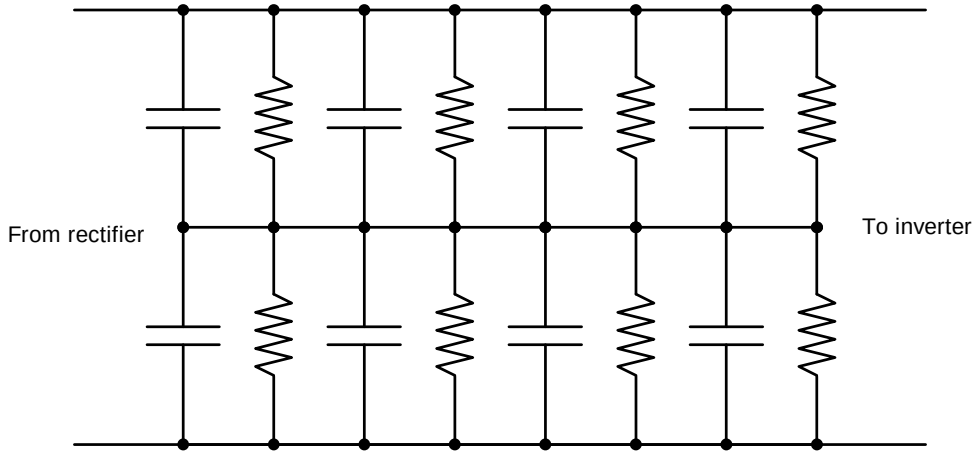


Figure 8.4 Detailed circuit diagram of the DC bus capacitor network

8.1.2 Inverter stack and cooling

A photograph of the inverter stack is shown in Figure 8.5.

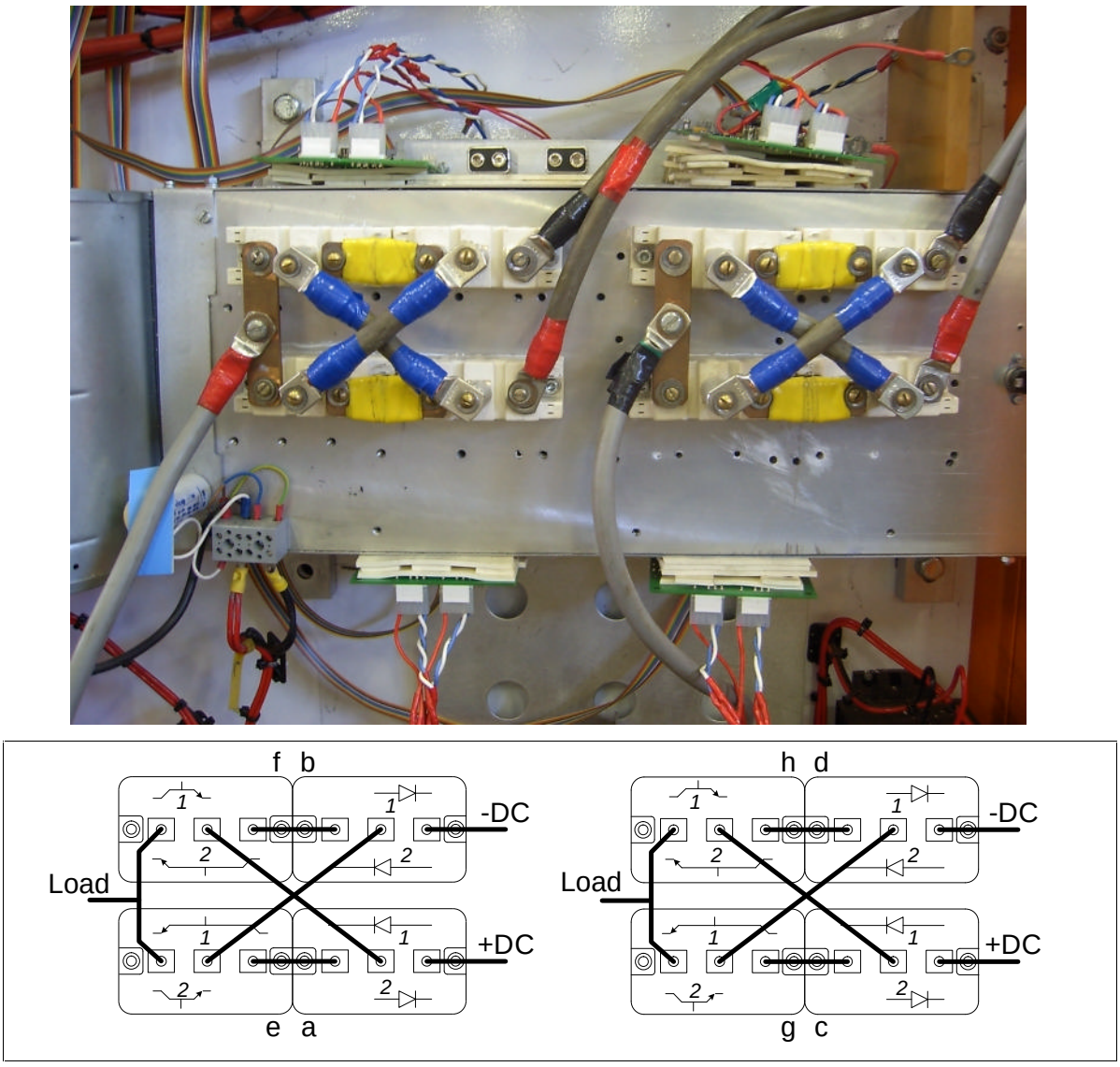


Figure 8.5 Inverter layout: photograph (top); schematic (bottom)

The snubbers, gate drivers and batteries have been removed for clarity. The figure shows that the modules were mounted on a force-cooled heatsink, as recommended by the manufacturer. Connections between devices were made using laminated busbar to help reduce stray inductance. Figure 8.5 also shows a schematic diagram of the setup. The circuit has been divided into two halves: the

left side of the load in Figure 7.1 (IGBT modules e and f and diode modules a and b) is mounted on the left of the heatsink, and the right side of the load (IGBT modules g and h and diode modules c and d) on the right of the heatsink. The two sections have separate connections to the DC bus.

8.1.3 IGBT drivers

An IGBT driver card is shown in Figure 8.6. One driver is required per module (two IGBTs). The driver is interfaced to the controller via ribbon cable, attached to the connector on the left of the driver, and the IGBTs are driven via the two connectors on the right. The drivers were mounted above and below the heatsink, as shown in Figure 8.5. The driver settings were adjusted as follows:

- R_G = 15 Ω – recommended by the manufacturer for the particular IGBT and DC bus voltage [71]
- Dead time = 10 μs – this is the maximum allowable value and was used because of the large voltage transients expected

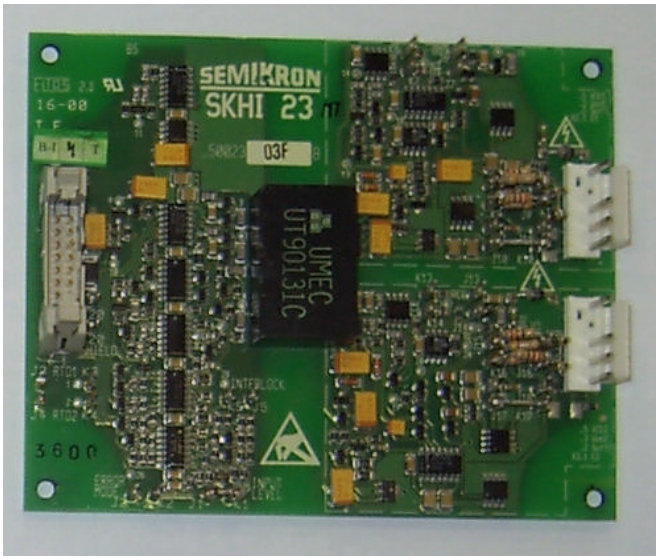


Figure 8.6 Semikron SKHI 23/12 IGBT driver card

8.1.4 IGBT controller circuit

The purpose of the controller circuit was to:

1. Generate the PWM signals to be fed to the IGBTs via the gate drivers

2. Set t_{on} and t_{off}
3. Allow the user to start and stop tests
4. Automatically stop a test if an error signal is received from one of the gate drivers via the ribbon cable and display which driver card issued the error signal on an LCD screen
5. Stop the test if the temperature of one of the heatsinks rises too high (in such a case an error signal would be received from one of the thermal cut-outs mounted on the two heatsinks)
6. Display the number of cycles applied in a test sequence
7. Store the number of cycles in non-volatile memory in case of a power failure

These parameters could be adjusted by changing the microcontroller's firmware. The circuit diagram of the complete controller is shown in Appendix C.

8.1.5 Snubbers

Snubbers were placed in parallel with all IGBTs and diodes. The two snubbers for each module were mounted together, as shown in Figure 8.7.

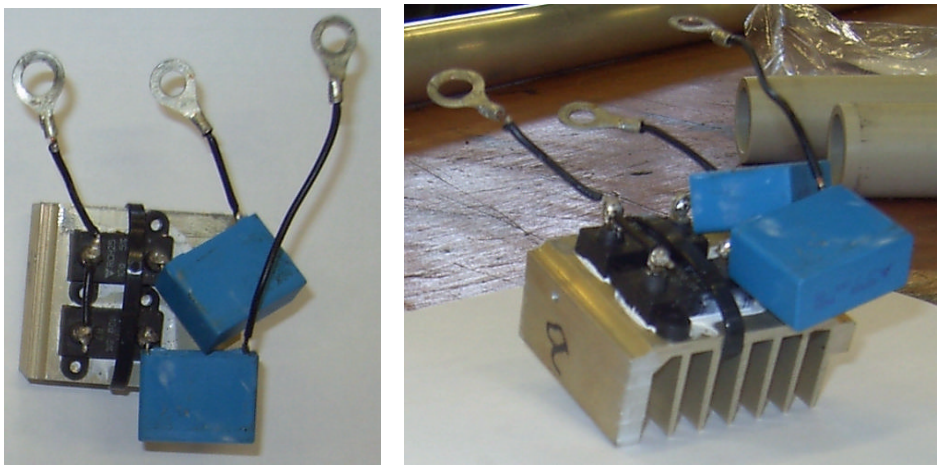


Figure 8.7 Two snubbers on a heatsink

The resistors, on the left in both figures, were mounted on naturally-cooled heatsink. RCH 25 10 resistors, manufactured by Vishay [79], were used. They

were chosen because of their low inductance (≤ 0.1 μH) and because of their high power rating (25 W when mounted on a heatsink). The latter was an important characteristic because the simulations showed that the snubbers would probably conduct high currents during switching. The capacitors were those recommended for DC bus snubbers by the IGBT manufacturer, and were also supplied by the manufacturer. The snubbers were mounted directly onto the IGBT and diode modules with the lugs.

8.1.6 SADs

An individual SAD is shown in Figure 8.8, with an IGBT module for comparison of size. Three SADs were mounted in series as closely as possible to the load.

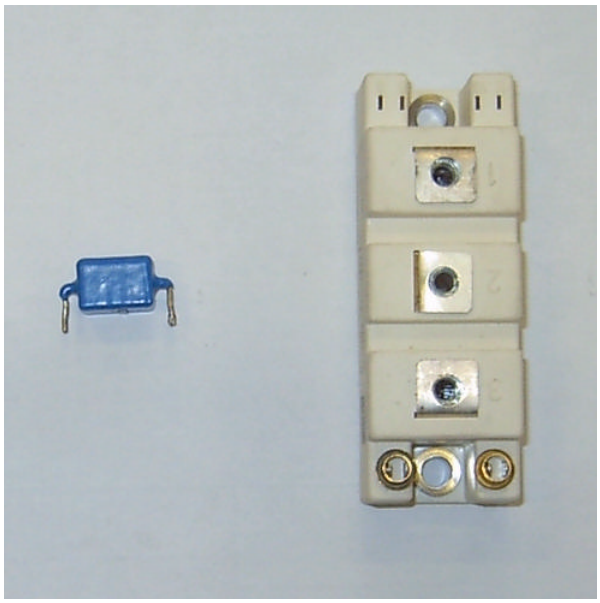


Figure 8.8 A silicon avalanche diode (SAD) and IGBT module

8.1.7 Load

The load is shown in Figure 8.9. This consisted of two commercially available inductor assemblies, each consisting of two separate inductor coils. The four coils were connected in series. The total inductance was approximately 10 mH.



Figure 8.9 The almost purely inductive load

8.2 Measurements

In this section the operation of the implemented circuit is compared to the predictions of the previous chapter. A switching frequency of 1 kHz is used throughout, for clarity. The DC bus voltage was approximately 160 V, giving a peak load current of 50 A.

8.2.1 Measurement equipment

All currents except snubber currents were measured using a CWT3 Rogowski coil manufactured by Power Electronic Measurements [80]. All voltage measurements were taken using Tektronix P5205 High Voltage Differential Probes [81]. Two such probes were available. Snubber current waveforms were determined by measuring the voltage across the snubber resistor and scaling by the resistance value (10 Ω). A Tektronix TDS3014 digital oscilloscope [82] was used for all measurements.

8.2.2 Load waveforms

Figure 8.10 shows typical load voltage and current waveforms for two 20 ms cycles during t_{on} for a PWM switching frequency of 1 kHz. These waveforms are very similar to the simulated waveforms (Figure 7.2). The SAD clamping voltage is about 5% higher than predicted. This can be attributed to the difficulty in accurately modeling the highly non-linear behaviour of SADs and to possible small manufacturing tolerances.

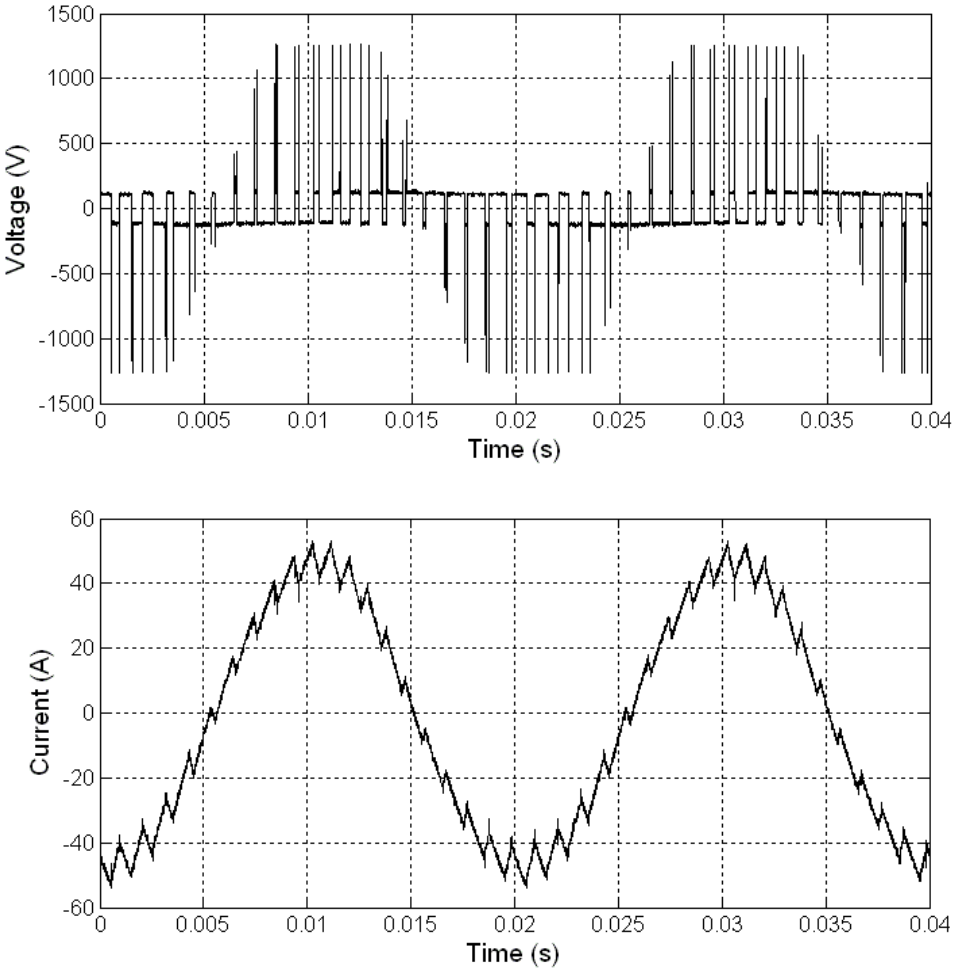


Figure 8.10 Load voltage and current waveforms

8.2.3 IGBT and diode waveforms

Recorded IGBT waveforms are shown in Figures 8.11 and 8.12, and diode waveforms in Figures 8.13 and 8.14. As in the simulations, identical waveforms

were recorded for all forward-conducting devices, and for all reverse-conducting devices. The following observations can be made about the measured waveforms:

1. The current waveforms, excluding transients, are similar to the predictions (Figures 7.3 and 7.4). However, there is a negative DC offset and a small low frequency oscillation, both of which are measurement errors from the Rogowski coil. These effects were removed in the calculations, as shown later.
2. The current transients during turn-on are smaller than in the simulated case and are of varying amplitude. This is due to the relatively large sampling time step of the oscilloscope: 10,000 samples are captured in a single screen. Therefore, to capture 20 ms worth of data each sample is 2 μs. Even if the 10 ms off period is ignored, as in the simulations because the losses are negligible, the time step is still only 1 μs. This is too large to accurately capture sub-microsecond rise and fall times. It will be shown later how this was compensated for.
3. The diode waveforms have transients during the 10 ms off period and a few small negative current transients, which are not present in the simulation results. These are snubber currents, because the sum of the diode current and its snubber current was measured. The individual diode current was not measured due to space limitations.
4. The IGBT measurements also show small negative current transients during the off period. These currents were conducted by the free-wheeling diodes included in the IGBT modules. It is not possible to measure these currents separately as they are connected to the same terminals as the IGBTs.
5. The magnitude of the voltage transients of the forward-conducting IGBTs are similar to the predictions, but the measured values are again about 5% larger than the predicted values. For reverse-conducting IGBTs the difference is about 9%. A 1 or 2 μs sampling time does not affect these measurements as the peaks are flat due to the clamping action of the SADs and are several microseconds long. Similarly, measured diode voltage transients during the 10 ms off period are about 5% larger than predicted.

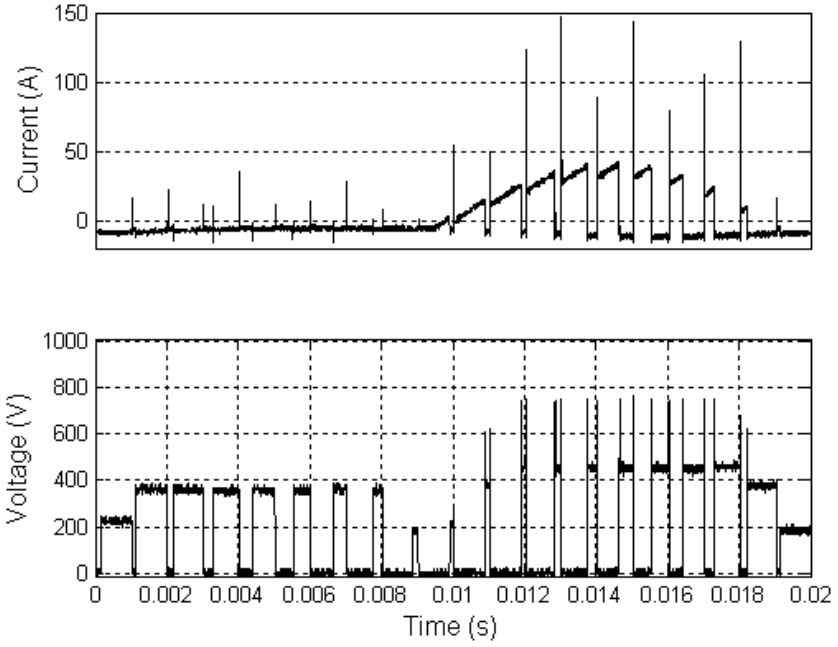


Figure 8.11 Forward conducting IGBT voltage and current waveforms

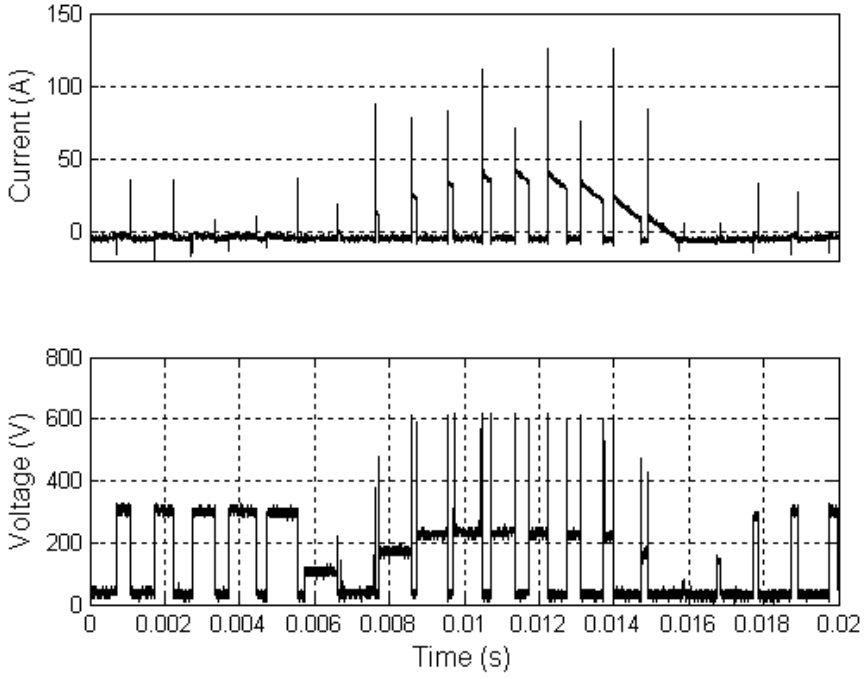


Figure 8.12 Reverse conducting IGBT voltage and current waveforms

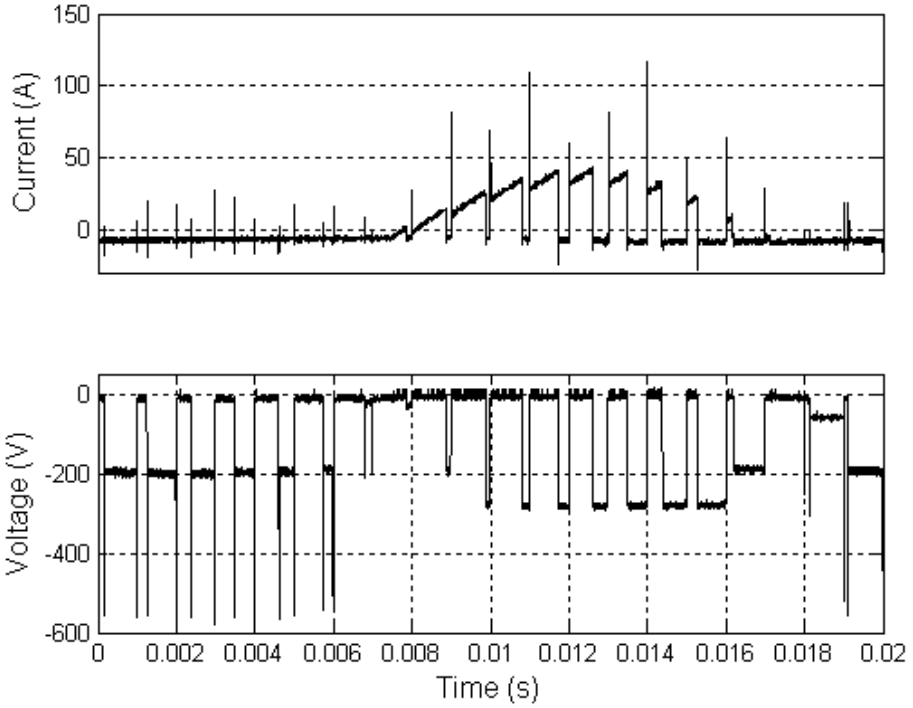


Figure 8.13 Forward conducting diode voltage and current waveforms

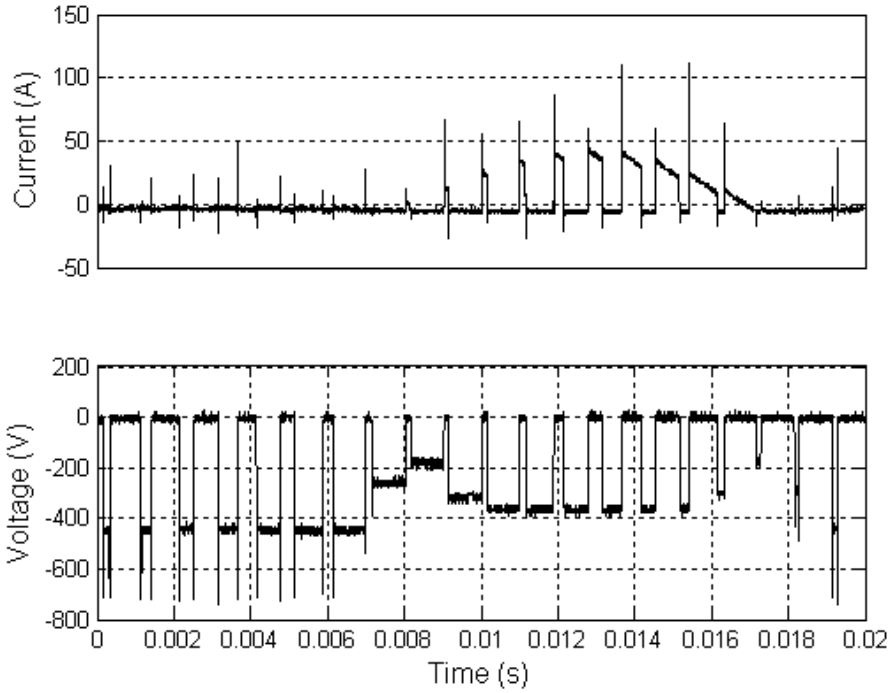


Figure 8.14 Reverse conducting diode voltage and current waveforms

6. The flat portions of the IGBT and diode voltage waveforms between the transients and when no transients are present are also similar to the predictions. This is more accurate for forward-conducting devices than for reverse-conducting devices. However, the accuracy of these is not important, as they do not affect device losses.
7. $V_{CE(sat)}$ is not accurately measured because this is small in comparison with the large peaks. This was also easily compensated for in the thermal calculations.

8.2.4 Turn-on and turn-off waveforms

Once again only forward-conducting devices are looked at because the same principle applies to both forward and reverse-conducting devices. Turn-on is illustrated in Figure 8.15. Note that the current waveform is the sum of the IGBT device and snubber currents, which is also the sum of diode device and snubber currents. These waveforms compare favourably to the predicted waveforms (Figure 7.5).

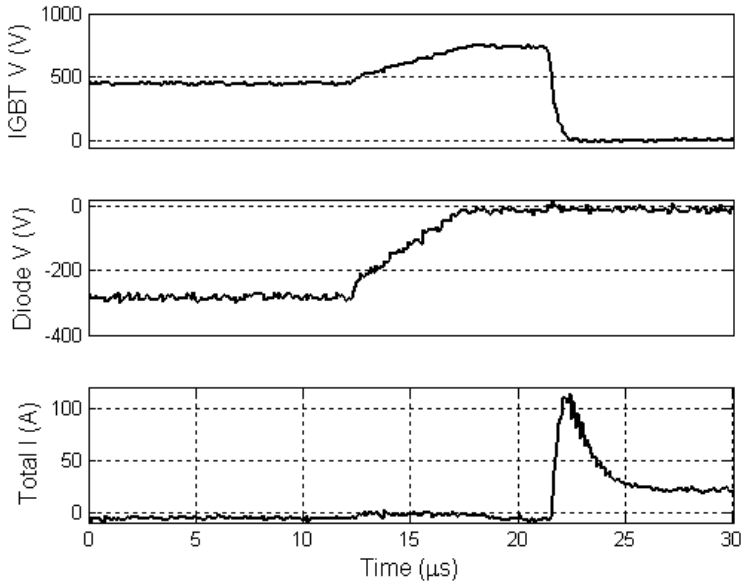


Figure 8.15 Turn-on waveforms: IGBT and series diode

Figure 8.15 illustrates the following:

1. The small current flow between the devices during discharge of the diode snubber capacitor and the consequent charging of the IGBT snubber capacitor
2. The voltage step due to the voltage drop across the snubber resistors
3. The 10 μs dead time (from 12 μs to 22 μs)
4. The magnitude of the current is lower than that of Figure 7.5. This is because the measured pulse is near the end of the 10 ms on period (see Figure 7.4), as explained by the smaller steady-state current. However, the mechanism is still the same as near the peak load current.

Turn-on waveforms for the IGBT only are shown in Figure 8.16. This time the device and snubber currents were measured separately, and the load current is closer to 50 A. These once again compare favourably with the predictions of Figure 7.5.

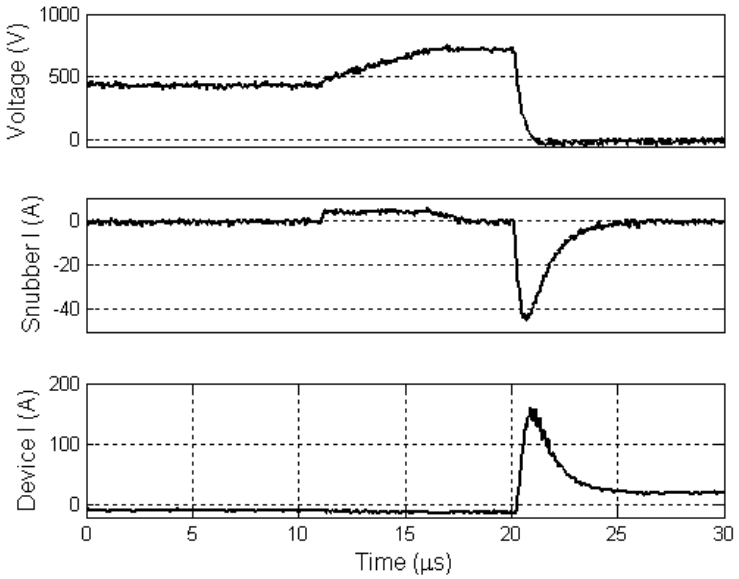


Figure 8.16 Turn-on waveforms: IGBT only

Turn-off waveforms are shown in Figures 8.17 and 8.18. The measurements are similar to the predictions of Figure 7.7. Again, the charging and discharging of the snubber capacitors, the dead time and the snubber resistor voltage drop are

evident. Figure 8.18 shows a small tail, of approximately 5 μs in length, in the IGBT current after turn-off. This justifies the long dead time chosen.

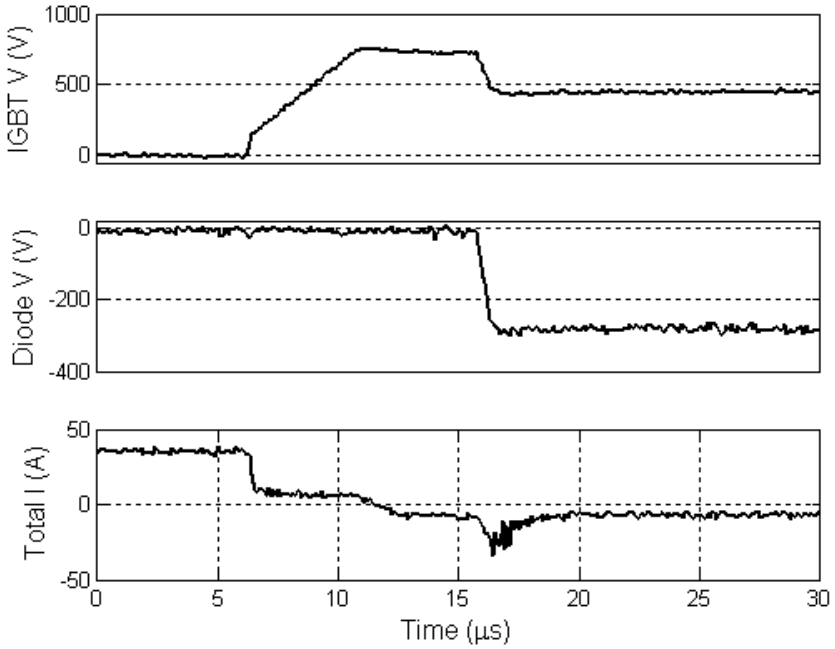


Figure 8.17 Turn-off waveforms: IGBT and series diode

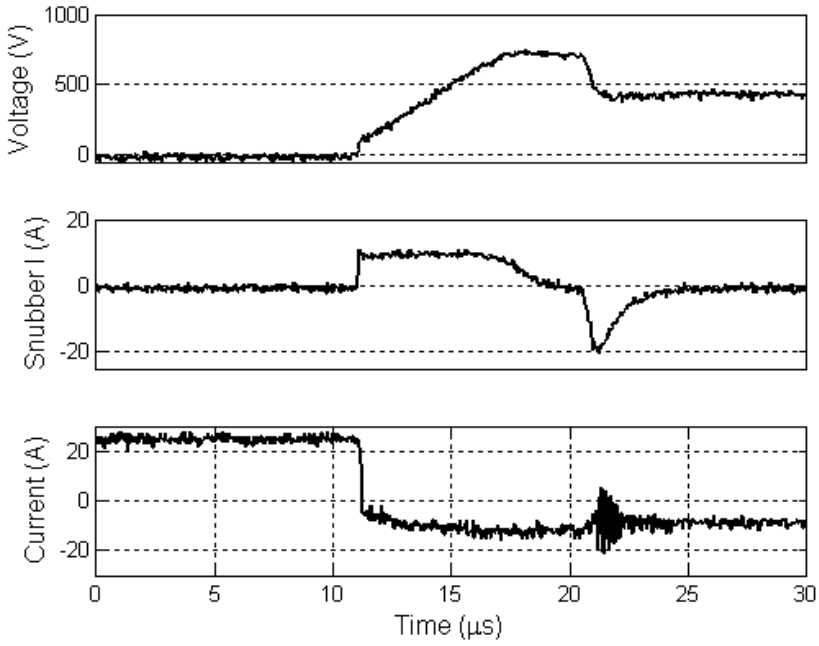


Figure 8.18 Turn-off waveforms: IGBT only

All current oscillations, such as that at 22 μs in the IGBT current (Figure 8.18), were determined to be measurement noise produced by the Rogowski coil.

SAD current waveforms during turn-on and turn-off are shown in Figure 8.19. These have a similar form to the predicted waveforms of Figures 7.5 and 7.7. The magnitudes differ from the predictions because different pulses are being compared: the greater the prospective peak voltage being clamped, the greater the current drawn by the SAD.

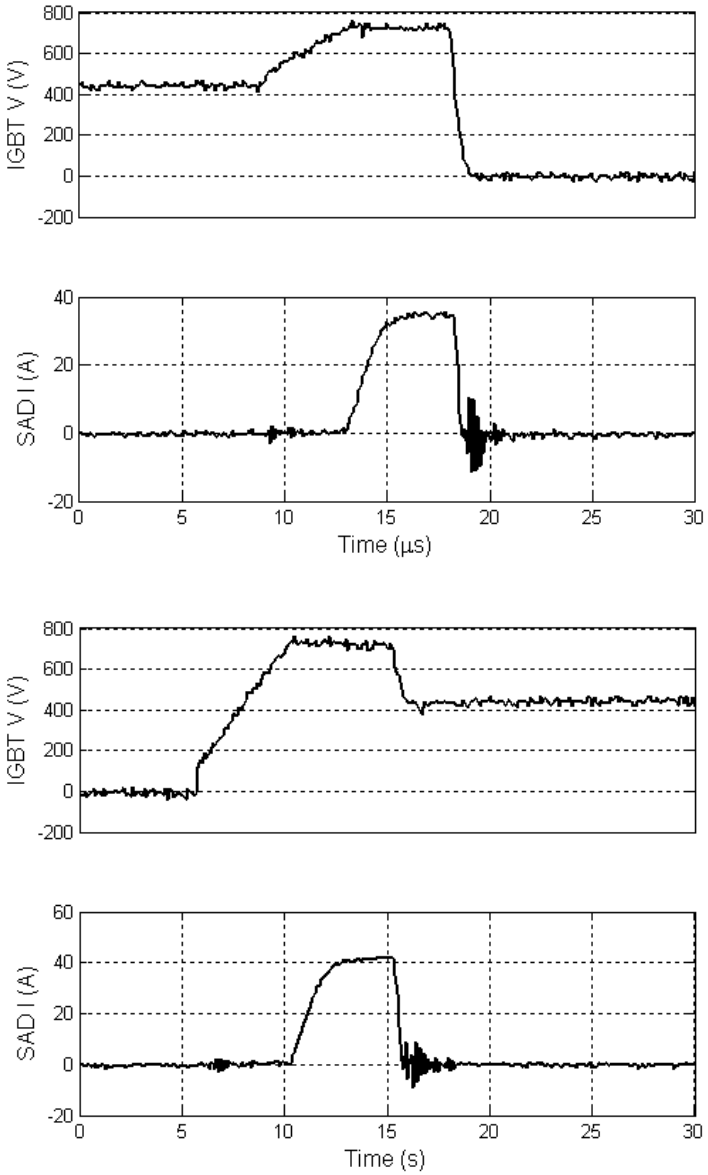


Figure 8.19 SAD current during turn-on (top) and turn-off (bottom)

It is clear from the above comparisons that the circuit behaves as predicted, with only small differences in some parameters.

8.3 Thermal calculations

The next step was to calculate power loss and ΔT_{jc} waveforms from the measured voltage and current waveforms. The calculation method is described first, followed by the results.

8.3.1 Calculation method

An example of the Matlab calculation is shown in simplified form in Appendix D. This is for an IGBT and is similar to that used for the simulations. The same method was used for diodes, except that switching losses were not calculated, the constants used to calculate $V_{CE(sat)}$ differed and a different thermal impedance curve was used.

The first step was to correct the current data for the negative DC offset and low frequency oscillation introduced by the Rogowski coil. These were handled together in two steps: adding a positive DC offset and then setting all small currents to zero. All negative voltage and current points, due to measurement inaccuracy at low scales, were also set to zero. These steps were found to alter the waveforms very little, other than to remove the desired measurement artifacts.

Next, the thermal impedance array was determined in the same way as for the simulations. Then $V_{CE(sat)}$ was calculated for small voltages in the same way as for the simulations. This was required because the measurements were not accurate enough at values low in comparison with the peak voltages measured (a few volts compared to several hundred volts). Conduction losses were calculated by multiplying voltage and current at each point, as before.

This was achieved in the same was as for the simulations (Equation 7.1). The peak voltage values were read off the measured waveforms. The maximum values of

the turn-on current transients were calculated by compensating for the errors introduced by the low sampling rate of the oscilloscope in comparison with the transient rise time. This was accomplished as follows:

1. The rise time of the current transients was determined from Figure 8.16 as about 750 ns, 14% longer than the value determined from the simulations.
2. For calculation purposes this rise time was set to 1 μs, the same as the sampling time of the oscilloscope. This change was compensated for by multiplying the calculated peak transient current by 1.2, as it was found that the current falls by approximately 20% in the 250 ns following its maximum, as shown in Figure 8.20.
3. With the entire 10 ms on period captured, turn-on waveforms such as those in Figure 8.21 were obtained. This clearly shows how the maximum IGBT current is affected by the 1 μs sampling time, while the maximum voltage is unaffected.
4. It was therefore necessary to interpolate the current data points, as shown in Figure 8.22. The current waveform was broken up into two parts: the front was modeled as a straight line and the tail as an exponential curve, as justified by the measurement of Figure 8.20. The tail is defined by the three points marked at 2, 3 and 4 μs. Its equation is determined using Matlab by exponential curve-fitting. It is plotted first. The front is defined by only one point – at 1 μs. Several lines are drawn through this point, and that line which has a 1 μs rise time is the correct one, as marked by the thick line. The new maximum current is therefore where the two curves cross (157 A in this case).
5. The maximum current determined above is now multiplied by 1.2 to obtain the estimated peak current for a 750 ns rise time. The final maximum is therefore 188 A.

Figure 8.18 shows that turn-off losses can be broken into two parts, in the same way as the manufacturer's waveform of Figure 2.4:

1. The same short fall-time used for the simulations (see Figure 7.7)
2. The extra current tail

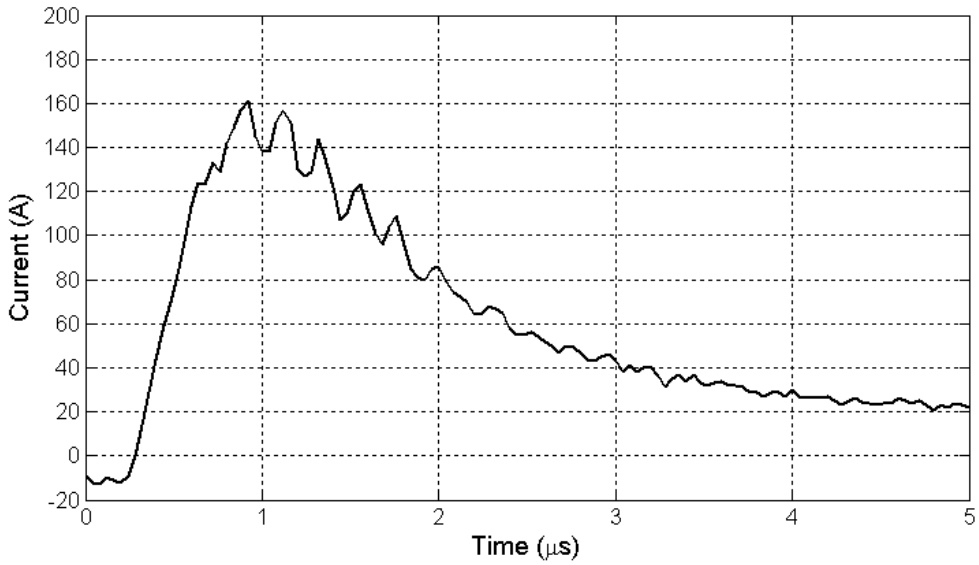


Figure 8.20 Measured IGBT turn-on current transient (magnified from Figure 8.16)

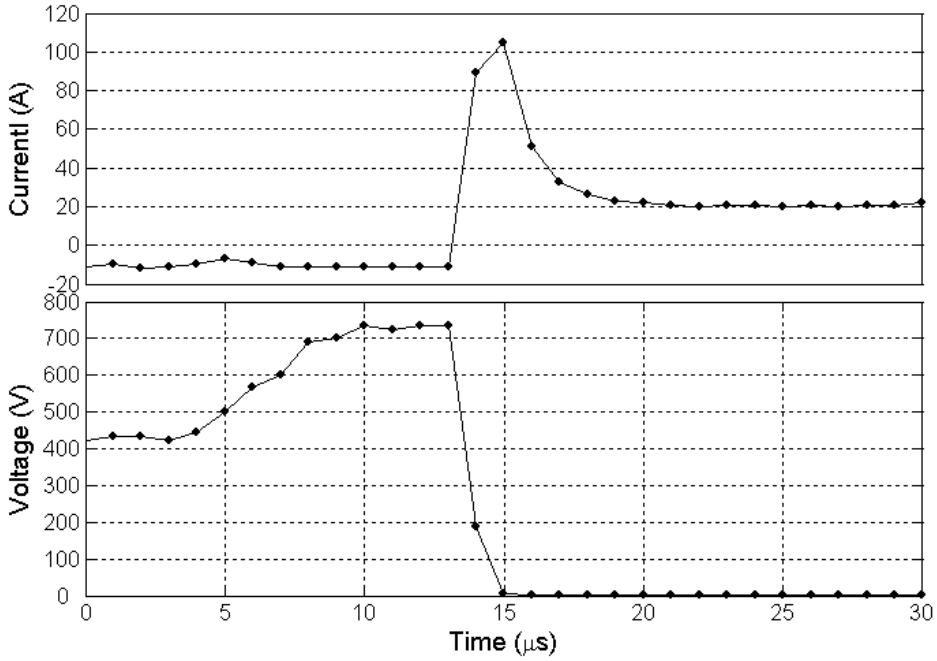


Figure 8.21 Measured IGBT turn-on current and voltage waveforms with 1 μs sampling time

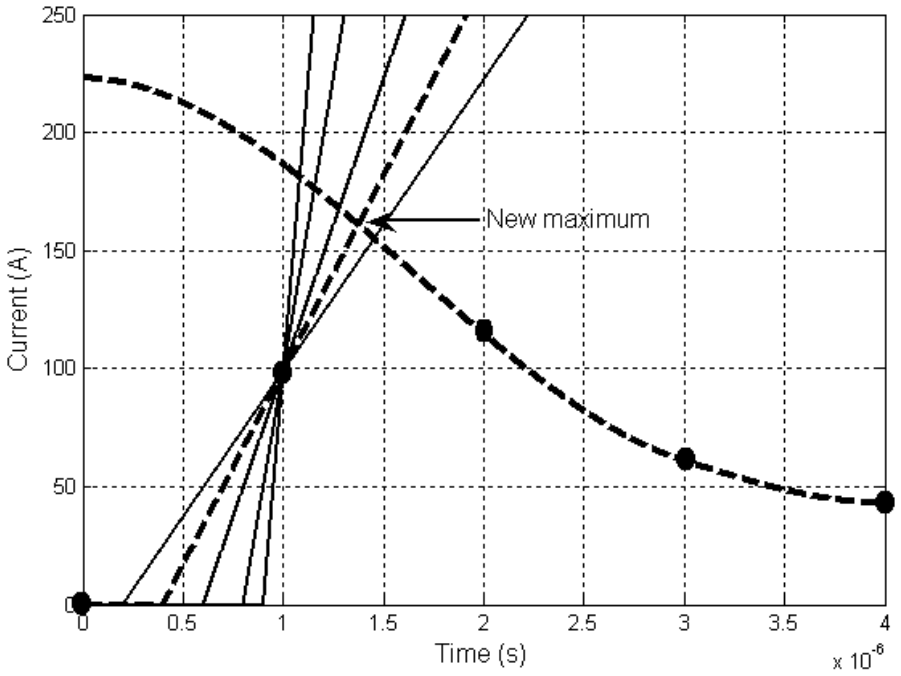


Figure 8.22 Interpolation of IGBT current data of Figure 8.21 to determine maximum turn-on transient value

The losses due to the former were calculated using Equation 7.2, as for the simulations. However, due to the large time scale compared to the turn-off time, measured as 200 ns, it was not possible to directly measure the voltage step magnitude (V_2 in Equation 7.2).

The snubber current magnitude was used to calculate this as follows:

1. Figure 8.18 shows that the snubber current after the voltage step is several μs long and is fairly constant. This magnitude can therefore be determined using a 1 μs time step.
2. V_2 is then simply the product of this snubber current and the snubber resistance (10 Ω), using Ohm's Law.
3. To further simplify the calculation, it was found that there is a constant factor relating the snubber current after turn-off to the IGBT current at turn-off (I_2 in Equation 7.2). This factor was found to be 3.5; therefore I_2 can be divided by 3.5 and multiplied by the snubber resistance to obtain V_2.

The losses due to the current tail were calculated as follows:

$$E_{off\,(tail)} = \frac{I_{tail} \cdot t_{tail}}{6} \cdot [V_2 + V_3] = \frac{I_2^2 \cdot t_{tail}}{105} \cdot \left[R_{snub} + \frac{t_{tail}}{C_{snub}} \right] \quad \text{..... (8.1)}$$

where $E_{off(tail)}$ = IGBT energy loss due to the tail current

I_{tail} = current at start of the tail

t_{tail} = duration of tail

V_2 = voltage at start of tail (see Figure 7.8)

V_3 = voltage at end of tail

I_2 = current being turned off (see Figure 7.8)

R_{snub}, C_{snub} = snubber resistor and capacitor

The first expression was obtained by simple integration, in the same way as Equation 7.2 was obtained. The second expression was used for the calculations and was obtained by substituting the following:

- Figure 8.18 shows that I_{tail} is approximately 20% of I_2
- The rate of rise of V_{CE} is governed by the snubber capacitor, therefore $V_3 = (dv_{CE}/dt).t_{tail}$
- Since the snubber current, I_{snub}, is constant during charging: $v_{CE}/dt = I_{snub}/C$
- $I_{snub} = I_2/3.5$ (as before)

Turn-off losses were once again found to be small in comparison with the turn-on losses, but were significantly larger than predicted due to the current tail.

Both turn-on and turn-off times were found to be larger than predicted. This is due to stray inductance in the circuit. This difference results in slightly larger switching losses, as expected.

Finally, the power losses and ΔT_{jc} were calculated and plotted, as before.

8.3.2 Results

The results are shown in Figures 8.23 to 8.26.

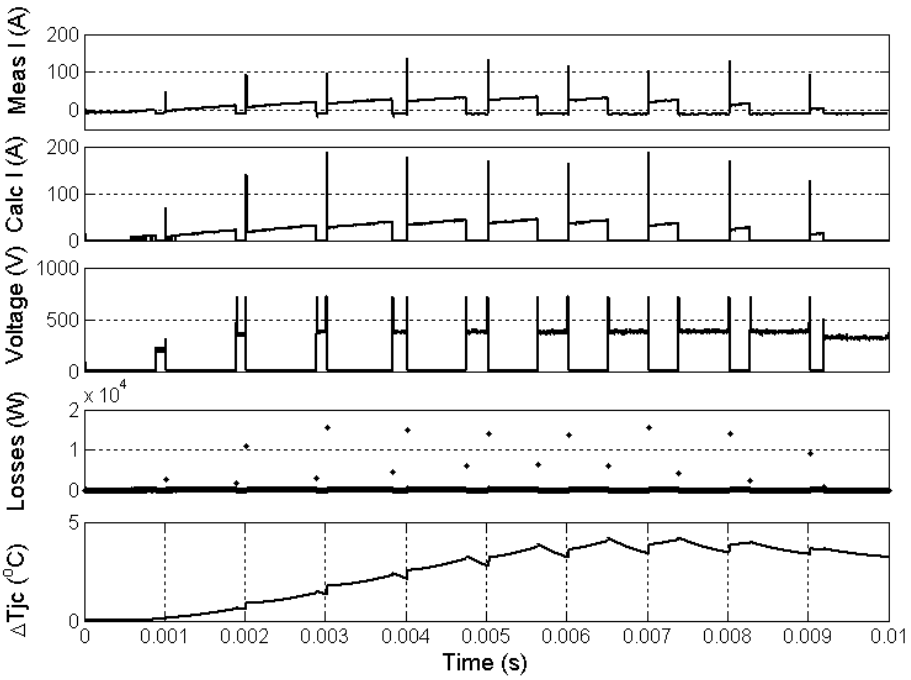


Figure 8.23 Measurements and calculations for forward-conducting IGBTs

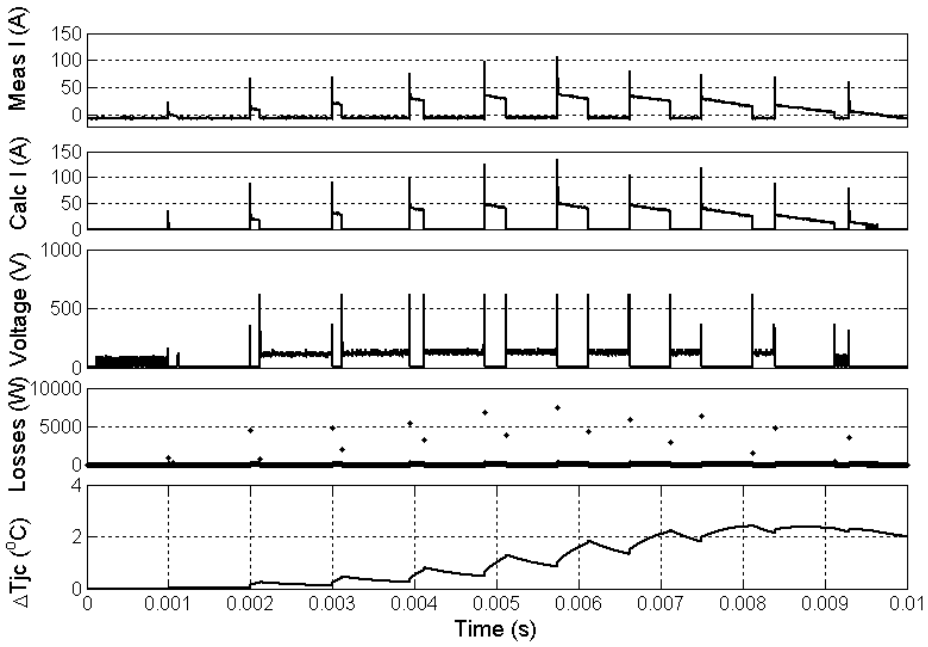


Figure 8.24 Measurements and calculations for reverse-conducting IGBTs

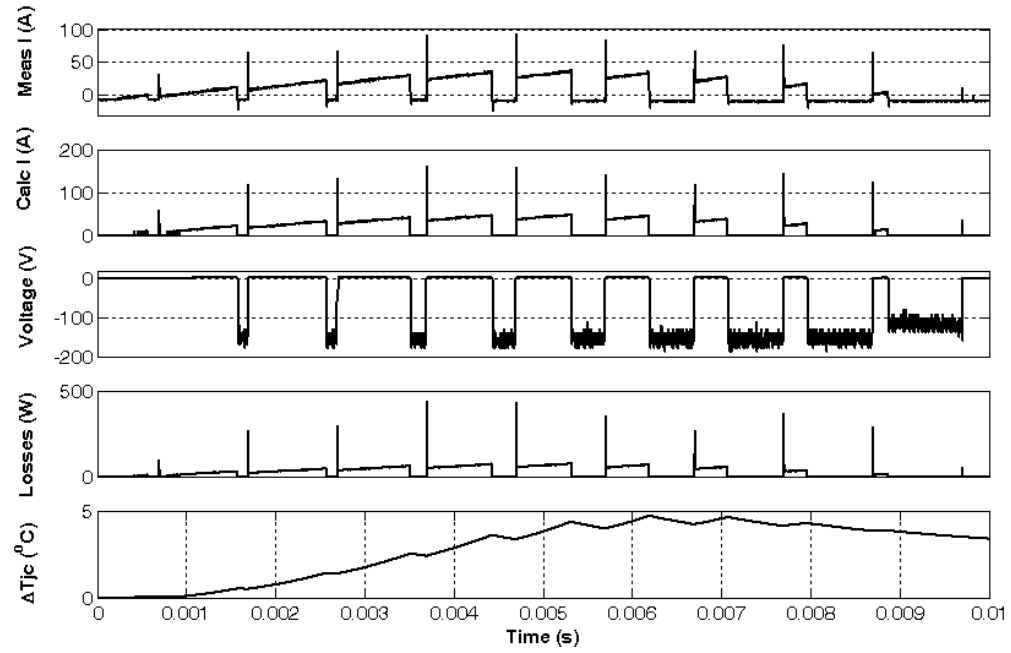


Figure 8.25 Measurements and calculations for forward-conducting diodes

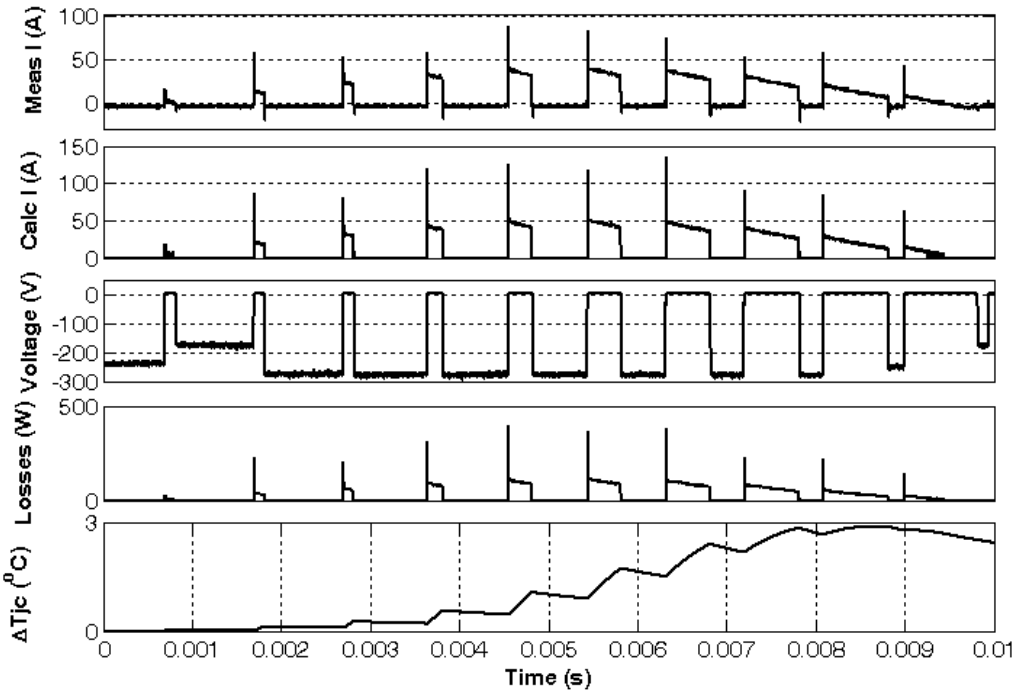


Figure 8.26 Measurements and calculations for reverse-conducting diodes

The following observations can be made about Figures 8.23 to 8.26:

1. The uppermost IGBT plots are the measured device current waveforms and the plots below them are these plots after they were processed as described above. Comparing these second plots to the predictions (Figures 7.9 and 7.10), shows that the method was a success.
2. Similarly, for the diodes the uppermost plots are the measured total waveforms (devices + snubbers), and the second plots are the results of the data manipulation. These plots compare favourably with the predictions of Figures 7.11 and 7.12.
3. The voltage plots are also as expected, with only small values affected as described as above.
4. The IGBT power plots show that the individual switching loss points are much larger than the conduction loss points, as for the simulations (the same time step was used for both).
5. Switching losses are absent from the diode power plots, as for the simulations. Once again, the power waveforms closely resemble the current waveforms.
6. The ΔT_{jc} waveforms are also similar to the predicted cases. The maximum values differ slightly from the predicted cases, but are similar, as will be shown in the next section.

8.4 Comparison with predictions

The circuit was operated at switching frequencies of 1, 2 and 3 kHz and the results were compared to the simulations. The variation in ΔT_{jc} is shown in Figure 8.27. All dashed lines are simulations and all solid lines are measurements. IGBT losses are shown in Figure 8.28 and diode losses in Figure 8.29. Average current is shown in Figure 8.30. In all instances measurement and prediction are similar. Differences can be attributed to the following:

- Higher measured IGBT switching losses are due to the current tail during turn-off, as shown in Figures 8.23 and 8.24. This results in generally

higher total losses and higher variation in ΔT_{jc}. Turn-on losses are similar due to longer turn-on but smaller peaks.

- Measured IGBT conduction losses are similar to the predictions. Differences can be attributed to measurement error, but the effect is again small.
- Measured diode conduction losses, and hence total losses and variation in ΔT_{jc}, are slightly lower than predicted, but the difference is small.

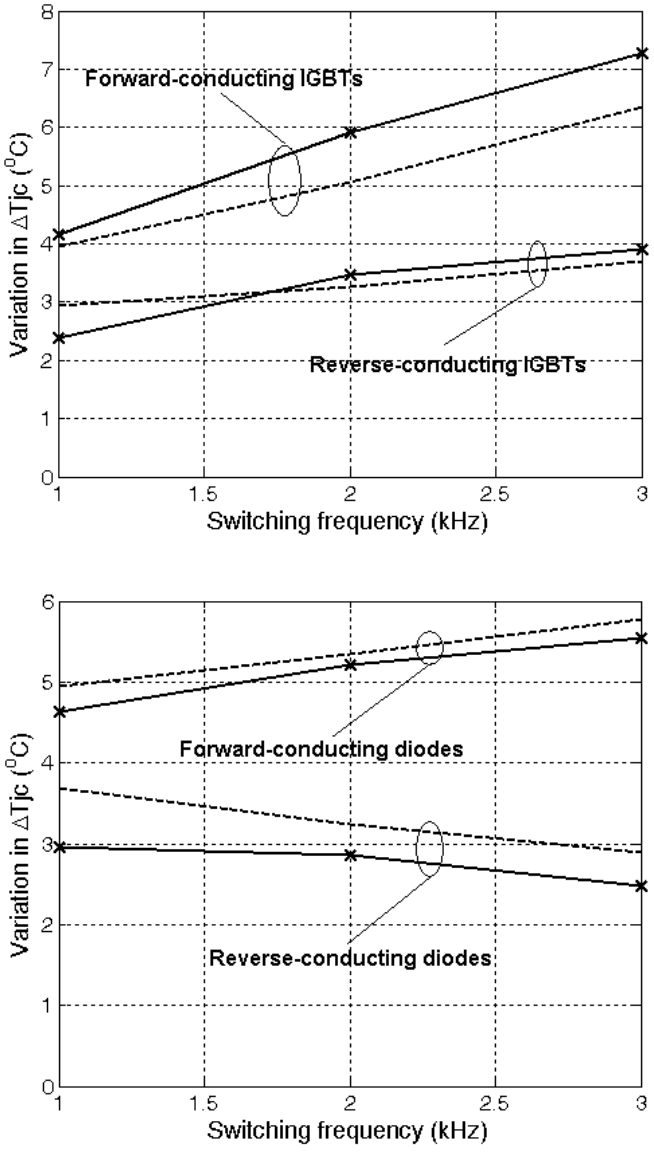


Figure 8.27 Comparison of variation in ΔT_{jc} between simulation and measurement (dashed lines = simulations; solid lines = measurements)

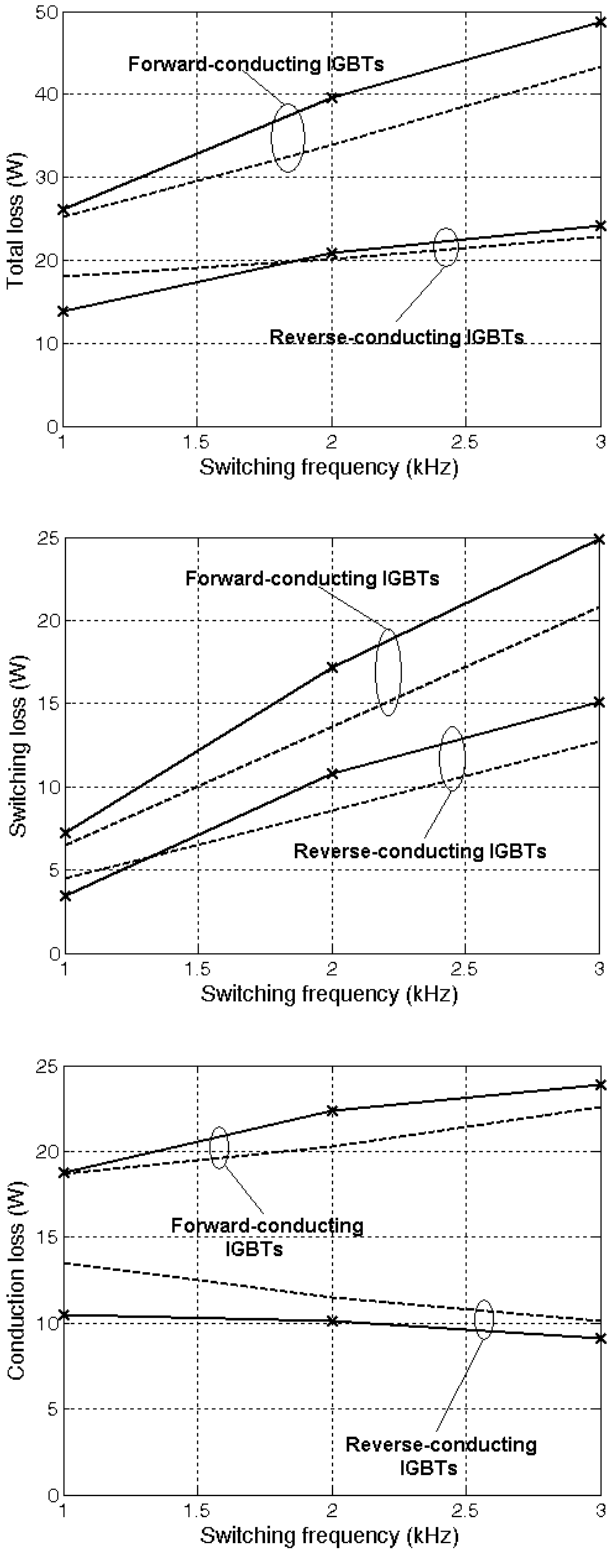


Figure 8.28 Comparison between measured and simulated average IGBT losses (dashed lines = simulations; solid lines = measurements)

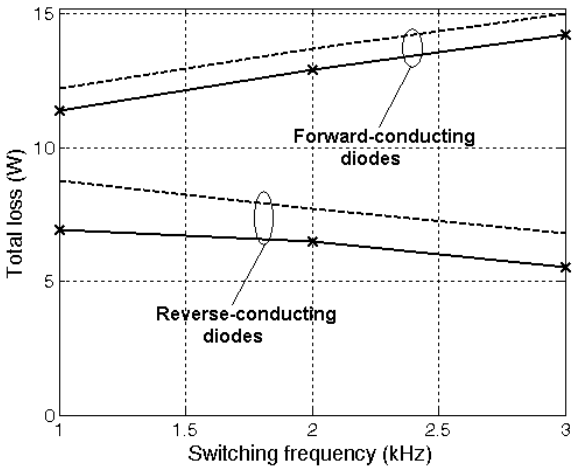


Figure 8.29 Comparison between measured and simulated diode losses (dashed lines = simulations; solid lines = measurements)

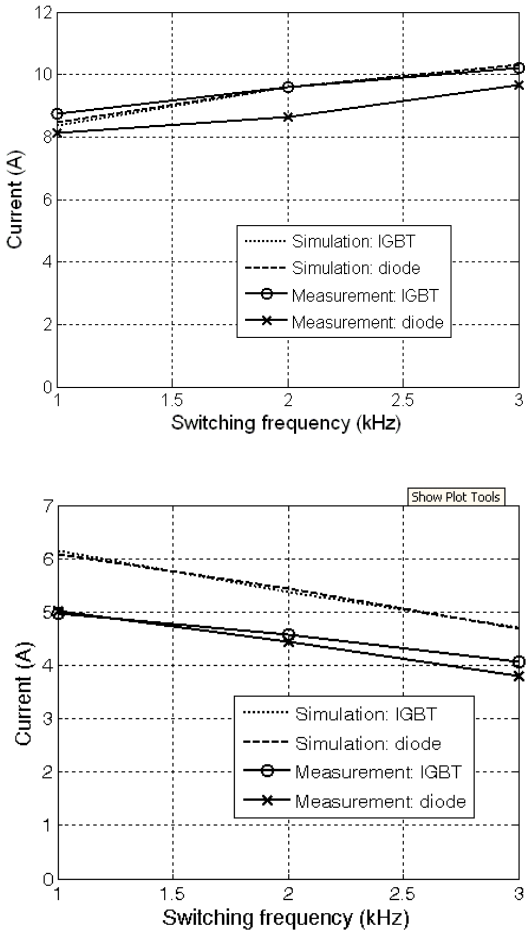


Figure 8.30 Comparison between measured and simulated average current: forward conducting devices (top), reverse-conducting devices (bottom)

8.5 Implementation issues

The above results show that the circuit meets the accuracy requirements. The effect of varying the different circuit parameters used to achieve this is now studied.

8.5.1 The effect of varying t_{on} and t_{off}

The values of t_{on} and t_{off} used were 240 ms and 1 second respectively. These values are both greater than the required minimum of 200 ms (see Section 7.1.1). The slightly longer on period was chosen to take any small variations in Z_{thjc} into account. The longer off period was needed to give the SADs sufficient time to cool down, as they were found to dissipate significant heat. This occurs for several reasons:

1. The SADs conduct current at every switching operation; therefore they dissipate greater heat at a 3 kHz switching frequency than at 1 kHz (1 second was needed for 3 kHz)
2. SADs have lower energy-handling capability than many MOVs [28] – the particular SADs were chosen because, to the author's knowledge, they have the greatest energy-handling capability of commercially available SADs
3. It is not possible to provide forced cooling for SADs, e.g. by mounting them on heatsink

It is very important to make sure that the SADs do not overheat, as this would lead to thermal runaway, causing them to fail. SADs generally fail as a short-circuit [28]; this would cause the load, and hence the DC bus, to be short-circuited. Also, SADs are expensive to replace.

The sensitivity of the results to the values of t_{on} and t_{off} is described below:

- The variation in ΔT_{jc}, the most important parameter, is not affected by t_{on} and t_{off}, as long as they are both greater than about 200 ms

- Increasing t_{on} is not recommended because this could cause excessive heating of the SADs
- Decreasing t_{on} slightly is possible, but an increase in IGBT or diode Z_{thjc} might affect the results; this is therefore also not recommended

8.5.2 The effect of different load surge arresters

The following changes may be made to the characteristics of the load surge arrester:

- Increasing the clamping voltage by adding more SADs in series would reduce individual SAD stresses, but is not recommended as the overall voltage would exceed 1.5 kV (see Section 7.1.3), and maximum device voltages would be too close to their rating of 1.2 kV.
- Reducing the clamping voltage by using fewer SADs in series is also not recommended as this would reduce IGBT switching losses and would increase SAD heating.
- Using MOVs with a similar clamping voltage is also not recommended as they would age at a fast rate due to the large number of transients conducted, and the clamping voltage is not as predictable as with SADs.
- Operation without a load surge arrester would cause device destruction due to the voltages exceeding their ratings, as shown by the simulated waveforms of Figure 8.31. The figure shows that the peak load voltage would be about 3 kV, exceeding the device rating of 1.2 kV.

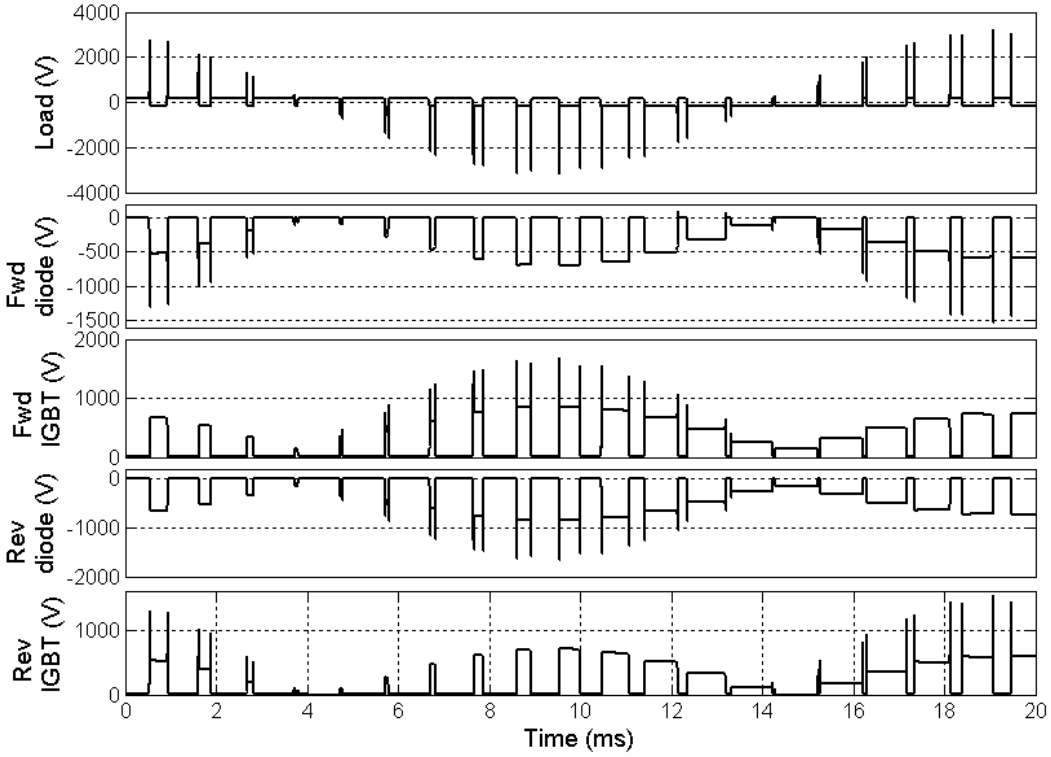


Figure 8.31 Predicted voltages without load SADs

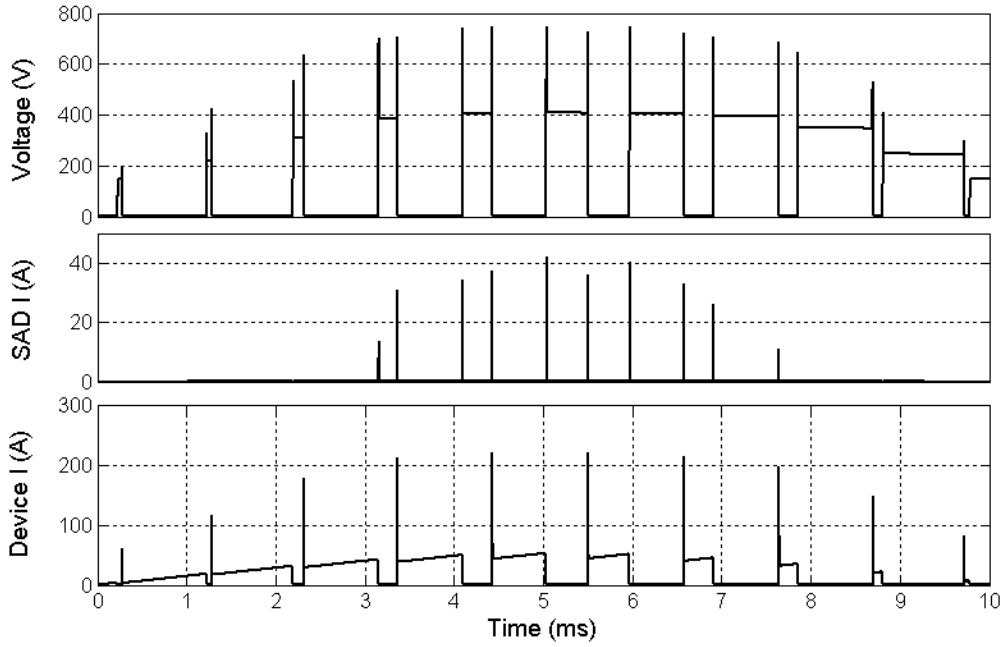
8.5.3 The effect of varying the dead time

The dead time is set on the driver card to 10 μs, the largest value allowed. Decreasing this value would be advantageous because this would reduce the time for the device voltages to increase, reducing the conduction time of the SADs. However, reducing this time so much that the SADs do not conduct any current would reduce the switching losses, which is not desirable, as the SADs are an effective way of controlling the switching losses – as shown by the very predictable measured voltage transient peaks of Figures 8.11-8.14.

As an example, the simulated waveforms of a forward-conducting IGBT of Figure 8.32 show that if the dead time is shortened to 5 μs, only the largest transients are clamped by the SADs, as shown by the SAD current waveform. This results in a rounder envelope to the voltage and current waveforms during the 10 ms on

period (cf. Figure 7.9). The effect of the shorter dead time is also evident in the turn-on and turn-off waveforms.

However, the IGBT turn-off waveform of Figure 8.18 shows that there is a small tail current. This tail current, approximately 4 μs long, prohibits decreasing the dead time, because if an IGBT is turned on while the previous IGBT is still conducting current – even a small current – the DC bus will be short-circuited.



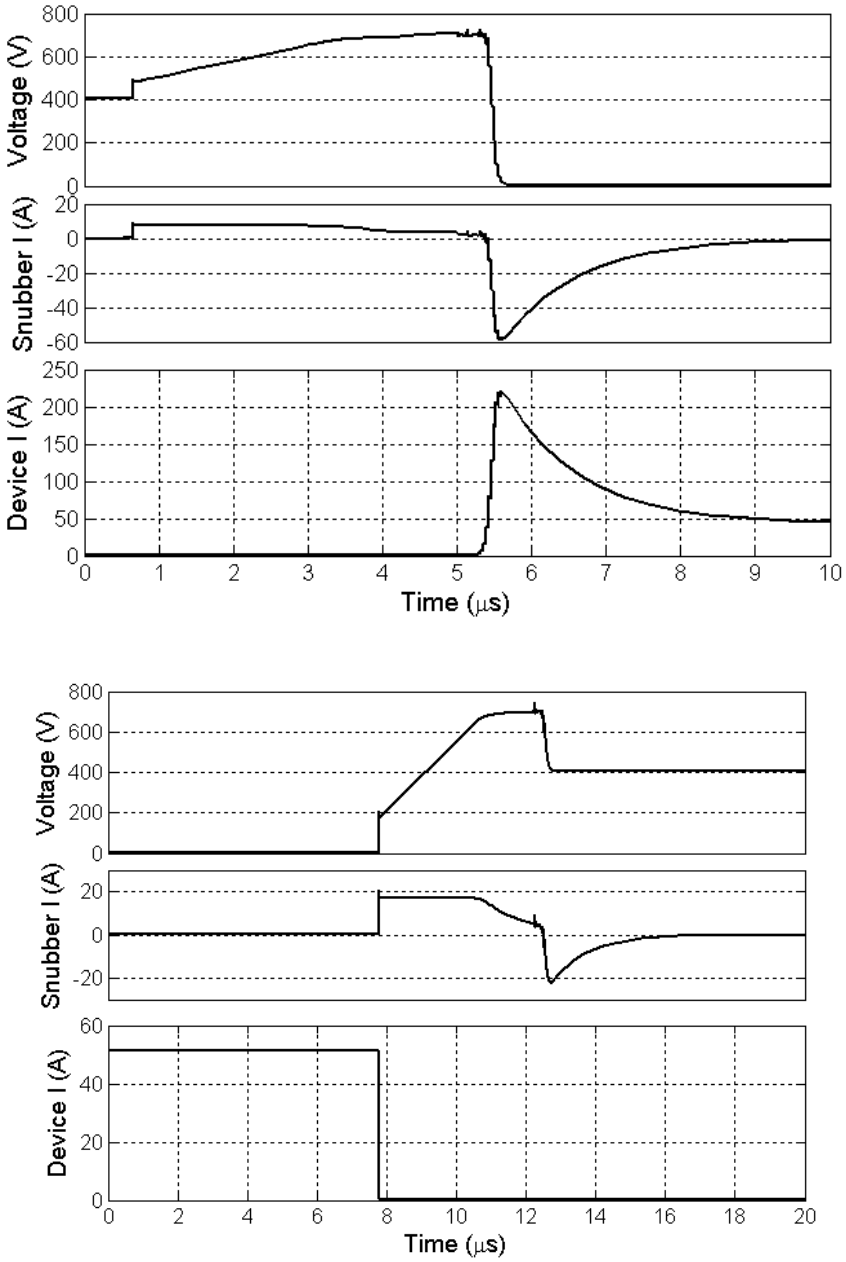


Figure 8.32 Predicted effect of halving the dead time to 5 μs on forward-conducting IGBT waveforms: 10 ms on period (top), turn-on (centre) and turn-off (bottom)

8.5.4 The effect of varying snubber values

Snubber resistance and capacitance, together with the SADs, determine circuit behaviour during switching, and hence affect IGBT switching losses. As shown

above, 10 Ω and 100 nF gave acceptable results. Changing them would have the following effects:

- The resistance was chosen as low as possible to increase IGBT switching losses without damaging the devices due to excessive turn-on current. Since this current is as high as the manufacturer recommends [76] reducing the resistance is not recommended. This is illustrated by Figure 8.33, where the effect of halving the resistor on forward-conducting IGBT waveforms is shown. The peak IGBT turn-on current has increased to about 350 A, due to the turn-on snubber current doubling to about 100 A. The rise time remains unchanged, while the transient decays faster due to the shorter snubber time constant. Turn-off losses are further decreased because the magnitude of the voltage step during turn-off is halved.

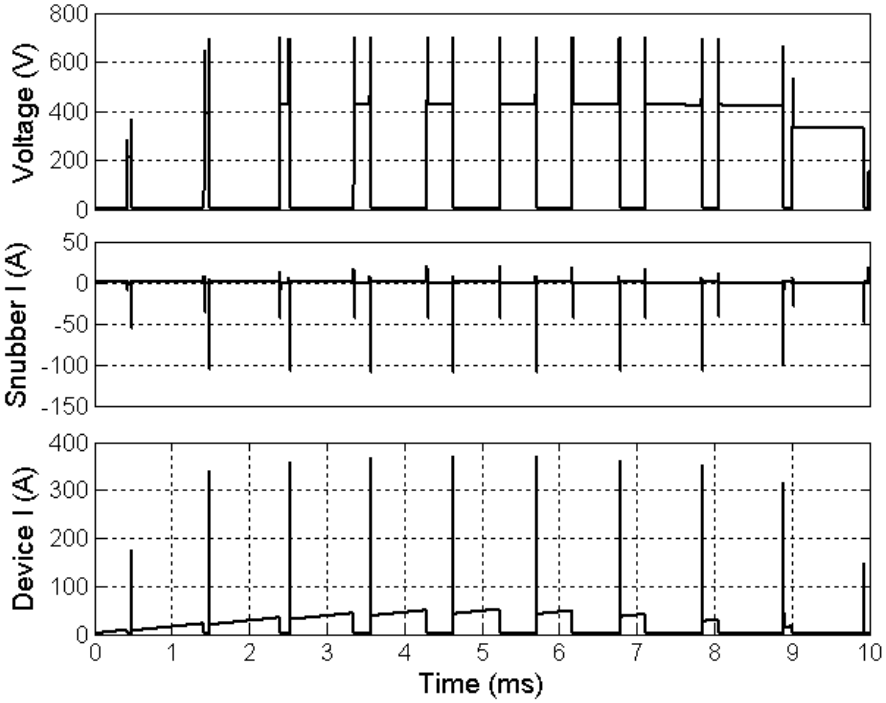


Figure 8.33 Simulated forward-conducting IGBT waveforms with all snubber resistors set to 5 Ω (capacitance remains at 100 nF)

- Increasing the resistance is possible, but would result in lower IGBT turn-on current and hence in lower switching losses and lower variation in ΔT_{jc}, and is therefore not recommended. As an example, the effect of doubling

the resistance to 20 Ω is shown in Figure 8.34. The peak IGBT turn-on current has been reduced to about 140 A, due to the turn-on snubber current almost halving to about 30 A. The rise time remains unchanged, while the decay time increases due to the larger snubber time constant. Turn-off losses are doubled because the voltage step doubles in magnitude; but turn-off losses are still negligible in comparison with turn-on losses.

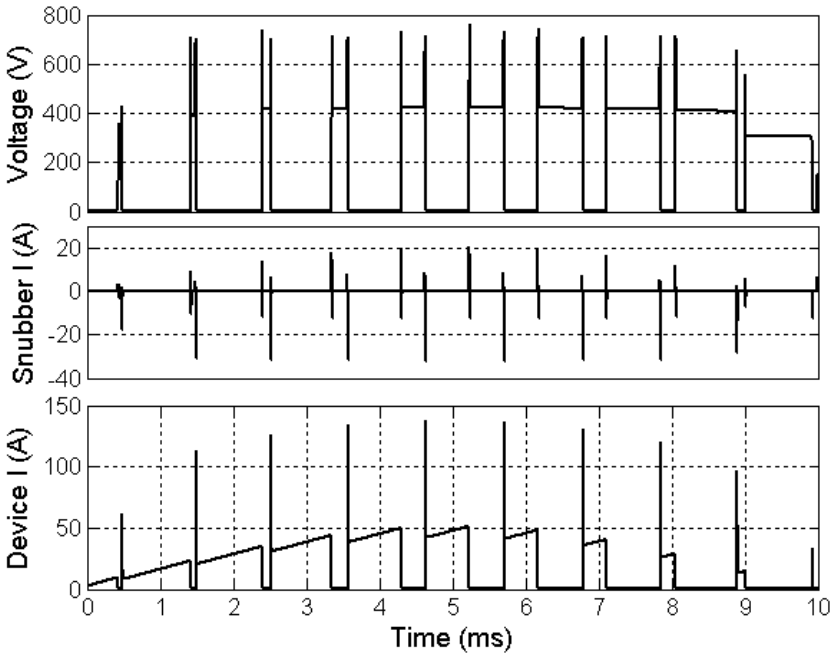


Figure 8.34 Simulated forward-conducting IGBT waveforms with all snubber resistors set to 20 Ω (capacitance remains at 100 nF)

- Decreasing the snubber capacitance has only a small effect, as shown in Figure 8.35. Halving the capacitance results in a slight reduction in the peak transient current. Once again the front time does not change, but the decay time decreases due to the change in snubber time constant. Turn-off waveforms remain unchanged.
- Doubling the snubber capacitance has the opposite effect, as shown in Figure 8.36: the peak transient current increases slightly and the decay time increases. The turn-on rise time and turn-off waveforms once again remain virtually unchanged.

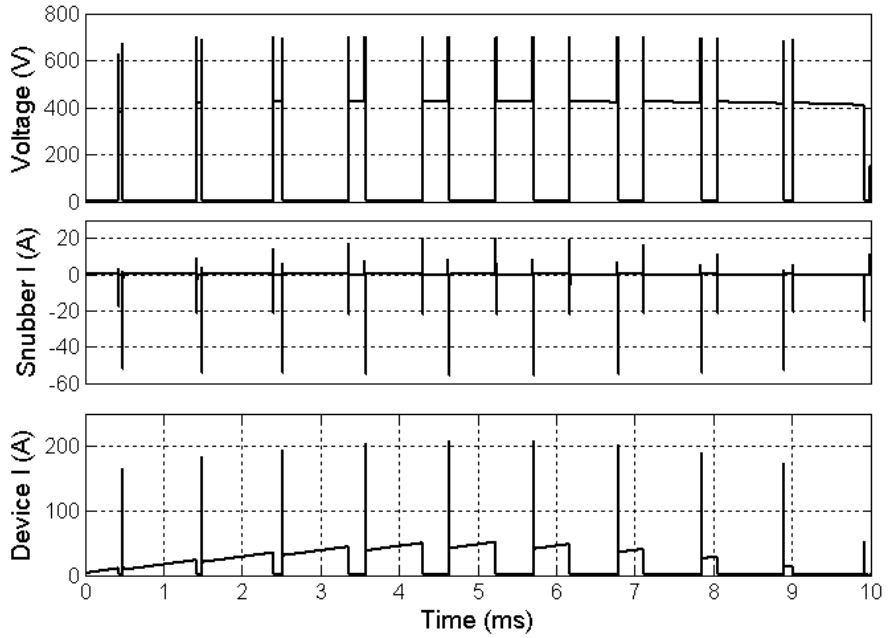


Figure 8.35 Simulated forward-conducting IGBT waveforms with all snubber capacitors set to 50 nF (resistance remains at 10 Ω)

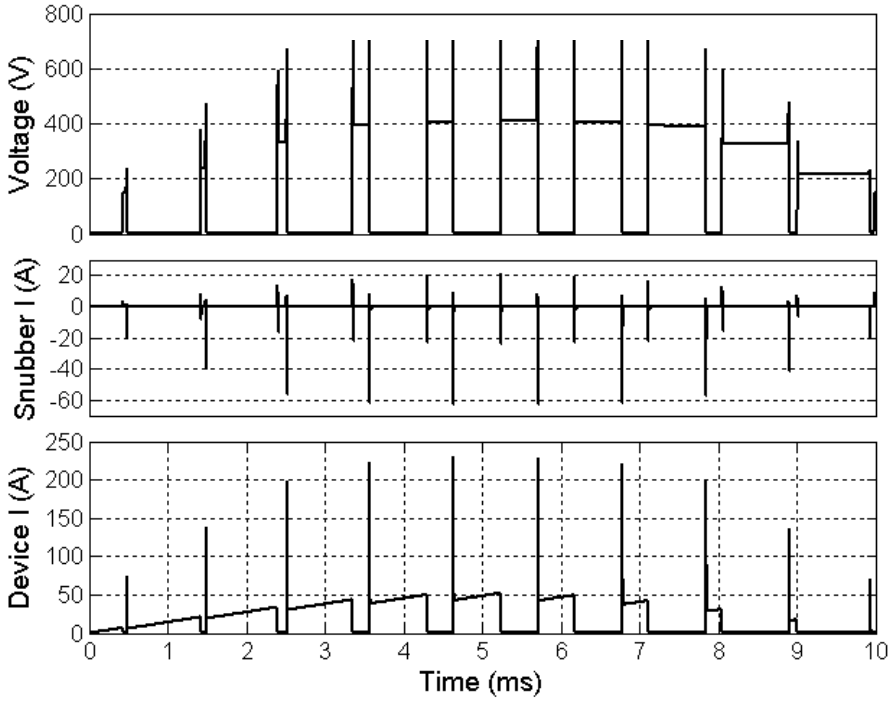


Figure 8.36 Simulated forward-conducting IGBT waveforms with all snubber capacitors set to 200 nF (resistance remains at 10 Ω)

8.5.5 The effect of varying R_G

The above simulations have shown how the values of snubber resistance and capacitance determine the magnitude of the turn-on current transient, and that the clamping voltage of the SAD sets the magnitude of the voltage transient during turn-on. These two parameters can therefore be used to control the turn-on losses, and hence the total losses and the variation in ΔT_{jc}. A third way of controlling turn-on losses is by changing the turn-on time (measured as 700 ns). This is controlled by the value of the gate resistance, R_G, which affects how fast the IGBTs turn on and off. R_G was set to 15 Ω, as recommended by the manufacturer.

Measurements were made of the turn-on transient using values of R_G from 3.6 Ω to the maximum allowed by the driver card (22 Ω). Turn-off was not considered because of its relatively small contribution to the overall switching losses. The rise time is plotted over this range in Figure 8.37. The peak current and decay time remained virtually unchanged, as expected.

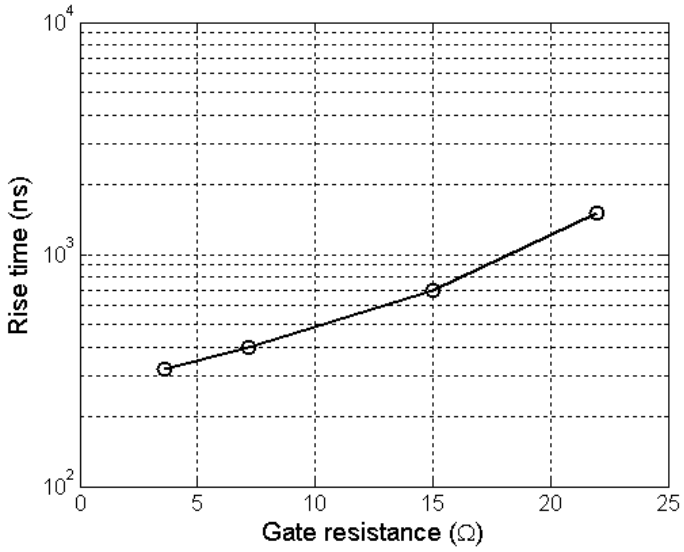


Figure 8.37 Measured rise time of the IGBT turn-on current transient as a function of gate resistance (R_G)

The figure shows that IGBT turn-on losses can also be controlled by varying R_G. The greater R_G is, the longer it takes the devices to turn on and hence the larger the losses. Conversely, switching losses can be reduced by reducing R_G. It must

be noted, however, that if R_G is too large, then the IGBT may be turned off too slowly during a fault condition and hence leading to possible destruction of the device. Reducing R_G too far could result in large voltage transients during turn-off under fault conditions, which could lead to the SADs being stressed too highly. Also, reducing switching losses is not desirable in this application. Therefore, 15 Ω is a suitable value of R_G.

8.5.6 Using different gate drivers

When one or more IGBT gate drivers (of the SKHI 23/12 type) were replaced by SKHI 23/17 gate drivers, because no other SKHI 23/12 drivers were available, waveforms such as those of Figure 8.38 were observed.

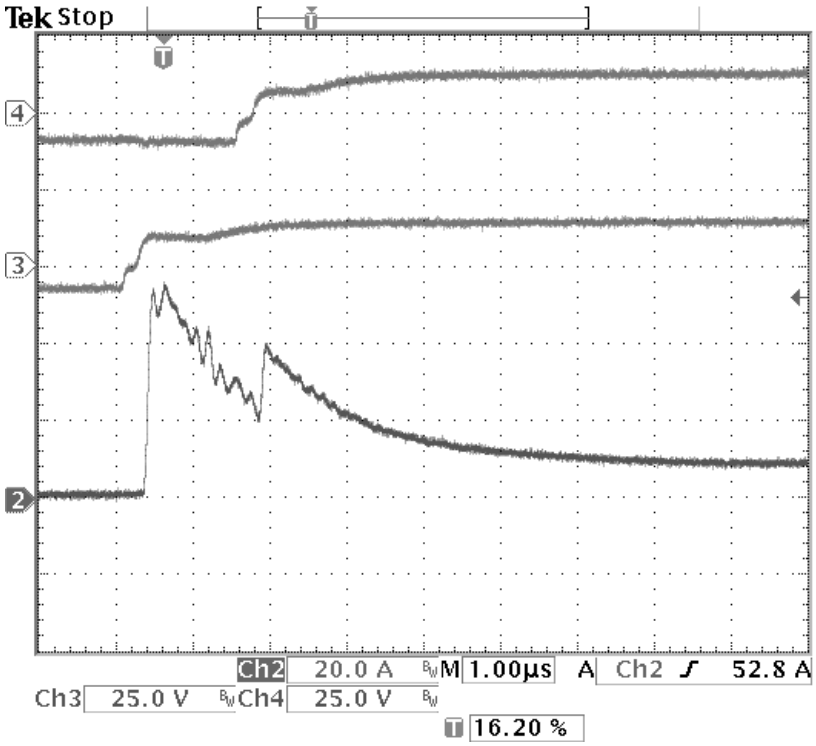


Figure 8.38 Using two different types of IGBT gate drivers: Ch2 = IGBT g2 turn-on current, Ch3 = IGBT g2 gate voltage, Ch4 = IGBT h2 gate voltage

It is clear that one gate driver responds slightly faster than the other, resulting in a distorted turn-on current transient. This caused one or more drivers to sense a short circuit at higher current levels and hence to turn their IGBTs off. The only

difference between the two drivers is their voltage rating: the SKHI 23/12 is rated at 1.2 kV and the SKHI23/17 at 1.7 kV. Therefore, all gate drivers must be of the same type.

8.5.7 Adding DC bus snubber capacitance

A capacitance of few μF on the DC bus was found to have no significant effect on the load or device waveforms. This was confirmed in the laboratory, where two snubber capacitors, of 2 μF each, were added to the DC bus at each half of the inverter.

8.6 Conclusion

The implementation of the modified inverter circuit has been described, as well as the measurements obtained. These measurements were found to be sufficiently similar to the predictions, validating the model. Several implementation issues were also discussed, showing the effect of changing various parameters and validating the choice of circuit parameters made.

9. CONCLUSION

The Insulated Gate Bipolar Transistor (IGBT), despite having several advantages, has been known to fail in the field when subjected to repeated variations in its power dissipation – this is known as power cycling. In this work, a novel power cycling test method for IGBTs and their free-wheeling diodes was proposed and verified.

A literature review was performed (Chapters 3, 4 and 5), which revealed that the parameter that most affects IGBT lifetime under power cycling conditions is the variation in its junction-case temperature difference (ΔT_{jc}).

The behaviour of a conventional single phase inverter (H-bridge) was then quantified by simulation in Chapter 6. The results showed the effect of load power factor and switching frequency on current, power loss and ΔT_{jc} waveforms. Based on these simulations and on the results of the literature review, a list of criteria for an alternating current (AC) test circuit were derived (Section 7.1.1).

A new test circuit, modified from the conventional circuit, was then designed and its performance was compared with the above criteria and with the conventional circuit by simulation in Chapter 7. Finally, the new circuit was built and its performance was compared to the predictions (Chapter 8). The measurements were found to be sufficiently similar to the simulation results, hence validating its performance.

The test circuit is novel for the following reasons:

1. The stresses on IGBTs and free-wheeling diodes used in a conventional H-bridge driving a high power factor inductive load are reproduced with the modified circuit using a low power factor inductive load to an adequate degree of accuracy, significantly reducing the energy costs of running such a test

2. IGBT switching losses are not actively reduced, as is normal practice, but instead are increased and controlled to produce the desired IGBT losses
3. Diodes are also tested, but do not have any significant switching losses, as total diode losses need to be reduced to achieve the required stresses under conventional conditions

Advantages of this method are:

1. The substantial energy cost savings of running a test
2. The circuit allows replication of the normal operating conditions of many applications, as switching losses may influence IGBT aging under power cycling conditions
3. It uses pulse width modulation (PWM) control, and hence the current and voltage waveforms are similar to the conventional circuit
4. The test setup was kept as simple as possible

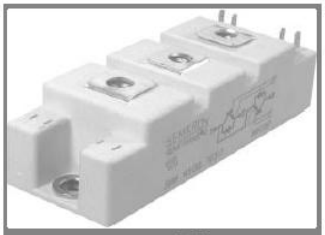
Disadvantages of the method are:

1. The duration of one power cycle (1.24 s) is not as short as it could be using a conventional H-bridge (400 ms), due to the heat dissipation constraints of the silicon avalanche diodes (SADs) used as surge arresters. This cannot be changed as the SADs are a necessary part of the circuit.
2. Twice the number of devices than are used in a conventional H-bridge are needed in the proposed circuit, resulting in higher cost; however, this also results in twice the number of data points per test, and is therefore not necessarily a disadvantage.

The above tradeoffs are needed to obtain the significant energy cost savings that use of a low power factor load brings, as such aging tests usually run for extended periods for time.

APPENDIX A – SKM 100 GB 123 D DATA SHEET [11]

SKM 100GB123D



SEMITRANS™ 2

IGBT Modules

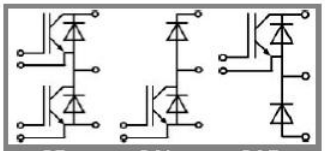
SKM 100GB123D
SKM 100GAL123D
SKM 100GAR123D

Features

- MOS input (voltage controlled)
- N channel, Homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 x I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (10 mm) and creepage distances (20 mm)

Typical Applications

- Switching (not for linear use)



GB GAL GAR

Absolute Maximum Ratings		T_c = 25 °C, unless otherwise specified	
Symbol	Conditions	Values	Units
IGBT			
V_{CES}		1200	V
I_C	T_c = 25 (80) °C	100 (90)	A
I_{CRM}	t_p = 1 ms	150	A
V_{GES}		± 20	V
T_{vj}, (T_{stg})	$T_{OPERATION} \leq T_{stg}$	- 40 ... + 150 (125)	°C
V_{isol}	AC, 1 min.	2500	V
Inverse diode			
I_F	T_c = 25 (80) °C	95 (65)	A
I_{FRM}	t_p = 1 ms	150	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	720	A
Freewheeling diode			
I_F	T_c = 25 (80) °C	130 (90)	A
I_{FRM}	T_c = 25 (80) °C, t_p = 1 ms	200 (180)	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	1100	A

Characteristics		T_c = 25 °C, unless otherwise specified			
Symbol	Conditions	min.	typ.	max.	Units
IGBT					
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 2 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, V_{CE} = V_{CES}, T_j = 25 (125) °C		0,1	0,3	mA
$V_{CE(TO)}$	T_j = 25 (125) °C		1,4 (1,6)	1,6 (1,8)	V
r_{CE}	V_{GE} = 15 V, T_j = 25 (125) °C		14,6 (20)	18,6 (25,3)	mΩ
$V_{CE(sat)}$	I_C = 75 A, V_{GE} = 15 V, chip level		2,5 (3,1)	3 (3,7)	V
C_{ies}	under following conditions		5	6,6	nF
C_{oes}	V_{GE} = 0, V_{CE} = 25 V, f = 1 MHz		0,72	0,9	nF
C_{res}			0,38	0,5	nF
L_{CE}				30	nH
$R_{CC'+EE'}$	res., terminal-chip T_c= 25 (125) °C		0,75 (1)		mΩ
$t_{d(on)}$	V_{CC} = 600 V, I_C = 75 A		30	60	ns
t_r	R_{Gon} = R_{Goff} = 15 Ω, T_j = 125 °C		70	140	ns
$t_{d(off)}$	V_{GE} = ± 15 V		450	600	ns
t_f			70	90	ns
E_{on} (E_{off})			10 (8)		mJ
Inverse diode					
V_F = V_{EC}	I_F = 75 A; V_{GE} = 0 V; T_j = 25 (125) °C		2 (1,8)	2,5	V
$V_{(TO)}$	T_j = 125 () °C			1,2	V
r_T	T_j = 125 () °C		12	15	mΩ
I_{RRM}	I_F = 75 A; T_j = 25 (125) °C		27 (40)		A
Q_{rr}	di/dt = 800 A/µs		3 (10)		µC
E_{rr}	V_{GE} = V				mJ
FWD					
V_F = V_{EC}	I_F = 75 A; V_{GE} = 0 V, T_j = 25 (125) °C		1,85 (1,6)	2,2	V
$V_{(TO)}$	T_j = 125 () °C			1,2	V
r_T	T_j = 125 () °C		9	11	mΩ
I_{RRM}	I_F = 75 A; T_j = 25 (125) °C		30 (45)		A
Q_{rr}	di/dt = A/µs		3,5 (11)		µC
E_{rr}	V_{GE} = V				mJ
Thermal characteristics					
$R_{th(j-c)}$	per IGBT			0,18	K/W
$R_{th(j-c)D}$	per Inverse Diode			0,5	K/W
$R_{th(j-c)FD}$	per FWD			0,36	K/W
$R_{th(c-s)}$	per module			0,05	K/W
Mechanical data					
M_s	to heatsink M6	3		5	Nm
M_t	to terminals M5	2,5		5	Nm
w				160	g

 © by SEMIKRON

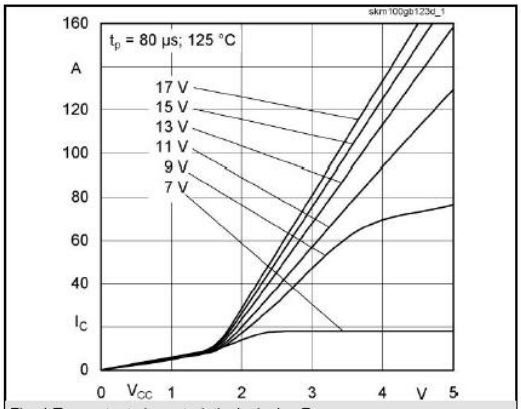


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

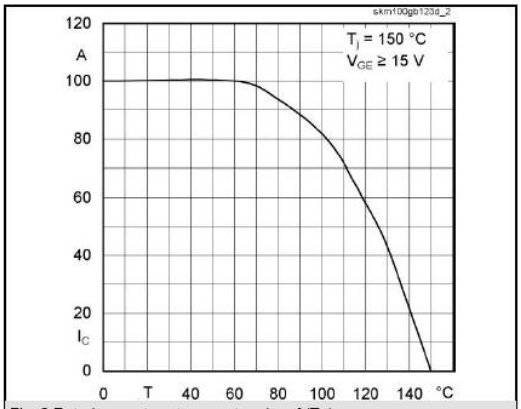


Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

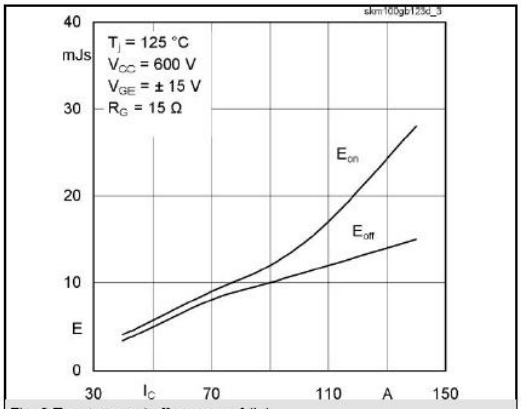


Fig. 3 Typ. turn-on /-off energy = f (I_C)

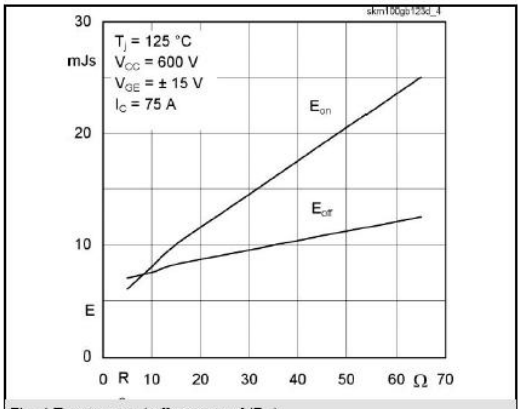


Fig. 4 Typ. turn-on /-off energy = f (R_G)

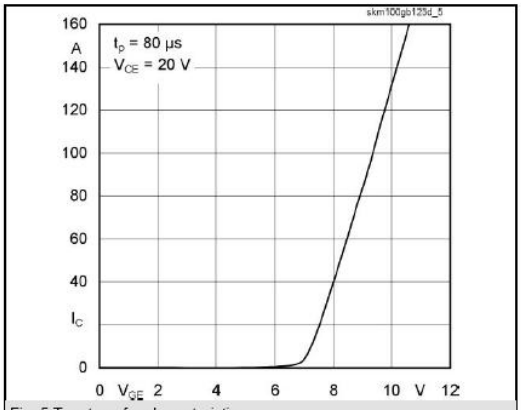


Fig. 5 Typ. transfer characteristic

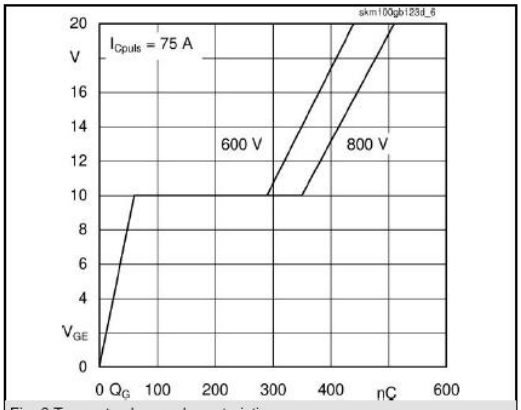


Fig. 6 Typ. gate charge characteristic

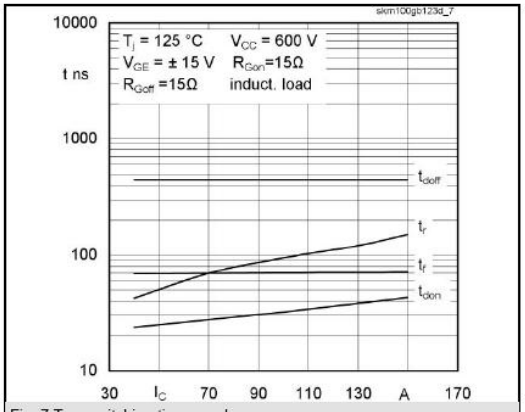


Fig. 7 Typ. switching times vs. I_C

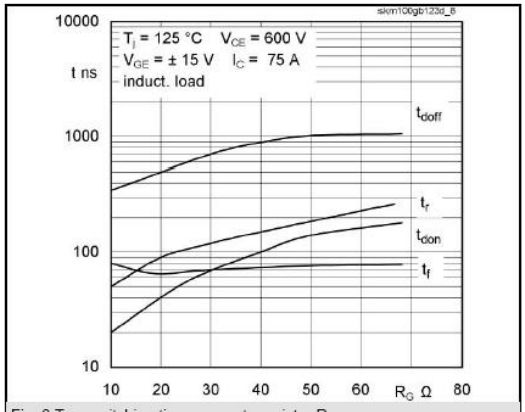


Fig. 8 Typ. switching times vs. gate resistor R_G

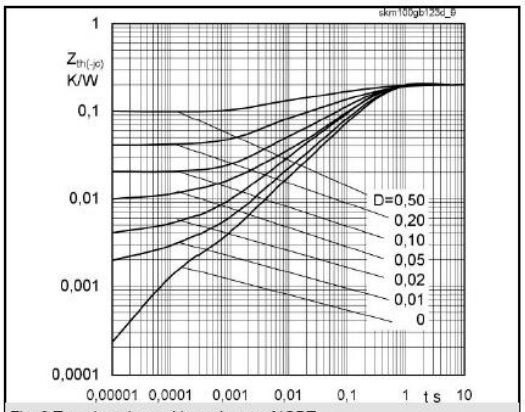


Fig. 9 Transient thermal impedance of IGBT

$Z_{th(j-c)} = f(t_p)$; $D = t_p / t_c = t_p * f$

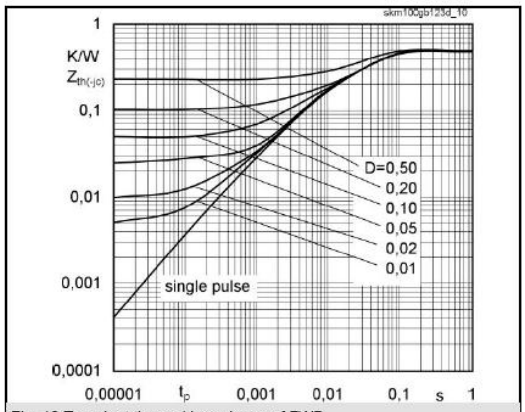


Fig. 10 Transient thermal impedance of FWD

$Z_{th(j-c)} = f(t_p)$; $D = t_p / t_c = t_p * f$

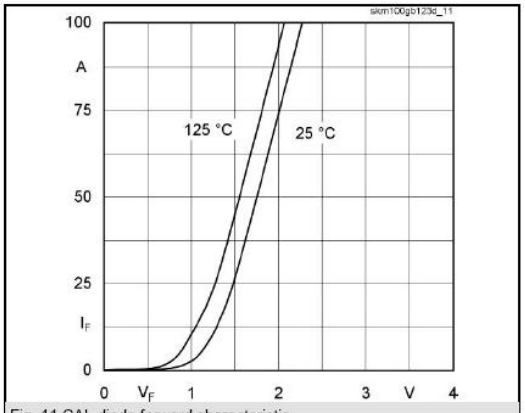


Fig. 11 CAL diode forward characteristic

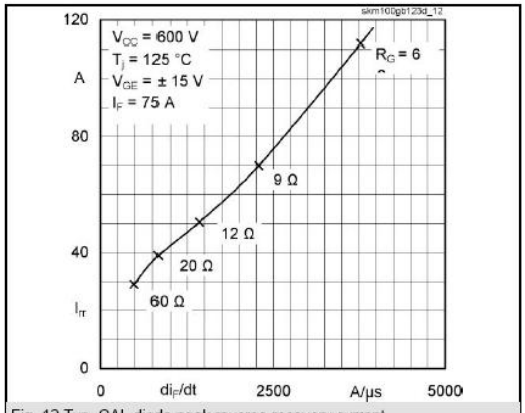


Fig. 12 Typ. CAL diode peak reverse recovery current

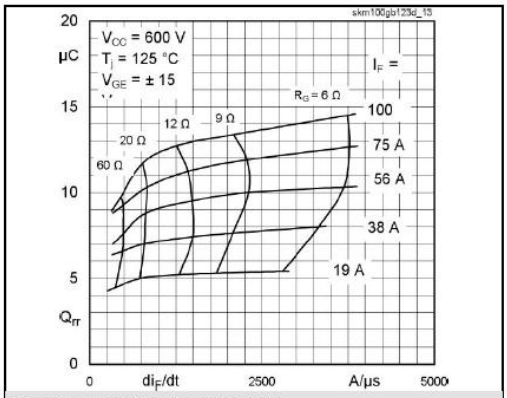
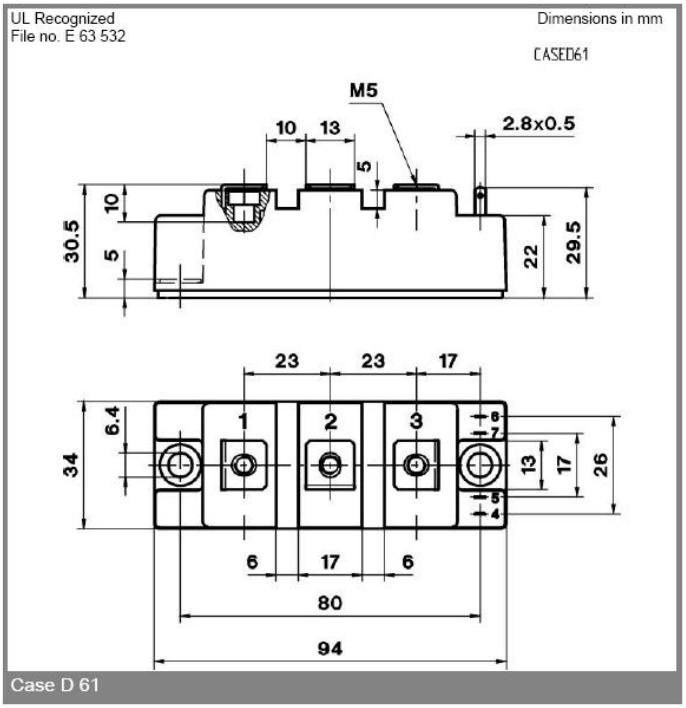
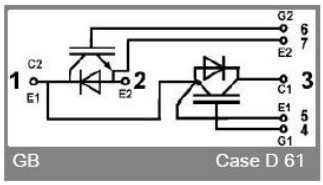


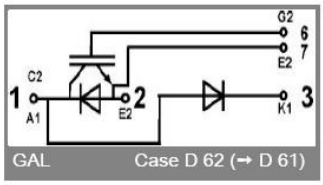
Fig. 13 Typ. CAL diode recovered charge



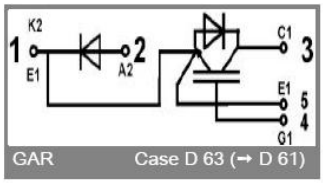
Case D 61



GB Case D 61



GAL Case D 62 (→ D 61)



GAR Case D 63 (→ D 61)

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

APPENDIX B – MATLAB CODE FOR ΔT_{JC} CALCULATION FROM SIMULINK MODEL

B.1 IGBT

```
% This is a complete calculation to determine the instantaneous conduction
% losses, switching losses, total losses, and variation in ΔTJC. There are 2
% input arrays: time and IGBT collector current; these must be of the same
% length. The total duration is 20 ms, i.e. one % 50 Hz cycle.

% Part 1: set all required constants

Vcc = 537;                                  % DC link voltage
VceN = 3.5;                                 % Rated Vce(sat) at rated current
Icrated = 100;                              % Rated current
Vce0 = 1.5;                                 % Approximated threshold Vce value
Vccref = 600;                               % Reference dc link voltage for
                                            % switching loss calculations
tsim = 20e-3;                               % Total duration of simulation (one
                                            % 50 Hz cycle in this case)
tstep = 2e-6;                               % Simulation time step

totalstep = tsim/tstep;                     % Total number of iterations

% Part 2: load electrical input data

load I1.out;                                % Current data
load t1.out;                                % Time data. There is a current data
                                            % point at each time point

% Part 3: sample switching energy curves

Icgraph = [0 10 20 30 40 50 60 70 80 90 100];
Eongraph = [0 1 2 3 4 5 7 9 10 12 15]*0.001;
Eoffgraph = [1 1 1 2 3 4 6 8 9 10 11]*0.001;
                                            % Sampling curves of Fig. 2 of App.
                                            % A; Icgraph = x axis, Eongraph =
                                            % turn-on energy, Eoffgraph = turn-
                                            % off energy

% Part 4: plot imported collector current waveform

figure(1);                                  % Plot collector current in Fig. 1
axes('FontSize',12);                        % Set font size for axis labels
xlim([0 tsim]);                             % Set scale on x axis
plot(t1,I1);                                % Plot collector current
grid on;                                    % Insert grid on graph
xlabel('Time (s)','FontSize',14);           % Label axes and give graph a title
ylabel('Current (A)','FontSize',14);
title('Collector current','FontSize',18);
```

```
% Part 5: calculate and plot instantaneous conduction losses

figure(2);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;                                    % All data points to be held on
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Conduction losses','FontSize',18);

for n = 1:totalstep
    Icpulse(n) = interp1(t1,I1,n*tstep,'cubic');
                                            % Resample the current with chosen
                                            % time step
    Vcesat(n) = ((VceN-Vce0)*(Icpulse(n)/Icrated)) + Vce0;
                                            % Calculate V_CE(sat) at each time step
                                            % from Fig. 1 of App. A, using
                                            % equation from [69]
    Pcond(n) = Icpulse(n)*Vcesat(n);        % Calculate conduction loss at each
                                            % time step
    Ptotal(n) = Pcond(n);                   % Set total loss equal to conduction
                                            % loss for addition of switching
                                            % losses later
    Zthjc(n) = (0.00001*(1 - exp(((-1)*n*tstep)/277.9483)))
             + (0.081752*(1 - exp(((-1)*n*tstep)/0.023123)))
             + (0.081752*(1 - exp(((-1)*n*tstep)/0.03813)))
             + (0.019953*(1 - exp(((-1)*n*tstep)/0.017818)))
             + (0.005559*(1 - exp(((-1)*n*tstep)/0.003289)))
             + (0.010965*(1 - exp(((-1)*n*tstep)/0.000555)));
                                            % Sample thermal impedance equation,
                                            % given by the manufacturer [9], for
                                            % use later
    plot(n*tstep,Pcond(n),'.');             % Plot conduction loss data on Fig. 2
end

% Part 6: calculate and plot instantaneous switching losses

figure(3);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Switching losses','FontSize',18);

for n = 3:totalstep
    if Icpulse(n-1) < 5                     % Is device switching on?
       onflag(n) = 1;
       if Icpulse(n) >= 5                   % If yes: perform loop
          Eon1(n) = interp1(Icgraph,Eongraph,Icpulse(n));
                                            % Normalized turn-on energy
          Eon(n) = Eon1(n)*(Vcc/Vccref);    % Actual turn-on energy
          Pon(n) = Eon(n)/tstep;            % Turn-on power
          Ptotal(n) = Pon(n);               % Total power at time step
          plot(n*tstep,Pon(n),'o');         % Plot turn-on power
       end
    end
```

```
    if Icpulse(n-1) >= 5                    % Is device switching off?
       offflag(n) = 1;
       if Icpulse(n) < 5                    % If yes: perform loop
          Eoff1(n-1) = interp1(Icgraph,Eoffgraph,Icpulse(n-1));
                                            % Normalized turn-off energy
          Eoff(n-1) = Eoff1(n-1)*(Vcc/Vccref);
                                            % Actual turn-off energy
          Poff(n-1) = Eoff(n-1)/tstep;      % Turn-off power
          Ptotal(n) = Poff(n-1);            % Total power at time step
          plot((n)*tstep,Poff(n-1),'x');    % Plot turn-off power
       end
    end
end

% Part 7: plot instantaneous total power losses

figure(4);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Total losses','FontSize',18);

plot((1:n)*tstep,Ptotal(1:n),'.');

% Part 8: calculate and plot instantaneous total variation in ΔTJC

figure(5);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('\DeltaTjc (^oC)','FontSize',14);
title('Temperature','FontSize',18);

lnH = plot(0,0,'.');
drawnow

Tjtotal = zeros(1,totalstep);               % Freeing sufficient contiguous
                                            % memory

for n = 1:totalstep
     Z1 = Zthjc(1,1:n);                     % Creating positive thermal impedance
                                            % pulses for superposition – refer to
                                            % Figure 6.3
     d = length(Z1);
     Zup = Z1(d+1-(1:d));
     Pup = Ptotal(1,1:n);                   % Creating positive power pulses for
                                            % superposition
     Tjup = Pup.*Zup;                       % Calculating pos. temperature pulses
     Pdown = Pup(1,1:n-1);                  % Creating negative power pulses
     Zdown = Zup(1,2:n);                    % Creating neg. thermal imp. pulses
     Tjdown = Pdown.*Zdown;                 % Calculating negative temperature
                                            % pulses
     Tjtotal(n) = sum(Tjup) - sum(Tjdown);
```

```
end                                          % Calculating total temperature

plot((1:n)*tstep,Tjtotal(1:n),'.');
```

B.2 Diode

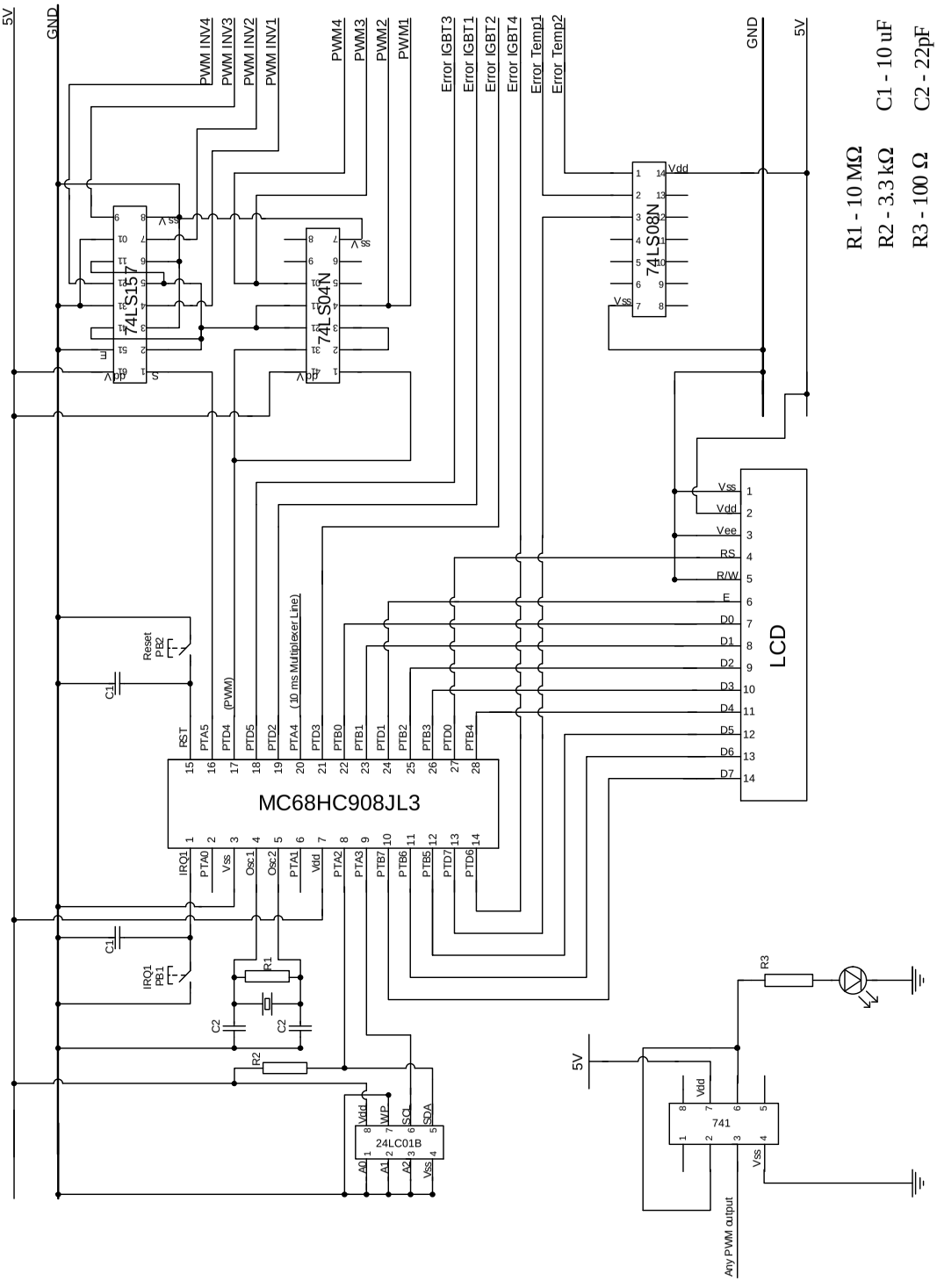
```
% This is a complete calculation to determine the instantaneous conduction
% losses, switching losses, total losses, and variation in ΔTJC. There are 2
% input arrays: time and IGBT collector current; these must be of the same
% length. The total duration is 20 ms, i.e. one 50 Hz cycle.

% Part 1: set all required constants

Vcc = 537;                                   % DC link voltage
VceN = 2.2;                                  % Rated Vce(sat) at rated current
Icrated = 100;                               % Rated current
Vce0 = 1;                                    % Approximated threshold Vce value
Vccref = 600;                                % Reference dc link voltage for switching
                                             % loss calculations
tsim = 20e-3;                                % Total duration of simulation (one 50 Hz
                                             % cycle in this case)
tstep = 2e-6;                                % Simulation time step


totalstep = tsim/tstep;                      % Total number of iterations

% Part 2: load electrical input data

load I1.out;                                 % Current data
load t1.out;                                 % Time data. There is a current data point
                                             % at each time point

% Part 3: create turn-off energy array

Icgraph = [0 19 38 56 75 100];
Eoffgraph = [0 5.2 7.3 9.5 11.2 12.8]*1e-6*Vcc;
                                             % Sampling manufacturer's diode recovery
                                             % charge curve of Fig 13 of App. A;
                                             % Icgraph = x axis, Eoffgraph = charge for
                                             % RG = 12 Ω multiplied by Vcc to get energy

% Part 4: plot imported anode current waveform

figure(1);                                   % Plot anode current in Fig. 1
axes('FontSize',12);                         % Set font size for axis labels
xlim([0 tsim]);                              % Set scale on x axis
plot(t1,I1);                                 % Plot anode current as a function of time
grid on;                                     % Insert grid on graph
xlabel('Time (s)','FontSize',14);            % Label axes and give graph a title
ylabel('Current (A)','FontSize',14);
title('Anode current','FontSize',18);
```

```
% Part 5: calculate and plot instantaneous conduction losses

figure(2);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;                                % All data points to be held on
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Conduction losses','FontSize',18);
for n = 1:totalstep
    Icpulse(n) = interp1(t1,I1,n*tstep,'cubic');
                                        % Resample the current with chosen time
                                        % step
    Vcesat(n) = ((VceN-Vce0)*(Icpulse(n)/Icrated)) + Vce0;
                                        % Calculate V_CE(sat) at each time step from
                                        % Fig. 11 of App. A, using eq. from [69]
    Pcond(n)=Icpulse(n)*Vcesat(n);      % Calculate conduction loss at each time
                                        % step
    Ptotal(n) = Pcond(n);               % Set total loss equal to conduction loss
                                        % for addition of switching losses later
    Zthjc(n) = (0.00001*(1 - exp(((-1)*n*tstep)/277.9483)))
             + (0.25923*(1 - exp(((-1)*n*tstep)/0.0398)))
             + (0.153993*(1 - exp(((-1)*n*tstep)/0.023411)))
             + (0.046238*(1 - exp(((-1)*n*tstep)/0.013045)))
             + (0.036308*(1 - exp(((-1)*n*tstep)/0.001806)))
             + (0.004217*(1 - exp(((-1)*n*tstep)/0.001146)));
                                        % Sample thermal impedance equation, given
                                        % by the manufacturer [9], for future use
    plot(n*tstep,Pcond(n),'.');         % Plot conduction loss data on Fig. 2
end

% Part 6: calculate and plot instantaneous switching losses

figure(3);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Switching losses','FontSize',18);

for n = 3:totalstep
    if Icpulse(n-1) >= 5                % Is device switching off?
       offflag(n) = 1;
       if Icpulse(n) < 5                % Device is switching off: perform loop
          Eoff1(n-1) = interp1(Icgraph,Eoffgraph,Icpulse(n-1));
                                        % Normalized turn-off energy
          Eoff(n-1) = Eoff1(n-1)*(Vcc/Vccref);
                                        % Actual turn-off energy
          Poff(n-1) = Eoff(n-1)/tstep;
                                        % Turn-off power
          Ptotal(n) = Poff(n-1);        % Total power at time step
          plot((n)*tstep,Poff(n-1),'x');
       end                              % Plot turn-off power
    end
end
```

```
% Part 7: plot instantaneous total power losses

figure(4);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('Instantaneous power (W)','FontSize',14);
title('Total losses','FontSize',18);

plot((1:n)*tstep,Ptotal(1:n),'.');


% Part 8: calculate and plot instantaneous total variation in ΔTJC

figure(5);
axes('FontSize',12);
xlim([0 tsim]);
grid on;
hold on;
xlabel('Time (s)','FontSize',14);
ylabel('Tjc (^oC)','FontSize',14);
title('Temperature','FontSize',18);

lnH = plot(0,0,'.');
drawnow

Tjtotal = zeros(1,totalstep-10);

for n = 1:totalstep-10                % Same method as for IGBT
     Z1 = Zthjc(1,1:n);
     d = length(Z1);
     Zup = Z1(d+1-(1:d));
     Pup = Ptotal(1,1:n);
     Tjup = Pup.*Zup;
     Pdown = Pup(1,1:n-1);
     Zdown = Zup(1,2:n);
     Tjdown = Pdown.*Zdown;
     Tjtotal(n) = sum(Tjup) - sum(Tjdown);
end

plot((1:n)*tstep,Tjtotal(1:n),'.');
```

APPENDIX C – CONTROLLER CIRCUIT

Hardware Implementation - Circuit Diagram



APPENDIX D – MATLAB CODE FOR ΔT_{JC} CALCULATION FROM MEASUREMENTS

```
% This is a complete calculation for an IGBT to determine the instantaneous
% conduction losses, switching losses, total losses and variation in ΔTJC. There
% are 3 input arrays: time and IGBT voltage and current; these must be of the
% same length. The total duration is 10 ms, i.e. only the half of 50 Hz load
% cycle that the IGBT conducts load current.

% Part 1: set all required constants

Ioffset = 10;                          % Correct current offset due to Rogowski
                                       % coil measurement error
tsim = 10e-3;                          % Total simulation time

VceN = 3.5;                            % Rated Vcesat at rated current
Icrated = 100;                         % Rated current
Vce0 = 1.5;                            % Approximated threshold Vce value

% Part 2: load electrical input data

load InputData.m;                      % Load data saved from oscilloscope (saved
                                       % as spreadsheet format, headers deleted
                                       % and saved as Matlab file)
t = InputData(:,1);                    % First column = time
I = InputData(:,2);                    % Second column = current
V = InputData(:,3);                    % Third column = voltage

% Part 3: correct data values

dur = max(t) – min(t);
totalstep = length(t);                 % Total number of data points (10,000)
tstep = dur/totalstep;                 % Time step = total time/no. of points

for n = 1:totalstep                    % Correct offset
        I(n) = I(n) + Ioffset;
end

for n = 1:totalstep                    % Set small currents to zero
        if abs(I(n))<6
           I(n) = 0;
        end
end

for n = 1:totalstep                    % Delete negative currents
        if I(n)<0
           I(n) = 0;
        end
end

for n = 1:totalstep                    % Delete negative voltages
        if V(n)<0
           V(n) = 0;
        end
```

```
end

% Part 4: create thermal impedance array

                                    % Same method as for simulations
for n = 1:totalstep
        Zthjc(n) = (0.00001*(1 - exp(((-1)*n*tstep1)/277.9483)))
                 + (0.081752*(1 - exp(((-1)*n*tstep1)/0.023123)))
                 + (0.081752*(1 - exp(((-1)*n*tstep1)/0.03813)))
                 + (0.019953*(1 - exp(((-1)*n*tstep1)/0.017818)))
                 + (0.005559*(1 - exp(((-1)*n*tstep1)/0.003289)))
                 + (0.010965*(1 - exp(((-1)*n*tstep1)/0.000555)));
end

% Part 5: calculate V_CE(sat)
                                    % Calculate VCE(sat) for small voltages
for n = 1:totalstep                 % using same method as simulations
    if abs(Ie2Vint(n))<80
       Vint(n) = ((VceN-Vce0)*(Iint(n)/Icrated)) + Vce0;
    end
end

% Part 6: enter switching times

ton1=1020;                          % Set samples at which turn-on occurs
ton2=2021;                          % (read manually off current plot)
ton3=3022;
ton4=4022;
ton5=5023;
ton6=6024;
ton7=7025;
ton8=8025;
ton9=9026;

toff1=891;                          % Set samples at which turn-off occurs
toff2=1891;                         % (read manually off current plot)
toff3=2892;
toff4=3836;
toff5=4748
toff6=5638;
toff7=6515;
toff8=7392;
toff9=8281;
toff10=9193;

% Part 7: correct turn-on current values

Iint(ton1)=59*1.2;                  % Correct turn-on current transients for
Iint(ton2)=118*1.2;                 % sampling errors
Iint(ton3)=156*1.2;
Iint(ton4)=147*1.2;
Iint(ton5)=142*1.2;
Iint(ton6)=138*1.2;
Iint(ton7)=157*1.2;
Iint(ton8)=141*1.2;
Iint(ton9)=107*1.2;
Iint(ton10)=65*1.2;
```

```
% Part 8: calculate conduction losses

for n = 1:totalstep
    Ptotal(n) = abs(Iint(n)*Vint(n));
end

% Part 9: calculate switching losses

Ptotal(ton1)=(Iint(ton1)*340*0.75e-6)/(6*tstep);
Ptotal(ton2)=(Iint(ton2)*680*0.75e-6)/(6*tstep);
Ptotal(ton3)=(Iint(ton3)*720*0.75e-6)/(6*tstep);
Ptotal(ton4)=(Iint(ton4)*730*0.75e-6)/(6*tstep);
Ptotal(ton5)=(Iint(ton5)*720*0.75e-6)/(6*tstep);
Ptotal(ton6)=(Iint(ton6)*720*0.75e-6)/(6*tstep);
Ptotal(ton7)=(Iint(ton7)*720*0.75e-6)/(6*tstep);
Ptotal(ton8)=(Iint(ton8)*720*0.75e-6)/(6*tstep);
Ptotal(ton9)=(Iint(ton9)*620*0.75e-6)/(6*tstep);
Ptotal(ton10)=(Iint(ton10)*410*0.75e-6)/(6*tstep);

Ptotal(toff1) = ((10*10*10*0.2e-6)/(6*3.5*tstep))
                +(((10*10*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff2) = ((24*24*10*0.2e-6)/(6*3.5*tstep))
                +(((24*24*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff3) = ((32*32*10*0.2e-6)/(6*3.5*tstep))
                +(((32*32*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff4) = ((39*39*10*0.2e-6)/(6*3.5*tstep))
                +(((39*39*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff5) = ((45*45*10*0.2e-6)/(6*3.5*tstep))
                +(((45*45*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff6) = ((46*46*10*0.2e-6)/(6*3.5*tstep))
                +(((46*46*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff7) = ((45*45*10*0.2e-6)/(6*3.5*tstep))
                +(((45*45*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff8) = ((37*37*10*0.2e-6)/(6*3.5*tstep))
                +(((37*37*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff9) = ((28*28*10*0.2e-6)/(6*3.5*tstep))
                +(((28*28*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));
Ptotal(toff10) = ((17*17*10*0.2e-6)/(6*3.5*tstep))
                 +(((17*17*5e-6)*(10+(5e-6/100e-9)))/(tstep*105));

% Part 10: calculate temperature

for n = 1:totalstep                  % Same method as for simulations
     Z1 = Zthjc(1,1:n);
     d = length(Z1);
     Zup = Z1(d+1-(1:d));
     Pup = Ptotal(1,1:n);
     Tjup = Pup.*Zup;
     Pdown = Pup(1,1:n-1);
     Zdown = Zup(1,2:n);
     Tjdown = Pdown.*Zdown;
     Tjtotal(n) = sum(Tjup) - sum(Tjdown);
end

plot((1:n)*tstep,Tjtotal(1:n),'.');
```

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