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Digital processing of partial discharge signals

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If an 8-bit analogue-to-digital converter is used and the entire mains cycle is converted, each cycle involves the storage of 400 000 bytes of information for a sampling rate of 20MHz. If a conversion is carried out for each discharge, and each conversion takes up 10 bytes of memory, the data will still occupy 10 times the memory occupied by the system which stores only the peak value and time of occurrence.

c. Limitation in the speed with which the data can be transferred to memory by a microprocessor.

If a 20MHz analogue-to-digital converter is used the data will be updated every 50 ns, during which time the microprocessor has to detect the change in data, store the data in memory, update the next memory location and then return to wait for the next piece of data. There is no freely available microprocessor with an instruction cycle fast enough to execute these instructions in 50 ns.

It is evident from the above firstly that commercially available systems do not fulfil the requirement of the partial discharge detection system, and that hence a system which will optimise data aquisition time and storage space used must be built. Secondly, the speed of waveform aquisition determines the rate at which data

can be transferred to a long term storage medium. If polarity, peak signal value and time of occurrence information are stored, only 6 bytes of data need to be used, and there is 20 micro seconds available to store it. If a fast microprocessor such as the Motorola MC 68000 is used it is possible to write code which will carry out these operations within 20 to 25 micro seconds.

6 Input filter

The instrument described in this paper has been designed to measure partial discharges of the order of 1mV up to 10V, and this must be resolved on mains signals up to 100KV. The standard RLC detector unit used has a fundamental frequency in the region of 80KHz and the power signal has a frequency of 50Hz. The minimum partial discharge to be detected is of the order 1mV, and the power frequency should be filtered to at least 3 orders of magnitude less.

The input filter must therefore filter a 100KV power frequency signal to 1 micro Volt, while not attenuating the 80KHz component of the partial discharge. The input filter must also not resonate at any frequency above or below the cut off point as this will either swamp the partial discharge signal or be superimposed

upon it.

The filter must have an attenuation of 220dB in a frequency span of just over three decades, or approximately 70dB/decade. If a cut off frequency of 50KHz were chosen a fourth order filter would remove the input waveform, but when such a filter was constructed it was found that it distorted the signal from the resonant circuit. A number of filters using lower cut off frequencies were designed and built, and the most workable compromise was found to be five cascaded RC filters with individual cut off frequencies of 10K; 5k; 2.5K; 1.25k and 625Hz.

7 Discharge detector unit (RLC Circuit)

The discharge detector unit is the input detector number two from the ERA discharge detector system. It was found that this filter/stretcher unit performed better than any unit which could be developed locally. The unit consists of a RLC input circuit with the inductor being the primary coil of a step-down transformer. The units which were locally manufactured suffered from severe self resonance of the inductor coils. It appears that very special care has been taken in earthing as well as in the design and construction of the transformer in the ERA unit as it does not suffer from this problem. The transformer is resonance free from DC

to over 1MHz which means that it produces a very clean pulse.

In this system the signal is taken from the RLC circuit on the input side of the transformer with the output of the step-down transformer short-circuited. This configuration gives the fastest decay time for the impulse. The detector unit yields an impulse, which decays to 0 volts in approximately 20 micro seconds consisting of the peak value followed by two overshoots. The value of the resistance is 3.3K, and the capacitance is 10pF, while the inductance is 400mH.

7.1 Characteristics of the signal produced by the discharge detector unit (See Figure 7.1)

The following points are important to note about the signal produced by the discharge detector unit:

a. Partial discharges to be detected lie in the range 1pC to 10000pC's. Because the output of the detector is directly proportional to the charge contained in the discharge, the output voltage from the detector is also in a four decade range.

b. Even though the signal is slowed considerably by the resonant circuit, the peak still takes only

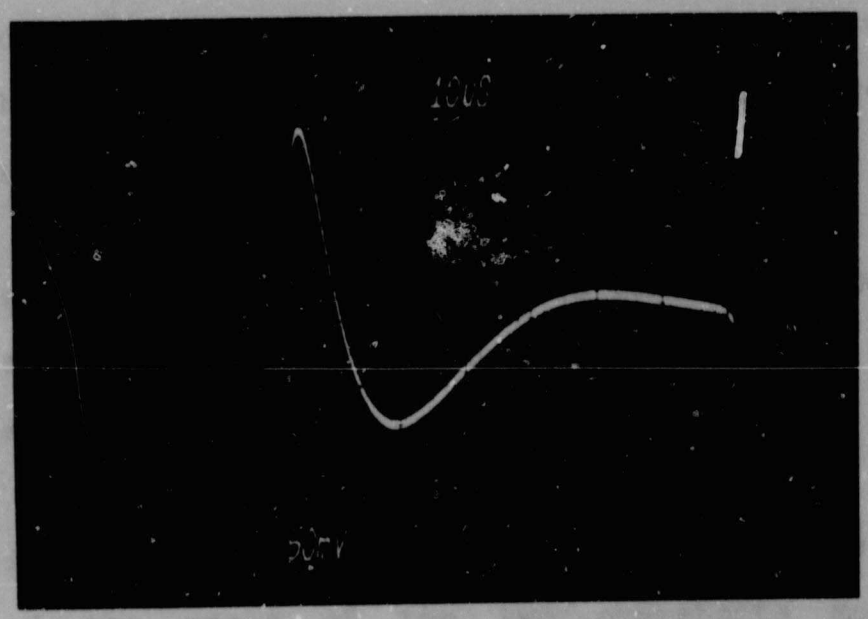


Figure 7.1 Waveform produced by discharge detection unit

2 micro seconds to decay to zero.

c. The rise time of the signal is of the order of tens of nanoseconds and this will cause slew rate limitation with even the fastest operational amplifiers.

d. The output pulse is referenced to ground and hence the peak value must also be referenced to ground.

e. The initial peak decay is very rapid, but the following two overshoots both rise and decay slowly.

f. Only the peak value is important and the value of the peaks of the two overshoots must be discarded.

8 Basic Operation of the circuit:

The basic block diagram of the system is shown in Figure 8.1.

The circuit operates as follows:

a. A partial discharge is produced by the

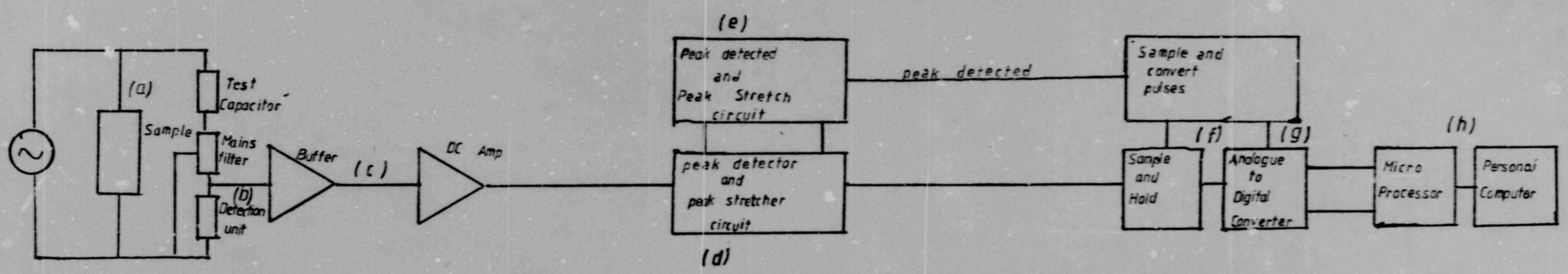


FIGURE 8.1 BASIC BLOCK DIAGRAM OF THE SYSTEM

sample.

b. The power frequency part of the signal is filtered leaving only the partial discharge.

c. The partial discharge is amplified.

d. The initial peak of the partial discharge is localised and the peak is held for a short period of time.

e. A pulse is generated as soon as the peak is detected.

f. This pulse is used as a sample signal to the sample-and-hold, which, in turn, is used to hold the signal peak for a period of time long enough to allow analogue-to-digital conversion to take plac

g. The trailing edge of the sample signal is used to start the conversion cycle of the analogue-to-digital converter.

h. A microprocessor is used both to log the data, and to carry out manipulations on it.

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g. The trailing edge of the sample signal is used to start the conversion cycle of the analogue-to-digital converter.

h. A microprocessor is used both to log the data, and to carry out manipulations on it.

The basic system described above has to be extended in

order that the peak value of the partial discharges, its polarity and time of occurrence (in the range 1pC to 10000pC), may be stored in memory.

The following problems become evident:

a. If an 8-bit analogue-to-digital converter is used (and for economy this is important) the basic resolution of a +/-10V signal is 80mV. But it has already been stated that signals as small as 1mV need to be detected, thus some form of scaling is required.

b. The accuracy of the peak detector and sample-and-hold deteriorates below 1V because of the 0.6V required to bias the diodes used in the storage circuits.

One possible solution to this is to use a 12-bit analogue-to-digital converter which will give a resolution of 0.15mV, but this is an expensive solution which does not alleviate the problem of low resolution levels in the peak detector and sample-and-hold.

An alternative solution to the resolution problem is to use a logarithmic amplifier, but these suffer from the problem that they have a severely limited band width and they give a bipolar output for a unipolar input.

A more complex solution would be to use a combination of both linear and logarithmic amplifiers. Four separate amplification channels are used: One for each of the ranges; 1-to-10mV, 10-to-100mV, 100mV-to-1V and 1V-to -10V.

The 1-to-10mV signal is multiplied by 1000, the 10-to-100mV signal by 100, the 100mV-to-1V signal by 10, and the 1-to-10V signal by 1. This means that each of the four decades has its own separate amplifier and that the peak detectors and sample-and-hold has to only handle signals in the range 1-to-10V.

The extended block diagram which carries out the multiplications described above is shown in Figure 8.2, contains a switching network which is used to select between the different channels. Only one peak detector output lies in the range 1V to 10V at any one time, and this is the value which must be passed to the sample-and-hold. This switch uses four level sensing circuits which selects the correct channel via the use of a control circuit.

The enlarged block diagram is shown in Figure 8.3 from which can be seen that there is a control circuit for the sample-and-hold and analogue-to-digital

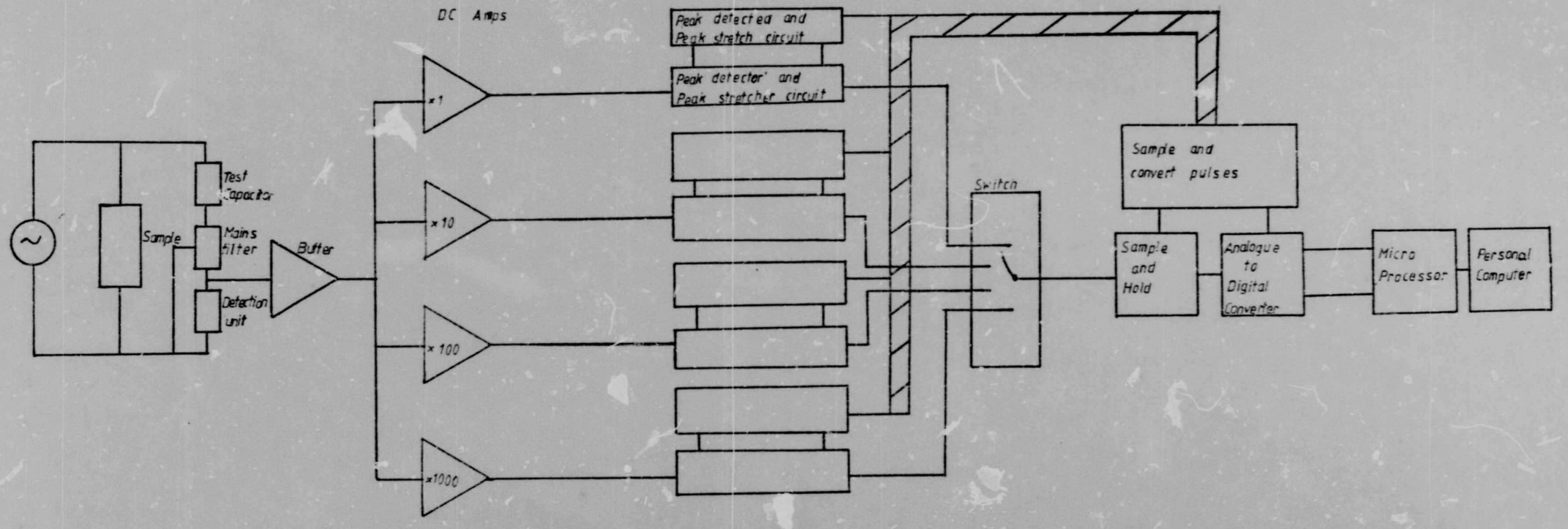


FIGURE 8.2 SYSTEM EXPANDED TO FOUR AMPLIFICATION CHANNELS

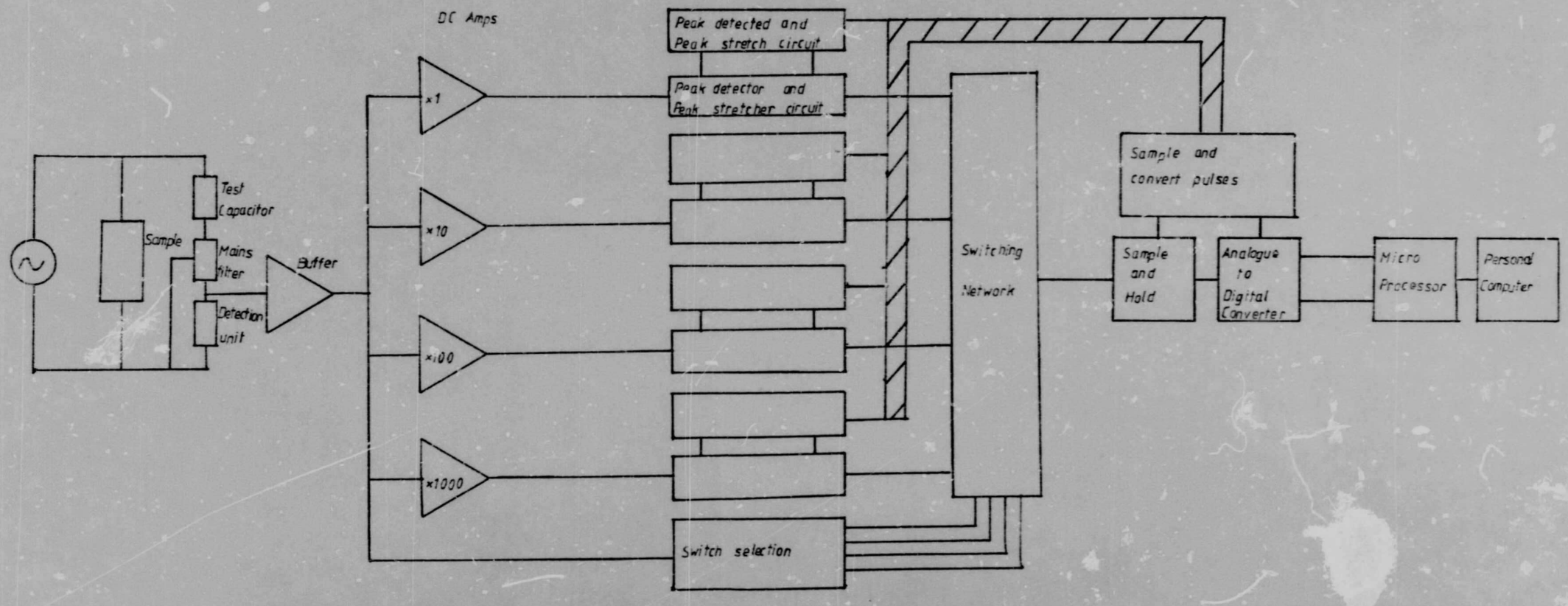


FIGURE 8,3 SYSTEM WITH SWITCHING NETWORK

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