

https://dspace.org/

The design and implementation of multi-node converters

Walters, David John

2010-07-21T13:20:57Z
http://hdl.handle.net/10539/8297

Downloaded from a DSpace repository. https://dspace.org/



THE DESIGN AND IMPLEMENTATION OF MULTI-NODE CONVERTERS

David John Walters

A dissertation submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, in fulfilment of the requirements for the degree of Master of Science in Engineering.

Johannesburg, 2009

DECLARATION

I declare that this dissertation is my own unaided work. It is being submitted for the Degree of Master of Science to the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination to any other University.

.....
(Signature of Candidate)

..... day of ..... year .....
day *month* *year*

ABSTRACT

A switched mode power converter with an extremely wide output range could take the place of numerous other, less flexible, power converters that are only capable of operating at or near to a single output. However, when developing converters with wide output ranges there is a compromise between how effectively the converter's components can be utilised and the output range. This leads to converters with wide output ranges suffering from weight, cost and size penalties.

This dissertation suggests a new converter architecture as a solution to this problem, where composite converters are implemented using multiple smaller converters (or nodes). The nodes can be connected in different series, parallel or series/parallel combinations, which allows the converter's components, and specifically its passive components, to be better utilised. This dissertation optimises the multi-node architecture using logical arguments and simulations coupled with a Genetic Algorithm. A prototype converter is then designed, analysed and built so that theoretical converter models can be experimentally verified.

ACKNOWLEDGEMENTS

I would like to thank my principal supervisor, Prof. Ivan Hofsajer for his guidance and support throughout my work. He has always made himself available when I've needed to consult and I have always felt like his door was open and he was there to talk to. I have really appreciated this.

The Machines Research Group and the School of Electrical and Information Engineering at the University of the Witwatersrand have helped me, not only with my work, but also with funding during my research. This is appreciated

The Paris Île-de-France region in France also deserves my thanks. Through their "Bourse Master Île-de-France" program I spent ten months living, working and experiencing the lifestyle in Paris. This has undoubtedly expanded my horizons and allowed me to see, do and experience so many things. It would never have been possible without their generosity.

I also owe a debt of gratitude to the staff and administration at ESIEE (*École Supérieure d'Ingénieurs en Électronique et Électrotechnique*) in Paris. My supervisor at ESIEE, Prof. Abdellatif REAMA, provided a great working environment and ensured that nothing prevented or impeded me in my work. However, he also allowed me the space and time I needed to travel and explore. My thanks also go to Prof. Arben CELA, Dominique TENTI, Mickael BELREPAYRE and the rest of the Department of Embedded Systems at ESIEE Paris for their help, guidance and generosity in sponsoring a large part of a conference trip to Nürnberg in Germany.

My friends and fellow postgraduates in South Africa and France were a great help with my research and also in brightening and making my days fun and a pleasure. Special thanks go out to Sarah, who also accompanied me on my French trip, and to Riccardo and Rory who keep me sane!

Throughout my academic career, my mother and father have also been extremely supportive. They have encouraged and enabled me throughout and for this, I will always be grateful for the opportunities that they have given me.

And finally, I would like to thank my fiancée Sheryl for being understanding when I needed to work, when I couldn't be with you or couldn't even be in the same country. I am really looking forward to being there all the time, with you, in the future!

SUMMARY

A switched mode power converter capable of outputting constant power over a wide output range would be useful since it could take the place of many, less flexible, power converters that can only operate at or close to a single operating point. However a paradox does exist between the flexibility of the converter's output and how effectively its component parts can be utilised. When the converter's output changes the current, voltage and thermal stresses that the converter's components are exposed to also vary. This means that to prevent component failure they must all be specified for their most stressful operating points over the output range. This results in the converter's components being over-specified at all other operating points. Due to this, the final converter is likely to be larger, heavier and more costly than a less flexible converter where the components can be better utilised.

In order to avoid this, the stresses the converter's components are exposed to need to be decoupled in some way from the converter's output. This dissertation presents the multi-node converter architecture as a solution to this problem. Multi-node converters consist of multiple smaller converters (henceforth known as nodes) that are placed within a mesh of switches that allow the interconnections between nodes to be changed. The nodes can be connected in series, in parallel or in a series/parallel configuration and this allows the voltage and current capabilities of the composite converter to be modified over a wide range while keeping the actual node outputs relatively constant. This allows the stresses experienced by the components within each node to be kept relatively constant, despite the composite converter's wide output range. Through this, it is hoped that the converter's component requirements can be reduced through an improvement in their utilisation.

Multi-node converters are first analysed and optimised from an architectural level. This involves determining how to choose the optimal number of nodes and also their relative sizes. It was found through logical arguments and theoretical simulations that identical nodes result in the converter's capacity being better utilised. The number of nodes should also be chosen to be equal to a number with many factors.

Once the architecture had been optimised, it was possible to develop and analyse a circuit implementation. The circuit implementation was based on the two-switch forward converter with multiple identical secondaries. The suggested converter implementation was analysed and theoretical models capable of predicting the converter's output and efficiency were developed. These could then be used to theoretically compare a traditional converter design with a multi-node converter. It was found that the multi-node converter design had generally lower component requirements and was able to show higher efficiency than the traditional converter.

The final section of the research attempts to experimentally verify the theoretical models that were developed for predicting a multi-node converter's output and efficiency. For this reason a multi-node

converter prototype is developed and its implementation is discussed. How its components were chosen and how the prototype was tested is shown.

Once the prototype converter had been developed, its output and efficiency was experimentally measured. The theoretical model was then calibrated such that it was able to simultaneously predict the experimentally measured output and efficiency. The circuit parameters, or coefficients, that were required to calibrate the model were then compared with their expected values and some mismatches were seen. The calibrated inductor resistance in particular was much higher than expected, however reasons for this and any other mismatches were found and were given.

It is suggested that future work should include a more rigorous and realistic estimation of the circuit parameters. This would allow the model's validity to be shown with certainty. However, at this stage it is noted that the discrepancies between the calibrated and expected circuit parameters were explained and that it does appear that the circuit model is valid. It is a valuable and useful tool for developing and optimising multi-node converters based on the suggested architecture.

Future work is suggested, including work on the design and implementation of a suitable control system for the converter and also an investigation into the optimal circuit topology for implementing multi-node converters.

RÉSUMÉ

Ce projet consiste à mettre en œuvre un convertisseur statique de puissance capable d'assurer un fonctionnement à puissance constante sur une grande plage de rendement. Il s'agissait de mettre au point un convertisseur statique reconfigurable selon les niveaux de tension et du courant exigés par la charge. Un tel convertisseur permet de remplacer avantageusement de nombreux convertisseurs de puissance moins flexibles à cause de la limitation de leur plage de fonctionnement.

Un paradoxe existe cependant entre l'efficacité d'utilisation des composants de puissance et la flexibilité du convertisseur vis-à-vis des exigences de la charge. Une variation du courant de sortie entraine également une variation de la tension de sortie ainsi qu'une variation des contraintes thermiques subies par les composants. Dans ces conditions, la protection des composants contre la destruction conduit forcément à leur surdimensionnement, ce qui entraine des convertisseurs plus volumineux, plus lourds et plus couteux qu'un convertisseur moins flexible dans lequel les composants sont dimensionnés de façon plus précise.

Afin d'éviter le problème mentionné ci-dessus, les efforts auxquels les composants du convertisseur sont exposés ont besoin d'être découplés du rendement du convertisseur. Ce mémoire présente l'architecture du convertisseur multi-nœuds comme une solution à ce problème. Les convertisseurs multi-nœuds se composent de plusieurs convertisseurs plus petits (dorénavant nommés 'nœuds') qui sont placés dans un grillage d'interrupteurs qui permettent aux maillages entre des nœuds destinés à être changés. Les nœuds peuvent être connectés en configuration série, en parallèle, ou en série/parallèle, ce qui permet aux caractéristiques de sortie (tension et courant) du convertisseur d'être modifiées dans une grande gamme tout en gardant les rendements des nœuds relativement constants. Ceci permet de maintenir relativement constants les efforts subis par les composants dans chaque nœud, malgré la grande gamme de rendement du convertisseur. Ainsi, on espère que les contraintes sur les composants du convertisseur pourront être réduites par une amélioration de leur utilisation.

Les convertisseurs sont d'abord analysés et optimisés du point de vue structure. Cela nécessite, au préalable, de déterminer le nombre de nœuds optimal ainsi que leurs tailles respectives. En utilisant des arguments logiques et des simulations théoriques, j'ai trouvé que des nœuds identiques avaient pour résultat une meilleure utilisation de la capacité du convertisseur.

Une fois l'architecture optimisée, il était possible de développer et analyser une implémentation du circuit correspondant. L'implémentation de circuit a été basée sur une structure : « Convertisseurs Forward à deux interrupteurs et plusieurs secondaires identiques. L'implémentation du circuit proposée a été analysée et des modèles théoriques capables de prédire les caractéristiques de sortie du convertisseur et son rendement ont été développés. Une comparaison théorique a été menée entre une

conception d'un convertisseur traditionnelle et celle d'un convertisseur multi-nœud. J'ai trouvé que la conception du convertisseur multi-nœud nécessitait en général moins de composants et qu'elle permettait d'obtenir de meilleurs rendements.

La dernière section de cette recherche tente de vérifier expérimentalement les modèles théoriques qui ont été développés pour la prédiction du rendement et des caractéristiques de sortie du convertisseur multi-nœud. Pour cela, un prototype de convertisseur multi-nœud a été développé et analysé du point de vue implémentation. Le choix des composants ainsi que leurs tests ont été présentés également.

Après le développement du convertisseur prototype, des mesures expérimentales ont été effectuées sur ses caractéristiques de sortie et son rendement. Ensuite, le modèle théorique a été calibré de façon à permettre une prédiction expérimentale de la mesure simultanée du rendement et caractéristiques de sortie.

La comparaison des paramètres du circuit (ou les coefficients qui étaient nécessaires à la calibration) aux valeurs attendues a indiqué la présence de quelques écarts. La résistance de la bobine calibrée était particulièrement beaucoup plus élevée que celle qui était prévue. Cependant, les raisons de ces disparités ont été trouvées et développées.

La suggestion des travaux futurs consiste concevoir une estimation réaliste et plus rigoureuse des paramètres du circuit. Cela permettrait de montrer la validité du modèle avec certitude. Cependant, malgré les disparités observées, il apparaît que le modèle du circuit est bien validé. Il constitue un outil précieux et utile pour le développement et l'optimisation des convertisseurs multi-nœuds basés sur l'architecture proposée.

Le travail futur consiste à étudier la conception et l'implémentation d'un système de contrôle bien adapté au convertisseur d'une part et faire un travail de prospective au niveau de l'optimisation de la topologie du circuit en vue de d'une implémentation des convertisseurs multi-nœuds d'autre part.

TABLE OF CONTENTS

Chapter 1 - Introduction 1

1.1 Introduction 1

1.1 Problem Statement 2

1.2 Constant Maximum Output Power over a Wide Range 2

1.3 Analysing a Traditional Converter with a Constant Output Power 5

1.3.1 The Buck Converter and its Component Stresses 5

1.3.2 Model Assumptions and Specifications 6

1.3.3 Component Stresses versus Output 6

1.3.3.1 Capacitor Stresses 6

1.3.3.2 Inductor Stresses 6

1.3.3.3 Thermal Stresses in the Components 7

1.3.4 Component Utilisation in the Buck Converter 8

1.3.5 Analysis 9

1.4 Organisation of the Dissertation 10

1.5 Published Works 10

1.6 Conclusion 10

Chapter 2 – Multi-Node Converters 12

2.1 Introduction 12

2.2 Multi-Node Converters 12

2.2.1 Introduction 12

2.2.2 A Multi-Node Converter’s V-I Curve 13

2.2.3 Individual Node Requirements 14

2.2.4 Multi-node Converter Switch Implementation and its Implications 15

2.2.4.1 Implementation with Semiconductor Switches 15

2.2.4.2 Implementation with Relays or Mechanical Switches 16

2.2.4.3 Implementation with Hard-Wired Connections 16

2.2.5 Analysis 16

2.2.6 Future Analysis 17

2.2.7 Conclusion 17
2.3 Multi-Node Converter Optimisation 17
2.3.1 Metrics for Analysing Multi-Node Converters 18
2.3.2 Choosing the Relative Node Sizes 19
2.3.3 How Many Nodes are Optimal? 21
2.3.3.1 The Number of Nodes and Utilisation 21
2.3.3.2 The Output Range 23
2.3.3.3 Complexity versus the Number of nodes 23
2.3.4 The Multi-Node Converter Simulator 24
2.3.4.1 Choosing the Software Platform 24
2.3.4.2 Assumptions 24
2.3.4.3 Algorithm Description 25
2.3.4.4 Multi-Node Converter Simulator Limitations 26
2.3.4.5 The Genetic Algorithm 27
2.3.4.6 The Genetic Algorithm's Results and Output 29
2.3.5 Conclusion 32
2.4 Conclusion 32
Chapter 3 – Theoretical Analysis of a Proposed Multi-Node Converter Implementation 34
3.1 Introduction 34
3.2 The Proposed Implementation 34
3.2.1 The Two-Switch Forward Converter 34
3.2.2 Ideal Steady State Voltage and Current Waveforms 35
3.2.3 Advantages and Disadvantages of the Two-Switch Forward Converter Topology 37
3.2.4 Current Sharing between Phases 37
3.2.4.1 Leakage Inductance Effects on Output Voltage 37
3.2.4.2 Leakage Inductance Effects on Current Sharing with Multiple Secondaries 39
3.2.4.3 Unequal Current Sharing Due to Component Tolerances 40
3.2.5 Filter Requirements versus Number of Nodes 40
3.2.5.1 Model Description 40

3.2.5.2 Determination of the Required Filter Inductance 42
3.2.5.3 Filter Inductance Requirements versus the Number of Nodes 43
3.2.5.4 Inductor Size, Weight and Cost versus the Number of Nodes 45
3.2.5.5 Filter Capacitor Requirements 48
3.2.5.6 Changes of Filter Technology Possible due to the Multi-Node Converter Architecture 49
3.2.6 Conclusion 49
3.3 Converter Modelling 50
3.3.1 Component Models, Assumptions and Losses 51
3.3.1.1 MOSFET Model 51
3.3.1.2 Diode Model 52
3.3.1.3 Inductor Model 52
3.3.1.4 Transformer Model 53
3.3.1.5 Capacitor Model 54
3.3.1.6 Modelling the Effect of Stray and other Resistances in the Converter 54
3.3.2 Parameter Definitions 54
3.3.3 Model One: Any Number of Identical Nodes 55
3.3.3.1 Assumptions 55
3.3.3.2 Derivation of the Model and the Output Voltage Expression 55
3.3.4 Model Two: Four Non-Identical Nodes 57
3.3.4.1 Assumptions 57
3.3.4.2 Derivation of the Model 57
3.3.4.3 Output Expression for Constant Output Power 59
3.3.5 Model Comparison 60
3.3.6 Conclusion 60
3.4 Comparative Design Example 61
3.4.1 Magnetics Design Procedures 62
3.4.1.1 Transformer Design Procedure 62
3.4.1.2 Inductor Design Procedure 63

3.4.2 Component Selection and Specification 63
3.4.2.1 Primary Side Power Switch Selection 63
3.4.2.2 Transformer Specification 64
3.4.2.3 Filter Inductor Specification 64
3.4.2.4 Filter Capacitor Selection 66
3.4.2.5 Rectifying Diode Selection 67
3.4.2.6 Control System Specifications 67
3.4.3 Theoretical Performance Analysis 68
3.4.3.1 Output Voltage versus Duty Cycle 68
3.4.3.2 Individual Component Losses 69
3.4.3.3 MOSFET Losses 69
3.4.3.4 Rectifier Losses 70
3.4.3.5 Inductor Losses 70
3.4.3.6 Transformer Losses 71
3.4.3.7 Power Train Losses 72
3.4.3.8 Topology Losses 72
3.4.4 The Theoretical Efficiency for both Converters 72
3.4.5 Analysis 73
3.4.6 Conclusion 74
3.5 Conclusion 74
Chapter 4 – Prototype Implementation and Testing 76
4.1 The Two-Switch Forward Converter Test Platform 76
4.1.1 Circuit Description 76
4.1.1.1 Control System 77
4.1.1.2 MOSFET Drivers 77
4.1.1.3 Power Stage 77
4.1.2 High-Side Driver Implementation Issues 78
4.1.2.1 Standard Implementation 78
4.1.2.2 Driver IC Usage in Two-Switch Forward Converters 80

4.1.3 Practical Implementation 81
4.1.3.1 Component Selection 81
4.1.3.2 Printed Circuit Board Design, Layout and Implementation 82
4.1.4 Testing with a Resistive Load 85
4.1.5 Testing with a Transformer Load 86
4.1.5.1 Transformer Load Specifications 86
4.1.5.2 Output Voltage Analysis 86
4.1.5.3 Transformer Primary Current 89
4.1.6 Suitability for Use 91
4.2 The Multi-Node Secondary 91
4.2.1 Current Sharing 92
4.2.1.1 Transformer Leakage Inductance Effects 92
4.2.1.2 Output Resistors 92
4.2.2 Practical Implementation of the Multi-Node Secondary 93
4.2.2.1 Secondary Specification 93
4.2.2.2 Transformer Design 94
4.2.2.3 Output Capacitor Selection 94
4.2.2.4 Inductor Design 95
4.2.2.5 Selection of other Components 95
4.2.2.6 PCB design and Implementation 96
4.2.3 Testing 97
4.2.4 Suitability for Use 100
4.3 Distribution Board 100
4.3.1 Circuit Description 101
4.3.2 Practical Implementation 101
4.3.3 Testing 102
4.3.4 Suitability for Use 102
4.4 Conclusion 102
Chapter 5 – Experimental Testing of the Multi-Node Converter Prototype 104

5.1 Introduction 104
5.2 Experimental Setup and Theoretical Validation 104
5.2.1 Experimental Setup 104
5.2.2 Theoretical Validation 106
5.2.3 Conclusion 107
5.3 Experimental Results 107
5.3.1 The Output Range 107
5.3.2 Current Sharing 109
5.3.3 Converter Efficiency 110
5.3.4 Conclusion 111
5.4 Model Calibration 112
5.4.1 Calibration Procedure 112
5.4.2 Inaccuracies in the Calibration Procedure 113
5.4.3 Modelling the Current Sharing Mismatch 114
5.4.4 Efficiency Prediction Mismatches 115
5.4.5 Conclusion 117
5.5 Circuit Parameter Comparison 118
5.5.1 Comparison between the Expected and Calibrated Circuit Parameters 118
5.5.2 Analysis of the Circuit Parameter Mismatches 119
5.5.2.1 The Inductor Resistance Mismatch 119
5.5.2.2 The Transformer Resistance Mismatch 120
5.5.2.3 Other Mismatches 120
5.5.3 Analysis 120
5.5.4 Conclusion 121
5.6 Conclusion 121
Chapter 6 – Conclusions and Future Work 123
References 127
Appendix A – Supplemental Prototype Analysis and Testing A-1
Appendix B – Circuit Diagrams, Parts Lists and PCB Layouts for the Multi-Node Converter Prototype B-1

Appendix C – Matlab Code, C++ Code and Other Ancilliary Information C-1

CHAPTER 1

INTRODUCTION

1.1 Introduction

In engineering and design there is a constant battle between how well a design can be optimised and how flexible the final product is. In other words, it is often difficult to optimise a product's design, or the design of its component parts, if the requirements for that product or part are allowed change. This often results in a design where significant compromises have to be made.

A good example for this is seen in the design of optical lenses which will be used as an analogy. A zoom lens that is able to vary its focal length is significantly more flexible than a single focal length prime lens. However, a single prime lens in the same focal length range is likely to be smaller, lighter, have a larger maximum aperture while suffering from fewer optical aberrations and being sharper. This occurs since lens designers are able to optimise the design of a prime lens far more than a zoom lens that must operate over a range of focal lengths.

An analogy can be drawn between this problem in lens design and the optimal design of power electronics. If a power converter is designed so that it operates at a specific operating point (i.e. at a constant output current and voltage) then the converter's designer can optimise each and every component within that converter. Any components that carry current can be specified such that they are capable of carrying only the required current. The voltage rating of any components that must withstand a voltage can also be chosen to withstand only that voltage and the capacity of any hardware required to cool the converter can, likewise, be fully utilised at all times since the losses experienced in the converter's components will be constant. This allows the full capacity of each and every component within the converter to be fully utilised at all times and means that the converter can be very well optimised.

This is then contrasted with a converter with the same power rating that is instead able to operate over a wide range of operating points with constant output power. When the converter's output voltage or current is changed, the stresses (current, voltage and thermal) that the converter's components are exposed to also change. This makes it difficult to optimally select the components within the converter since their requirements are always changing. The result of this is that the converter is likely to be heavier, larger and more costly than the converter that only operates at a single operating point.

If we return to the lens design analogy, lens designers seeking to better optimise a zoom lens resort to using advanced techniques and exotic materials. These techniques and materials have allowed modern

zoom lenses with manageable size, cost and weight penalties to approach levels of performance formerly seen only in prime lenses.

But what techniques are available to the modern power electronics designer for solving an analogous problem? In other words, what methods or materials allow the size, weight and cost penalties suffered by a converter that operates over a wide range to be minimised?

This is the focus of the research and multi-node converters, which are later presented and discussed, are suggested as a possible method whereby this can be achieved. The remainder of this dissertation describes the problem further and then presents the multi-node converter architecture. Since the architecture is new, it is then analysed and optimised from an architectural level before a proposed circuit implementation is given. This circuit implementation allows a prototype converter to be developed and means that theoretical work performed on the proposed implementation can be experimentally verified in the laboratory.

The problem will now be discussed in more detail before the layout and breakdown of this document is presented. The details of any work published during the research will then be given.

1.1 Problem Statement

The introduction discussed the problem that is being addressed in general terms. This section formalises the research that is underway and analyses a research statement. The research statement is given as:

*"We would like to develop a **DC/DC converter** that is capable of delivering **constant maximum output power** to a load over a **wide output range.** The converter should also **utilise its capacity effectively at all operating points**. High efficiency over the entire output range and minimum size, weight and cost are also a concern"*

This statement is broken down and discussed in the next section. Once it has been clarified, a traditional converter topology is analysed where the reasons why traditional converter topologies are not capable of meeting the research statement's criteria will be apparent.

1.2 Constant Maximum Output Power over a Wide Range

The research statement states that we would like to develop a converter that is capable of outputting the same maximum output power over a wide output range. This is contrasted to how converters are normally developed and specified. It is not unusual to encounter a converter with only a given maximum output voltage and current. These ratings are unrelated to one another and the converter is capable of outputting maximum output voltage and current simultaneously. Figure 1.1 shows the possible region of operation for such a generic converter as a V-I curve.

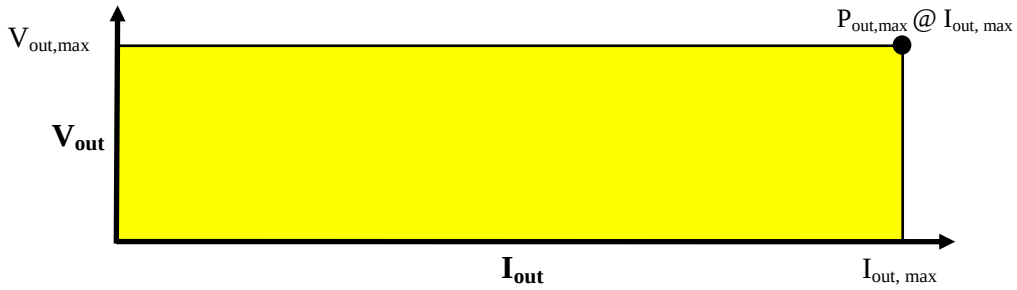


Figure 1.1: The V-I curve for a generic converter.

The generic converter is capable of operating within the shaded region. Operation outside the region exceeds the converter's specifications and may lead to failure. Figure 1.2 shows the maximum output power that the converter can deliver as a function of output current.

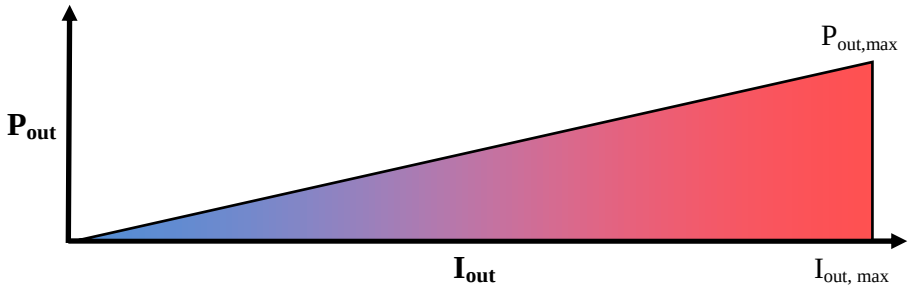


Figure 1.2: Maximum output power versus output current.

The figure shows that the converter's maximum output power increases with increasing current. The converter may then be described as being a "$P_{out, max}$ Watt Converter". This is a little bit misleading as the converter is only capable of generating that maximum output power at a single output current and voltage. It would be preferable if the converter could deliver its maximum output power over a wide range of current outputs. Figure 1.3 shows the required V-I curve for such a converter.

The hyperbolic section in the figure corresponds to operation at constant output power (In other words where $V_o.I_o$ is constant). A converter possessing such an operating region could truly be called a "P_o Watt Converter" as it is capable of producing that output power at any operating point in the output range. One way of visualising the difference between such a converter and a generic converter is to compare their V-I curves. If both converters have the same maximum output power and current or the graphs are normalised to the maximum output power and current then they can be compared directly. The V-I output curve for a generic converter is also shown in Figure 1.3 (as the hatched region).

The figure shows the differences between the two operating regions. The converter capable of constant maximum output power over a wide range is able to increase its output voltage when the output current drops. However, at high currents it is not capable of the same high output voltages. This means that the converter's capacity can be fully utilised at all points. The challenge is developing a converter with an operating region like the shaded region in the figure.

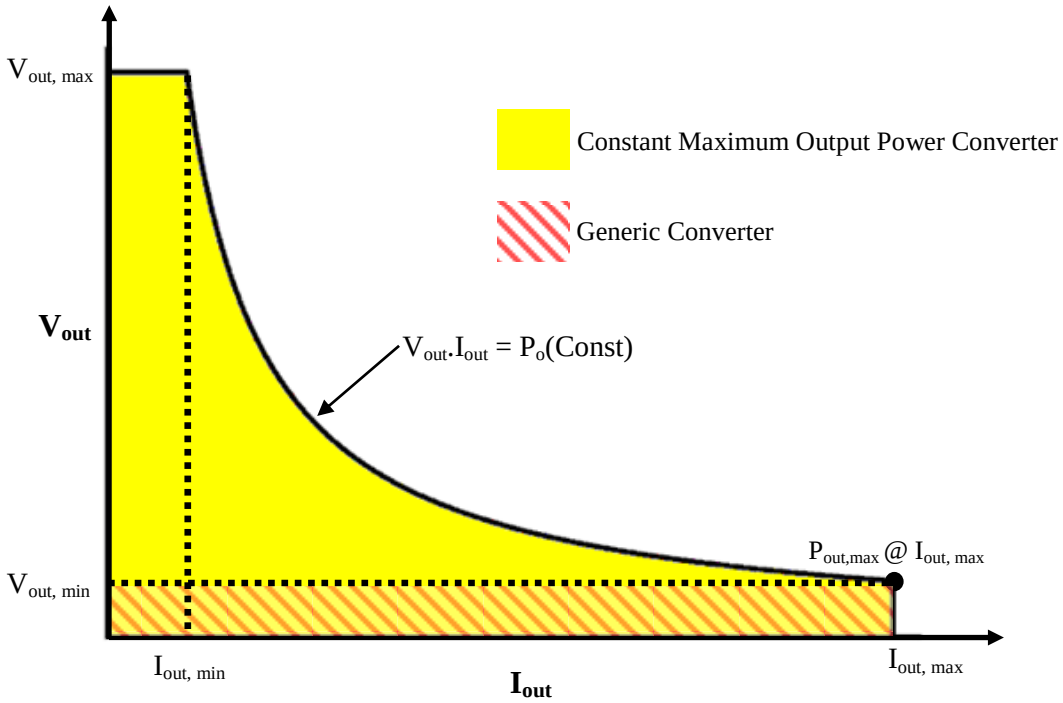


Figure 1.3: A V-I curve for constant maximum output power

The practical limitations to having a constant output power over the entire range also need to be considered. Operation at constant power and zero current or constant power and zero voltage are not practical since they demand infinite output voltage and current respectively. For this reason a minimum output voltage and current for constant power operation must be defined. These are shown as $V_{out,min}$ and $I_{out,min}$ in the figure. Figure 1.4 shows the maximum output power versus output current for a converter with a constant maximum output power.

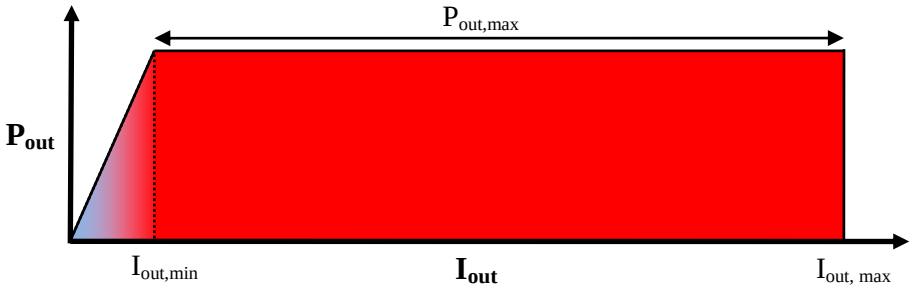


Figure 1.4: Constant maximum output power over a wide range

In the figure, the region where constant output power is possible is clearly visible and the length of this region should be maximised by maximising the ratio of $V_{out,max}$ to $V_{out,min}$ (or the ratio $I_{out,max}$ to $I_{out,min}$ – the ratios are equal for a constant output power). This means that the converter is able to deliver a constant maximum output power over the widest possible region of operation. This is an aim of the research. Specifically, how can the output range over which constant maximum output power

can be delivered to the load be widened? The next section analyses a traditional converter topology so that this problem is better understood.

1.3 Analysing a Traditional Converter with a Constant Output Power

This section analyses a traditional converter (the Buck Converter) when it is operated with a constant power output over a wide range. Why the traditional converter's component requirements change with output is then analysed, which allows a discussion about what new properties a converter capable of constant maximum output power over a wide range should have. In this discussion, particular attention is paid to the passive components in the converter. This is because they are often the heaviest, largest and costliest components in a converter [1] [2]. If we would like to make strides in reducing these three properties of any converter then it makes sense to start here.

1.3.1 The Buck Converter and its Component Stresses

Figure 1.5 shows the circuit diagram for a standard Buck Converter. The Buck converter is one of the simplest and most popular converter topologies and its operation is discussed in numerous texts on power electronics [3] [4]. It is a step down converter with an ideal conversation ratio given by the converter's duty cycle if operated in the Continuous Conduction Mode (CCM).

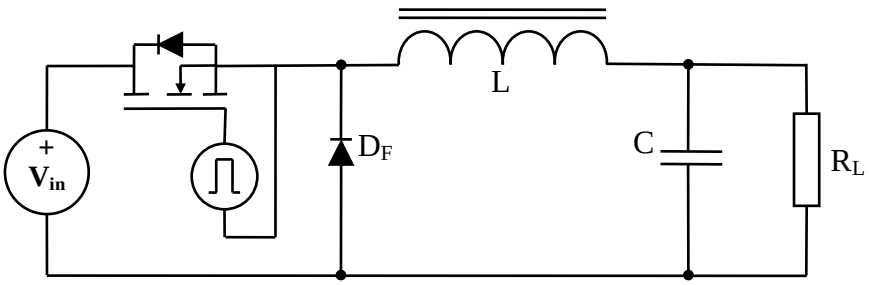


Figure 1.5: A standard Buck Converter

The Buck converter will now be analysed with a focus on how the stresses that the components must withstand vary with output. However the term "component stresses" should first be defined.

By component stresses one or more of the following is meant:

- The current that the component must be able to conduct before failure.
- The voltage the component must be capable of withstanding.
- The heat that the component must be capable of dissipating without suffering thermal failure.

Each component has different stresses depending on the nature of the component. For example, for an inductor current stresses are far more relevant than voltage stresses. However, for a capacitor the voltage stresses are more important and in semiconductor switches both the voltage and current stresses are important.

Thermal stresses are a concern for any component. The higher the thermal stress a component must withstand the more effort required to cool that component. Thermal stresses are addressed in Section 1.3.3.3.

1.3.2 Model Assumptions and Specifications

The Buck Converter circuit has been modelled using the following assumptions and specifications:

- A constant output power of 100 W is maintained by varying the load resistance.
- The circuit is powered by a 100 V DC bus.
- A switching frequency of 50 kHz is used.
- Suitable parameters for each component at the power level have been assumed.
- The converter operates in the Continuous Conduction Mode (CCM) throughout the output range.

A mathematical model was then developed from low level circuit analysis techniques and this model was implemented in Matlab. The Buck converter mathematical model is included in Appendix C.

1.3.3 Component Stresses versus Output

How the stresses in the converter's components vary with output is now discussed.

1.3.3.1 Capacitor Stresses

When specifying the capacitor in the converter we mainly focus on the voltage rating and the capacitance. Other factors, such as a capacitor's ripple current rating and Equivalent Series Resistance (ESR) also matter, but are not discussed here. From Figure 1.5 we can see that the capacitor voltage always equals the output voltage in a Buck Converter. This means that the voltage **stresses imposed on the capacitor vary directly with the output**. To prevent failure, the capacitor must be rated at or above the highest possible output voltage (equal to the input voltage). This means that at lower output voltages, the capacitor's voltage withstand capabilities are not fully utilised.

1.3.3.2 Inductor Stresses

In terms of the inductor's specifications we are mainly focused on the current rating and the inductance. By analysing the Buck converter circuit we see that the average inductor current and the output current must always be equal. For a small ripple current, this means that the inductor's **stresses vary directly with the output current**. The inductor's current rating should be specified at the highest expected output current (and the lowest voltage) to prevent failure. This means that the inductor's current carrying capacity is not well utilised at lower output currents.

1.3.3.3 Thermal Stresses in the Components

The thermal stresses that each component must withstand are determined by calculating the losses that each component experiences during operation of the converter. Different components experience different losses depending on their nature.

The MOSFET in the converter experiences both conduction and switching losses. The conduction losses are given by the product of the on-resistance of the MOSFET and the square of the RMS current that flows through it. The switching losses are dependent on many factors, but the largest contribution to the switching losses generally occurs because the MOSFET is hard switched. The losses due to hard switching the MOSFET are dependent on the peak current and voltage that the MOSFET experiences before and after any switching transition and the time a switching transition takes. These losses occur every switching cycle and so they are linearly dependant on the switching frequency [3].

The diode experiences conduction losses that are given by the product of its forward voltage and the average current that flows through it. There is also a small resistive component in the diode's loss, but this is generally negligible for diodes at lower power ratings. The diode can cause other losses in the circuit due to reverse recovery; however Schottky diodes mitigate this as they do not suffer from reverse recovery effects.

The inductor's losses are due to conduction and core losses. The inductor's winding is slightly resistive and so the conduction losses are given by the product of the inductor's parasitic resistance and the square of the RMS current that flows through it. Core losses are also present and are due to eddy currents in the core and hysteresis effects. For ferrite cores, losses due to eddy currents are generally small while the losses due to hysteresis can be predicted from the manufacturer's datasheet for the core and the expected B-H curve during operation of the converter.

Figure 1.6 now shows the converter's theoretical component losses (switching and conduction losses combined where appropriate) and how they change when the converter's duty cycle is varied over a wide range while the output power is kept constant at 100 W. The trend that the losses follow is more important in this figure than the actual numbers.

It is clear that the component losses are higher at lower duty cycles where the output current increases. This is where the components would face their highest thermal stresses. The amount of heat that the components can dissipate and any cooling hardware must therefore be specified at this operating point. However, since the component losses vary over such a wide output range, the capacity of any cooling hardware cannot be well utilised throughout the output range.

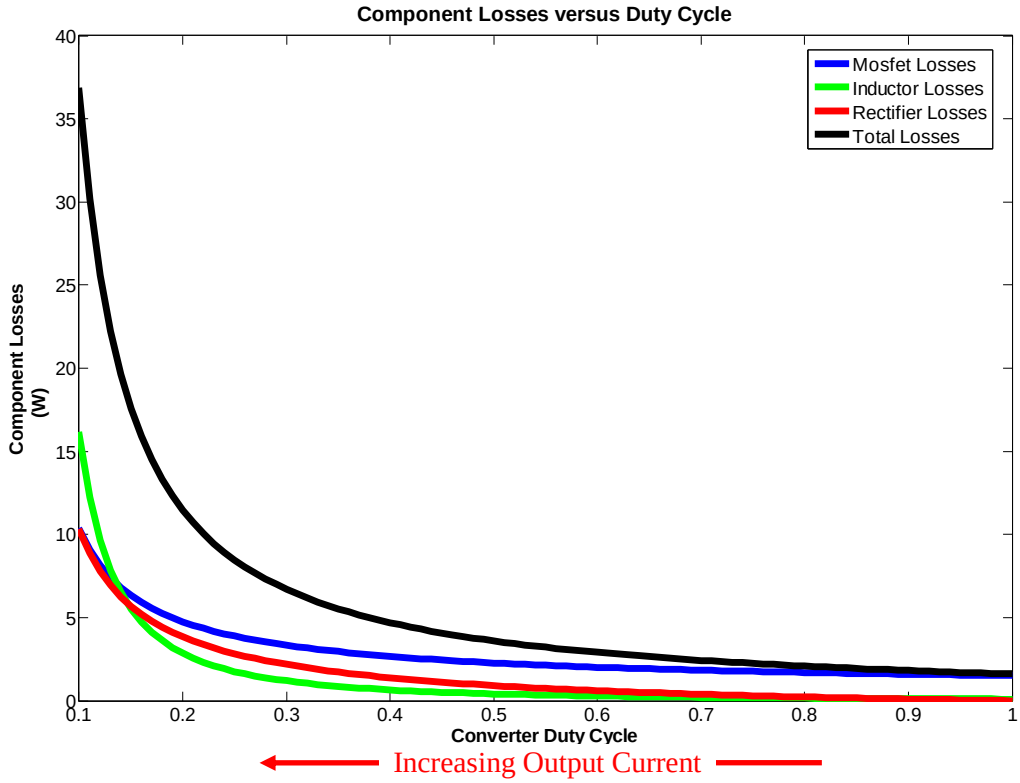


Figure 1.6: Component losses versus duty cycle

1.3.4 Component Utilisation in the Buck Converter

When addressing component utilisation within switched mode converters, many authors only address the utilisation of the controllable semiconductor switches [3] [4]. Erickson justifies this by stating that the largest single cost within a converter is often the cost of the controllable switches. However with recent advances in semiconductor switches this may no longer be true. The controllable switches are also some of the smallest and lightest components within a converter and the actual size and weight of the switches have very little impact on the final size and weight of a converter. Therefore, with the aim of minimising a converter's size, weight and cost it makes sense to also focus on the utilisation of the passive components.

For this reason the stresses in all of the converter's components have been analysed and it was shown that when the converter is operated over a wide range the component stresses also vary over a wide range. For the converter to operate successfully we therefore need to specify each component at its most stressful operating point (in terms of current, voltage and thermal stresses). If this procedure is followed then a converter capable of operating with constant output power over a wide range can be developed. However, consider the points below:

- The capacitor's voltage rating is only fully utilised at the highest output voltage.

- The inductor and semiconductor switches only utilise their current carrying capacity fully at the maximum output current (i.e. at the lowest output voltage).
- The maximum thermal stresses only occur at the maximum output current and so the capacity of any hardware used to cool the components is not well utilised at lower output currents.

This results in the final converter being composed of components that have much higher specifications than required most of the time. Their capacity cannot be fully utilised throughout the converter's output range.

If we compare such a converter to one that is optimised to operate at a single operating point then the wide output range converter will likely be larger, heavier and more expensive. This is because in the converter that operates at only one operating point, the components can be specified so that their capacity is fully utilised. There is no wasted capacity. However, we cannot optimise the specifications of the components in a converter with a wide output range because the required specifications change with the output.

1.3.5 Analysis

The component stresses and how they vary with output was analysed in a conventional Buck converter. It was noticed that the stresses varied significantly as the output changed. This means that in order to allow operation over the entire output range the components must be specified at their most stressful operating points. However, this results in the final converter being composed of components that are much higher rated than required at most operating points. Using over specified components is not desirable since it means that the final converter design is likely to be larger, heavier and more expensive than required. It would be better if we would operate a converter over the wide output range while avoiding this problem. This is what "high utilisation of capacity" in the research statement means. We want to develop a converter that operates at constant power over a wide range while utilising its components effectively throughout that output range.

Unfortunately the other standard topologies (Buck-Boost, Boost etc.) suffer from the same problem as the Buck Converter. Namely their component stresses vary significantly with output. This means that a new topology or method of operation is required so that we can optimise component usage over a wide output range.

The way to optimise the component usage is to try to prevent the stresses (thermal, current and voltage) placed on the converter's components from varying with the output. In other words to partially decouple the component stresses from the output. It is not suggested that they can be completely decoupled as this would mean that the component stresses are completely independent of the output. What is merely suggested is that the range over which the stresses vary could be reduced in some way. If this is feasible then it may be possible to better optimise the choice of components

and ultimately reduce the component requirements. This may lead to size, weight and cost reductions. Multi-node converters may achieve this aim. They are presented in the next chapter.

There is also one glaring omission in the analysis of the Buck converters component requirements. How the required filter capacitance and inductance vary with output was not discussed. This will be discussed in Chapter 3 when the filters required in multi-node converters and how they compare to a traditional converter's filters is analysed. This will allow a comparison that is not possible until the multi-node architecture has been presented.

1.4 Organisation of the Dissertation

This dissertation is divided into six main chapters, followed by references and finally appendices. The first chapter (this one) introduced and described the problem that is being addressed in the research. Multi-node converters are then presented and analysed in Chapter 2. The second chapter also describes how the converter architecture is optimised from an architectural level.

Chapter 3 then uses Chapter 2's results to develop a suggested circuit implementation for multi-node converters. The proposed implementation is then analysed and theoretical models describing the converter's operation are developed. These theoretical models allow a comparative design between a traditional converter and a multi-node converter with the same specifications to be performed. The two designs are compared in terms of their component requirements, output and efficiency.

In order to verify the theoretical models that were developed a prototype multi-node converter has been built. This prototype and its implementation are described in detail in Chapter 4. The prototype was tested and the results of this are discussed in Chapter 5. The experimental results are then used to comment on the validity of the theoretical models developed in Chapter 3.

Chapter 6 summarises the important results from the research and concludes. Future work is then suggested. Appendices follow after Chapter 6.

1.5 Published Works

One paper was published during the course of the research:

> **D.J. Walters**, I.W. Hofsajer, A. Reama, "A Theoretical Analysis of Multi-Node Power Supplies" in proc. PCIM Europe 2009 Conference, May 2009, pp. 552-557

This paper is included in Appendix C.

1.6 Conclusion

This chapter serves as an introduction to the research that has been performed and describes why multi-node converters are being investigated. The topic of research was introduced and it was stated

that a method that allows a converter to utilise its components effectively, even if the converter's output is changed, is being investigated.

This topic was then formalised using a research question or statement. The meaning and implications of the research question were then analysed. What is meant by utilisation of components and by constant output power over a wide range have both been discussed. A Buck converter was then modelled and why it, and other popular topologies, are not capable utilising their components effectively over a wide output range was apparent. This low component utilisation is likely to lead to a final converter design that is heavier, larger and more expensive than if the component parts of the converter were better utilised. Multi-node converters will be presented in the next chapter where the stresses seen by the converter's components can be partially decoupled from the output. This can lead to better utilisation of the converters components. Whether this results in a cost, size or weight savings is addressed in later chapters.

CHAPTER 2

MULTI-NODE CONVERTERS

2.1 Introduction

The first chapter introduced the research topic and discussed why traditional converters are not capable of fulfilling the requirements set out in the research statement. Multi-node converters were then mentioned as a solution that is being researched. This chapter introduces and discusses the multi-node converter concept.

Once a basic introduction to multi-node converters has been given, other more advanced topics regarding the multi-node converter architecture will be discussed. The architecture will be optimised at an architectural level so that later chapters can discuss the design and practical implementation of an actual converter prototype.

2.2 Multi-Node Converters

2.2.1 Introduction

Multi-node converters are being proposed as a method of increasing the output range of a DC/DC converter while still maintaining high utilisation of the components. Figure 2.1 shows a multi-node converter schematic. It consists of multiple smaller converters or nodes embedded within a matrix of switches. The position of these switches determines the interconnection of the nodes. In other words whether the nodes are connected in series, in parallel or in a combination of the two is determined by which switches are conducting.

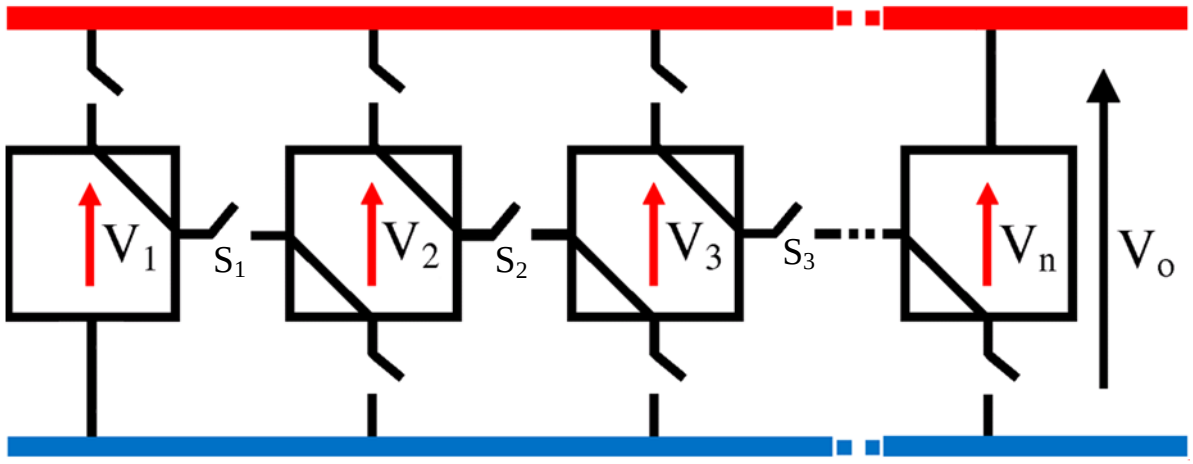


Figure 2.1: The multi-node converter schematic with the switches numbered

In the schematic, if the top and bottom rows of switches are closed then the nodes will all be connected in parallel. This results in a low output voltage with a high output current. Similarly, if the middle row of switches is closed then the nodes are connected in series. This results in a high voltage and low current output. Through this technique a converter that has a changing voltage and current capacity can be produced despite the fact that its components are unchanged. If the switches are controllable in real time then it is possible to develop a flexible converter capable of changing its capacity in real time. This is discussed in the next section when the V-I curves and the output power for a multi-node converter are discussed.

2.2.2 A Multi-Node Converter's V-I Curve

Figure 2.2 shows the theoretical V-I curve for a multi-node converter consisting of 12 identical nodes. How the converter is connected for each output is shown schematically in the figure and a constant power curve is also plotted.

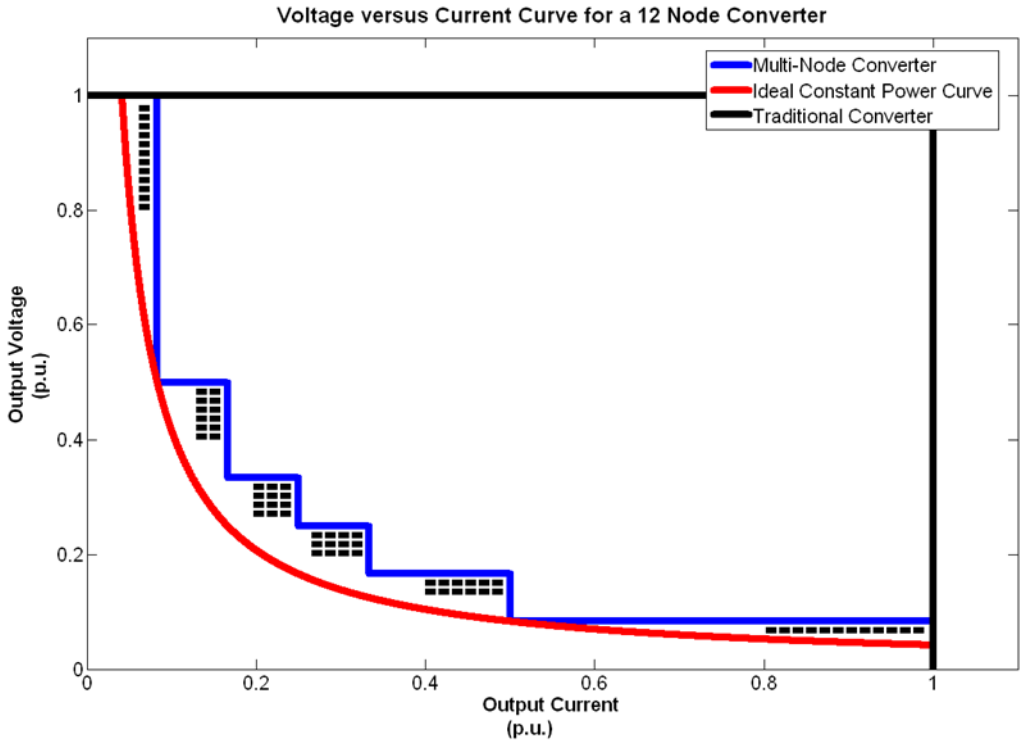


Figure 2.2: The V-I curve for a multi-node converter with 12 identical nodes

An ideal converter would be able to change its installed voltage and current capacity along the ideal hyperbolic curve. This means that an ideal converter never has any excess capacity. If the converter can operate outside the area demarcated by the constant power curve then it is over specified at that point.

The multi-node converter's attainable V-I curve does not exactly follow the ideal constant power curve and instead overlaps at most output currents. This means that the converter has excess capacity

at most operating points. However, it is over specified to a much lower degree than a traditional converter (The V-I curve for a traditional converter is also shown in the figure). Figure 2.3 shows the converter's maximum output power versus output current with one unit equal to the constant output power. The region over which the converter can provide constant output power is shaded. We see that the converter is over specified by as much as two times over the output range. This is not ideal; however its maximum output power is twelve times lower than the maximum output power that a traditional converter would be able to produce (for a converter with 12 identical nodes). In other words, the multi-node converter only requires one twelfth of the installed capacity to produce the same output. This reduced installed capacity requirement can lead to significant reductions in converter cost, size and weight (as long as the hardware required to implement the multi-node architecture does not negate this).

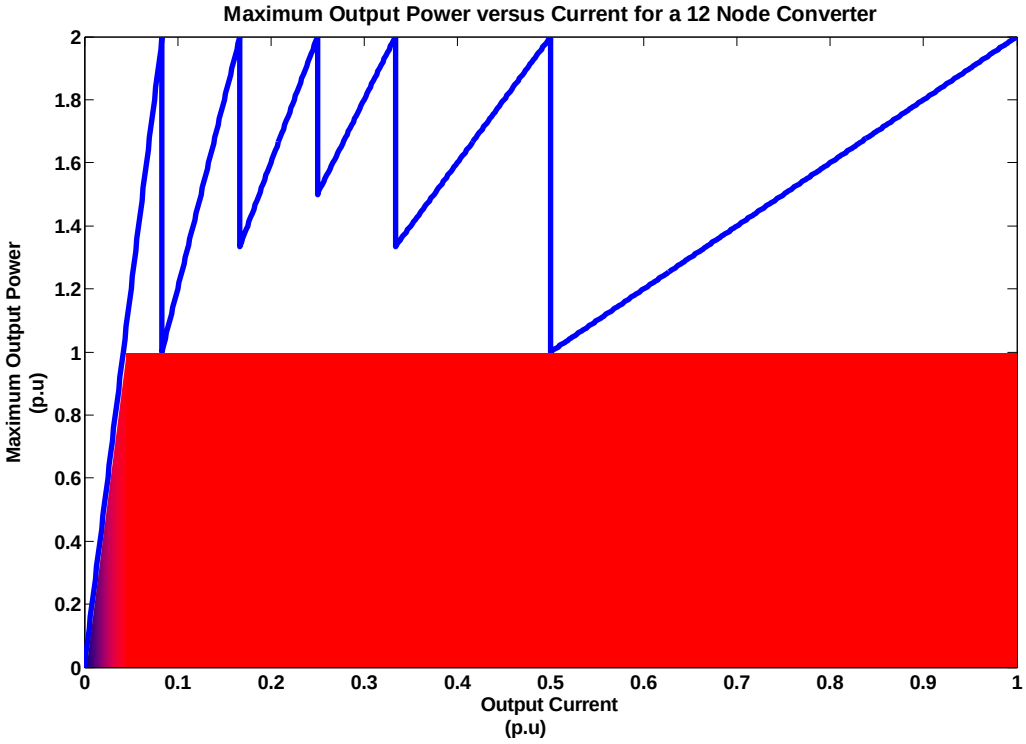


Figure 2.3: Maximum output power versus output current for a 12 node converter

2.2.3 Individual Node Requirements

The nodes were originally described as "multiple smaller converters". In a practical converter they have certain requirements and these requirements determine how they are implemented. The nodal requirements are:

- Each node needs to be separately isolated. In other words their outputs cannot have a common ground as this would not allow them to be serially connected.

- Each node requires an adjustable output to span the entire output range. If a continuous output voltage range is to be produced with an even number of identical nodes then each node requires a two times output range. i.e. each node must be capable of delivering constant power even if its output voltage varies by up to 50 % below its nominal voltage.
- When paralleled the nodes must be capable of sharing current equitably between themselves. The current should be shared in proportion to the capacity of the nodes. For identical nodes this means that the current would be shared equally between the nodes.

The first requirement means that it is likely that each node will consist of a forward or flyback converter [3] [4]. This provides the necessary isolation between nodal outputs due to the high frequency transformer or coupled inductor present in these topologies. A two times output range will be possible with these topologies, although it will result in over specification at some of the node's operating points. Current sharing is also possible using passive means or by individually controlling the current of each node. Current sharing is discussed in the next chapter.

2.2.4 Multi-node Converter Switch Implementation and its Implications

Figure 2.1 shows a multi-node converter schematic where the switches in the schematic are simply shown as ideal switches. How these switches are practically implemented has a large effect on the capabilities of the converter and also on its complexity. Three main choices exist for how to implement these switches: with semiconductor switches, with relays or manual switches and with hard-wired connections. Each of these options are discussed further below.

2.2.4.1 Implementation with Semiconductor Switches

In this implementation the architectures switches are implemented with semiconductor switches, such as MOSFETs or IGBTs. In such an implementation an intelligent controller would be able to change the converter's configurations rapidly and in real time. This means that a converter with the capability of changing its current and voltage capabilities in real time can be produced. From a performance and capabilities perspective this is the most capable multi-node converter implementation, however implementing the switches using semiconductor devices may be complicated and expensive.

The drivers required for any semiconductor switches must be capable of keeping the switch on for indefinite time periods and most of the drivers must also drive a high-side switch. These two requirements will introduce significant complexity to the converter and may also negate some weight, cost and size advantages held by the topology (discussed further in the next chapter). For this reason it may only be worth implementing a multi-node converter with semiconductor switches at higher power levels (where the cost, weight and size of the drivers is negligible compared to the passive components) or where high performance over a very wide range is a defining requirement for a design.

2.2.4.2 Implementation with Relays or Mechanical Switches

In this case the switches are implemented using relays or mechanical switches. The converter would not be capable of real time configuration changes under load, but it is still capable of changing its voltage and current capabilities with very little difficultly. However, complex driver circuitry is not required to control the switches and a multi-node converter can be built with very little size, weight and cost overheads due to the switch implementations. This implementation allows for some middle-ground between the semiconductor and hard-wired implementations.

2.2.4.3 Implementation with Hard-Wired Connections

Since it can take an experienced engineer significant time to design, prototype and finalise a new switched mode converter design [5], any way to minimise this time and associated cost would be welcome.

Multi-node converters could shorten this lead time in many cases. A multi-node converter can be designed to output a certain output power with a wide output range. When a converter with a specific output voltage and approximately that power is required the converter can simply be hardwired into the correct configuration. With this technique one converter design can be used to provide power at many different voltage levels without most of the multi-node converter hardware. Utilising this method would shorten design times and lower development costs for converters in the chosen output power range. However, using a multi-node converter in this way would most likely not be economically viable if the manufacturer was intending to mass produce the converter. In this case it would be better to design a new converter. The method would however be viable when smaller numbers of custom converters are being produced.

2.2.5 Analysis

A new multi-node converter topology has been presented. The topology consists of multiple smaller converters that are connected in different series or parallel configurations depending on the required output. This allows the installed capacity required to implement a converter capable of constant output power over a wide range to be decreased significantly. Reducing the installed capacity could result in significant weight, size and cost improvements over a traditional converter if the overhead required to implement the topology does not negate the advantages completely. This will be analysed in later chapters.

One significant difference between a multi-node converter and a traditional converter is how the component stresses vary with output. In a traditional converter the current and voltage stresses that the components must withstand vary directly with the output of the converter. However, in a multi-node converter these component stresses instead vary with the output of the node and not directly with the converter’s output. Through this, some level of decoupling between the component stresses and the

converter's output is obtained. For the example multi-node converter (with 12 identical nodes), the nodal outputs only need to vary by 50 %. This means that the node's component stresses (specifically the voltage and current stresses) will also vary by 50 %. However, the composite converter has a 24 times output range. This means that the component stresses in the 12 node converter vary 12 times less than in a traditional converter.

2.2.6 Future Analysis

The multi-node architecture has been presented in this section. Its operation has been discussed and how it allows a converter's components to be better utilised has been analysed. There are however questions that still need to be addressed before a multi-node converter is built. The questions are:

1. How many nodes should a multi-node converter contain? What affects this choice?
2. Should all the nodes be identical? Or should some nodes have higher voltage and current capabilities than others?
3. How can the topology be implemented in the simplest way?
4. How does the converter's efficiency vary with output?

The first two questions are addressed in the remainder of this chapter. Question three is then answered when a proposed circuit implementation for the converter is given in Chapter 3 and implemented as a prototype in Chapter 4. Chapter 5 then experimentally determines the efficiency of the prototype converter and attempts to verify theoretical models developed in Chapter 3.

2.2.7 Conclusion

A basic introduction into the operation of multi-node converters and their benefits has been given in this section. The multi-node converter architecture allows a converter to output constant power over a wide range; however the stresses that the components in the converter are exposed to only vary over a small range. This allows the converter's components to be better utilised throughout the output range and means we can optimise their selection better than in a traditional converter topology. There are still many questions that need to be answered with regard to how to design, build and operate a multi-node converter. These questions are answered in the following sections and chapters where the architecture is theoretically analysed and modelled. Once the topology is understood a prototype is developed and tested in later chapters.

2.3 Multi-Node Converter Optimisation

This section analyses multi-node converters from an architectural level. It discusses how to choose the relative sizes (in terms of voltage and current capacity) of the nodes and also discusses how many nodes should be used in a converter. This discussion is then verified by simulation using a multi-node converter simulator and a Genetic Algorithm written for the purpose.

2.3.1 Metrics for Analysing Multi-Node Converters

Before the design of a multi-node converter can be optimised there need to be some sort of metrics or measurements by which the design's suitability can be quantified. The reason for developing multi-node converters was to allow the converter's components to be effectively utilised over a wide range. This results in two metrics for determining the suitability of a multi-node converter design:

1. How wide is the output range? This is answered by determining the ratio of $V_{out,max}$ to $V_{out,min}$, where $V_{out,max}$ and $V_{out,min}$ are the converter's maximum and minimum output voltages while delivering constant power (see Figure 1.4).
2. How effectively are the converter's components utilised? How to measure this is more difficult and still needs to be discussed.

The reason for maximising component utilisation is to lower the cost, size and weight of the passive components. The utilisation in these components could be determined by calculating the average inductor current and average capacitor voltage over the entire output range. These metrics are direct measurements of the component utilisation and they would be a useful tool for evaluating the effectiveness of the converter. However, they are not the simplest metrics to calculate. In order to determine these metrics, the average inductor current or capacitor voltage needs to be calculated for any converter that is analysed. This is possible once a circuit implementation has been chosen, and once this has been done, this is how utilisation will be determined. But we would like to first analyse and optimise multi-node converters from an architectural level (i.e. how many nodes should be used and whether or not they should be identical). For this reason a metric that can be easy determined without knowledge of how the nodes are actually implemented is required. For example, a metric for utilisation that can be determined directly from the converter's V-I or P-I curves.

For this reason, two metrics have been chosen and are used to analyse multi-node converters. They are known as the utilisation of installed capacity and as the minimum power ratio. Both of these metrics can be quickly and easily calculated directly from a converter's output curves (V-I or P-I).

Figure 2.4 shows the maximum output power versus output current for a 12 node converter (i.e. its P-I curve). The current axis is normalised to the maximum output current and the power axis is normalised to the converter's installed capacity. The installed capacity is defined as the maximum output power that the converter is able to deliver. In the case of a multi-node converter, the individual installed capacity for all the nodes is summed.

The average utilisation of installed capacity is shown in the figure. This metric is calculated by finding the average output power that the converter is capable of delivering over the output range. This average is then divided by the converter's installed capacity. Maximising this ratio means that

the converter is able to deliver the maximum average power over the output range for a given amount of capacity.

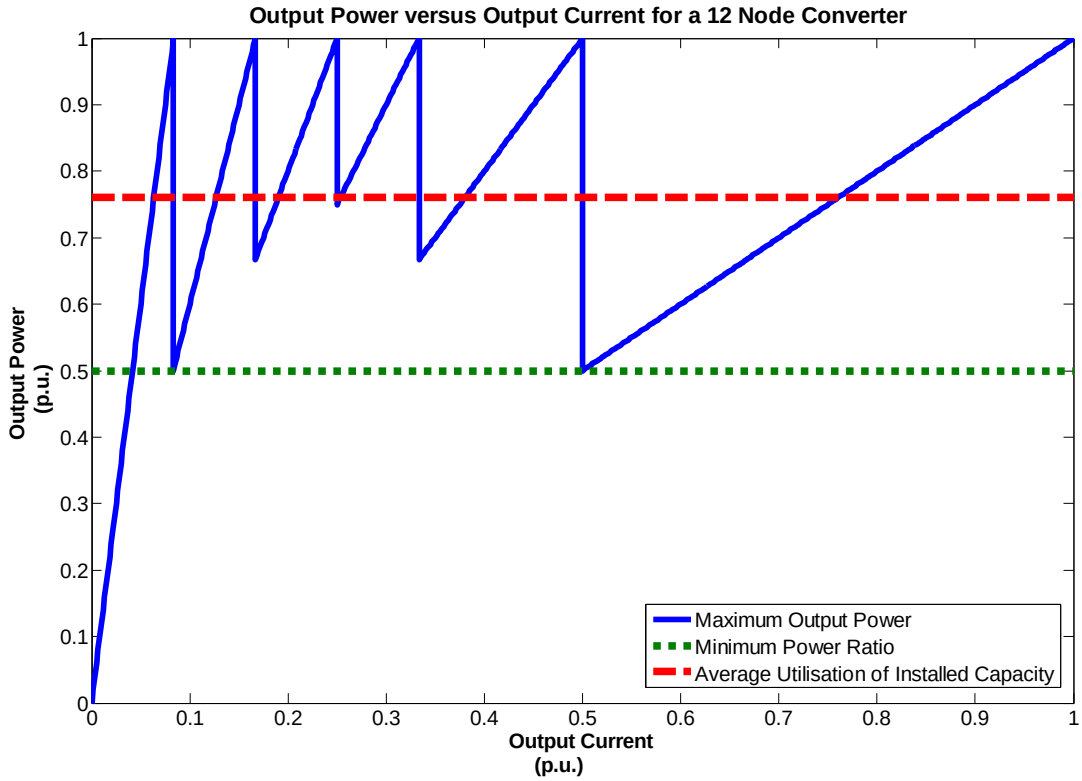


Figure 2.4: Output power versus output current for a 12 node converter

The minimum power ratio is also of importance when designing a multi-node converter. This ratio is calculated by finding the minimum power the converter can deliver over the output range (between $I_{out,\ max}$ and $I_{out,min}$) and then dividing by the installed capacity. This ratio is useful for multi-node converters as it gives a measure of the converter's constant output power potential versus how much capacity is installed. In Figure 2.4 the minimum output power ratio is 50 %. This occurs in all multi-node converters with an even number of identical nodes.

Maximising the minimum power ratio also means that the required output range for each individual node is generally minimised. This is a desirable as it means that range over which the individual node output currents and voltages must vary is smaller, resulting in the components within the nodes being better utilised.

2.3.2 Choosing the Relative Node Sizes

In order to determine what the optimal sizing (in terms of voltage and current ratings) for nodes in a multi-node converter is, we need to decide what criteria affect this choice. The primary criterion is maximising the utilisation of components in the criteria. This is quantified using the utilisation of

installed capacity metric that has already been discussed. Another criterion is to choose relative node sizes that would simplify the design and construction of the converter and its control system.

Identically sized nodes (i.e. with the same voltage and current capabilities) would make it simpler and easier to design, build and control a multi-node converter. This is because if each node is identical then only one node would have to be designed and tested while the rest would simply be copies. This would also simplify manufacturing. If non-identical nodes were used then each individual node would have to be separately designed and tested. Controlling a converter with identical nodes may also be far simpler if current sharing could be implemented passively. So from a practical perspective, identical nodes are a more logical choice.

It can also be argued intuitively that identical nodes also allow the utilisation of installed capacity to be increased. Since, if one chooses nodes with different voltage capabilities then the node with the higher voltage cannot fully utilise its capabilities when it is connected in parallel with lower voltage nodes. This means that the node cannot be fully utilised at all times and there is some lost capacity. The reciprocal argument also applies when one considers nodes with unequal current capabilities. In this case the current capabilities of the larger node cannot be fully utilised when it is connected in series with a smaller node. Figure 2.5 shows the composite V-I curves for two non-identically sized nodes connected in series and parallel. The hatched region corresponds to lost capacity due to the connection of non-identical sized nodes. This factor points toward identical nodes providing better utilisation.

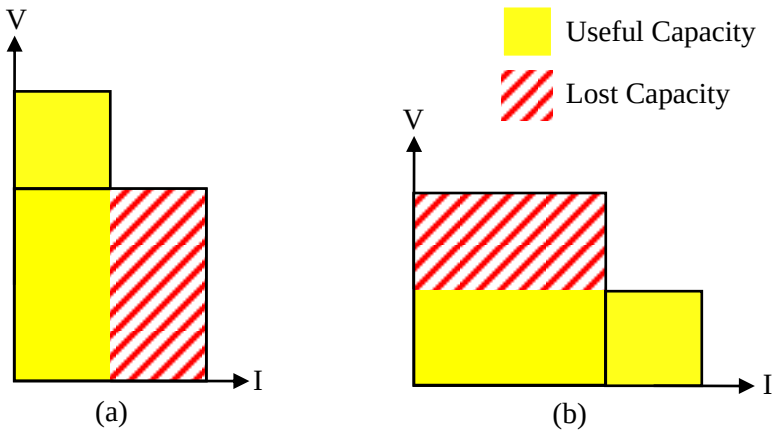


Figure 2.5: Lost capacity with non-identical nodes. (a) Current capacity is lost when a node with a lower current capability is connected in series. (b) Voltage capacity is lost when a node with a lower voltage capability is connected in parallel.

However, this argument does not conclusively prove that identical nodes will help to increase the utilisation of the converter's installed capacity. To further strengthen the argument a simulation program has been written. This simulation program and the results from it are discussed further in Section 2.3.4.

2.3.3 How Many Nodes are Optimal?

When designing a multi-node converter it is important to choose the number of nodes optimally. The number of nodes has an effect on the utilisation of capacity, on the output range of the converter and also on the complexity of the system. This section discusses these issues and provides some guidance for choosing the optimal number of nodes for a multi-node converter.

2.3.3.1 The Number of Nodes and Utilisation

The number of nodes has an effect on the utilisation of installed capacity in the converter due to it affecting the possible flexibility in the system. We need to maximise this flexibility, or the number of useful ways that the nodes can be connected by choosing the number of nodes intelligently.

Figure 2.6 shows the average utilisation of installed capacity versus the number of identical nodes in a multi-node converter. This utilisation curve was generated from a Matlab script written for calculating the utilisation of installed capacity for identical nodes only. It is independent and separate from the multi-node converter simulator presented in Section 2.3.4. The source code for this script is included in Appendix C.

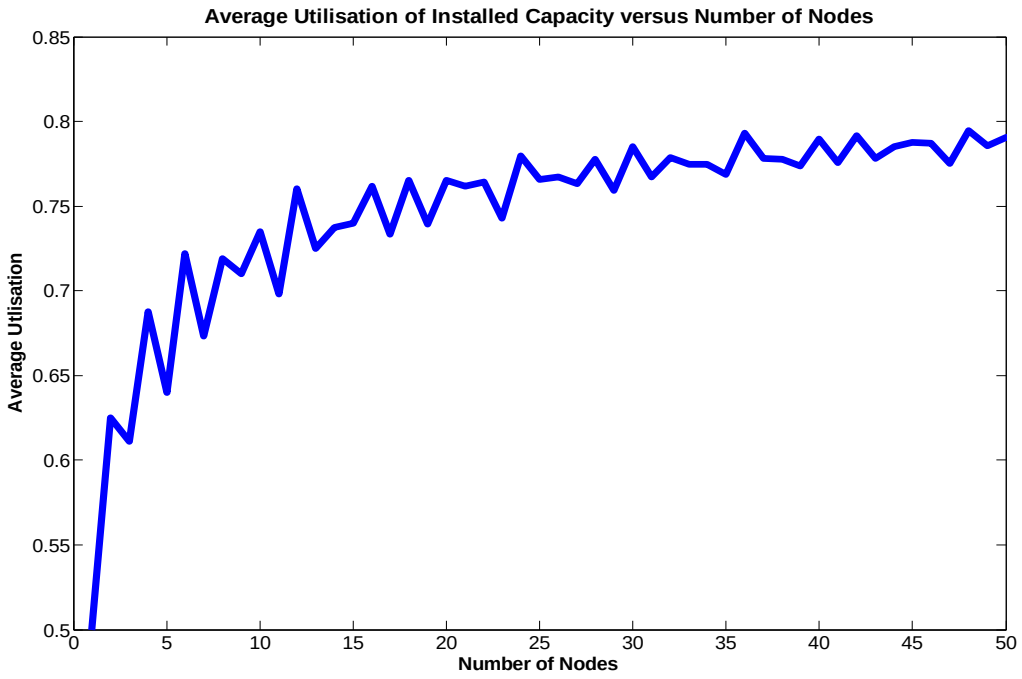


Figure 2.6: Utilisation of installed capacity versus number of nodes

The graph is discrete in nature and some choices for the number of nodes show significantly higher utilisation then their neighbours. These peaks are seen to occur for numbers of nodes with many factors. For example, 6 node, 12 node and 18 node converters all show significantly higher utilisation than their neighbours. This is intuitive since it means that the number of configurations that the converter can be connected in, without leaving out one or more nodes, is increased.

Other choices with fewer factors lead to lower utilisation since not all the nodes can be used at all times. Figure 2.7 illustrates what should be avoided graphically. The figure shows the V-I curve for a converter with five identical nodes and also the V-I curves for each of the three possible configurations with five nodes. When the nodes are connected in series or in parallel all five nodes can be utilised. However, in the series parallel configuration the 5th node cannot be utilised at all. It is wasted and with it 20 % of the converter's installed capacity. This leads to a significant decrease in utilisation over the range. A converter with five nodes actually shows a lower utilisation of installed capacity than a four node converter, despite the increased complexity in the system.

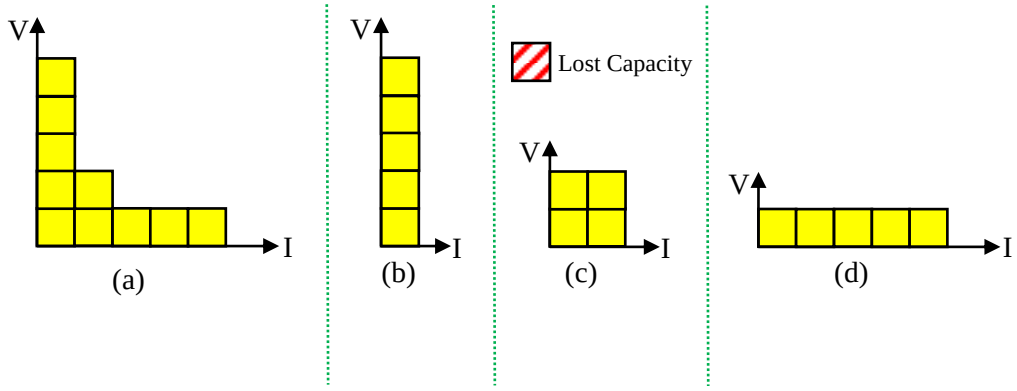


Figure 2.7: (a) The V-I curve for a converter with five identical nodes. (b) Serially connected nodes. (c) Nodes connected in a series/parallel combination. (d) Nodes connected in parallel.

The number of nodes should therefore be chosen such that a situation where one or more nodes cannot be utilised is avoided. The best way to achieve this is to choose the number of nodes to be a number with many factors.

Several other observations can also be made when analysing Figure 2.6.

- Many of the advantages of multi-node converters are available with as few as four nodes.
- The curve becomes less "spiky" when more nodes are used. This is because if one node is not utilised in a converter with many nodes then the lost capacity is less as a percentage than if one node is not used in a converter with only a few nodes.
- The curve flattens out considerably for a high number of nodes. Figure 2.8 shows why this occurs. The figure shows the maximum output power that a theoretical 32 node converter can output versus output current. The maximum possible output power, and thus the utilisation of the converter's capacity, is lower than the average for currents between 0.5 p.u. and 0.75 p.u. This low utilisation in the second half of the figure occurs because the converter is confined to only a single configuration over this range. For multi-node converters with an equal number of identical nodes the average utilisation of installed capacity in the second half of the output current range is 75 %. This limits the maximum theoretical utilisation for these converters to 87.5 % for an infinite number of nodes.

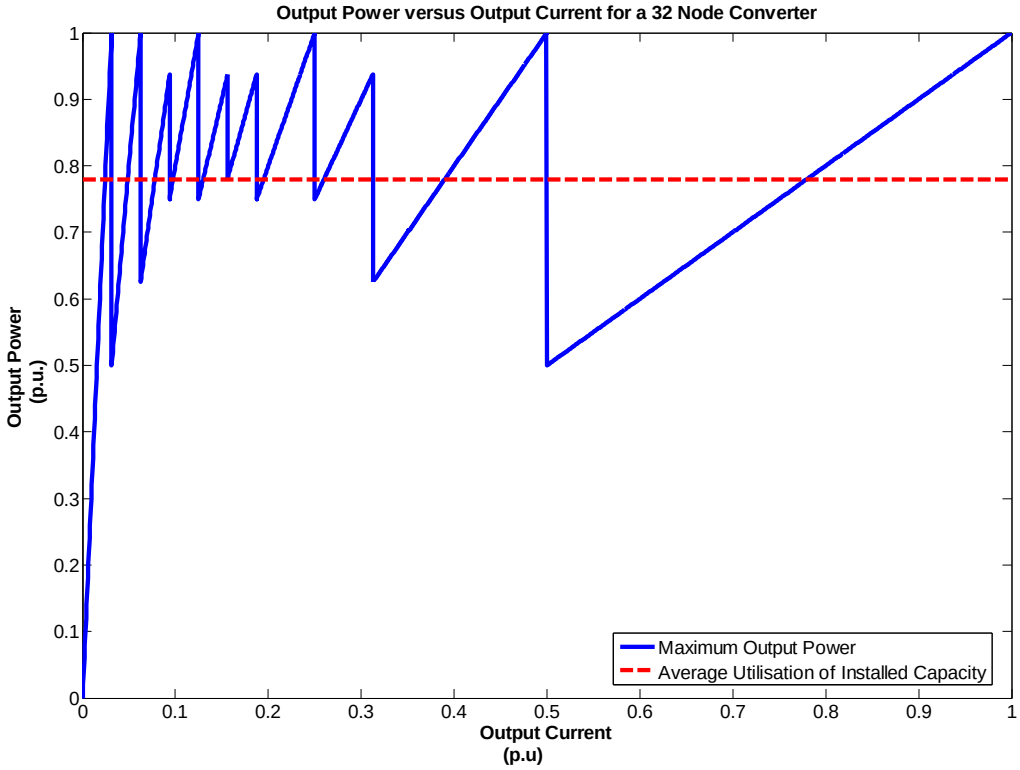


Figure 2.8: Output power versus output current for a 32 node converter

This, combined with low utilisation at very low output currents results in the flattening of the utilisation curve shown in Figure 2.6.

2.3.3.2 The Output Range

The graph showing the average utilisation of installed capacity versus the number of nodes (Figure 2.6) does not tell the full story of multi-node converters since it does not address how a converter's output range varies with the number of nodes. Converters with more nodes may only show a slight increase in utilisation but they may have a much larger output range. The output range for a converter with an even number of identical nodes is equal to twice the number of nodes. For example, a four node converter with nodes that have a two times range will have an overall range of eight times. This seems to imply that we can develop a converter with any arbitrary output range; however we are limited in practice due to the increased complexity of a system with more nodes.

2.3.3.3 Complexity versus the Number of nodes

Increasing the complexity in a system is undesirable if the increased complexity does not bring benefits that are not possible in a simpler implementation. The multi-node converter architecture is inherently more complicated than a traditional converter but it does bring benefits in that it increases the range over which a converter's components can be effectively utilised. However, as the number of nodes is increased farther the system becomes more and more complicated.

We should therefore choose the number of nodes such that the fewest nodes are needed to meet given specifications. The system's complexity is also affected by the complexity of each node and so the nodes should be implemented in the simplest and easiest way. This is another argument for identical nodes as they may allow simpler architectures to be used. This is discussed further when a proposed circuit implementation is presented in Chapter 3.

2.3.4 The Multi-Node Converter Simulator

The multi-node converter simulator is in essence a computer program that was written to allow the suitability of a multi-node converter to be determined in an automated way. The simulator accepts a given nodal configuration (the number of nodes, their current and voltage capabilities and the order of the nodes) and then outputs that converter's V-I curve. It also provides functions for evaluating the design of the converter. For example, the simulator is able to calculate the metrics discussed in Section 2.3.1. This allows multiple converter configurations to be compared and optimised in a short time. The simulator was then coupled with a real-valued Genetic Algorithm that is used to optimise the relative sizes of the nodes. The remainder of this section discusses the simulator and the GA algorithm.

2.3.4.1 Choosing the Software Platform

A multi-node simulator could be implemented on many different software platforms, where each platform has different advantages and disadvantages for the application. Two platforms were considered, namely Matlab and C++. These two platforms were considered due to their suitability and also due to the author being familiar with both. Developing a multi-node simulator would be simpler and easier in Matlab since it includes many different functions for plotting and manipulating data. This means that plotting and other ancillary routines would not have to be written. However Matlab tends to manipulate data and algorithms that aren't in matrix form much slower than C++. For this reason C++ was chosen as the platform for the simulator. Microsoft's Visual C++ compiler was used since it is a free, fully featured and supported product.

2.3.4.2 Assumptions

The following assumptions are made by the multi-node converter simulator.

- Each node has a rectangular area of operation or V-I curve defined by its maximum output current and voltage.
- Each node's output voltage and current can be individually controlled.
- The order of the nodes is defined and does not change.

2.3.4.3 Algorithm Description

The simulator accepts a defined converter configuration in terms of the number of nodes and their individual maximum voltage and current capabilities. The order that the nodes are defined in is also relevant, as this is the order in which the nodes are placed next to one another in the simulated multi-node converter. How the switches are numbered in the simulator is also shown in Figure 2.1. The simulator then tries each and every possible switch configuration by using each bit of an integer to represent the position of each of the switches. If the mth bit of the integer is set then this indicates that the mth node is connected serially to the $(m + 1)^{th}$ node. If the bit is not set, then the relevant node is connected to output rail. For an n node converter an (n-1) bit integer is required and 2^{n-1} combinations must be tried. This does mean that the algorithm scales exponentially with the number of nodes and the runtime will increase significantly when more nodes are added to the converter being simulated.

Once a switch position is defined the algorithm needs to determine the V-I curve for the converter with this switch configuration. How this is achieved is outlined in Figure 2.9 for an example converter consisting of five nodes with different voltage and current capabilities.

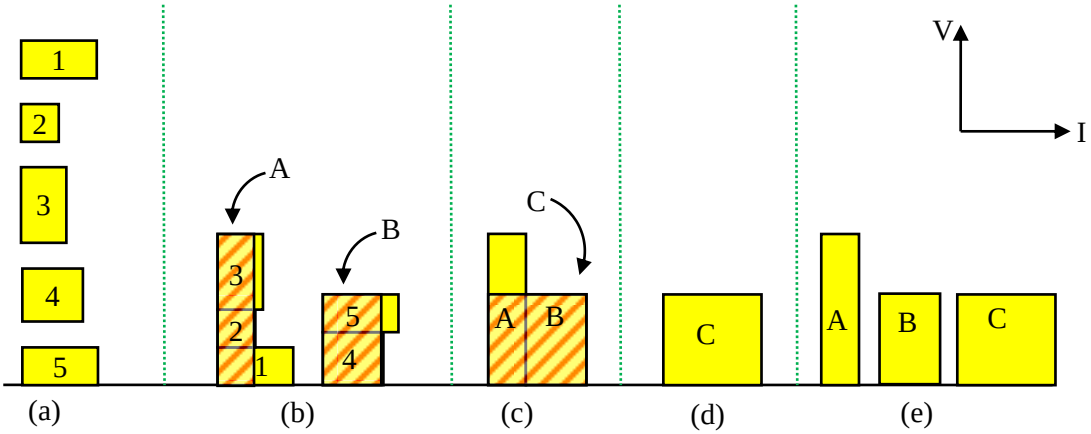


Figure 2.9: (a) The individual V-I curves for the 5 nodes. (b) The nodes are combined into node strings consisting of one or more nodes depending on which switches are closed. The V-I curves are combined accordingly. (c) The node strings then combined to get the final V-I curve for this configuration. (d) The final V-I curve for the configuration. (e) the V-I curves that are saved for these nodes with the given switch position

Figure 2.9 (a) shows the individual V-I curves or the operating capabilities of the individual nodes. They are numbered from one to five. The nodes are then combined in Figure 2.9 (b) using a given switch position. In the example, there are two series strings of nodes. Node one, two and three are connected in series and form the first string (String A) and node four and five are connected serially and form the second string (String B). The capabilities of the combination of nodes in each string is then determined and this is shown as the hatched region. For a string of series nodes, the node with the lowest current rating determines the current rating of the string while the node voltages are added.

Node String A and Node String B are then combined in parallel. Figure 2.9 (c) shows the V-I curve for the parallel combination of the two node strings. When the strings are connected in parallel the

node string with the lowest voltage sets the output voltage for the combination, while the currents are added. The combined V-I curve for the two node strings is labelled as 'C' and is shown as the hatched region in Figure 2.9 (c) and as Figure 2.9 (d). This V-I curve is then the possible area of operation for the nodes with the given switch position. The operating regions or V-I curves for each of the node strings (A and B) and also for them combined (C) are then stored. The three V-I curves that would be stored for the example are shown in Figure 2.9 (e). Operation outside of these regions could lead to the failure of one or more nodes.

This procedure is then repeated for each and every possible switch combination (by incrementing the integer describing the state of each switch in the converter) and the V-I curves for each configuration are stored.

Once all of the converter's possible V-I curves with each possible switch position has been determined and stored they are combined. How this is achieved is explained with the help of Figure 2.10. Figure 2.10 (a) shows some V-I curves that may have been stored after the previous step. They have been sorted by decreasing voltage capability and nodes with identical voltages are sorted by decreasing current capabilities. These nodes are now combined and form the composite V-I curve shown as Figure 2.10 (b). Once this V-I curve has been derived it is relatively trivial to determine the utilisation of installed capacity and minimum power ratios. This allows different configurations to be easily compared in an objective and automated manner.

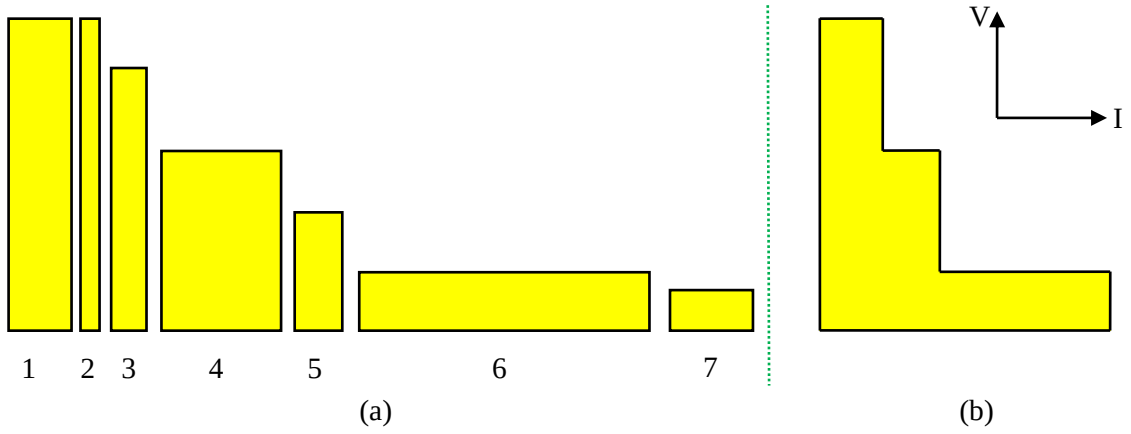


Figure 2.10: (a) Possible V-I curves for all of the different switch positions. (b) The final V-I curve.

2.3.4.4 Multi-Node Converter Simulator Limitations

The multi-node converter simulator's major limitation is the maximum number of nodes that it can simulate. The algorithm that has been developed scales rapidly in both computation time and memory requirements when more nodes are added. The sort procedure that sorts the V-I curves into decreasing voltages is the main reason for this. This sort procedure has been rewritten, using different techniques and algorithms, but this procedure continues to play a large part in limiting the maximum number of

nodes that can be simulated. At present the simulator is limited to approximately 10-12 nodes. Simulating more nodes is possible however the time taken to simulate a converter becomes prohibitive if many configurations need to be compared.

2.3.4.5 The Genetic Algorithm

The multi-node converter simulator is a valuable tool for determining the suitability of multi-node converter configurations. However, it provides no actual tools for optimising the multi-node architecture. For this reason it was decided that a modern optimisation algorithm should be integrated with the simulator so that the multi-node converter architecture could be optimised. This optimisation could have been achieved by a complete search of the search space or with randomly trying a large number of different configurations, however it was hoped that a modern search technique such as a Genetic Algorithm (GA) could decrease the runtime significantly.

For this reason a Genetic Algorithm optimisation routine was written for choosing the node sizes. The Genetic Algorithm works on the principle of evolution and gradual mutation or survival of the fittest [6] [7]. The algorithm that was written and used in the final simulator is shown as a flowchart in Figure 2.11. The final algorithm and the mutation and reproduction methods that were used were the result of testing with the simulator to determine which methods were best suited to the problem.

The algorithm works by initially guessing a population of genomes. In the case of the multi-node converter problem this statement means that a certain number (a population) of converter configurations with randomly sized nodes are generated. Each converter configuration is then known as a genome. Each genome thus consists of multiple real numbers referring to the maximum output voltage and current for each node.

Each genome or converter is then simulated using the converter simulator and the fitness of each configuration is determined and stored. This term “fitness” with regard to Genetic Algorithms refers to how optimal the genome is at solving the problem. In this implementation the fitness is simply equal to the average utilisation of installed capacity for a particular genome and we are looking for the optimal converter configuration which is most fit or which has the highest utilisation.

The population of genomes is then passed through an evolutionary model where individual genomes are reproduced, combined and mutated. Reproduction refers to which genomes are passed onto the next generation and will be tested again. Genomes with higher fitness’s are given preference and are more likely to continue to the next population. This is similar to in nature where the strongest individuals are supposed to be most likely to reproduce successfully.

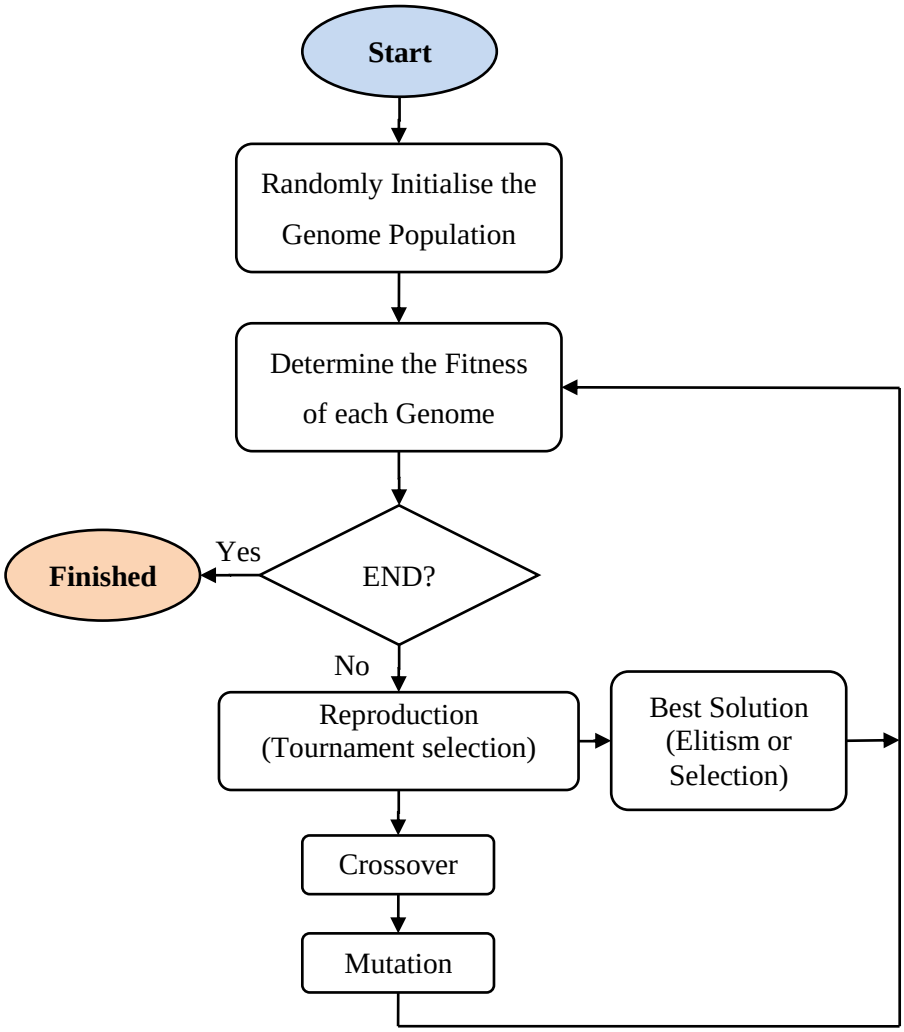


Figure 2.11: Genetic Algorithm flowchart

Reproduction in Genetic Algorithms is commonly modelled using statistical means or by tournament selection. In statistical reproduction, each genome has a statistical change of passing onto the next generation and this statistical chance is related to the genomes fitness. Fitter genomes are thus more likely to reproduce. Tournament selection is where (k) different genomes are randomly selected and the fittest of the (k) individuals is passed onto the next generation. This is repeated until the required numbers of genomes for the next generation have been chosen. By varying the number of genomes that are compared (k), a balance can be struck between allowing weak genomes to reproduce and converging on a solution too quickly. This can lead to local maximums being selected instead of true global optimums. Tournament selection was used in this GA implementation [6].

Once reproduction has occurred, the genomes are modified using two genetic operators, namely crossover and mutation. In crossover two or more genomes are spliced and combined so that a new genome combining properties of each "parent" is produced. Crossover can be compared to an individual receiving genes from both their parents. In other words, the individual or genome is a combination of both parents or both parent genomes. Finally, mutation takes place where each

genome has a statistical chance of being modified slightly [7]. In the case of a real valued genome this is often achieved by adding or subtracting a small number. Mutation is very important to Genetic Algorithms and is used to help the Genetic Algorithm to find a true global optimal solution instead of zoning into a local maximum.

The result of the reproduction, crossover and mutation stages is a brand new population of genomes that are related to the previous genome but not identical. The fact that higher fitness genomes were more likely to reproduce and continue to the next generation also means that the fitness of the population generally increases with time. The chances of the average fitness increasing can also be increased by using elitism (also known as selection). This procedure selects the fittest individual of every population and makes sure that it passes onto the next generation unmodified [6] [7].

Once the new population has been generated it is then passed through the simulator again so that the fitness for each converter configuration in the new population can be determined. This process of reproduction, crossover and mutation followed by re-evaluation of the fitness is repeated until an optimal solution has been found or until a certain number of generations have passed. If the algorithm is designed and optimised correctly then this should result in an optimal genome being found. However, there is some danger as this is a statistical process and so local maximums may be found occasionally. To guard against this it is wise to run the algorithm more than once.

2.3.4.6 The Genetic Algorithm's Results and Output

The Genetic Algorithm was used to determine the optimal converter configuration with different numbers of nodes. It was found that the converter generally showed a higher utilisation of installed capacity when the nodes were the same size. However, there were some exceptions to this rule that were noticed when the number of nodes meant that not all of the nodes could be used at all times. This is often seen when the number of nodes is a prime number (see Section 2.3.3.1). In this situation better utilisation can often be achieved with fewer nodes. This can be seen in Figure 2.6 where converters with 3, 5 or 7 nodes all exhibit lower utilisation than 2, 4, or 6 node converters. In this case the GA optimises the converter by making either the first or last node negligibly small. This is achieved by making the voltage or current capacity of that node very small or zero. In essence the Genetic Algorithm optimises a 3, 5 or 7 node converter by turning it into a 2, 4 or 6 node converter. This shows how important it is to choose the number of nodes intelligently.

The multi-node node architecture has only been optimised for up to eight nodes due to the computational complexity and time involved in simulating converters with more than eight nodes. An example output for a six node converter is shown as Table 2.1, Figure 2.12 and Figure 2.13. Table 2.1 shows the genome with the highest fitness found by the GA after 300 generations. If we look at the relative node sizes we can see that they are all approximately equal in size. This corresponds with the

prediction that identically sized nodes lead to higher utilisation. The final utilisation found by the GA on this run was 0.719 which is close to the utilisation with identically sized nodes (0.722).

Table 2.1: The Genetic Algorithm's optimal node sizes for a six node converter

	Voltage Rating (p.u.)	Current Rating (p.u.)
Node 1	0.166742	0.165807
Node 2	0.166633	0.166936
Node 3	0.166909	0.166077
Node 4	0.165509	0.165547
Node 5	0.167059	0.167971
Node 6	0.167148	0.167661
Total	1	1
Average Utilisation of Installed Capacity	**0.719212**	

Figure 2.12 then shows the output from the GA. Each line in the figure corresponds to one generation of genomes. From the figure, we also note that the highest utilisation found by the algorithm has been constant for several generations. This is often a good time to stop the algorithm as it will take many more generations to find an exact optimal solution than it takes to find a ballpark solution. If an exact solution is required then it is recommended that the search space be searched exhaustively near to the GA's solution.

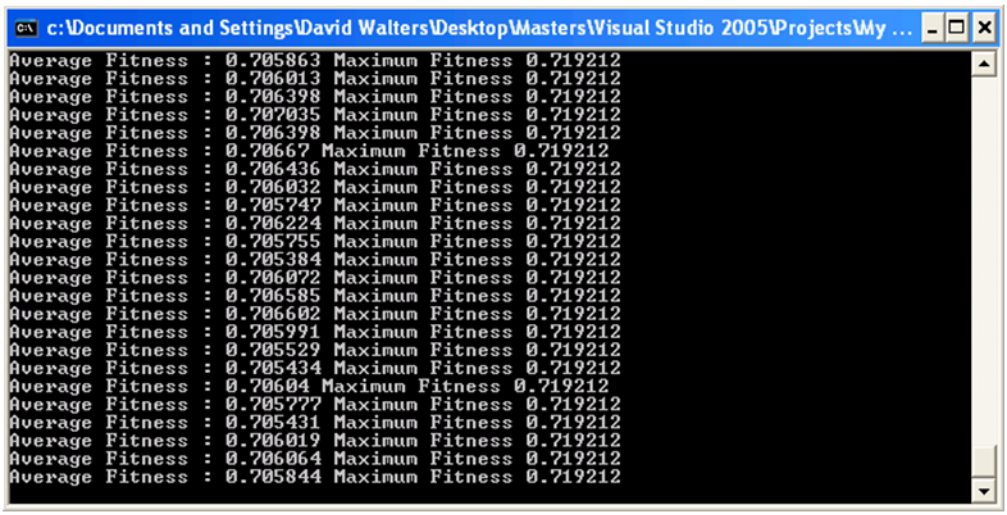


Figure 2.12: The Genetic Algorithm's output while simulating a six node converter

Figure 2.13 shows the output from the multi-node simulator (a V-I curve) for the fittest individual found (see Table 2.1).

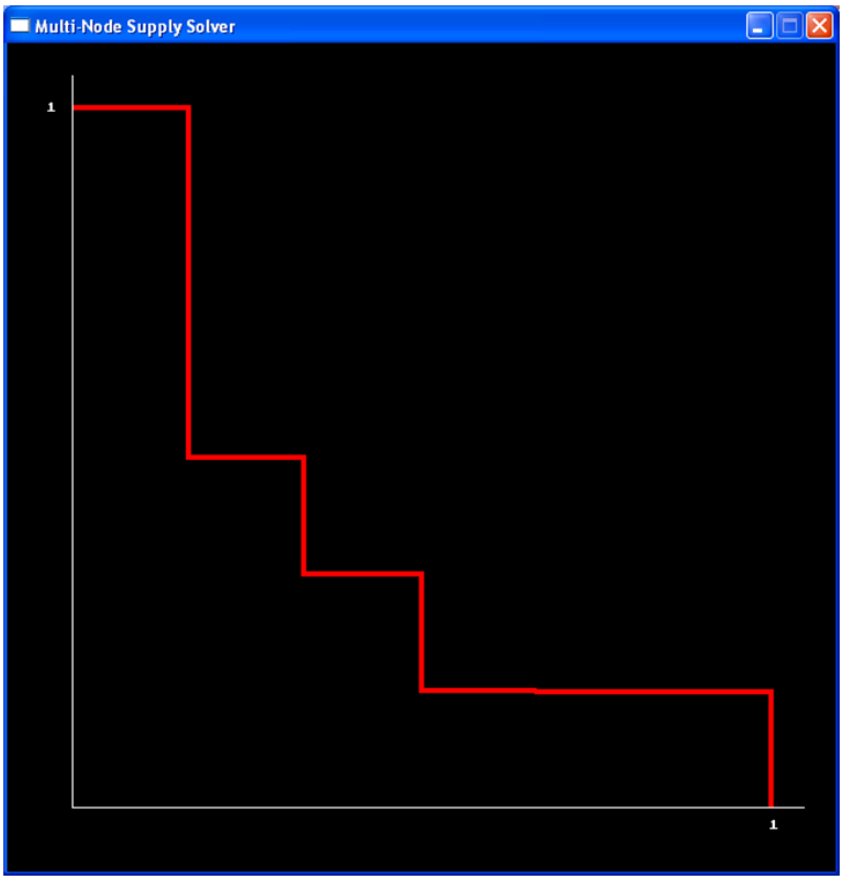


Figure 2.13: The multi-node converter simulator output showing the V-I curve for the fittest genome found for a six node converter. (The vertical axis is voltage p.u. and the horizontal axis is current p.u.)

Table 2.2 now shows the Genetic Algorithm's optimisation of a seven node converter. We can see that node seven's influence has been removed by its output current being very low. The other nodes have current capabilities that are almost equal.

Table 2.2: The GA's optimisation for a seven node converter

	Voltage Rating (p.u.)	Current Rating (p.u.)
Node 1	0.152870	0.167793
Node 2	0.152703	0.168340
Node 3	0.153310	0.166605
Node 4	0.153041	0.168411
Node 5	0.153436	0.164450
Node 6	0.153550	0.163976
Node 7	0.081090	0.000426
Total	1	1
Average Utilisation of Installed Capacity	**0.718782**	

Table 2.2 also shows the voltage capabilities for the seven node converter. The first six nodes all have approximately equal voltage capabilities. The seventh node has a different voltage capacity; however this is irrelevant to both the output of the converter and its utilisation due to that nodes negligible current capacity. The only effect of the seventh node is to change the per unit voltage values for the

other six nodes. It is also noticed that with a negligibly sized first or seventh node the utilisation for a seven node converter is close to that of a six node converter.

2.3.5 Conclusion

The multi-node converter architecture has been analysed with regard to how to choose the number of nodes and whether or not they should be identically sized. This analysis was carried out using logical arguments and simulations written for the purpose. A multi-node converter simulator was written in C++ and this simulator was coupled with a Genetic Algorithm that is capable of optimising the converter's configuration. The results of the simulation and optimisation corresponded with the logical deductions that were made.

It was found that identically sized nodes resulted in higher utilisation of installed capacity for the converter. Identically sized nodes are also easier to control and simplify the design and implementation of a converter. Thus, identically sized nodes are currently seen as the best choice for multi-node converters.

How to choose the optimal number of nodes was then considered, and it was found that choosing the number of nodes to be equal to a number with many factors increased the utilisation of the converter. This is intuitive as such a converter can be arranged in many different configurations without a node being wasted. This result was confirmed using the multi-node converter simulator and a Genetic Algorithm, where converters where the number of nodes was a prime number were optimised by negating the effect of some of the nodes. In the example presented a seven node converter was optimised by making the seventh node negligibly small. In essence the seven node converter was optimised by turning it into a six node converter.

This theoretical analysis of the multi-node converter architecture is now used to develop and analyse a proposed practical implementation. This proposed implementation will now be discussed before a prototype converter is presented in Chapter 4.

2.4 Conclusion

This chapter introduced the multi-node converter architecture. How the architecture is able to improve the utilisation of the components within the converter was then discussed. The strength of the multi-node converter is that it is able to output constant power over a wide output range despite the fact that the stresses that its components are exposed to only vary over a small range. It is expected that this will allow a multi-node converter's passive components to be smaller, lighter and cheaper than the components within a traditional converter. Whether or not this is true is discussed in Chapter 3.

How to optimise a multi-node converter at an architectural level was then presented and it was found that identical nodes tend to result in better utilisation of the converter's capacity. It was also argued

that choosing the number of nodes to be equal to a number with many factors is also beneficial. A multi-node converter simulator was then written so that these results could be confirmed. The simulator was coupled to a Genetic Algorithm so that the multi-node converter architecture could be optimised. The Genetic Algorithm confirmed the initial arguments made with regard to the number of nodes and their relative sizes. In other words, a multi-node converter with identical nodes is currently regarded as the optimal multi-node converter configuration. The number of nodes should also be chosen to be a number with many factors.

Now that the multi-node converter architecture has been optimised it is possible to develop, analyse and model a proposed circuit implementation. This is the subject of the next chapter.

CHAPTER 3

THEORETICAL ANALYSIS OF A PROPOSED MULTI-NODE CONVERTER IMPLEMENTATION

3.1 Introduction

The first chapter showed why a traditional converter is unable to utilise its components effectively when its output varies over a wide range. Multi-node converters were then presented and why they are able to show improved utilisation of their installed capacity was discussed in the second chapter. The multi-node converter architecture was then optimised at an architectural level.

This chapter presents a proposed circuit implementation for a multi-node converter based on the results of the optimisation of the architecture. Implementation issues such as current sharing in the converter and the filter requirements for each node are then theoretically analysed. Mathematical models describing the operation of the converter, including component losses, are then developed. These models allow a multi-node converter to be compared with a traditional converter in a comparative design example. Once this theoretical analysis is complete the practical implementation and testing of a multi-node converter can be discussed in later chapters.

3.2 The Proposed Implementation

The multi-node converter prototype will be implemented using a forward converter with multiple identical secondaries. A forward converter was chosen since it is generally regarded as a robust and reliable topology. After considering both the single switch and the two-switch forward converter topologies, the two-switch forward converter topology was selected. Its operation is now analysed and reasons for selecting it over the more common single switch topology are given. How to passively share current between multiple nodes and also how the filter components and their requirements change when more nodes are added is then discussed.

3.2.1 The Two-Switch Forward Converter

The two-switch forward converter topology is shown as Figure 3.1 [3] [4]. Multiple identical secondaries or phases have been added to the topology so that multiple outputs can be generated with only one transformer. A coupled inductor is used for the filter inductors and so only two cores are required to implement the topology. The converter's operation is now discussed.

In the two-switch topology, the two MOSFETs (M_1 and M_2), are operated simultaneously, i.e. both are on or off at the same time. When both switches are on, current flows from the source, through the

transformer's primary winding, and back to ground. The transformer's secondaries also conduct and power is delivered to the filters and load.

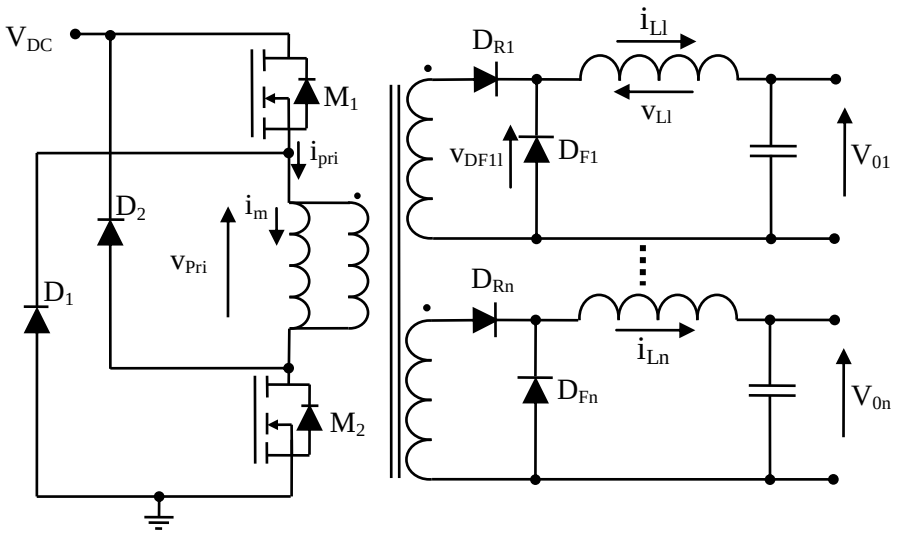


Figure 3.1: The two-switch forward converter with multiple identical secondaries

When the MOSFETs are turned off, the transformer's magnetising current (i_m) continues to flow by forward biasing the clamping diodes (D_1 and D_2). This reverses the transformer's primary side voltage (v_{pri}) and means that the core is reset each cycle to prevent saturation of the core without a separate demagnetising winding being required. To ensure that there is sufficient time for the core to reset each cycle, it is important to ensure that the MOSFET's duty cycle is kept below 50 % [3]. The duty cycle must be limited by the PWM controller. The operation of the converter is further described in the next section.

3.2.2 Ideal Steady State Voltage and Current Waveforms

Some pertinent steady state waveforms for the two-switch forward converter are shown below as Figure 3.2. The voltage seen by the transformer primary (v_{pri}), the magnetising current (i_m), the current flowing in one secondaries inductor (i_{L1}) and the total primary current (i_{pri}) are all shown in the figure.

The converter's operation can be divided into three time periods: t_1, t_2 and t_3, where the sum of these time periods equals the switching period for the converter. During t_1, the main semiconductor switches are conducting and power is transferred to the secondary side filters via the rectifying diodes (D_{R1} to D_{Rn} in Figure 3.1). The secondary side filter inductor currents (i_{L1} to i_{Ln}) and the transformer's magnetising inductance current (i_m) both increase during this time period. The length of t_1 is set by the converter's duty cycle.

During the second time period, the main semiconductor switches have been switched off and the transformer's magnetising inductance current commutates to the clamping diodes (D_1 and D_2 in Figure

3.1). This reverses the voltage seen by the transformer primary and starts to reset the core. This time period continues until the transformer's magnetising current (i_m) reaches zero and the clamping diodes switch off. This occurs when area 'A' in Figure 3.2 equals area 'B', or when the average voltage applied to the transformer's magnetising inductance equals zero. At this time the core has been successfully reset. Note that in the ideal case, t_1 and t_2 are equal in length (if one neglects the two clamping diode forward voltage drops). Throughout this time period, power is not delivered from the primary to the secondary side and the filter inductor current flows through the rectifier's freewheeling diodes (D_{F1} to D_{Fn} in Figure 3.1).

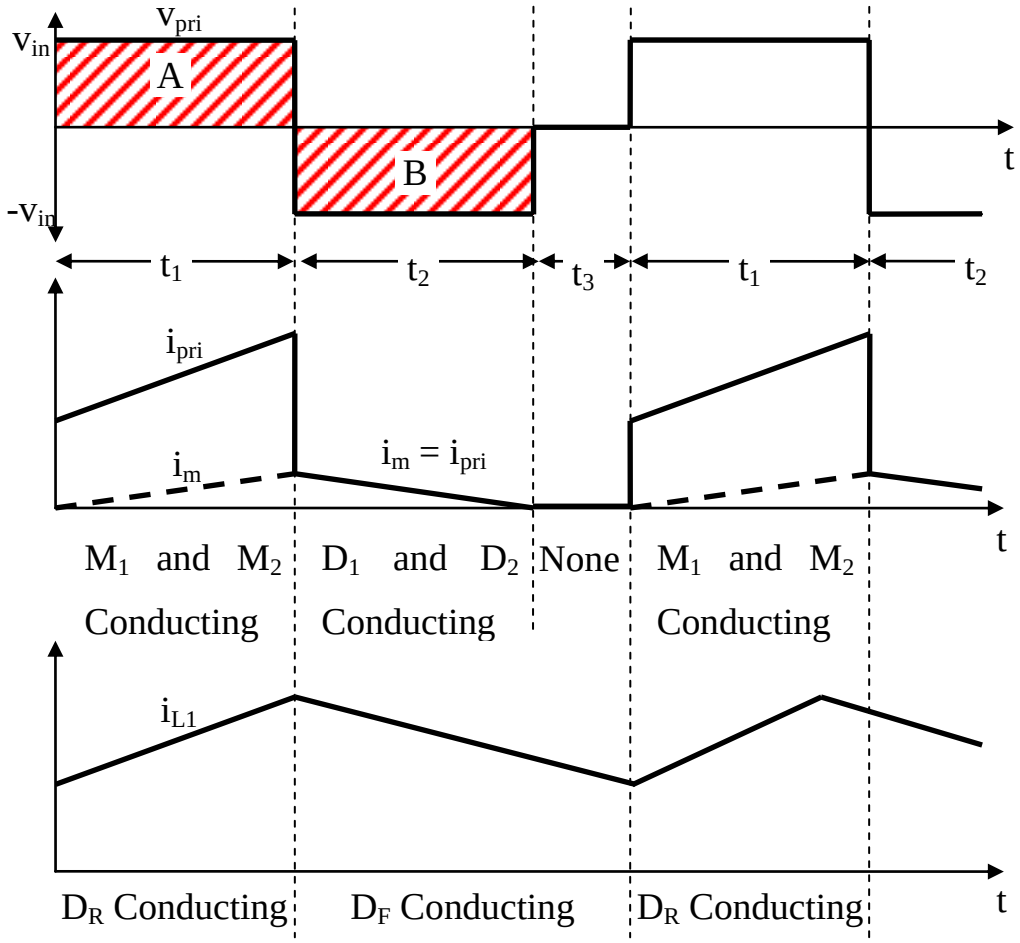


Figure 3.2: Ideal voltage and current waveforms for the two-switch forward converter

Once the core has been reset, t_3 begins. Time period t_3 is simply the remaining time left in each switching period after t_1 and t_2 have finished. During this period, no current flows in the main semiconductor switches or in the clamping diodes. Power is also not transferred to the secondary side and so the secondary side inductor current continues to flow through the freewheeling diodes (for CCM). Note that, although t_3 may be very short, it must exist in every switching cycle. Otherwise the core is not being reset correctly, which leads to saturation.

3.2.3 Advantages and Disadvantages of the Two-Switch Forward Converter Topology

The two-switch forward converter topology has numerous advantages over the standard single switch topology. These advantages include the fact that each of the MOSFETs must only withstand half of the voltage as in a single switch topology and that their voltages are also clamped to the DC bus voltage by diodes D_1 and D_2 when they turn off. Another, more pertinent, advantage for the application is that the transformer core does not require a separate demagnetising winding as in a single switch forward converter. This means that numerous transformer configurations can be built and tested while not worrying about how to include the demagnetising winding and whether the core will be reset properly each cycle. This will simplify transformer design and is the primary reason why this topology has been selected over the more common single switch forward converter [3].

Some disadvantages for the topology include the fact that two switches are required and that one of the switches will require a high-side driver. Established methods exist for driving this high-side MOSFET, and even through two MOSFETs are required, they can be smaller than the MOSFET required in a single switch forward converter. Therefore, these disadvantages are not an onerous as they could seem and it has been decided that for the topology, the advantages outweigh the disadvantages. It has therefore been chosen as the topology for the prototype converter.

3.2.4 Current Sharing between Phases

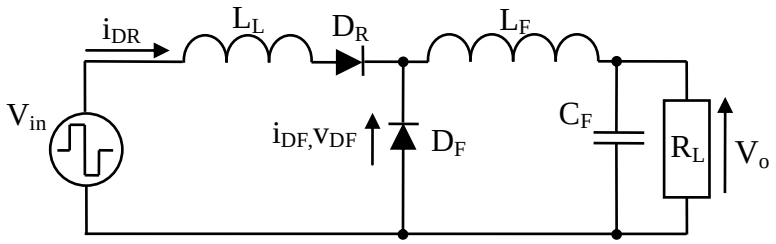
In order to share component stresses equally among the nodes, it is important to share the load current between phases when they are paralleled. To achieve this, the factors that degrade current sharing in the topology need to be analysed. This section will discuss current sharing mismatches due to the transformer's leakage inductance and due to component mismatches.

3.2.4.1 Leakage Inductance Effects on Output Voltage

Each of the secondary outputs shown in Figure 3.1 has a slightly different leakage inductance due to how it is wound on the core. In most cases this leakage inductance plays a larger part in degrading cross and load regulation in the converter than any other factor [8]. Therefore, the part that leakage inductance plays in degrading the converter's performance needs to be analysed so that its effects can be minimised.

Figure 3.3 shows a single phase output for a forward converter. The figure also shows the definition for the model's input voltage where:

- v_{DC} is the primary side DC bus voltage.
- N_s/N_p is the transformer's turns ratio.
- D is the converter's duty cycle at the switching period T_s.



$$V_{in}(t) = \begin{cases} v_{dc}.\frac{N_s}{N_p} & \text{For } (k-1)T_s < t < kDT_s \\ -v_{dc}.\frac{N_s}{N_p} & \text{For } kDT_s < t < 2kDT_s \\ 0 & \text{Otherwise} \end{cases}$$

$k = 1,2,3...$

Figure 3.3: A single phase forward converter model with the transformer's leakage inductance included

Due to the leakage inductance (L_L), current cannot be commutated instantaneously from the freewheeling diode (D_F) to the rectifying diode (D_R). This means that there is a finite time interval between when the rectifying diode begins to conduct and when the freewheeling diode can switch off. During this time interval the rectifier output voltage (v_{DF}) cannot rise since it is pulled low by the freewheeling diode which has not yet turned off. Figure 3.4 shows the current and voltage waveforms for the output model.

In Figure 3.4 at time t_1 the inductor's current begins to commutate from the freewheeling (D_F) to the rectifying diode (D_R). The current rises until all of it flows in the rectifying diode and the freewheeling diode switches off at time t_2. The rectifier's output voltage only goes high at this time. At time t_3 the current begins to commutate back from the rectifying diode (D_R) to the freewheeling diode (D_F). Note that the rectifier output voltage (v_{DF}) drops immediately when the freewheeling diode (D_F) begins to conduct [4] [9].

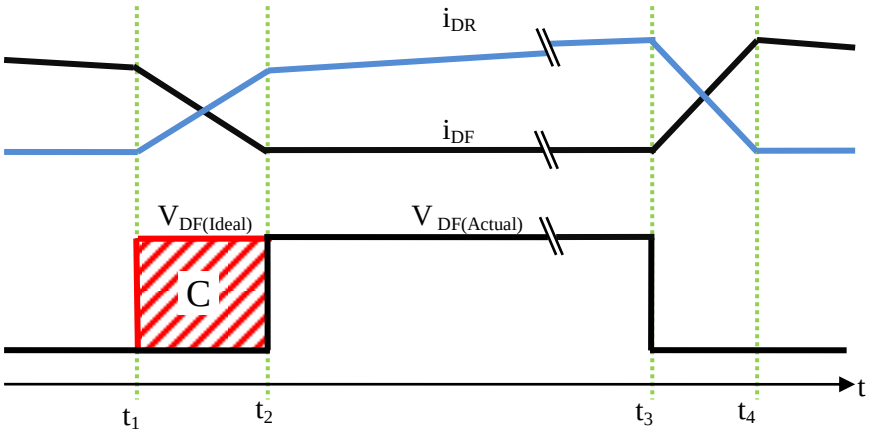


Figure 3.4: Voltage and current waveforms for the single phase forward converter model

The area C in the figure represents a reduction in the volt-second area applied to the filter inductor each switching cycle due to the leakage inductance preventing instantaneous current commutation between D_R and D_F. This causes the output voltage to be slightly lower than expected. Equation (3.1) shows the average output voltage from an ideal forward converter with the leakage inductance's effects included [9].

$$V_o = \frac{N_s}{N_p}.D.V_{dc} - \frac{(Area\ C)}{T_s} = \frac{N_s}{N_p}.D.V_{dc} - \frac{I_l.L_L}{T_s} \quad \textbf{(3.1)}$$

From Equation (3.1), we can visualise the difference in the output voltage due to the leakage inductance as an equivalent lossless series resistance with a value of L_L / T_s. We can also clearly see that the converter's load regulation is affected linearly depending on the leakage inductance and the switching frequency [9]. This is not an insurmountable problem in a closed loop converter design with a single output as the control system can easily compensate by increasing the duty cycle. However it is a problem when multiple secondaries are wound on the same transformer as it leads to cross regulation errors between the phases.

3.2.4.2 Leakage Inductance Effects on Current Sharing with Multiple Secondaries

Equation (3.1) showed how the leakage inductance in a high frequency transformer leads to a forward converter's output voltage being lower than expected. If a forward converter with multiple secondaries is built this leads to a potential problem for cross regulation between the outputs. If each secondary has a slightly different leakage inductance, then the difference between each phase's ideal and actual output voltages will be different. This means that each and every output produces a slightly different output voltage.

From Equation (3.1) we expect the secondary with the lowest leakage inductance to output the highest voltage. Even though this voltage will only be slightly higher than in other secondaries this can lead to a significant current mismatch. The cross regulation error cannot be corrected for using a single feedback loop. If cross regulation in the converter is to be improved then there are two main choices:

- Add additional feedback loops and change the circuit topology presented in Figure 3.1 so that each node's output can be varied individually. i.e. use active current sharing.
- Attempt to minimise the effect of the leakage inductance by careful magnetic design.

The first option results in a far more complex circuit design. It would not be possible to use a common transformer core or common primary side semiconductor switches. For this reason, the design of the transformer will be focused on so that each phase's leakage inductance is equal and a simple circuit design is possible.

The transformer's leakage inductance is caused by magnetic flux that does not completely link the primary and secondary windings [4]. In other words, some flux may only link one of the windings or may only link part of either winding. This is modelled by placing a leakage inductance in series with the transformer windings. Due to the origin of the transformer's leakage inductance, it is intuitive that its value can be modified by varying the physical placement of the windings in the core's window. For this reason, if equal leakage inductances are required then the physical placement of each and

every winding within the winding window needs to be as similar as possible. To achieve this, the transformer's secondaries will be wound multi-filar. This will help to ensure that each and every winding has the same leakage inductance and will minimise the detrimental effect that unequal leakage inductances have on current sharing.

3.2.4.3 Unequal Current Sharing Due to Component Tolerances

Current sharing is also degraded due to component tolerances. Each diode in the rectifier will have a slightly different forward voltage and the inductor and trace resistances in each phase will also vary. This will lead to current sharing unequally in the phases. The resistive effects can be mitigated by designing and building the final PCB and inductor carefully so that there is a low variance between the different phase resistances.

However the effect that different diode forward voltages have on current sharing is difficult to address. If this proves to be a problem in the final design then it may be necessary to add a series resistance to each phase to correct for this. This is discussed in Chapter 4, Section 4.2.1.2.

3.2.5 Filter Requirements versus Number of Nodes

The multi-node converter architecture has been developed as a way of allowing a converter to output constant power over a wide range while still utilising the capacity its components effectively. Through this it is hoped that the component requirements can be reduced. Reducing the passive component's requirements is a particular focus since they are often the largest, heaviest and costliest components in a converter [1] [2]. We thus need to analyse the passive component requirements for multi-node converters and how these requirements change when the number of nodes is changed. This is the focus of this section. How to specify the filter inductor for constant output power, how the required inductance per phase varies with the number of nodes and what effect this has on the final inductor's size and weight are discussed. The filter capacitor's requirements will then be analysed using these results.

3.2.5.1 Model Description

The filter inductance will be specified so that the converter stays in the Continuous Conduction Mode (CCM) at all times. Since the converter's operating point changes, the operating point where the highest inductance is required to maintain CCM needs to be found. This point will be found by analysing a single phase forward converter using the model shown in Figure 3.5. The model's input voltage is also defined in Figure 3.3.

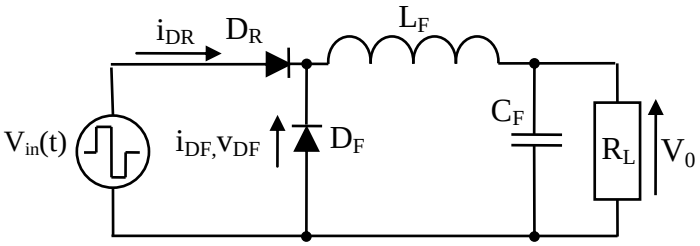


Figure 3.5: Single phase forward converter model

The circuit has been analysed and Figure 3.6 shows the current and voltage waveforms for the filter inductor and the output voltage in the steady state. There are two distinct periods evident in the waveforms, t_1 and t_2, which correspond to the times when either D_R or D_F are conducting.

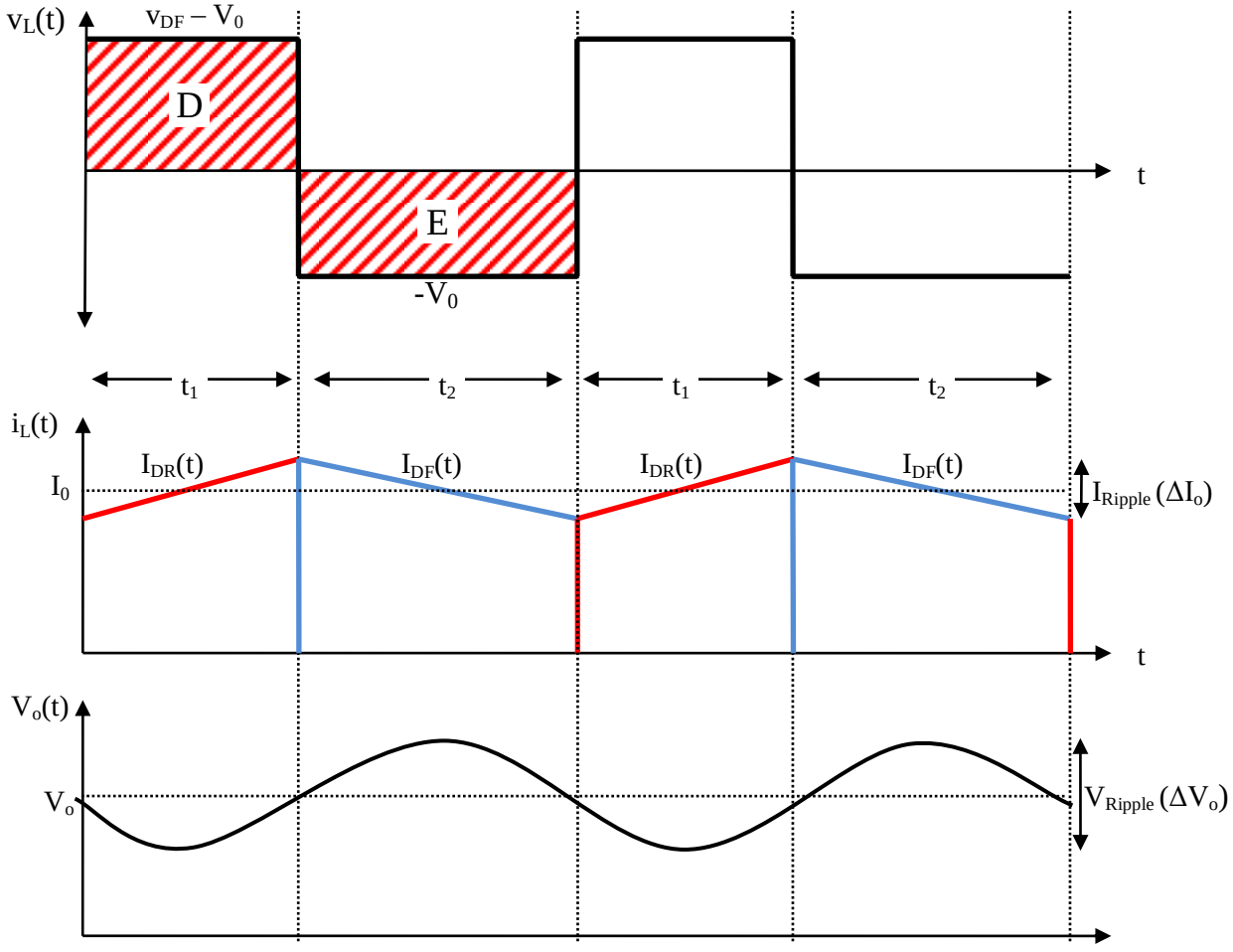


Figure 3.6: Filter waveforms in the Continuous Conduction Mode (CCM)

During t_1, the primary side MOSFETs (not shown in Figure 3.5, see Figure 3.1) and the rectifying diode (D_R) conduct and power is delivered via the filter inductor to the load. During this time period, the inductor current (i_L) increases as positive voltage is applied to it. Once the primary side transistors

turn off, t_2 begins, and the current flowing through the rectifying diode commutates to the freewheeling diode (D_F). This means that the voltage across the inductor becomes negative and approximately equal to the converter's output voltage. This process continues in the steady state with the inductor current repetitively increasing and decreasing each cycle. The inductor's ripple current flows into and out of the output capacitor (C_F) and causes the ripple voltage superimposed on the output. This ripple voltage is highly exaggerated in the figure and in practice the ripple is normally limited to a few percent of the output voltage by using a large filter capacitor with a low ESR.

In the inductor voltage waveform (v_L), area 'D' is equal to area 'E'. In other words, the average inductor voltage over one cycle is zero for steady state operation. This principle can then be used to show that the ideal DC output voltage for the converter is given by Equation (3.2) [4]. This model will now be used to derive an expression for the converter's required filter inductance and how it varies with duty cycle with a constant output power.

$$V_o \approx \left(\frac{N_s}{N_p}\right).V_{DC}.D \tag{3.2}$$

3.2.5.2 Determination of the Required Filter Inductance

The familiar inductor voltage/current equation is shown as Equation (3.3).

$$v_L(t) = L_F.\frac{di_L(t)}{dt} \tag{3.3}$$

For $v_L(t) = V_L$, we can rewrite this as:

$$V_L.\Delta t = L_F.\Delta I_L \tag{3.4}$$

For the time period t_2, and by noting that ΔI_L is equal to twice the output current for the CCM/DCM boundary [4], we can state that:

$$V_o.\Delta t = 2.L_F.I_O = 2.L_F.\frac{P_o}{V_o} \tag{3.5}$$

Where the converter has a constant output power given by P_o.

Then, using Equation (3.2), and recognising that Δt is equal to t_2 or $(1\text{-}D)T_S$, the inductance required to maintain CCM while outputting constant power is expressed as:

$$L(D) = \left(\frac{v_{DC}N_s}{N_p}\right)^2 . \frac{(D^2 - D^3)}{2P_o} . T_s \qquad \textbf{(3.6)}$$

Figure 3.7 shows the shape of the curve defined by Equation (3.6), and how the filter inductance required to maintain CCM varies with the duty cycle can be seen. The minimum inductance required to ensure CCM operation throughout the range can now be found by maximising Equation (3.6) while recognising that the two-switch forward converter is limited to duty cycles less than 50 %. The maximum inductance requirement is therefore found to occur at **D = 0.5**.

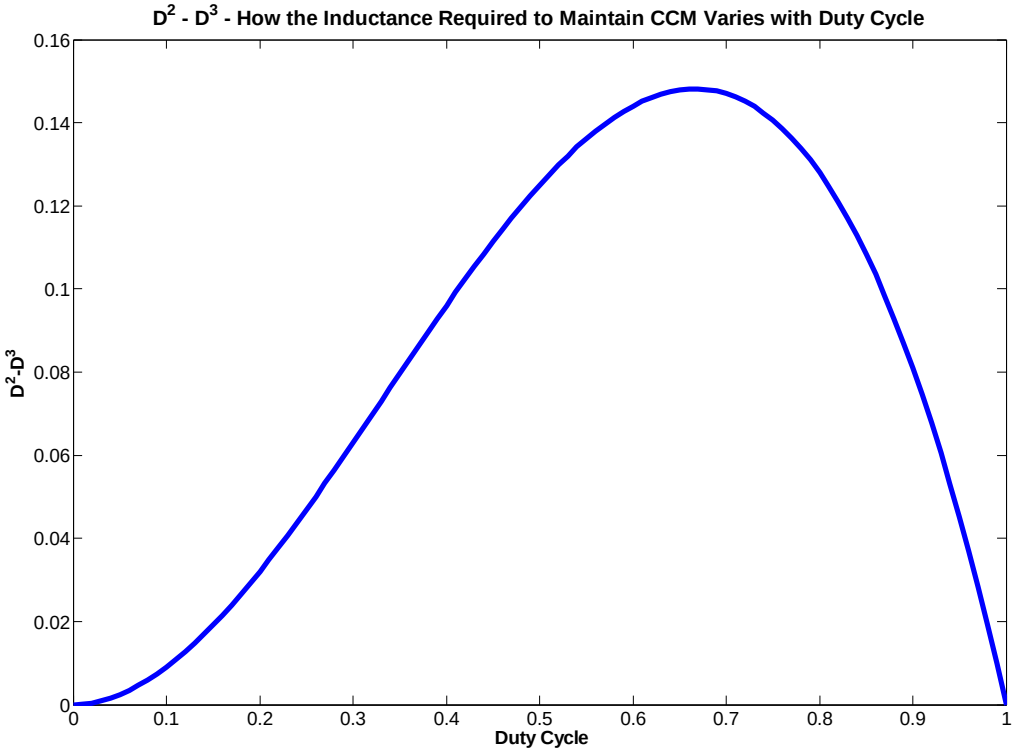


Figure 3.7: Required filter inductance versus duty cycle

Note that for a different forward converter topology, which allows duty cycles greater than 50 %, the minimum inductance requirement is actually at **D = 0.66.** This is possible with active clamp forward converters or forward converters with separate demagnetising windings [4].

3.2.5.3 Filter Inductance Requirements versus the Number of Nodes

The inductance required to maintain CCM in a constant power converter that operates over a wide range has been analysed. This result allows the minimum inductance to be determined for a converter. However, how the inductance required per phase changes when more nodes are added in a multi-node converter still needs to be analysed, as this has significant size and volume implications for the inductor.

This analysis will be done by considering the changing voltage and current requirements for each node when the number of nodes is increased. This is outlined in Table 3.1. The scaling factor shown in the table corresponds to the required rating for each node normalised to the output of the entire converter. Adding nodes decreases the required maximum node voltage and maximum node current. It does not affect the minimum voltage and current ratings.

Table 3.1: Per node current and voltage requirements.

Required Rating (per node)	Scaling Factor	Node Connection	Comment
Maximum voltage rating	$\frac{1}{n}$	Series	When connected in series, the node voltages add. So adding another node means that each node now needs to output a lower voltage to meet the composite converter's specification.
Minimum voltage rating	**1**	Parallel	This rating is determined when the nodes are in parallel. Adding more nodes has no effect on this rating as each node must still be capable of the minimum voltage.
Minimum current rating	**1**	Series	This rating is determined when the nodes are in series. Adding more nodes has no effect on this rating as each node must still be capable of the minimum current while maintaining CCM.
Maximum current rating	$\frac{1}{n}$	Parallel	Current sums when the nodes are connected in parallel, so more nodes mean that each node needs to source less current.

These scaling factors can now be used to predict how the required inductance per phase changes with the addition of more nodes. To guarantee that the inductor remains in CCM throughout the range we must analyse the inductor at its most challenging operating point. From Equation (3.6) or Figure 3.7, this occurs at D = 0.5. At D = 0.5 the nodes are outputting their maximum voltage and minimum current and so we can express the inductance required so that each node remains in the CCM as Equation (3.7).

$$L_{node} = \frac{V_{node,max}}{I_{ripple}}.\Delta t = \frac{V_{node,max}}{2.I_{node,min}}.\Delta t \quad \textbf{(3.7)}$$

From Table 3.1, we can substitute for the maximum node voltage and minimum node current:

$$L_{node} = \frac{1}{n}.\frac{V_{Converter,max}}{2.I_{Converter,min}}.\Delta t \quad \textbf{(3.8)}$$

For n = 1, the equation simplifies to the inductance that is required in a traditional converter or single node converter. We may then state Equation (3.9).

$$L_{node}(n) = \frac{L_{traditional\ Converter}}{n} \quad \textbf{(3.9)}$$

Equation (3.9) can also be predicted from analysing Equation (3.6). When more nodes are added we expect each node's output power and also each secondaries turns ratio to decrease as 1/n. If (P_o) is replaced with (P_o/n) and (N_s/N_p) is replaced with (N_s/n.N_p) then Equation (3.6) becomes Equation (3.10), where L(1, D) is the required inductance in a single node or traditional converter. This equation is in the same form as Equation (3.9).

$$L(n, D) = \left(\frac{v_{DC} N_s}{n.\, N_p}\right)^2 . \frac{(D^2 - D^3)}{2\frac{P_o}{n}} . T_s = \frac{1}{n} . L(1, D) \quad \textbf{(3.10)}$$

Equation (3.9) and (3.10) both show that for each additional node that is added the required inductance per phase decreases. This means that for the same core, fewer turns are required on the inductor. This will affect the inductor's final size and weight. From the two equations, it is also clear that the total inductance, or the sum of the inductances across all the phases, remains constant.

It is also important to remember that although the per phase inductance requirement decreases, an additional inductor is needed for each additional node. This means an additional winding must be added to the coupled inductor. Further analysis is required to determine the size and weight implications due to the additional windings.

3.2.5.4 Inductor Size, Weight and Cost versus the Number of Nodes

How the final inductor's size, weight and cost scales with the number of nodes in a multi-node converter is analysed in this section. This is achieved by analysing the required window area for a multi-node converter's coupled inductor and how this window area varies with the number of nodes.

The required window area can be expressed as Equation (3.11) [4].

$$A_w = \frac{n.\, N.\, A_{cu}}{K_u} \quad \textbf{(3.11)}$$

Where:

- A_w is the total window area required by the windings for a given core.
- K_u is the winding fill factor.
- n is the number of inductors coupled on the core. i.e. n is equal to the number of nodes.
- N is the number of turns for each inductor.
- A_{cu} is the cross sectional area of each wire.

The required window area and how it changes with the number of nodes can be analysed using Equation (3.11). This will be done by analysing each term in the equation separately and then combining them.

By definition, the per phase filter inductance (L_{node}) is the flux linked by the coil (N.Φ) per unit of current that flows in the coil (*i*) [4]. I.e.

$$L_{node} = \frac{N.\Phi}{i}$$

By using relations for reluctance ($\mathcal{R}$) and MMF we can show that the inductance of a coil can be given by [4]:

$$L_{node} = \frac{N^2}{\mathcal{R}}$$

By rearranging terms and using Equation (3.9), we can show Equation (3.12).

$$N = \sqrt{\frac{L_{Traditional\ Converter}.\mathcal{R}}{n}} \quad \textbf{(3.12)}$$

From this equation it is seen that the required number of turns per phase decreases with an increasing numbers of nodes. It is seen to decrease as one over the root of the number of nodes if the core's reluctance is kept constant.

The required conductor area also changes with the number of nodes, as the maximum current each phase is required to supply decreases. If the current density (*J*) in the coils is kept constant, then the required conductor area (A_{cu}) can be expressed as a function of the number of nodes using Equation (3.13)

$$A_{cu} = \frac{I_{out,max}}{n.J} \quad \textbf{(3.13)}$$

Equation (3.14) follows after substituting Equations (3.12) and (3.13) into Equation (3.11). The equation expresses the required window area for a coupled inductor in a multi-node converter as a function of the number of nodes and other quantities.

$$A_w = \frac{1}{K_u}.\left(\frac{\sqrt{L_{Traditional\ Converter}.\mathcal{R}}}{\sqrt{n}}\right).\left(\frac{I_{out,max}.}{J}\right) \quad \textbf{(3.14)}$$

The maximum output current ($I_{out,max}$), the current density in the coils (J) and the inductance that would be required in a traditional converter's filter ($L_{Traditional\ Converter}$) are all constant and come from

or are derived from the converter's specifications. The reluctance ($\mathcal{R}$) is a function of the core and the air-gap in that core, which is considered constant for the next analysis. Equation (3.14) is thus re-written as:

$$A_W = \frac{1}{K_u.\sqrt{n}}.(Const) \quad \textbf{(3.15)}$$

Equation (3.15) predicts that the required window area for a multi-node converter's coupled inductor decreases when more nodes are added if K_u does not decrease faster than $\sqrt{n}$ increases. Whether this is true or not must be analysed by considering the factors that lead to the window area not being fully utilised. K_u is primarily the result of the insulation required between the windings, the small gaps left between windings due to their round shape and because some area is required for a bobbin on most transformers [2] [4]. The literature shows how these factors vary with wire gauge and K_u will be discussed for two different cases: For a small number of nodes and for a large number of nodes.

1. In this discussion, a small number of nodes is defined as less than eight nodes. In this case, the wire gauge that would be used in a multi-node converter is within about six gauges (AWG) of that required in a traditional converter design (from Equation (3.13) for constant J). Tabulated data in the literature predicts that the utilisation factor is unlikely to decrease by more than 15 % for this change in gauge [2]. This value corresponds well with the expected values of K_u given in other literature (0.5 – 0.6 for "practical round conductors") [4]. If this result is used in Equation (3.15) with n = 2..8, then it is clear that the window area required for the multi-node converter will be lower than that required in a traditional converter.
2. For a large number of nodes (>> 8 nodes) the ratio between the insulation and the conductor cross sectional areas will increase [2]. This means that the total window area increases when more nodes are added. The result of this is that for a large numbers of nodes the coupled inductor may be larger in size than the inductor in a traditional converter due to the winding fill factor (K_u) decreasing. Other factors, such as difficulty in working with very fine wire and winding many phases will also start to become a problem if the number of nodes becomes very high.

From this, we can say that the window area required by the windings for a coupled inductor for a multi-node converter with a low number of nodes will be lower than that required in a traditional converter. If the same core is used then the final inductor will be lighter and will require less raw materials (less copper for the windings). Unless the added cost of winding extra phases costs more than the cost of the raw materials that are saved, the final inductor will be cheaper too. Due to less window area being required it may even be possible to use a smaller core than that needed for a traditional design. However this is difficult to predict, since if a smaller core is used then more turns are required to prevent saturation due to the lower core cross sectional area. What can be said is that

in many cases a multi-node converter's inductor will be smaller, lighter and cheaper compared to the inductor required in a single phase traditional converter.

3.2.5.5 Filter Capacitor Requirements

The filter capacitor is specified in conjunction with the filter inductance so that a specified minimum output voltage ripple is attained. By considering the charge transfer between the filter capacitor, the load and the filter inductor over one cycle, the percentage output voltage ripple can be shown to be equal to Equation (3.16) [4]:

$$\%\ Ripple\ Voltage = \frac{\Delta V_o}{V_o}.100\% = \frac{1}{8}.\frac{T_s^2.(1-D)}{L_F.C_F}.100\% \qquad \textbf{(3.16)}$$

Where the equation's terms are as defined in Figure 3.5 and Figure 3.6.

Although this equation neglects the effect that the capacitor's Equivalent Series Resistance (ESR) has on the ripple voltage, it will be used to determine how the required filter capacitance will vary with addition of more nodes.

The capacitor requirements will now be discussed using three criteria: the number of capacitors that are required, their capacitance and their voltage ratings.

- A multi-node converter requires the same number of filter capacitors as it has nodes.
- Equation (3.9) and (3.10) showed that that the filter inductance required in a multi-node converter can be decreased as one over the root of the number of nodes. Combining this fact with Equation (3.16) means that the output capacitance will need to be increased if the same ripple voltage specification must be met. For the same technology, a higher capacitance means that the capacitor is likely to be heavier, larger and more expensive. This can be seen in the datasheet of any large capacitor series (e.g. Panasonic's FC series of electrolytic capacitors).
- The filter capacitors in a multi-node converter require a lower voltage rating than in a traditional converter. The voltage rating is equal to the maximum node output voltage and decreases as one over the number of nodes (see Table 3.1). Lower voltage capacitors are generally smaller for the same technology of capacitor.

Whether the filter capacitance requirements in a multi-node converter are more or less onerous than those in a traditional converter is once again a question of magnitude. Does the higher capacitance requirement mean that the capacitor will be larger even though a smaller voltage rating is needed? Answering this question generally is difficult and it is suggested that this should be considered on a design by design basis. However, it is likely that the total weight, volume and cost of the capacitors in multi-node converters will be higher due to more capacitors being required.

3.2.5.6 Changes of Filter Technology Possible due to the Multi-Node Converter Architecture

In the previous section it was concluded that a multi-node converter's filter capacitor requirements are likely to be more onerous than those in a traditional converter. This conclusion was based on both converters using the same capacitor technology.

This conclusion is not necessarily true since changes in technology may be possible due to the use of a multi-node converter. Since the filter capacitors in a multi-node converter require a lower voltage rating than a traditional design, it is possible that other capacitor types (that are not available at higher voltage ratings) may be used in some multi-node converter implementations. As an example, Panasonic's SP-Cap series of aluminium polymer capacitors have many desirable properties for SMPS designers. They combine high ripple current capabilities (all are above 1 A_{RMS} at 100 kHz), have low ESR (0.11 Ω max, but most are ~0.01 Ω), are surface mount (the largest is 7.3 x 4.3 x 4.3 mm) and are available in the 2.2 µF to 560 µF range. However, the highest available voltage rating is only 16 V, and many of the higher capacitance values are limited to less than 6.3 V. A multi-node converter may allow these capacitors, or ones like them, to be used in a converter that outputs voltages higher than the maximum capacitor voltage provided by the manufacturer.

Such a technology shift won't be possible in all multi-node converter implementations. However, when the converter specifications allow such a shift it could result in the capacitor requirements in a multi-node converter being lower than in a traditional converter design.

3.2.6 Conclusion

The two-switch forward converter topology has been proposed for the implementation of a multi-node converter. Numerous identical secondaries can be added to the converter to produce the multiple nodes required to implement the multi-node architecture. If the nodes are suitably identical, then the output current can be shared passively when the nodes are paralleled. This helps to simplify the design and implementation of the final converter significantly.

How to design the nodes so that their outputs were equal was thus addressed. The literature indicated that the transformer's leakage inductance will play the largest part in degrading cross regulation. For this reason, how the transformer should be wound so that each phase has an equal leakage inductance was investigated. It was concluded that the phases should be wound multi-filar so that each phase's physical distribution within the winding window was as identical as possible. This should result in the leakage inductances for the phases being approximately equal.

The passive filter components in multi-node converters and how their requirements change with the number of nodes was then analysed. It was found that if constant output power was required for a single phase, then the filter inductor should be specified at a duty cycle of 50 %. This is the most challenging operating point for the inductor in the two switch topology. The filter inductance was then

analysed and it was shown that the filter inductance required per phase decreases inversely with the number of nodes. How this affects the final size of the coupled filter inductor was discussed and it was concluded that for small numbers of nodes the coupled inductor in a multi-node converter is expected to be cheaper, smaller and lighter than the inductor in a traditional converter.

The filter capacitors in multi-node converters are expected to be heavier, larger and costlier than in a traditional converter due to more than one being required. This result was based on the assumption that the same capacitor technologies would be used for both traditional converters and multi-node converters. This assumption will not be true in all cases and changes in technology will be possible in many multi-node converter implementations. This can lead to size, weight and cost reductions for the filter capacitors in a multi-node converter compared to a single node or traditional topology.

3.3 Converter Modelling

Once a topology for implementing a multi-node converter had been proposed it was possible to develop models for the converter at the component level. Two models have been developed, one which models a multi-node converter with any number of identical nodes and a second model that only models four node converters, but caters for component tolerances and variations between the nodes. Both of these models are presented in this section and are derived from the circuit shown as Figure 3.1 and repeated as Figure 3.8 for convenience. The models are later used to develop a comparative design for a multi-node converter and a traditional converter. They are also used in later chapters to verify and predict experimental results, such as efficiency and output voltage, performed on a prototype multi-node converter.

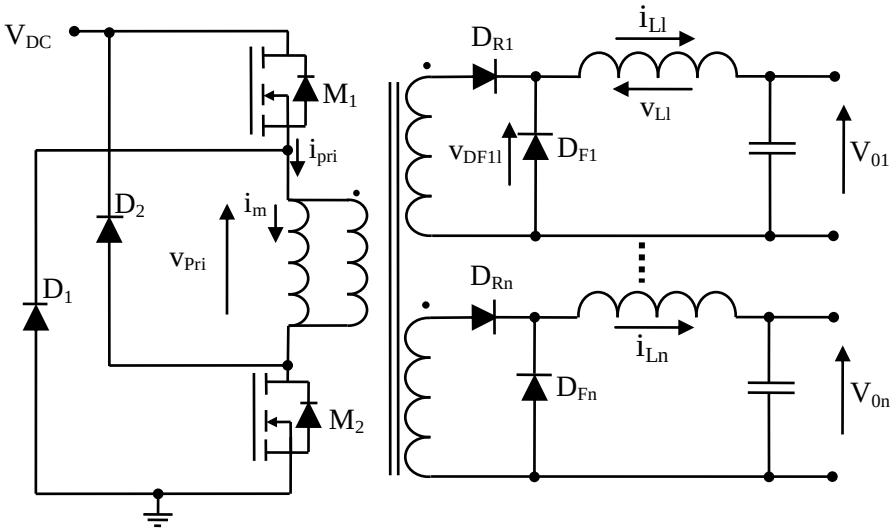


Figure 3.8: The two-switch forward converter with multiple identical secondaries

Before presenting the models it is important to discuss each component in the converter and to show how they have all been modelled. This is shown in the section below. The assumptions that are used when developing the models and also definitions for the parameters within the models are also shown.

3.3.1 Component Models, Assumptions and Losses

This section discusses how each component in the multi-node converter was modelled. Each component type is described in its own section below. The component models are biased toward low powered devices that would be suitable for use in converter with an output power of less than 100 W and a 60 V DC bus. The models may not be valid or accurate under other conditions or power levels. The models have also been simplified as much as possible in the interests of simplifying the final circuit and model. If there are any significant deviations between the experimental work to follow and the model then the assumptions that are made and the component models will be revisited.

3.3.1.1 MOSFET Model

Figure 3.9 shows the MOSFET model that was used when modelling the two primary side MOSFETs in the two-switch forward converter. It consists of an ideal MOSFET, a series on-resistance ($r_{ds(on)}$) and an output capacitance (C_{oss}).

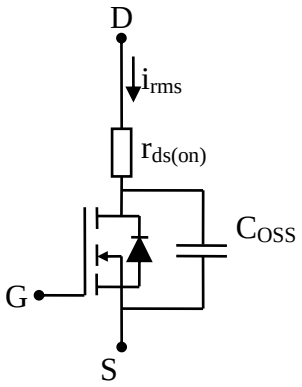


Figure 3.9: MOSFET model with losses

Two types of losses were calculated for the MOSFET: Conduction losses and switching losses.

Conduction losses occur when the MOSFET is conducting and some power is dissipated due to the MOSFET's on-resistance. This conduction loss (P_{Cond}) is calculated using Equation (3.17).

$$P_{Cond} = r_{ds(on)}.{i_{RMS}}^2 \quad \textbf{(3.17)}$$

The current that is used to calculate the conduction losses (i_{RMS}) in the MOSFET is the RMS equivalent of the trapezoidal current that flows in the MOSFET. This current (i_{pri}) is shown in Figure 3.2.

The MOSFET's switching losses consist of three different components: Switching losses due to the MOSFETs' gate charges, due to the MOSFETs' output capacitances and due to the MOSFETs being hard switched [3]. All three of these losses are accounted for in the model. The most significant of the switching losses is due to the MOSFETs being hard switched and this loss is calculated for each MOSFET using Equation (3.18).

$$P_{sw} = V_{DC}.F_s\big((0.5).I_{mos,min}.t_{on} + (0.5).I_{mos,max}.t_{off}\big) \quad \textbf{(3.18)}$$

Where:

- P_{sw} is the loss hard switching causes in the two MOSFETs.
- V_{DC} is the converter's DC Bus voltage.
- F_S is the converter's switching frequency.
- $I_{pri,max}$ and $I_{pri,min}$ are the minimum and maximum of the trapezoidal current that flows in the MOSFETs and transformer primary.
- t_{on} and t_{off} are the times taken to switch the MOSFET.

3.3.1.2 Diode Model

The diode model consists of an ideal diode with a forward voltage drop (v_d). No series resistance was included in the model since this loss was considered insignificant compared to the loss due to the forward voltage drop. This may not be true at high current levels, where a real diode's resistance may be significant [4]. Since the resistive component is neglected, the total diode losses are equal to the product of the average current that flows in the diode and the diode's forward voltage.

Reverse recovery is also not considered in the model as Schottky diodes are assumed. These diodes are suitable at the voltage and power level and do not suffer from reverse recovery.

3.3.1.3 Inductor Model

The converter's filter inductor was modelled as shown in Figure 3.10. The model consists of a series resistance, the filter inductance and a core loss resistance connected in parallel with the inductance. The series resistance consists of only the DC resistance of the coil. The AC resistance due to the skin, proximity or other stray effects is not accounted for. Neglecting these effects may mean that the inductor's resistance is optimistically low, but this is discussed further when the experimental and theoretical results are compared in Chapter 5.

The inductor current consists of a DC component with a triangular AC component superimposed on it (see i_{L1} in Figure 3.2). This AC current component means that the core flux has an AC component and results in core losses. This can be modelled by the core loss resistor (r_{core}) shown in the figure. The value of this resistor can be estimated from the core manufacturer's datasheet, but it was decided that

this approach would not be used in the model in the interests of simplifying the circuit for analysis. The core losses are instead estimated from the manufacturer's datasheets and included as a constant core loss in the converter model. The losses in the inductor are thus equal to the sum of the conduction losses (calculated from the RMS inductor current) and the constant core losses. r_{core} is then not considered when analysing the model.

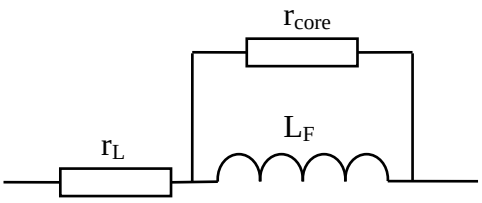


Figure 3.10: Inductor model

3.3.1.4 Transformer Model

The converter's transformer was modelled as shown in Figure 3.11. The model consists of an ideal transformer, a magnetising inductance, a winding resistance and a core loss resistance. The winding resistance consists of the combination of the primary side winding resistance and the secondary side resistances referred to the primary side. Similarly to the inductor, the DC resistance of these windings is used and the skin effect, proximity effect and any other stray effects are not accounted for.

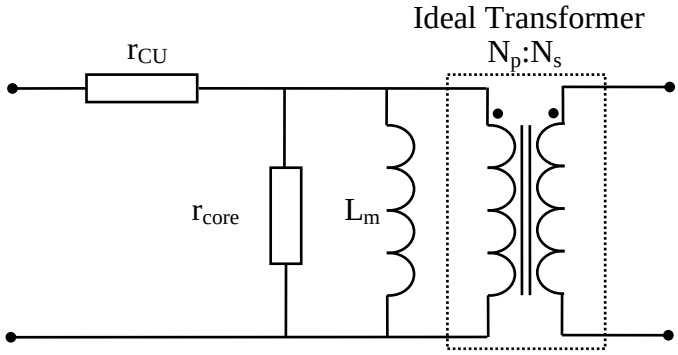


Figure 3.11: Transformer model

The transformer's core losses were accounted for in the same way as the inductor's core losses. i.e. r_{core} is neglected from the transformer model. The transformer's losses are also equal to the sum of the conduction losses (calculated from the primaries RMS current) and a constant core loss.

The leakage inductance has not been included in the model and so it will not be considered in the final converter model. This simplifies the model's derivation and it is expected that neglecting the leakage inductance will not affect the model's output significantly if the leakage inductances are all similar.

3.3.1.5 Capacitor Model

The filter capacitor has been modelled as an ideal capacitor in series with the capacitor's specified Equivalent Series Resistance (ESR) at the switching frequency. The losses in the filter capacitors are likely to be small, but they can be calculated from the RMS inductor ripple current and the ESR of the capacitor. Since the losses in the filter capacitors are likely to be small they are not considered by the model, however the ripple voltage caused by the capacitor's ESR is accounted for.

3.3.1.6 Modelling the Effect of Stray and other Resistances in the Converter

Other resistances within the circuit can also have an effect on the output. The two main resistances that are considered are the power train resistance and the output resistance for each node. The origin of these resistances and their location are shown schematically in Figure 3.12.

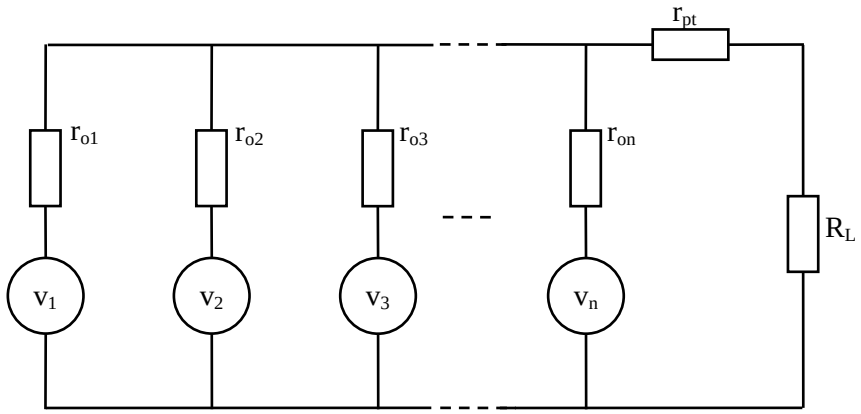


Figure 3.12: Origin and position of the power-train and output resistances in the multi-node converter model

The power train resistance (r_{pt}) is the small stray resistance in the leads between where the nodal output's are combined and where the actual load is connected. This resistance can result in some efficiency losses if r_{pt} is not insignificant compared to the load resistance. The second model caters for this small loss by modelling it as a simple resistor is series with the load.

Each node's output resistance (r_{o1} to r_{on}) is any resistance between a node's output and where is it combined with the next node. This resistance can consist of the resistance of any switch used to connect the nodes, any current sense resistor connected in series with the nodal output and also any stray resistances in the path. The losses caused by this resistance are included in the model as a current sense resistor is used to measure the output current from each node in the prototype developed in Chapter 4.

3.3.2 Parameter Definitions

The terms that will be used when developing and presenting the model have all already been defined in this chapter. However, for clarity and convenience, they are redefined in Table 3.2.

Table 3.2: Parameter definitions for the two models

Parameter	Reference	Description
D		The converter's duty cycle.
n		The number of nodes in the converter.
N_s and N_p	Figure 3.11	The number of primary and secondary side turns.
r_{cu}	Figure 3.11	The transformer's winding resistance referred to the primary.
$r_{ds(on)}$	Figure 3.9	The on-resistance of each primary side MOSFET.
r_L	Figure 3.10	The inductor's resistance.
R_L		The resistance of the converter's load.
v_d	Section 3.3.1.2	The rectifying diode's forward voltage drop.
V_{DC}	Figure 3.8	The DC bus voltage.
v_{on}	Figure 3.8	The output voltage for the n'th node.

In the second model, the nodes are not assumed to be identical. In this case, some parameters may be different for different nodes and the parameter is also subscripted with the number of the node. For example, r_{L1} and N_{s4} refer to the inductor resistance in phase one and the number of turns on phase four's transformer secondary.

3.3.3 Model One: Any Number of Identical Nodes

Now that each component within the converter has been described, it is possible to model the entire converter by analysing the circuit shown as Figure 3.8 (with each component replaced by its component model). The first model was developed with the number of nodes as a parameter that is specified before runtime. This section describes the model, how it was developed and with what assumptions.

3.3.3.1 Assumptions

Certain assumptions were made when developing the first theoretical model. In addition to the component model assumptions already mentioned, the following assumptions are made by the first model:

- Identical nodes are assumed. This means that the effect of component variation in the converters is not included.
- The power required by the control system for the converters has been neglected.
- The effect of power train resistance is not included.

3.3.3.2 Derivation of the Model and the Output Voltage Expression

The first model was developed using basic circuit analysis techniques (KVL and KCL) and criteria for operation at steady state (Inductor volt-second balance). The final output expression for a single secondary is given as Equation (3.19).

$$V_o(D, R_L) = \frac{D.\frac{N_s}{N_p}V_{DC} - D.V_d}{n.D.\left(\frac{N_s}{N_p}\right)^2.\left(2\frac{r_{ds(on)}}{R_L} + \frac{r_{cu}}{R_L}\right) + \frac{r_L}{R_L} + 1} \quad \textbf{(3.19)}$$

This equation is difficult to apply as it depends on the output resistance (R_L) which is unknown and is actually dependant on the output voltage. In other words the load resistance is actually a function of the output voltage. The load resistance should be chosen such that each secondary outputs constant output power (P_o). In other words:

$$R_L(V_o) = \frac{{V_o}^2}{P_o} \quad \textbf{(3.20)}$$

If we substitute Equation (3.20) into Equation (3.19) then we can use the quadratic formula to solve for each node's output voltage in terms of the node's constant output power (P_o), duty cycle (D) and other known quantities. This is shown as Equation (3.21):

$$v_o = \frac{\left(v_{DC}.\frac{N_s}{N_p}.D - v_d\right) \pm \sqrt{(v_{DC}.\frac{N_s}{N_p}.D - v_d)^2 - 4\left(n.D.P_o\left(\frac{N_s}{N_p}\right)^2.(2.r_{ds(on)} + r_{cu}) + P_o.r_L\right)}}{2} \quad \textbf{(3.21)}$$

Equation (3.21) can be used to determine the output of a node and it forms the core of this theoretical model. The equation gives two results, one due to the addition of the root and one due to the subtraction. Which is the correct result needs to be determined. This can be done by considering a node's output in the ideal case. In an ideal converter v_d, $r_{ds(on)}$, r_{cu} and r_L are all zero and Equation (3.21) simplifies to:

$$v_o = \frac{\left(v_{DC}.\frac{N_s}{N_p}.D\right) \pm \left(v_{DC}.\frac{N_s}{N_p}.D\right)}{2} \quad \textbf{(3.22)}$$

If we consider the addition and the subtraction of the second term we can see that the subtraction results in an output of zero while the addition correctly predicts the theoretical output voltage given by Equation (3.2). The addition term is therefore used in the model.

Once the output current and voltage for each node is known, it is relatively trivial to determine the average or RMS current through each component in the converter. The primary side currents can also be calculated since the number of nodes is known (the number of nodes is specified before runtime). This allows the losses in each component to be easily calculated. The model was then implemented in Matlab. The model is capable of determining the output of any number of identical nodes. It can

produce curves showing the output of each node (voltage and current) in terms of duty cycle. Curves showing the losses in each component in the converter versus the each node's output are also possible and this means that efficiency can also be plotted over the output range. This model will be verified using the second model and finally using experimental data.

The models will be used extensively in a comparison between a traditional converter design and a multi-node converter that follows in Section 3.4. The commented code listing for the first model is included in Appendix C.

3.3.4 Model Two: Four Non-Identical Nodes

The second model is limited in the fact that it can only model four node converters. However it is also more flexible than the previous model since it does not require the nodes to be identical. The second model allows each parameter (for example, the turns ratio, diode forward voltage drop, inductor resistance etc.) in each node to be individually varied. This allows the effects of non-ideal current sharing to be modelled. The derivation of this model is now discussed. Figure 3.8 and Section 3.3.1 are relevant to this discussion.

3.3.4.1 Assumptions

The second theoretical model has the same assumptions as the first model. The only differences are that identical nodes are no longer assumed and that the power train resistance's effects are included.

3.3.4.2 Derivation of the Model

The previous model was primarily based on Equation (3.21). This equation predicts the output voltage for a node given a certain duty cycle and output power. This equation was key to developing the model and once it had been derived the other required quantities for predicting the converter's performance (RMS inductor currents, average diode current etc.) and losses could be easily calculated. This approach was initially tried for the second model; however the complexity of the model became prohibitive. More than 22 terms (four diode voltage drops, four inductor resistances, four turns ratios, four output resistances, the DC bus voltage etc.) are required to predict the output voltages for the nodes. This makes it cumbersome to determine an equation similar to Equation (3.21) for the second model.

For this reason a matrix approach for solving simultaneous equations describing the converter was chosen. In defining the converter's operation there are nine unknowns that must be solved for, namely the output voltage and current for each node (four each for a total of eight unknowns) and then either the total output current or voltage (if the load resistance is known then knowing either the load current or voltage is equivalent). Depending on the connection of the nodes, the number of unknowns reduces to either five (for series or parallel connected nodes) or seven (for series/parallel connected nodes).

This occurs since some of the unknowns become equal (for example, for serially connected nodes the output current and all of the node currents are the same). The unknowns in each configuration are shown in Table 3.3. Due to the unknowns changing it was decided that a model for the circuit would be developed for each configuration (series, parallel and series/parallel). In other words, three models will be developed so that the circuit can be modelled in all three configurations.

Table 3.3: Unknowns for each circuit configuration

Configuration	Number of Unknowns	Unknown	Symbol	Description
Series	5	1,2,3,4	v_{o1}, v_{o2}, v_{o2}, v_{o2}	The output voltage for each node
		5	i_o	The output current (equal to each node's current)
Parallel	5	1,2,3,4	i_{o1}, i_{o2}, i_{o3}, i_{o4}	The output current for each node
		5	i_o	The total output current
Series/Parallel	7	1,2,3,4	v_{o1}, v_{o2}, v_{o2}, v_{o2}	The output voltage for each node
		5	i_{o1}	The output current for node 1 and 2 (Equal since node 1 and 2 are serially connected)
		6	i_{o3}	The output current for node 3 and 4 (equal since node 3 and 4 are serially connected.)
		7	i_o	The total output current

To uniquely solve for a given number of unknowns simultaneously we need the same number of equations as we have unknowns. We thus need to develop either five or seven independent or non-trivial equations describing the unknowns shown in Table 3.3. Once these equations have been derived in terms of the circuit parameters (inductor resistance, diode forward voltage, turns ratio etc.), matrix methods can be used to solve for the unknowns. This means that the output voltage and current for each and every node will be known.

Applying the inductor volt-second balance principle (i.e. the average voltage applied to each inductor each cycle is zero in the steady state) on each phase's inductor yields four simultaneous equations for each configuration [3]. We thus have four equations for each circuit configuration and only need to derive one more equation for the parallel and series configurations and three equations for the series/parallel configuration. These additional equations are developed using KVL and KCL in the output loop and where the nodes are combined.

As an example, Equation (3.23) and (3.24) show the five simultaneous equations used to describe the converter when the nodes are connected in series. Equation (3.23) is repeated for each node where N_{sn}, v_{dn}, and v_{on} are replaced with the respective parameters for each of the four phases. This is not a trivial equation since the circuit parameters in each phase may be different. The simultaneous equations for the other converter configurations are similarly derived.

$$D.V_{DC}.\frac{N_{sm}}{N_p} - v_{dm} = v_{on} + \frac{N_{sm}}{N_p}.D.\left(2.r_{ds(on)} + r_{cu}\right).\left(\frac{N_{s1}}{N_p} + \frac{N_{s2}}{N_p} + \frac{N_{s3}}{N_p} + \frac{N_{s4}}{N_p}\right).i_o \quad \textbf{(3.23)}$$

m = 1,2,3,4

$$0 = v_{o1} + v_{o2} + v_{o3} + v_{o4} - i_o\left(R_L + r_{o1} + r_{o2} + r_{o3} + r_{o4} + r_{pt}\right) \quad \textbf{(3.24)}$$

In the equations, v_{o1} to v_{o4} and i_o are unknown and must be solved for. The other quantities are all known or are specified. The simultaneous equations for the series configuration (Equation (3.23) and (3.24)) are then written in matrix form as:

$$A = B.X \quad \textbf{(3.25)}$$

Where:

- A is a k x 1 matrix (k is equal to the number of unknowns or equations and is equal to five for the series configuration) consisting of terms that are not multiplied with any of the unknowns (the left hand side terms in Equation (3.23)).
- B is a k x k matrix consisting of terms that contain unknowns (the right hand side terms in Equation (3.23) and (3.24)).
- X is a k x 1 matrix containing the unknowns. This definition is consistent with Table 3.3.

All of the unknowns can then be solved for by using matrix inversion and multiplication as shown in Equation (3.26).

$$X = B^{-1}.A \quad \textbf{(3.26)}$$

The simultaneous equations for the parallel and series/parallel configurations are then solved in the same manner. This means that each node's output voltage and current is then known for all of the configurations for a given duty cycle and load resistance. The total output current is also known and the output voltage for the entire converter can be solved for by multiplying the output current by the load resistance. The same techniques used in the previous model can now be used to determine the parameters required to calculate the losses in the converter. For example, if the output voltage, output current and filter inductance for a node are known, then the ripple current in the filter inductor can be determined. This means that the inductor's RMS current and its conduction losses can be calculated.

3.3.4.3 Output Expression for Constant Output Power

In the previous model, Equation (3.20) was used to substitute for the load resistance in Equation (3.19) and this resulted in a quadratic solution for the output voltage (Equation (3.21)). This closed form solution allowed the output voltage and current to be predicted for a converter with a given duty

cycle and output power. It also meant that the converter's output could be plotted versus duty cycle for a constant output power without the required load resistance being known. However, this approach is not as trivial in the second model; as if we substitute for the load resistance then the simultaneous equations that result are no longer linear. Solving numerous, non-linear, simultaneous equations is difficult and so another approach was sought.

This approach involved estimating the load resistance and then calculating the output current and voltage (and hence the output power). Since constant power is desired the load resistance is then adjusted and the output is recalculated. This procedure is repeated until the correct load resistance (the one that results in the desired output power) has been found. The duty cycle is then modified and the above is repeated for each new duty cycle until the entire output range has been spanned. This allowed output curves to be plotted against duty cycle for constant output power even though the required load resistance is not known in advance.

The second models source code is included in Appendix C.

3.3.5 Model Comparison

The two models were compared by simulating the same converter and checking to see whether the outputs were consistent. For this to be valid, the different assumptions made by the two models needed to be considered. For this reason two converters, with four identical nodes and no power train resistance were simulated. The two models correspond in terms of output and component losses (and thus by efficiency too). Ensuring that the two different models, which were derived differently, are consistent was a useful step in validating the models. The two models will now be used interchangeably, depending on the converter being simulated and which factors need to be taken into account.

3.3.6 Conclusion

Two Matlab models have been developed for simulating the operation of multi-node converters. The two models have different assumptions and capabilities.

The first model allows any number of nodes to be simulated but assumes that they are all identical. The effects of mismatched currents between the phases and power train resistance cannot be simulated. The derivation of this model was presented and it is primarily based on a closed form solution for the output voltage of a node given the output power and other circuit parameters.

The second model was then presented. This model only allows converters with four nodes to be modelled but it does allow each phase to have different parameters. It can therefore model the effect of unequal current sharing between the phases. This model was derived differently to the first model

in that no closed form solution for the output was determined due to the prohibitive number of terms involved. For this reason a matrix solution was used.

The models were then compared by using both models to simulate a converter with the same parameters. The effect of the different assumptions made in the two converters was negated by simulating a converter with four identical nodes and no power train resistance. It was found that the two models were consistent and did correspond in terms of both the output of the converter and also the losses in its components. This imbued more confidence in both models and so they are used to evaluate the performance of two converters as part of a comparative design example. This comparative design example is presented next.

The models will also be compared to experimental results on a prototype converter. This converter's implementation and the testing of each individual section of the converter are described in Chapter 4. The testing of the converter as a whole is presented in Chapter 5.

3.4 Comparative Design Example

This section describes the design and specification of a four node multi-node converter and a traditional converter with the same specifications. The specifications for the converters are shown in Table 3.4. This section is not meant to be a general analysis of the differences in the design and specification of traditional converters versus multi-node converters. It is simply an illustrative example showing how the component requirements change for a given converter specification when a multi-node converter is used.

Table 3.4: Converter specifications

Constant Output Power	30 W
Output Voltage Range	6 V to 48 V (an 8 times range)
Switching Frequency	50 kHz
Input Voltage	60 V
Output Voltage Ripple	2 % maximum
CCM/DCM?	CCM

Throughout this section the components required in the two converter designs will be compared in terms of their specifications, their weight and size. What is interesting in this section is how the components and the technologies that are used to implement them are different in the two designs despite the identical converter outputs. Once the components have been specified the losses present in each component will be calculated using the converter models that have already been developed.

The losses present in each component and how they differ in the two converters can then be discussed. This is an interesting topic for analysis since how the losses vary over the output range determines how effectively any hardware used to cool the components is utilised. The total losses in the converters will then be used to compare the expected efficiency in both converters.

However, before the component selection for the two converters is shown a note on how the magnetic components were designed is given. This is because these components were designed specifically for the converter and were not selected off the shelf like the other components.

3.4.1 Magnetics Design Procedures

The transformers and inductors within the two converters were designed using an iterative procedure on a spread sheet. A basic overview of the procedure followed for designing the magnetic components is outlined in this section. The spreadsheets used to design the magnetic components are included in Appendix C.

3.4.1.1 Transformer Design Procedure

The transformer's turns ratio was first determined using the maximum possible duty cycle (50 %), the maximum output voltage (including the diode forward voltage drops and a margin for safety) and the DC bus voltage (using Equation (3.2)).

Once the turns ratio was known, an E-core was chosen for the transformer. The size of the core was initially chosen as a best or educated guess and a material suitable for the application and frequency was chosen. The minimum number of primary side turns required to limit the core's flux density to an acceptable level (dependant on the allowable specific power loss in the core or on the saturation flux density) was then calculated. The turns ratio can then used to calculate the number of secondary turns.

The maximum current that the transformer is expected to carry is used to select the wire gauges for the primary and secondary windings. This calculation was based on recommended current densities in the literature (2 – 5 A/mm^2 or 400 – 1000 circular mills per ampere [5]). The conductor's skin depth is also considered and the wire diameter should be kept below twice the skin depth (0.29 mm at 50 kHz for copper [2]) to prevent excessive conduction losses due to the Skin effect [4]. If the required conductor's radius is thicker than this then the winding should be composed of multiple strands of wire with a radius smaller than the skin depth. For this reason the thickest wire used in the comparative designs will be AWG 22.

The required window area can then be calculated using the area of each strand of wire, the number of strands, the number of turns, and an utilisation factor of 0.4 [2]. The required window area was then compared with that available in the chosen core. If the window area was large enough to contain the windings then the next smallest core was checked, until the smallest possible core had been found. If the required window area was larger than that available, a larger core was tried.

This process was repeated iteratively on a spread sheet until the smallest core capable of containing the windings had been found. This core was then used in the final design.

3.4.1.2 Inductor Design Procedure

The inductor used in the converter designs was specified in terms of its current carrying capacity, the number of phases coupled onto the same core and the required phase inductance. The number of turns required to meet the inductance specifications was calculated by considering the cores reluctance. It can be shown that the inductance is given by Equation (3.27) [4]:

$$L = \frac{N^2}{\mathcal{R}_{core}} \tag{3.27}$$

Since the core is gapped, the core's reluctance ($\mathcal{R}_{\text{core}}$) is approximated by the reluctance of only the air-gap. For small gaps, this will result in the inductor having an inductance lower than specification. Adding a few extra turns on the inductor to compensate for this may be required.

The number of turns required by each inductor on a particular core (the first core that is tried is chosen using an educated guess) was then solved with the air-gap's reluctance replacing $\mathcal{R}_{\text{core}}$. The thickness of the wires is then calculated using a current density dependant on whether the designer wishes to optimise the design for low conduction losses or small size. A value of 4 A/mm^2 was chosen for the two designs that are compared in this analysis. The required window area is then calculated using the number of turns, the number of phases, the wire thicknesses and an utilisation factor. Larger or smaller cores can then be tried until the smallest suitable core has been found.

3.4.2 Component Selection and Specification

This section documents the components that are used in the two converters that are being compared. Some of the components have been selected off the shelf while others (the magnetic components) have been designed to specification. Each component type is presented in its own section so that the differences between the components for the two converters are apparent. A short discussion on the differing component requirements for each converter is also given.

3.4.2.1 Primary Side Power Switch Selection

Table 3.5 shows the required primary side MOSFET specifications for the two converter designs. Both converters require 100 V devices that are rated according to the DC bus voltage plus a margin for safety.

Table 3.5: Required primary side MOSFETs

	Multi-Node Design	**Single Node Design**
Voltage Rating	100 V	100 V
Current Rating	1.3 A_{RMS} – 3 A_{Peak}	2.25 A_{RMS} – 10 A peak

The traditional converter's MOSFET requires a higher current rating than multi-node converter's MOSFET. This is because the traditional converter's MOSFET is forced to operate at a lower duty cycle while still delivering the same power. This results in higher peak currents flowing in the MOSFET and also a higher RMS equivalent for that current. IRF6644 MOSFETs were chosen for both converter designs. The IRF6644 is a 100 V, 10 A MOSFET with a drain-source resistance of 10 mΩ. It is recommended for use as a primary side MOSFET in isolated converters and also for synchronous rectification.

3.4.2.2 Transformer Specification

The characteristics for the transformers in the two converters are shown in Table 3.6. The traditional design requires higher current windings for the same reason it requires higher current MOSFETs. This results in thicker windings being needed on the traditional design's primary side and ultimately a larger core being required.

Table 3.6: Transformer characteristics for the two designs

	Multi-Node Design	**Single Node Design**
Core	E 30/15/7 (EPCOS N87)	E 34/14/9 (EPCOS N87)
Primary turns	40 turns (AWG 22)	30 turns (two strands of AWG 22)
Secondary turns	19 turns each (AWG 25)	50 turns (two strands of AWG 24)
Primary Current Rating	1.20 A_{RMS}	2.25 A_{RMS}
Mass (Excluding the Bobbin[1])	36.8 g (22 g core and 14.8 g windings)	52.2 g (28 g core and 24.2 g windings)
Predicted Window Utilisation (With a copper fill factor of 0.4)	91.88 %	90.87 %

The multi-node converter requires more primary turns than the traditional converter design. This is because the E30 core has a lower cross sectional area than the E34 core used in the traditional design. This means that for the same total flux, the flux density in the E30 will be higher. More turns are therefore required to limit the flux density in the E30 core to an acceptable level. This prevents excessive core losses and saturation. The turns ratios for the two transformers are also very different since the multi-node converter requires secondaries with much lower output voltages.

3.4.2.3 Filter Inductor Specification

The filter inductors for the converters are detailed in Table 3.7 below. The multi-node converter utilises a coupled inductor which means that only one core is required to implement all of its inductors.

The filter inductance was determined using Equation (3.6) and it was found that 150 µH and 600 µH inductors were required for the multi-node and traditional converters respectively. These inductances are specified for an output power of 30 W and if the output power decreases then CCM can no longer

[1] The mass of the bobbins are not specified by the manufacturer and so they have not been included.

be guaranteed. For this reason it was decided that both of the inductances would be tripled so that the converter is able to operate at lower power. The converter will thus remain in the CCM over the entire output range for output powers as low as 10 W.

Table 3.7: Filter inductor requirements

	Multi-Node Design	**Single Node Design**
Core	E30/15/7 (EPCOS N87)	E36/18/11 (EPCOS N87)
Required Inductance	450 μH per phase	1.8 mH
Number of Turns	25 Each (AWG 22)	35 (Four stands of AWG 22)
Required Current Capabilities	1.25 A per secondary	5 A
Air-gap	100 μm	100 μm
Total Mass (Excluding the Bobbin[1])	38.3 g (22 g core and 16.3 g windings)	79 g (50 g core and 29 g windings)
Predicted Window Utilisation (With a copper fill factor of 0.4)	101 % (The core is very slightly too small, but K_u = 0.4 is likely to be conservative)	89.25 %

The coupled inductor in the multi-node converter is significantly smaller and lighter than the traditional converter's inductor. This was predicted by the analysis in Section 3.2.5.4. Not only has the required window area been reduced, but a smaller core can also be used.

However, both filter inductors are large given the power output of only 30 W. There are three main reasons for this:

- A high filter inductance is required to maintain CCM. By rearranging Equation (3.5), increasing the output voltage or decreasing the output current in a forward converter where CCM is required means that the filter inductance must be increased. Due to the constant output power requirement, the operating point where the output voltage is a maximum also has the lowest output current. This results in the large filter inductance being required and means that many turns are needed to meet the specification. In this situation, operation in the Discontinuous Conduction Mode (DCM) where a smaller filter inductance could be used may be preferable (however a larger filter capacitor will be required to meet the ripple voltage specification).
- The filter is simultaneously specified for maximum filter current and inductance. Due to the topology the filter inductor's requirements (current carrying capacity and inductance) change significantly depending on the converter's output (similarly to the Buck converter discussed in Chapter 1, Section 1.3.1). Thus, to ensure correct operation of the converter, the filter inductor must be specified simultaneously for maximum current and inductance. This means that the size of the filter inductor increases due to the converter's wide output range. The multi-node converter is able to utilise its filter inductor better and this is the reason why its filter inductor is smaller than the traditional converter.

- The 50 kHz switching frequency. The converter's switching frequency is low given the switching performance of modern power MOSFETs. Modern switching converters with much higher switching frequencies are not uncommon [10]. From Equation (3.6), increasing the switching frequency means that a lower filter inductance is required to maintain CCM. This means that if the switching frequency had been increased, then the final inductor would have been smaller.

3.4.2.4 Filter Capacitor Selection

The filter capacitors for the converters were initially sized for a ripple voltage of 2 % using Equation (3.16). This result of this calculation was 4.33 µF and 1.31 µF for the multi-node and traditional converters respectively. These small capacitances are a direct result of the large filter inductors that were used to guarantee CCM. The filter inductors limit the ripple current seen by the capacitor to a low level and mean that only a small capacitance is required to smooth the output voltage.

After considering available capacitors, the capacitors shown in Table 3.8 were selected. Two different capacitor choices (one electrolytic and the other aluminium polymer) are shown for the multi-node converter. All three capacitors have higher capacitances than predicted by Equation (3.16). When capacitors with the predicted capacitance were considered it was found that the ESR of the capacitor was too high to meet the 2 % ripple voltage specification. For this reason the capacitance of the filter capacitors was increased until a suitably low ESR capacitor was available.

Table 3.8: Filter capacitor selection

	Multi-node Design (Aluminium Polymer)	**Multi-Node Design (Electrolytic)**	**Single Node Design (Electrolytic)**
Capacitor	Panasonic EEFCD1C8R2R	Panasonic EEUFM1C680	Panasonic EEUFC1J220
Capacitance	6.8 µF	68 µF	22 µF
Voltage Rating	16 V	16 V	63 V
Ripple Current Rating (at 100 kHz and 105°C)	1 A_{RMS}	280 mA_{RMS}	240 mA_{RMS}
R_{ESR} (at 100 kHz and 20°C)	0.07 Ω	0.3 Ω	1 Ω
Case Size	7.3 x 4.3 x 1.8 mm (SMT)	5 x 11 mm (ø x L)	6.3 x 11.2 mm (ø x L)

The aluminium polymer capacitor shown in the table is a change in technology that has been enabled by the multi-node converter topology. The aluminium polymer capacitor is from Panasonic's SP-Cap range and has a very high ripple current capability due to its low ESR. However, these capacitors are only available at voltage ratings less than 16 V. Due to this they cannot be used in the traditional converter design where a 63 V capacitor is required. The use of aluminium polymer capacitors allows the filter capacitors for the multi-node converter to be smaller and lighter than the capacitor required in the traditional converter. The capacitors are also surface mount and this is likely to simplify manufacturing due to automation. However there is a financial cost to be paid as these capacitors are currently ten times the cost of the traditional converter's capacitor.

Due to the cost of the aluminium polymer capacitors, an electrolytic capacitor choice is also shown for the multi-node converter. This 16 V capacitor is approximately the same size as the one required in the traditional converter. Due to four of them being required, we can say that the capacitors required in the multi-node converter are likely to be larger and heavier than the traditional converter's single filter capacitor if the same capacitor technology is used in both converters. This is expected from Section 3.2.5.5 and 3.2.5.6.

3.4.2.5 Rectifying Diode Selection

Both converters operate at voltage and power levels that allow Schottky diodes to be used for the rectifiers. This is beneficial due to Schottky diodes having a generally lower forward voltage drop. Reverse recovery is also not a concern with Schottky diodes. Table 3.9 shows the diodes that were selected in the two converters.

Table 3.9: Rectifying diode selection

	Multi-Node Design	Single Node Design
Diode	31BQ06- International Rectifier	20CTQ150 – International Rectifier
Voltage Rating	60 V	150 V
Current Rating	3 A	10 A per leg
Forward Voltage	0.4 V	0.6 V
Package	SMT (7 x 6 mm)	TO-220
Devices per package	1	2

Both rectifiers are manufactured by International Rectifier and their ratings are different due to the topology changes. One factor that is apparent is that the traditional converter's rectifiers have a higher forward voltage. This will have an effect on the efficiency of the converter, but it is reasonable considering that the traditional converter's rectifiers need to block a higher voltage.

3.4.2.6 Control System Specifications

The control system for the traditional converter would make use of a simple, off the shelf, IC controller. When combined with feedback and compensated correctly this would provide reliable, robust and accurate control of the converter.

The control system for the multi-node converter is quite different. It can be implemented in two ways: Where the nodes can be switched into different series parallel combinations in real time or where the configuration is manually changed (this is discussed in Section 2.2.4). This choice has large implications for the flexibility of the converter, how easily the output can be changed and also the complexity and losses associated with the control system.

If the converter is simply hardwired into a specific topology then the control system would also make use of a simple IC controller. This would be an almost identical implementation as in a traditional converter.

If the multi-node converter is to change its configuration in real time then a more complicated controller would be required. How to control numerous series or parallel connected converters has been addressed in the literature [11]. However, the controller would also require a means to change how the nodal outputs are combined and logic to allow it to determine the correct secondary side configuration. Such a controller could be implemented using a microcontroller (e.g. Microchip's PIC16 series of microcontrollers). This would allow a reliable controller to be developed, but it would be more costly, larger and heavier than a standard controller implementation. At lower power levels, this means that the control system may negate many of the size and weight advantages held by multi-node converters. This would need to be carefully considered design-by-design.

3.4.3 Theoretical Performance Analysis

3.4.3.1 Output Voltage versus Duty Cycle

Figure 3.13 shows the output voltage for the multi-node and traditional converters plotted against duty cycle. The effect of a change in configuration on the multi-node converter's output is evident from the horizontal sections of the multi-node converter's curve. These horizontal sections are not areas of operation but only show a topology transition. The upward sloping section of the voltage curves is expected from Equation (3.2), which shows that the output voltage for the converter varies linearly with the duty cycle in the ideal case.

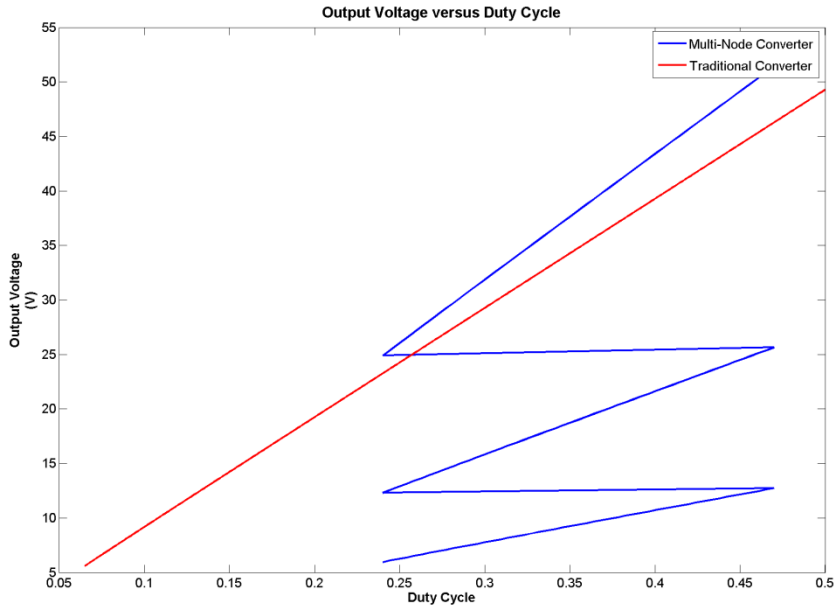


Figure 3.13: Output voltage versus duty cycle.

Both converters are able to meet the output range specifications that were given in Table 3.4, but it is clear that the multi-node converter's duty cycle varies over a smaller range than the traditional converter. In order to achieve a wide output range the traditional converter is forced to operate at very low duty cycles (less than 10 %). The minimum controllable on time for the primary side MOSFETs

eventually limits this range and may even limit the possible switching frequency in a converter where a very wide output range is required [12].

3.4.3.2 Individual Component Losses

The losses experienced by the power components in both converters have been predicted and are shown as Figure 3.14. The effect of a change in topology is clearly visible in the multi-node converter's curves and this appears as a discontinuity. The loss curves for the multi-node converter also repeat for the three different configurations as the losses in the multi-node converter are dependent on each node's output and not directly on the output of the converter.

It is also clear that there is some overlap in the multi-node design's output current curve. This means that the converter is able to produce the same output current using two different nodal configurations. This is required in a practical implementation of the converter. Each of the loss curves is discussed in more detail in the sections below.

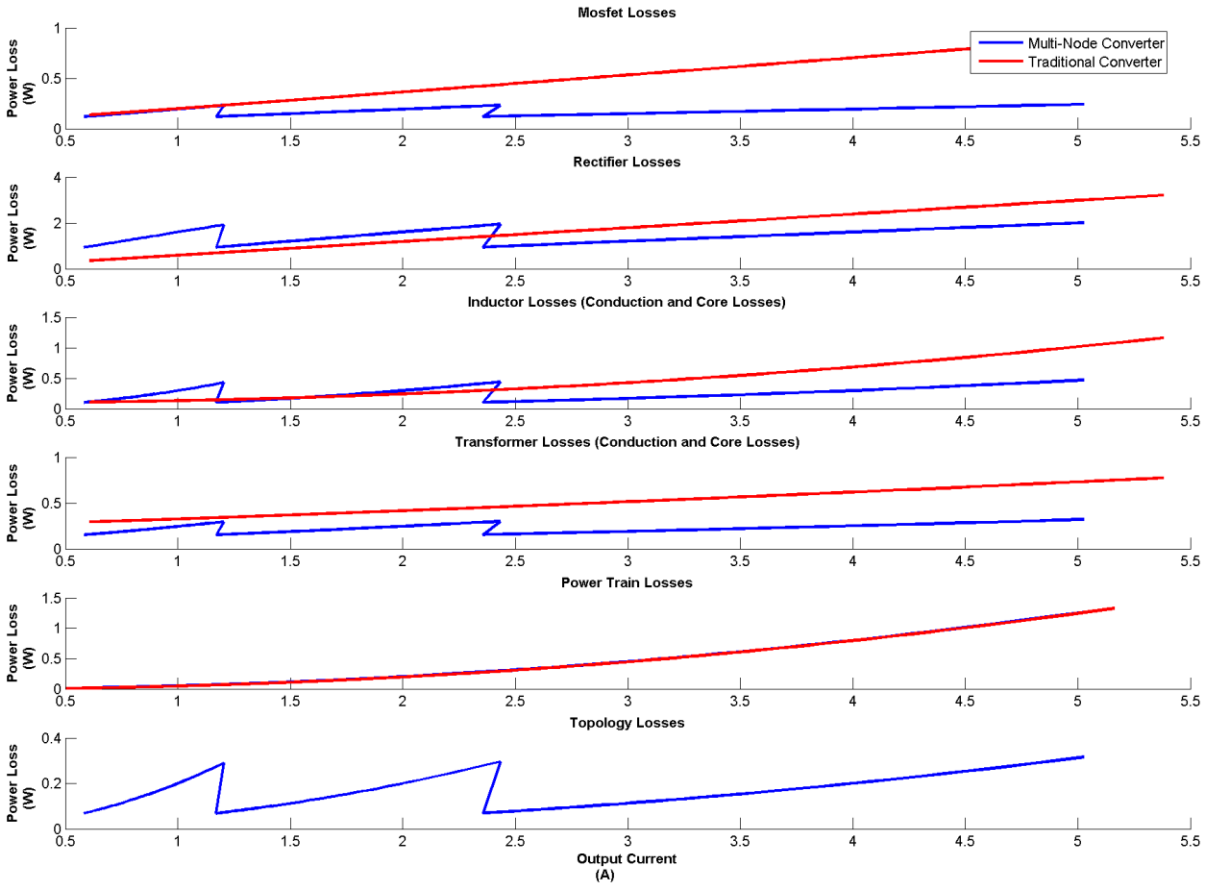


Figure 3.14: Component losses for both converters

3.4.3.3 MOSFET Losses

The MOSFET losses consist of conduction losses, switching losses, gate drive losses and losses due to the MOSFET output capacitance. It is clear from the figure that the multi-node converter design exhibits significantly lower MOSFET losses at higher output currents. The multi-node converter's

lower MOSFET losses are the result of its MOSFETs being exposed to lower peak currents. This results in lower switching losses and also lower conduction losses since the MOSFETs' equivalent RMS currents are also reduced.

3.4.3.4 Rectifier Losses

The rectifiers are responsible for the largest losses of any component in the converters. For this reason it is important that the rectifiers are selected carefully for the lowest forward voltage drop. Reverse recovery and its effects are not considered since both converters utilise Schottky rectifiers. Due to the high losses in the rectifiers, synchronous rectification may be worthwhile if any efficiency gain this brings is worth the additional implementation costs and effort.

The rectifiers in the multi-node converter are seen to exhibit higher losses than the traditional converter's rectifier at low output currents. This is due to the multi-node architecture, as when nodes are connected serially the full output current is sourced through multiple rectifiers. In essence the full load current flows through n rectifiers (n is the number of nodes) and experiences n diode drops. This is compared to the traditional converter where only one diode drop is encountered and this results in the multi-node converter showing higher losses at low load currents.

When the nodes are connected in parallel, the multi-node converter still experiences n diode forward voltage drops, but now only a fraction (1/n) of the load current flows through each rectifier. The result of this is that the rectifier losses remain at the same levels seen at low current outputs (when the nodes are serially connected) and do not increase significantly over the output current range. The traditional converter's rectifier losses are directly dependant on output current and it is clear that they increase linearly with output current and thus vary over a wide range. At higher output currents, the multi-node converter experiences lower rectifier losses since its rectifiers have a lower forward voltage drop.

3.4.3.5 Inductor Losses

The inductor losses that have been shown include both core and conduction losses. The conduction losses are dependent on the square of the RMS current ($i_{L,\,RMS}^2$) that flows through the inductors and so this is shown as Figure 3.15. The figure shows the square of the RMS current flowing in the traditional converter design's inductor and also in one phase of the multi-node converter design.

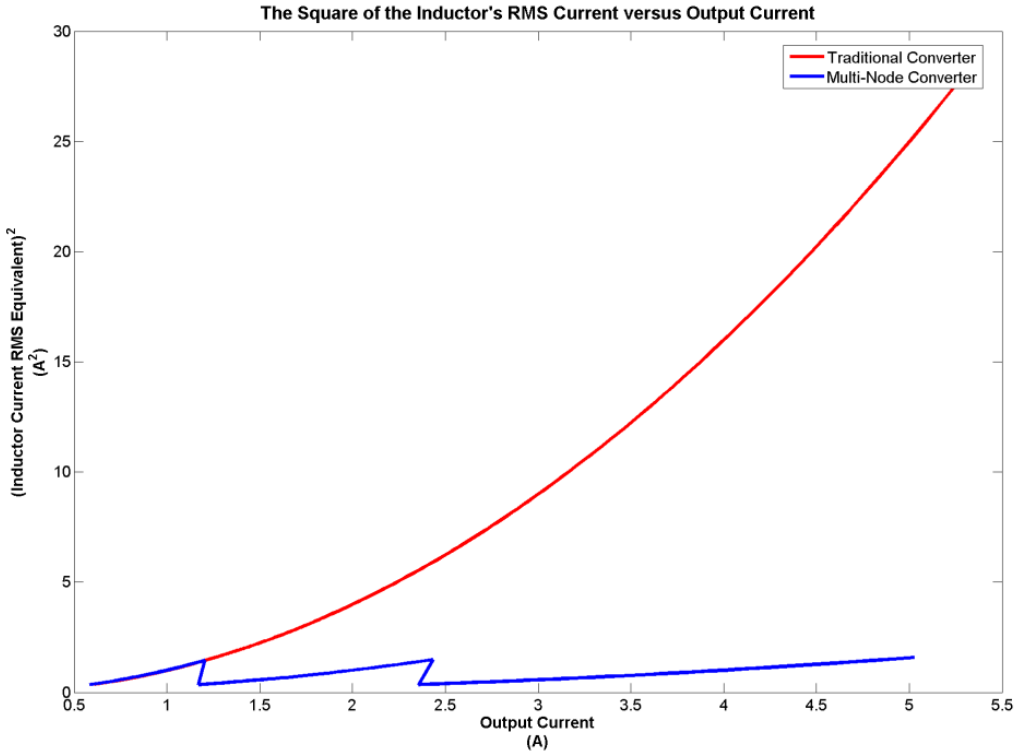


Figure 3.15: RMS inductor current squared over the output range

From Figure 3.15, we can see that $i_{L,RMS}^2$ for the multi-node converter is equal to that of the traditional converter at low output currents when the nodes are serially connected. This results in the higher inductor losses seen in the multi-node converter at low output currents since the multi-node converter's inductor has a higher resistance and there are also four inductors that experience this loss.

However at higher output currents $i_{L,\,RMS}^2$ for the traditional converter begins to rise dramatically. This leads to higher losses in the traditional converter's inductor at high output currents. This is contrasted to the square of the RMS current that flows in the multi-node converter's inductors, which remains relatively constant due to the nodal configuration changing.

3.4.3.6 Transformer Losses

The transformer losses were predicted using the DC resistance of the coils and core loss estimates from the manufacturer [13]. The results show that the traditional converter's transformer experiences higher losses compared to the multi-node converter's transformer. This is particularly evident at high output currents where, similarly to the RMS current in the inductors, the RMS current flowing in the traditional converter's transformer windings increases dramatically.

The core losses in the traditional converter are also greater than in the multi-node converter. This is evident when one considers that they are both made from the same core material and they are also both designed for the same peak flux density. The specific loss for both cores will thus be equal, but since the traditional converter's core is larger, it will experience higher absolute core losses. If equal core losses are desired in both designs then the peak flux density in the traditional converter's

transformer will need to be reduced. This will however mean that a larger core will be needed to contain the extra windings and also that the copper losses will likely increase.

3.4.3.7 Power Train Losses

Power train losses are any losses in the converter that are caused by any resistance between the output of the converter and where the actual load is connected (See Section 3.3.1.6 and Figure 3.12). This resistance has been modelled as a 0.05 Ω resistance in both converters and therefore the losses in both power train resistances are equal.

3.4.3.8 Topology Losses

Topology losses are only present in the multi-node converter and these losses are due to the resistance of any interconnections between the nodes. They have been modelled as a 0.05 Ω resistor between nodes that are connected. This resistance is based on easily available MOSFETs that could be used to connect the nodes. It is seen that these resistances dissipate approximately 0.5 W depending on the output current. This has an effect of the efficiency of the multi-node converter. Both converter's efficiencies are presented next.

3.4.4 The Theoretical Efficiency for both Converters

Figure 3.16 shows both converter's efficiency versus output current.

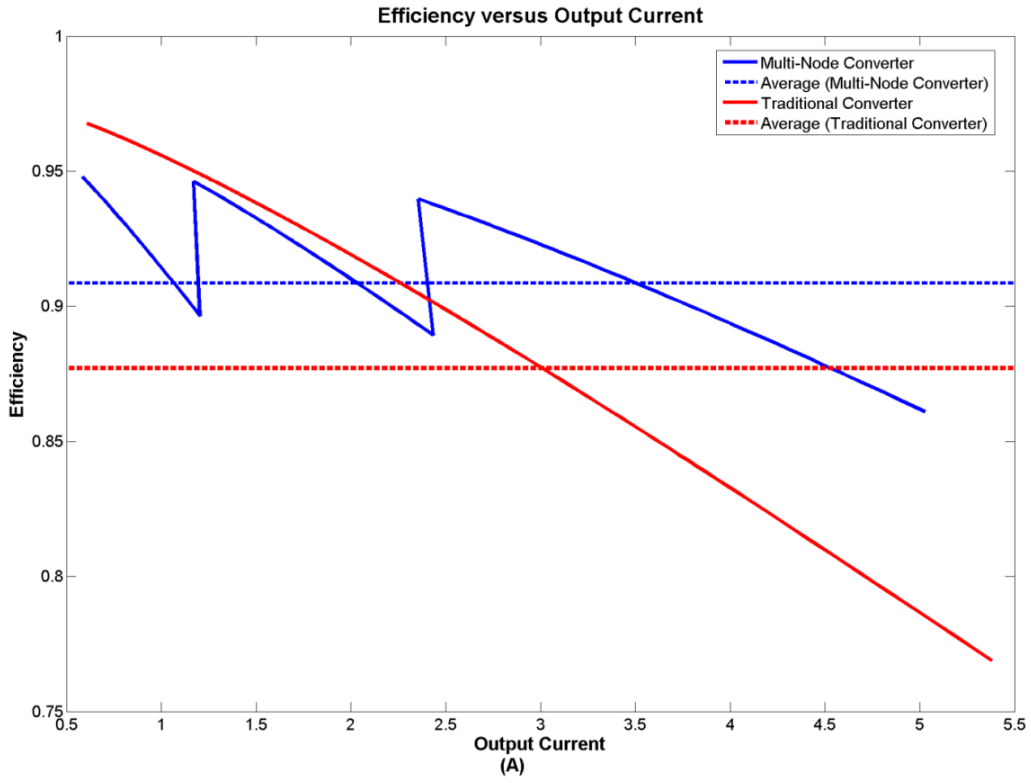


Figure 3.16: Efficiency versus output current for both converters

The traditional converter shows higher efficiency at low output currents. This is mainly due to the rectifier losses already discussed. However, losses in the multi-node converter's inductor at low output currents and the topology losses also contribute to this.

At higher output currents, the multi-node converter exhibits higher efficiency than the traditional design. This is expected since Figure 3.14 shows that the traditional converter tends to have higher component losses in almost every component at higher output currents.

The average efficiency for both converters is also shown in Figure 3.16. The average efficiency for both converters was calculated over a current range from 0.625 A to 5 A (the 8 times range). Any sections of the curve outside this range were not included in the efficiency calculation. The multi-node converter's average efficiency (90.9 %) is approximately three percent higher than the traditional converter's (87.7 %).

3.4.5 Analysis

A multi-node and a traditional converter have been designed to output the same constant output power over a wide range. The component choices and designs for the two converters were discussed and presented. It was found that the filter inductor for the multi-node converter was smaller and lighter than the inductor that would be required in a traditional design. This was predicted in Section 3.2.5.4.

The transformer in the multi-node converter was also smaller and lighter than the transformer required in the traditional converter. This was attributed to the RMS currents that flow in the multi-node converter's windings being lower. The smaller core also means that lower core losses are experienced for the same peak flux density since the core has a lower volume.

Section 3.4.2.4 showed the filter capacitors that were specified for the two converters. The requirements for the two converter's filter capacitors are very different since the traditional converter requires a capacitor with a higher voltage rating, yet a lower capacitance (due to its higher filter inductance). The lower capacitor voltage in the multi-node converter means that aluminium polymer capacitors can be used in this design. These capacitors meet the required specifications using a small surface mount package. This means that the filter capacitors in the multi-node converter were smaller than the capacitor in the traditional converter. However, the cost of aluminium polymer capacitors may be prohibitive and so a traditional electrolytic capacitor was also specified for the multi-node converter. When traditional electrolytic capacitor technology is used in the multi-node converter its filter capacitors are larger and heavier than the traditional converter's single capacitor. This was predicted when the filter capacitor requirements in multi-node converters were discussed in Sections 3.2.5.5 and 3.2.5.6.

Once the power components had been specified, the theoretical models that were developed in Section 3.3 were used to predict the output and losses for both converters. The models show that both

converters are able to meet the output range specification; however the traditional converter's duty cycle and the stresses its components are exposed to vary over a much wider range

The multi-node converter experiences higher losses at low output currents due mainly to the losses in its rectifiers and filter inductors. The reasons for these losses being greater than in a traditional converter were explored and have been discussed. Both converters' predicted efficiencies were then shown and the multi-node converter showed a higher average efficiency (3 % higher). This is despite its passive component requirements being generally lower than the traditional converters. This is possible due to the components being better utilised.

3.4.6 Conclusion

A multi-node converter design and a traditional converter design for outputting constant power over an eight times range were presented. The component requirements for both converters were discussed and why they are different was analysed. Each converter's performance was then quantified using the multi-node converter models that had already been developed. It was found that both converters were able to meet the output specifications, but that the multi-node converter had generally lower component requirements due to it being able to utilise its components more effectively. The multi-node converter also exhibited higher average efficiency over the output range.

3.5 Conclusion

The two-switch forward converter with multiple secondaries was proposed as a practical implementation of the multi-node architecture. The two-switch forward converter's operation was discussed and it was analysed with a focus on issues relevant to the multi-node architecture. Current sharing between paralleled phases was researched and the literature indicated that the leakage inductance being different for each phase was the primary reason for poor passive current sharing in the topology. It was then concluded that by careful magnetic design and implementation this could be mitigated.

How the filter component requirements changed with the number of nodes was addressed in Section 3.2.5, and it was shown that the coupled inductor in a multi-node converter will be smaller and lighter than the inductor in a traditional converter for a reasonable number of nodes. This reduction in size and weight is possible due to better utilisation of the component. However, the filter capacitors required in a multi-node converter are expected to be heavier and larger than those required in a traditional converter. This conclusion was based on the assumption that the same capacitor technology would be used for both converters. This assumption is not always true and the multi-node converter architecture may enable the use of different technologies that cannot be used in a traditional design. A change in capacitor technology may mean that a multi-node converter's filter capacitors may be significantly smaller and lighter than a comparable traditional converter's single filter capacitor.

Models for predicting the performance of multi-node converters with a two-switch forward converter topology were then developed. The first model allows any number of nodes to be simulated but it is limited in that the nodes must all be identical. The second model allows the nodes to be different, but it is limited to four node converters. The derivation of both models was discussed and they have been compared to one another. It was found that the models were consistent in predicting both the output of the converter and also the losses in the individual components. The two models were then used to predict the output and efficiency of a traditional converter and a multi-node converter in a comparative design example.

A multi-node converter with four identical nodes was compared with a traditional converter design. Both converters were required to operate over a wide range and the component requirements for both converters were compared. It was found that the multi-node converter had generally lower component requirements and was able to provide power over the required range with a higher average efficiency.

The next chapter (Chapter 4) uses the theoretical background presented in this chapter to develop and test a prototype multi-node converter with the same specifications as the comparative design. The components used in the prototype, its construction, and other practical issues are all addressed. Each section of the prototype is then tested. Chapter 5 will then test the prototype as a whole and evaluate its performance. The validity of the models developed in this chapter will then be discussed further.

CHAPTER 4

PROTOTYPE IMPLEMENTATION AND TESTING

The previous chapter theoretically analysed a proposed circuit implementation for a multi-node converter. These results are now used in the development of a prototype converter.

This chapter provides a description of a final multi-node converter prototype, its constituent parts and their testing. Chapter 5 then describes the testing and evaluation of the entire prototype and attempts to verify the theoretical models developed in the previous chapter.

Figure 4.1 below shows a schematic of the prototype and its component parts.

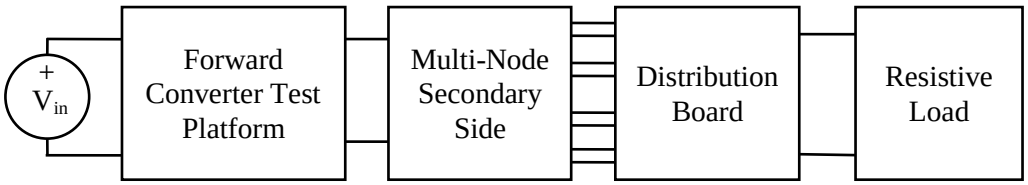


Figure 4.1: Final prototype schematic

The prototype consists of three circuit boards: a forward converter test platform, a multi-node secondary board and finally the distribution board. The three boards are all described and discussed in separate sections that follow.

4.1 The Two-Switch Forward Converter Test Platform

The standard forward converter architecture requires a separate demagnetising winding in the transformer to reset the core every switching cycle. This is inconvenient when one wants to test multiple transformers and secondary side configurations, as it means that each device under test must include hardware to allow the core to be reset. This hardware must be duplicated in every new device that is tested. It would be easier if all the hardware required to reset the core was fully contained within the test platform and only implemented once. The two-switch converter allows this as it does not require a demagnetising winding in each transformer that is tested [3] [4]. The topology and its operation were described in detail in Chapter 3.

4.1.1 Circuit Description

Figure 4.2 shows the test platform's basic structure with MOSFETs as the semiconductor switches. The sections shown in black are all contained within the converter test platform, while the grey section is a multi-node secondary board that is easily replaceable depending on the desired secondary side configuration. The test platform therefore consists of three main sections: A controller, MOSFET drivers and a power stage. A short discussion of each section follows.

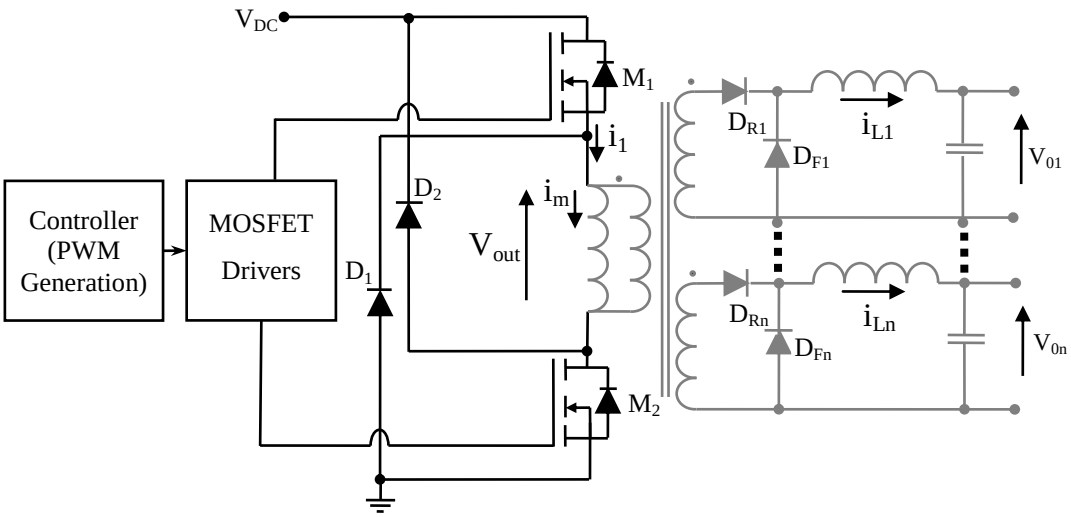


Figure 4.2: The two-switch forward converter test platform

4.1.1.1 Control System

The controller consists of a simple open loop PWM control system with the frequency of operation and pulse-width fully controlled by the operator. Open loop control is used due to its simplicity (no hardware is required on the secondary side for operation) and to allow the operator to have full control over the converter at all times. For a description of control system, its implementation, operation and testing, see Appendix A.

4.1.1.2 MOSFET Drivers

The MOSFET drivers allow the primary side MOSFETs to be switched rapidly. They source, or sink, current on the order of amperes to rapidly charge, or discharge, the MOSFET's gate capacitance. This allows the switching losses within the MOSFET to be minimised by minimising the length of a switching transition. There are many ways to implement the MOSFET drivers, however this is not the focus of the research and so a simple, practical solution in the form of a MOSFET driver IC was sought. Many driver ICs also implement hardware required for the operation of a high-side (not referenced to ground) switch. For more information on the implementation and testing of the drivers refer to Section 4.1.2 and Appendix A.

4.1.1.3 Power Stage

The power stage consists of the two MOSFET switches and the two primary side diodes. The switches are operated simultaneously and when both are on, power is transferred to the secondary side and load. Core resets are achieved using the two diodes. When both switches are turned off, the transformer's magnetising inductance current must continue to flow and so these diodes are forward biased and the DC bus voltage is applied to the transformer with opposite polarity. This continues until the core has reset and the diodes switch off (since the magnetising current flowing through them

reaches zero). This method allows reliable core resets to be performed using no additional transformer windings. The converter's operation was discussed in detail in the previous chapter.

4.1.2 High-Side Driver Implementation Issues

The largest implementation issue faced when building the prototype was ensuring reliable high-side driver operation. A combined high-side and low-side driver IC (IR2113) was used in the converter test platform [14]. The problem that is faced is that a gate-source voltage of approximately 15 V needs to be generated in order to successfully switch the high-side MOSFET. This is a challenge since the high-side MOSFET already floats to the highest potential available in the circuit. This means that an additional potential above the DC bus voltage needs to provided or generated. A common solution to the problem is discussed below.

4.1.2.1 Standard Implementation

A common solution for this problem is shown in Figure 4.3. A Buck Converter containing a high-side switch is depicted with a bootstrap capacitor (C_b) and diode (D_b) highlighted [14] [15].

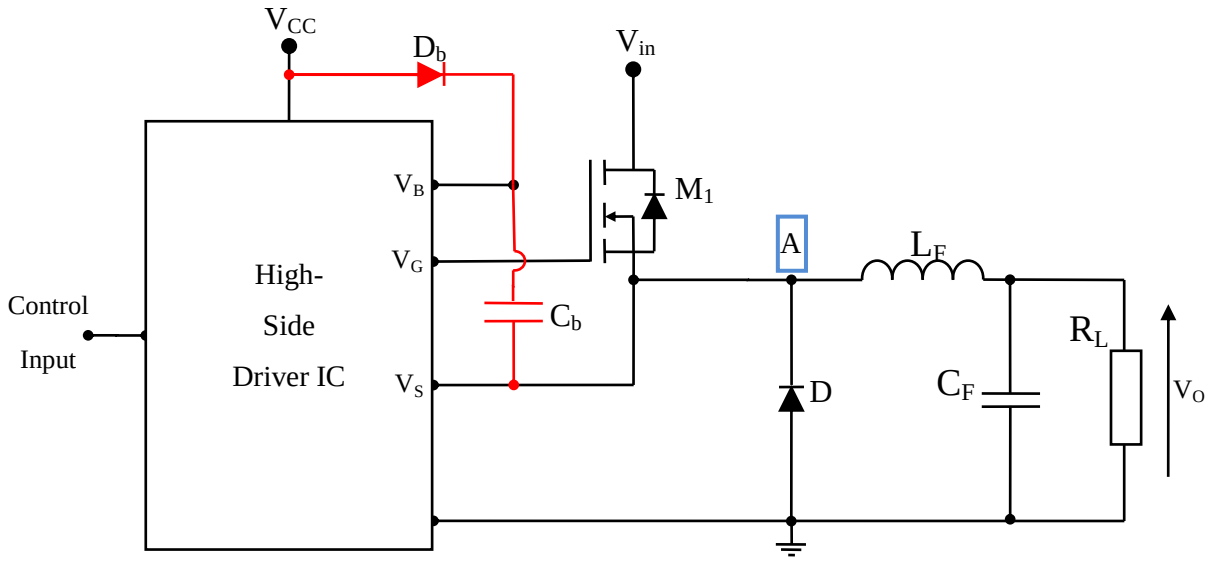


Figure 4.3: Typical high-side driver implementation

When the circuit is initially turned on, the bootstrap capacitor (C_b), is fully discharged and the MOSFET is in its off state. The voltage at node A is also at ground potential since the filter capacitor is discharged and no current is flowing in the inductor. This means that the bootstrap diode (D_b) becomes forward biased and current flows into the bootstrap capacitor, charging it to V_{CC} minus the diode's forward voltage drop. When the control signal applied to the driver IC goes high, it uses the charge stored in the bootstrap capacitor to turn the MOSFET on. As the MOSFET switches into its on state and begins to conduct the voltage across it will decrease. The MOSFET's source and the

bootstrap capacitor then float up to very nearly the input voltage for the converter, V_{in}. Now, even though the MOSFET's source is floating higher than the input voltage to the driver IC, the MOSFET remains on as the bootstrap capacitor provides an auxiliary supply referenced to the MOSFET source.

Once the control signal to the driver IC goes low, the MOSFET is switched off and current commutates to diode D_1. Since D_1 is conducting, the source of the MOSFET and capacitor are pulled back down to ground. This ensures that the bootstrap capacitor can be charged again as the bootstrap diode becomes forward biased. This process is repeated each switching cycle where the bootstrap capacitor is charged when the control signal is low and prevented from discharging by the bootstrap diode when it is high.

The above technique relies on node A being pulled to ground for long enough to transfer charge to C_b each cycle. This can be ensured in the case of a Buck Converter in CCM by limiting the maximum duty cycle. However this is more difficult with the two-switch forward converter. Consider Figure 4.4 which shows the converter with a bootstrap-diode based high-side driver connected.

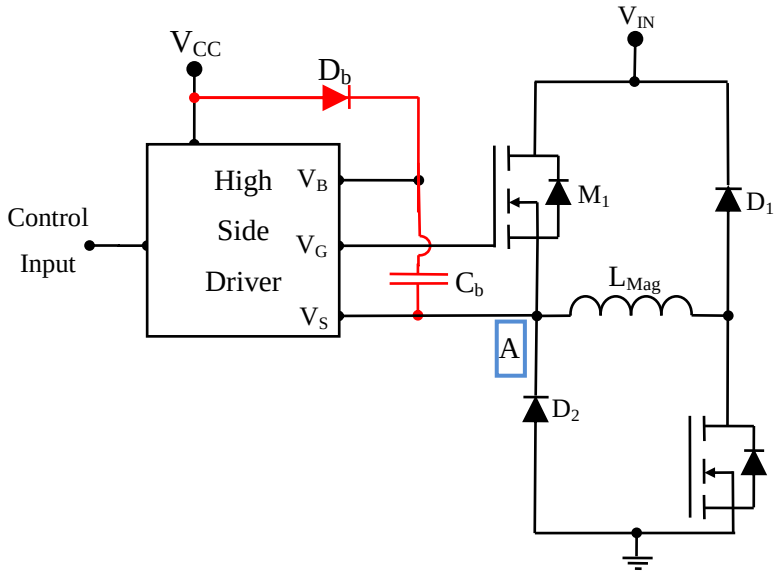


Figure 4.4: Bootstrap capacitor operation with a two-switch forward converter

In order to charge the bootstrap capacitor we once again need node A, in Figure 4.4, to be pulled low. At start up the capacitor is initially charged when the low side MOSFET is turned on. However, during normal operation, the capacitor only gets charged when D_2 is conducting and the core is being reset. In practice, this can become unreliable when the duty cycle, and thus the core reset time, becomes small. In order to allow correct operation of the converter, without any lost cycles, modifications to the standard design should be made that allow the bootstrap capacitor to be charged every cycle, no matter what the converter's operating point.

4.1.2.2 Driver IC Usage in Two-Switch Forward Converters

The author has encountered two main methods for ensuring that the bootstrap capacitor remains charged when a two-switch forward converter is used. The first method involves the usage of a switched capacitor supply for transferring charge to the bootstrap capacitor (even when it is high) [16] and the second method simply ensures that node A is pulled low for long enough to charge the capacitor every cycle [15].

The first method's operation is shown schematically as Figure 4.5. The circuit has two modes of operation depending on the position of the switch. When the switch is in position 1, C_1 is charged through D_1. This raises the potential on the first capacitor to approximately V_{cc} (Normally 15 V). When the switch's position is now changed to position 2, the charged capacitor (C_1) forward biases D_2 and delivers charge to C_2. By this method charge can be continuously delivered to C_2, which is prevented from discharging back into C_1 by diode D_2. This creates a supply where charge is delivered to C_2 when it floats above ground. This circuit takes the place of the bootstrap arrangement shown in Figure 4.4 and has been shown to be effective [16].

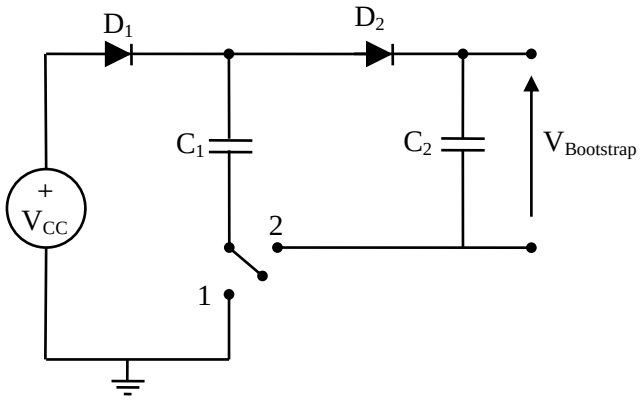


Figure 4.5: Charge pump supply schematic

Actually implementing the switched capacitor circuit is however more complex than the simple circuit diagram implies. Implementing it with semiconductor switches takes two MOSFETs, three diodes and a clock signal with which to clock the switches is also needed. This means that this method may be more complex than necessary if the high-side switch does not require indefinite on times.

The second method for ensuring that the bootstrap capacitor remains charged involves modifying the standard bootstrap circuit. This is the method that was used in the final converter test platform and the final schematic is shown as Figure 4.6 with an IR2113 high- and low-side driver IC from International Rectifier. The modifications that would be made to a standard implementation are highlighted [15]. The point of the modifications is to ensure that the bootstrap capacitor is pulled low for long enough to charge the bootstrap capacitor every cycle.

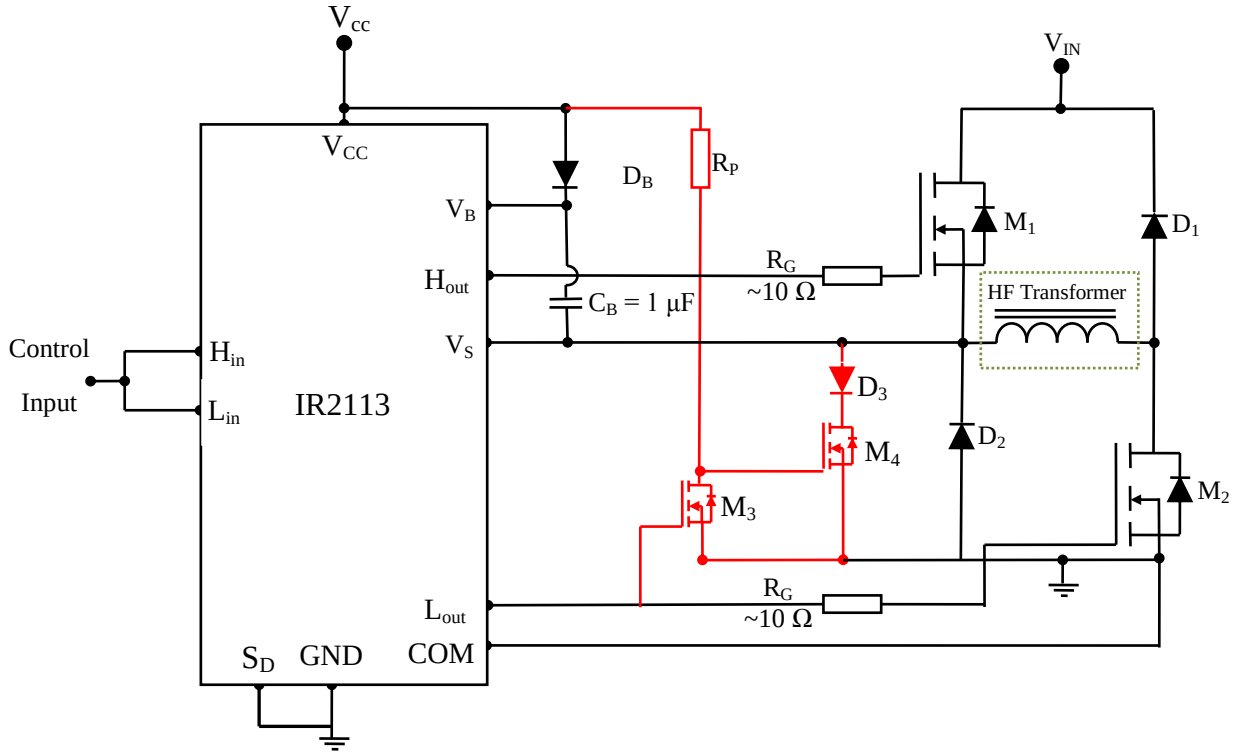


Figure 4.6: The final high- and low-side driver schematic

The modifications consist of a MOSFET inverter made up of M_3, M_4 and a pull-up resistor R_p. When the drivers go low, M_3 turns off, allowing the pull-up resistor to turn M_4 on. This pulls the bootstrap capacitor low for as long as the drivers remain low. The bootstrap capacitor is then allowed to charge. As soon as the drivers go high, M_3 switches on, which turns off M_4 and allows the bootstrap capacitor to float up to the DC bus voltage. These modifications were made to the standard design and implemented as part of the forward converter test platform. The modifications were successful and their effectiveness will be seen when the test platform is tested. Appendix A also shows how the drivers and the modifications made to the standard implementation were tested.

4.1.3 Practical Implementation

The practical implementation issues surrounding the development of the converter test platform are discussed in this section.

4.1.3.1 Component Selection

It needs to be pointed out that the converter being built is actually a test platform for multiple secondary configurations. This makes the selection of the converter's components difficult as the primary side component requirements are inextricably linked to the secondary side configuration (which is not known and will change). For this reason it was decided that the converter's components should be highly specified so that they would be able to operate with any likely secondary

configuration or primary side DC bus voltage. Easily available 500 V and 20 Ampere MOSFETs (IRFP 460) were chosen as the primary side switches. The diodes used for resetting the core were 400 V ultra-fast diodes (UF4004) and the DC bus capacitor consists of a 68 µF 400V electrolytic capacitor in parallel with a 220 nF metal film capacitor.

The controller was implemented with an UC-3825 High-Speed PWM controller from Texas Instruments. It allowed a controller with variable frequency and duty cycle to be developed simply and easily and also allowed for other features, such as soft starting and maximum duty cycle limitation (to less than 50 %). As mentioned earlier, closed-loop control was not used in the test platform in the interests of simplifying the design and also allowing the operator to have full control of the converter.

4.1.3.2 Printed Circuit Board Design, Layout and Implementation

Printed circuit board layout can be a significant challenge when designing an effective switching converter. Due to currents of significant magnitude being switched and commutated quickly (i.e. with high di(t)/dt), it is important to reduce stray inductance in the circuit where fast changes of current are expected. This can improve switching performance, reduces interference to nearby circuits and ringing in the power stage [17]. For these reasons, the layout of the board and its effects on switching performance must be analysed so the pertinent sections of the PCB can be optimised.

In order to reduce stray inductance in the power stage we need to minimise the area contained between the "go" and "return" current paths in the converter. How this area changes before and after a switching transition is also of prime importance. Optimising the layout of paths containing a larger series inductance (for example the leakage inductance of a transformer connected to the output) is also counterproductive, since this series inductance is likely to be orders of magnitude larger than the stray inductance caused by the board's layout. By analysing the circuit it was determined that the area between the DC bus capacitors and the power stage and the change in area when the transformer magnetising current is commutated to the clamping diodes should be minimised. These are therefore the electrical layout goals for designing the converter's PCB.

There are also other practical constraints to consider when designing the PCB:

- The MOSFETs should be placed in a position where they can be easily heat-sinked.
- Provision for a series RC snubber across the output is required.
- The test platform nature of the converter means that connecting various secondaries must be simple and easy. This means that the output connecter should be placed at the edge of the board.
- Space to work and to take measurements is required as this is a prototype converter. The layout and design of the circuit needs to be designed with this in mind. It would be

counterproductive to design the circuit with best electrical layout in mind if this meant that measurements were difficult to take.

- A single sided board is preferable to a multi-layer board. Two layers is the maximum imposed by the available prototyping facilities.
- The final constraint is due to the physical size and shape of each component.

Figure 4.7 shows the final layout of the power stage in the converter test platform after these constraints and the electrical layout goals were considered. The yellow and red paths respectively show where current flows with the MOSFETs and the diodes conducting.

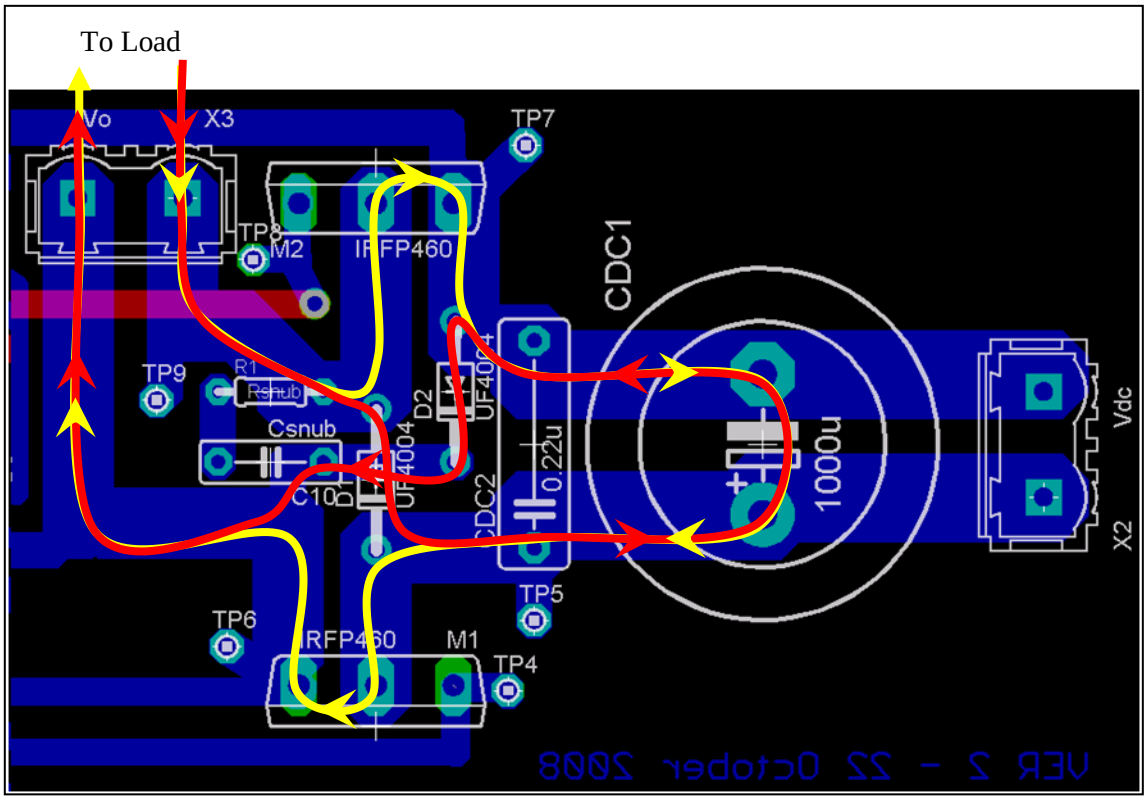


Figure 4.7: Converter test platform power stage

The DC bus capacitors have been placed as close to the power stage as possible and we can also see the other design constraints in evidence. For example, the MOSFETs are at the edges of the board and can be easily heat-sinked.

Once the power stage had been designed the controller and drivers were also placed on the same board. The final board, including drivers and controller is shown as Figure 4.8.

When designing the board, additional goals and requirements were developed. Separate logic and power grounds were used to keep high frequency switching currents flowing in the power ground from affecting the operation of the logic subsections. These two grounds were then connected at only a single point. The connecters, on-switch and potentiometers for controlling frequency and duty cycle were also placed where they could be easily accessed. Finally, test points were included and

components with polarisation (e.g. diodes and IC's) were placed with the same orientation when possible. This simplifies troubleshooting and testing of the board since if a polarised component is installed backwards it is immediately obvious.

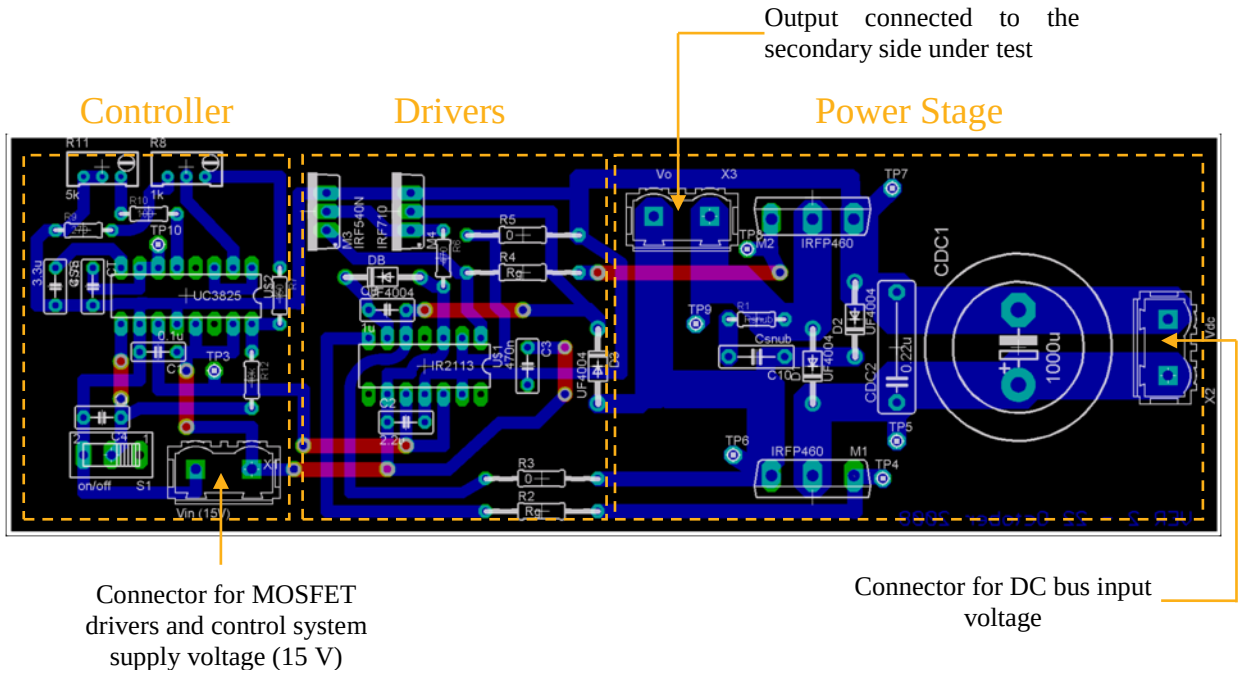


Figure 4.8: Converter test platform PCB design

Once the board layout was developed it was manufactured and populated. The final test platform, that was used in testing and for the final prototype is shown in Figure 4.9. The test platform is further documented in Appendix B, where circuit diagrams and a parts list are shown.

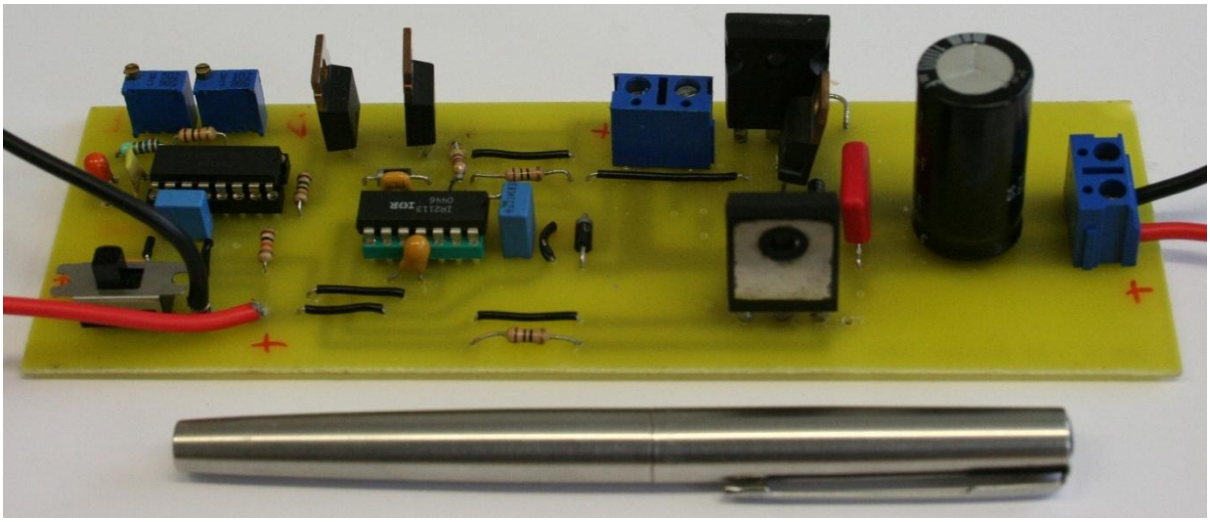


Figure 4.9: The two-switch forward converter test platform

4.1.4 Testing with a Resistive Load

The forward converter test platform was tested using a 100 Ω resistive load and a 60 V DC bus. The converter's output voltage (V_{out} in Figure 4.2) is shown as Figure 4.10. The forward converter outputs a square wave into the resistor with a duty cycle that is varied between zero and 45 %.

There is a slight glitch on the waveform as it goes low after each cycle. This glitch is due to the wirewound resistor that was used as the load having a slight inductive component. This inductive component rings with the primary side MOSFET and diode stray capacitances when the MOSFETs switch off. A similar effect is discussed in detail when the test platform is tested with a transformer load in Section 4.1.5.

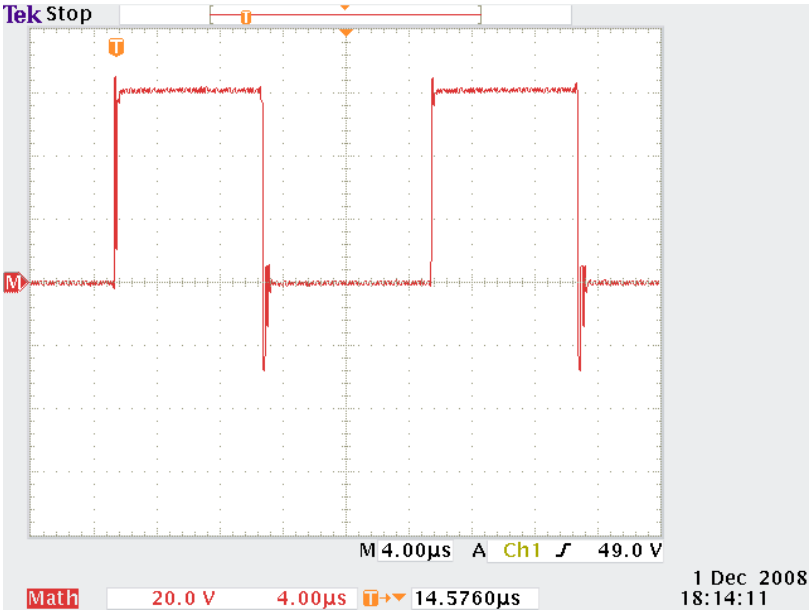


Figure 4.10: Output into a 100 Ω load

It is also noted that the converter is able to consistently switch the high-side MOSFET, despite the fact that the primary side clamping diodes (D_1 and D_2 in Figure 4.2) do not conduct for a resistive load. This implies that the modifications made to the original high-side driver design (to ensure that the bootstrap capacitor remains charged under these circumstances) are working correctly. With the modifications the converter was able to switch reliably, without any missed cycles. This is shown in Figure 4.11, where the converter switched reliably for 50 cycles with a resistive load (without the modifications, the converter only switched reliably for 4-5 consecutive cycles before missing a cycle).

It is also noted that the glitches shown in Figure 4.11 seem to show some sort of sinusoidal modulation. The modulation frequency did not seem to correlate with any frequency that should be present in the circuit. For this reason it was postulated that the modulation seen was simply due to the digital nature of the oscilloscope's display. The same waveform was then displayed at different time and voltage scales and it was noted that the effect ceased. From this it was concluded that the

sinusoidally modulated glitches seen in the figure are simply the result of the oscilloscope's digital display and do not represent a true phenomenon.

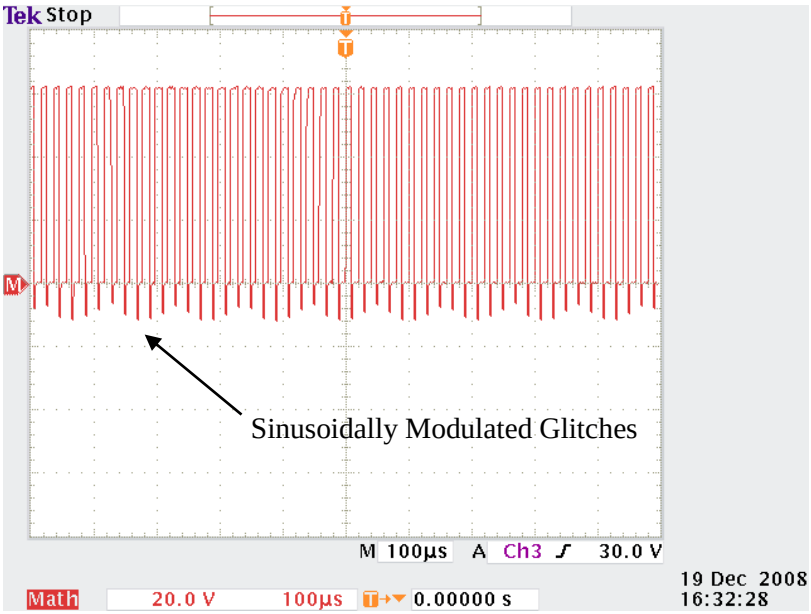


Figure 4.11: Output into a 100 Ω load

4.1.5 Testing with a Transformer Load

4.1.5.1 Transformer Load Specifications

The transformer load that was used to test the converter has the following characteristics:

- An E30 core from EPCOS (N87 Material).
- A primary side consisting of 32 turns of 0.5 mm diameter copper wire.
- Four identical 12 V, 1 A secondaries, each consisting of 17 turns of 0.5 mm diameter wire. The secondaries are all wound multi-filar to ensure that their leakage inductances are as similar as possible.
- Each secondary output is then individually rectified, filtered and then connected in parallel with the other outputs and a 4.7 Ω resistive load.

This forms a representative load, that the converter test platform would be expected to drive when researching multi-node converters. It is therefore suitable for assessing the test platform.

4.1.5.2 Output Voltage Analysis

The measured primary transformer voltage (V_{out} in Figure 4.2) is shown as Figure 4.12. There is a significant deviation in the practical measurement compared to the ideal converter waveforms shown in Chapter 3, Figure 3.2. This deviation is labelled in Figure 4.12.

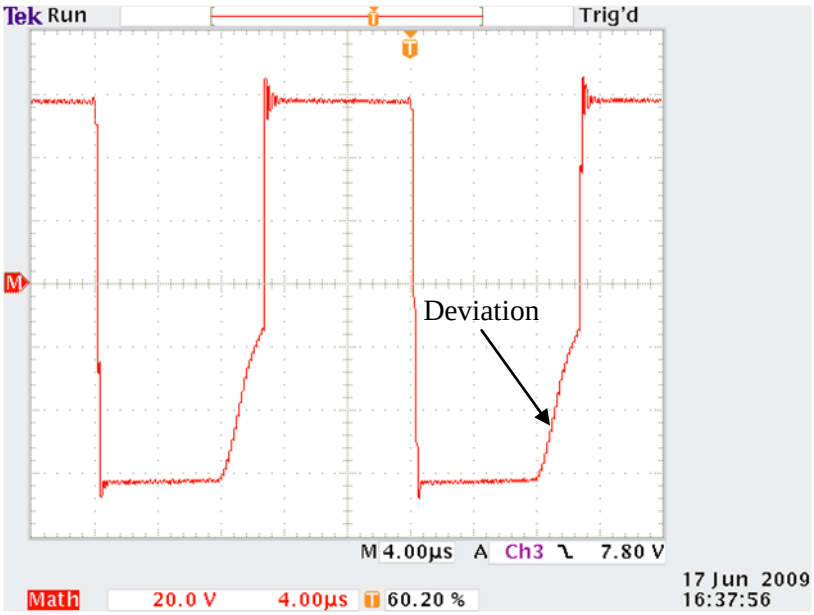


Figure 4.12: The forward converter test platform's output into a transformer load

The deviation occurs after the transformer core is reset and the clamping diodes turn off. The output voltage then slowly begins to rise toward zero. This rise time is very slow and does not correspond with the ideal converter waveforms from Chapter 3. The deviation occurs after the clamping diodes turn off when the core's magnetising inductance resonates with the output and junction capacitances in the primary side MOSFETs and diodes. The equivalent circuit during this period is derived in Figure 4.13 below (Parasitic resistances in the tracks and components are ignored). The effect of the high-side driver is also noted as it pulls the one side of the transformer's primary to ground. This shorts the MOSFET and diode parasitic capacitances in that leg of the model to ground.

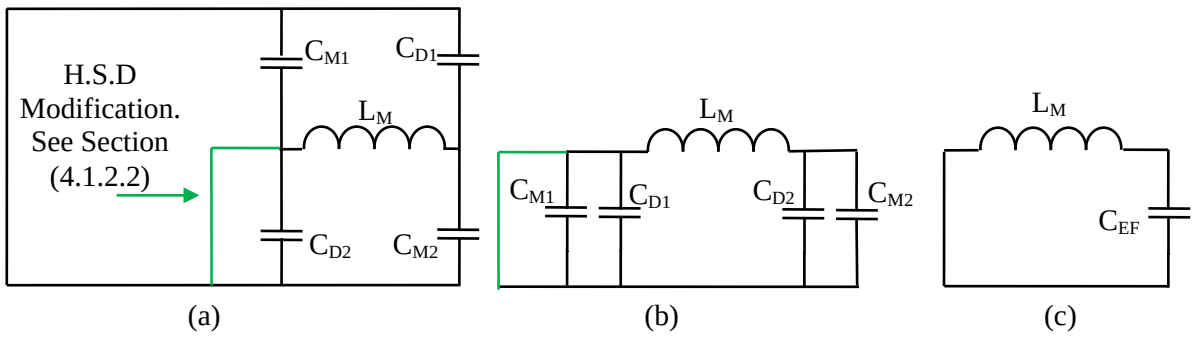


Figure 4.13: A simplified equivalent LC circuit for the two-switch forward converter once the clamping diodes have turned off

When the clamping diodes turn off the low-side MOSFET's output capacitance (C_{M2}) is initially charged to the converter's DC input voltage. After combining the capacitors in the model and taking note of their orientation, the final effective LC circuit can be derived. This circuit consists of a single

inductor and capacitor and is shown as Figure 4.13 (c). Since C_{EFF} is initially charged, a voltage begins to oscillate between the inductor and capacitor. The slow rise time seen in the practical prototype is the initial section of this oscillation. If the specified output and junction capacitances from the semiconductor's data sheets are used and if the magnetising inductance's magnitude is known then the frequency of oscillation can be predicted. The magnetising inductance has been measured at 3 mH (calculated from the current waveforms in the following section) and the semiconductor capacitances are specified as 500 pF and 20 pF for the MOSFETs and diodes respectively. The natural frequency of oscillation is then given by Equation (4.1) [4] [18].

$$\omega = \sqrt{\frac{1}{L_M C_{EFF}}} \tag{4.1}$$

The predicted oscillation has a period of 7.84 μs. Determining the period of the oscillation seen in Figure 4.12 is difficult since only a small section of the waveform is seen. However, from the figure, a period of 7.84 μs is reasonable for the waveform and it is concluded that the slow rise time seen in Figure 4.12 is caused by the transformer's magnetising inductance resonating with the primary side semiconductor's stray capacitances.

However, there is one other interaction in the circuit that has not yet been mentioned. Once the voltage across the transformer primary goes positive, the oscillation stops completely. This is due to how the high-side driver was practically implemented. Once the transformer voltage goes positive, the low side MOSFET's body diode and diode D_3 in Figure 4.6 become forward biased and provide a current path through M_4 for the magnetising current. This effectively ends the oscillation. An equivalent circuit for this time period is shown in Figure 4.14. During this time period, the transformer's primary voltage is clamped by the two diodes in the current loop and no significant voltage is applied across the magnetising inductance. This means that the magnetising current remains relatively constant and the MOSFET's body diode and D_3 continue to conduct until the next switching cycle.

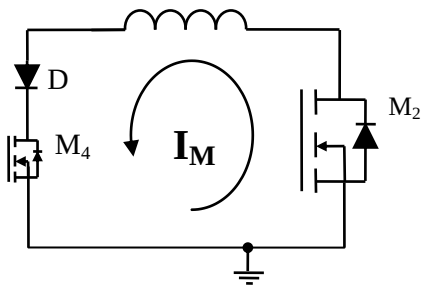


Figure 4.14: Equivalent circuit when the oscillation ends

One unfortunate side effect of the oscillation is that the transformer's magnetising current is not zero for the remainder of the cycle. This is not a catastrophic problem as the current that does flow is very low and does not have a tendency to increase each cycle. The transformer's magnetising current simply starts each cycle from a small negative value. This does not negatively influence the performance of the converter or its output.

But, if one desires "text-book" waveforms from the converter, then this effect can be negated further. The simplest, and best way to achieve this would be to choose MOSFETs with a lower output capacitance (the MOSFETs have by far the largest stray capacitance in the prototype). However, a MOSFET with lower current capabilities may have to be used to achieve this. A second method, where a diode is inserted in series with the low side MOSFET was also tried. This had the effect of reducing the effective capacitance in the resonant circuit and increased the slow rise time. The transformer primary voltage with this modification is shown in Figure 4.15, where the rise time after the clamping diodes switch off is faster. The disadvantage with this method is that the diode does have an effect on efficiency as it is directly in the main current path.

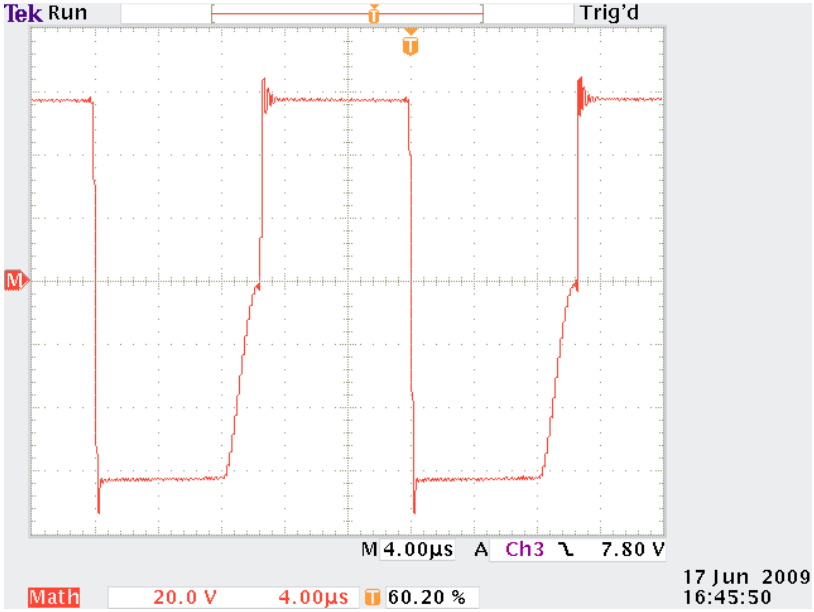


Figure 4.15: Transformer output voltage with the series diode modification

For the final prototype it was decided that operation without the diode was preferable. This is because the deviation from ideal operation does not negatively impact the output of the converter due to the rectifying diodes on the secondary side. The diode is therefore an unnecessary extra loss and an extra complication when modelling the prototype theoretically.

4.1.5.3 Transformer Primary Current

The current that flows through the transformer primary was also measured using a Hall Effect current probe. Figure 4.16 shows the current that flows in the transformer primary. The primary current waveform is of the same form as predicted in Chapter 3, Figure 3.2.

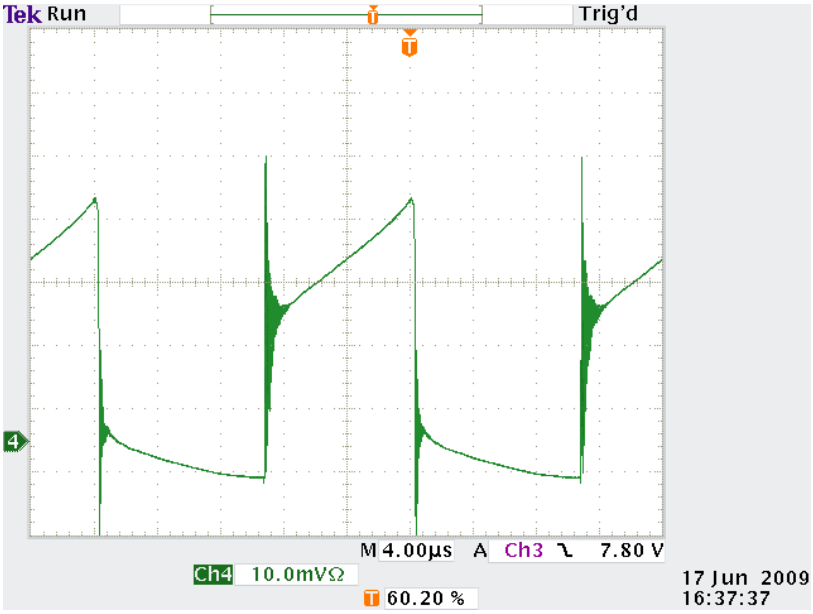


Figure 4.16: The transformer's primary current (200 mA/div)

The primary current has two sections: one where the main semiconductor switches are conducting and the second where the clamping diodes conduct and the transformer core is reset. In the figure above the section of the waveform with the positive gradient is where the semiconductor switches are conducting. In this section, positive voltage is applied to the transformer's magnetising inductance and also to the output filter inductors on the secondary side of the converter. This causes the current in both to rise and leads to the positive current gradient. From the figure, it is also clear that the secondary side filter inductors are in the CCM. We can see this since the current waveform begins to rise from a non-zero level.

The second section of the waveform is also crucial. In this section the transformer core is reset to prevent it from saturating. The clamping diodes in the converter conduct and the voltage applied to the transformer's primary is reversed. This means that the transformer's magnetising inductance current is gradually reduced to zero, thus resetting the core. Note that the current that flows in the secondary side output filter inductors does not affect the primary side transformer current in this section (due to the secondary side inductor current flowing in the freewheeling diodes on the secondary side at this time).

There is also a glitch or resonance in the current waveform as the primary side MOSFETs switch on and the current begins to rise. The literature predicts that this oscillation could be caused by the transformer's leakage inductance resonating with parasitic capacitances in the rectifying diodes [18]. This same effect can be seen in the rectifier output voltage waveforms in Section 4.2.3, where it is analysed farther.

4.1.6 Suitability for Use

The test platform has been tested with a variety of loads and it was found that the converter operated reliably and was able to consistently switch at even low duty cycles or with resistive loads. Whether the test platform was able to reset the core of an inductive load was also analysed and it was found that the core reset diodes performed as predicted. During testing a deviation from ideal, textbook, behaviour was noticed due to the transformer's magnetising inductance resonating with stray capacitances in the primary side semiconductors. It was decided that the deviation would have a negligible effect on the performance and output of the converter due to the rectifiers present in a forward converter secondary. This will however be checked when the secondary side is tested.

The forward converter test platform will now be used to test the secondary side and it will also be used when evaluating the performance of the final prototype in the next chapter.

4.2 The Multi-Node Secondary

The multi-node secondary board consists of multiple identical forward converter secondaries on the same board. This circuit is connected to the output of the forward converter test platform and each secondary separately rectifies and filters the transformer's output to generate multiple DC outputs. These outputs are then combined in series/parallel combinations with the distribution board to form a multi-node converter. Figure 4.17 shows the multi-node secondary circuit, highlighted in black, in the context of the entire converter's schematic.

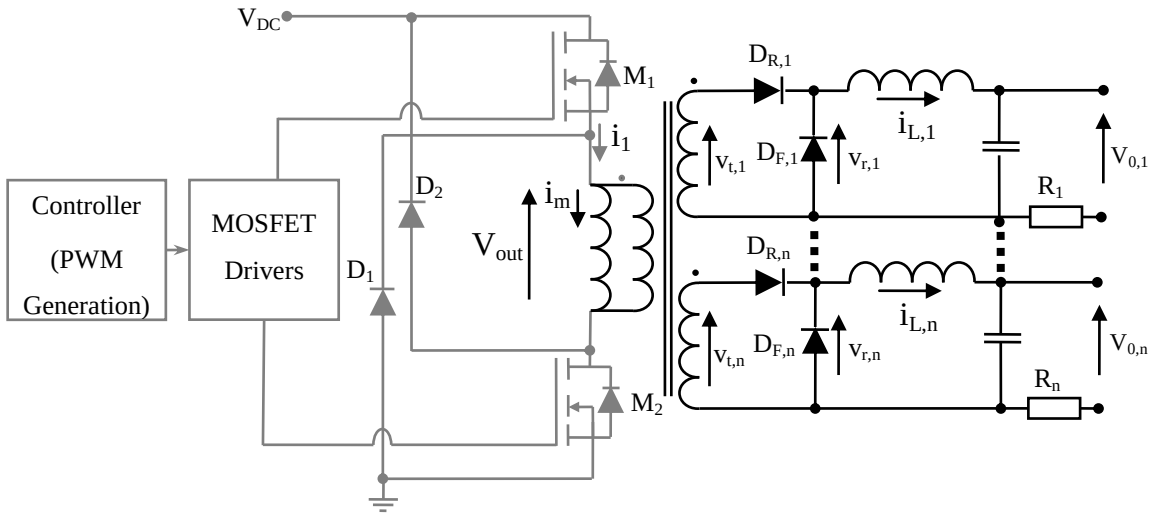


Figure 4.17: The two-switch forward converter test platform

The phases are all isolated due to the transformer and when the phases are paralleled, current is shared passively. How to optimise the passive current sharing is therefore important and is analysed. The design, implementation and testing of the multi-node secondary board is then discussed.

4.2.1 Current Sharing

4.2.1.1 Transformer Leakage Inductance Effects

Section 3.2.4 in Chapter 3 showed that if the transformer secondaries have unequal leakage inductances, then cross regulation errors occur and current sharing in the topology is degraded. These unequal leakage inductances are often the largest single factor that degrades cross regulation [8]. Poor cross regulation will directly lead to unequal current sharing in the phases due to each phase outputting a slightly different output voltage. For this reason it is important that each and every phase has equal leakage inductance.

The leakage inductances depend on the actual windings in the transformer. To ensure that each phase has equal leakage inductance we should ensure that each phases windings and their distribution in the transformer window are as identical as possible. For this reason the secondary windings were would multi-filar. This was the easiest way of ensuring that the difference in leakage inductances between the secondaries is negligible.

4.2.1.2 Output Resistors

Even if care is taken to ensure that the turns ratios and leakage inductances for the transformer are equal, the outputs of the different secondaries will all be different due to component tolerances. For example, each diode will have a slightly different voltage drop and the parasitic resistances in each phase will not be equal either. This can cause significant current sharing errors.

The effect of these component tolerances can be mitigated by placing small droop resistors ($< 0.5\ \Omega$) in series with each output (Resistors R_1 to R_n in Figure 4.17). These resistors will lower system efficiency to some degree, but they also tend to improve current sharing. The reason for this is illustrated in Figure 4.18.

Two converters with output voltage regulation curves (V_{01}) and (V_{o2}) are connected in parallel. These output voltage curves are not the same due to component tolerances in the converters. When the converters are paralleled their output voltages must be equal (illustrated by the dotted horizontal line). In order for this to occur each converter sources current such that their output voltages are equal. For converter one (with regulation curve V_{01}) this means that it must source more current than converter two. Converter one sources (I_{o1}) and converter two sources (I_{02}). The current mismatch ($|I_0/2 - I_{01}|$) that occurs can be influenced by changing the slope of each converter's current regulation curve. This is seen when comparing Figure 4.18 (a) and (b) where (b) has a steeper voltage regulation curve and results in better current sharing. This is known as the droop method for current sharing [19].

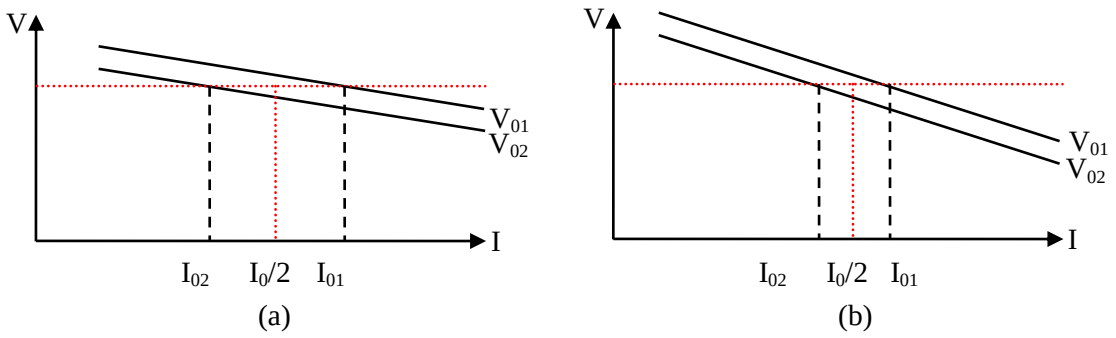


Figure 4.18: The droop current sharing method (a) with a shallow voltage regulation curve. (b) with a steep voltage regulation curve [19].

Adding a resistor in series with each current output steepens each converter's current regulation curve and will tend to improve current sharing in paralleled converters at the expense of efficiency. This has been considered and it was decided that for the multi-node converter prototype, this advantage outweighs the disadvantage. Small droop resistors will therefore be placed in series with each output.

The output resistors also have a second advantage, in that they also act as current shunts that allow the current in each phase to be quickly and easily measured. This is desirable in a multi-node converter prototype and will allow measurements to be taken more easily.

4.2.2 Practical Implementation of the Multi-Node Secondary

This section describes the design and practical implementation of a four node converter secondary. The implementation of the magnetic components, the selection of the filter capacitors and the layout and implementation of the printed circuit board are all discussed.

4.2.2.1 Secondary Specification

The multi-node secondaries specifications are given in Table 4.1. The specifications are the same as those used for the comparative design example in Chapter 3, and are repeated here for convenience. The specifications were used during the selection and design of the components in the multi-node secondary, which may be different to those specified in the comparative design due to component availability. These components are described in the following sections.

Table 4.1: Multi-Node secondary specifications

Number of Nodes		4
Maximum Node Voltage	$V_{o,\,max}$	12 V
Minimum Node Voltage	$V_{o,\,min}$	6 V
DC Bus Voltage	V_{DC}	60 V
Output Power (per node)	P_n	7.5 W
Switching Frequency and switching Period	F,T_a	50 kHz, 20 µs
Max Duty Cycle	D_{max}	0.45
Output Voltage Ripple	ΔV_o	2 %

4.2.2.2 Transformer Design

The multi-node secondaries transformer consists of a primary and four identical secondaries wound on the same ferrite core. The core is an E30 that is made from Epcos' N87 material. This core's properties are suitable for operation in the application and at the selected frequency. The minimum number of primary side turns required to prevent core saturation were calculated so that a given maximum flux density (less than B_{SAT}) occurs in the core during operation at the maximum duty cycle.

Once the number of primary turns is known the secondary turns can be specified by using the required turns ratio. This ratio is determined by considering the specifications of the converter. Equation (4.2) gives the output voltage for an ideal forward converter where n_s and n_p are the number of primary and secondary turns respectively [4]. The maximum output voltage that the converter can output is then calculated by maximising this equation to yield Equation (4.3).

$$V_o = V_{DC}.\frac{n_s}{n_p}.D \tag{4.2}$$

$$V_{o,max} = V_{DC}.\frac{n_s}{n_p}.D_{max} \tag{4.3}$$

Solving for n_s/n_p, we see that n_s/n_p must be greater than 0.44 for the maximum output voltage requirement to be met in an ideal converter. Due to other voltage drops in the circuit (for example, the rectifier's forward voltage drops and resistive losses) this turns ratio will be increased to approximately 0.5. This gives some leeway and ensures that the maximum output voltage requirement can be met.

The primary was wound onto the transformer's bobbin first and consisted of 32 turns of 0.5 mm enamel insulated copper wire. The secondaries were then wound multi-filar and each consists of 17 turns of the same wire. Each winding was then tested for continuity and short circuits between different windings were checked for. No other tests were performed on the transformer at this time; it is tested further in-situ as part of the secondary side.

4.2.2.3 Output Capacitor Selection

The filter capacitor plays a large part in reducing the output voltage ripple present in the converter. This ripple can be estimated using Equation (3.16) which is repeated as Equation (4.4) [4].

$$\%\ Ripple\ Voltage = \frac{\Delta V_o}{V_o}.100\% = \frac{1}{8}.\frac{T_s^2.(1-D)}{L_F.C_F}.100\% \quad \textbf{(4.4)}$$

Equation (4.4) predicts that at least a 4 µF capacitor is required to limit the output voltage ripple to less than 2 % with the filter inductor described in the section below. However, it is difficult to find electrolytic capacitors with sufficient ripple current capabilities in the capacitance range. For this reason, 100 µF electrolytic capacitors with 290 mA_{RMS} ripple current ratings at 100 kHz were selected (Panasonic EEUFC1E101S).

Provision for a supplemental parallel connected metal film capacitor is also provided in each phase in the final design. However, this was not required in the final prototype.

4.2.2.4 Inductor Design

A coupled inductor, where all the phases are wound on a common core, is used in the multi-node converter secondary. This helps to reduce component counts, costs and size. An identical core to that used in the transformer was selected due to suitability and availability. The required number of turns for each phase can now be predicted once the required inductance per phase is known.

The required phase inductance is determined by two factors:

- The minimum inductance required to guarantee operation in the CCM. This is analysed in Chapter 3, Section 3.2.5.2.
- The minimum inductance required to limit the inductor's ripple current to less than the capacitor's ripple current specification.

In the prototype, the capacitor's ripple current specification resulted in the most challenging requirement for the filter inductance. This resulted in the final filter inductor being specified as 500 µH and this achieved by winding 26 turns per phase on the core with an air-gap of approximately 100 µm. The number of turns was determined from the core manufacturer's datasheet. The expected flux density was then calculated and it was found to be suitably below the saturation flux density for the material.

Continuity was then checked in each phase and short circuits between phases were tested for. If there are any other problems with the inductor they will be apparent during testing of the secondary side.

4.2.2.5 Selection of other Components

Schottky diodes will be used for rectifying each stage. They are used due to their low forward voltage drops and lack of reverse recovery. If standard ultra-fast diodes had been used their forward voltage drops would have been in the 0.7-0.9 V range. This results in significant efficiency losses when the output voltage is only 5 V. If Schottky diodes are rather used then the diode drop can be expected to

be in the 0.4-0.5 V range, this can result in a significant efficiency increase. MBR20100 Schottky diodes from International Rectifier were selected. These devices consist of two 10 A, 100 V Schottky diodes in one TO-220 package and are specifically optimised for use in switching converters.

The shunt resistor included in each phase (R_{CS1} - R_{CSn}) is composed of four 1.2 Ω resistors in parallel to yield an effective resistance of 0.3 Ω. The reason for paralleling multiple resistors is to increase the possible power dissipation for the shunt and also because 1.2 Ω resistors were the smallest resistors on hand when prototyping.

4.2.2.6 PCB design and Implementation

The layout of the final multi-node secondary PCB is shown as Figure 4.19. The main aim of the PCB design was to ensure that measurements could be taken as simply and easily as possible. For this reason numerous test points are provided and there has not been any attempt to minimise the physical size of the board as this would provide less space for working with probes and measurement equipment. This will not degrade the performance of the board significantly as minimising stray inductance is far less important on this board compared to the test platform. The only fast current commutations occur between the rectifiers. Minimising the stray inductance for this commutation is not critical due to the transformer leakage inductance swamping the stray inductance due to board layout anyway.

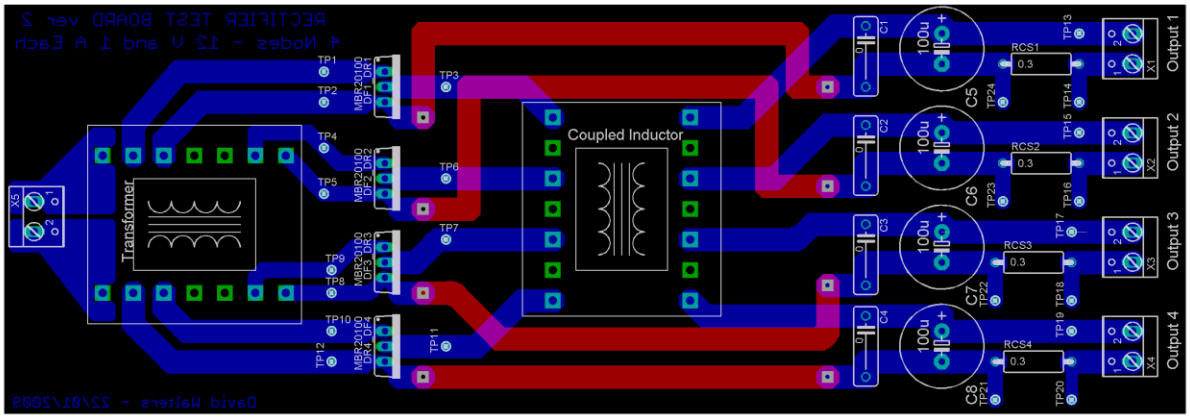


Figure 4.19: The multi-node converter secondary board's layout

The board was manufactured with a single layer and was then populated. The final prototype multi-node secondary is shown in Figure 4.20. The board's implementation is discussed further in Appendix B.

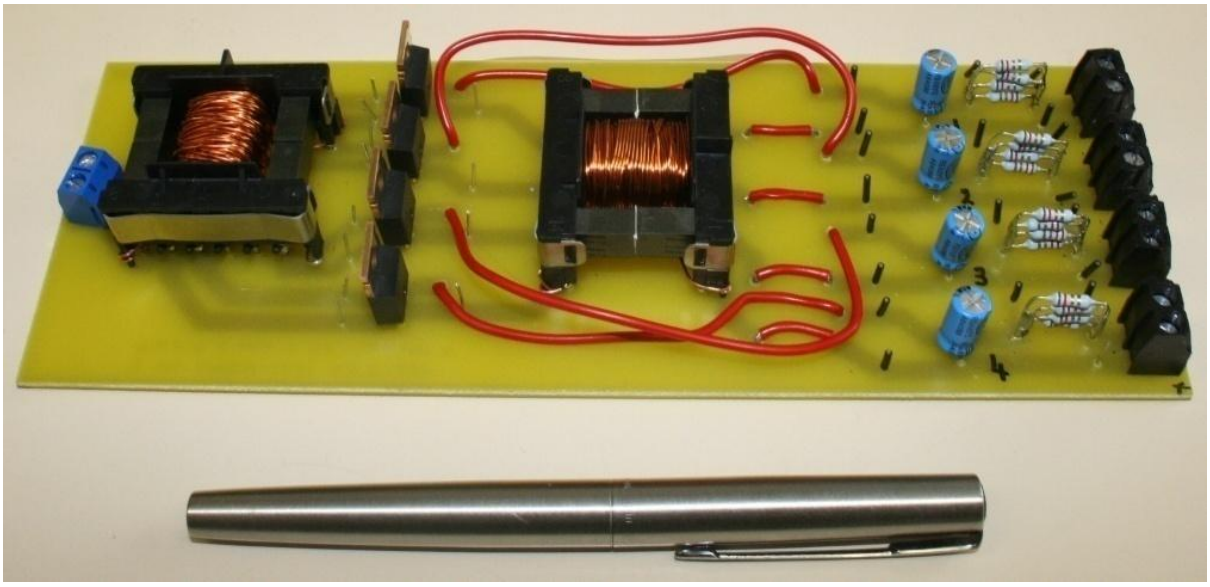


Figure 4.20: The multi-node converter secondary prototype

4.2.3 Testing

The test platform already described is now used to test the operation of the multi-node secondary. This section is focused on verifying the correct operation of the board and not with quantifying its performance, efficiency or current sharing. This is addressed in the next chapter, where the entire prototype is tested and evaluated as a whole.

One of the transformer's output voltages ($v_{t,1}$ from Figure 4.17) is shown in Figure 4.21. If this waveform is compared with Figure 4.12, then the transformer's action can be seen. The deviation from the ideal waveforms mentioned in Section 4.1.5.2 is also still present. A significant oscillation is also seen on the rising edge of the rectifier's voltage waveform. If we briefly look at the magnitude of the waveform we can see that the transformer's turns ratio is approximately half, which is expected. It is also worth noting that the outputs from the other phases are all very similar in form and magnitude to the representative waveform that is shown. This is also expected due to them being wound multi-filar and them being identical in every way that it was possible to make them.

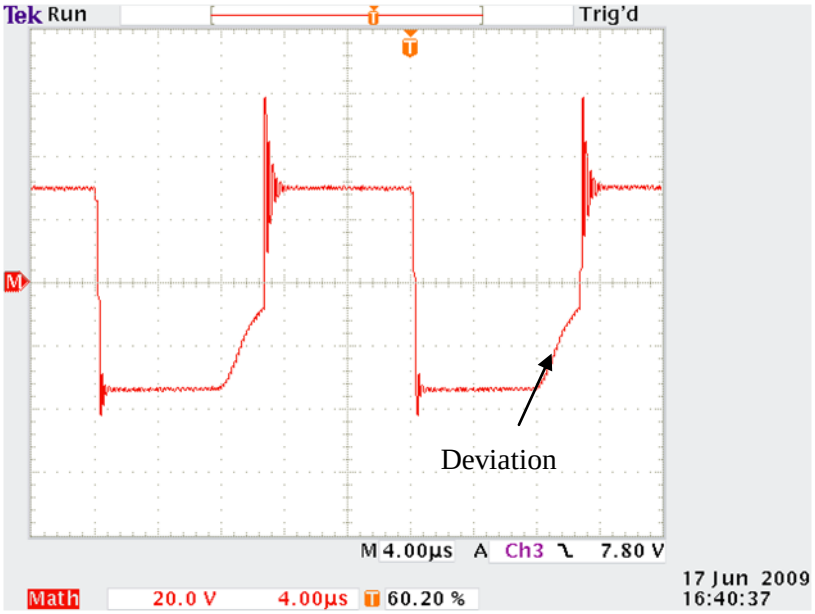


Figure 4.21: The transformer's output voltage

The transformer's output is then rectified and the rectifier's output ($v_{r,n}$ in Figure 4.17) for one phase is shown in Figure 4.22. We can see that Section 4.1.5.2's deviation has been removed by the rectification of the waveform and should have no effect on the output of the converter.

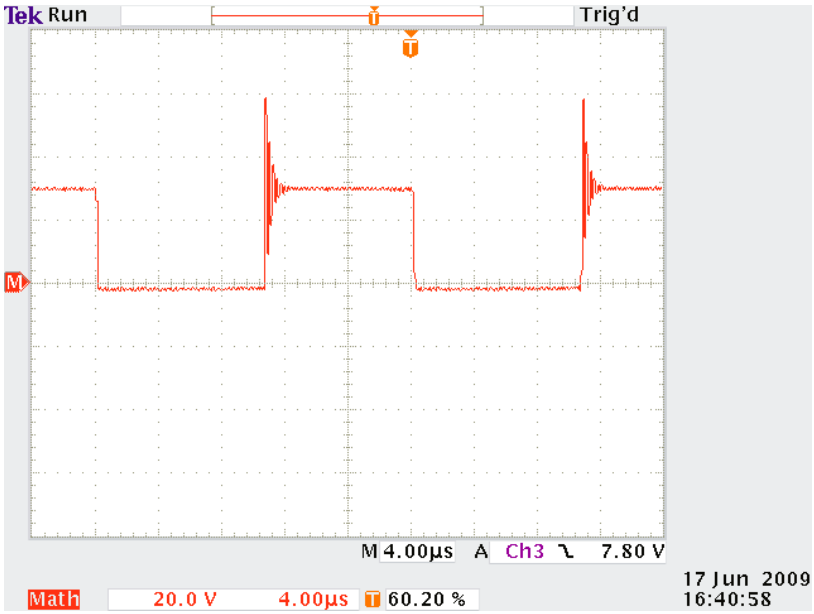


Figure 4.22: The rectifier's output voltage

The oscillation present on the rising edge of the rectifier's output voltage is still present and it is postulated that this oscillation also causes the oscillation seen in the primary side current (see section 4.1.5.3). This ringing is thought to be due to a resonance between the transformer's leakage

inductance and the rectifier stray capacitance [18]. Both the transformer's primary current oscillation and the rectifier's output voltage oscillation are shown in Figure 4.23. Both oscillations share the same starting time and frequency (measured as 9.26 MHz). This frequency is now compared with the predicted frequency of oscillation due to the transformer's leakage inductance resonating with the diode's stray capacitances.

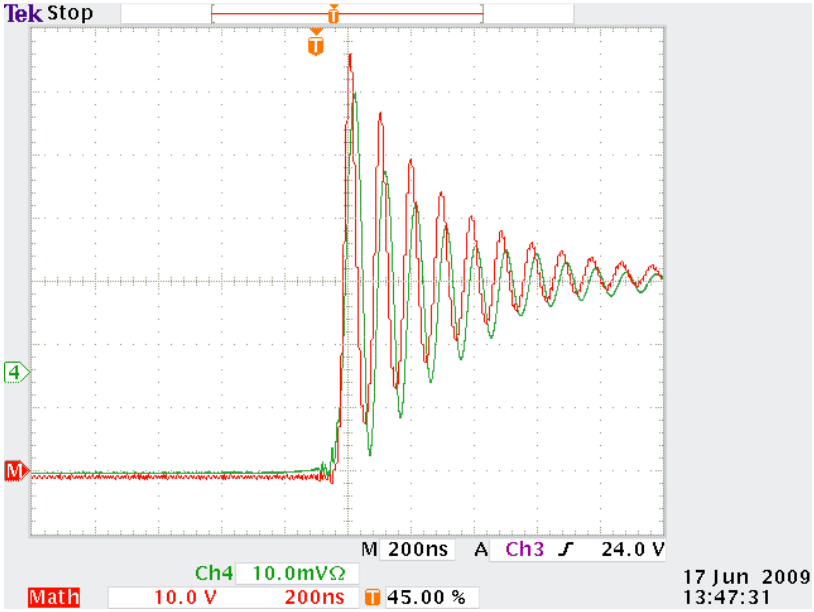


Figure 4.23: Transformer primary current (green at 200 mA/div) and rectifier output oscillation (red)

The transformer leakage inductance has been measured at as 2.86 µH and the rectifier manufacturer specifies a junction capacitance of approximately 120 pF (for a 35 V blocking voltage). Equation (4.1) predicts a natural frequency of oscillation of 8.6 MHz and a simulation predicts 8.54 MHz. Given the relative uncertainty in both the leakage inductance and diode capacitance values, we can say that the oscillation could be caused by a resonance between these components. Since the literature also points toward these two components resonating, we will conclude that this is the cause of the oscillation [18]. The oscillation does mean that the rectifying diodes require almost twice the blocking voltage that would be required if the oscillation was not present. If the prototype was meant to result in a final, production ready, design then removing the oscillation might be worthwhile. The literature also shows that the oscillation can be reduced by snubbing both diodes [18]. However this will not be done in this implementation as the glitch is not caused by or related to the focus of the research.

Finally, the output from one of the phases ($v_{o,n}$ in Figure 4.17) is shown in Figure 4.24. As expected, it is a clean DC waveform with low ripple. This is expected and is what was required. We also note that there is no longer any sign of the resonance seen on the rectifier output voltage. This is not surprising given that the low pass filter's 3 dB cut-off frequency is at 1 kHz and the resonance is in the megahertz range.

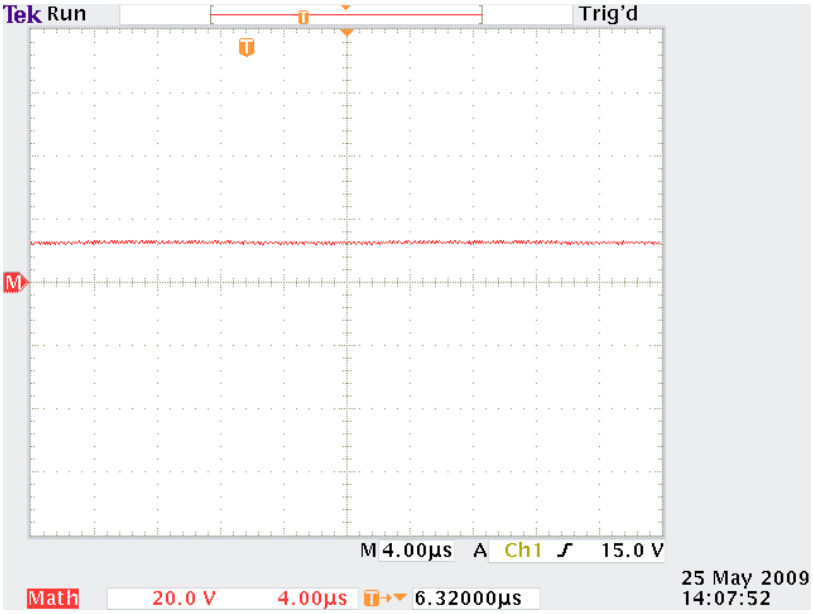


Figure 4.24: One converter secondaries output voltage

After testing the nodes at constant power it was found that the nodes could provide rated power (7.5 W) to the load over a range of 5 V to 13 V. This exceeds the specifications and means that the multi-node secondary will be suitable for use for evaluating the multi-node converter architecture.

4.2.4 Suitability for Use

The implementation of a four node secondary side has been discussed. The design and specification of the components in the secondary side was shown. The board's implementation was then discussed and finally the basic testing performed on the secondary side was detailed. Despite the converter deviating from its ideal waveforms, the converter's operation on the whole and its output is considered suitable for use for evaluating a multi-node converter prototype. It will therefore be used in the next chapter where the performance of the entire prototype is experimentally measured and quantified.

4.3 Distribution Board

The distribution board is a board that allows the outputs from the multi-node secondary board to be easily connected in various series/parallel configurations. It consists of eight switches, with which the four outputs from the secondary board can be combined in series, in parallel and in a series/parallel combination. It is worth noting that the distribution board is not essential for testing the converter. The prototype could have been tested by wiring the outputs from the multi-node secondary in the correct configuration. However, this makes changing configurations tedious and time consuming and so it was decided that a distribution board should be built.

Mechanical toggle switches were used in the board due to their simplicity. The switches are not required to switch quickly, repetitively or under load, which allows a mechanical switch to be used.

Relays, MOSFETs or IGBTs can be used in a final application, but this means that driver hardware has to be developed or purchased.

4.3.1 Circuit Description

The distribution board consists of multiple identical sub-circuits which allow each node's input source and output direction to be selected. A sub-circuit schematic is shown in Figure 4.25. The sub-circuit consists of an input connector (to which an output from the multi-node secondary is connected) and two single pole double throw switches. With this arrangement, the four nodes can be connected in any of the three possible configurations with four nodes, namely in series, in parallel and in series/parallel.

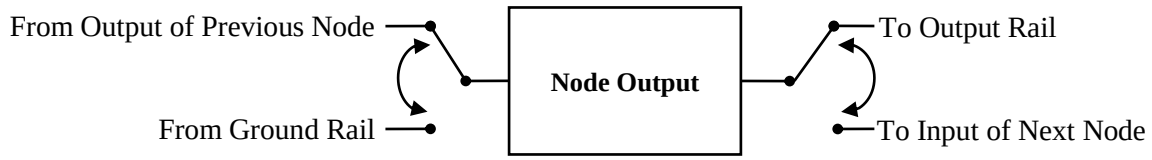


Figure 4.25: The sub-circuit schematic

4.3.2 Practical Implementation

The board was implemented on a single layer with the layout shown in Figure 4.26.

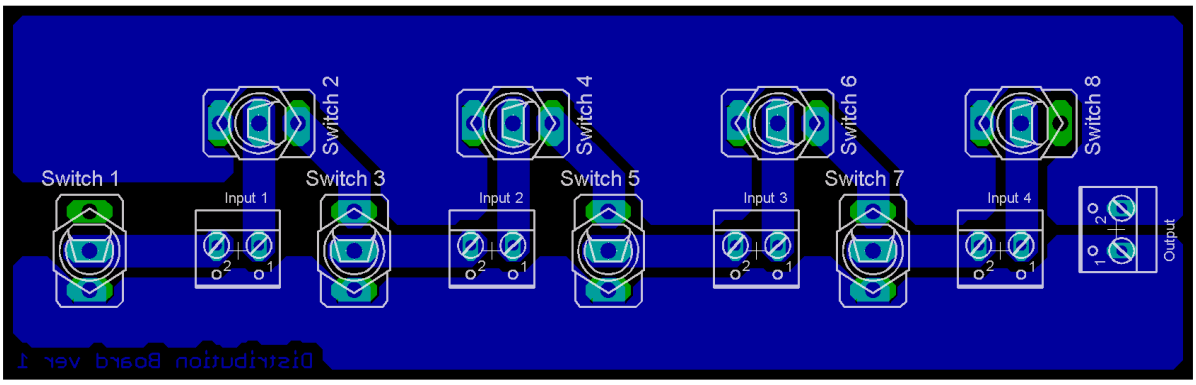


Figure 4.26: Distribution board layout

The circuit board layout has not been optimised for high frequency operation and stray inductance and capacitances have not been considered. This is not required in this board as only DC current flows in the switches and tracks (Except for a small ripple current). The track resistance is of far greater concern as this will have an effect on the DC current flowing in the tracks. For this reason large copper planes were used where possible and short, wide tracks were used elsewhere. The final PCB, once populated, is shown in Figure 4.27. The toggle switches and markings to indicate polarity can all be seen. It is also noted that one switch is missing and has been replaced with a wire (bottom left). This is because only seven switches were on hand and the first node does not require two switches

since it does not need to be connected to the input of any preceding nodes. The distribution board's implementation is described further in Appendix B.

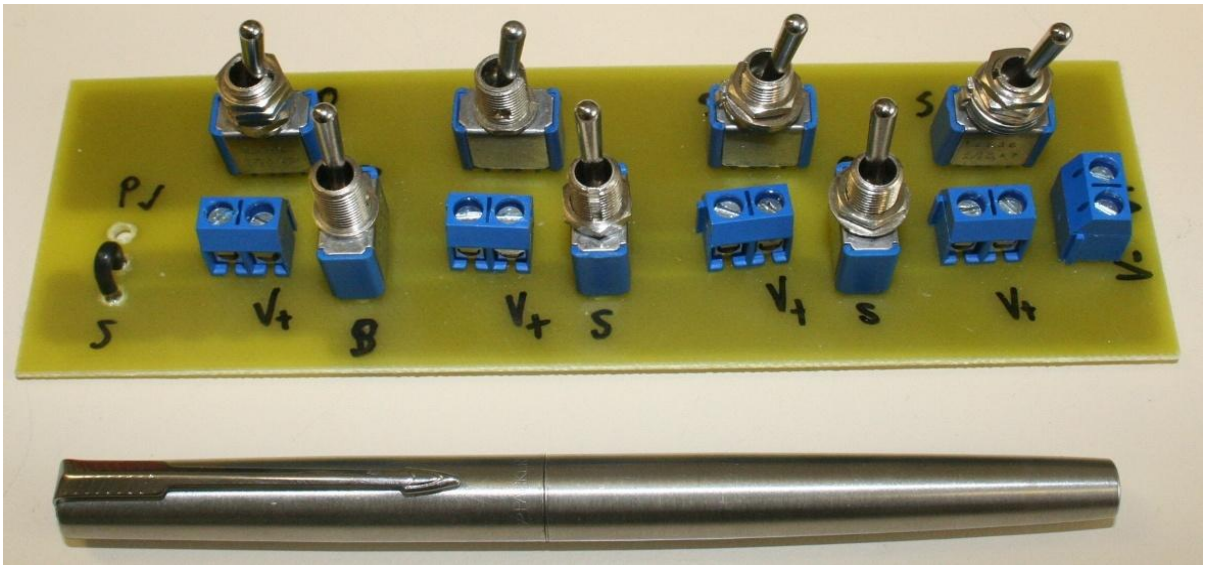


Figure 4.27: The prototype distribution board

4.3.3 Testing

The distribution board is simple in nature and did not require major testing to evaluate its suitability. The interconnections between the nodes was tested with a multi-meter to make sure no errors were made during the design or manufacturing of the board. None were apparent and so it was decided that the board would be used during testing. Any problems with the board would be apparent immediately during testing of the composite system.

4.3.4 Suitability for Use

The board was declared fit for use and is used during testing of the multi-node converter prototype.

4.4 Conclusion

The design, implementation and testing of the component parts of a multi-node converter prototype have been presented. How each subsection of the prototype was tested was also shown.

There were some deviations from ideal operation in the two-switch forward converter test platform and also in the multi-node converter secondary. Both of these were due to resonances between the transformer's leakage or magnetising inductances and stray capacitances in the semiconductors. Both of these resonances can be removed if desired but it was decided that it was not necessary given the focus of the research underway and the fact that these resonances do not affect the output or performance of the converter. Each part of the converter has thus been declared as fit for use for

testing a multi-node converter prototype. The next chapter evaluates and quantifies the performance and operation of the composite multi-node converter.

CHAPTER 5

EXPERIMENTAL TESTING OF THE MULTI-NODE CONVERTER PROTOTYPE

5.1 Introduction

The previous chapter used a theoretical understanding of multi-node converters and the proposed multi-node converter implementation presented in Chapter 2 and Chapter 3 to develop a multi-node converter prototype. The prototype's component choices were discussed and how it was implemented was shown. It then showed how each individual section of the prototype was individually tested and evaluated.

This chapter describes the testing of the multi-node converter prototype as a whole and also assesses the validity of the multi-node converter models that were presented in Chapter 3. The multi-node converter prototype will be operated at its specified output power (30 W) over its output range (48 V down to 6 V) and its output and efficiency will be measured. How the output current shares between the phases is also important and is experimentally measured.

The experimental results are then used to verify the theoretical models that were derived in Chapter 3. Since a current sharing mismatch is seen in the experimental results, this discussion is particularly relevant to the second theoretical model and it is focused on (since the first theoretical model cannot model current sharing mismatches). If the model is shown to be valid, then it will be a useful tool for designing, analysing and improving multi-node converter designs.

5.2 Experimental Setup and Theoretical Validation

This section describes the experimental setup that was used when testing the multi-node converter prototype and evaluating its performance. The connection and usage of measurement equipment is also described.

The second part of the section describes the procedure that was followed when validating the theoretical models used to predict the output and performance of the converter.

5.2.1 Experimental Setup

Figure 5.1 shows the experimental setup that was used for testing the multi-node converter prototype. The forward converter test platform, the secondary side and the distribution board have already been discussed in detail in Chapter 4. The three PCBs are connected and measurement equipment is added to the setup. This configuration will allow current sharing in the converter and the converter's efficiency to be experimentally measured.

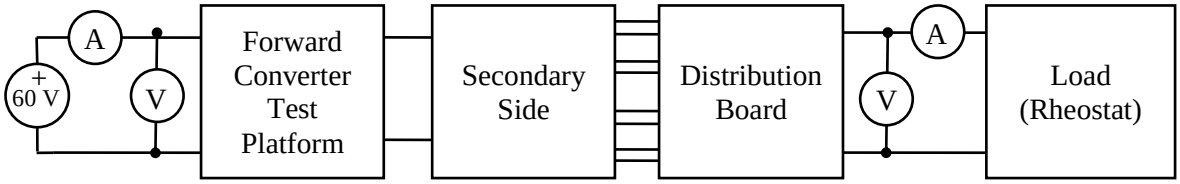


Figure 5.1: Experimental setup

In order to determine the converter's efficiency, its input power and output power must be measured. The efficiency is then the ratio of the output power divided by the input power. Measuring the input and output power for the converter can be difficult if high frequency current and voltage components are present on the input and output. Since the converter is a DC/DC converter this should not be the case. However, the input current waveform was measured using a Hall Effect current probe and a significant high frequency current component was seen (i.e. the input current contained significant current pulses). The DC bus capacitor in the two-switch forward converter was then replaced with a 1000 µF 63V electrolytic capacitor (it was originally a 68 µF 400 V electrolytic capacitor) and the input current was measured again. After replacing the capacitor, the input current no longer contained any significant HF components. The input and output power for the converter can thus be determined by measuring the input and output current and voltages using digital multi-meters. These are shown schematically as the ammeters and voltmeters in Figure 5.1.

The current that flowed in each phase was measured using the shunt resistors included in the multi-node converter secondary. The resistors are a known resistance and so measuring the voltage across each resistor allows the current through the resistor to be calculated. The accuracy of this measurement is dependent on how accurately the resistances are known and so some inaccuracy may result. However the resistors that were chosen were 5 % metal film resistors and this is considered sufficient for the measurements that will be taken.

While the experimental measurements were being taken, it was noted that the order in which the multi-meters were connected made a significant difference to the measurements. For example, if the voltmeter was connected after the ammeter on the output side, the voltage drop across the ammeter resulted in a measurement error that lowered the measured efficiency significantly (up to ten percent lower). This was particularly apparent when the converter was operated at a high output current with a low output voltage (e.g. 5 V output at 6 A). Figure 5.1 shows the correct order in which the multi-meters that measure current and voltage should be connected to prevent measurements errors due to the voltage drop across an ammeter. The orders are reversed on the input and output sides.

5.2.2 Theoretical Validation

Up until this point, the second theoretical model has not been verified and its validity was taken on faith. This chapter attempts to verify the theoretical model using the experimental measurements that were taken in the laboratory.

Figure 5.2 shows the converter model schematically.

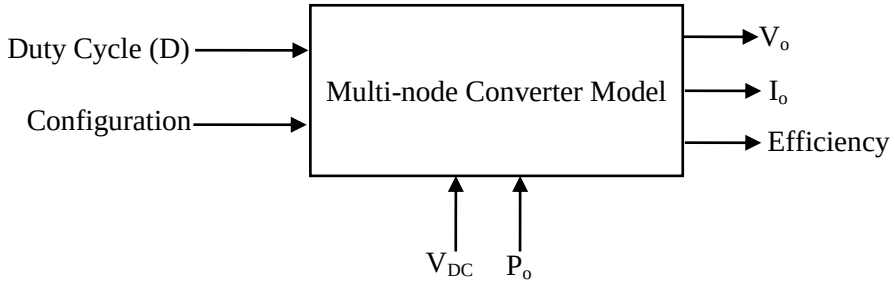


Figure 5.2: A schematic showing the converter model

The model accepts the current duty cycle (D), which configuration the converter is in (series, parallel or series/parallel), the DC bus voltage (V_{DC}) and the converter's output power (P_o). If the model is valid then it should be able to correctly predict the prototype converter's output voltage (V_o), output current (I_o) and efficiency.

However to correctly predict the converter's output and efficiency the model needs to know other information about the converter. This information consists of circuit parameters describing the operation of each component within the converter. These circuit parameters include, but are not limited to, the inductor's resistance for each phase, the primary side MOSFET's on-resistance and the forward voltage drops for each rectifier. If these parameters are correctly assigned and the model is valid, then the model should correctly predict the converter's experimental results.

If the model's predictions do not match the measurements taken on the prototype converter then either the measurements are inaccurate, the model is invalid or the model's parameters are incorrectly assigned (or any combination of the three). The problem with this procedure is although there is confidence in the practical measurements there is uncertainty with regard to the values of the circuit parameters in the model. For example, calculating the actual inductor resistance during operation of the converter is difficult due to many non-ideal magnetic effects. The skin effect [4], proximity effect [4] and fringing near the inductor's air-gap [20] all lead to significantly higher AC resistances in the windings and thus lead to higher losses than expected. This means that even if the converter model is valid and correct it may not accurately predict the behaviour of the prototype converter since the model's circuit parameters may be incorrect.

For this reason, it was decided that the problem would be rearranged from whether or not the model can accurately predict the experimental results, to whether or not the experimental results can be used

to predict the model's circuit parameters. These circuit parameters can then be compared to their expected values (datasheet values for standard components or calculated values for the custom magnetic components) and if an accurate correlation between the expected and calibrated circuit parameters is obtained then the model is as equally valid as if it was used to predict the output of the converter. If any discrepancies between the expected and calibrated circuit parameters are seen then the reason for these can be investigated and the validity of the model can be commented on pending this investigation.

The first step in verifying the experimental model is thus to calibrate the model such that it is able to simultaneously and accurately predict the output and efficiency of the converter prototype. This procedure involves fitting the output of the model to the practical measurements by modifying the circuit parameters within the model. The result of this calibration will be seen when the practical measurements are presented. How the model was calibrated will then be described after the experimental results have been presented.

5.2.3 Conclusion

The laboratory setup that was used to measure the multi-node converter prototype's output and efficiency, while it is operated over its output range, has been discussed. During testing the converter's efficiency, current sharing and output were measured. Simple digital multi-meters are used since the parameters that must be measured are DC waveforms that do not contain any significant high frequency components.

The procedure that will be used to validate the theoretical work that has been done on modelling the converter has also been presented. If the converter model is valid then it should be able to predict the output and efficiency of the multi-node converter prototype if its circuit parameters are accurately known. However, if the circuit parameters are unknown then a valid model should also be able to predict the circuit parameters using the experimental data. This is the procedure that will be followed and the validity of the model will be commented on depending on how accurately the model is able to predict its circuit parameters.

5.3 Experimental Results

This section presents the experimental results taken when testing the multi-node converter prototype in the laboratory. The converter's output range, how current shares between the phases and the converter's efficiency are all measured.

5.3.1 The Output Range

The multi-node converter was connected as per Figure 5.1 and measurements were taken over the output range. The output range that the converter was operated over is shown in Figure 5.3. The

converter's output voltage and current (and hence the output power) are controlled by varying the converter's duty cycle and the load resistance (using the rheostat). The resultant VI curve is a hyperbola since the output power is kept constant. The figure also shows the duty cycle that the converter operated at versus the output current. A change in the connection of the nodes can be clearly seen as a discontinuity on the duty cycle curve.

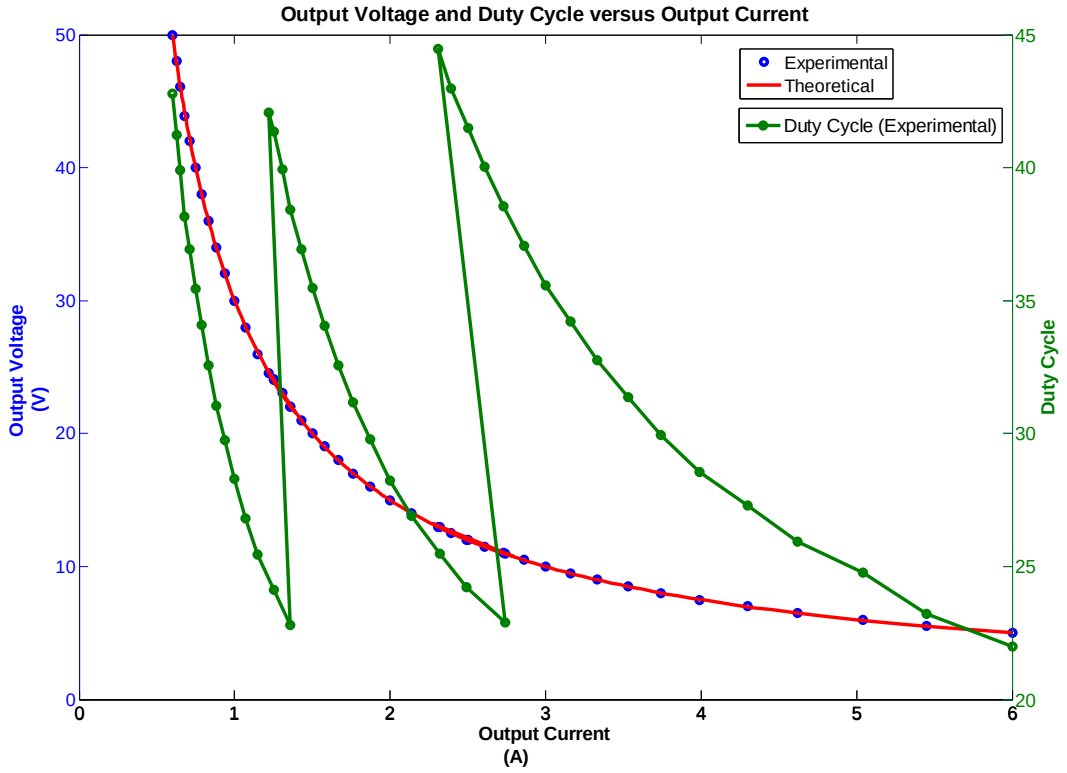


Figure 5.3: Output voltage versus output current showing a constant power output

The converter's output voltage is also plotted versus duty cycle for the constant output power. This is shown in Figure 5.4

From Figure 5.3 and Figure 5.4 it is clear that the converter's duty cycle is only modified over a two times range. This, combined with changes in the connections of the nodes, results in a ten times output range at constant power. The ten times output range is beyond the specification of the converter (an eight times range was specified).

Both figures also show the calibrated output from the second theoretical model. From Figure 5.4 we can see that the theoretical model is able to predict the converter's output voltage given the duty cycle. How the model was calibrated is discussed in Section 5.4.

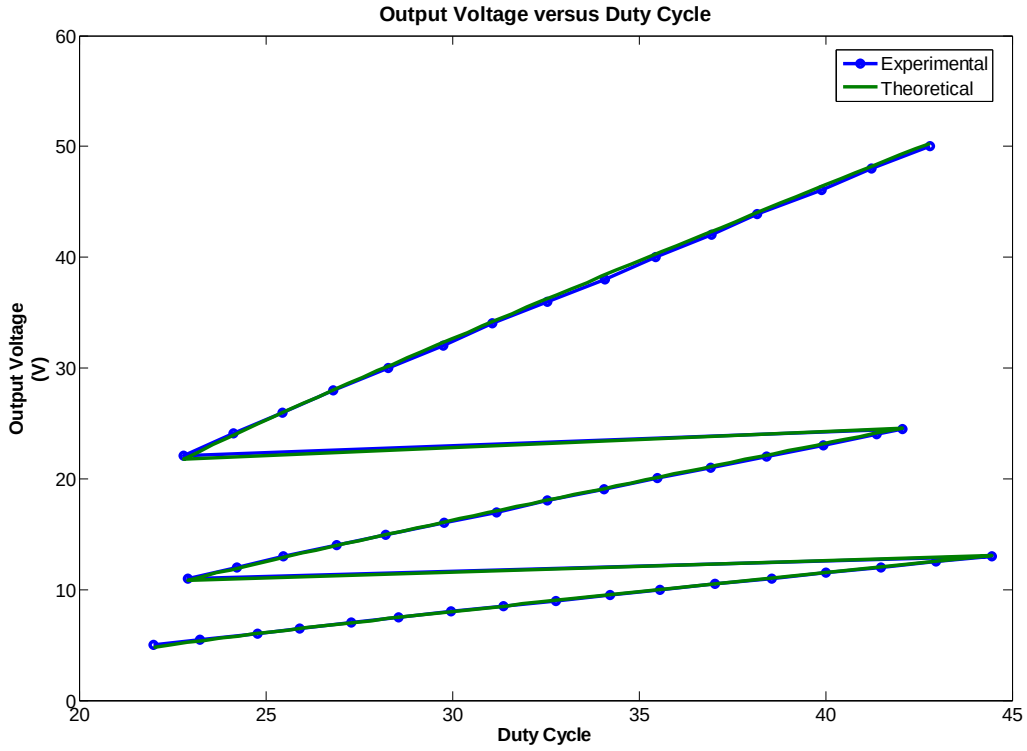


Figure 5.4: Output voltage versus duty cycle

5.3.2 Current Sharing

Figure 5.5 shows the current that each node sourced when the multi-node converter prototype was tested. At low output currents the nodes all output the same current. This is logical since the nodes are connected in series at this operating point and thus their output currents must be equal. The nodes are then connected in a series/parallel configuration and a 2 % current mismatch between the two series strings of nodes can be seen. The nodes are finally connected in parallel and each of the four node output currents are measured. The output current mismatch is seen to vary from 5 % to 7 % when the nodes are connected in parallel. This level of current sharing mismatch does not have any significant effects on lowering converter efficiency (<< 1 %). The biggest drawback to the current sharing mismatch is that that some level of over specification will have to be present in a multi-node converter secondary with imperfect current sharing. This is so that the phase that carries more than an equal share of the load current does not fail.

The current sharing mismatch is due to two main factors:

- Each phase has a slightly different leakage inductance and this leads to cross regulation errors (See Chapter 3, Section 3.2.4).
- Component variations between the phases. For example, each node may have differing inductor resistances, rectifier forward voltage drops, turns ratios etc.

Care has been taken to ensure that each phase's leakage inductance is as similar as possible. This was achieved by winding the transformer's secondaries multi-filar. A current mismatch will therefore be introduced in the multi-node converter model by varying the component parameters between the phases. This is discussed in Section 5.4.

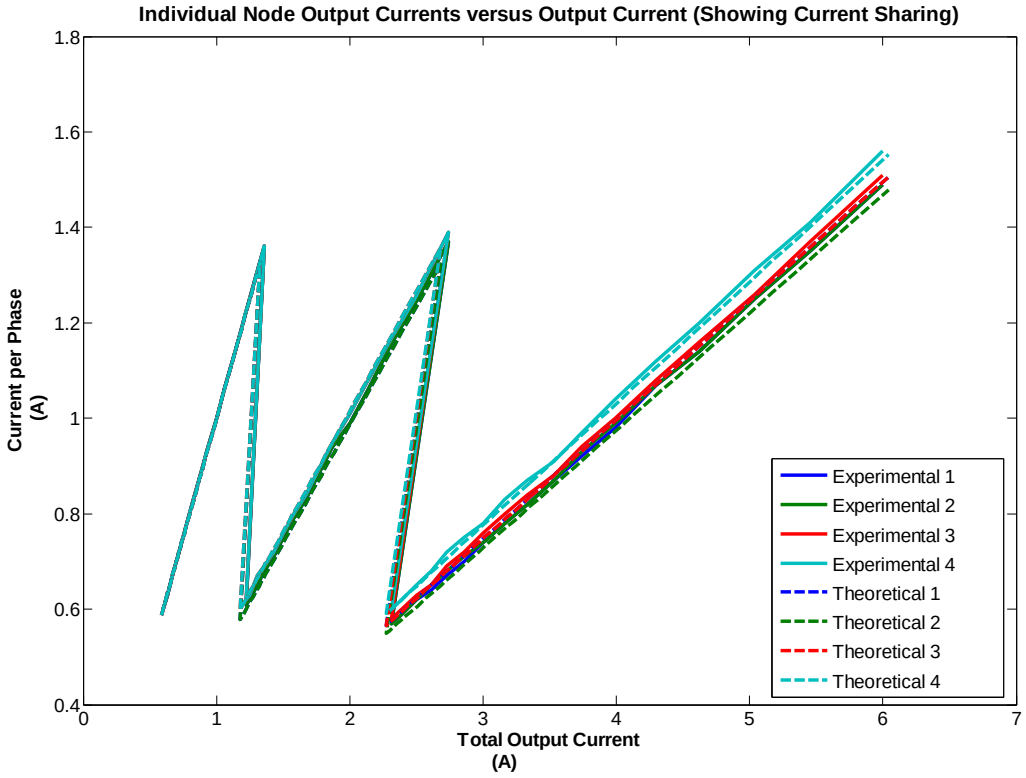


Figure 5.5: Individual node output currents versus converter output current showing current sharing

5.3.3 Converter Efficiency

Figure 5.6 shows the experimentally measured and theoretically predicted efficiency for the multi-node converter prototype. The converter's average efficiency (80.5 %) over the output range (0.6 A to 5 A) has also been calculated from the measured results and this is also indicated in the figure. The three converter configurations are clearly visible due to the discontinuities created when the configuration is changed.

The average efficiency is approximately ten percent lower than predicted in the comparative design in Chapter 3, however this is expected since the components that were used in the prototype converter are not optimised for high efficiency and were instead selected for a test platform application where the converter specifications were unknown.

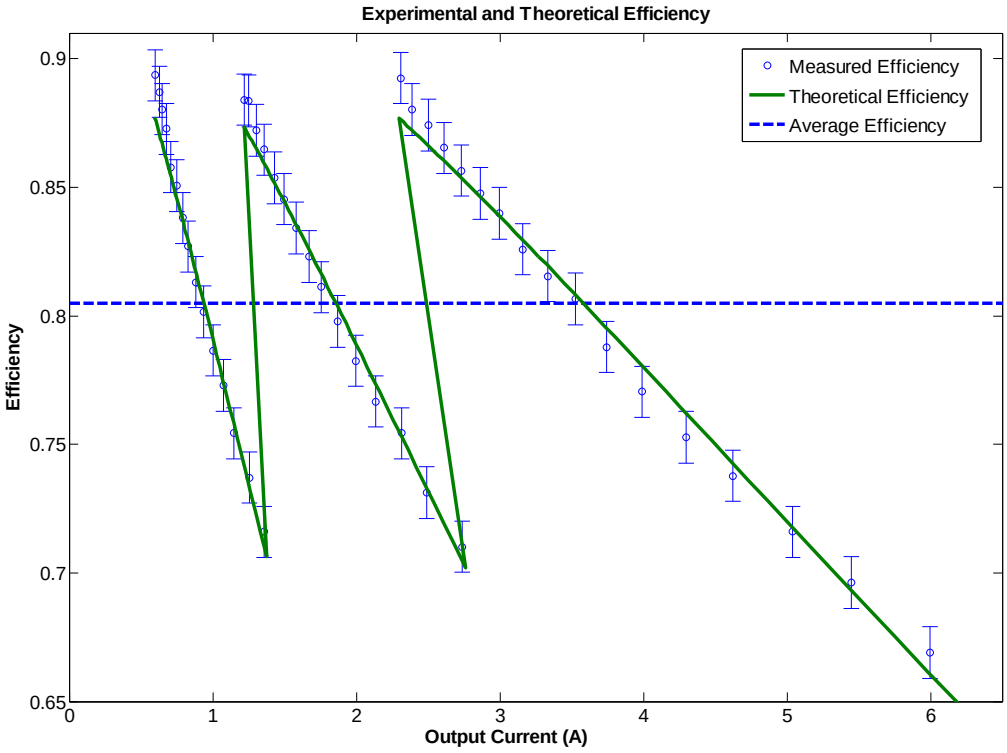


Figure 5.6: Experimental and theoretical converter efficiency

Error bars are also shown on the theoretical efficiency measurements. These error bars are based on the manufacturer's specifications for the multi-meters used to take the theoretical measurements. Fluke 45 multi-meters were used to measure current and their current accuracy is specified as 0.2 % for DC currents up to 10 A. The Fluke 73 III multi-meter that was used to measure voltage has a voltage accuracy specified as 0.3 %. These accuracies were used and a worst case efficiency error was calculated and used for the error bars.

The efficiency predicted by the calibrated converter model is also shown in the figure. The theoretically predicted efficiency curve does follow the experimental results. However there are some noticeable deviations from the predicted curve. These are most noticeable at higher efficiencies. This is discussed Section 5.4.

5.3.4 Conclusion

The experimental results that were obtained when testing the multi-node converter prototype have been presented in this section. The results show that the multi-node converter prototype was able to output constant power (30 W) over a ten times output range. Current sharing between the phases was also analysed and it was seen that current shared between the phases with a maximum mismatch of 7 % over the output range. This level of current mismatch does not have any significant effect on the performance or efficiency of the converter.

The converter's efficiency was then shown versus the output current. This graph consists of three roughly linear sections corresponding to the three converter configurations. The average efficiency seen over the output range was 80.5 %.

Each measurements curve also showed a theoretical prediction based on a calibrated multi-node converter model. The model was able to accurately predict the output of the converter given the duty cycle and also modelled current sharing mismatches between the nodes. The theoretically predicted efficiency did show some deviations from the measured values and these will be discussed in the next section where the model's calibration is discussed.

5.4 Model Calibration

This section describes the procedure that was used when calibrating the multi-node converter model such that it was able to accurately predict the experimental results taken on the prototype. How a current sharing mismatch was induced in the converter model is explained and why the predicted and measured efficiencies are not exactly the same is also discussed.

5.4.1 Calibration Procedure

Calibrating the converter model involves assigning each circuit parameter such that the model's output matches the experimental output and efficiency curves with the lowest possible error. This could have been achieved using an automated procedure or optimisation algorithm. For example, a Genetic Algorithm or another modern optimisation algorithm could be used to optimise each of the circuit parameters. However it was decided that implementing one of these algorithms would have been more difficult than calibrating the model manually since the model only needed to be calibrated once. The model was thus manually calibrated.

Before manual calibration of the model could begin it was important that each parameters effect on the output of the converter and its efficiency was fully understood. For example, increasing a resistive parameter (either the inductor's resistance, the MOSFET's on-resistance, the output resistance or the transformer's equivalent resistance) results in a steeper efficiency-current curve and also causes the voltage-duty cycle curve to steepen. Meanwhile, increasing the rectifier forward voltage drop results in a steeper efficiency curve but has very little effect on the slope of the voltage-duty cycle curve. Once the effect of each and every circuit parameter was understood the model's calibration was started.

The circuit parameters were initially set to their expected values (shown in Section 5.5). The resultant efficiency predicted by the converter is shown in Figure 5.7. The figure shows that the converter model initially predicted an efficiency curve with a slope that was too low. The slope of the voltage-duty cycle curve was also to shallow and together with the efficiency curve this indicated that a resistive parameter needed to be increased. Of the four resistive terms, the inductor and transformer

resistances are known with the least accuracy and thus these were increased. This procedure was then repeated, where the output and efficiency curves were analysed and incrementally modified by changing the relevant parameters. Once calibration was complete the theoretical results already presented were predicted by the model.



Figure 5.7: Efficiency versus output current before and after calibrating the converter.

5.4.2 Inaccuracies in the Calibration Procedure

One question that must be posed during the calibration procedure is whether or not only one unique set of circuit parameters results in the model matching the experimental results. Answering this question depends on whether or not each circuit parameter has a unique and measurable effect on the measurements that are taken. For example, it was mentioned previously that increasing a resistive parameter in the model tends to steepen the slope of the converter's efficiency curve and its voltage-duty cycle curve. However, increasing the rectifier's forward voltage drop steepens the slope of the efficiency curve but has very little effect on the voltage-duty cycle curve. Due to this difference the effect of the resistive components can be separated from the effects of the rectifiers.

The problem occurs when trying to differentiate between parameters that have the same effect on the measured results. For example, how does one separate the effect of the inductor's resistance and the effect of the output resistance? These are serially connected resistances that have an almost identical effect on the output of the converter (the only difference is that the inductor carries current with a significant ripple. At higher duty cycles, close to D = 0.5, the ripple current magnitude is greater and leads to slightly lower efficiency since the inductor's RMS equivalent current increases relative to its

DC current). The solution here is to decide on how confidently one can predict each of the resistive terms. The output resistance's value can be measured and thus when calibrating the model this terms is known with a high level of confidence. If the experimental results show that either the inductor or output resistance needs to be increased to calibrate the model, then the inductor resistance would be increased. This principle, where the confidence in each parameters value is evaluated before deciding which parameter to change, is used throughout the calibration procedure.

Other parameters are extremely difficult to evaluate unless other measurements are taken. For example, as long as the converter stays in the CCM, the filter inductor's value has a small effect on the converter's efficiency and output. For this reason its value cannot be determined from these measurements. This is equally true for the transformer's magnetising inductance. As long as the magnetising inductance is large (such that the transformer's magnetising current is small compared to the total primary current) its effect on the converter's efficiency and output is negligible. For this reason these parameters were specifically measured.

Even after measuring the parameters that can be measured, it is difficult to separate the effects of some of the components. The main culprit in this regard is how to differentiate between the inductor and transformer resistances and their effects. This is a problem and it is likely that it will lead to some error in the calibrated transformer and inductor resistance values.

5.4.3 Modelling the Current Sharing Mismatch

The current sharing mismatch seen in the multi-node converter prototype's testing was modelled theoretically by varying the circuit parameters for each of the four phases. The circuit parameters that were used in each phase are shown in Table 5.1.

Table 5.1: Model parameters for inducing a current sharing mismatch

	Output Resistance[2]	Indutor Resistance	Rectifier Forward Voltage
Node 1	0.33 Ω	0.4 Ω	0.60 V
Node 2	0.34 Ω	0.4 Ω	0.61 V
Node 3	0.33 Ω	0.4 Ω	0.60 V
Node 4	0.32 Ω	0.4 Ω	0.58 V

The table shows that node four has been modelled with a lower rectifier forward voltage drop and output resistance. Node two has a highest output resistance and rectifier voltage. This causes node four to output a higher voltage than the other nodes and results in it sourcing a higher output current when it is paralleled. Similarly, node two sources the least current. The result of the component variations that were introduced is that the node output currents show a mismatch of approximately

[2] This resistance includes the resistance of any switches used to change the configuration of the converter.

7 % or the same seen in the experimental results. This is visible in Figure 5.5, where the theoretically predicted and experimentally measured current in each phase are plotted.

5.4.4 Efficiency Prediction Mismatches

From Figure 5.6 there are some deviations between the experimentally measured and theoretically predicted converter efficiency curves. The largest deviation tends to occur at higher efficiencies where the measured efficiency is noticeably higher. Figure 5.8 shows the difference between the experimentally measured efficiency and the theoretically predicted efficiency on a logarithmic current axis. The logarithmic axis normalises the width of each difference curve and reveals a pattern in the difference curve. All three curves (for the three different configurations) follow a trend where at low node output currents the difference is high in magnitude but negative. The magnitude of the difference then decreases before becoming positive in the middle of each curve. Finally, the magnitude of the difference drops and becomes negative at high node output currents.

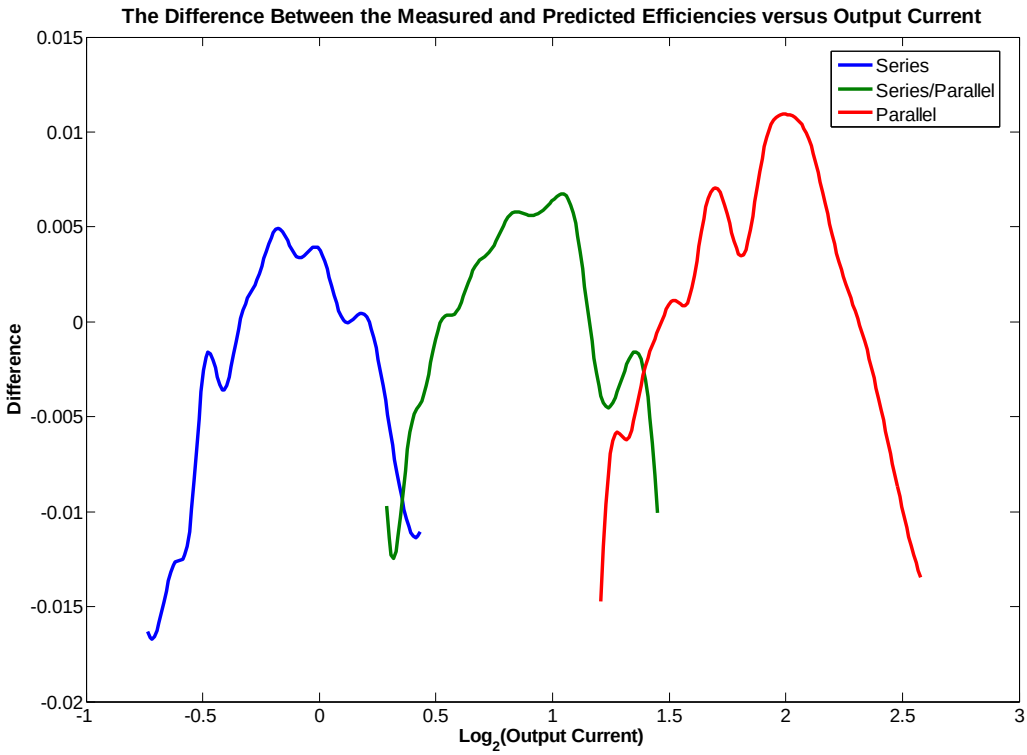


Figure 5.8: The difference between the experimentally measured and theoretically predicted efficiencies versus $\log_2(I_o)$

The reason for this trend in the difference curves is seen by considering the measured efficiency in Figure 5.6 and how the marked data points are positioned relative to the predicted efficiency curve. The raw efficiency measurements and the curve predicted by the model actually arc in different directions. I.e. if the raw efficiency measurements follow a slightly concave arc then the theoretical efficiency curve is convex. This is unlikely to be the result of experimental error or inaccuracies with

the measurement equipment since this is a trend that is seen and is repeated for all three nodal configurations.

For this reason the difference between the curves is likely to be due to a mistake in the models derivation and implementation or due to inaccuracies introduced by the model's assumptions and simplifications. Since the two theoretical models that were developed were consistent it is likely that the different between the measured and theoretical predictions is caused by assumptions made when developing the model.

It is suggested that the difference seen in Figure 5.8 could be explained by the circuit parameters changing depending on the output. For example:

- The converter's rectifiers (D_{Rn} and D_{Fn} from Figure 3.1) were modelled as having a constant forward voltage drop. Given that rectifier's current changes, this assumption is not strictly true and the diodes forward voltage drop would be lower when a node's output current is low.
- As a node's output current increases the DC current that flows in that node's inductor must also increase. This causes higher inductor losses and causes the temperature of the inductor windings and their resistance to increase.
- The transformer and inductor core losses also vary slightly with output. At high duty cycles, the transformer encounters higher peak AC flux densities and this results in higher core losses. At the same time, the ripple current in the output inductors is higher and results in higher peak AC flux densities in the inductor and thus higher inductor core losses. When this was investigated it was found that, although true, the effect on the efficiency curve was negligible for the prototype converter.

In order to test these hypotheses, and their effects on the performance of the converter, the second theoretical model was modified such that the rectifier forward voltage drop and the inductor and output resistances could be modified during the operation of the converter. The result of these new simulations is shown in Figure 5.9. The figure shows the converter's efficiency in the parallel configuration versus output current and predicts the effects of changing the rectifier's forward voltage drops and the inductors' resistances. The rectifier's forward voltage is linearly modified from 0.6 V to 0.45 V and the inductor's resistance is decreased linearly by 20 % over the range.

Changing the component parameters over the output range resulted in the model predicting higher efficiencies at low output currents. This matches the trend seen in the multi-node converter's experimental results and by careful calibration of the component parameters and how they change over the output range, the theoretical efficiency curve could be better matched to the experimental results.

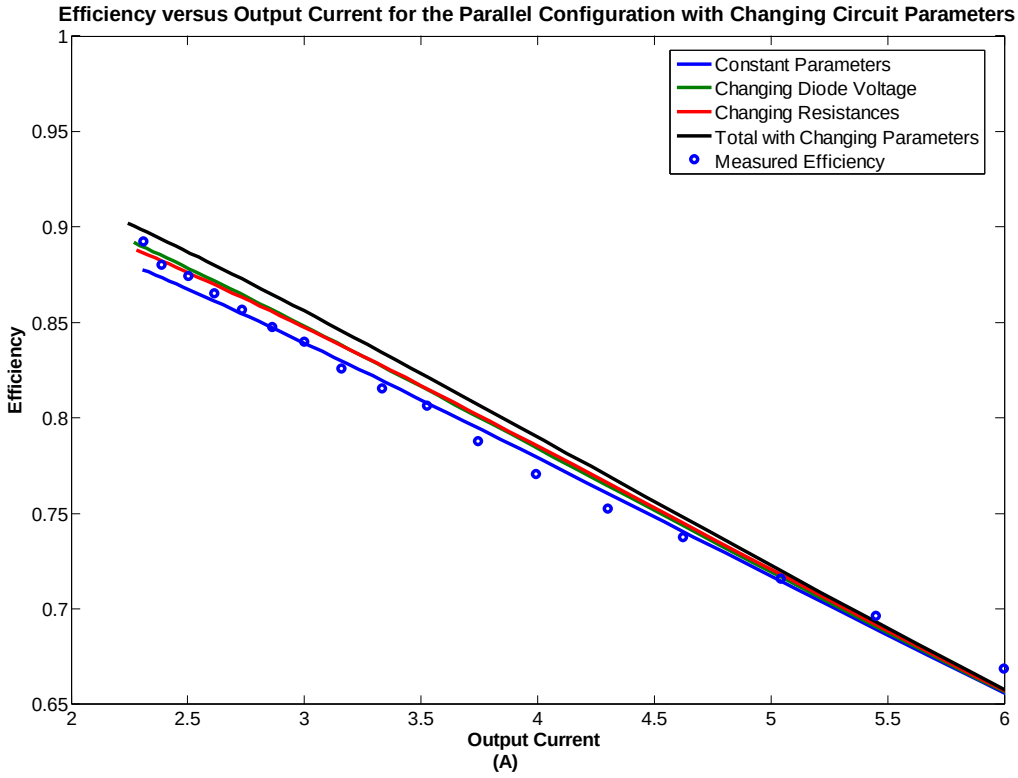


Figure 5.9: Predicted efficiency curves with changing circuit parameters

5.4.5 Conclusion

Various aspects regarding the calibration of the second multi-node converter model have been presented in this section. The second multi-node converter model was calibrated manually since implementing an optimisation algorithm would have been more difficult than manually calibrating a single model. How the effect each circuit parameter has on the converter's output and efficiency was used to calibrate the model was then briefly discussed. Whether or not the calibration procedure results in a unique set of calibrated circuit parameters was also addressed.

It was also noted that it is difficult to calibrate parameters when two or more different circuit parameters have exactly the same effect on the output and efficiency of the converter. In this situation, the circuit parameter that is known with the least certainty was generally modified.

The experimental results also showed a current mismatch between paralleled phases. This current mismatch was reproduced in the theoretical model by varying the output resistance and rectifier forward voltage for the different phases.

A discrepancy between the model's predicted and theoretical efficiency was then addressed. The experimental results showed higher efficiencies than predicted at high duty cycles and it was postulated that this was due to the converter's circuit parameters changing depending on the output. The theoretical model was then modified such that the rectifier forward voltage, inductor resistance

and output resistance could be modified during operation of the converter. This model reproduced the same trend seen in the experimental results and it was thus concluded that changing circuit parameters were responsible for the discrepancy seen between the experimental and theoretical efficiencies.

Now that the model's calibration has been discussed, it is possible to present and compare the expected and calibrated circuit parameters. This is the subject of the next section.

5.5 Circuit Parameter Comparison

Now that the multi-node converter model's calibration has been discussed, its circuit parameters will be compared with their expected values. If the circuit parameters show good correlation with their expected values then it will be concluded that the model is valid. However, if any discrepancies are present between the expected and calibrated circuit parameters then these discrepancies will need to be investigated. Whether or not it is concluded that the multi-node converter model is valid or not will then depend on these investigations.

5.5.1 Comparison between the Expected and Calibrated Circuit Parameters

The expected and calibrated circuit parameters are shown in Table 5.2. How the expected value for each parameter was determined is also indicated in the last column. The table shows that most of the calibrated circuit parameters are in fact equal to their expected values. There are however some deviations, with the magnetic components showing the greatest difference between their expected and calibrated parameter values. The differences between the expected and calibrated circuit parameters are now discussed in the following section.

Table 5.2: Calibrated and expected parameters for the multi-node converter model

Parameter	Symbol	Expected Value	Calibrated Value	Difference (%)	Source
Power-train resistance	r_{pt}	< 0.1 Ω	0.035 Ω	0 %	Estimated
Output Resistance	r_o	0.33 Ω	0.32 Ω - 0.34 Ω	0 %	Measured
Inductor resistance	$r_{L1} – r_{L4}$	0.1275 Ω	0.40 Ω	+213.7 %	Calculated
The filter inductor's inductance	$L_{F1} – L_{F4}$	440 µH	440 µH	0 %	Measured
Inductor core losses	L_{core}	0.016 W	0.016 W	0 %	Calculated
Primary side MOSFET on-resistance	$r_{ds(on)}$	0.27 Ω	0.27 Ω	0 %	Datasheet
Primary side MOSFET switching time	t_{on} and t_{off}	80 – 130 ns	100 ns	0 %	Datasheet
MOSFET output capacitance	C_o	480 pF	480 pF	0 %	Datasheet
Transformer winding resistance	r_{cu}	0.251 Ω	0.35 Ω	+39.4 %	Calculated
Transformer magnetising inductance	L_{mag}	3 mH	3 mH	0 %	Measured
Transformer turns ratio	$n_1 – n_4$	17/32	17.3/32	+1.8 %	Calculated

Transformer core losses	T_{core}	0.16 W	0.16 W	0 %	Calculated
Rectifier diode forward voltage drop	v_d	0.55 – 0.6 V @ 2 A	0.58 – 0.61	1.67 %	Datasheet

5.5.2 Analysis of the Circuit Parameter Mismatches

This section analyses and explains why mismatches are seen between the expected and calibrated circuit parameters in the multi-node converter model.

5.5.2.1 The Inductor Resistance Mismatch

The inductor resistance predicted by the calibrated circuit model is 213.7 % greater than the expected inductor resistance. The inductor's equivalent resistance is difficult to predict due to many non-ideal effects. The skin effect [4], proximity effect [4] and losses due to fringing flux from the gapped core passing through the windings all lead to higher than expected losses in the inductor [20].

The skin effect has been mitigated by selecting wire with a diameter less than the skin depth of copper at the switching frequency. However the triangular current waveform that flows in the inductor does contain higher frequency components. The skin depth for these components will be less than the radius of the windings and will affect the effective AC resistance of the winding. However, the skin effect is unlikely to influence the AC resistance of the winding as much as the Proximity effect which is described next.

The proximity effect occurs when current carrying conductors are placed in close proximity to one another (such as in the inductor's windings). The current flowing in one wire creates a magnetic field which induces eddy currents in nearby windings. Dowell [21] developed an analytical solution for predicting how the AC resistance of a winding changes depending on the number winding layers, the skin depth of the conductors and their heights. After analysing normalised power dissipation curves for windings based on Dowell's work and presented by Mohan [4], it is predicted that the AC resistance of a prototype converter's winding could be as much as two to three times as much as the inductor's DC resistance. In future multi-node converters, where coupled filter inductors are used, it may be worthwhile if every second phase was wound in the opposite direction. This will help to reduce the MMF within the winding window and will reduce proximity effect losses at the expense of increased complexity for the windings. This is similar to how a transformer's primary and secondary side windings can be sectioned and interleaved to reduce the transformer's proximity effect losses and leakage inductance [4].

The inductor's losses are also influenced by fringing flux near to the core's air-gap passing through nearby windings. Any perpendicular component (perpendicular to the direction of current flow) of this flux that passes through a winding causes localised eddy currents and thus conduction losses in

the winding. Predicting this loss component is difficult and most authors resort to Finite element Modelling (FEM) [22]. However some authors have developed analytical models for predicting this loss [23]. Techniques for reducing this loss include using a distributed (or quasidistributed) air-gap instead of a single lumped air-gap [22] and also shaping the windings near to the air-gap such that they are less influenced by fringing flux [24]. These techniques were not used in the multi-node converter prototype's inductor and the losses caused by the fringing flux intersecting the windings will have an effect on the inductor's losses.

The three effects that have been discussed were not included when calculating the expected inductor resistance. The proximity effect alone is sufficiency to explain the increased winding resistance predicted by the calibrated circuit model and thus it is concluded that the calibrated inductor resistance is a reasonable value for the prototype converter's inductor.

5.5.2.2 The Transformer Resistance Mismatch

The transformer's winding resistance in the calibrated model is 39.4 % greater than expected. This increased winding resistance can be explained by many of the same phenomena discussed for the inductor. The losses caused by fringing flux interacting with the windings is less of a concern in the transformer since its core is not gapped, however the skin and proximity effects are still relevant and cause higher than expected AC resistances in the transformer windings. This can explain the mismatch seen between the expected and calibrated transformer resistances and similarly to the inductor resistance, it is concluded that the transformer's calibrated resistance is a reasonable value.

5.5.2.3 Other Mismatches

The rectifier forward voltage drop and turns ratios predicted by the calibrated model also show a slight mismatch from their expected values (1.67 % and 1.8 % respectively). These mismatches are not significant and are explained by component tolerances.

5.5.3 Analysis

The expected and calibrated circuit parameters for the multi-node converter model have been compared and some discrepancies were found. The largest discrepancy was for the inductor resistance. It was noted that the inductor's expected resistance was simply based on its DC resistance and other non-ideal effects were not included. Three different non-ideal effects were discussed (the skin effect, the proximity effect and losses due to fringing flux intersecting the windings) and it was concluded that the large discrepancy between the expected and calibrated inductor resistance was due to these effects.

The transformer's resistance was then discussed and it was also concluded that non-ideal magnetic effects were responsible for the discrepancy between the expected and calibrated transformer

resistance. The skin and proximity effects are responsible in this case, while fringing flux is not as much of a concern due to the core not having a gap.

There were no other significant discrepancies between the expected and calibrated circuit parameters and since explanations have been given for the differences that were seen it is concluded that the multi-node converter model appears to be valid. It is however difficult to conclude this with absolute certainty until further work is done on accurately predicting the transformer and inductor resistances. If it can be shown, through analytical or numerical methods, that the inductor and transformer resistances are in fact expected to be equal to their calibrated values then the model's validity would have been shown. This is recommended as future work.

5.5.4 Conclusion

The converter model was calibrated such that it was able to predict the experimental results taken on the multi-node converter prototype. After calibration, the model was able to simultaneously predict the output and efficiency of the multi-node converter prototype with reasonable accuracy given the assumptions made when developing the model.

Once the model had been calibrated, the expected and calibrated circuit parameters were compared. The majority of the circuit parameters were equal or close to their expected values. However, it was found that a large mismatch was present between the expected and calibrated inductor and transformer resistances. This mismatch was attributed to non-ideal effects in the magnetic components such as the proximity and skin effects.

The theoretical model, once calibrated, was able to predict the output and efficiency for the multi-node converter prototype. However, due to the mismatches seen between the theoretical and expected circuit parameters it is difficult to conclude that the model is valid with certainty. What is recommended is that the expected inductor and transformer resistance values should be revisited in future work. However, given that valid reasons for the mismatch have been found, it does appear that the model is valid and can be used to further analyse and optimise multi-node converter designs based on the proposed implementation.

5.6 Conclusion

This chapter presented the experimental testing of the multi-node converter prototype. The experimental setup was presented and the general strategy that would be followed for validating the theoretical converter model was discussed. This strategy was to calibrate the model such that it replicated the experimental data in terms of both output and efficiency. The calibrated circuit parameters that were required to reproduce the experimental output with the model could then be compared and verified with their expected values. If these corresponded then the model's validity would have been demonstrated.

The experimental measurements taken on the multi-node converter prototype were then shown. The converter was operated over a ten times range with a constant 30 W output power. The converter's efficiency and how well current shared between its phases was then measured. It was found that the current shared with a mismatch of less than 7 % over the output range. This level of current mismatch would not result in any significant efficiency losses in the converter. The converter's experimental efficiency was then presented. The converter's average efficiency over the output range (80.5 %) was significantly lower than the efficiency seen in the comparative design presented in Chapter 3. This is because the multi-node converter prototype is not optimised for efficiency and is rather a test platform.

The multi-node converter model was then calibrated such that its output matched the experimental results. How the model was manually calibrated was discussed and it was noted that this procedure may not result in a unique set of calibrated circuit parameters when two or more parameters have the same effect on the model's output. How this was addressed was then explained.

The current sharing mismatch seen in the experimental results was then reproduced in the converter model by varying the circuit parameters between phases. The experimental results also showed higher than expected efficiencies at lower node currents (i.e. higher converter duty cycles). It was postulated that this is caused by the converter's circuit parameters changing depending on the output of the node. The converter model was then modified such that each node's rectifier forward voltage, inductor resistance and output resistance could be modified depending on the output of the node. This resulted in the same trend seen in the experimental results (higher efficiency at low node output currents) and it was concluded that with careful calibration of the circuit parameters and how they change depending on each node's output, the experimental results could be reproduced with the converter model.

The final step in validating the converter model was to compare the expected and calibrated circuit parameters. Most of the circuit parameters did correspond, however significant mismatches were seen in the inductor and transformer resistances. This was analysed and it was concluded that these discrepancies were due to the skin effect, the proximity effect and fringing flux entering the windings. These non-ideal effects do explain the discrepancies seen, but are unfortunately difficult to predict in practical magnetic components. If further verification of the converter model is required then these non-ideal effects in the magnetic components should be accounted for. This will allow the model's validity to be verified with certainty.

Despite this, valid reasons for the mismatches seen in the expected and calibrated circuit parameters were found. The converter model was also able to match the experimental results and so it does appear that the model is valid and it is a valuable tool for optimising and evaluating multi-node converters based on the proposed implementation.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

When a traditional converter topology is used to output constant power over a wide output range, its components cannot be effectively utilised throughout the output range. This is fundamental since the stresses imposed on the components vary directly with the output of the converter. This can result in the components, and specifically the passive components in the converter, being heavier, larger and more expensive than if they were better utilised. What is required is a method whereby the stresses the components are exposed to may be partially decoupled from the converter's changing output.

Multi-node converters were developed as a solution to this problem. They consist of multiple smaller converters, or nodes, that are placed within a mesh of switches. This allows the nodes to be connected in series, in parallel or in a series parallel combination. Depending on how the nodes are connected the composite converter's voltage and current output capabilities (in other words its voltage and current capacity) can be changed. This allows the stresses seen by the converter's components to be kept relatively invariant of the entire converter's output.

The multi-node converter architecture was then theoretically analysed so that the optimal number of nodes and their relative sizes could be determined. It was argued that identical nodes result in higher utilisation and also simplify the design, implementation and control of the converter. Using simulations, it was then shown that the number of nodes should be chosen to be a number with many factors. This maximises the number of configurations that the converter can be connected in, without wasting one or more nodes. These two results were verified using a multi-node converter simulator written for the purpose. The simulator was coupled with a Genetic Algorithm which allowed the relative node sizes to be optimised for maximum utilisation of the converter's capacity. These results confirmed the previous analysis, in other words identical nodes are preferable and the number of nodes should equal a number with many factors.

How to implement a multi-node converter was then discussed and it was decided that a two-switch forward converter with multiple identical secondaries would be used. Current would be shared passively and thus, how to improve the accuracy of the current sharing was analysed. It was found that each transformer secondary should have the same leakage inductance to minimise cross regulation errors that result in unequal current sharing. This was achieved by winding the transformer multi-filar.

How the converter's component requirements change with the number of nodes was then analysed. It was shown that, for a reasonable number of nodes, the coupled filter inductor used in a multi-node converter would likely be smaller and lighter than the inductor required by a traditional converter. The

filter capacitors required in a multi-node converter may however be larger unless a change in technology is enabled by the new configuration.

Once the multi-node architecture and its proposed implementation were better understood, models describing the converter were developed. One model assumed that the converter's nodes were identical but allows the number of nodes to be varied. The second model assumed that the converter consisted of four nodes, but does not assume that the nodes are identical. This allows the effects of component tolerances and their effects on current sharing to be ascertained. The two theoretical models were consistent given their different assumptions and they were thus used in a comparative design example.

Both a traditional converter and a multi-node converter were designed. The converters had identical output specifications but it was seen that the multi-node converter allowed significantly lighter and smaller magnetic components to be used. The filter capacitors required by both converters were also compared and it was found that whether the filter capacitors in the multi-node converter were larger or smaller than those in the traditional converter depended on the technology of capacitor that was used. These two results confirmed what was predicted when the component requirements for multi-node converters and how they change with the number of nodes was analysed.

Once a solid theoretical understanding on multi-node converters was present a prototype converter could be designed and built. The prototype converter is also based on the two-switch forward converter topology with four identical nodes and passive current sharing. The design and implementation of each part of the prototype converter was discussed. Each section of the prototype was then individually tested and evaluated.

The final chapter then evaluated the performance of the converter as a whole and attempted to verify the second theoretical model. The converter's output, how well current shares between its phases and the converter's efficiency were experimentally measured. The converter was able to operate over a ten times range while outputting constant power. In order to achieve this wide output range the output from the individual nodes only had to be varied over a much smaller range (approximately two times). This demonstrates the stated aim of partially decoupling the stresses that the converter's components are exposed to from the converter's output.

The second theoretical model was then calibrated such that it was able to simultaneously predict the prototype converter's output and efficiency. How the model was calibrated was discussed and the difficulties that were encountered were described. Deviations between the experimental results and the calibrated model's predictions were found and these were attributed to simplifying assumptions made when deriving the model. The model's calibrated circuit parameters were then compared with the expected circuit parameters. A large mismatch was seen between the inductor's expected and calibrated resistances. This was attributed to non-ideal effects that occur in the inductor windings. A

mismatch between the transformer's expected and calibrated resistance was also attributed to this cause. Due to these discrepancies, it is difficult to conclude with absolute certainty that the model is valid. It is recommended that the expected transformer and inductor resistances be revisited in future work by taking non-ideal effects into account. If the expected values for these parameters are then comparable with those predicted by the model, then the models validity will have been demonstrated. However, in the meantime it will be said that the model does appear to be valid and can be a valuable tool for evaluating and optimising multi-node converters based on the proposed implementation.

There is scope for future work regarding the design and implementation of multi-node converters. This future work includes:

- The multi-node converter simulator was coupled with a Genetic Algorithm to optimise the multi-node converter architecture. It would be preferable if a closed form proof could be found to confirm the results seen in the simulator.
- How to control a multi-node converter where the interconnection of the nodes is dynamically changed has not been addressed. Such a control system could be based around a small micro-controller. Systems capable of switching numerous high-side switches and keeping them on indefinitely will also need to be developed or sourced since it is likely that semiconductor switches would be used.
- The multi-node converter prototype was based on a topology with passive current sharing and a fixed number of nodes. The multi-node converter configuration is not limited to this and it could equally be implemented with multiple nodes that are completely independent of one another. This brings numerous advantages:
    - Redundancy and gradual degradation if a single node were to fail.
    - The capabilities of the composite converter could be changed by adding or removing nodes as required.
    - The nodes can be mass-produced and then combined into a converter as per the composite converter's requirements.
- The validity of the converter model should be revisited by calculating the expected inductor and transformer resistances by considering non-ideal effects in the windings.
- The practical implementation and mass-production of multi-node converters still needs to be addressed. For example, in the comparative design presented in Chapter 3 the multi-node converter configuration allowed surface mount capacitors to be used. This means that different manufacturing techniques could be used for mass-producing of the converter. This needs to be investigated further.
- This dissertation focused on implementing the multi-node converter architecture with a forward converter topology. However, an investigation into the optimal circuit topology for

implementing a multi-node converter has not yet been performed. This is recommended as future work.

- Section 3.2.5.4 discussed how the coupled filter inductor in a multi-node converter is likely to be smaller, lighter and cheaper than an inductor used in a comparable traditional converter. However, how the size, weight and cost of a multi-node converter's transformer compares to a transformer in a traditional design has not been analysed and discussed. This is recommended as future work.

REFERENCES

[1] W. M. Flanagan, *Handbook of Transformer Design and Applications*, Second ed. McGraw Hill, 1992.

[2] W. T. McLyman, *Transformer and inductor design handbook*, Third ed. New York, Marcel Dekker, 2004.

[3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Second ed. Kluwer Academic Publishers, 2001.

[4] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters Applications and Design*, Second ed. John Wiley & Sons, Inc., 1995.

[5] M. Brown, *Practical Switching Power Supply Design*, First ed. Academic Press, 1990.

[6] R. L. Haupt and S. E. Haupt, *Practical Genetic Algorithms*, 2nd ed. Wiley-Interscience, 1998.

[7] T. Weise, *Global Optimization Algorithms - Theory and Applications*, Second ed. http://www.it-weise.de/, last accessed 05 June 2009.

[8] L. H. Dixon, *Transformer and Inductor Design for Optimum Circuit Performance*. Unitrode/TI Design Seminars, Texas Instrument Incorporated, 2003.

[9] L. H. Dixon Jr., "The Effects of Leakage Inductance on Switching Power Supply Performance," in *Unitrode Power Supply Design Seminar*, 1990, pp. 21-27.

[10] W. A. Eberle, "MOSFET Current Source Gate Drivers, Switching Loss Modeling and Frequency Dithering Control for MHz Switching Frequency DC-DC Converters," Queens University, Ontario, 2008.

[11] W. Chen, X. Ruan, H. Yan, and C. K. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1463-1474, Jun. 2009.

[12] J. Tucker, *Understanding output voltage limitations of DC/DC Buck Converters*. Texas Instruments Incorporated, 2008.

[13] Ferroxcube International Holding B.V., *Soft Ferrites and Accessories*. 2008.

[14] International Rectifier, *IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF: High and Low Side Driver*. Data Sheet No. PD60147, Rev U, 2005.

[15] International Rectifier, *Application Note AN-978: HV Floating MOS-Gate Driver ICs,*

REV D.

[16] S. Park and T. Jahns, "A Self-Boost Charge Pump Topology for a Gate Drive High-Side Power Supply," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, 2005.

[17] Maxim Integrated Products, "App Note 2997: Basic Switching-Regulator-Layout Techniques," Jan. 2004.

[18] M. H. Rashid et al., *Power Electronics Handbook*. Academic Press, 2001.

[19] B. T. Irving and M. M. Jovanović, "Analysis, Design, and Performance Evaluation of Droop Current-Sharing Method," in *Applied Power Electronics Conference and Exposition (APEC)*, 2000, pp. 235-241.

[20] P. Wallmeier, N. Fröhleke, and H. Grotstollen, "Improved analytical modelling of conductive losses in gapped high-frequency inductors," in *Proc. IEEE Ind. Applicat. Conf*, St. Louis, 1998, pp. 913-920.

[21] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the IEE*, vol. 113, no. 8, pp. 1387-1394, Aug. 1966.

[22] J. Hu and C. R. Sullivan, "AC Resistance of Planar Power Inductors and the Quasidistributed Gap Technique," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 558-567, Jul. 2001.

[23] W. G. Odendall, J. A. Ferreira, and W. A. Cronje, "Combined Numeric and analytic methods for foil winding design," in *Power Electronics Specialists Conference (PESC)*, 1994, pp. 843-849.

[24] D. C. Pentz and I. W. Hofsajer, "Novel Technique for Shaped Planar Inductor Winding Optimisation in Gapped Core Applications," in *Power Engineering Conference and Exposition in Africa*, Johannesburg, 2007.

[25] Texas Instruments, "UC-3825 High Speed PWM Controller Datasheet," April 2004.

APPENDIX A

SUPPLEMENTAL PROTOTYPE ANALYSIS AND TESTING

A.1 Introduction

This appendix presents supplemental analysis and design work that has been done on the multi-node converter test platform. The operation and implementation of the control system is first described. Practical testing on the control system, including its frequency and duty cycle ranges is then shown.

The second section describes how the multi-node converter test platform's MOSFET drivers were tested. Measurements taken on the drivers and also on the necessary high-side driver modifications are presented. Circuit diagrams for the controller and the MOSFET drivers are not shown in this appendix. Appendix B contains full circuit diagrams and parts lists for the entire prototype.

A.2 Controller Analysis and Testing

A.2.1 Introduction

This section describes the design and operation of the PWM controller that was used in the test platform. Once the operation of the controller has been explained, experimental test results from the prototype controller are presented.

The controller is open-loop so that the user has full control over the converter and is based on the UC-3825 PWM controller from Texas Instruments. This controller IC's features and operation are discussed in the next section.

A.2.2 The UC-3825 High-Speed PWM Controller

The UC-3825 is a general purpose high-speed PWM controller manufactured by Texas Instruments [25]. The controller is capable of voltage and current mode control of converters and includes two PWM outputs that can be used to switch MOSFETs directly in some SMPS (Switched Mode Power Supply) topologies. It is available in a P-DIP package, which simplifies prototyping and provides an all in one approach for controlling SMPSs. The controller has the following features:

- An integrated error amplifier with sufficient gain and bandwidth to implement feedback control.
- A built in oscillator with frequency set by external passive components (A resistor and a capacitor)
- A programmable soft start feature that is set using only a single capacitor.
- Leading edge blanking.
- A current limit pin that doubles as a TTL compatible shutdown pin.
- An internal 5.1 V reference.

Most of the features commonly required when developing a SMPS controller are integrated into a single package. This means that simple controllers requiring only a single IC and some passive components can be developed. How the controller generates a PWM signal and some of its other features are explained in the following sections.

A.2.3 PWM Controller Design

A.2.3.1 Principle of Operation

The PWM control circuit operates by comparing a control signal with a repetitive waveform of the correct frequency (Normally a Saw-tooth or triangular waveform). This is illustrated in Figure A.1. When the control signal is greater in magnitude than the magnitude of the triangular waveform, a high output is generated. Otherwise the output is set low. By modifying the control voltage, the output's duty cycle can thus be modified. The output is also set low, no matter what the control voltage, when the triangular waveform's gradient is negative. This leads to a maximum possible duty cycle that is less than 50 % and depends on the negative gradient of the waveform.

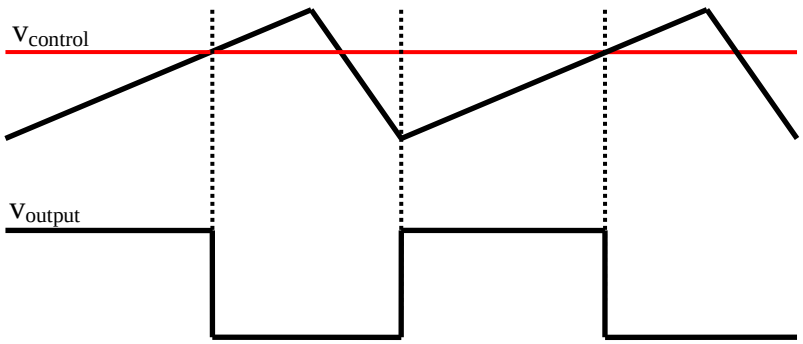


Figure A.1: Generation of PWM using a triangular waveform and a comparator

Since the PWM signal's duty cycle can be varied by varying the control voltage, it is easy to implement open loop control of a SMPS. Figure A.2 shows how open loop control of a SMPS using the UC-3825 can be implemented. A variable control voltage is applied to the error amplifier, whose output is fed back to the amplifier's inverting input. This forms a unity gain buffer and ensures that the error amplifier's output is approximately equal to the control voltage input (due to the amplifier's high gain). This voltage is then sent as the control voltage to the comparator. This means that the user can directly change the PWM signal's duty cycle by modifying the control voltage using a potentiometer.

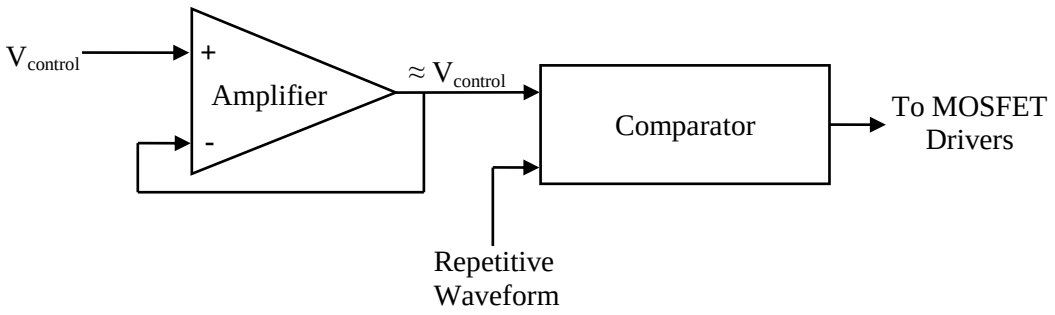


Figure A.2: A schematic showing open loop control of a SMPS

It is also possible to remove the error amplifier and to simply feed the control voltage directly into the comparator. However, if one chooses to use this method then it would be impossible to use the soft start capabilities provided by the controller. This is due to the fact that the controller implements a soft start by limiting the error amplifier's output to the soft start capacitor voltage. Bypassing the error amplifier would therefore cripple the soft start. The soft start capabilities for the controller are discussed further in Section A.2.3.5. How the triangular waveform is generated is discussed next.

A.2.3.2 Oscillator Design

The controller's oscillator needs to produce a regular repetitive waveform of variable frequency that can be sent to the comparator. A saw or triangular waveform is normally selected for this application and a schematic of how this waveform in produced in the UC-3825 is shown as Figure A.3. [25]

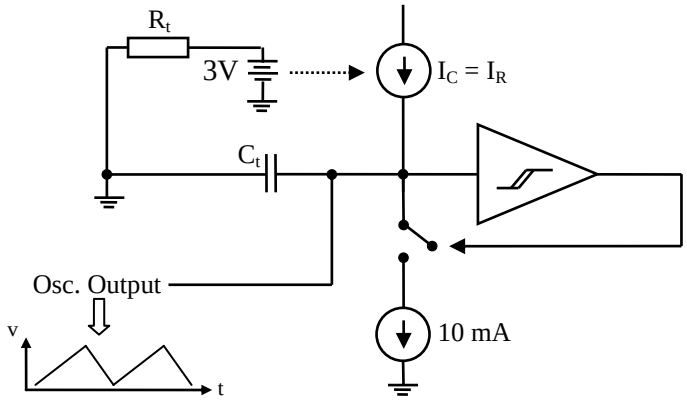


Figure A.3: Oscillator schematic [25]

The 3 V source supplies current I_R through the external timing resistor R_t. This current is mirrored and also flows through the upper current source. Until the comparator is triggered, all of this current flows into C_t, which produces a linearly increasing voltage or the upward sloping section of the triangular waveform. The slope of this waveform is therefore dependant on R_t and on C_t. Once the comparator triggers, the 10 mA source discharges the capacitor through the switch. Since I_c still flows during this time, the capacitor is discharged by 10 mA minus I_C, which determines the waveform's downward slope. Since this downward slope is dependent on I_R, and the output from the controller is always low

when C_t is being discharged, this leads to a maximum duty cycle restriction that depends on R_t and on the operating frequency. At higher frequencies, I_R is larger which means that it takes longer to discharge the capacitor each cycle, which lowers the maximum duty cycle. So at higher frequencies the maximum possible duty cycle will decrease.

The process described above repeats producing an even, regular output waveform which is then sent to the comparator. The output frequency is dependent on both the capacitor and the resistor magnitudes. Decreasing the resistor's magnitude leads to the charging current flowing into the capacitor increasing which means a faster rise time and higher frequency (and a slower fall time, but the faster rise time compensates for this and a higher frequency results). Decreasing the size of the capacitor means that less charge is required to charge and discharge the capacitor, and results in faster rise and fall times and thus higher output frequencies.

A.2.3.3 Error Amplifier Operation

The error amplifier is primarily needed when a feedback loop is required. The output from the converter is filtered and compensated and is then fed back into the error amplifier. A reference voltage is also sent to the amplifier and the difference between the two voltages is amplified and sent to the comparator. If the converter output voltage is too low then the difference between the reference and output voltage will be large, this leads to a large output from the amplifier which results in the duty cycle being increased and the converter's output increasing. The opposite happens if the output voltage is too high. This results in simple, yet robust feedback control. Closed loop control will however not be used in this controller, as direct control over the PWM signal's frequency and duty cycle is required for testing the multi-node converter topology.

A.2.3.4 The Output Stage

The controller's output stage provides high current outputs that are able to drive MOSFETs directly in some topologies. A simplified schematic of the output stage is shown as Figure A.4. The PWM signal that has already been described is sent to a toggle flip-flop and also to a NOR gate, whose output controls a totem-pole MOSFET driver [25].

The toggle flip flop ensures that only one of the outputs is high at any one time. For an output to be high it has to be currently set as the active output by the toggle flip flop and the comparator has to be low. This arrangement, with the toggle flip flop and NOR gates, means that the highest achievable duty cycle for the controller is limited to 50 % per output. If a duty cycle of greater than 50 % is required then both outputs need to be tied together.

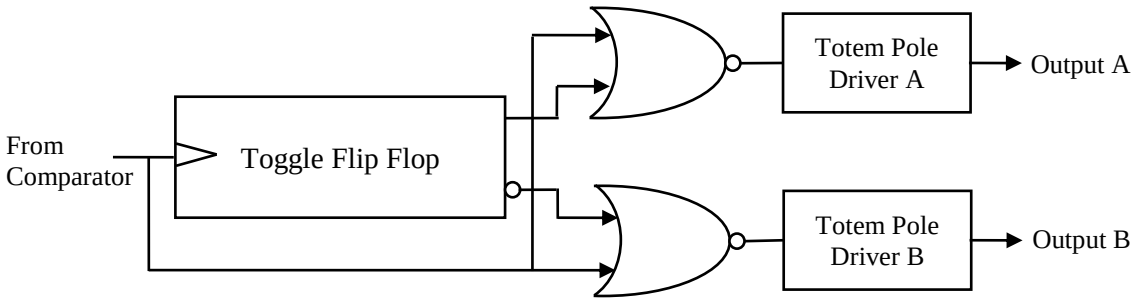


Figure A.4: Output stage schematic [25]

For a Two-Switch Forward Converter, the controller must limit the maximum duty cycle to less than 50% so that the transformer can be reset each cycle. If only a single controller output is used then this protection is already implemented by the controller.

A.2.3.5 Soft Start

Soft start capabilities are also built into the UC-3825. The soft start works by limiting the output of the error amplifier (the voltage that is compared to the triangular waveform) to the voltage present on the soft start pin. A capacitor is connected from the soft start pin to ground and is charged by an internal 9 µA current source. This causes the capacitor voltage to rise linearly until it reaches 5 V. Since the error amplifier's output and therefore the comparator input voltage are all limited by the soft start capacitor voltage, the duty cycle rises linearly with the soft start capacitor voltage until normal control takes over. This produces a slow, linear increase in duty cycle for the converter with the soft start time being set by the capacitor value. One can simply choose a capacitor value that gives the required soft start time by considering the charge that needs to be delivered to the capacitor by the 9 µA current supply. I.e. $C_{SS}= \frac{t_{ss}(9\mu A)}{5\ V}$ where t_{ss} is the soft start time.

A.2.3.6 Current Limit and TTL Shutdown

The current limiter is used to ensure that the converter's output current does not exceed the converter's specifications. A current loop or series resistance in the current path is required and the output from the sensor is sent to the current limit pin. If the voltage on the pin exceeds 1V then the current limit triggers and both outputs go low. Once the fault is cleared, the controller automatically begins a soft start.

The current limit pin also doubles as a TTL compatible shutdown pin. Placing a logic high on this pin forces both outputs low until the shutdown condition is removed. As soon as the shutdown condition is removed a soft start is automatically performed.

A.2.4 Analysis and Testing

The controller circuit (shown as Figure B.2 in Appendix B) was built and tested with regard to its achievable frequency and duty cycle ranges. The oscillator resistance (R_t) and capacitance (C_t) were selected to allow an output frequency that is modifiable around 50 kHz. The soft start capacitance was chosen for a two second soft start time. The results of the testing are presented below.

A.2.4.1 Duty Cycle Range

Figure A.5 shows the output from the PWM controller and also its ramp and control voltages at 50 kHz. The controller's output is high as long as the ramp voltage is below the control voltage. The effect the controller's dual outputs have on the output voltage is also visible in the figure, as the output for the one controller channel only goes high every second cycle (limiting the duty cycle to less than 50 %).

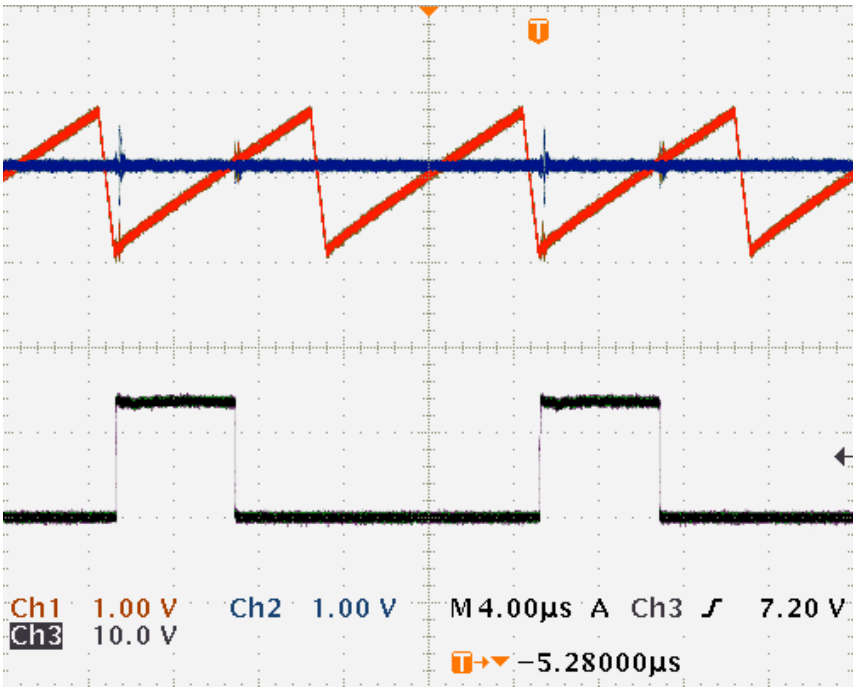
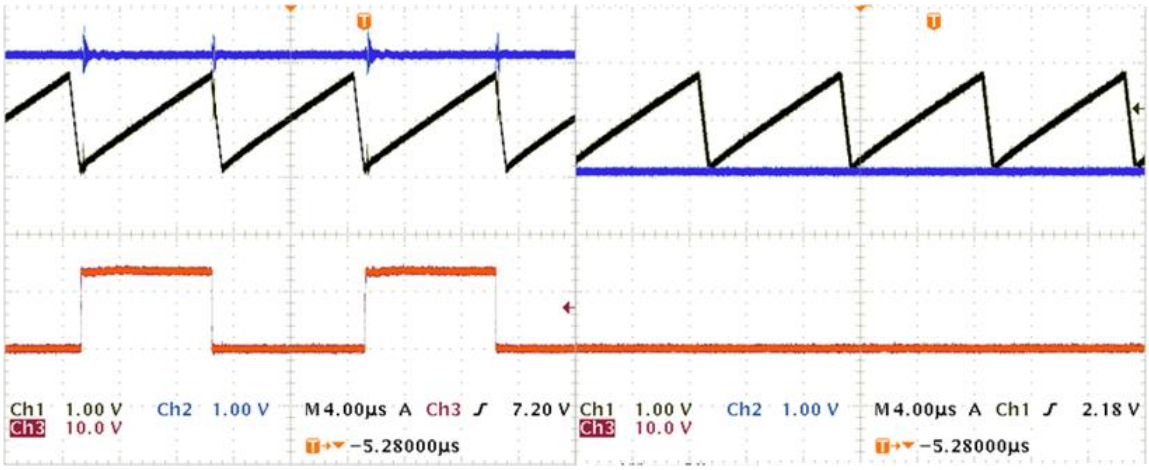


Figure A.5: PWM ramp and control voltages with the resultant controller output

Figure A.6 shows the output from the controller at its maximum and minimum duty cycles. The control voltages that result in these duty cycles are also shown. When the control voltage is higher than the ramp voltages peak, the duty cycle is maximised. However, when the control voltage is lower than the ramp voltages trough, the duty cycle becomes zero. By varying the amplitude between these two extremes, the duty cycle can be set to any value between zero and a maximum duty cycle that is dependent on frequency (always less than 50 %).



(a) (b)

Figure A.6: The controller's ramp, control and output voltages at the maximum (a) and minimum (b) duty cycles.

A.2.4.2 With Varying Frequency

The timing resistor's magnitude (R_t) was varied with the controller set to output maximum duty cycle. The results of the test are shown in Table A.1. The controller's output frequency can be varied anywhere between 35 kHz and 175 kHz. At these extremes the maximum achievable duty cycle varies between 0.475 at 35 kHz and 0.211 at 175 kHz. The maximum recommended frequency is that frequency that limits the maximum duty cycle to 0.35. Varying D_{max} below this value is not recommended by the manufacturer [25].

Table A.1: Measured PWM output frequency results

	Frequency	**Max Duty Cycle**	**Timing Resistance**
Maximum Frequency	175 kHz	0.211	100 Ω
Maximum Recommended Frequency	149 kHz	0.35	707 Ω
Minimum Frequency	35 kHz	0.475	5.38 kΩ

The controller will initially be used in conjunction with a Two-Switch Forward Converter that operates at 50 kHz. At this frequency the controller's maximum duty cycle is 0.46. This is suitable for use with the converter, since it will allow the duty cycle to be varied over a wide range while always allowing suitable off time for the converter's transformer to be reset each cycle.

A.2.5 Conclusion

This section has described the operation and features of the UC-3825 High-Speed PWM controller that was used in the multi-node converter test platform. The controller IC allows converters to be controlled using either current or voltage mode control using only the IC and a few passive external

components. However, for the test platform, a simple open-loop controller was required and was implemented.

Once the controller had been designed it was tested with regard to its duty cycle and frequency ranges. The results showed that the controller is suitable for use as the controller for the multi-node converter test platform.

A.3 MOSFET Driver Analysis and Testing

A.3.1 Introduction

The design and operation of the MOSFET drivers was discussed in Section 4.1.2 of the main text. This section describes how the converter's MOSFET drivers were tested. The operation of the modifications that were made to ensure the high-side driver's correct operation is then shown. Finally, the MOSFET's operation during switching transitions is discussed by presenting the voltage waveforms seen by the MOSFET while switching.

A.3.2 Driver Output

Figure A.7 shows the output from the MOSFET drivers into two IRFP460 MOSFETs, which are part of the Two-Switch Forward Converter test platform. Once the converter's MOSFETs and frequency of operation (50 kHz) were selected the bootstrap capacitor could be chosen. The choice was based on the frequency of operation and the required MOSFET gate charge. After considering this, a 1 µF ceramic capacitor was chosen [15].

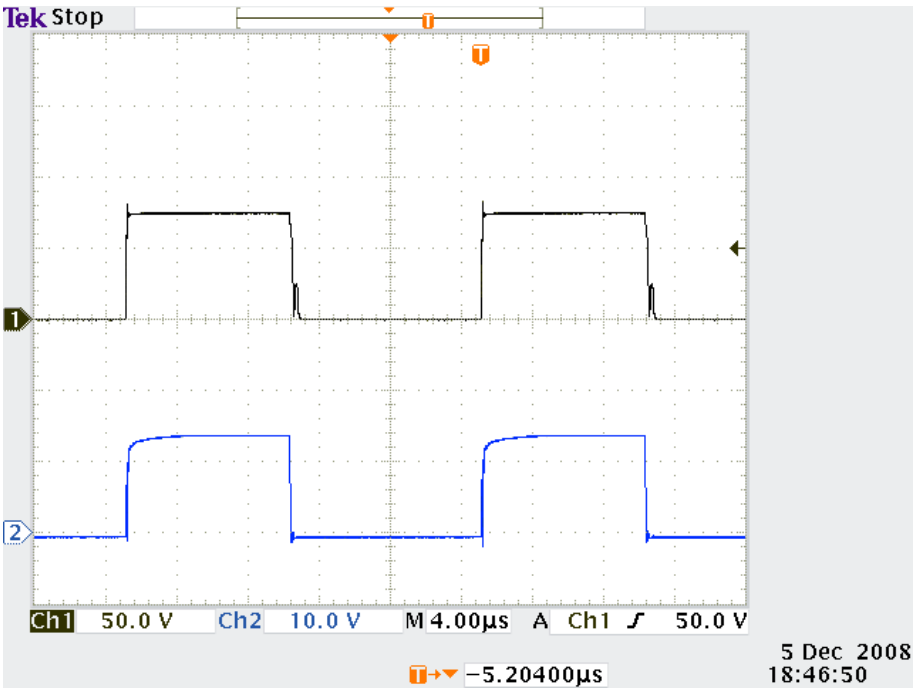


Figure A.7: MOSFET driver outputs (high-side on top)

The converter was tested with a DC bus voltage of 60 V, and therefore the high-side MOSFET floats up to this voltage when it is switched on. This can be seen in the figure below where both gate drive voltages are referenced to ground. The maximum gate voltage reached is approximately 75 V for the high-side MOSFET, which means that the high-side MOSFET's gate-source voltage is approximately 15 V.

The low side driver's output voltage waveform is also shown in the figure. The high and low side MOSFETs are switched simultaneously in accordance with the requirements of a Two-Switch Forward Converter. The gate drive voltages are relatively clear of any glitches at this time base, but both the rise and fall times for the drivers will still be examined in a later section.

A.3.3 Modifications Made to the High-Side Driver

The modifications that were made to the high-side driver were so that the driver could continue to operate even if the conduction time for the clamping diodes in the Two-Switch Forward Converter became short. When this occurs, the bootstrap capacitor can be at a higher potential than the supply that is meant to recharge it. This leads to the capacitor not being charged and eventually the high-side drive failing to switch the high-side MOSFET until the capacitor has been charged. In order to avoid this problem the modifications suggested in the main text (Section 4.1.2) were made and have been tested. Figure A.8 shows the action of the modifications made on the prototype converter when testing with a resistive load (i.e. the clamping diodes turn on for a very short time period if at all).

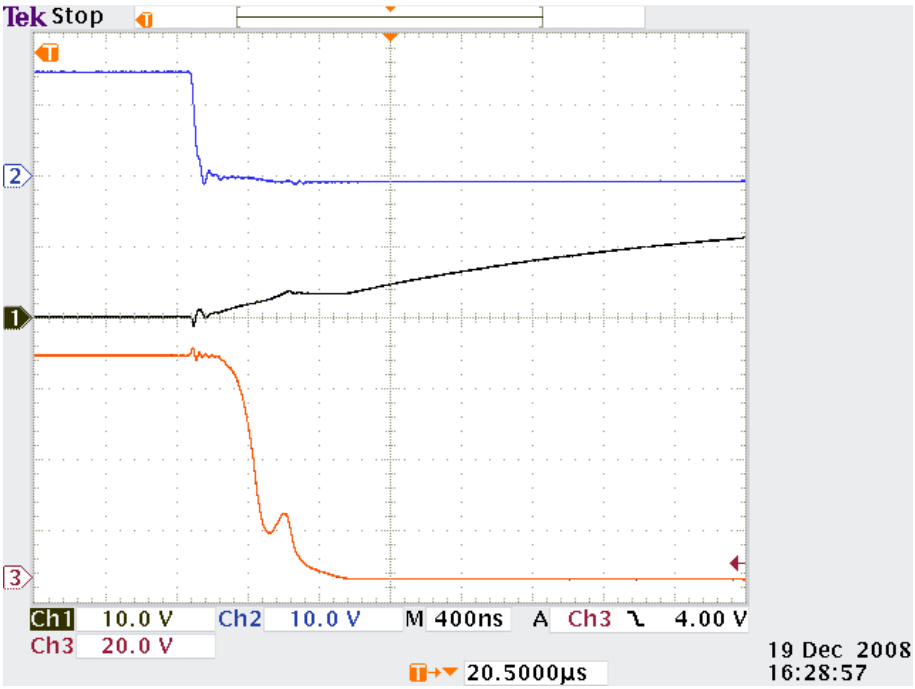


Figure A.8: Operation of the modifications made to the high-side driver

In the figure, the top waveform is the low side driver's output voltage. As the gate drive goes low, MOSFET M_4's gate is charged through resistor R_p. The middle waveform shows the gradual increase in MOSFET M_4's gate voltage due to the relatively large magnitude of R_p. The Miller plateau is clearly evident in the waveform. Once the MOSFET has turned on, the bootstrap capacitor is pulled low to ground as shown in the bottom waveform. The capacitor's negative plate is then held low, at ground, so that it can be charged. This continues until the two drivers are required to switch on again, where M_4 is turned off. This allows the bootstrap capacitor to float up to the required potential.

A.3.4 MOSFET Gate and Drain Voltage Rise and Fall Times

Switched mode converters operate their semiconductor switches in either their full on or off modes. Operating the power switch in an active region leads to extremely high instantaneous power dissipation in the switch. This is to be avoided and so the switching transitions for the semiconductor switches need to be kept as short as possible. In order to achieve this, the MOSFET drivers need to provide high currents to the MOSFET gate's for short durations. This charges the MOSFET's gate and switches the device as quickly as possible. The rise and fall times for the gate drive voltage and also for the drain source voltage are therefore of interest and are documented below. An inductive load is used for all of these measurements.

A.3.4.1 Low Side Drive

The rise and fall times for the low side MOSFET's gate drive signal and for its drain source voltage are shown in Figure A.9.

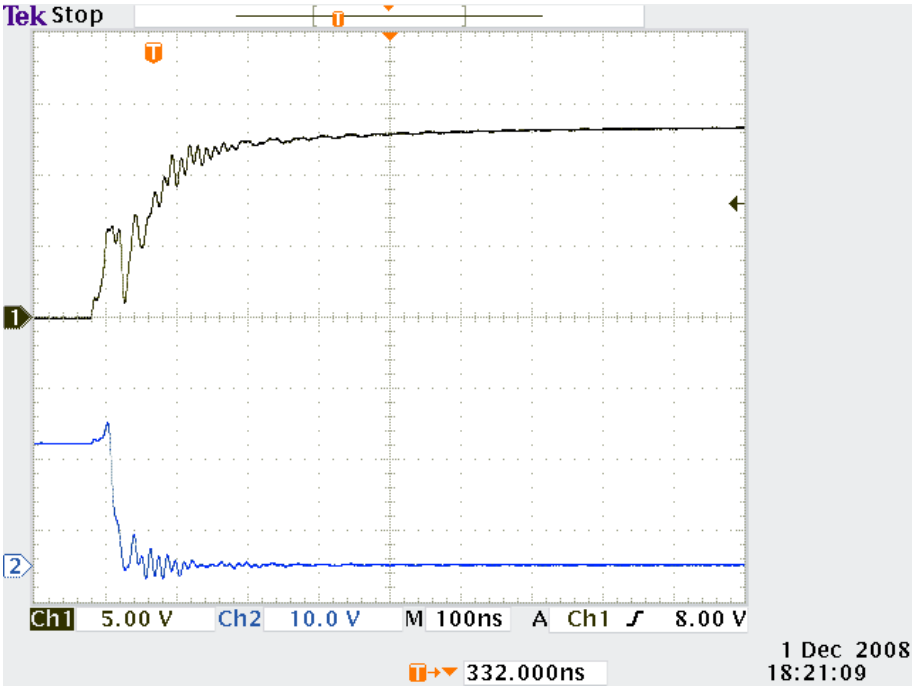


Figure A.9: Gate and V_{DS} voltage for the low side MOSFET (Turn on transition)

The gate drive signal is seen to rise until it reaches approximately 5 volts at which time the MOSFET begins to turn on. V_{DS} then begins to fall to a low voltage determined by the MOSFET's on-resistance and the current through the MOSFET. The driver is specified to switch a MOSFET with a 1 nF input capacitance in 25-35 ns. But since the chosen MOSFET (IRFP460) has an input capacitance of 5 nF, we can expect a rise time in the region of 125 ns to 175 ns. This corresponds well with that exhibited by the converter and shown in Figure A.9.

Figure A.10 shows the fall time for the low side MOSFET gate and the rise time for its drain source voltage. The gate drive is seen to have a fall time close to 75 ns which does correspond well with information given by the manufacturer.

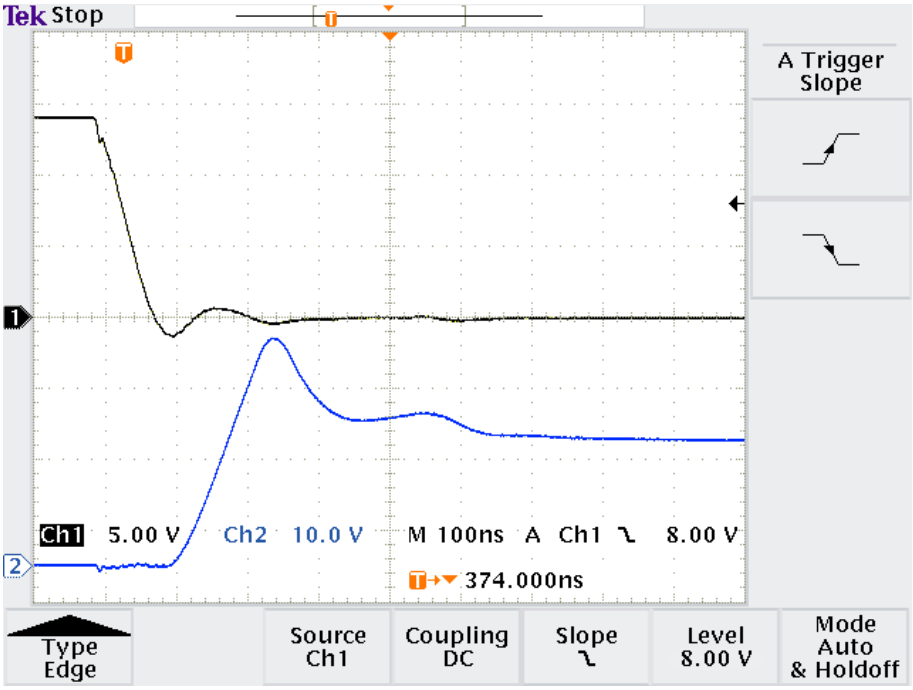


Figure A.10: Gate and V_{DS} voltage for the low side MOSFET (Turn off transition)

Right after the low side MOSFET is switched off, a resonance occurs between the parasitic capacitances in the primary side semiconductors and the inductive load. This was discussed in Chapter 4, Section 4.1.5.2. The resonance causes the peak in the low side MOSFET's drain-source voltage after it switches off. Once this resonance ends, the low side MOSFET voltage falls to its DC level.

A.3.4.2 High-Side Drive

The gate source and drain source voltages for the high-side MOSFET have also been measured and are shown in Figure A.11. The gate voltage exhibits very similar characteristics to the gate voltage for the low side driver. It also appears that gate resistance should be added to the high-side drive to further dampen the visible oscillations. The rise time for the gate voltage is approximately 150 ns,

which does match that of the low side driver and also the specifications given by the manufacturer for the driver IC.

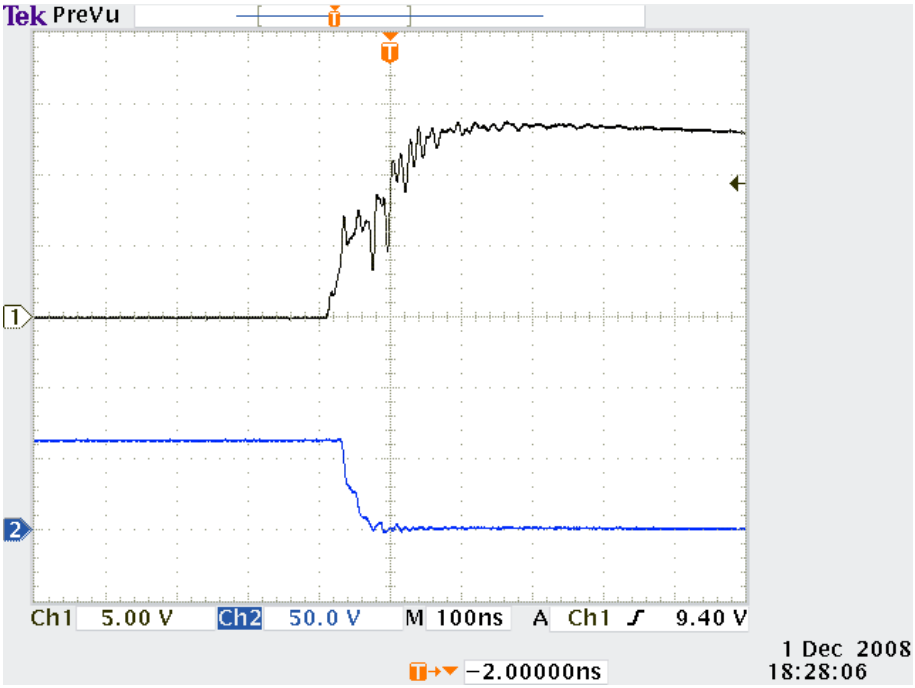


Figure A.11: Rise and fall times for the high-side MOSFET gate and drain-source voltages

Figure A.12 shows the high-side MOSFET's gate and drain-source voltages when it switches off. Some non-ideal behaviour is seen in this waveform due to resonances with the load and other effects. However, the origin of all of this non-ideal behaviour is not related to the subject of the research and will not be analysed at this time.

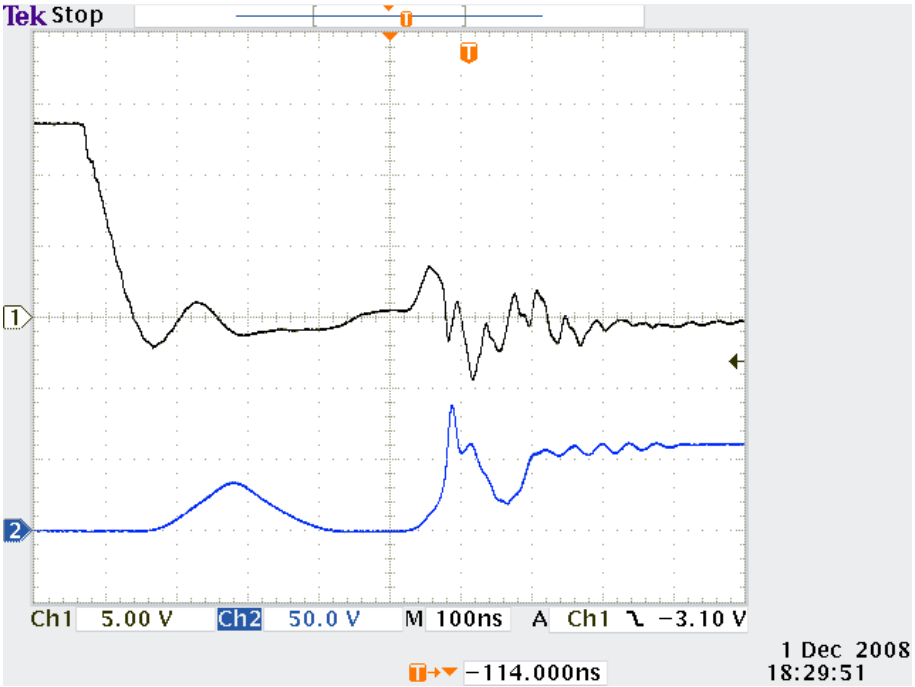


Figure A.12: Fall times for the high-side MOSFET gate and drain source voltages

A.3.5 Final Analysis

The MOSFET gate drives were able to reliably switch MOSFETs in a Two-Switch Forward Converter. The modifications that were made to ensure that the bootstrap capacitor stays charged were successful. This means that the converter is able to operate with very small duty cycles or even with a resistive load.

The switching waveforms for the converter's MOSFETs were also shown. They are not ideal for many reasons. These include oscillations on the MOSFET gates and also anomalies that occur when the MOSFETs switch off. These mean that the MOSFET gate drives are not perfect, and certainly do not switch the MOSFETs as quickly and as effectively as is possible. Possible modifications that are recommended include increasing the gate resistance and also modifying the physical layout of the board (especially moving the gate drive IC closer to the main MOSFET switches and minimising the inductance in this current loop). This would help to reduce the ringing that is seen on the MOSFET gates. The anomalies seen when switching the MOSFETs off could also be addressed.

The reason for which the drivers were developed does however need to be considered. They were developed to switch the MOSFETs in a Two-Switch Forward Converter test platform. This means that optimising the gate drivers may not be required since this is not the topic of the research that is underway. If the converter was for commercial use, then it may be worthwhile optimising farther. But since the anomalies in the switching waveforms will not greatly influence operation of the prototype converter, the drivers do not need to be optimised further at this time. The drivers will therefore be used, unmodified, in the switching converter test platform.

A.3.6 Conclusion

This section has described the testing and evaluation of the drivers used in the multi-node converter test platform. The drivers were tested with a resistive load so that the operation of the modifications made to a standard high-side driver implementation could be shown. It was found that the modifications worked according to expectations.

The drivers' operation were then analysed by presenting the gate and drain-source voltages during normal converter operation with an inductive load. The MOSFET voltages were not ideal and contained some significant anomalies. These anomalies are not related to the research that is underway and they are thus not addressed further. The drivers were therefore declared as fit for use in the multi-node converter test platform.

A.4 Conclusion

This appendix described the design, operation and testing of the control system used in the multi-node converter test platform. The controller is based on the UC-3825 high-speed PWM controller from

Texas Instruments. The operation of the IC was described, along with the features it provides. The controller's testing (as part of the test platform) was then presented. Both the controller's frequency and duty cycle ranges were discussed.

The second part of this appendix presented the results of the MOSFET driver's testing. It was found that the modifications made to a standard high-side driver implementation worked as expected. The MOSFETs' behaviour during switching transitions were then analysed by presenting their gate and drain-source voltages during switching transitions. The switching transitions were not ideal and numerous anomalies were seen in these waveforms. However, the anomalies were not addressed in detail since this is not the subject of the research. The drivers were thus declared as suitable for use in the test platform.

APPENDIX B

CIRCUIT DIAGRAMS, PARTS LISTS AND PCB LAYOUTS FOR THE MULTI-NODE CONVERTER PROTOTYPE

B.1 Introduction

This appendix documents the implementation of the multi-node converter prototype. The three sections that follow show the parts lists, circuit diagrams and PCB layouts for each section of the multi-node prototype. The Two-Switch Forward Converter test platform is presented first, followed by the multi-node secondary and finally the distribution board. How the converter prototype was tested is not documented here, this is described in Chapter 4 of the main test and in 0.

B.2 The Two-Switch Forward Converter Test Platform

The converter test platform and how it was implemented is described in this section. The entire circuit diagram for this PCB has been broken into three sections: the power stage, the controller and the drivers. This was done to make the circuit diagram more legible and understandable. Figure B.1 shows a schematic of the test platform's power stage. It consists of a DC bus stiffened by two capacitors, the two power MOSFETs and the clamping diodes. These clamping diodes are used to reset the core of any transformer connected to the output.

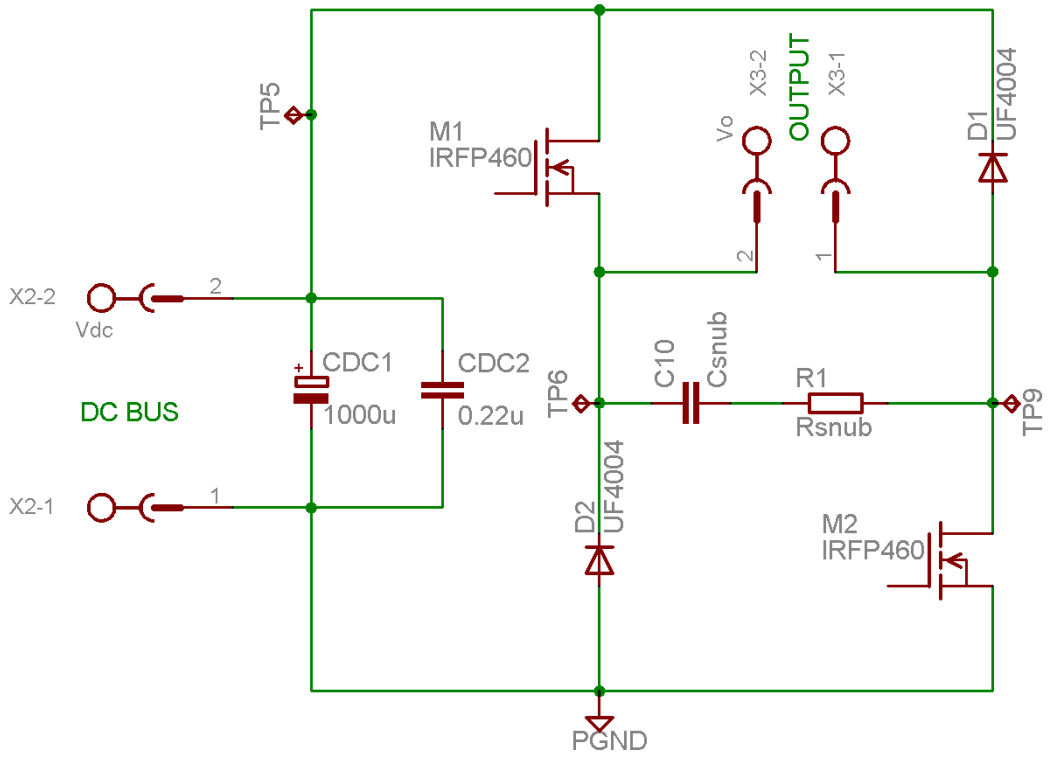


Figure B.1: Power stage schematic

The power stage also allows for the connection of a RC snubber across the output. This was not included in the final prototype since testing showed that it was not necessary. Test points are also shown, which help when taking measurements.

Figure B.2 shows a schematic for the test platform's controller. It consists of a UC-3825 high speed PWM controller from Texas Instruments. The controller's frequency of operation can be varied by changing C_T or by varying potentiometer R_{11}. This allows the converter's switching frequency to be changed simply and easily. R_7, R_8 and R_9 form a voltage divider whose output voltage can be varied by modifying the resistance of potentiometer R_8. This output voltage is sent to the controller's internal comparator and sets the controller's duty cycle. This allows open loop control of both the switching frequency and duty cycle by simply varying the value of two potentiometers.

The controller's soft start feature is also used where the soft start time constant is set by capacitor C_{ss}. Increasing the capacitance results in a slower soft start. Switch S_1 is an on/off switch. For more information on the controller and its operation, design and testing see 0.

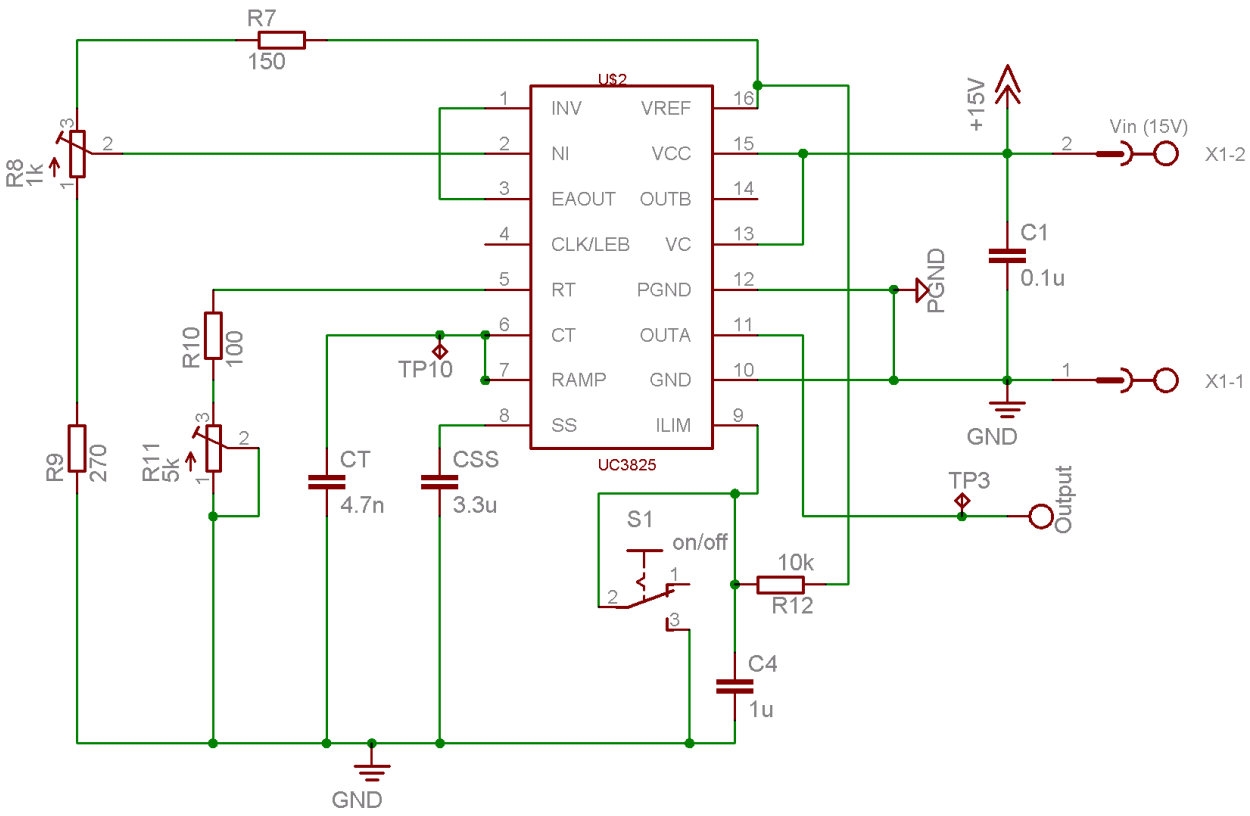


Figure B.2: Controller schematic

Figure B.3 shows how the drivers were implemented in the test platform. The drivers are based on an IR2113 high and low side driver from International rectifier. This driver IC is based on the Bootstrap capacitor principle and this can be seen by the presence of the bootstrap diode and capacitor (D_B and C_B). Some modifications have been made from a standard implementation due to the nature of the Two-Switch Forward Converter. These modifications consist of resistor R_3, diode D_3 and MOSFETs

M_3 and M_4. They ensure that the bootstrap capacitor remains charged even if diode D_2's (in Figure B.1) conduction time becomes short. For more information on the high-side driver's implementation and testing, see Section 4.1.2 and Appendix A.

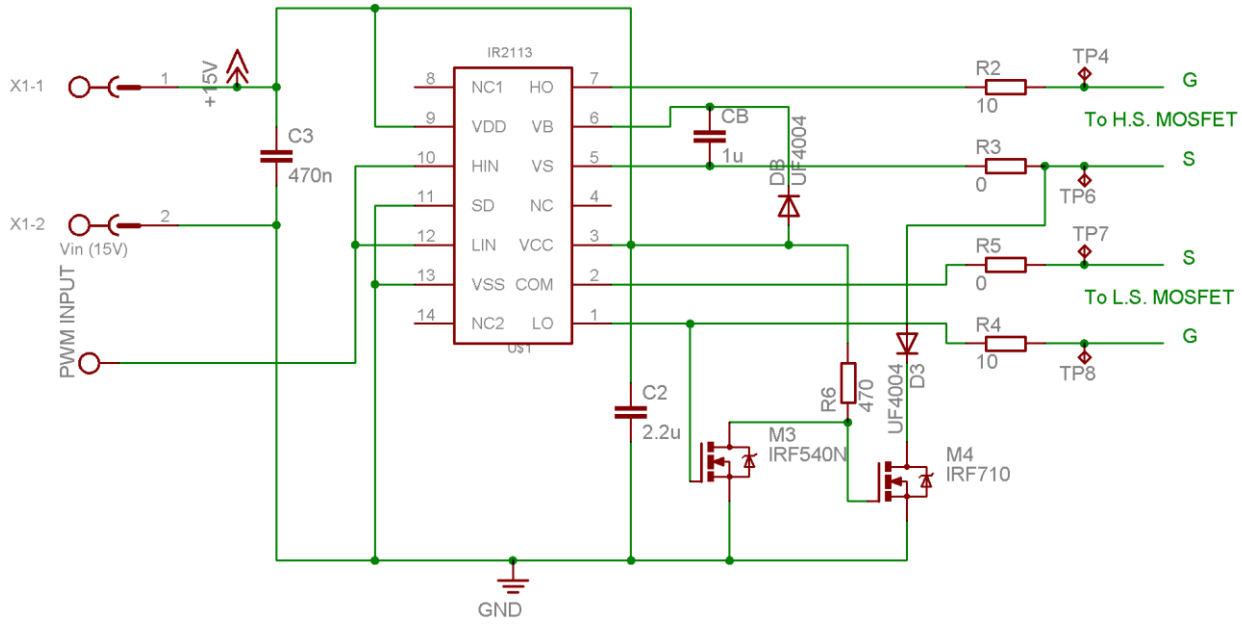


Figure B.3: Driver schematic

The three circuit subsections already discussed were combined and implemented on a single sided board. The PCB layout for the final Two-Switch Forward Converter test platform is shown in Figure B.4. There are some tracks shown on a second layer, however these were replaced with fly wires in the prototype so that a single layer board could be used. For a discussion on what criteria were used to design the board layout see Chapter 4, Section 4.1.3.2.

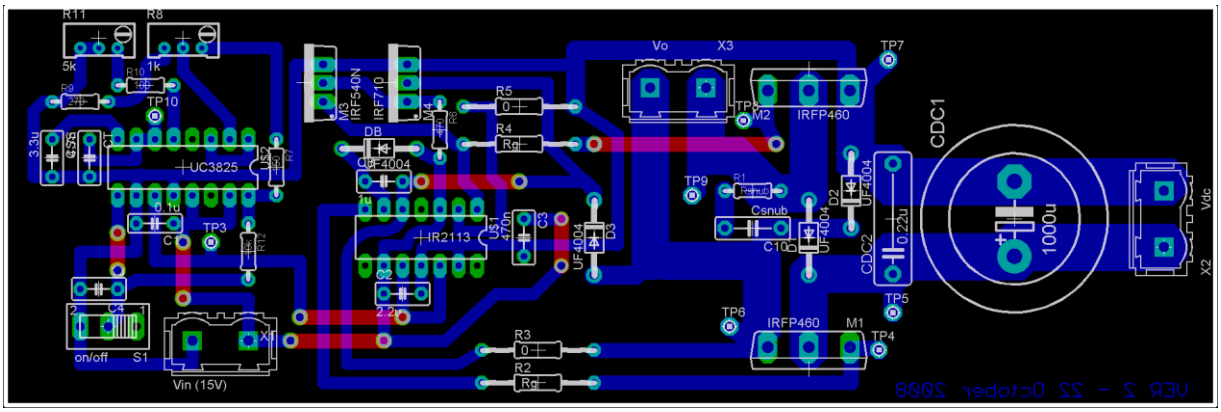


Figure B.4: PCB layout for the converter test platform

Each component within the converter test platform is now listed in Table B.1. How these component values were determined is not discussed here. This is discussed in Chapter 4 in the main text and in 0.

Table B.1: Parts list for the converter test platform

Component	Silkscreen Symbol	Value/Part Number	Description	Quantity
Driver IC	IR2113	IR2113	High and low side driver	1
Controller IC	UC3825	UC3825	PWM control IC	1
MOSFET	M_1, M_2	IRFP460	Main power MOSFETs	2
MOSFET	M_3	IRF540N	For the high-side driver modification.	1
MOSFET	M_4	IRF710	For the high-side driver modification.	1
Ultrafast Rectifier	D_1, D_2, D_3, Db	UF-4004	Two are used for the converter's clamping diodes, one for the bootstrap diode. Diode D_3 is part of the high-side driver modifications	4
Electrolytic capacitor	C_{DC1}	1000 µF	Bulk DC bus capacitor	1
Tantalum capacitor	C_{SS}	3.3µF	Soft start capacitor for the UC3825	1
Tantalum capacitor	C_2	2.2 µF	Bypass capacitor on the IR2113	1
Ceramic capacitor	C_B, C_4	1 µF	The Bootstrap capacitor and also switch debouncing on the on/off switch	2
Ceramic capacitor	C_3	470 nF	Bypass capacitor on the IR2113	1
Metal film capacitor	C_{DC2}	220 nF	DC bus capacitor (For higher frequency current components)	1
Ceramic capacitor	C_1	0.1 µF	Bypass capacitor for the UC3825	1
Ceramic capacitor	C_T	4.7 nF	Capacitor for setting the frequency of operation on the UC3825	1
Multi-turn potentiometer	R_{11}	5 kΩ	For adjusting the UC3825's operating frequency	1
Multi-turn potentiometer	R_8	1kΩ	For setting the UC3825's duty cycle	1
¼ W resistor	R_{12}	10 kΩ	Pull-up on reset pin for PWM controller on/off switch	1
¼ W resistor	R_6	470 Ω	Pull-up resistor for high-side driver modification	1
¼ W resistor	R_9	270 Ω	Part of the voltage divider for setting the PWM duty cycle	1
¼ W resistor	R_7	150 Ω	Part of the voltage divider for setting the PWM duty cycle	1

Component	Silkscreen Symbol	Value/Part Number	Description	Quantity
¼ W resistor	R_{10}	100 Ω	In series with 5kΩ pot for setting PWM frequency	1
¼ W resistor	R_2, R_4	10 Ω	MOSFET gate resistors	2
Slide switch	On/Off		A three pin switch for shutting down the converter	1
14 pin DIP carrier			For holding the IR2113	1
16 pin DIP carrier			For holding the UC-3825	1
Test points	TP3-TP10		Various test points to help with taking measurements	8
Terminal blocks	V_{DC}, V_{IN}, V_O		7.62 mm, 2-way	3

B.3 The Multi-Node Secondary

The multi-node secondary and its practical implementation are shown in this section. Figure B.5 shows the circuit diagram for this circuit board.

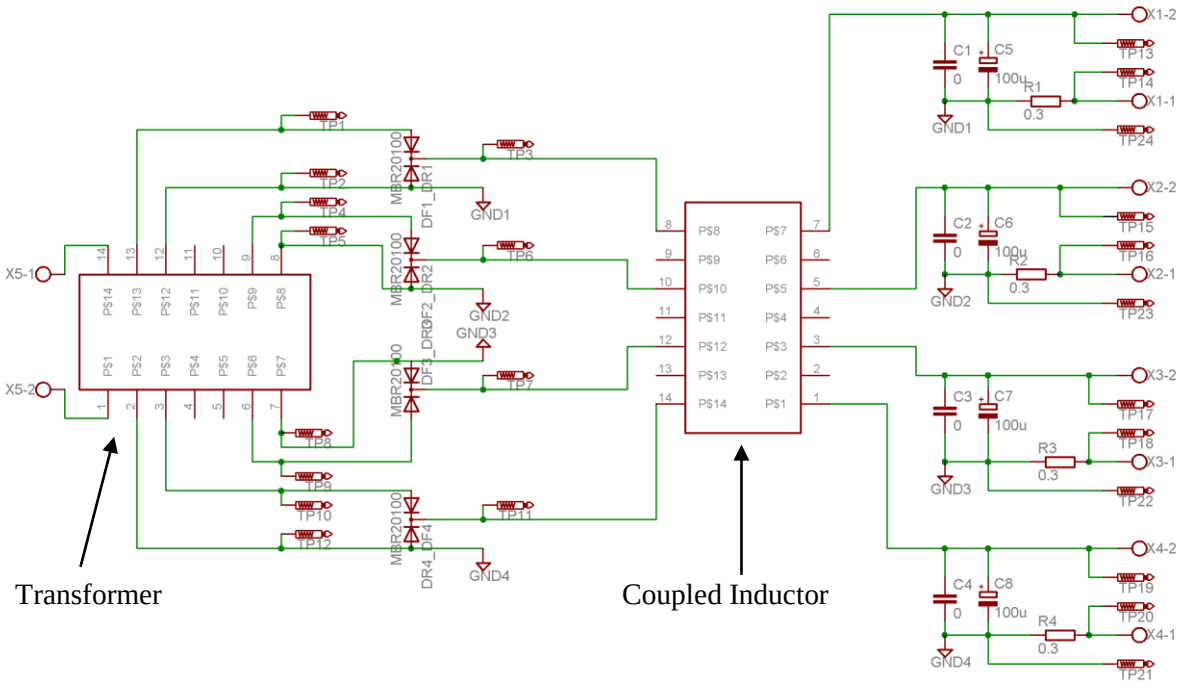


Figure B.5: Multi-node secondary schematic

Each node in the circuit consists of a transformer secondary, a rectification stage and a filter stage. To minimise the component requirements, the filter inductor is coupled and only a single transformer,

with four identical outputs, is used. This allows the entire secondary to be implemented using only two cores. For more information on the design of this board see Chapter 4, Section 4.2.

The multi-node node converter's secondary was implemented on a single sided PCB and the layout of this board is shown as Figure B.6. The tracks shown on the top layer were replaced with fly wires so that a single sided board could be used.

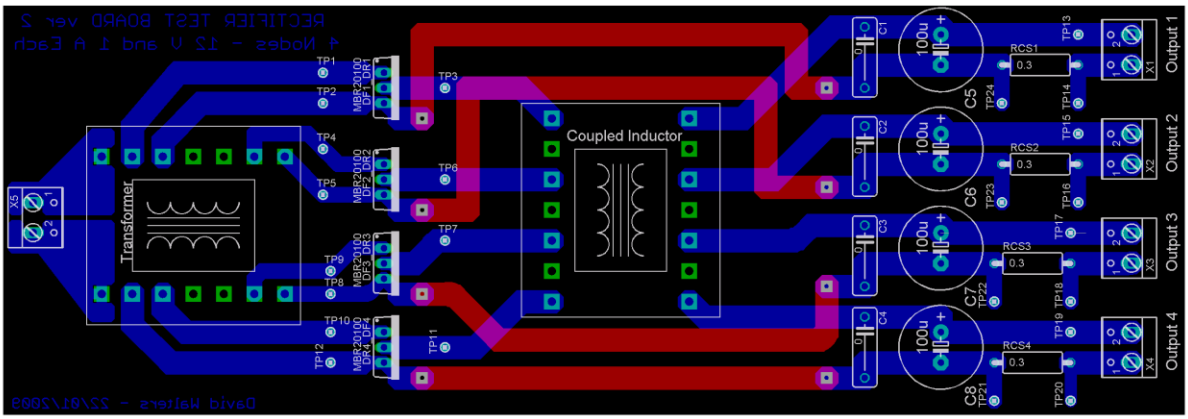


Figure B.6: Multi-node secondary PCB layout

Table B.2 shows a part list for the multi-node converter secondary board. Most parts are selected off the shelf, while the magnetic components are custom designed and built.

Table B.2: Parts list for the multi-node secondary

Component	**Silkscreen Symbol**	**Value**	**Description**	**Quantity**
Coupled inductor	Coupled inductor	4 x 500 µH	Four identical inductors wound on the same E30 core.	1
Transformer	Transformer		Transformer with 4 identical outputs wound on the same core. 32 and 17 turns of 0.5 mm wire on the primary and each secondary respectively.	1
Schottky Rectifier	DR_1_DF_1, DR_2_DF_2, DR_3_DF_3, DF_4_DF_4	MBR20100	Dual Schottky rectifiers in a single TO-220 package	4
Metal film capacitors	C_1-C_4	0	Not required and so not installed	0
Electrolytic capacitor	C_5-C_8	100 µF	Filter capacitors	4
Resistors	R_1-R_4	0.3 Ω (4 x 1.2 Ω in parallel)	Current sense resistors	4
Test points	TP_1–TP_{24}		Various test points to help with taking measurements	24

Component	Silkscreen Symbol	Value	Description	Quantity
Terminal blocks	Output 1-4, Input		5.08 mm, 2 way	5

B.4 The Distribution Board

This section documents the implementation of the multi-node converter's distribution board. Figure B.7 shows the distribution board's circuit schematic. The board is relatively simple and only consists of toggle switches and connectors. With the arrangement of switches, the four inputs can be connected in any series, parallel or series/parallel configuration depending on the switch position.

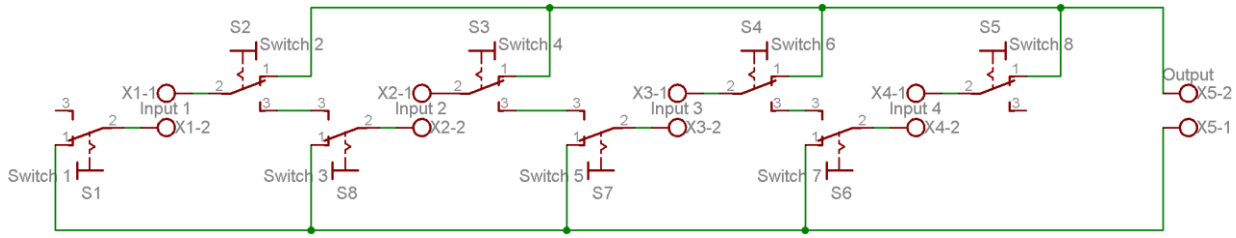


Figure B.7: Distribution board schematic

The distribution board was implemented on a single sided PCB with the layout shown in Figure B.8. Short wide traces and copper planes were used to reduce the DC resistance of the tracks and other interconnections.

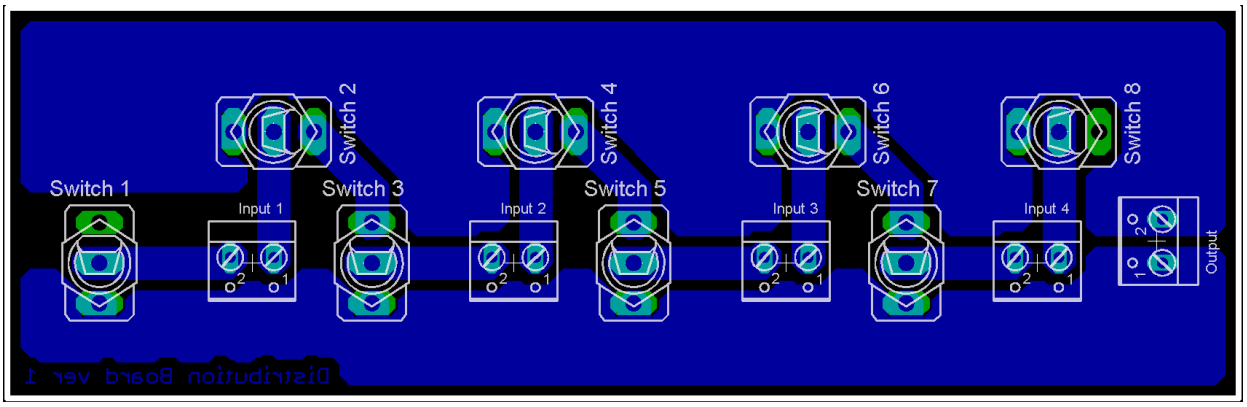


Figure B.8: Distribution board PCB layout

Table B.3 shows the parts list for the distribution board.

Table B.3: Parts list for the distribution board

Component	Silkscreen Symbol	Value	Description	Quantity
Toggle switches	Switch 1 - 8	n/a	Toggle switches used to change each input's input and output.	8
Terminal blocks	Input 1-4, Output	n/a	5.08mm, 2 way	5

B.5 Conclusion

The multi-node converter prototype's implementation has been discussed in Chapter 4 and further documented in this appendix. The circuit diagrams, PCB layouts and parts lists for each section of the prototype were shown. With this information it is possible to manufacture a copy of the multi-node converter prototype.

APPENDIX C

MATLAB CODE, C++ CODE AND OTHER ANCILLIARY INFORMATION

This appendix is on the CD included with this dissertation. The CD contains the following:

- Matlab Code
  - Buck Converter Losses Model (Matlab .m file)
  - Multi-node converter utilisation calculator for identical nodes (Matlab .m file)
  - The first converter model for any number of identical nodes (Matlab .m file)
  - The second converter model for four non-identical nodes (Matlab .m file)
- C++ Code
  - Multi-node converter utilisation calculator for identical nodes (a faster C++ implementation, Microsoft Visual C++ compiler project directory)
  - The Genetic Algorithm Toolbox with the Multi-node Converter Simulator (Microsoft Visual C++ compiler project directory). SDL and SDL Graphics must also be installed before running this program.
- Experimental Measurements
  - Efficiency and output measured on the prototype converter (Excel spreadsheet)
- Dissertation
  - The entire dissertation including appendices (Microsoft Word .docx and PDF formats)
- Papers
  - A copy of a paper presented at SAUPEC 2009 in Stellenbosch. This paper was submitted as a discussion paper and so is not part of the proceedings (PDF and .docx).
  - A copy of a paper presented at PCIM 2009 in Nuremberg (PDF, .docx and a copy of the poster presentation in .pptx format).
- Spreadsheets
  - The spreadsheets used to design the inductors and transformers used in the comparative design.