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Retaining the integrity of dc-link voltage in variable speed drives applications

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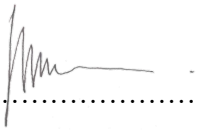
A dissertation submitted to the Faculty of Engineering and Built Environment, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Master of Science in Engineering.

February 2021

Declaration

I, Freeman Chiranga, declare that the content of this report is my own unaided work. Where material from other sources is used, this is appropriately acknowledged. The research is being submitted for the Degree of Master of Science in Engineering at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination at any other university.

Signed:……

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Thirdly, I would also like to acknowledge my industrial supervisor Dr M Manyage for providing the necessary alignment between my research work and industrial challenges being experienced by Eskom.

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Abstract

This research is concerned with the development of a power electronics module that utilises a switched capacitor for retaining the integrity of the dc-link voltage of a variable speed drive (VSD) during a short-term power interruption (STPI). Many industrial processes are now very much dependent on solid-state AC VSDs. Their susceptibility to voltage dips and STPIs, resulting in disruptions of critical processes, loss of production and revenue is a major concern. To support the transmission grid, power station equipment is required to withstand certain voltage disturbances anticipated on the transmission network. In South Africa, these requirements are specified in the South Africa Grid Code (SAGC). Non-compliance to SAGC requirements, production and revenue losses can be avoided by enhancing the voltage dip ride-through capability of the VSD. This research work only focuses on the worst-case voltage disturbance of a 0.2 s STPI.

Capacitor switching onto the dc-link was accompanied by an inrush current. To limit this current, the module was initially equipped with a fixed resistor. A method for sizing this resistor and capacitor for a v/f-controlled drive using readily available VSD and motor nameplate was developed and validated. The methodology is meant for low voltage (<1000V) and low power (100kW) applications. Simulation and experimental work were conducted for the validation of the proposed module. Fixed resistor inrush limiting experimental results show a 10.6% drop in torque and a 2.5% drop in speed with torque pulsations of 13% and 14% at start and end of compensation respectively. Module efficiency was estimated to be 94.8%. Fixed resistors resulted in an undesirable 7.7% voltage drop across the resistor and loss in efficiency which led to the investigation and development of a further three inrush current limiting techniques. These include, the use of a variable resistor, inductor and equipotential voltage switching. Variable resistor technique resulted in a 9.8% drop in torque and 1.7% drop in speed with torque pulsations of 12% and 9% at start and end of compensation respectively. Voltage drop between the dc-link and capacitor during compensation was reduced to 1.9%. An overall module efficiency of 99.3% was obtained. Use of an inductor resulted in a 10.1% drop in torque and 1.2% drop in speed with torque pulsations of 15% and 12% at start and end of compensation respectively. Module efficiency of 99.5% was obtained. Equipotential voltage switching resulted in the least voltage and torque drops of 9.9% and 3.2% respectively. It provided the highest estimated efficiency of 99.6%. Low torque pulsations of 6.8% and 9.8% at start and end of compensation respectively were observed. With this technique, considerable high frequency inverter currents flow through the capacitor resulting in the need of a capacitor with a higher ripple current rating.

VSD and motor performance were found to be influenced by the inrush current limiting technique adopted. The proposed module did not eliminate the drop in dc-link voltage but ensured that the dc-link voltage remained above the VSD under-voltage trip level thereby allowing the VSD to ride-through the 0.2s STPI while supplying load power.

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Chapter 1
Introduction

1.1. Research Background

Many industrial processes are now very much dependent on solid-state AC motor variable speed drives (VSDs). Their increased use is due to efficiency improvements, energy savings and process control flexibilities [1]. VSDs however, are often susceptible to voltage disturbances such as dips, surge and short-term power interruptions (STPIs) resulting in disruptions of critical processes, loss of production and revenue. To support the transmission grid, most power utilities in the world are required to comply to certain voltage disturbances anticipated on the transmission grid [2].Various transmission grid codes have a common way of defining which grid disturbances have to be tolerated. They also specify frequency of occurrence of these disturbances. In South Africa, these requirements are specified in the South African Grid Code (SAGC). Amongst these requirements are voltage dips and STPIs occurring on the point of connection for which power station units connected to the transmission grid should be able to withstand without tripping [3]. Utility power stations in South Africa have experienced VSD trips on under voltage protection during SAGC characterised voltage dips. Such trips have resulted in the loss of generating capacity due to loss of key processes in power generation, increased risk of load shedding, reduced power quality and non-compliance to SAGC.

Studies carried out by numerous researchers to analyse the behaviour of a VSD during a voltage dip, have identified the dc-link undervoltage as the main reason for the voltage source inverter (VSI) VSDs tripping during a voltage dip [1] [4] [5]. VSD trips on dc-link undervoltage protection during voltage dips and STPI can thus be prevented by maintaining the dc-link voltage above the under-voltage trip level of the VSD. Maintaining a healthy dc-link voltage during a voltage dip and thus avoiding a VSD dc-link undervoltage trip constitutes what is generally referred to as ride-through of a VSD [2]. Ride-through can be achieved through a number of techniques which fall under three main categories. These are, (a) hardware modifications (e.g. increasing dc link capacitance), (b) improvement in power supply conditions (e.g. use of uninterruptible power supply) and (c) modifications to the VSD control algorithm (e.g. kinetic energy recovery) [6].

There is an abundant number of VSDs on the market comprising of different makes and models which gives rise to differences in susceptibility and response to voltage dips and STPI [5]. Existing drive topologies can be modified to enhance their ride-through capability. Most modifications to existing topologies would require close collaboration with different manufacturers to access design base technical information. Such arrangements present challenges due to intellectual property which is closely guarded by manufacturers and thus not readily available for access by users of VSDs. Modifications to the drives must then be limited to an electrical connection only between the existing VSDs and ride-through

enhancing module. This results in limited options available for enhancing ride-through capability for existing VSDs. Modifications to existing VSDs should also consider impact on device ratings, module performance and power quality.

For voltage disturbances of the same duration, a STPI results in the most significant voltage drop on the dc-link. This is because during a STPI, dc-link storage elements will supply all the power required by the load. To be able to ride-through a STPI, a sufficient energy reserve is required. A variety of energy storage technologies are candidates for providing the required power during a STPI and dip. Battery backup systems, supercapacitors, motor-generator sets, flywheel energy storage systems, superconducting magnetic storage and fuel cells are some examples of these technologies [1].

To achieve a successful STPI ride-through, this research work proposes an add-on power electronic module incorporating an energy storage device. Correct design of this add-on module is key in maintaining the dc-link voltage integrity of a VSD during a voltage dip and STPI. This work also aims to develop a sizing methodology of the module for low voltage VSD applications.

1.2. Problem Statement

The SAGC, states that "Any *unit* or *power station* equipment shall be designed with anticipation of the following voltage conditions at the point of connection:

- A voltage deviation in the range of 90% to 110% of nominal voltage.
- A 3-phase voltage drop to zero for up to 0.2 seconds, to 75% for 1 second, or to 85% for 60 seconds provided that during the 3-minute period immediately following the end of the 0.2 second, 2 second, or 60 second period the actual voltage remains in the range 90% to 110% of the nominal [3].

Figure 1-1 summarises SAGC voltage disturbance ride-through requirements for equipment. The area above the curve represents voltage dips which power station equipment should withstand.

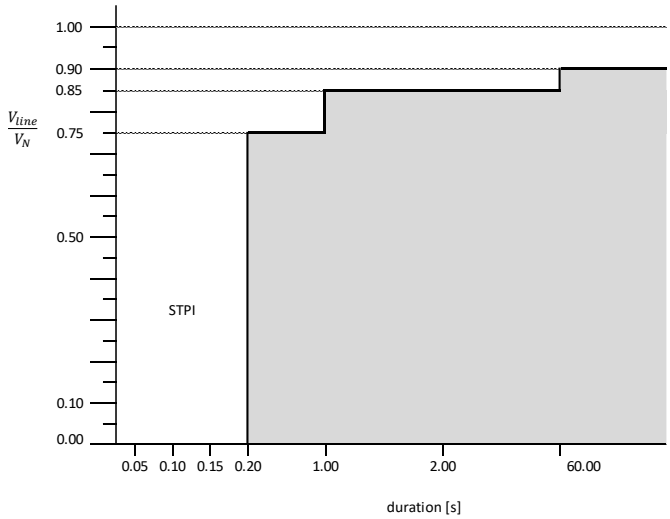


Figure 1-1.SAGC Voltage Disturbance Withstand Requirements

A voltage dip on the power station point of connection propagates throughout the station's electrical reticulation system. Typically, the point of connection refers to the 275kV/400 kV busbars where the power station equipment connects to the transmission network. Steady state values at low voltage boards during the dip depends on the system configuration and the type of dip. Thus, if the steady state value falls below under-voltage trip setting, the VSD will trip on dc-link undervoltage protection. A number of critical processes in most utility coal fired power stations are equipped with VSI drives. One such process involves regulating the amount of coal flow into a boiler. This is achieved through the use of a coal feeder conveyor system as shown in Figure 1-2.

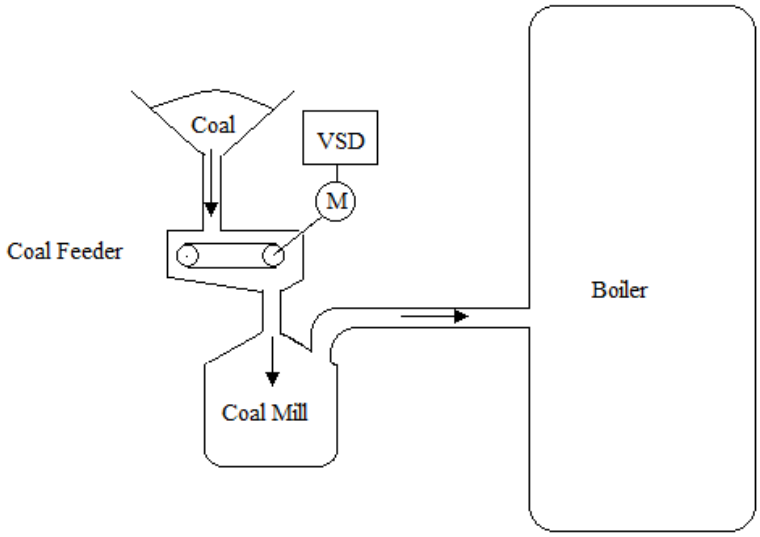


Figure 1-2. Typical Mill System Overview

Coal used for firing the boiler is ground into a fine powder to increase the surface area for combustion. This results in the complete combustion of the coal and an increase in the boiler efficiency. A mill is used to grind the coal used which is then fed into the boiler. A coal mill feeder conveyor system regulates the amount of coal fed into the coal mill for grinding. A trip in the coal feeder conveyor system affects coal flow into the boiler resulting mostly in the boiler instabilities and trips. When the coal mill feeder VSD trips on dc-link undervoltage protection, the motor shaft leads to an immediate stop of the conveyor system due to the mill coal feeder conveyor system having a low system inertia and a constant load torque. Such conveyor stops introduce instabilities in the boiler which can result in the generating unit tripping leading to a loss of power. Voltage dip ride-through capability enhancement of the coal mill feeder motor VSD will minimise such trips.

The coal mill drive system is a constant torque application. The system is sensitive to rapid changes in torque which can damage mechanical system components, Large speed variations from pre-dip values are not acceptable as these negatively affect coal flow into the boiler.

1.3. Research Objectives

To address the challenge of non-compliance to SAGC, the following research objectives need to be achieved:

- Establish ride-through capability of existing VSDs so as to identify short-comings which when addressed will allow the VSD to ride-through a SAGC characterised voltage dip.
- Develop a power electronics module that retains the dc-link voltage of a VSD so as to avoid a dc-link undervoltage trip in compliance with the SAGC.
- Develop a sizing methodology which will allow the module to be sized for different VSD ratings using readily available data such as, motor and VSD nameplate, etc.

1.4. Research Questions

To be able to achieve the stated objectives of this research, some key questions need to be answered. These include:

- What method can be used to maintain a VSD dc-link voltage above the under-voltage trip level during a STPI?
- What is the impact of the operation of the module on VSD (dc-link voltage) and motor performance (torque and speed)?

1.5. Research Approach

The main goal of this research is to improve the undervoltage ride-through of a VSD to SAGC characterised voltage dips. To achieve this, the following approach was be adopted:

1. Design, model and simulate using Simulink, the dc-link voltage compensating module.
2. Analyse effect of module operation on motor performance (torque and speed).
3. Develop an experimental method that emulates different SAGC voltage dips.
4. Build and test a lab prototype of the dc-link voltage retaining module. Assess the impact of module operation on dc-link voltage, motor torque and speed.
5. Develop a sizing methodology which will allow the module to be sized for different VSD ratings using readily available data such as motor and VSD nameplates.

1.6. Dissertation Outline

The dissertation is organised as follows:

Chapter 2 explores the workings of a VSD in particular its behaviour undervoltage dips and impact on the incoming supply and motor performance. A review of voltage dip ride-through improvement alternatives of VSDs, their pros and cons are investigated in Chapter 3. Details of the proposed ride-through solution incorporating an additional switched dc-link capacitor, sizing of the additional capacitor,

sizing of inrush current limiting resistors and circuit analysis of the proposed solution are made in Chapter 4. Simulation and experimental work of the proposed compensating device incorporating fixed resistor inrush current limiting technique is made in Chapter 5. Module losses determination, efficiency estimation and impact of module operation on VSD and motor performance is also carried out. Experimental validation of sizing methodologies for capacitor and inrush current limiting resistor concludes this chapter. Chapter 6 looks at the challenge of inrush currents and investigates three inrush current limiting techniques which include a variable resistor, inductor and equipotential voltage switching (EVS). Their impacts on VSD and motor performance and module efficiency are assessed. Chapter 7 concludes the dissertation with a summary of the work that was done and recommends possible areas for future research.

1.7. Dissertation Contributions

1.7.1. Chapter 4

A power electronics module which allowed a VSD to ride-through a 0.2 s STPI was designed, developed, and validated. A framework for the selection and sizing of key components of the module was also developed. Such framework highlights key aspects to consider when selecting IGBTs, diodes and energy storage devices. One important outcome of the framework is a method for sizing of the additional capacitor and inrush current limiting resistors utilising readily available data (motor and VSD nameplate data). This allows the proposed module to be scaled for use with different sized v/f control based VSDs. The proposed module configuration allows adaptation for use with supercapacitors bringing flexibility to the design.

1.7.2. Chapter 5

A Simulink model incorporating the proposed compensating module and a v/f controlled VSI VSD was developed and tested. Such a model can be used for assessing the behaviour of v/f controlled VSI VSD and a squirrel cage induction motor to different voltage dips. A voltage dip generator for emulating SAGC characterised voltage dips on input supply was devised and successfully tested. An experimental set-up of the module including the VSD-motor assembly was assembled and tested with successful monitoring of key VSD and motor parameters. An experimental set-up of this nature allows for validation of desktop work. A model for assessing energy losses and estimating overall module efficiency was developed in PLCES. Such a model is invaluable for assessing thermal behaviour of electronic circuits and recommending appropriate thermal devices (heat sinks, fans) for controlling the circuits thermal environment.

1.7.3. Chapter 6

Three inrush current limiting techniques employing an inductor, a variable resistor and equipotential voltage switching (EVS) were developed, assessed, and tested. Their impact on VSD and motor performance was established. Models for assessing losses incurred and overall efficiency were developed. These models allow for the optimisation of designs based on identified loss contributions of each circuit component.

1.8. List of Publications

1.8.1. Conference Papers Published

F. Chiranga, L. Masisi, **Variable Speed Drive DC-link Undervoltage Ride-through Improvement Using Switched Capacitors**: 2020 International SAUPEC/RobMech/PRASA Conference, 2020: pp. 1–5. https://doi.org/10.1109/SAUPEC/RobMech/PRASA48453.2020.9040960.

1.8.2. Journal Articles Submitted

F. Chiranga, L. Masisi, **Managing Inrush Current in a Variable Speed Drive Short Term Power Interruption Ride-through Module**, IEEE Journal of Emerging and Selected Topics in Power Electronics: Special Issue on Emerging Applications of Power Electronics in Developing Economies, 2021.

F. Chiranga, L. Masisi, **Variable Speed Drive Voltage Dip Proofing using Additional DC-link Switched Capacitors**, IEEE Journal of Emerging and Selected Topics in Power Electronics: Special Issue on Emerging Applications of Power Electronics in Developing Economies, 2021.

Chapter 2

Variable Speed Drives

2.1. Introduction

The focus of this research work is on improving the response of a VSD to a 0.2 s STPI. It is important to understand the workings of a VSD in particular its behaviour when subjected to voltage dips. This chapter explores that background information on VSDs. An assessment on typical voltage dips that VSDs are exposed to is made. Behaviour of the VSD due to voltage dips is assessed by analysing the energy balance disturbance during a dip. Inrush currents associated with operation of VSD and power supply harmonic pollution are also explored.

2.2. VSD Topology

A VSD produces AC power of variable magnitude and frequency from AC power of fixed magnitude and frequency. Figure 2-1 shows a typically VSD comprising a rectifier, dc-link and inverter. Rectifier converts AC voltage into DC voltage.

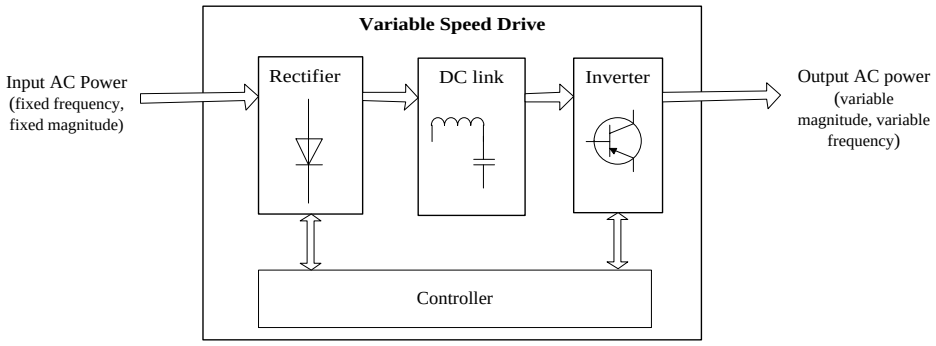


Figure 2-1. Typical VSD Topology

The dc-link smoothens the rectified voltage and the inverter converts DC voltage into AC voltage of variable magnitude and frequency. VSDs fall into two main categories i.e. voltage source inverters (VSI) drives and current source inverters (CSI) drives. VSI drives incorporate a dc-link capacitor which acts as a constant voltage source to the inverter and also serves as an energy storage for supplying power to the inverter during a voltage dip thereby assisting in maintaining the dc-link voltage for a limited time. VSI drives are further split into pulse-width modulated VSI with a diode rectifier and square-wave VSI with a thyristor rectifier. The dominant type for drives up to 100 Hp use the PWM-VSI type [7]-[8]. CSI drives use an inductor in the dc-link to supply a relatively constant current to the inverter. The presence of diode rectifiers in PWM-VSI drives result in the drives having limited response possibilities during a voltage dip or STPI [2] [6]. This makes them more susceptible to voltage dips or STPI when compared to CSI drives.

2.3. Voltage Dips & Short-Term Power Interruptions

A voltage dip is a momentary reduction in voltage magnitude. It is usually defined by its magnitude and duration with typical values of magnitude between 0.1- 0.9 p.u. and duration ranging from 0.5 cycles to 60 seconds [6]. A voltage dip resulting in a residual voltage of less than 0.1p.u or a complete loss of supply on one or more phase conductors for a duration between 0.5 cycles and 3 s is termed a STPI [1]. Voltage dips are mainly caused by short circuits and the starting of large induction motors [4]. Voltage dips can be balanced or unbalanced. With balanced dips, all three phases drop in magnitude with the same amount and for an unbalanced dip, the three phases are affected differently. For a short period of time, a STPI may only appear as a flicker. A dip is much more likely to occur than a STPI [9]. Voltage dips have been classified into seven groups i.e. four types due to one or three phase faults and three due to two phase faults [11] [4]. According to survey reports, voltage dips of 0.1-0.3 p.u. below nominal for 3-30 cycle durations account for the majority of power system disturbances and are the major cause of industry process disruptions with single-phase and phase-phase faults accounting for the majority [11]. Conclusions from literature indicate that voltage dips due to three-phase faults are a serious problem for VSDs when compared to single-phase and phase-phase faults [4]. For the same voltage dip duration, a balanced three-phase dip or STPI is the most severe as it results in the reduction of the dc-link voltage which is proportional to the ac source voltage and if supply restoration is delayed can lead to a trip on undervoltage protection. Unbalanced dips (even for the most severe ones), do not result in the dc-link voltage dropping below 80% of its nominal value and can be tolerated by adding a relatively small amount of dc-link capacitance [4]. This research focuses on a balanced three-phase STPI because it results in the largest dc-link voltage drop and thus poses the highest trip risk to the VSD.

2.4. VSD DC-Link Undervoltage Protection

Every VSD is designed for full operation with a certain level of undervoltage, compensated by elevated input current. Such operation results in a trade-off in performance parameters such as torque developed, speed and current drawn. The VSD can be operated outside specifications for defined criteria or limits [2]. Once the dc-link voltage falls below the design threshold, the VSD trips on undervoltage protection. Undervoltage trip setting for most VSDs is 50-60% of nominal dc-link voltage [12]. Thus, SAGC voltage dips with a residual value of up to 0.75 V_{dc} do not pose a trip risk but affect performance parameters. Most low-voltage VSDs can only survive a STPI of up to 0.05 s and will most likely trip when exposed to a SAGC 0.2 s STPI.

VSDs are equipped with dc-link undervoltage protection:

- as a safety measure against losing control of the drive if the power supply cannot sustain adequate voltage for the control electronics [5];
- as a protective measure against processes which cannot tolerate speed and torque variations and to protect equipment against damage especially when the voltage dip is cleared.

VSD tripping under voltage dips can occur due to several phenomena which include trip due to an active intervention by the undervoltage protection, VSD controller trip, overcurrent protection trip during/post dip due to capacitor inrush charging currents or process driven trip. The most common cause for VSD trips is undervoltage protection trip [4].

The sensitivity of VSDs to voltage dips are affected by many factors which include voltage dip types, loading and operating condition of the drives, threshold settings in the protection of the drives and the control method employed (v/f versus vector control) [7] [13] The more severe a voltage dip, the higher are the chances of the VSD tripping. The larger the load torque or speed, the higher the probability of the VSD tripping. A VSD utilising vector control has a better chance to ride-through a voltage dip when compared to one on v/f control. Other factors affecting the ride-through capability of VSD include harmonics and initial phase angle. Modern drives restart immediately when the voltage is restored. Others restart after a certain time delay or only after a manual restart. The various automatic restart options are dependent on whether the driven equipment or process tolerates variations in speed and torque during the dip.

In order to maintain full power flow during a symmetric voltage dip, load current has to increase inversely to the voltage dip. Depending on severity of the dip, this can lead to the VSD tripping on overcurrent protection [2]. During a STPI, power required by the load is drawn from the dc-link capacitor resulting in the capacitor voltage dropping. Depending on the duration of the STPI, the VSD can trip on dc-link undervoltage protection. Balanced voltage dips or STPI are usually used to set dc-link undervoltage protection whilst asymmetric dips are used to set overcurrent protection of VSDs [6].

2.5. VSD DC-link Energy Balance During a Voltage Dip and STPI

During a voltage dip, the energy flow to the load is disturbed [2]. Energy stored in the VSD and rotating masses in the system will be consumed by the load if the energy from the grid isn't restored. Energy within the system during a voltage dip or STPI can be represented by (1), the energy balance equation.

$$E_L = E_c + E_{kin} \tag{1}$$

Where E_L is the energy to the load, E_C is the energy supplied by the capacitor and E_{kin} is the kinetic energy in the rotating masses [14]. The kinetic energy E_{kin} is given by

$$E_{kin} = \frac{1}{2} J_t \omega^2 \tag{2}$$

where J_t is the inertia of the rotating assembly and ω is the rotational speed. The energy stored in a capacitor E_C is given by

$$E_C = \frac{1}{2} C V^2 \tag{3}$$

where C is the capacitance and V is the capacitor voltage. During a voltage dip, the capacitor and rotating masses provide energy to the load resulting in the reduction of voltage and speed respectively.

E_L can thus be written as

$$E_L = \frac{C}{2}\{V_c^2(t_2) - V_c^2(t_1)\} + \frac{J_l}{2}\{\omega^2(t_2) - \omega^2(t_1)\} = \int_{t_1}^{t_2} T_l\, \omega . \delta t \quad (4)$$

where T_l is the load torque, t_1 and t_2 are initial and final time instances. It can be seen from (4) that the behaviour of a VSD during a voltage dip of duration t is influenced by three main parameters:

- The dc-link capacitance C which determines the electric energy E_C stored in the dc-link.
- The load inertia J_l which determines the mechanical energy E_{kin} stored in the rotating parts.
- The motor load $T_l\, \omega$.

2.6. Inrush Currents

Inrush current in a VSI VSD is generated when the dc-link capacitor is charged. This is due to the capacitor behaving like a short circuit when voltage is initially applied. Such inrush currents can range from several tens to several hundreds of amperes [15] [16]. Left unaddressed, such inrush currents can damage rectifier components, cause nuisance tripping of incoming ac breaker, cause dc-link to fall out of voltage regulation and cause electromagnetic interference in adjacent circuits [6] [18].

The magnitude of inrush current into a capacitor is determined by the slope of the voltage ramp and is given by.

$$i_{inrush} = C\frac{dV}{dt} \quad (5)$$

where i_{inrush} is the magnitude of inrush current,

C is the capacitance

dV is the change in voltage across capacitor during charging time

dt is voltage rise time

A number of techniques for limiting capacitor inrush charging currents are discussed in [19]. These can be categorized under two main broad categories i.e. passive inrush limiting and active inrush limiting. Passive inrush limiting include use of series connected resistors, inductors and negative temperature coefficient resistors to limit the magnitude of the inrush currents [20]. Active inrush limiting techniques are premised on increasing the voltage rise time across the dc-link capacitance thereby slowing down the rate at which the capacitors charge [17]. These include the use of soft starters, load switches and power switching.

A typical circuit used for limiting inrush currents is shown in Figure 2-2. Resistor R limits the inrush current due to dc-link capacitor C. When the VSD is switched on, R is kept in the main power flow circuit thus limiting the magnitude of the inrush current.

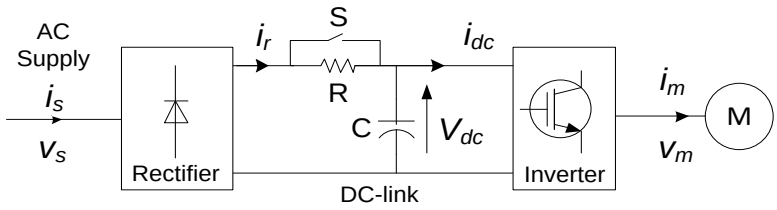


Figure 2-2. VSD Circuit with Pre-charging Facility

Once the dc capacitor is almost fully charged, *R* is bypassed by a shunt switch S to minimise losses.

2.7. Harmonics due to VSDs

VSDs generate harmonic currents through two main mechanisms. The first mechanism is the rectifier operation which injects harmonic currents into the supply system by an electronic switching process. The second mechanism is the inverter operation. A three-phase input rectifier with a dc-link capacitor draws current in abrupt pulses (ripples) due to line commutation of rectifier diodes coupled with the charging and discharging of the dc-link capacitor. These ripples cause harmonic injection into the supply system [21]. A larger electrolytic dc-link capacitor generates significant input current harmonics and distortion [22] [23]. In order to reduce line current harmonics and the associated voltage distortion to within necessary limits as per NRS048 and IEEE 519 guidelines, passive or active harmonic mitigation techniques are required. Depending on the application, the mitigation may be applied as an integral part of the VSD (e.g., a line harmonic filter) or as a standalone item (e.g., an active or passive filter connected to a switchboard). The mostly used mitigating techniques for VSDs include the use of reactors, passive filters, active filters, active front-end rectifiers, 12 or 18 pulse front-end converters [24]. Most of these measures are applicable for continuous harmonic injection mitigation. A larger capacitor connected permanently onto the dc-link results in the continuous injection of harmonics.

2.8. VSD Summary

VSI drives with a passive front-end are more susceptible to voltage dips. When compared to other voltage dips, a STPI is the worst voltage disturbance that a VSD can be subjected to because it results in the biggest voltage drop on the dc-link of a VSD. The ability of a VSI-PWM to ride-through a voltage dip is mainly influenced by the energy storage capacity of the dc-link capacitor, the speed and inertia of the load, the power consumed by the load and the undervoltage trip protection settings. The capacitor installed in the dc-link of PWM-VSI drives is used primarily for filtering rectifier output voltage. It also provides limited energy storage for a VSD to ride-through voltage dips. Most trips occurring during a voltage dip are due to dc-link undervoltage protection. Restoration of supply after a voltage dip is accompanied with inrush current flow as the dc-link capacitor charges up, which if not limited can cause damage to equipment and cause nuisance trips. Increasing the capacitance on the dc-link results in an increase in harmonic pollution on the supply.

Chapter 3

VSD Under-voltage Ride-through Improvement Methods

3.1. Introduction

The ride-through capability of a VSD can be defined as the ability of a VSD to remain operational during a voltage dip or STPI i.e. no protection trip on dc-link undervoltage. Various research work has investigated a number of alternatives of improving the ride-through capability of a VSI VSD to voltage dips [5]-[6] [8]-[12]. These include the use of capacitors (ordinary/super capacitors), battery back-up systems, motor-generator sets, flywheel energy storage, super conducting magnetic energy storage, fuel cells. A detailed assessment of these and other undervoltage ride-through alternatives is made in this chapter.

3.2. Undervoltage Ride-through Techniques

Classic undervoltage ride-through of a VSD usually implies zero torque at the motor shaft during the dip or STPI. Advanced control strategies with modern power electronics have opened new ride-through possibilities which include reduced and full torque ride through [2]. Three types of voltage dip ride-through improvement alternatives for low voltage VSDS are reported in literature [5]-[6]. These are, hardware modifications (e.g. increasing ac side inductors, dc-link capacitance), improvement in power supply conditions (e.g. use of UPS) and modifying control algorithm (e.g. load inertia energy recovery). All these alternatives are based on maintaining the dc-link voltage above the undervoltage trip level during a voltage dip. They essentially ensure the supply of sufficient energy to the load and control electronics to maintain operation during a dip. Energy may be from a stored source, or from the supply via boost converters, or from the kinetic and magnetic energy of the machinery. For existing drive topologies, alternatives available for improving ride-through capability include adding more capacitance to the dc-link, use of load inertia, operating VSD at reduced speed and/or load, and using lower voltage motors [11]. Alternatives for improving ride-through capability can also be classified according to whether or not they can allow ride-through for a total loss of power (STPI). Invariably, those that can offer ride-through for a STPI incorporate an energy storage device.

3.2.1. Use of additional ordinary capacitors

Capacitors installed on the dc-link of a VSD are used primarily for the control of voltage ripple on the dc-link.[25] Typical values are between 75 and 360μF/kW [14]. They also store a limited amount of energy which can be supplied to the load during a voltage dip or STPI. Additional electrolytic capacitors can be connected to the dc-link resulting in an overall increase in the dc-link capacitance. A larger capacitor will sustain the dc-link voltage longer for the same loading but offer limited ride-through since

its voltage magnitude decays as well. Once it reaches the undervoltage threshold, the VSD will trip. When a 3-phase dip initiates, the ac supply voltage rms becomes less than the dc-link voltage thus reverse biasing diodes in the rectifier circuit. During this time, all electrical energy for load comes from capacitor. The capacitor will continue to discharge until there is a new equilibrium point between ac supply and dc-link voltage. The rate at which the capacitor discharges is determined by the load and capacitance. The duration during which a capacitor discharges is determined by magnitude of dip.

In the event of a STPI, the VSD dc-link capacitor is left to provide all the power to the motor and will quickly drop in voltage. The VSD normally trips on undervoltage protection within a few milliseconds [1]. A comparison of VSDs from different manufactures indicates that most low-voltage VSDs can only survive a STPI of up to 0.05s. DC-link voltage dynamics can be analysed and assessed through either the current-voltage relationship or using the electrical energy storage in the capacitor [26]. The energy stored in a capacitor with capacitance C and voltage V is given by:

$$E = \frac{1}{2}CV^2 \tag{6}$$

If V_2 is the lower voltage threshold below which a VSD will trip, for a load power P, the time t for the capacitor to discharge from nominal dc-link voltage V_1 to V_2 can be calculated from:

$$Pt = \frac{1}{2}C\{V_1^2 - V_2^2\} \tag{7}$$

The capacitance C required for a ride through duration t can be calculated from (7) leading to

$$C = \frac{2Pt}{V_1^2 - V_2^2} \tag{8}$$

Advantages and disadvantages

Advantages for using additional capacitors include the solution being simple and rugged. There is no transfer time when switching from one power source to another. Capacitors can handle rapid charging and discharging cycles, have a longer life-cycle, require minimal or no maintenance and do not require any specialised ventilation, handling or disposal. However, capacitors require large cabinet space, additional pre-charge circuits and safety considerations. This solution is very expensive for larger loads but suitable for smaller loads. A larger capacitor also increases the level of harmonic pollution on the VSI input supply.

3.2.2. Use of batteries

Batteries can be used as energy storage devices which supply power to the dc-link and thus maintain the voltage during a voltage dip or STPI. They operate similarly to adding capacitive energy storage with the advantage that their energy ratio per volume ratio is much higher than standard capacitors [27] . Batteries

have a lower power density when compared to capacitors. The required battery current is dependent on the load. Because batteries store energy in electrochemical form, their operation is subject to several limits which include cycle life and depth of discharge. In addition, the ambient temperature and the proper charging current must be monitored and kept within limits [11].

Advantages and disadvantages

Batteries are readily available on the market and can provide ride-through for deep sags and full outages with transfer time being almost instantaneous. The rapid charging and discharging cycles damage the batteries resulting in a low life cycle, increased maintenance and replacement costs [11]. Additional hardware and space is required. In the case of lead acid types, special ventilation systems will be required to ensure safe exhaust of gases emitted during operation of the batteries. The electrolyte being corrosive will need to be properly disposed off when depleted.

3.2.3. Use of supercapacitors

Supercapacitors, also known as electric double-layer capacitors, electrochemical double layer capacitors (EDLCs) or ultracapacitors are electrochemical capacitors that have an unusually high energy density when compared to common capacitors, typically several orders of magnitude greater than a high-capacity electrolytic capacitor [28]. To compare the power and energy capabilities, a representation known as the Ragone plot or diagram has been developed. Figure 3-1 shows a simplified Ragone plot which indicates that batteries can be considered to be high-energy storage devices, whereas supercapacitors are considered to be high-power energy storage devices. Supercapacitors fill the void gap among energy storage devices between batteries and common capacitor. Supercapacitors offer substantial increases in energy density over conventional capacitors due to the choice and preparation of the electrode materials and increases in the effective capacitive plate surface area [11] [29].

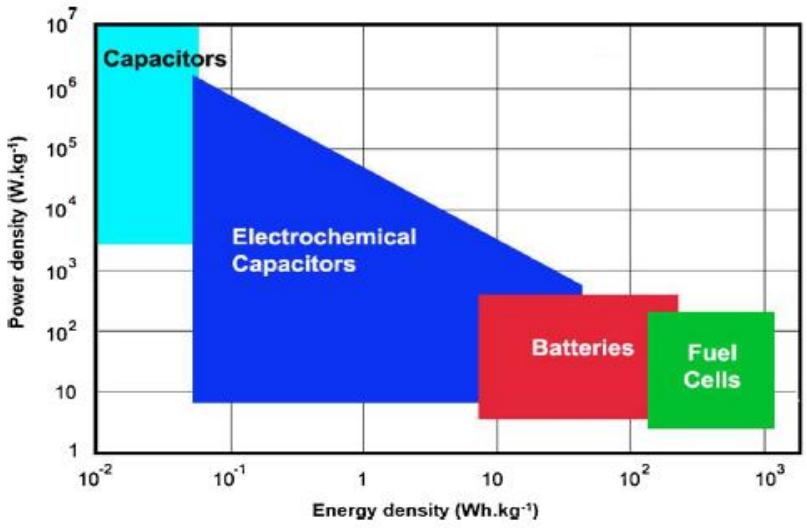


Figure 3-1. Ragone Chart: Power Density as a Function of Energy Density for Various Energy Storage Devices [30]

Advantages and disadvantages

Supercapacitors can provide ride through for severe dips and STPI. They offer long life cycle and fast recharges rates. Their state of charge can be monitored easily. Minimal maintenance is required. Additional hardware and space are required although not as much as with standard capacitors. Supercapacitors have a low cell voltage rating typically 2.7 V. This makes them difficult to use in high voltage applications. When required to be used in such applications, large series banks can be assembled. Such series strings can result in unbalanced charging among cells which pose a reliability issue as the lifetime of supercapacitor cell/module is mostly determined by the individual cell voltage and temperature [27] [31]. To address risk of unbalanced charging, balancing circuits are required which add onto the already high of supercapacitors. Addition of supercapacitors to a dc-link result in an increase of in-rush charging currents. Just like capacitors, they require the re-design of the rectifier and pre-charging circuits of the VSD.

3.2.4. Motor-Generator Sets

Motor-generator (M-G) sets use their rotating mass to supply energy during a voltage dip or STPI. They can provide up to 15 s of ride-through for STPI at full load [11]. A M-G set can supply power directly to the dc-link of the VSD through an AC-motor driven DC generator. In order to reduce the size of the M-G set and the rotor mass, a flywheel can be used for the storage of kinetic energy.

Advantages and disadvantages

M-G sets can provide ride-through for severe dips and STPI. They are very reliable and can provide up to 15 s of ride through for STPI. However, due to increased number of rotating components, considerable maintenance is required resulting in increased life cycle costs. Additional hardware and space are also required.

3.2.5. Use of flywheels

A flywheel is a mechanical storage device which stores energy in the form of rotational kinetic energy. The input energy to the flywheel ESD is usually drawn from an electrical source coming from the grid. It typically consists of a spinning rotor, M-G set, bearings, power electronics interface and a containment. A typical flywheel system is shown in Figure 3-2.

The flywheel speeds up as it stores energy and slows down when it is discharging. The rotating flywheel is driven by an electrical-generator (MG) performing the interchange of electrical energy to mechanical energy and vice versa.

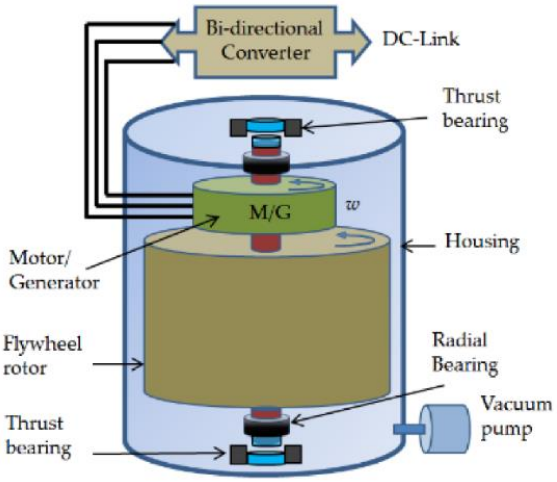


Figure 3-2. Structure and Components of a Flywheel[32]

Advantages and disadvantages

Flywheels have a high energy and power density. They respond instantly to an energy demand. They can provide ride-through for severe dips and STPI. When used with M-G, they significantly reduce the size and necessary mass of M-G sets. They are, however, expensive, require space and are maintenance intensive.

3.2.6. Superconducting Magnetic Energy Storage

A superconducting magnetic energy storage system (SMES) circulates a large amount of current in a superconducting coil or magnet which is then supplied to the system when required. The SMES is a dc current source rather than a voltage source.

Advantages and disadvantages

SMES can handle rapid repeated discharging and charging without affecting their performance. They are reliable and require little maintenance. However, to remain superconducting, the coil or magnet must be cooled to cryogenic temperatures which requires a fairly sophisticated refrigeration subsystem [11]. Additional hardware and space are required. The system is expensive and poses safety concerns.

3.2.7. Boost converters

A boost converter maintains the dc-link voltage to a set point during the dip. The boost converter can be connected to the dc-link of a VSD, but more commonly is connected in parallel to the VSD. It uses the remaining voltage during a dip to supply the dc-link. They do not use an energy storage device. Boost converters can be integrated into new drives between the rectifier and the dc-link capacitors or retrofitted as an add-on module [11] [33]. During a voltage dip, the boost converter will sense a drop in the dc-link

voltage and begin to regulate the dc-link to a minimum voltage required by the inverter. Another boost converter type utilises the VSD dynamic braking semiconductor as in Figure 3-3.

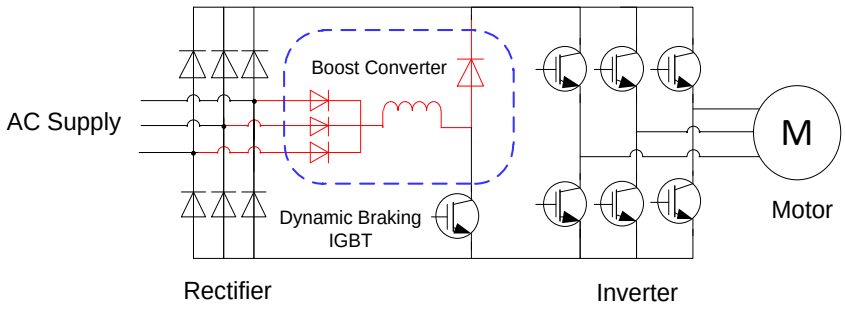


Figure 3-3. VSD with a Boost Converter Utilising Dynamic Braking Semiconductor

This configuration requires modifications to the VSD control algorithm to allow for the use of the dynamic braking semi-conductor.

Advantages and disadvantages

Boost converters can provide ride-through for deep voltage dips up to 50%. The dc-link voltage can be regulated as required by the inverter and is user adjustable. Boost converters however, cannot provide ride-through for a STPI. They require additional hardware which will have to suitably rated due to increased current drawn during a dip. Such additional hardware increases fault current at the device which would cause more damage in the event of a fault.

3.2.8. Active Rectifier Front End VSD

An active front end VSD is realised by replacing the diode rectifier with an active PWM rectifier. Such a system is available from many VSD manufacturers up to 500 kVA. The active front end provides a boost function which controls the dc-link voltage during a voltage dip. It provides four-quadrant power flow which enables regenerative braking. This feature can add improved efficiency in some applications. It also minimises distortion on the line side of the VSD. Ride-through capability is limited only by the current rating of the rectifier. A suitable rectifier de-rating is necessary to provide full-power ride through under a dip. By de-rating the rectifier by a factor of 1.5, the ride-through capability can be extended to dips of up to 40% at full load [5].

Advantages and disadvantages

PWM rectifiers minimise input current harmonics and enhances compliance to IEEE 519 harmonic limits. They allow for power flow in both directions enabling regenerative braking. They are however expensive (almost twice the cost of a diode-based rectifier), larger in size compared to diode-based rectifier, difficult to retrofit existing VSDs and cannot provide ride-through for STPI.

3.2.9. Operating VSD at Reduced Speed/Load

The dc-link current varies with the frequency of the drive for variable torque loads. A reduction in the speed and consequently the load torque, will result in a reduction in the dc-link current and therefore be able to operate for a longer period during a voltage dip. Similarly, if the motor load were reduced, the dc-link current would be reduced and thus a longer ride-through duration can be achieved.

Advantages and disadvantages

Operating the VSD at reduced speed or load does not require any additional hardware. At 50% speed and load, it would provide four times the ride-through of a normal drive system [11]. This solution however is only applicable if the process does tolerate a reduced speed or load operation. It is only useful for variable torque applications.

3.2.10. Oversize Drive

Oversizing the drive inherently offer some additional ride through in the drive because the DC capacitor size varies linearly with the power rating of the VSD, so increasing the size of the drive increases the size of the capacitors and the ride-through.

Advantages and disadvantages

Use of an oversize drive does not require any additional hardware. An oversize drive is costly as this requires replacement of existing drives with a significantly more expensive drive. This alternative does not always guarantee success.

3.2.11. Use of load inertia and electromagnetic energy recovery

Use of load inertia and electromagnetic energy recovery interventions aim to maintain the dc-link voltage above the trip threshold during the undervoltage condition by converting kinetic energy in the rotating masses and electromagnetic energy stored in the motor windings into electrical power through the operation of an induction motor as a generator. This strategy is applicable where the rotating systems have sufficient rotational inertia. For existing VSDs, the inverter control software can be modified such that when a voltage dip causes the dc-link voltage to fall below a specified threshold, the inverter will adjust to operate at a frequency slightly below the motor frequency, causing the motor to act like a generator. The drive will absorb a small amount of energy from the rotating load to maintain the dc-link at the specified level. Commercial VSDs are available on the market with this feature, and will maintain the specified dc-link voltage for 2s during a dip that does not exceed 20% [11].

Electromagnetic energy in the form of flux stored in motor windings can also be recovered to support the VSD dc-link during a STPI or dip. This type of energy recovery involves forcing the inductance of the motor windings to act as a current source and feeding this stored energy back into the dc-link [34]. The

motor requires flux to act as an induction generator and hence this type of recovery is normally possible only after kinetic energy recovery.

Advantages and disadvantages

This solution does not require any additional hardware. Only software modifications are required. Commercial drives with this capability are available on the market. There are no delays in accelerating the motor once the dip clears since phasing between the drive and motor is maintained and the motor's magnetic field is not de-energised. During a voltage dip, however, motor speed is reduced and the torque is reversed which may not be acceptable for certain types of loads. Ride-through duration is dependent on the load inertia.

3.3. Selection of Appropriate VSD Ride Through Enhancement Technology

Research analysis on the most cost-effective and practical VSD ride-through improvement alternatives based on the cost, rating and ride-through duration show that no single ride-through improvement alternative can meet the requirements for all applications which creates a need for a comprehensive analysis on a case by case basis [11]. Figure 3-4 summarises VSD ride-through characteristics and cost.

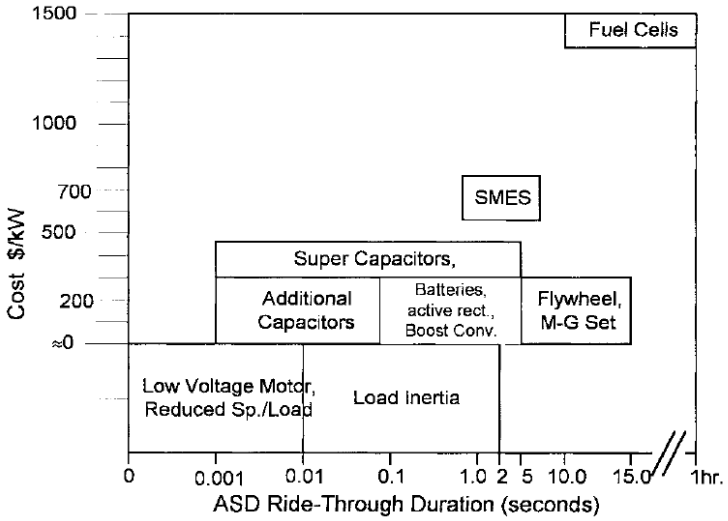


Figure 3-4. Ride-through time versus cost [11]

In order to determine the cost effectiveness of implementing a VSD ride-through solution, interruption costs can be estimated. Interruption costs can be estimated using the following equation:

$$Interruption\ Cost = Production\ Loss + Outage\ Costs - Outage\ Savings \quad (9)$$

Using average annual events statistics, downtime costs can be predicated and a comparison made with the cost of installing a VSD ride-through improvement. Figure 3-5 suggest the most appropriate VSD ride-through technique for critical loads requiring full power (full speed and torque) ride-through.

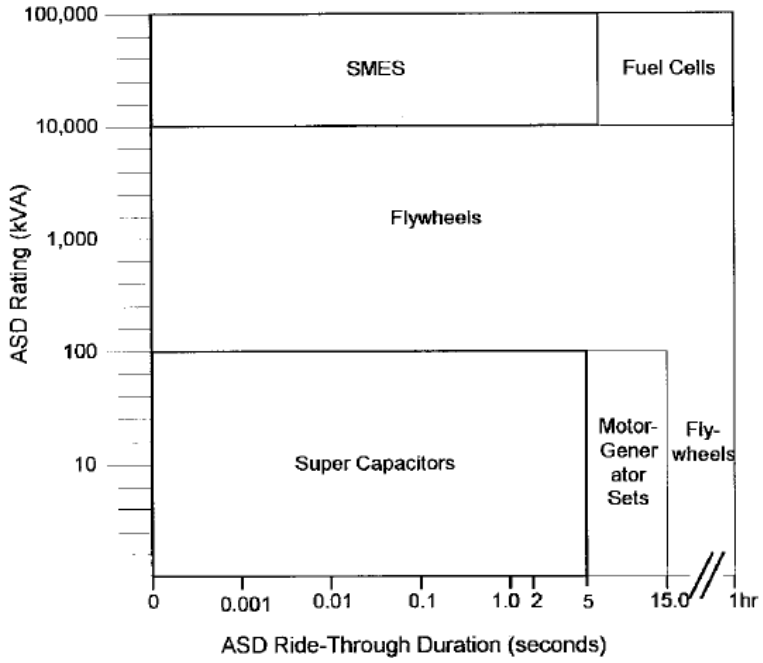


Figure 3-5. Ride-through duration versus VSD rating for full power applications [11]

Ride-through improvement of an existing VSD to a STPI requires a solution incorporating an energy storage to provide required power during loss of supply. For low voltage (<1000 V), low power (100 kW) applications, ordinary capacitors, supercapacitors and batteries are suitable candidates. For new VSDs, the requirements for STPI ride-through capability can be specified upfront and provisions made during design stage. Improving the ride-through capability of existing VSDs by adding extra dc-link capacitance results in increased inrush currents which would necessitate resizing of rectifier and pre-charge circuits and upstream protection equipment. If the highlighted challenges can be addressed, use of additional capacitors can become an attractive alternative for use on existing VSI VSD requiring STPI ride-through capability.

3.4. Summary of VSD ride-through enhancement alternatives

Various VSD ride-through improvement alternatives to voltage dips were explored. Application considerations, advantages and disadvantages of each alternatives were highlighted. The most cost-effective and practical ride-through solutions were matched with the most appropriate VSD kVA ratings, and ride-through durations.

Chapter 4

Proposed Voltage Dip Compensating Module

4.1. Introduction

Improving the ride-through capability of an existing VSD to a 0.2 s STPI requires adoption of a solution that incorporates an energy storage device. The proposed solution should ensure that the VSD electrical and thermal ratings are not exceeded. Solution should minimise harmonic pollution on ac supply. The proposed module should minimize torque transients to avoid damage to mechanical system components. Torque and speed reduction should be minimised to within 10% pre-dip values. A modular solution which allows for upscaling is preferable. Details of the proposed solution including selection of components, circuit analysis and sizing of key components are explained in this section.

4.2. Ride-through Requirements

The proposed voltage dip compensating module (module) is required to ensure that a low voltage source inverter variable speed drive can ride through a 0.2 s STPI while maintaining load torque and speed within permissible full load variations. Table 4-1 summarises the ride-through specifications.

Table 4-1: Ride-through Specification Requirements

Ride-through time	0.2 s
Maximum voltage disturbance	STPI
Minimum acceptable dc-link voltage	85% nominal
Induction motor power rating:	1.5 kW

4.3. Selection of Module Components

4.3.1. Energy Storage Device Selection

There are three technical characteristics that determine which specific energy storage technology is suitable for a particular application. These include energy density and power density, charge and discharge time which must be aligned with proposed use and cycle life [35]. Other factors to consider when deciding selection also include cost and spare constraints. From [11], additional capacitors, super capacitors and batteries are possible candidates for a 1.5 kW VSD requiring a 0.2 s STPI ride-through capability. To achieve the required application voltage rating, it might be necessary to connects capacitors in series. For a 400 Vac, 1.5 kW VSD with a peak dc-link voltage of 566 V, at least 210 supercapacitor units with a cell voltage of 2.7 V are required. Besides the cost associated with such a large number of cells, connecting these in series require special cell balancing schemes to avoid overloading individual cells. Batteries have a low power density and cannot handle repeated quick charging and discharge cycles.

They have a low cell voltage and would require a large series connection string to achieve required application voltage. Ordinary electrolytic capacitors on the other hand have a high cell voltage (typically maximum 500 Vdc) and are cheaper than supercapacitors. Due to cost limitations, for purposes of this research, ordinary electrolytic capacitors were used. It should be easy to extend the solution to a supercapacitor considering the similarities in operating behaviours of the two.

4.3.2. Switching Device Selection

To minimise harmonic pollution associated with an increase in dc-link capacitance, additional capacitance needs to be connected to the dc-link only when compensation and charging is required. This requires use of switching devices for connecting and disconnecting the capacitor from the dc-link. A comparison of VSDs from different manufactures indicates that most VSDs can only survive a STPI of up to 0.05 s. Thus, the detection of a STPI, connection of capacitor to dc-link and positive flow of energy into the dc-link should be done within 2.5 electrical cycles if an undervoltage trip of the VSD is to be avoided. Switching speed is of paramount importance. Electromechanical contactors are slow and are prone to contacts bouncing during operating. IGBTs and MOSFETS on the other hand are fast, do not consume a lot of power when switched on and do not exhibit bouncing phenomenon. Choosing between IGBTs and MOSFETS is very application specific. Cost, size, speed and thermal requirements require due considerations. IGBTs are suited for high voltage (>1000 V), low frequency (<20 kHz) and large output power applications whilst MOSFETSs are suited for high frequency (>200 kHz), low voltage (<250 V) and low output power applications. A detailed comparison between IGBTs and MOSEFT are made in [36]. For this specific application, the IGBT appears to be the device of choice due to the application involving low power (1.5 kW), low frequency of switching (<5 kHz) and medium voltage (>600 Vdc).

4.3.3. Inrush Current Limiting

Charging of a capacitor results in an inrush current. To avoid damaging existing VSD rectifier diodes and dc-link components due to inrush currents associated with charging the VSD capacitor (during compensation) and additional capacitor, an inrush current limiting scheme is required. A basic scheme utilising series fixed resistors in is proposed.

4.4. DC-link Voltage Compensation

VSI PWM VSDs have a dc-link comprising 2 capacitors connected at the neutral point of the dc-link giving rise to a neutral clamped inverter [37]. The neural point is typically grounded. The design and operation of the PWM inverter is based on the neutral point being approximately half the dc-link voltage (V_{dc}), thus the voltages of the dc-link capacitors are approximately balanced. This gives rise to a voltage of + and - voltage for the 2 rails with respect to the neutral point. The positive rail of the dc-link is denoted as + dc-link and the negative rail as - dc-link.

Most VSI VSDs are equipped with a provision to access the dc-link rails. This provision is mostly used for connecting a dynamic braking resistor. Interface between the VSD and module is to be done through these dc-link connection points. Ride-through improvement to a 0.2 s STPI is to be achieved by energy injection into the VSD dc-link during the STPI. Figure 4-1 shows the single line drawing of the VSD and the compensation leg of the module.

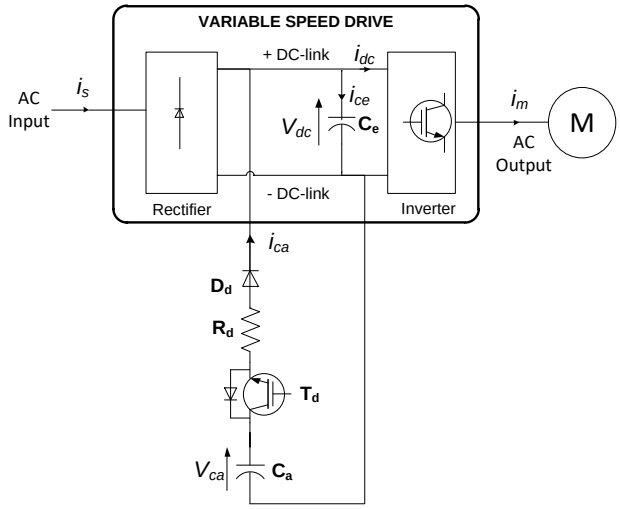


Figure 4-1. Single Line Diagram of VSD and Voltage Dip Compensating Leg

The compensation leg is made up of an energy storage capacitor C_a and a switching circuit comprising of IGBT T_d, diode D_d and resistor R_d. IGBT T_d connects C_a to VSD dc-link when compensation is required and disconnects it at the end of compensation. Resistor R_d is used for limiting inrush current generated at start of compensation when VSD capacitor charges up. Diode D_d ensures directional power flow from the capacitor into the dc-link.

4.4.1. Analysis of Voltage Dip Compensating Module During Compensation

A PWM inverter - ac motor assembly can be modelled in different ways. It can be modelled as a resistance, a constant power load, a constant current load or a more complex model [38] [40]. When there is a change in inverter voltage, an ac motor can be considered as a constant resistance, viewed from the dc side of the VSD if the motor speed is supposed to be constant. If the speed changes, the ac motor can be considered a constant power load. Extensive simulations by [40] show that a constant current model gives intermediate results between a constant resistance and constant power model. The constant current load model for the inverter and ac motor will be utilised for the VSD analysis.

The equivalent circuit of the VSD and module during compensation is shown in Figure 4-2. The system is assumed to have a low inertia. Thus, kinetic energy extracted from rotating masses is minimal and can be omitted from the analysis. Capacitor voltage $V_c(t)$ at time t during charging or discharging of a pre-charged capacitor is governed by

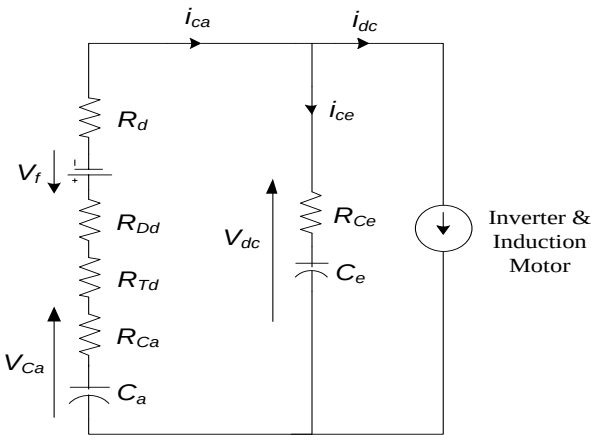
$$V_c(t) = V_c(t_2) + \left(V_c(t_1) - V_c(t_2)\right)e^{-t/RC} \quad (10)$$

where $V_c(t_2)$ final steady state capacitor voltage

$V_c(t_1)$ initial steady state capacitor voltage

R resistance between the two capacitors

C capacitance of the capacitor



R_{ca} Capacitor C_a equivalent series resistance

R_{ce} Capacitor C_e equivalent series resistance

R_{Td} IGBT T_d on resistance

R_{Dd} Diode D_d on resistance

R_d Discharge inrush current limiting resistance

i_{dc} Inverter input current

i_{ce} Capacitor C_e charging current

i_{ca} Capacitor C_a discharge current

V_f Diode D_d forward voltage

V_{ca} Capacitor C_a voltage

V_{dc} DC-link voltage

Figure 4-2. Equivalent Circuit of Voltage Dip Compensating Module During Compensation

The current i_{ca} supplied by C_a in Figure 4-2 is given by

$$i_{ca} = i_{ce} + i_{dc} \tag{11}$$

The discharge leg resistance of the module, R_{disch} is given by

$$R_{disch} = R_{Ca} + R_{Td} + R_d + R_{Dd} \tag{12}$$

The total series resistance between C_a and C_e R_{total} is given by

$$R_{total} = R_{disch} + R_{Ce} \tag{13}$$

Combining (12) and (13), R_{total} can also be written as

$$R_{total} = R_{Ca} + R_{Ce} + R_{Td} + R_{Dd} + R_d \tag{14}$$

Assuming that C_a is initially charged to V_{ca} and C_e is charged to the dc-link voltage V_{dc}. Once T_d is switched on, C_a supplies energy to the dc bus voltage and charges up C_e towards V_{ca}. The total current i_{ca} supplied by capacitor C_a at time t is given by

$$i_{ca}(t) = \frac{V_{ca} - V_{dc} - V_f}{R_{total}} e^{-t/R_{total}C} + i_{dc} \tag{15}$$

Assuming that at the start of compensation (t=0), C_a is pre-charged to voltage V_C and dc-link voltage (voltage across C_e) has decayed to V_{dc_trig}, inrush current $i_{d,}$ can be calculated from

$$i_d = \frac{V_C - V_{dc_trig} - V_f}{R_{Ca} + R_{Ce} + + R_d + R_{Td} + R_{Dd}} \tag{16}$$

It can be deduced from (16) that the magnitude of inrush current at start of compensation is a function of dc-link to capacitor voltage and total series resistance between C_e and C_a at the instant of IGBT T_d and T_c closing. During a STPI the total energy E_{Ca} supplied by dc-link capacitors to the load and dissipated in R_{disch} is given by

$$E_{Ca} = P_i t = \frac{C_T}{2}\{V_{dc1}^2(t_1) - V_{dc2}^2(t_2)\} + i_{ca}^2 R_{disch} \quad (17)$$

where Pi power input into the PMW inverter

t STPI duration

$V_{dc}(t_1)$ dc-link voltage at start of STPI inception

$V_{dc}(t_2)$ dc-link voltage at time t_2

C_T total dc-link capacitance = C_e + C_a

For low power applications, loss due to R_{disch} is minimal and can be ignored and E_{Ca} is thus given by

$$E_{Ca} = P_i t = \frac{C_T}{2}\{V_{dc1}^2(t_1) - V_{dc2}^2(t_2)\} \quad (18)$$

From (18), dc-link voltage $V_{dc}(t_2)$ after time t is given by

$$V_{dc}(t_2) = \sqrt{V_{dc}^2(t_1) - \frac{2P_i t}{C_T}} \quad (19)$$

It can be seen from (19) that the final dc-link voltage is influenced by dc-link capacitance and the duration of the dip. For the same power demand, a large capacitance results in a smaller voltage drop and vice versa. The longer the duration of the dip, the larger is the voltage drop and vice versa. For a fixed dip duration, the final dc-link voltage can be determined by selecting a suitable value of C_a.

4.5. Capacitor Charging

After compensation, the additional capacitor requires charging in preparation for the next round of compensation. Charging of the additional capacitor is done from the dc-link once VSD parameters have stabilised after ac supply restoration. Figure 4-3 shows the single line drawing of the VSD and the charging leg of the module. The charging leg comprises capacitor C_a, IGBT T_c, resistor R_c and diode D_c. Charging occurs when IGBT T_c switches on thereby connecting C_a to the dc-link and is suspended when T_c is switched off. Resistor R_c limits C_a charging inrush current. Diode D_c ensures directional power flow from the dc-link to capacitor C_a. To avoid excessive loading of the dc-link during charging, soft charging of C_a is implemented. With this scheme, C_a charging current is not continuous but pulsed. This is achieved by configuring the charging circuit to switch off T_c once the dc-link voltage drops to below a pre-set value and switch it on when it recovers above a threshold. This repeated switching on and off results in a pulsed charging current.

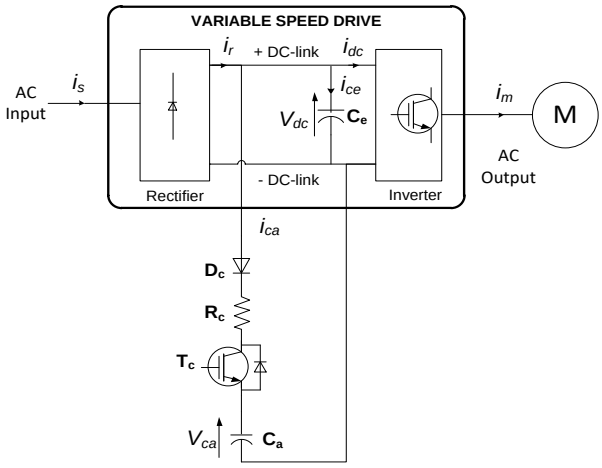


Figure 4-3. Single Line Diagram of Voltage Dip Compensating Module During Charging

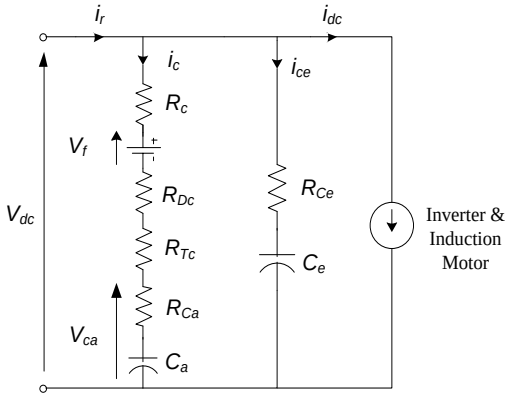
4.5.1. Analysis of Voltage Dip Compensating Module During Charging

The equivalent circuit for the VSD and module during charging is shown in Figure 4-4. Assuming that C_a has discharged to V_{ca} when the STPI clears. During charging, from (10), the voltage $V_c(t)$ across capacitor C_a at time t is given by

$$V_{ca}(t) = V_{dc} + (V_{ca} - V_{dc})e^{-t/R_{charg}C_a} \tag{20}$$

where R_{charg} is the charging leg resistance of the module and is given by

$$R_{charg} = R_{Ca} + R_{Tc} + R_{Dc} \tag{21}$$



R_{ca} Capacitor C_a equivalent series resistance
R_{Tc} IGBT T_c on resistance
R_{Dc} Diode D_d on resistance
R_c Charging current limiting resistance
i_{ca} Capacitor C_a charging current
V_f Diode D_c forward voltage
i_r Diode rectifier output current

Figure 4-4. Equivalent Circuit of Voltage Dip Compensating Module During Charging

The charging current $i_c(t)$ of capacitor C_a at time t is given by

$$i_{ca}(t) = \frac{V_{dc} - V_{ca} - V_f}{R_{charg}} e^{-t/C_a R_{charg}} \tag{22}$$

Inrush current that flows from rectifier (t = 0) can be calculated from

$$i_c = \frac{V_{dc_n} - V_{C2} - V_f}{R_{Ca} + R_{Tc} + R_C + R_{Dc}} \tag{23}$$

Where V_{C2} is the voltage of capacitor C_a at the end of compensation and V_{dc_n} is the normal dc-link voltage.

4.6. Complete Voltage Dip Compensating Module

Figure 4-5. shows the combined module for retaining the dc link voltage of a VSI VSD.

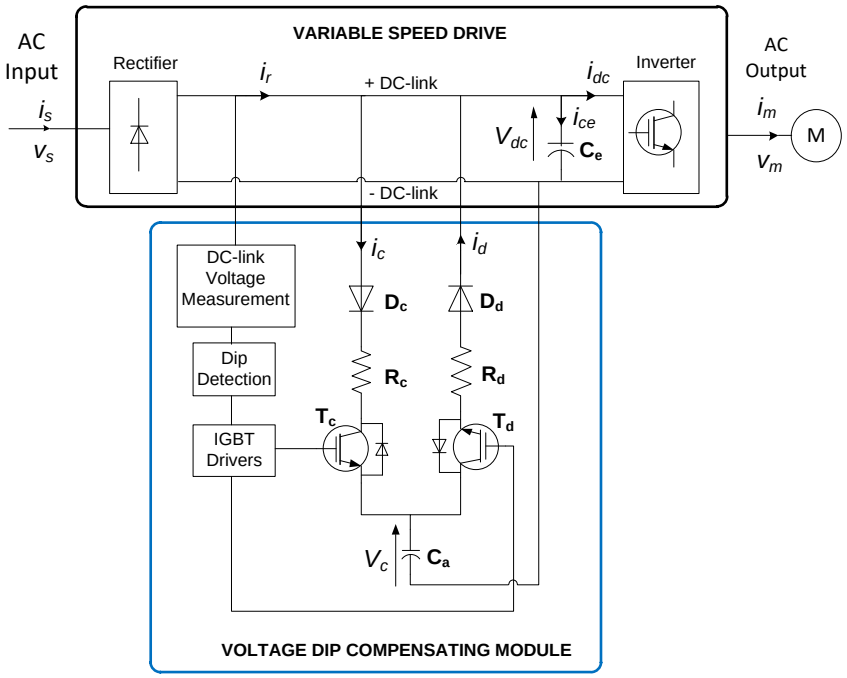


Figure 4-5. Proposed Voltage Dip Compensating Module Topology

DC-link voltage feedback provides reference for control. Detection of STPI and switching of IGBTs is controlled by the dip detection circuit.

4.6.1. Module Operating Philosophy

Before the module is activated after loss of supply, VSD capacitor C_e supplies all power to the load. This results in the dc-link voltage V_{dc} decaying. When V_{dc} has decayed to the module activation level V_{dc_trig}, IGBT T_d is switched on. This results in energy injection into the dc-link. Start of compensation is associated with the charging of C_e which results in an inrush current. Resistor R_d is incorporated in the discharge leg to ensure that this inrush current is kept within VSD dc-link component ratings. Diode D_d ensures directional power flow into the dc-link during compensation. As C_a injects power into the dc-link, its voltage decays accordingly. T_d is switched off once supply is restored.

Once ac supply is restored and VSD parameters stabilised, charging of C_a can commence. Charging is initiated by switching on of IGBT T_c. When charging starts, capacitor voltage is lower than the initial value due to compensation during the STPI. The connection of C_a results in an inrush current which is limited to rectifier and upstream component ratings by resistor R_c. Diode D_c ensures directional power flow from the dc-link to C_a. Charging stops when the capacitor has been charged to the required level. T_d and T_c are switched in a complementary fashion to avoid simultaneous charging and discharging of the capacitor.

4.7. Module Components Sizing

4.7.1. Discharge Inrush Current Limiting Resistor Sizing

From (16), R_d, the resistance required to limit inrush current at start of compensation can be calculated from

$$R_d = \frac{V_C - V_{dc_trig} - V_f}{i_{d_max}} - (R_{Ca} + R_{Ce} + R_{Td} + R_{Dd}) \tag{24}$$

where i_{d_max} is the maximum permissible output current of the VSD. A method for sizing inrush current limiting resistor R_d using readily available VSD and motor nameplate data is shown in Figure 4-6.

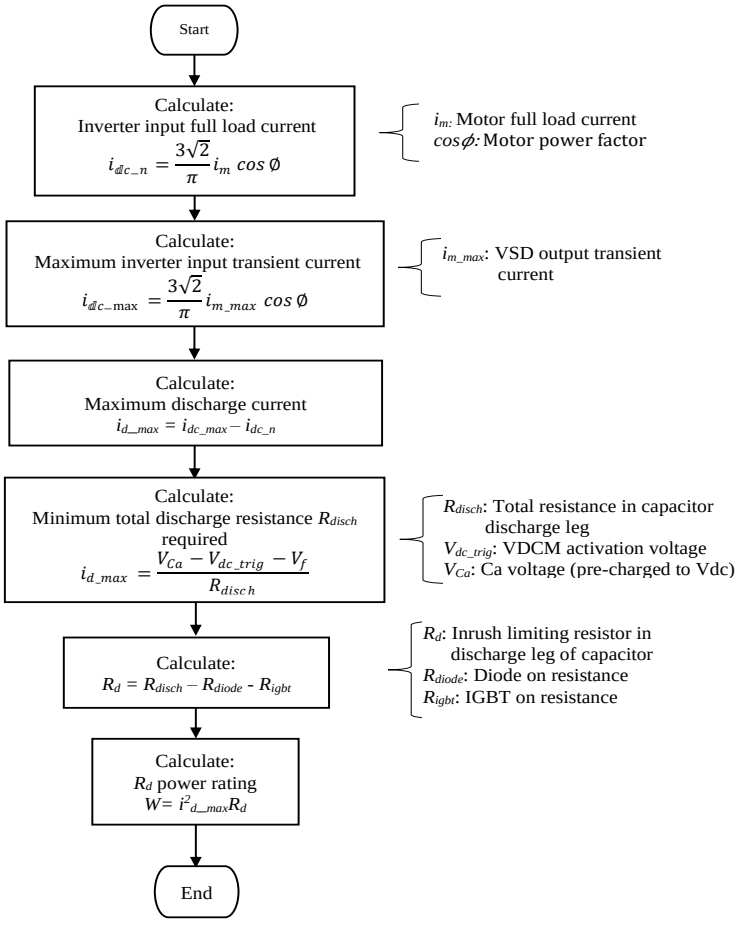


Figure 4-6. Discharge Inrush Current Limiting Resistor Sizing

4.7.2. Charging Inrush Current Limiting Resistor Sizing

Using (23), R_C, the resistance required to limit inrush current when C_a starts charging can be calculated from

$$R_C = \frac{V_{dC_n} - V_{C2} - V_f}{i_{c_max}} - (R_{Ca} + R_{Tc} + R_{Dc}) \tag{25}$$

where i_{c_max} is the maximum permissible input current into the VSD. Figure 4-7 summarises the steps for sizing R_C using readily available VSD and motor nameplate information.

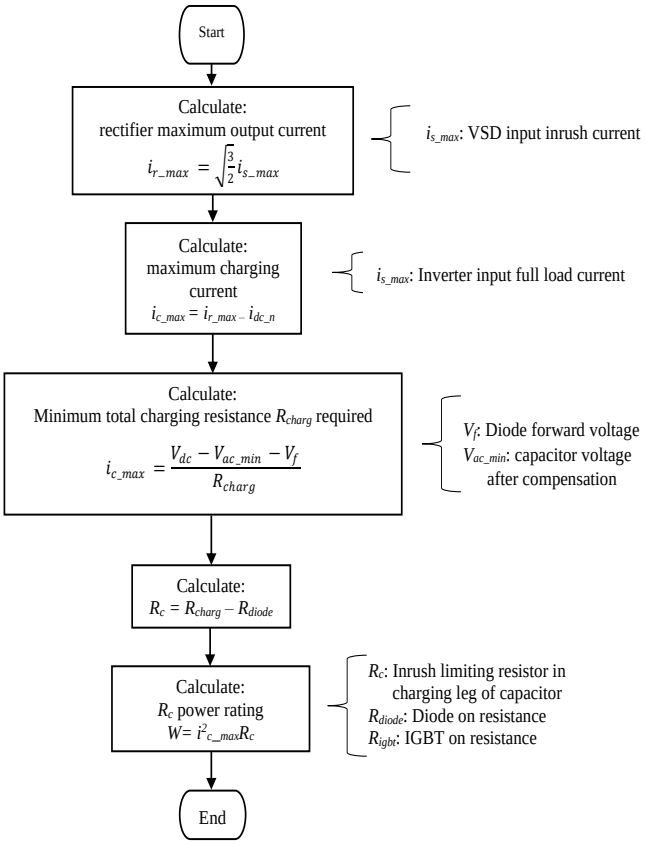


Figure 4-7. Charging Inrush Current Limiting Resistor Sizing Flowchart

4.7.3. Capacitor Sizing

The amount of additional energy injected into the dc-link during a STPI is determined by capacitor size. For this application, the VSD is required to ride-through a 0.2 s STPI whilst delivering rated load power. A method for sizing this capacitor using readily available data (e.g. motor nameplate, VSD nameplates, etc) is proposed. This is shown in Figure 4-8.

4.7.4. Diode Sizing

The main parameters considered for specifying a diode include its forward current, peak reverse voltage, forward voltage drop, leakage current and junction operating temperature. Peak reverse voltage refers to the maximum voltage a diode can withstand in the reverse direction. Maximum forward current refers to the maximum current that the diode can carry in the forward direction when the case temperature is maintained at a specified value between 25ºC and 75ºC below the maximum allowable junction temperature.

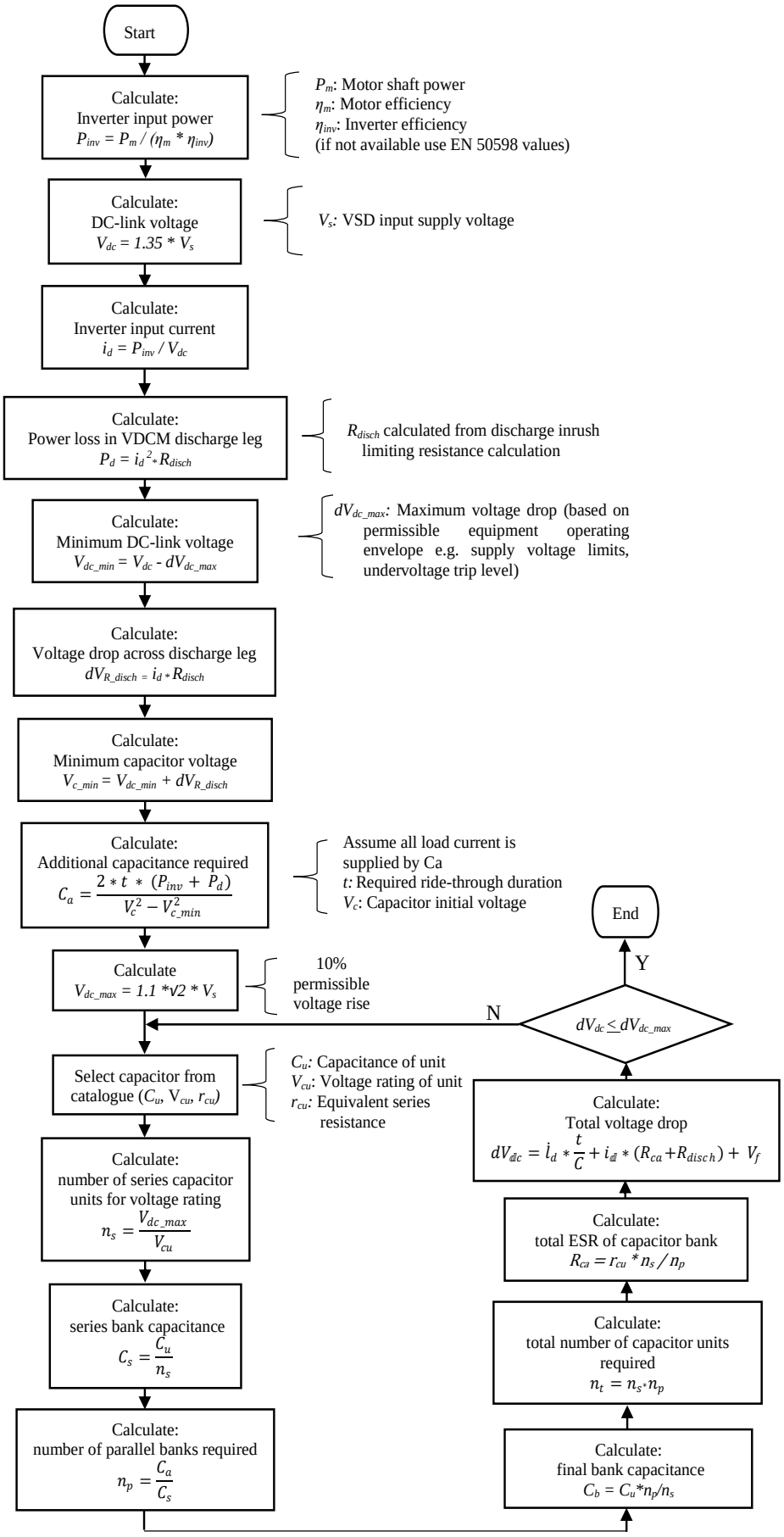


Figure 4-8. Capacitor Sizing Methodology

4.7.5. IGBT Sizing

The use of IGBTs for switching in this module is such that the operating points of the IGBTs fall within their safe operating area (SOA). The SOA of an IGBT is defined as the collector-emitter voltage and collector current conditions over which an IGBT can be expected to operate without self-damage or degradation and often shows multiple curves for different pulse widths. Figure 4-9 shows a typical forward biased safe operating area (FBSOA) for an IGBT.

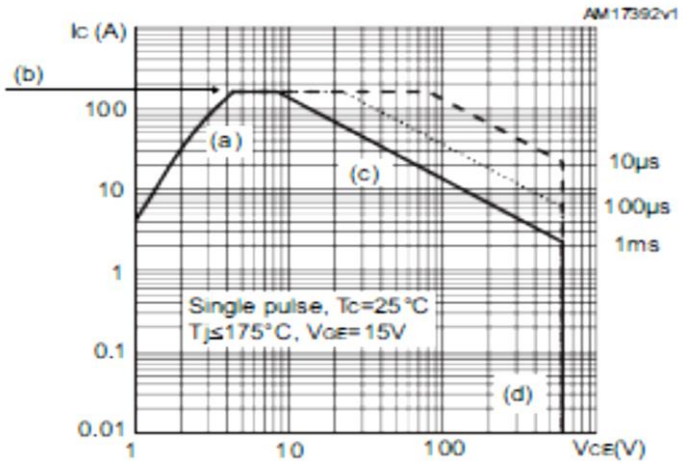


Figure 4-9. Forward Biased Safe Operating Area [41]

Area (a) is limited by conduction loss $V_{CE(sat)}$ at maximum junction temperature. Area (b), the top limit is related to the maximum pulsed collector current. Area (c) depends on the pulse length of the applied power pulse, the thermal impedance changes and leads to different maximum power losses. Area (d) is limited by the maximum breakdown voltage $V_{(BR)CES}$. Reverse-bias safe operating area (RBSOA) shows collector current and collector-emitter voltage conditions over which an IGBT can be turned off without self-damage. RBSOA is bound by maximum pulsed collector current rating, intrinsic characteristics of IGBT and maximum collector-emitter voltage rating.

4.8. Summary

A module for improving the ride-through capability of a VSI VSD was developed. The module interfaces directly with the VSD dc-link. It is configured to be active during a STPI and utilises a capacitor as an energy storage device. Ride-through is achieved through power injection into the dc-link during a STPI. Bi-directional power flow occurs between VSD dc-link and capacitor during compensation and capacitor charging. Circuit analysis of module utilising fixed resistors inrush current limiting during compensation and charging was carried out. Guidelines for use in the selection and sizing of key components of the module are presented.

Chapter 5

Simulation and Experimental Results of Compensating Module

5.1. Introduction

This chapter is concerned with the validation of the proposed dc bus voltage compensating module. Simulations and experimental work were carried out to assess the behaviour of the module. Impact of module operation on VSD and motor performance is also assessed to ensure that parameters are kept within permissible values. Finally, module losses are established and efficiency estimated.

5.2. Simulation of the Voltage Dip Compensating Module

A Matlab Simulink model of the proposed compensating module was developed. This is shown in Figure 5-1.

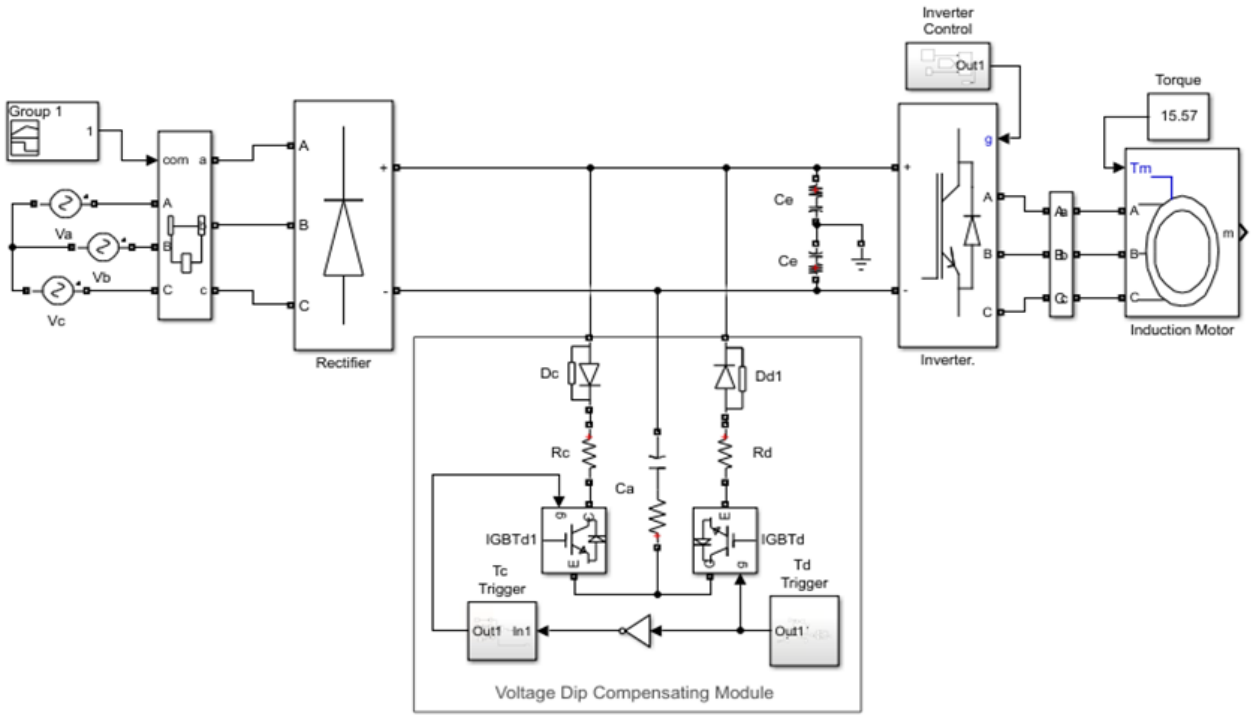


Figure 5-1. Simulink Model for VSD, Induction Motor and Voltage Dip Compensating Module

The model is made up of a voltage source inverter variable speed drive (comprising a full bridge diode rectifier, dc-link equipped with a capacitor C_e and a v/f controlled PWM inverter drive) connected to a 1.5kW induction motor. The proposed voltage dip compensating module is interfaced to the VSD through the dc-link. V/f control was selected because most control process applications in which VSDs are used do not need very fast and precise speed control [23]. Technical details for the VSD and induction motor used in the model are listed in Table 5-1 and Table 5-2.

Table 5-1. 1.5kW VSD Rating Information

	Input	Output
Voltage	380-500 V, 3ϕ	380-500 V, 3ϕ
Frequency	50 Hz	0.5-500 Hz
Current	6.4_{max} A	4.1 A
Maximum inrush current	10 A	
DC-link undervoltage trip	300 V	

Table 5-2. Induction Motor Parameters

Power	1.5 kW
Voltage	400 V
Current	3.84 A
Speed	920 rpm
Efficiency at full load	75.2%
Power factor	0.75
Stator resistance*	4.38 Ω
Stator leakage inductance*	17.1 mH
Rotor resistance*	4.11 Ω
Rotor leakage inductance*	16.5 mH
Magnetising inductance*	476 mH
Rotor inertia*	0.036 kgm^2

*typical value for a 1.5kW,400V, 50Hz motor

VSD simulation parameters are listed in Table 5-3.

Table 5-3. VSD Simulation Parameters

Rectifier	3-arm Diode Bridge
Inverter	3-arm IGBT PWM
Inverter Control	V/f
Switching Frequency	4 kHz
Sample Time	10 µs

5.2.1. Response of VSD to STPI - Without DC-link Voltage Compensation

When the motor is running at rated speed and load torque, a 0.2 s STPI is applied to the model without dc-link voltage compensation. This is achieved by opening the incoming ac supply breaker for a duration of 0.2 s. Figure 5-2 shows the simulation results obtained. As soon as the VSD is subjected to the 0.2 s STPI, the dc-link voltage starts decaying at a constant rate from an initial value of 556 V as the VSD dc-link capacitor supplies all the power to the motor. The drop in dc-link voltage is accompanied by a drop in torque and speed. The dc-link voltage continues to drop until 300 V, the under-voltage trip setting, at which stage the VSD trips. This is indicated by the flattening of dc-link voltage curve. VSD trips after 0.024 s (approx. one electrical cycle).

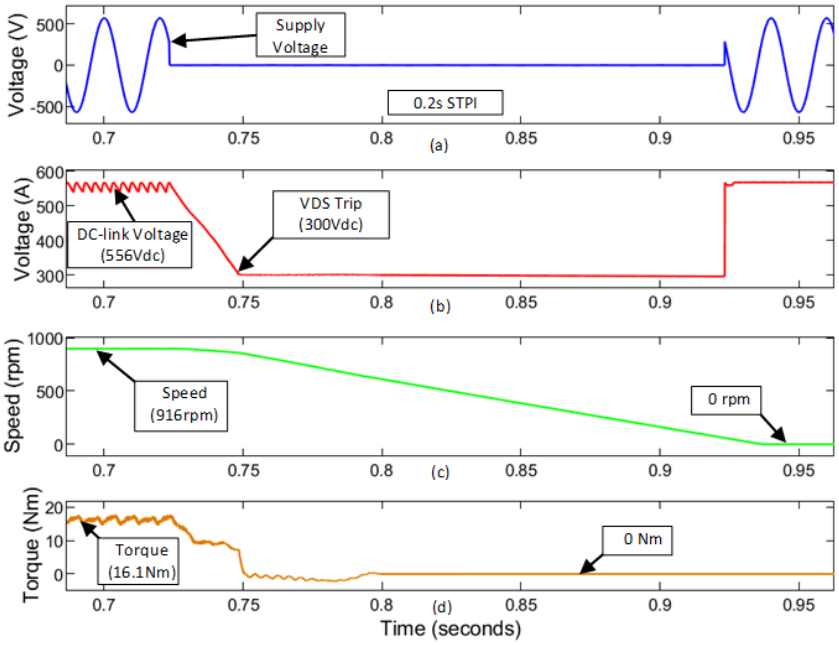


Figure 5-2.Simulation Results for a 0.2s STPI Without DC-link Voltage Compensation, (a) Supply voltage, (b) DC-link voltage, (c) Speed and (d) Torque

A significant drop in torque (52%) and a gradual reduction in speed (8%) are observed for the duration between STPI initiation to VSD trip. When the STPI clears after 0.2 s, an inrush current on the ac supply is observed as shown in Figure 5-3. This is due to the charging of the VSD capacitor after the STPI.

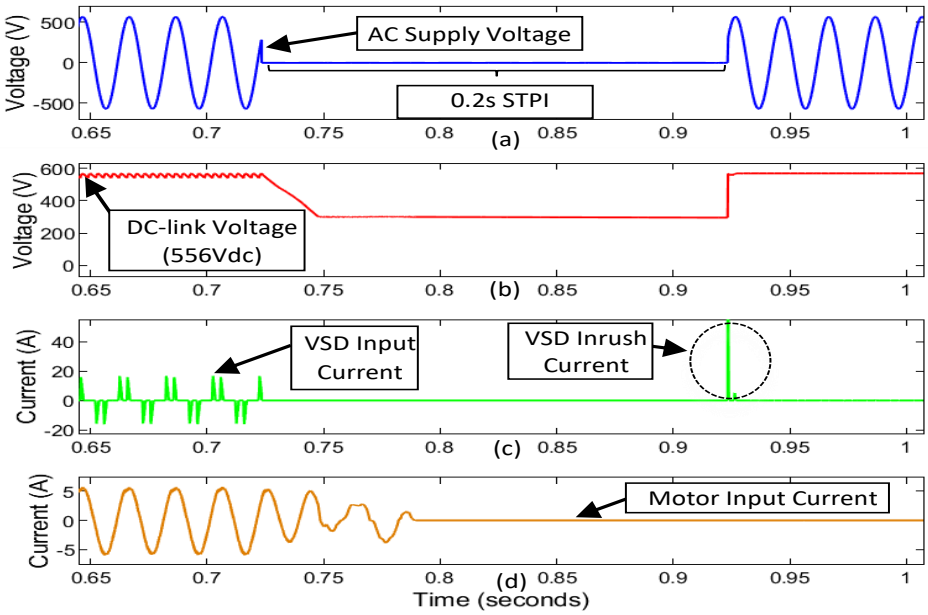


Figure 5-3. Simulation Results Without DC-link Voltage Compensation (a) Supply Voltage, (b) DC-link Voltage, (c) VSD Input Current and (d) Motor Input Current.

5.2.2. Response of VSD to STPI - With DC-link Voltage Compensation and Inrush Limiting

This time the simulation was run with the compensating module on standby and a 16 mF additional capacitor pre-charged to a voltage of 544 V. Sizing of this capacitor was done using the proposed sizing

methodology for a dc-link voltage drop of 15%. Using the proposed sizing methodology for inrush current limiting resistors, R_d and R_c required to limit inrush current to 4.2 A and 8.4 A during compensation and charging respectively were calculated as 6.91 Ω and 8.2 Ω respectively. Figure 5-4 shows simulation results for the same 0.2 s STPI test. A 8% drop in the dc-link voltage accompanied with a 16% drop in torque is experienced before the module is activated. A small drop in speed is observed. Change in speed is slow due to inertia of the rotating assembly.

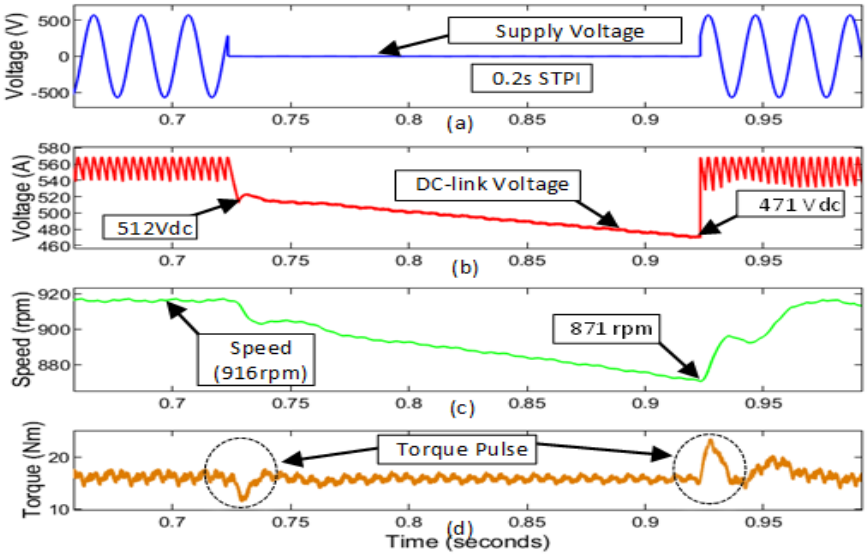


Figure 5-4. Simulation Results with DC-link Voltage Compensation, (a) Supply Voltage, (b) DC-link Voltage, (c) Speed and (d) Torque

Once the dc-link voltage has dropped to the trigger voltage of 512 V, the dc-link voltage compensating device is activated resulting in the connection of the pre-charged capacitor to the dc-link. This is shown by the sudden halt and a subsequent increase in the dc-link voltage from 512 V to 524 V. The connection of the additional capacitor to the dc-link is accompanied by an inrush current as C_e charges up. This is shown in Figure 5-5 The observed inrush current is limited by resistor R_d. The dc-link voltage continues to drop at a lower rate which is determined by the additional capacitor. A torque pulse of 18% is experienced at start of compensation. This is caused by a drop in dc-link voltage due to loss of supply and sudden recovery of the dc-link voltage at start of compensation. Motor current is not affected at start of compensation. There is a steady increase in current drawn as the STPI progresses as a result of the drop in inverter output voltage. To maintain the same torque at reduced voltage, the induction motor draws more current. At the end of compensation, a torque pulsation of 23% is observed and a momentary increase in motor current observed as supply is restored. The observed torque pulse is due to the sudden increase in the dc-link voltage.

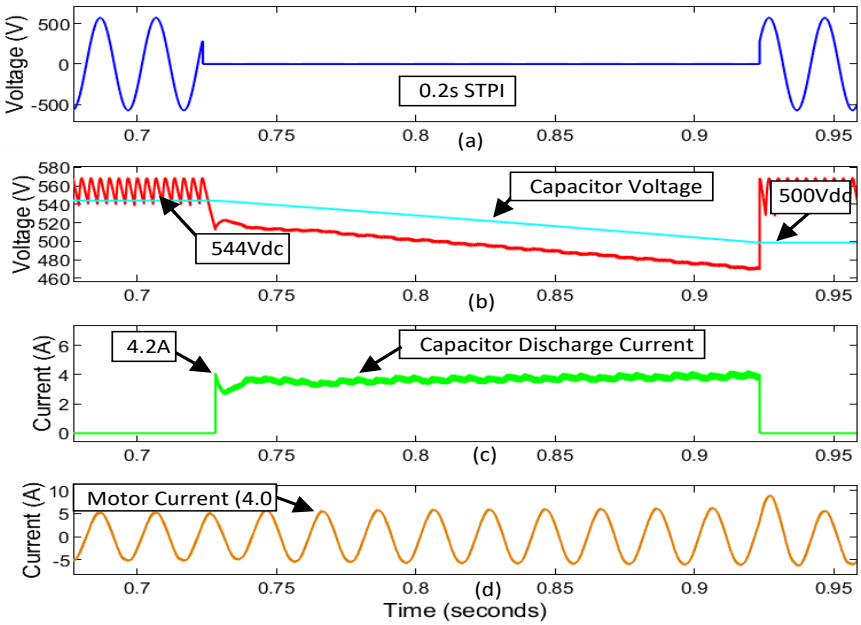


Figure 5-5. Simulation Results with DC-link Voltage Compensation, (a) Supply Voltage, (b) DC-link and Capacitor voltage,

Table 5-4 shows the summary of the simulation results. A drop in dc-link voltage leads to a drop in torque developed by the motor. This results in a reduction in speed. Voltage drops between capacitor and dc-link are different due to voltage drop across the inrush current limiting resistor R_d and discharge components parasitics.

Table 5-4. Summary of Changes in Key Parameters During STPI

Parameter	Value at STPI Inception	Value at STPI Clearance	% Change[1]
DC-link Voltage	556 V	470 V	-15.5%
Capacitor Voltage	544 V	500 V	-8.1%
Electrical Torque	16.0 Nm	15.2 Nm	-5.5%
Speed	917 rpm	876 rpm	-4.4%

[1] negative sign indicates a reduction in the measured parameter

5.2.3. Response of VSD to STPI – With Compensation and Without Inrush Current Limiting

To verify the need for inrush current limiting at start of compensation and charging, a calculation and simulation study was carried out. Typical values for the components used in the compensating module are listed in Table 5-5.

Table 5-5. Component Values Used for Analysis

Parameter	Value
Diode forward voltage V_f	0.8 V
Capacitor C_a equivalent series resistance R_{Ca}	0.018 Ω
Capacitor C_e equivalent series resistance R_{Ce}	0.474 Ω
IGBT T_d / T_c on-resistance R_{Td} / R_{Tc}	0.008 Ω
Diode D_d /D_c on-resistance R_{Dd}/ R_{Dc}	0.004 Ω

Assume capacitor voltage V_c and dc-link voltage V_{dc} at start of compensation and charging are as per values listed in Table 5-6.

Table 5-6. DC-link and Capacitor Voltage Variations During STPI

Parameter	**Value at start of**	
	Compensation	**Charging of Ca**
V_{Ca}	544 V	500 V
V_{dc}	510 V	566 V[1]

[1] DC-link voltage selected at start of charging is the maximum possible dc-link voltage

Using (16) and (23) and the values listed in Table 5-5 and Table 5-6, inrush currents were calculated the results are shown in Table 5-7.

Table 5-7. Inrush Currents Calculation and Simulation Results

Parameter	**Calculated Value**
Peak discharge current (i_d)	62 A
Peak charging current (i_c)	2140 A

The charging inrush current is considerably higher than the discharge current due to:

- a low charging total series resistance (0.03 Ω) when compared to the discharge total resistance (0.504 Ω) and
- a higher dc-link - capacitor voltage difference (66 V) at start of charging when compared to the voltage difference at start of discharge (34 V).

Simulation results obtained for the module without inrush current limiting are shown in Figure 5-6.

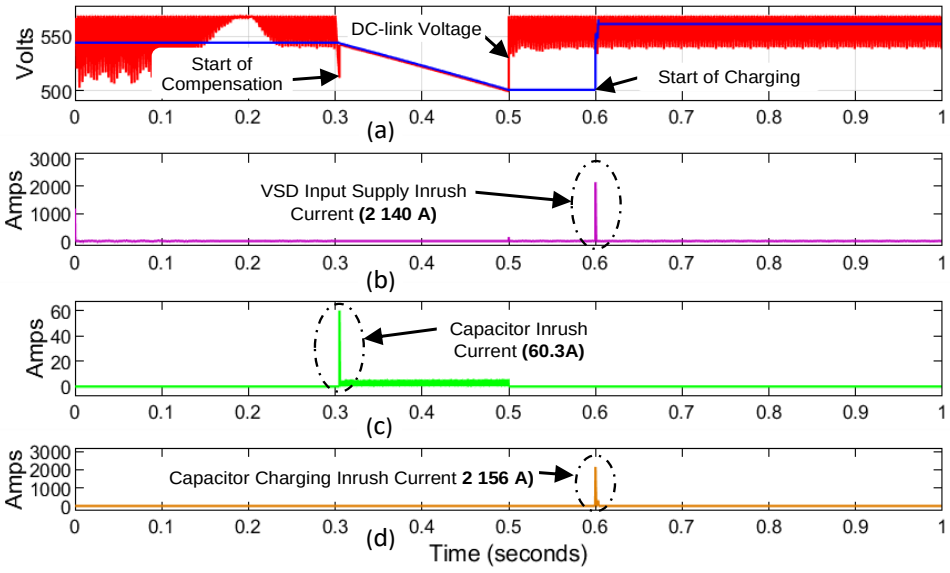


Figure 5-6. Inrush Current Without Any Limiting Technique, (a) DC-link and Capacitor Voltages, (b) VSD Input Supply Current, (c) Capacitor Discharge Current (d) Capacitor Charging Current

It is clear from calculation and simulation results that such magnitude of inrush if not limited will damage VSD components. Thus, parasitic elements alone cannot limit inrush current to equipment safe levels. Additional inrush limiting thus necessary. Simulation results obtained with fixed resistor inrush current limiting are presented in Table 5-8.

Table 5-8. Comparison of Calculated and Simulated Inrush Currents

Parameter	Value	
	Start of Compensation	Charging of Ca
VSD maximum current rating	4.2 A	8.4 A
Simulated Inrush Current	4.2 A	8.2 A

By incorporating fixed resistors R_d and R_c, inrush current was limited to be within VSD rating.

5.3. DC-link Charging

Once STPI has cleared and the dc-link voltage stabilized, charging of C_a from the dc-link commences. Figure 5-7 shows the simulation results. To avoid continuous and excessive loading of the dc-link due to charging action, pulse charging was adopted. This can be seen from the pulsed charging current trend. This approach results in minimum impact on the torque and speed of the motor.

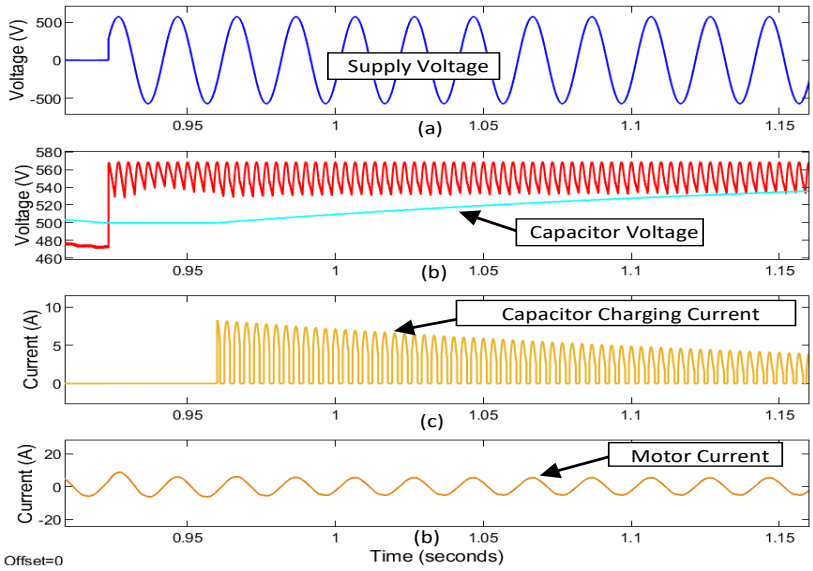


Figure 5-7.Simulation Results for DC-link Charging of Capacitor Ca,
(a) Supply Voltage, (b) DC-link and Capacitor Voltage, (c) Capacitor Charging Current and (d) Motor Input Current

Once charging commences, the dc-link voltage ripple magnitude increases. This is due to extra loading on the dc-link because of charging. There is a gradual reduction in the magnitude of current as capacitor voltage increases. No noticeable impact on motor current.

5.4. Module Losses and Efficiency

Efficient utilisation of energy is key in any design. This utilisation is reflected by the efficiency measure of the design. The presence of semiconductor devices (IGBTs, diodes) and resistors in the module cause energy losses which result in a reduction in module efficiency. Semi-conductor losses are largely due to switching and conduction losses. Leakage losses when compared to conduction and switching losses are small and can be ignored in loss calculations. Resistor losses are due to i^2r losses. To cater for such losses,

the capacitor might require oversizing. In addition, a cooling system might be necessary to keep device temperatures within limits. Such losses need to be identified, quantified and controlled. The efficiency metric serves as a base measure for improving the designTo quantify the impact of losses on the efficiency of the compensating module, a model for the module was developed in PLECS. Component losses considered in the model are summarized in Table 5-9. Switching and conduction losses for the respective semiconductor devices were obtained from datasheets for the respective components.

Table 5-9. Module Component Losses Considered

Component	**Losses**	
	Conduction	**Switching**
IGBT	+	+
Diode	+	+ (reverse recovery)
Resistor	+	-

Figure 5-8 shows the proposed PLECS model. In the model, the current into the inverter which is pulsed due to switching action of inverter IGBTs is modelled as a controlled current source. The averaging time utilized for calculating losses is 0.0002 s.

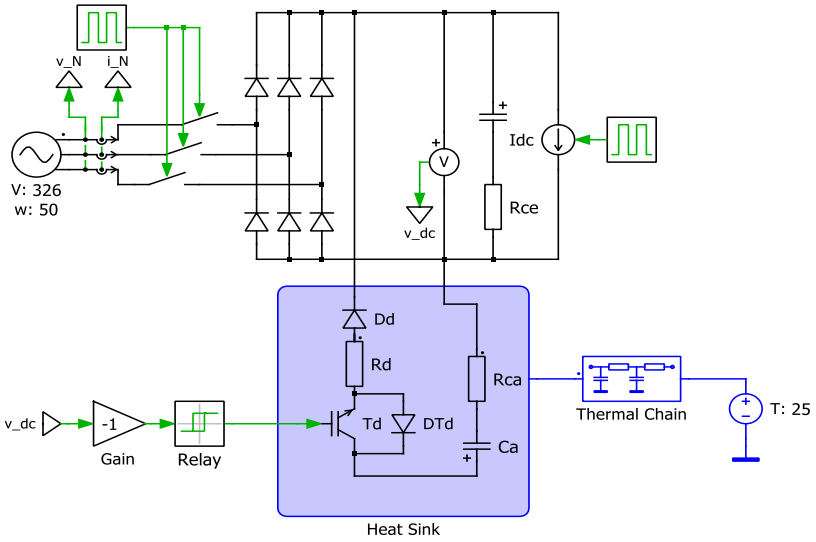


Figure 5-8. Fixed Resistor Loss Determining Model

Figure 5-9 shows simulation results obtained for the loss model. The overall efficiency of the module with fixed resistor inrush limiting technique is 94.8%. Resistor R_d conduction losses constitute 88% of total module losses. Thus, loss in module efficiency is largely caused by resistor R_d.

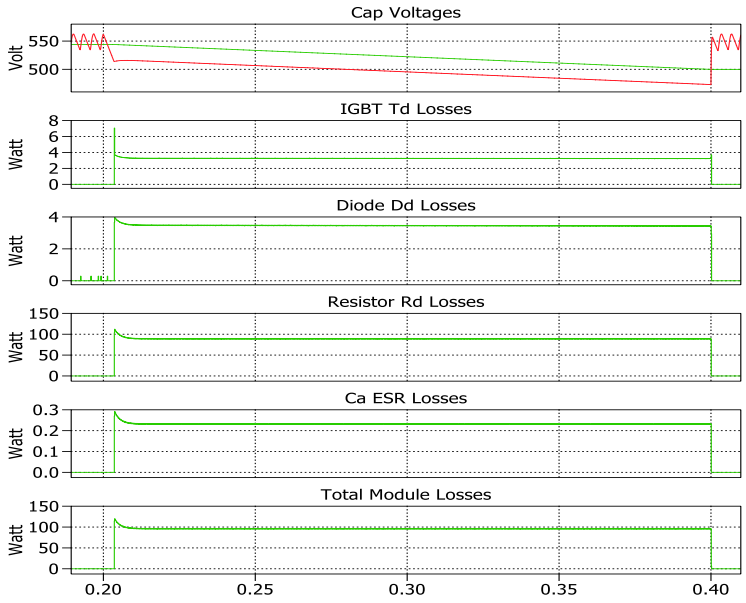


Figure 5-9. Module Losses with Fixed Resistor Inrush Current Limiting Technique

5.5. Experimental Set-up

To illustrate the operation of the proposed dc-link voltage compensating module and to validate sizing of capacitor and inrush current limiting resistor, an experimental set-up was devised. The block diagram for the experimental set-up is shown in Figure 5-10. The proposed compensating module (VDCM) is connected to a 2-quadrant VSD driving a 1.5 kW induction motor. A 2.2 kW induction generator coupled to the induction motor provides the required shaft torque. This is achieved using a 4-quadrant VSD operating in regenerative mode.

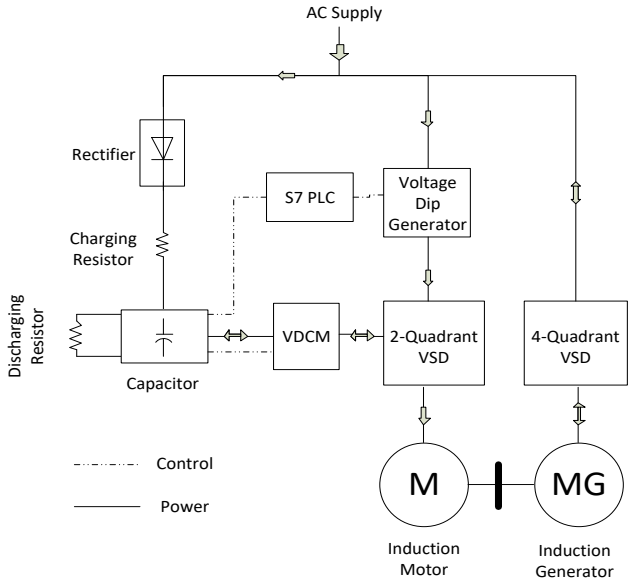


Figure 5-10. Block Diagram of Experimental Set-Up

Control of the motors, voltage dip generator, pre-charging and discharging of the additional capacitor is undertaken through an S7 PLC. Speed and torque are measured by a torque transducer mounted on the motor-generator coupling. Before the capacitor is put on standby for dc-link compensation, charging is

carried out through a separately powered bridge rectifier. Commands for the operation of motors, pre-charging and discharging of the capacitor bank and voltage dip generation are issued through the control panel. The laboratory set-up is shown in Figure 5-11.

Tests carried out involved assessing the behaviour of the VSD with and without dc-link voltage compensation when subjected to a 0.2 s STPI. Tests were carried out with the induction motor loaded to rated torque. To avoid damage to the VSD, key protection schemes including dc-link under-voltage protection were left enabled. Onboard dc-link voltage recovery slip compensation and torque compensation control schemes were disabled to ensure alignment with the Simulink model.

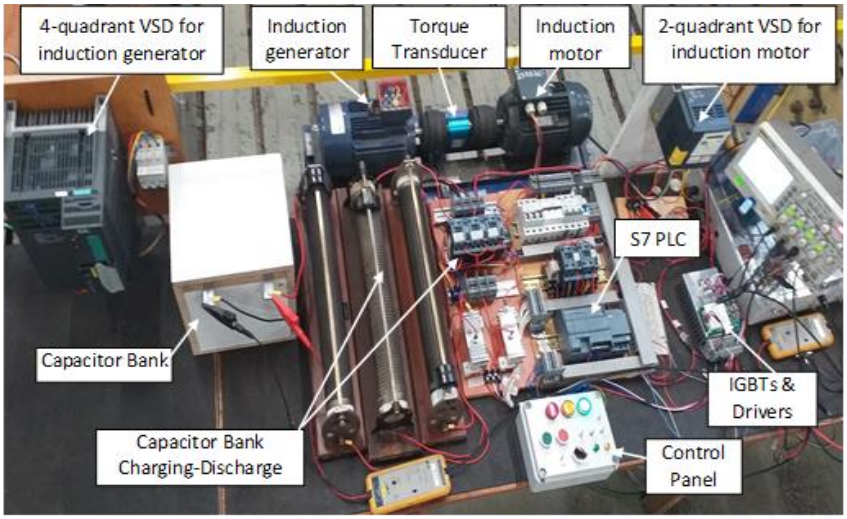


Figure 5-11. Laboratory Set-up for DC-link Voltage Compensating Module

5.5.1. Voltage Dip Generator

To emulate voltage dips and STPI, a circuit shown in Figure 5-12 was used. It comprises a variable AC transformer (variac), contactors S1 and S2 and S7 PLC. The required voltage dip magnitude is adjusted through the variac. The duration for the dip is set in S7 PLC. A voltage dip is generated by opening contactor S1 and then closing S2. Only balanced three-phase dips were investigated whose magnitude and duration could be easily controlled.

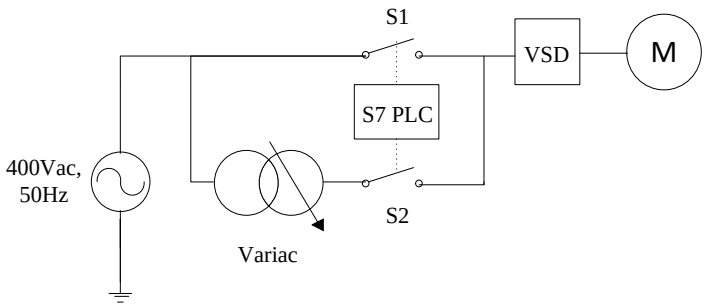


Figure 5-12. Voltage Dip Generator Experimental Set-Up

5.5.2. Experimental Results Without DC-link Voltage Compensation

Figure 5-13 shows the results obtained when the 2-quadrant VSD is subjected to a 0.2 s STPI. Once supply to the VSD is lost, the dc-link voltage immediately starts decaying as the VSD dc-link capacitor supplies all the required motor power. A drop in torque (and consequently speed) is observed as the dc-link voltage decays. The VSD trips once the dc-link voltage has decayed to below the undervoltage trip setting of 288 V. This is indicated by the flattening of the dc-link voltage curve. Once the VSD trips, a torque imbalance occurs between the induction motor and generator. The 1.5 kW motor starts operating as an induction generator with the 2.2kW now acting as an induction motor.

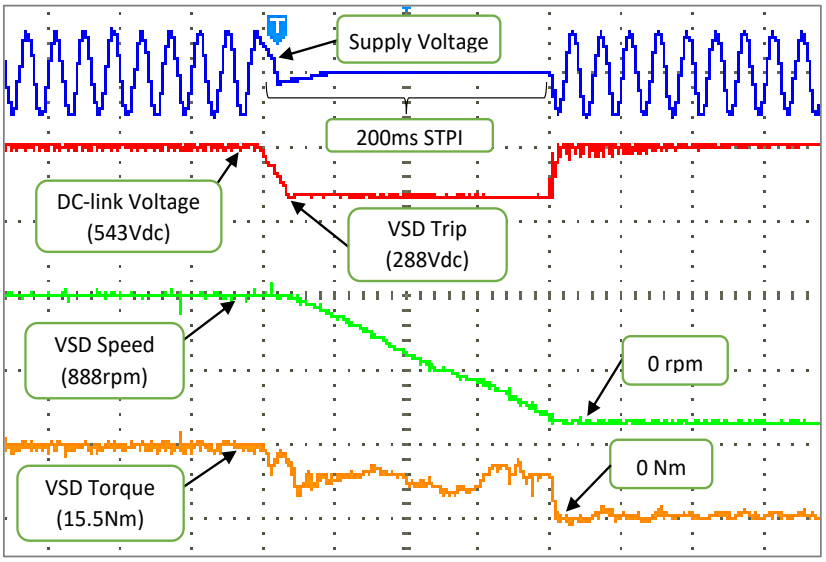


Figure 5-13. VSD - Motor Behaviour Without DC-link Voltage Compensation

Figure 5-14 shows changes in VSD input and motor input currents before, during and post STPI. Motor current flows through even after the VSD trips as it operates in generator mode. The speed keeps dropping until the rotating assembly is at standstill at which point supply to the 2.2 kW induction motor is cut.

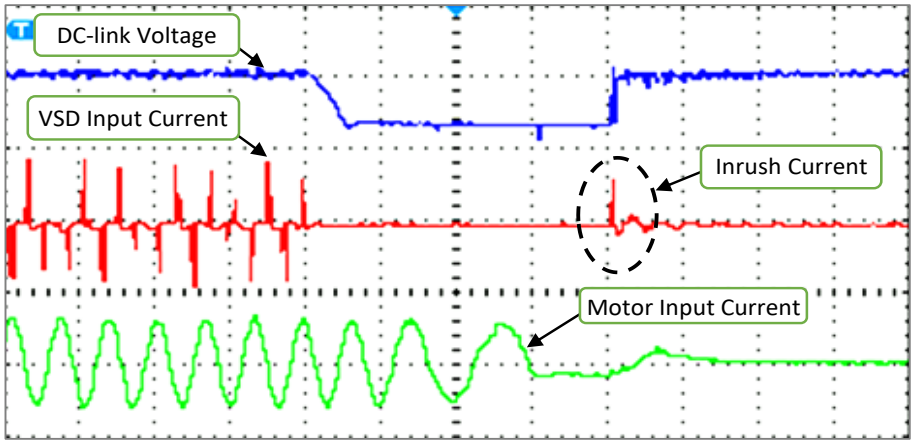


Figure 5-14.VSD - Motor Behaviour Without DC-link Voltage Compensation

Restoration of supply at the end of the dip is accompanied with rapid increase in dc-link voltage to its nominal level with some initial oscillations. The clearance of the dip is accompanied with a spike in the VSD supply current as the dc-link capacitor charges up to nominal dc-link voltage.

5.5.3. Experimental Results With DC-link Voltage Compensation

Before the test was carried out, the capacitor was pre-charged to a voltage of 544 V. As shown in Figure 5-15, dc-link voltage starts decaying from 556 V immediately when supply is lost.

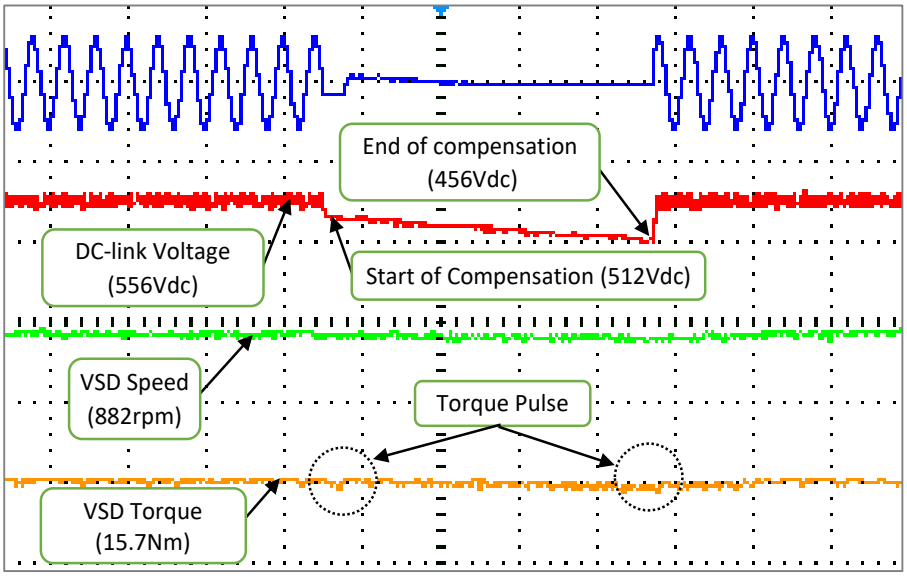


Figure 5-15. Experimental Results With DC-link Voltage Compensation

Once the voltage has decayed to 512 V, the trigger circuit is activated resulting in the capacitor bank being connected to the dc-link. In Figure 5-16, the sudden increase in the discharge current from the additional capacitor is evident as power is injected into the dc-link.

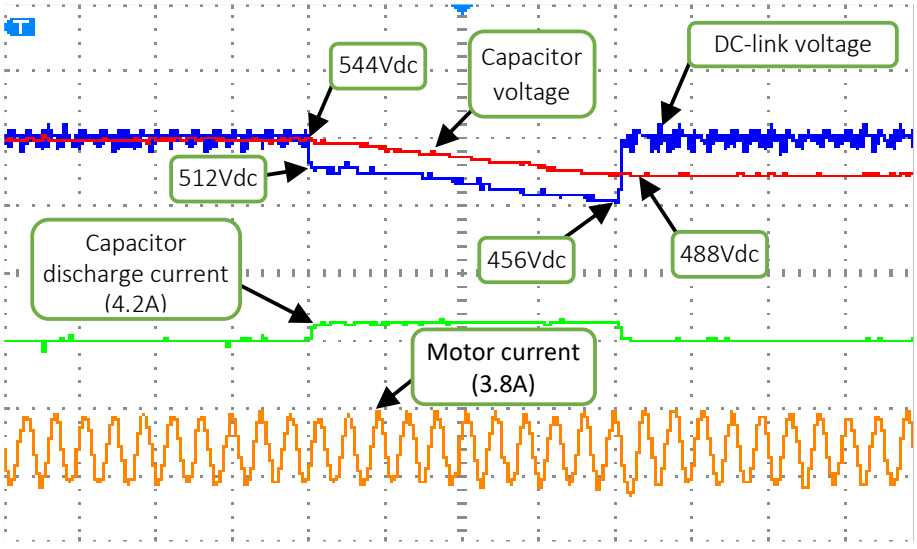


Figure 5-16. DC-link Voltage Variation During Voltage Compensation

A voltage difference of 32 V exists between dc-link voltage and capacitor voltage. This can be attributed to the voltage drop across C_a, R_d, T_d and D_d. Torque pulses of 12.8% and 14.3% are observed at the start of dc-link voltage compensation and restoration of supply. These pulsations are due to changes in the dc-link voltage.

5.6. Charging of Capacitor from DC-link

Figure 5-17 shows the results of charging from the dc-link of the VSD. Pulse charging of the capacitor is evident in the charging current. As the capacitor charges up towards dc-link voltage, the magnitude of the charging current reduces and once fully charged, the charging IGBT is switched off and current decays to zero.

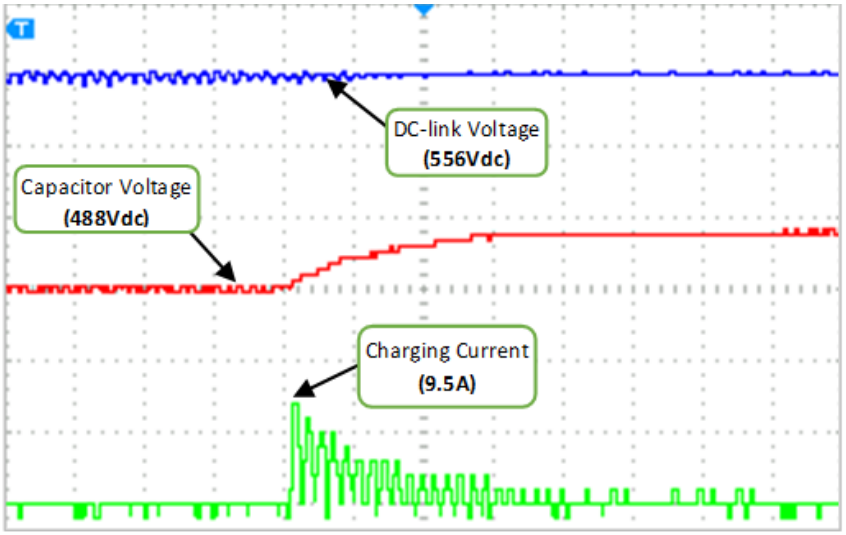


Figure 5-17. DC-link Charging of Capacitor Ca

5.7. Analysis of Results

Table 5-10 summarises the variations in the dc-link voltage and capacitor voltage during compensation obtained during the experiment.

Table 5-10. Variation of DC-link and Capacitor Voltages During Compensation

Parameter	Value at Start of STPI	Value at End of STPI	% Change[1]
DC-link voltage	556 V	456 V	-18.0 %
Capacitor Voltage	544 V	488 V	-10.3 %

[1] negative sign indicates a reduction in the measured parameter

It can be seen from Table 5-10 that the voltage drop across the capacitor is less than that of the dc-link. This is as a result of the voltage drop across the inrush current limiting resistor during compensation. The impact of the compensating module on motor torque and speed is shown in Table 5-11.

Table 5-11. Impact of Module Operation on Motor Speed and Torque

Parameter	Value at Start of STPI	Value at End of STPI	% Change[2]
Speed	882 rpm	860 rpm	-2.5 %
Torque	15.7 Nm	14.0 Nm	- 10.3 %

[2] negative sign indicates a reduction in the measured parameter

The drop in dc-link voltage leads to a drop in torque generated and consequently a drop in speed. Torque pulsations of 12.8% and 14.3% obtained at start and end of compensation respectively are due to transients in dc-link voltage.

A comparison of changes in key parameters as per calculation (using proposed sizing methodology), simulation and experimental results are summarised in Table 5-12.

Table 5-12. Comparison of Calculated, Simulation and Experiment Results on Key Parameters

Parameter	Change in Value[3]		
	As per sizing methodology	As per Simulation	As per Experiment
DC-link voltage drop (%)	15.0%	15.6%	18.0%
Cap voltage drop (%)	7.7%	8.3%	10.3%

[3] refers to change in value at the end of compensation compared to at start of compensation

A maximum variance of 3% in dc-link voltage drop is obtained between calculated and experimental results. A 2.6% variance in capacitor voltage drop is observed between calculated and experimental results. Simulation results fall within the above variances. The close similarity between results obtained by calculation, simulation and experiment confirm adequacy and validity of the proposed capacitor sizing methodology for the module equipped with fixed resistors for inrush current limiting. These results also validate the simulation model utilised.

Discharge current during compensation and charging current are summarised in Table 5-13.

Table 5-13. Capacitor Discharge and Charging Currents

Parameter	Value		
	As per sizing methodology	Simulation Result	Experiment Result
Discharge current (A)	4.2 A	4.2 A	4.1 A
Charging current (A)	8.4 A	8.3 A	9.5 A

There is a also strong correlation between calculated values (as per sizing methodology), simulation and experimental results for the proposed voltage dip compensation. These results validate the proposed inrush current limiting resistor sizing methodology.

To further test the proposed capacitor sizing methodology for a different sized VSD, a calculation and simulation study was undertaken for a 7.5 kW motor. Data used for the 7.5 kW induction motor used for the assessment is listed in Table 5-14.

Table 5-14. 7.5kW Induction Motor Technical Details

Parameter	**Value**
Power	7.5 kW
Efficiency	89.3%
Power Factor	0.81
Pole Pairs	2
Rotor Speed	1450 rpm

The results of the study for variation in key parameters are summarised in Table 5-15.

Table 5-15.DC-link and Capacitor Voltage Variation for a 7.5kW Compensating Module

Parameter	**Value**		
	As per sizing methodology	**As per Simulation**	**% Variance (calculated vs simulated**
DC-link voltage drop	83.4 V	82.8 V	0.7%
Cap voltage drop	54.0 V	51.2 V	5.3%

Calculated and simulated results for dc-link voltage compensation for a 7.5 kW induction during a STPI are very comparable. Thus, the proposed sizing methodology can be used for different sized motors.

5.8. Summary

The proposed dc-link voltage compensating module incorporating an additional switched capacitor was successfully developed, simulated and tested. An overall dc-link voltage drop of 18% was obtained from the experiment. This is against a target value of 15% as per capacitor sizing methodology. As a result of this drop in dc-link voltage, a drop in torque of 10.6% and a drop in speed of 2.5% were measured. During the experiment, torque pulsations of 12.8% and 14.3% were observed during start and end of compensation respectively. The need for inrush current limiting was confirmed by both calculation and simulation. Significant inrush currents at start of compensation and charging were observed. These were minimised successfully by using fixed resistors. A method for sizing the additional capacitor and inrush current limiting resistors based on readily available equipment information was tested and validated. The use of series fixed resistors in limiting inrush currents was simple and easy to implement. However, two major short comings were identified i.e. unwanted voltage drop across resistor and significant energy losses leading to a reduction in module efficiency. It became necessary to investigate other inrush current limiting techniques for the module.

Chapter 6

Inrush Current Limiting Techniques

6.1. Introduction

The use of fixed resistors in limiting inrush current resulted in unwanted voltage drops across the limiting resistor and energy losses leading to a reduction in module efficiency. To address these short comings, three additional inrush current limiting techniques utilising a variable resistor, inductor and equipotential voltage switching (EVS) are proposed, assessed and compared. Their impact on VSD-motor performance is also explored. Loss and efficiency assessments of each technique are conducted and compared.

6.2. Variable Resistor Inrush Current Limiting Technique

The set-up is a modified version of the fixed resistor technique with an additional switch, T_{d1} connected across resistor R_d. Figure 6-1 is a schematic representation of the technique showing the discharge leg of the module connected to the VSD. At the start of compensation (when the additional capacitor is connected to the dc-link), an inrush charging current flows through the discharge leg as the VSD capacitor C_e charges up towards the additional capacitor C_a voltage. This inrush current is limited by resistor R_d. Bypassing of R_d commences once this initial inrush current has subsided and is undertaken through PWM switching of the switch, T_{d1}. The beginning of PWM switching of T_{d1} also results in an inrush current as C_e is further charged towards C_a voltage. At this stage the inrush current depends on the voltage appearing across R_d. A smaller R_d will result in a lower voltage difference between C_e and C_a and a lower inrush current. This translates to a reduced strain on the IGBT during switching.

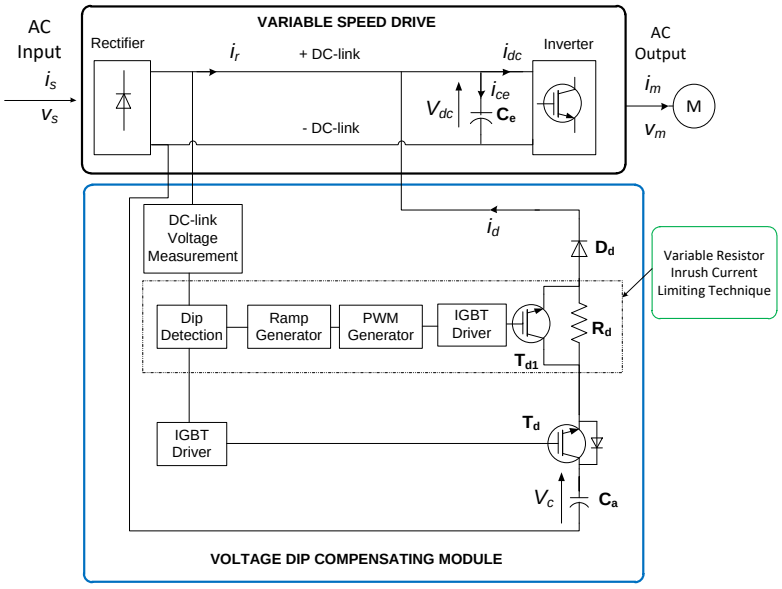


Figure 6-1. Variable Resistor Current Limiting Technique

The maximum permissible output current of a VSD is limited by the continuous current rating of the inverter IGBTs whose pulse current rating is significantly higher than its continuous current rating. In most cases, their maximum pulsed current rating is 2 to 3 times the continuous current rating [42] [43]. The maximum output pulsed current rating of the VSD is obtained by multiplying its maximum output continuous current rating with a factor of 2 or 3.

6.2.1. Simulation Results

Capacitor and dc-link voltage at start of compensation are set at 540 V and 530 V respectively. Using the proposed inrush current resistor sizing method, a value of 1.6 Ω for R_d was calculated. Simulation results obtained are shown in Figure 6-2 and Figure 6-3. At the start of compensation, resistor R_d limits the inrush current to 4.3 A. Once PWM switching of the T_{d1} is initiated, pulses in discharge current are observed. These correspond to instances when R_d is bypassed by IGBT T_{d1}. As the duty cycle of bypass switch increases, the current pulses progressively become small and so does the voltage drop between the dc-link and capacitor.

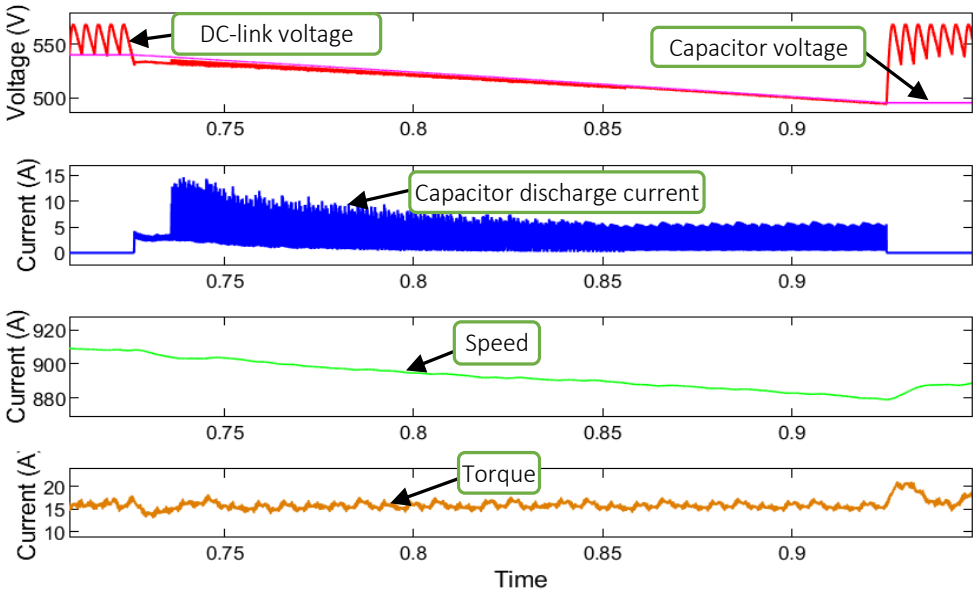


Figure 6-2. Simulation Results of Variable Resistor Inrush Current Limiting Technique, (a) Capacitor and DC-link Voltage, (b) Capacitor Current, (c) Speed and (d) Torque

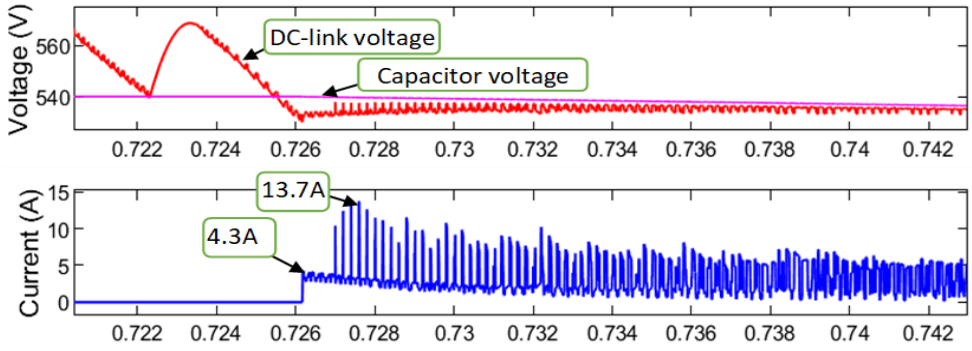


Figure 6-3. Simulation Results of Variable Resistor Inrush Current Limiting Technique, (a) Capacitor and DC-link Voltage and (b) Capacitor Current

Inrush currents obtained by this technique are contained in Table 6-1.

Table 6-1. Simulation Result of Variable Resistor Inrush Current Limiting Technique

Parameter	Value
Initial inrush current	4.3 A
Peak inrush current (during PWM switching)	13.7 A
Current (mean during PWM switching)	4.1 A

Whilst the peak values at the start of PWM switching are high, their duration dictated by PWM duty are low resulting in an overall low mean current value. Impact of module operation on VSD and motor parameters are shown in Table 6-2.

Table 6-2. Impact of Variable Resistor Inrush Current Limiting Technique on VSD and Motor Performance

Parameter	Value
Drop in dc-link voltage	10.4%
Drop in capacitor voltage	8.1%
Drop in torque	4.0%
Drop in speed	3.0%

With this technique, difference between voltage drop on the dc-link and capacitor has been reduced. This is a result of bypassing of resistor R_d.

6.2.2. Experimental Results

Figure 6-4 shows experimental results for the gate control signal used to generate PWM switching of the bypass IGBT T_{d1} at a base frequency of 5kHz. Once the module activation signal is received, a 10 ms delay is introduced to allow the initial inrush current to subside. Thereafter the PWM duty cycle is increased from zero to 100% through a ramp function. Ramping of the duty from 0% to 100% is done over a period of 0.15 s.

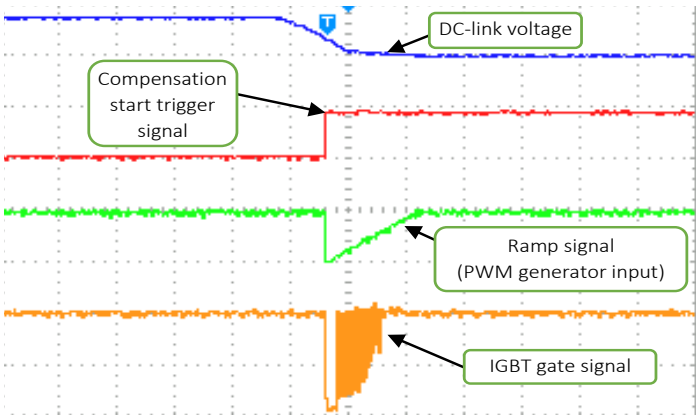


Figure 6-4. Variable Resistor Control Circuit Signals

Experimental results obtained with the module utilizing variable resistor inrush current limiting technique are shown in Figure 6-5. At module activation, resistor R_d limits inrush current to 5.2 A. A voltage difference between the capacitor and the dc-link due to the voltage drop across R_d is evident. As PWM

switching of the IGBT, T_{d1} is carried out on a linearly increasing duty cycle, the dc-link voltage starts recovering towards the capacitor voltage.

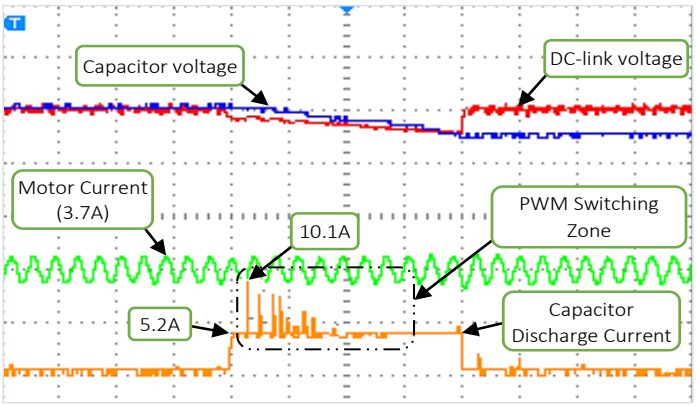


Figure 6-5. Experimental Results of Variable Resistor Inrush Current Limiting Technique

The resulting current pulses due to PWM switching are visible. Current measured is shown in Table 6-3.

Table 6-3. Inrush Currents with Variable Resistor Technique

Parameter	**Value**
Initial Inrush Current	5.2 A
Peak Current (during PWM switching)	10.1 A

At the time the duty is 100%, the dc-link voltage is almost the same as the capacitor voltage at which stage R_d has been fully bypassed. Figure 6-6 shows the impact of variable resistor inrush current limiting technique on VSD and motor performance.

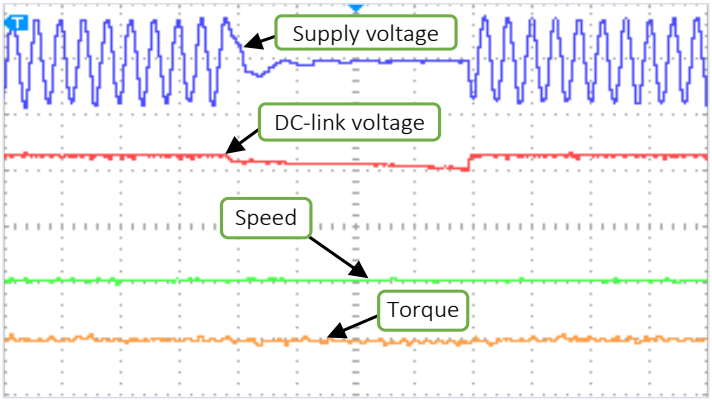


Figure 6-6. Impact of Variable Resistor Inrush Current Limiting Technique on VSD and Motor Performance

Torque pulses of 11.6% and 9.1% are observed at the start of compensation and restoration of supply respectively. Changes in key VSD and motor parameters during compensation are summarized in Table 6-4.

Table 6-4. Impact of Variable Resistor Technique on VSD and Motor Performance

Parameter	Value
Drop in dc-link voltage	12.2%
Drop in capacitor voltage	10.3%
Drop in torque	9.8%
Drop in speed	1.7%

As expected, there is an overall reduction in dc-link voltage drop due to bypassing of resistor R_d.

6.2.3. Module Losses and Efficiency

Figure 6-7 shows the PLECS simulation model used to determine the losses and efficiency of the compensating module incorporating variable resistor inrush current limiting technique.

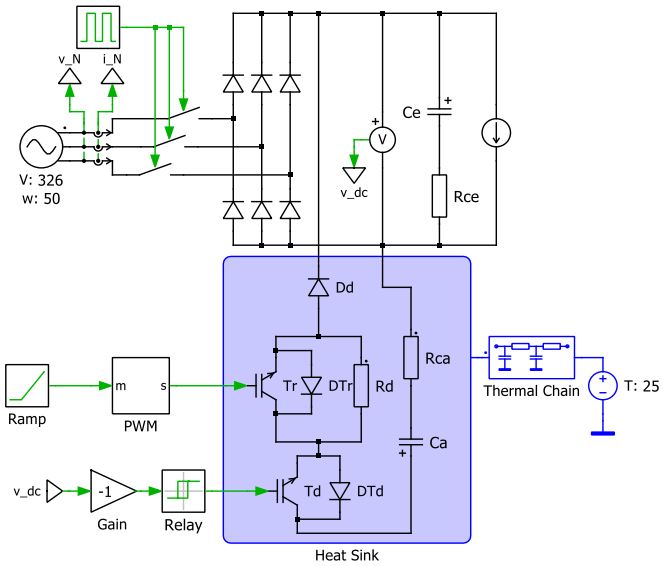


Figure 6-7. Variable Resistor Losses and Efficiency Model

Losses incurred by the module incorporating a variable resistor inrush current limiting technique are shown in Figure 6-8. The bulk of the losses are incurred during the PWM switching period arising from bypass IGBT T_r switching losses and resistor R_d conduction losses. PWM switching at a lower voltage difference between the dc-link and capacitor results in lower switching losses. Bypassing R_d results in a significant reduction of total module losses. This results in an increase in efficiency of the module to 99.3%.

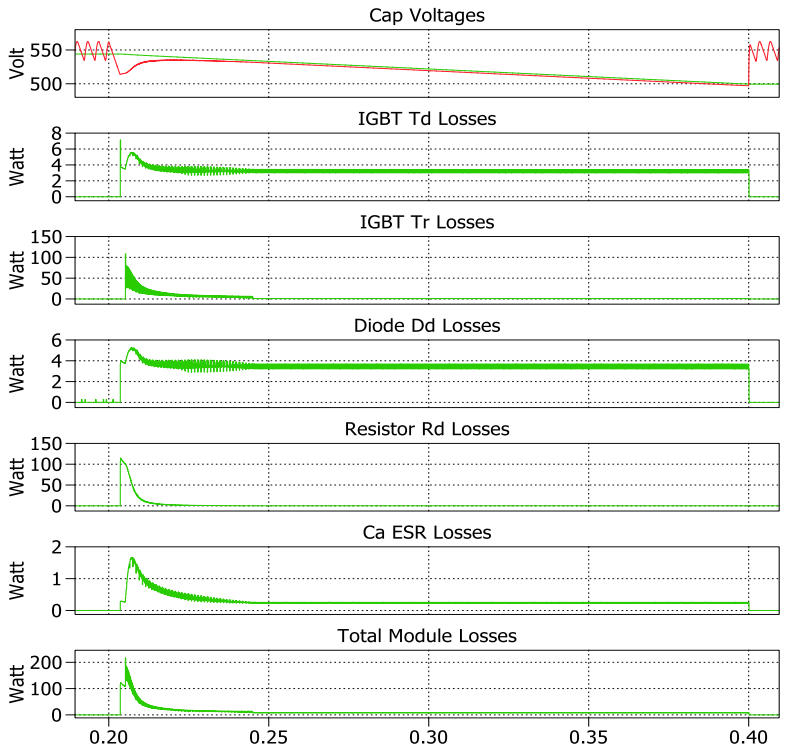


Figure 6-8. Module Losses with Variable Resistor Inrush Current Limiting Technique

6.2.4. Advantages and Disadvantages of Variable Resistor Inrush Current Limiting Technique

Compared to the fixed resistor inrush current limiting technique, the variable resistor technique results in reduced ohmic losses which results in an increase in module efficiency. It also results in a smaller dc-link voltage drop. The technique however is not easy to implement, requires additional components and thus expensive. Another inrush current associated with PWM switching is experienced even though at lower values. Care needs to be exercised when selecting capacitor voltage, module trigger voltage and inrush limiting resistor value to avoid damage to equipment due to this second inrush.

6.3. Inductor Inrush Current Limiting Technique

Inrush current limiting is achieved by adding a series inductor in the discharge leg of the compensating module. Refer to Figure 6-9. A free-wheeling diode is connected across the inductor. The freewheeling diode acts as a damper to the circuit by providing a path for current to flow when the dc-link capacitor C_e is fully charged. It also protects equipment components against dangerous voltage build-up when module is switched off.

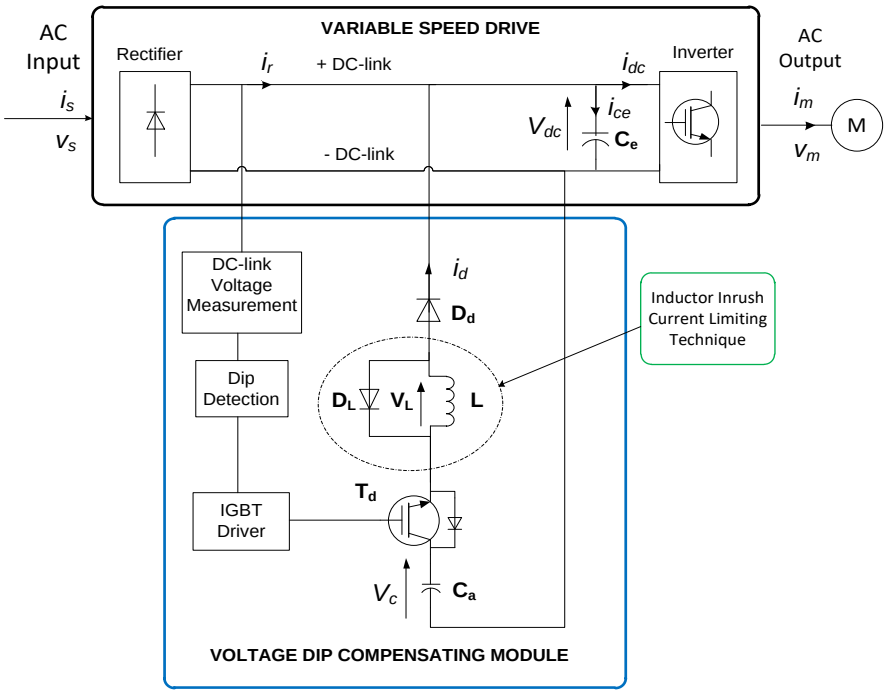


Figure 6-9. Inductor Inrush Current Limiting Technique

At the instant of IGBT T_d switching on, the voltage appearing across the inductor V_L is given by

$$V_L = V_C - V_{dc_trig} - V_f \tag{26}$$

where V_c is the capacitor voltage, V_{dc_trig} is the dc-link when the module is activated and V_f is the diode forward voltage drop. Current i_d flowing through the inductor increases linearly as governed by the following

$$V_L = L\frac{di_d}{dt} \tag{27}$$

Energy supplied by capacitor C_a at start of compensation is used to charge up VSD capacitor C_e, energize inductor L and supply energy to the load. Energy, E_L stored in the inductor during energization is given by

$$E_L = \frac{1}{2}Li_d{}^2 \tag{28}$$

where L is inductance and i_d is the current flowing through the inductor. Energy stored in the inductor is maximum when the current flowing through it is at maximum i.e. at inrush current peak. Voltage drop across the inductor at this stage should be minimum.

Energy balance at start of compensation to inrush peak is governed by

$$E_{Ca} = E_L + E_{Ce} + E_{inv} \tag{29}$$

where E_{ca} is the energy supplied by the capacitor, E_L is the energy stored in the inductor and E_{inv} is the energy input into the inverter. Equation (29) can be written as

$$\frac{C_a}{2}\{V_{C1}^2(t_1) - V_{C2}^2(t_2)\} = \frac{C_e}{2}\{V_{dc1}^2(t_1) - V_{dc2}^2(t_2)\} + \frac{1}{2}Li_d{}^2 + P_{inv}(t_2 - t_2) \tag{30}$$

where $V_c(t)$ and $V_{dc}(t)$ are capacitor *Ca* and *Ce* voltages respectively at time *t*, P_{inv} is the inverter input power and (t_2 - t_1) is duration. For an inrush current i_d, the inductance *L* required to limit inrush current can thus be calculated from (30).

6.3.1. Simulation Results of Inductor Inrush Current Limiting Technique

Assume capacitor is pre-charged to a voltage of 540 V, module trigger voltage is set at 530 V, additional capacitance C_a is 16 mF, C_e is 265 µF, duration (*t2* - *t1*) is 1.5 ms and inverter power is 2.1 kW (motor and inverter efficiencies included). At maximum discharge current, there is no voltage across inductor and voltage difference capacitor and dc-link is due to parasitics. Using (29), the inductance required to limit inrush current to 6.2 A is calculated to be 2.5 mH.

Figure 6-10 shows simulation trends obtained with a 2.5 mH inductor. When module is activated for compensation, the voltage difference between C_a and dc-link appears across inductor *L*. Capacitor C_a does not immediately supply load current due to the inductor acting as an open circuit at start of compensation. This causes the dc-link capacitor to keep supplying power alone beyond the trigger voltage. Current through inductor linearly increases as capacitor C_e gets charged resulting in the dc-link voltage recovering and peaks at 6.3 A.

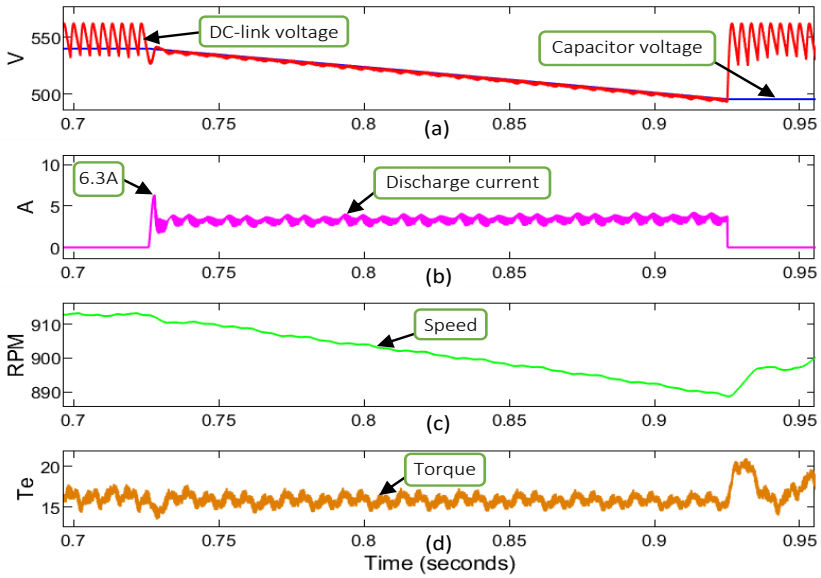


Figure 6-10.Simulation Results of Inductor Inrush Current Limiting Technique,
(a) Capacitor and DC-link Voltages, (b) Capacitor Discharge Current, (c) Speed and (d) Torque

When the dc-link capacitor is fully charged, there is a reduction in current demand but because inductor does not reduce current flow immediately, dc-link capacitor is overcharged above capacitor voltage. A change in direction of inductor voltage forward biases free-wheeling diode, allowing extra current to flow, where it is dissipated as heat in the diode. This allows the dc-link voltage to drop. Initial dc-link voltage oscillations are damped by the free-wheeling diode but not eliminated completely. These initial oscillations in the dc-link voltage result in significant torque and speed pulsations at start of compensation. Overall variations in key VSD and motor performance parameters are shown in Table 6-5.

Table 6-5. Impact of Inductor Inrush Current Limiting Technique on VSD and Motor Performance

Parameter	Value
Drop in dc-link voltage	10.6%
Drop in capacitor voltage	8.1%
Drop in torque	4.3%
Drop in speed	2.6%

6.3.2. Experimental Results

Figure 6-11 shows experimental results obtained using an inductor as the inrush current limiting element. An inrush current of 7.1A is measured at the start of compensation.

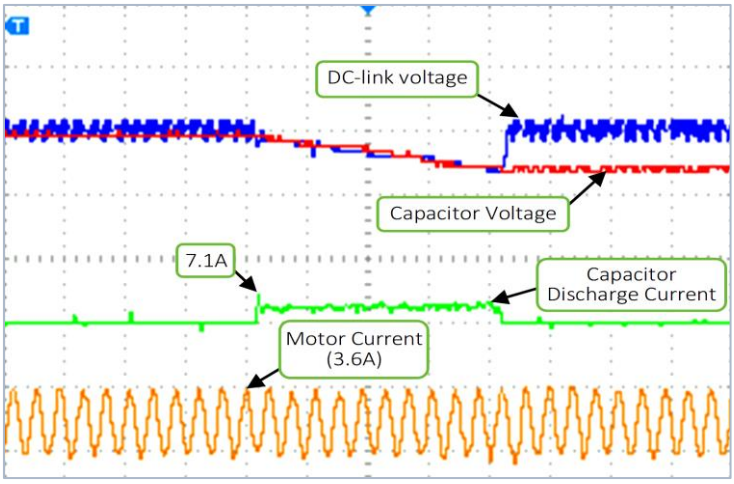


Figure 6-11. Experimental Results of Inductor Inrush Current Limiting Technique

The dc-link voltage decays at almost the same rate as the capacitor voltage. Instances where the dc-link voltage is greater than capacitor voltage indicate oscillations. Impact of module operation on torque and speed are shown in Figure 6-12.

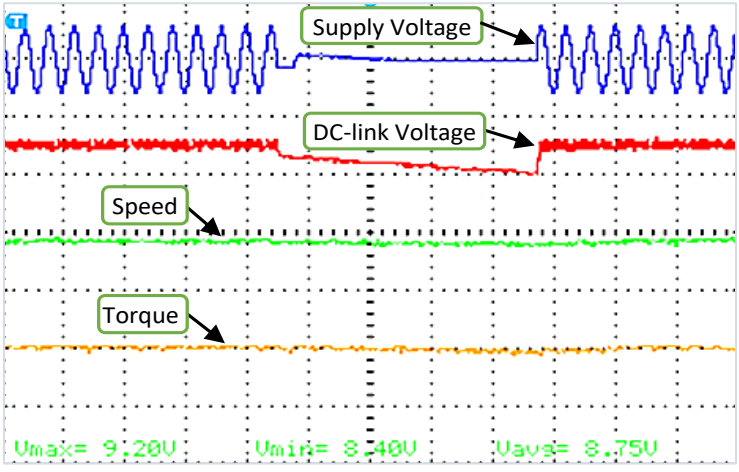


Figure 6-12. Impact of Inductor Inrush Current Limiting Technique on VSD and Motor Performance

Torque pulses of 15% and 12% are observed at start of compensation and restoration of supply. Table 6-6 summarizes the impact of inductor inrush current limiting technique on VSD and motor performance.

Table 6-6. Impact of Inductor Inrush Current Limiting Technique on VSD and Motor Performance

Parameter	Value
Drop in dc-link voltage	11.9%
Drop in capacitor voltage	9.9%
Drop in torque	10.1%
Drop in speed	1.2%

The drop in dc-link voltage is almost the same as of the capacitor with the final values at the end of compensation the same. This is so because of the small voltage drop appearing across the inductor, IGBT T_d, IGBT T_{dl}, and D_d at steady state. Oscillations in the dc-link voltage are evident. These oscillations are probably due to ringing between additional capacitor, VSD capacitor, VSD EMI suppression circuit and inductor. Care needs to be exercised with this technique to avoid introducing instability in the VSD due to excessive oscillations.

6.3.3. Module Losses and Efficiency

Figure 6-13 shows the PLECS simulation model to determine the losses and efficiency of the compensating module incorporating an inductor for inrush current limiting.

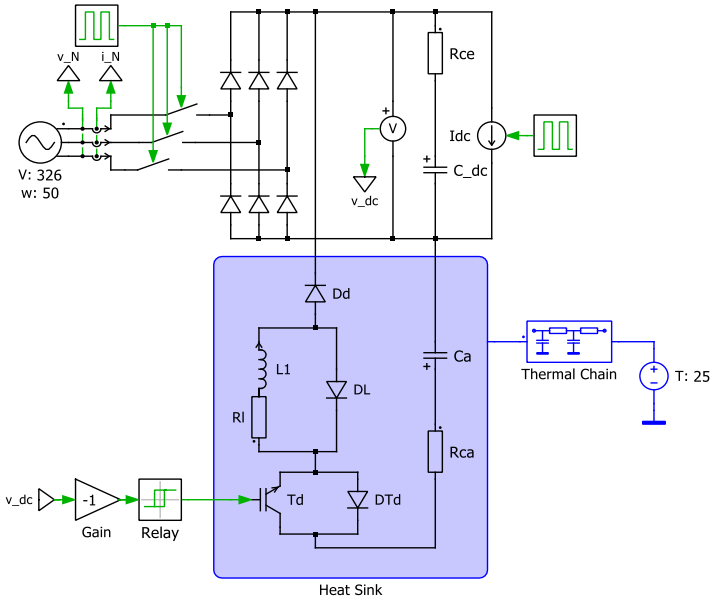


Figure 6-13. Module Losses and Efficiency Determination PLECS Simulation Model

Losses incurred by the module are shown in Figure 6-14. The overall efficiency of the module with variable resistor inrush limiting technique is 99.5%.

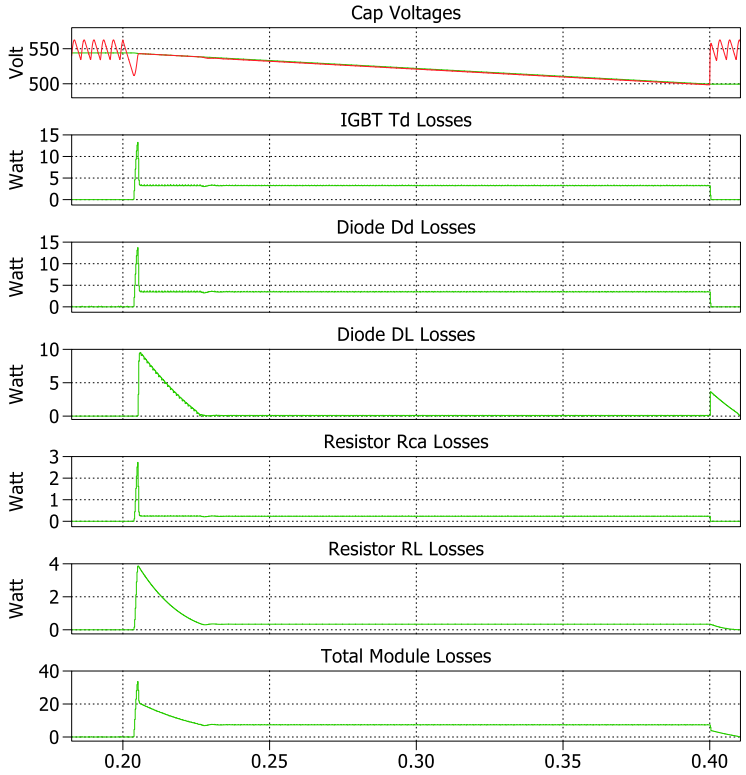


Figure 6-14. Inductor Inrush Current Limiting Technique Losses

Most losses are incurred at the start of compensation. Losses in the freewheeling diode at the start of compensation are linked to its damping action and at the end of compensation due to dissipation of energy trapped in the inductor.

6.3.4. Advantages and Disadvantages of Inductor Inrush Current Limiting Technique

Inductor inrush current limiting technique is easy to implement, results in reduced ohmic losses and a lower dc-link voltage drop. However, the dc-link voltage recovery is low which results in pronounced transient disturbances. The technique poses a risk of oscillations which, if not properly damped can introduce instabilities in the VSD.

6.4. Equipotential Voltage Switching (EVS) Technique

Inrush current flow at start of compensation is influenced by parasitic impedances of the discharge leg components, capacitor and dc-link voltages at instance of IGBT switching. This technique is premised on connecting the capacitor and dc-link when they are at the same voltage. Connecting the two capacitors at the same voltage minimises inrush flow. The only current expected to flow at that instant is the load current. This technique requires the capacitor to be pre-charged to the module trigger voltage.

6.4.1. Simulation Results

Figure 6-15 shows simulation results obtained. Simulation results indicate that inrush current is almost eliminated with this technique. DC-link and capacitor voltages drop at the same rate. Drops across dc-

link voltage and capacitor are the same indicating that the technique also eliminates the unwanted voltage drop.

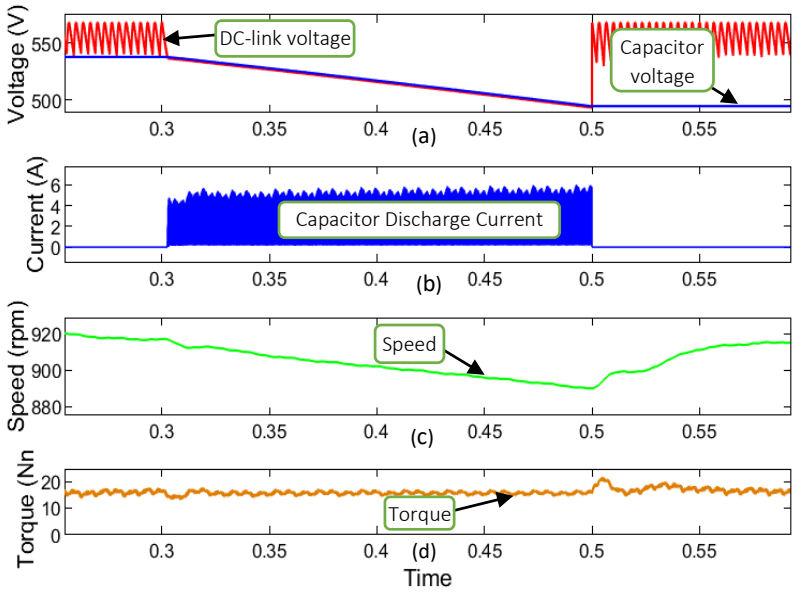


Figure 6-15. Equipotential Voltage Switching Inrush Current Limiting Technique, (a) DC-link and Capacitor Voltages, (b) Discharge Current, (c) Speed, (d) Torque

A gradual load transfer from dc-link capacitor to additional capacitor can be seen from Figure 6-16. This gradual transfer in load coupled with the reduced dc-link voltage results in a dip in torque which recovers once current has increased to nominal levels. The additional capacitor takes over the role of supplying high frequency currents flowing into the inverter from the VSD capacitor.

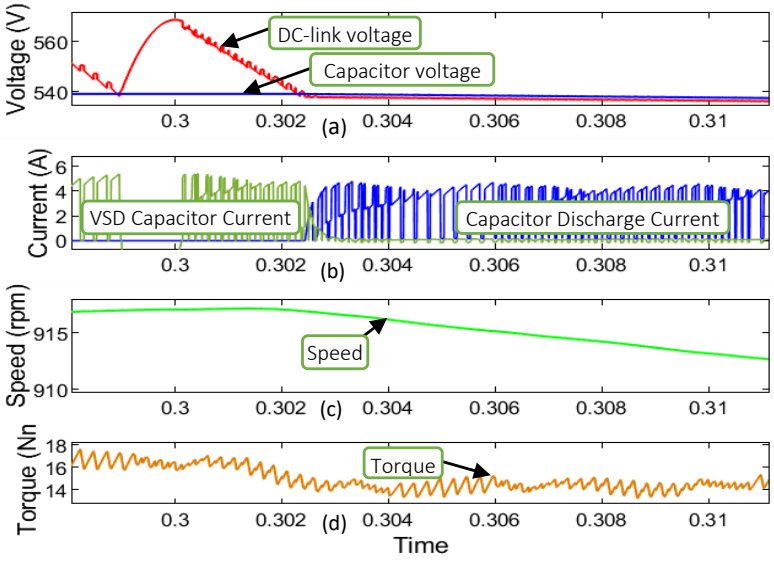


Figure 6-16. Equipotential Voltage Switching Technique Load Transfer During Compensation, (a) DC-link and Capacitor Voltages, (b) DC-link & Capacitor Currents, (b) Speed and (d) Torque

Inrush current at start of compensation is 4.8 A. This is against a VSD maximum continuous rating of 4.2A. Impact of technique on motor performance is summarised in Table 6-7.

Table 6-7. Impact of Equipotential Voltage Switching on VSD and Motor Performance

Parameter	Value
Drop in dc-link voltage	9.9%
Drop in capacitor voltage	9.8%
Drop in torque	3.2%
Drop in speed	1.2%

Torque pulsations of 6.8% and 9.8% are observed at start and end of compensation. As anticipated, voltage drop across the dc-link and capacitor are same. The technique produces a small drop in torque during the compensation period.

6.4.2. Module Losses and Efficiency

Figure 6-17 shows the PLECS simulation model to determine the losses and efficiency of the compensating module utilizing equipotential voltage switching inrush current limiting technique.

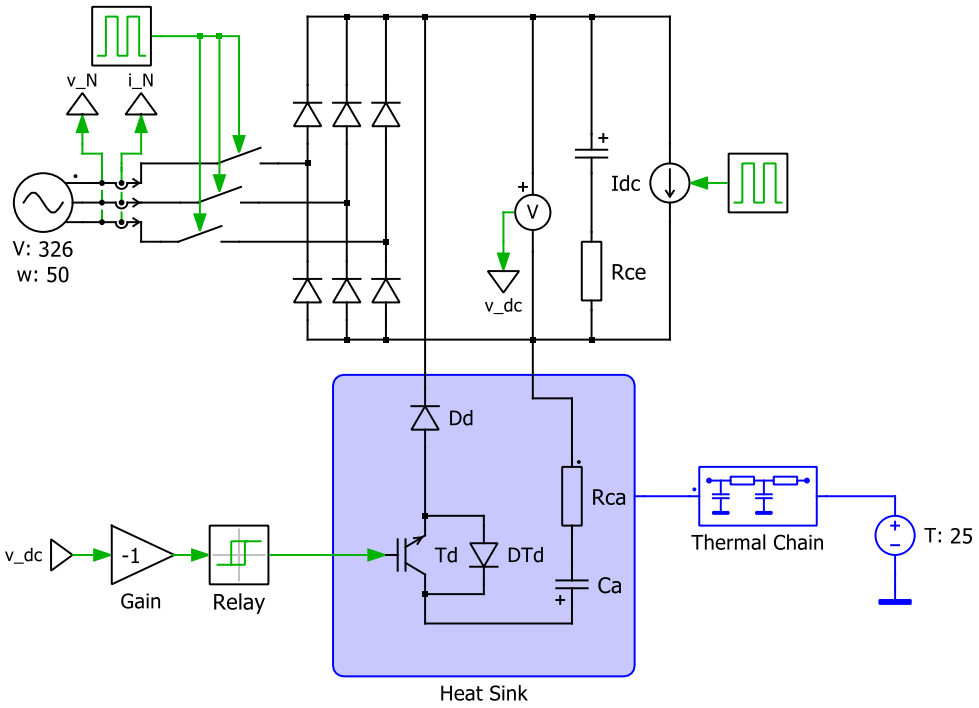


Figure 6-17. Module Losses and Efficiency Determination PLECS Simulation Model

Losses incurred by the module incorporating EVS inrush current limiting technique are shown in Figure 6-18. The overall efficiency of the scheme is computed to be 99.6%.

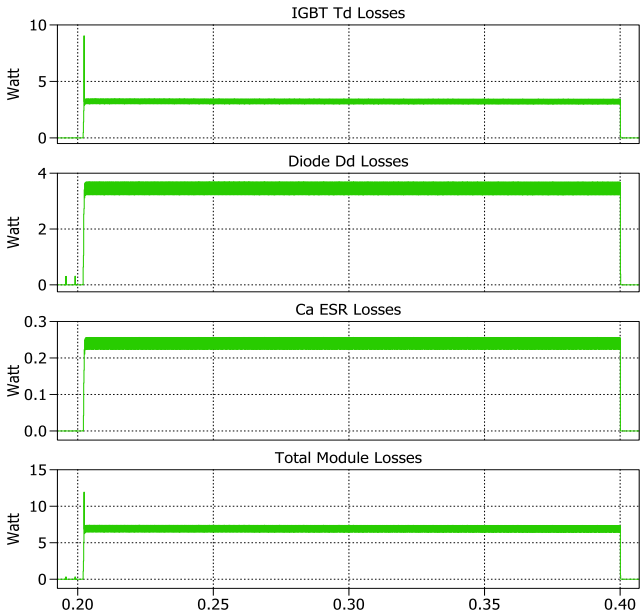


Figure 6-18. Equipotential Voltage Switching Technique Losses

Overall losses for this scheme are low.

6.4.3. Advantages and Disadvantages

Equipotential voltage switching technique minimises unwanted voltage drop and reduces losses resulting in a higher efficiency. It results in lower dc-link voltage, torque and speed drop during compensation. Torque pulsations experienced during start and end of compensation are low. With this technique less components are required. High frequency ripple currents from PWM inverter flow through the capacitor. The additional capacitor needs to be sized to withstand these high frequency currents. Detection and measurement circuit needs to be fast and accurate to ensure that switching is done when dc-link voltage and capacitor voltages are the same. A special charging scheme is required to keep the capacitor pre-charged to a lower voltage which increases the overall complexity of the scheme.

6.5. Comparisons of Inrush Current Limiting Techniques

Results of comparisons between the inrush current limiting techniques are summarized in Table 6-8, Table 6-9 and Table 6-10.

Table 6-8. Comparisons Between Inrush Current Limiting Techniques

Technique	DC-link Voltage Drop	Cap Voltage Drop	Torque Drop	Speed Drop	Torque pulse at start of compensation	Torque pulse at restoration of supply
Fixed resistor	18.0%	10.3%	10.6%	2.5%	12.8%	14.3%
Variable resistor	12.2%	10.3%	9.8%	1.7%	11.6%	9.1%
Inductor	11.9%	9.9%	10.1%	1.2%	15.0%	11.9%
ESV	9.9%	9.8%	3.2%	1.2%	6.8%	9.8%

Table 6-9. Efficiency Comparisons

Technique	Efficiency
Fixed Resistor	94.8%
Variable Resistor	99.3%
Inductor	99.5%
EVS	99.6%

Table 6-10. Qualitative Comparison of Inrush Current Limiting Techniques

	Fixed Resistor	Variable Resistor	Inductor	EVS
Voltage drop across element	Significant	Low	Low	Low
Voltage rate of rise	High	High	Low	Low
Current rate of rise	High	High	Low	Low
Copper losses	High	Moderate	Low	Low
Complexity	Basic	High	Basic	High

The fixed resistor inrush limiting technique produces the greatest drops in torque and speed over the STPI and is the least efficient. This can be attributed to the largest dc-link voltage drop caused by the additional voltage across the limiting resistor and conduction losses. A larger drop in dc-link voltage causes a significant drop in torque. Equipotential switching technique results in the least dc-link voltage drop, least drop in torque and produces the highest module efficiency. Module efficiency is high due to a reduction in additional parasitic resistances as a result of few components. The inductor technique produces the highest torque and speed pulsations at the start of compensation. It poses some oscillation risk in the dc-link voltage. Design of a damping circuit for use with inductor technique without the knowledge of VSD circuit parameters presents a challenge when implementing a solution for an existing VSD. Module efficiencies with equipotential voltage switching, variable resistor and inductor techniques are high and very comparable. The requirement for a fast and accurate detection and switching system for ESV technique makes it highly complex. In addition, it requires a capacitor with a higher ripple current rating.

6.6. Summary of Inrush Current Limiting Techniques

The use of the fixed resistor does reduce the inrush current however results in increased losses and reduced dc bus voltage during a short-term interruption. Proposed inrush current limiting schemes utilizing an inductor, variable resistor and equipotential voltage switching were investigated. The three schemes were found to increase the overall module efficiency and reduce voltage drop across the discharge leg. The inductor poses a risk of oscillations which requires a proper damping circuit to avoid ringing with the capacitors. Equipotential voltage switching technique results in the least dc-link voltage drop, least drop in torque, introduces least disturbances during start and end of compensation and produces the highest module efficiency. However, it is complex to implement and requires a higher ripple current rating capacitor which is more expensive.

Chapter 7
Conclusions and Future Work

7.1. Conclusions

7.1.1. Chapter 3

From literature review, it can be concluded that there is no single ride-through alternative that can meet requirements for all applications. A case-by-case evaluation needs to be made considering equipment sizes, interruption costs and capex requirements. Thus, before a solution is developed, a technical and financial evaluation to determine most appropriate technique needs to be carried out.

7.1.2. Chapter 4

VSD ride-through improvement utilising additional capacitors requires inrush currents to be minimised. Magnitude of inrush current at start of compensation and charging is influenced by dc-link voltage, capacitor voltage and total leg resistance. By altering any one of these, inrush current can be controlled by varying degrees. It has been established that size of additional capacitor required for the module is influenced by load demanded, characteristic of voltage disturbance (magnitude and duration), inrush current limiting technique adopted and VSD operating envelope. When sizing the additional capacitor for module incorporating fixed resistors for inrush current limiting, provisions for energy losses and voltage drop across the resistor must be made.

7.1.3. Chapter 5

The proposed power electronics module for improving the undervoltage ride-through of a VSI-VSD to a 0.2s STPI was successfully tested. A drop in dc-link voltage resulted in a drop in torque and speed of the motor. Methods for sizing the additional capacitor and inrush current limiting resistors using readily available information were tested and validated. A module sizing method for different sized VSDs is possible. Use of fixed resistors for inrush current limiting result in loss of module efficiency and results in unwanted voltage drops. Even though the objective of the module in retaining the operation of the VSD is achieved.

7.1.4. Chapter 6

Use of inductor, variable resistor and equipotential voltage switching results in increased module efficiency and a reduction in voltage drop across limiting element. When using the variable resistor for inrush current limiting technique, sizing of components needs to factor inrush current flowing during PWM switching. to avoid exceeding pulse rating of the device. Use of an inductor for inrush current limiting needs proper circuit damping to avoid continuous oscillations. From comparisons made, equipotential voltage switching inrush current limiting technique appears to be the most favourable inrush

technique based on quantitative measurements. However, its complexity and cost when compared to the variable resistor makes it less attractive for use with the module. This leaves the variable resistor technique as the technique of choice for use with the module.

7.2. Summary

Ride-through improvement solution for a 1.5kW drive to a 0.2 s STPI incorporating a capacitor as an energy storage device was developed. During testing of the solution, it was observed that the start of compensation and charging was associated with high inrush currents which affected the motor's transient behaviour (torque pulsation, torque drop and speed drop). To manage inrush current and consequently the motor's dynamic behaviour, 4 techniques were investigated. Each technique impacted the motor transient behaviour differently. Maximum speed drop of 2.5% and maximum torque drop of 10.6% during the 0.2 s STPI were achieved. Maximum torque pulsation of 15% were also achieved. Sizing methodologies for a capacitor, inrush current limiting resistor and inrush current limiting inductor for use on different sized VSDs were developed, tested and validated making the solution scalable.

7.3. Future Work

The research study focused on investigating and implementing a solution to allow a VSD to ride-through a 0.2s STPI which represents the worst-case voltage disturbance. The module was developed and tested successfully for a case in which the VSD and motor were in steady state prior to the STPI. To further improve on the current solution, the following future activities are recommended:

a. Investigate and establish thermal behaviour of the module.
b. Investigate module behaviour during VSD and motor transient conditions.
c. Investigate and establish behaviour of VSD and motor when under vector control.

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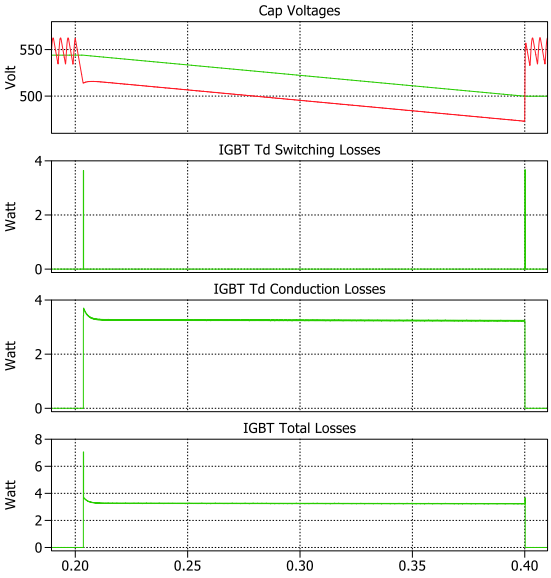
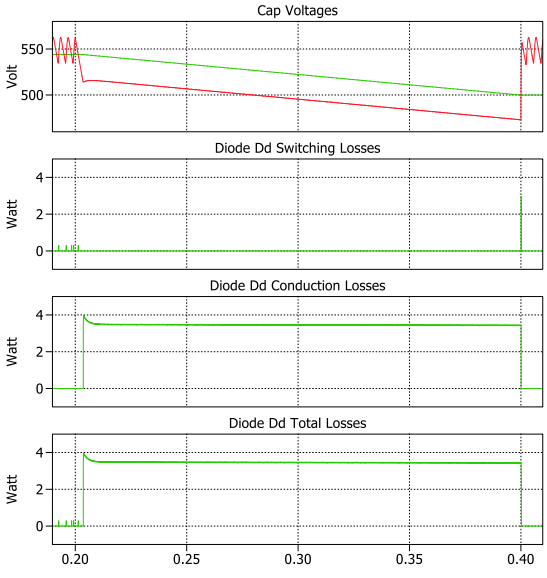
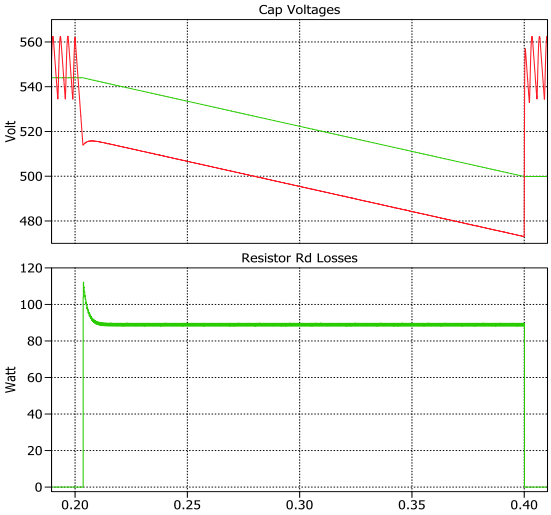
Appendix 1-1: Fixed Resistor Inrush Current Limiting Technique Losses



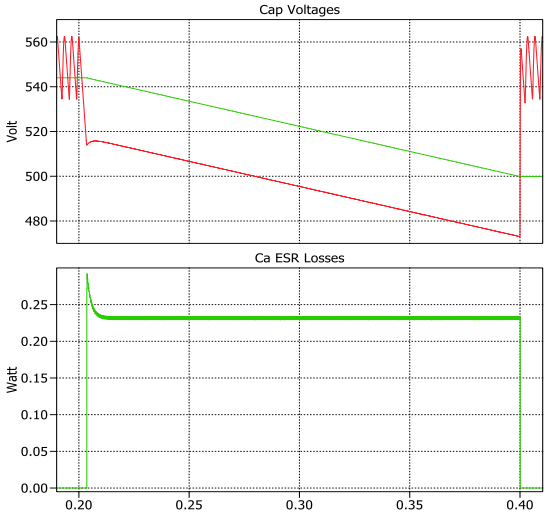
IGBT Td Losses



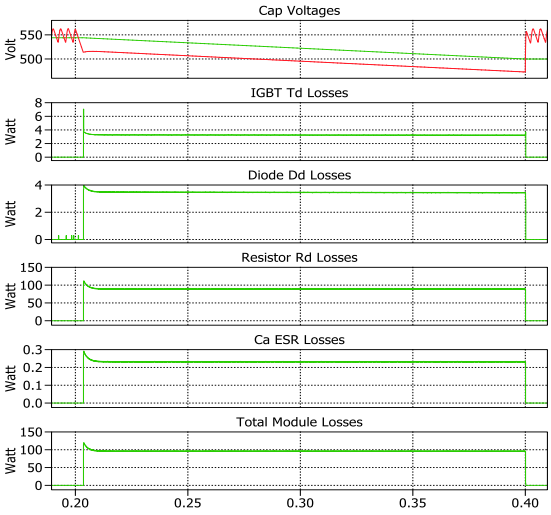
Diode Dd Losses



Resistor Rd

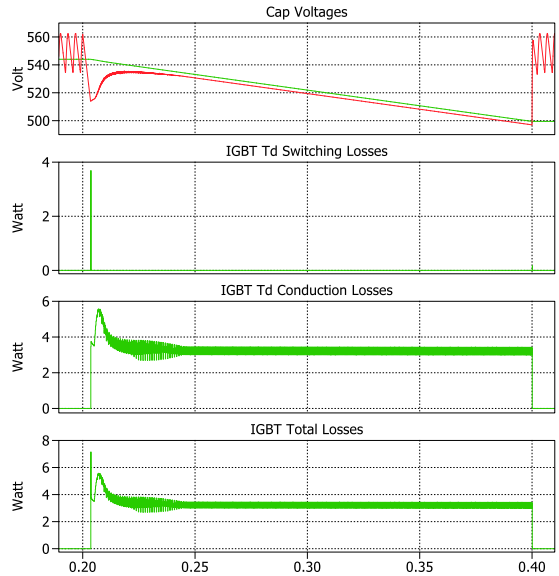


Ca ESR

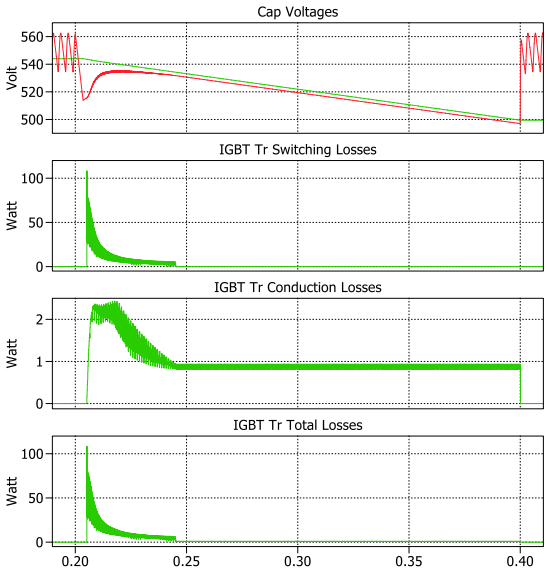


Total Losses

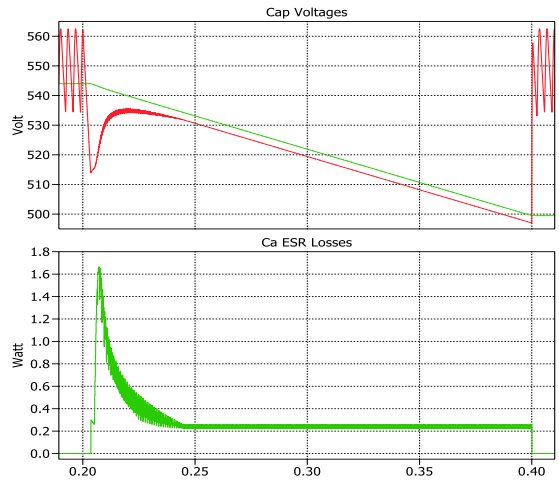
Appendix 1-2: Variable Resistor Inrush Current Limiting Technique Losses



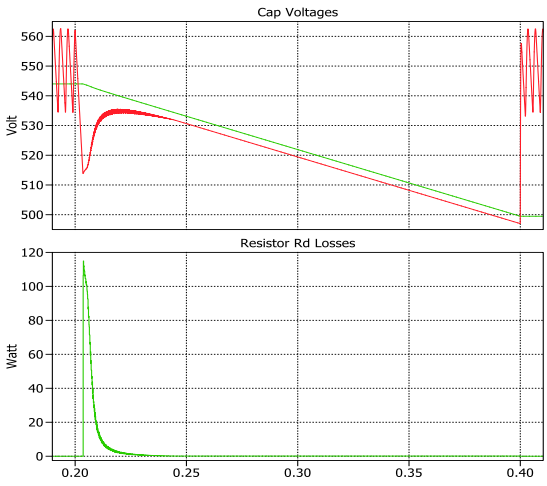
IGBT Td Losses



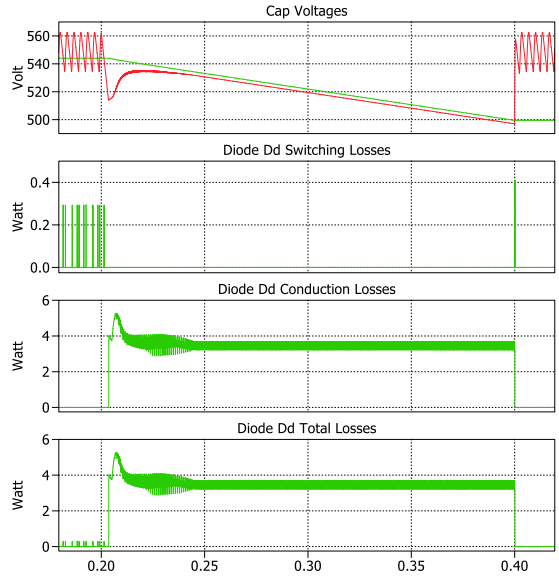
IGBT Tr Losses



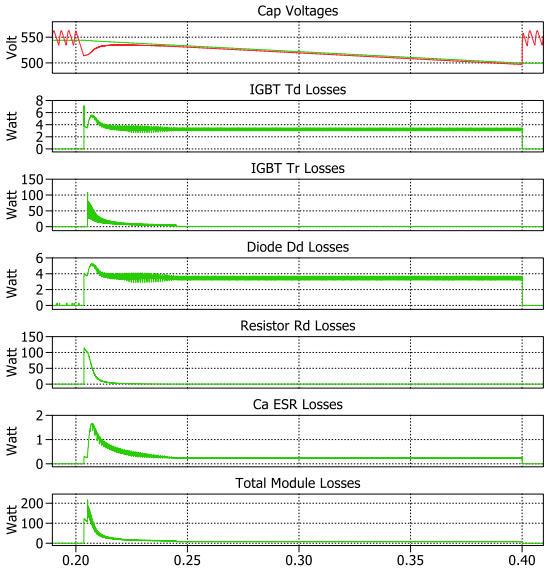
Ca ESR Losses



Resistor Rd Losses

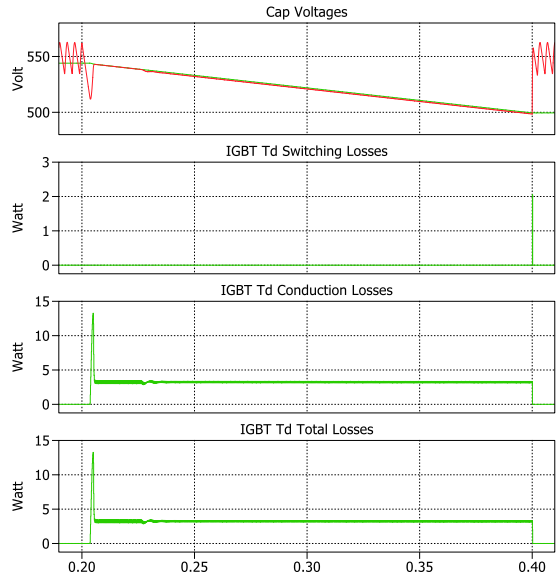


Diode Dd Losses

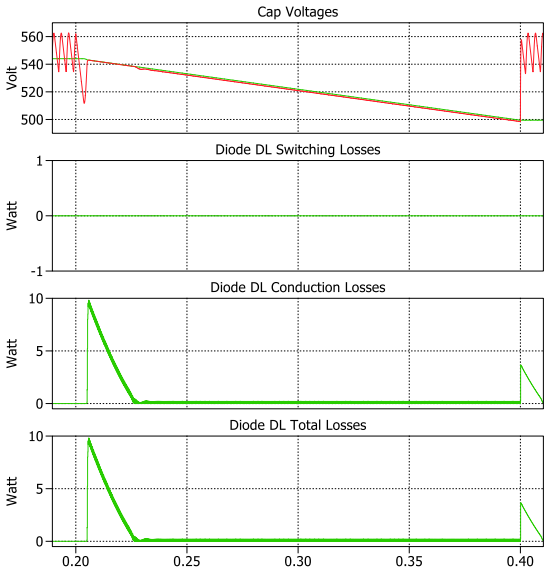


Total Losses

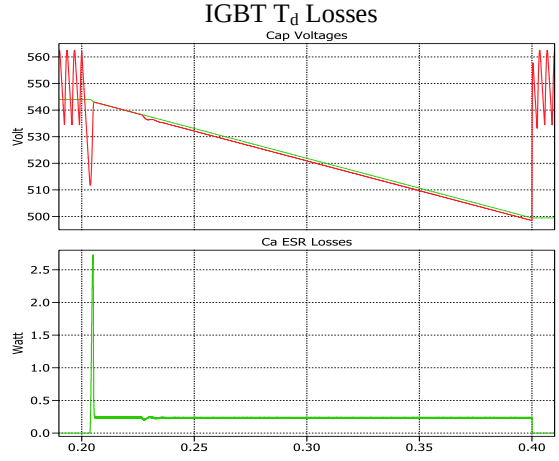
Appendix 1-3: Inductor Inrush Current Limiting Technique Losses



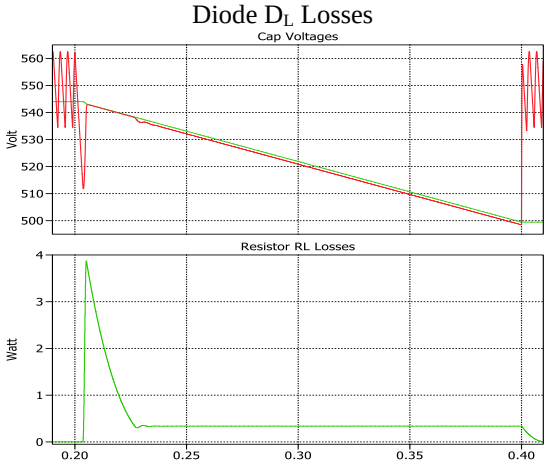
IGBT T_d Losses



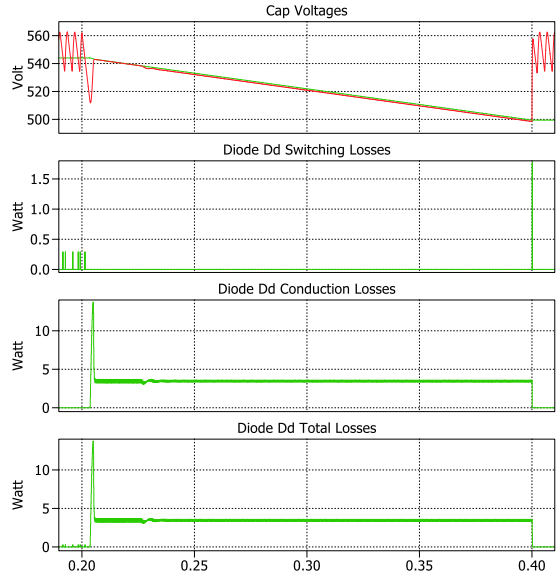
Diode D_L Losses



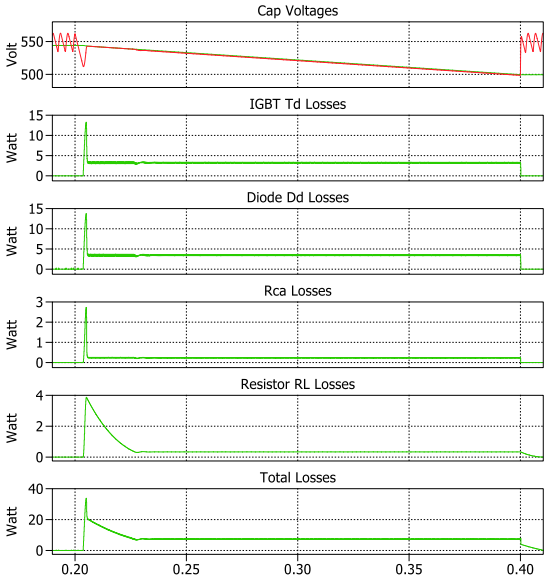
Ca ESR Losses



Resistor R_L

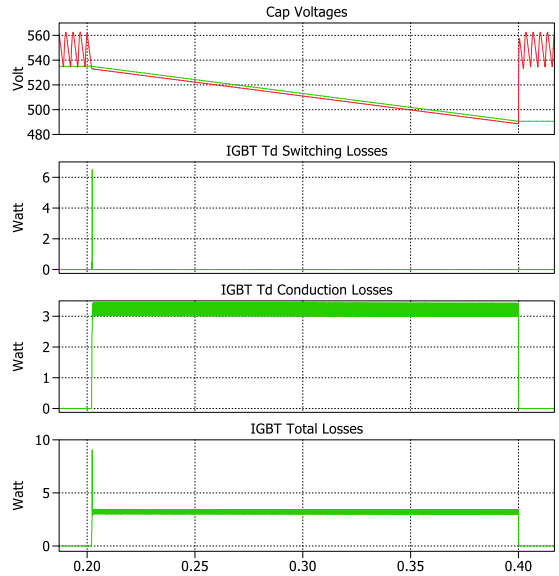


Diode D_D Losses

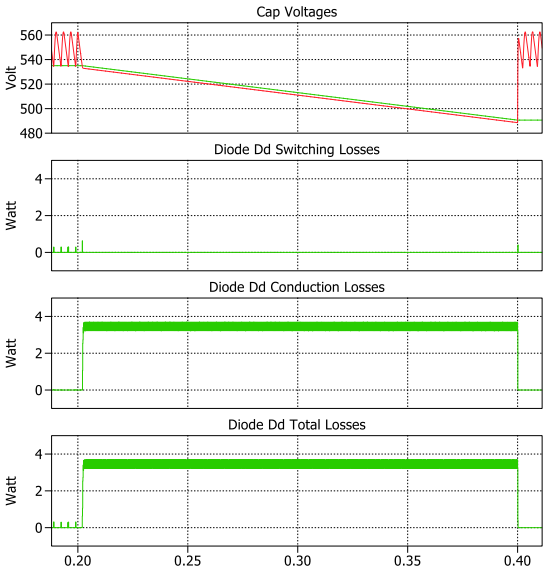


Total Losses

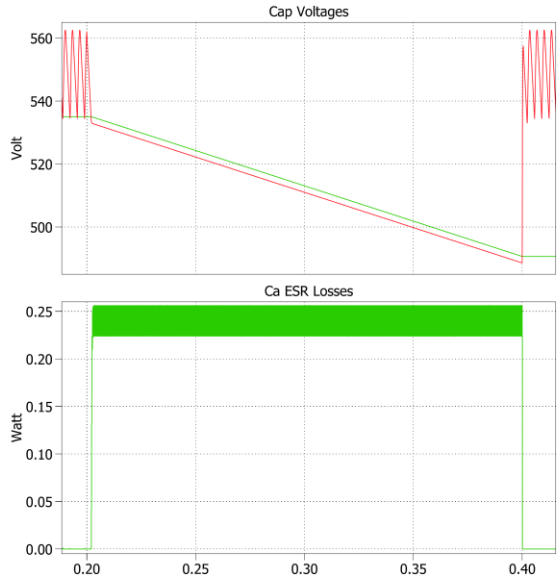
Appendix 1-4: Equipotential Voltage Switching Technique Losses



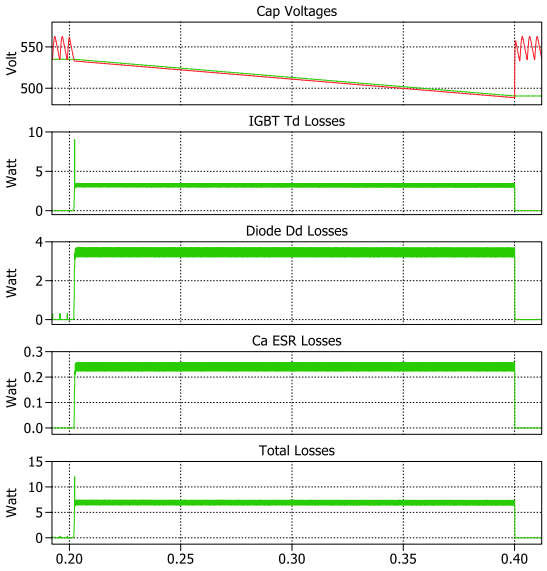
IGBT T_d Losses



Diode D_D Losses

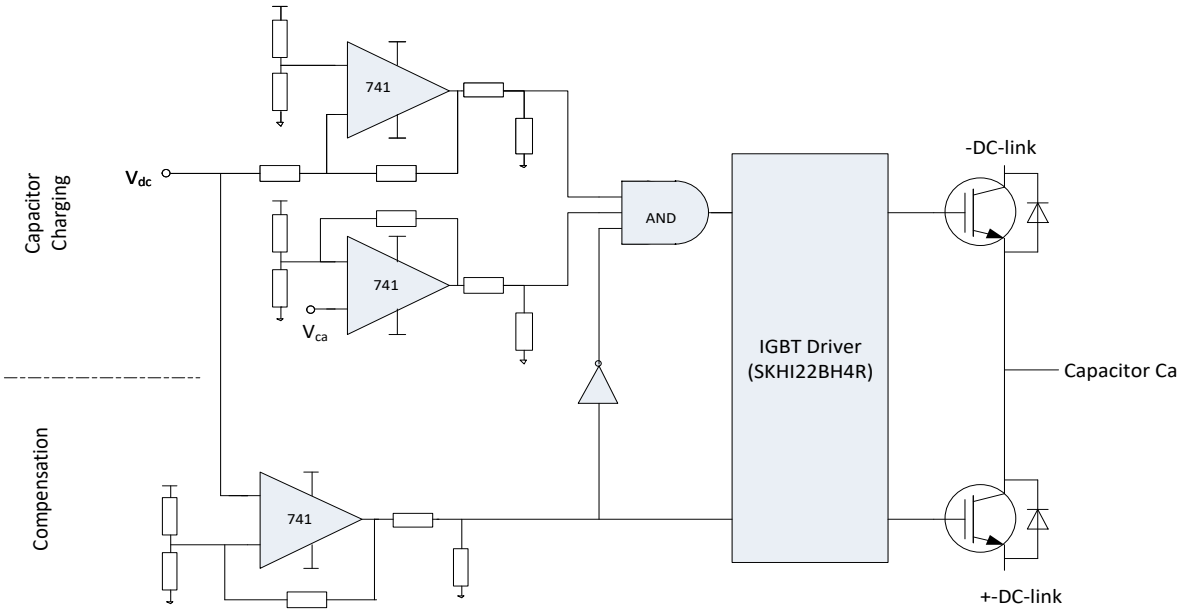


Ca ESR Losses

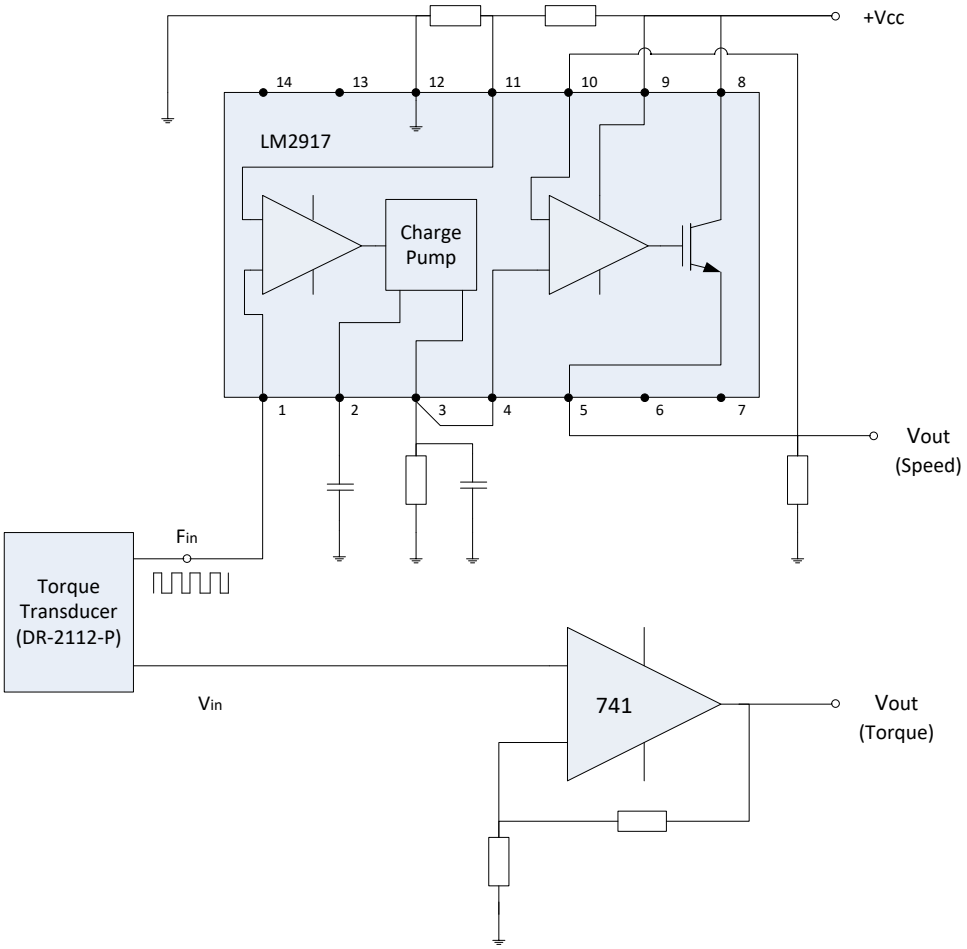


Total Losses

Appendix 2: Compensating and Charging Control Circuit



Appendix 3: Torque and Speed Measurement Circuit



Appendix 4: Component Details

Variable Speed Drives	Manufacturer	Part Number
2-quadrant VSD	Schneider	ATV312HU15N4
4-quadrant VSD	Siemens	6SL3225-0BE25-5AA1

Electrical Motors	Manufacturer	Serial No
1.5kW induction motor	Marathon	822208/021-002
2.2kW induction motor	Actom Electrical Machines	4018193/013/HL

Programmable Logic Controller	Manufacturer	Part Number
S7 PLC	Siemens	6ES7214-1BG40-0XB0

Transducers	Manufacturer	Part Number
Torque Transducer	Lorenz Messtechnik	DR-2112-P
Voltage Transducer	LEM	LV25-P
Current Transdcuer	LEM	LA55-P
Frequency to voltage converter	Texas Instruments	LM2907-8

Compensating Module

Component	Manufacturer	Part Number
IGBT	Semikron	SKM75BG12V
IGBT Driver	Semikron	SKHI22BH4R
Directional Diodes	Semikron	SKN2F50
Capacitor	Kemet	ALS7(1)(2)243QT350

Inductor Inrush Current Limiting Technique

Component	Manufacturer	Part Number
Inductor	Hammond Manufacturing	195E30
Diode	ON Semiconductor	FFP3065B

Variable Resistor Inrush Current Limiting Technique

Component	Manufacturer	Part Number
Voltage controlled pulse width modulator	Linear Technology	LTC6992-1
IGBT	Semikron	SKM300GA12V