

## APPENDIX A

Detailed description of the design and operation of the circuit

- 1 The major circuits can be divided up as follows:
  - a. Input filter.
  - b. Resonance circuit.
  - c. Amplification/ Peak detector/ reset circuitry.
  - d. Switch selection circuit.
  - e. Analogue switch/ sample-and-hold/ analogue-to-digital converter circuit.
  - f. Microprocessor interface board.

- 2 Input filter

The input filter is designed to remove all mains frequencies and components of the mains frequency while leaving the partial discharge unattenuated. A partial discharge is very close to an impulse in character and hence it contains a very wide spectrum of frequencies. The bandwidth of signals is in the region of DC to 400MHz, but the bandwidth of the main signal up to the tenth harmonic is only 500Hz.

In this system the resonance circuit used has a fundamental frequency of 80KHz, which means that it is more than three decades from the mains fundamental, and



more than two decades above the tenth mains harmonic. Thus all frequencies below 80KHz can be filtered irrespective of whether they are generated by the mains or the partial discharge. This alleviates the need for a notch filter to remove the mains.

The minimum output voltage from the resonance circuit is 1mV, and the mains must be attenuated to at least 3 orders of magnitude less than this. The maximum power voltage input is 100KV, and this requires attenuation to 1 micro volt, leaving the 80KHz signal produced by the resonance circuit unaffected. This is an attenuation of 220dB in a frequency span of just greater than three decades, or approximately 70dB/decade. If a cut off frequency of 50KHz were chosen, a fourth order filter would remove the input waveform, but this cut off frequency distorts the signal from the resonance circuit.

The most workable compromise was found to be five cascaded RC filters with individual cut off frequencies of 10; 5; 2.5; 1.25KHz and 612Hz.

The coupling capacitor from the high voltage supply is used as the first capacitor in the filter, and hence this value is set. Further, the filter has the capability of accepting input capacitors in the range



10pF to 1nF while not affecting the performance of the filter unduly. The filter is shown in Figure A1.

### 3 Resonant circuit

The resonant circuit used is a commercially available unit produced for the ERA discharge detector system. It is an extremely well designed unit which produces a very clean decaying sine wave. Great care has been taken in the design and construction of the unit. This unit contains a parallel RLC which resonates at a fundamental frequency of 80KHz and produces a signal with an initial peak and two overshoots.

When used with the ERA discharge detector the resonant circuit coil is the primary winding of a stepdown transformer. This makes the signal too small for the digital system to process and hence the signal needed to drive the input of the digital detector is derived from the input side of the resonant circuit. The decay time is reduced quite considerably if the output of the stepdown transformer is short circuited, and this is done in the system. The circuit diagram is shown in Figure A2.

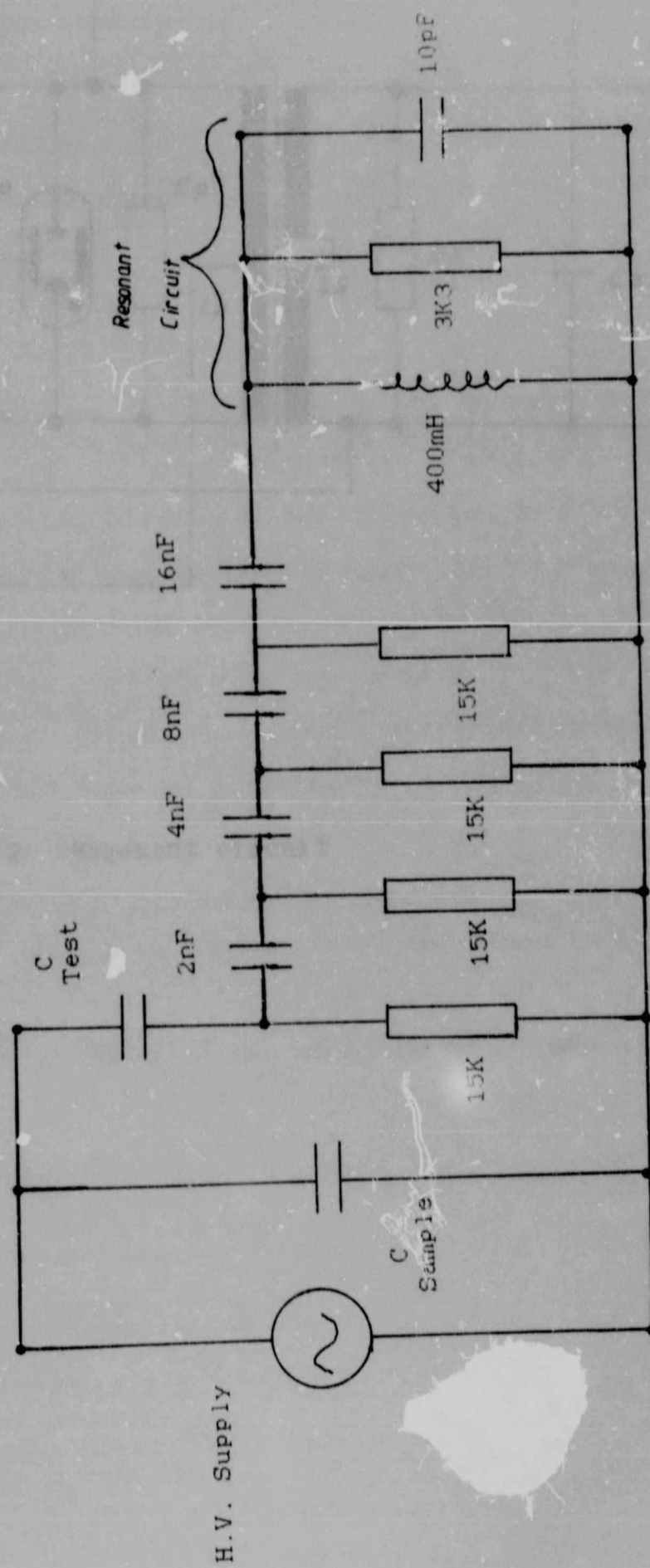


Figure A1 Input filter



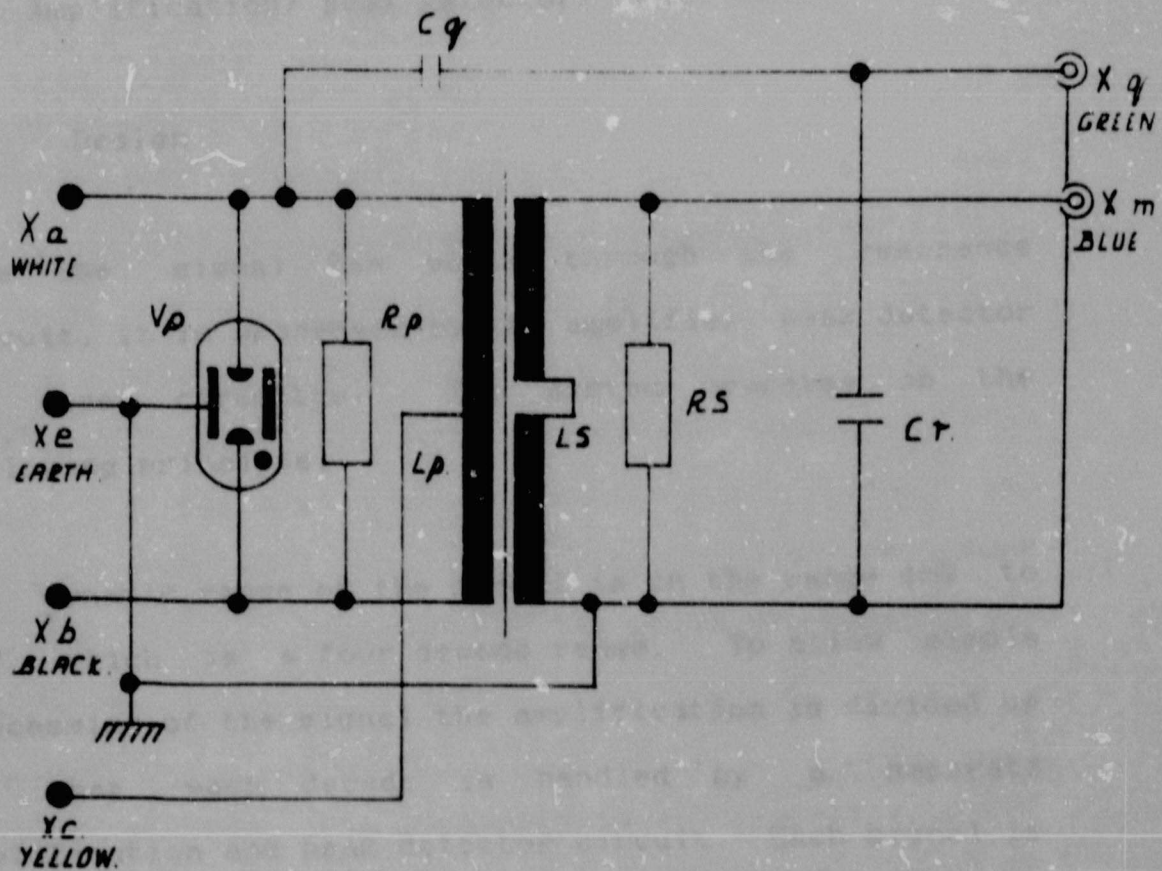


Figure A2 Resonant circuit



#### 4 Amplification/ peak detector/ reset circuitry

##### 4.1 Design

Once the signal has passed through the resonance circuit, it is processed by the amplifier, peak detector and reset circuitry. The system operates on the following principle:

The dynamic range of the signal is in the range 1mV to 10V, which is a four decade range. To allow simple processing of the signal the amplification is divided up so that each decade is handled by a separate amplification and peak detector circuit. Each signal is amplified until it lies in the range 1 to 10V which enables the peak detectors and the sample-and-hold to operate in their areas of greatest linearity. The four decade ranges are:

1mV to 10mV, 10mV to 100mV, 100mV to 1V and 1V to 10V.

The 1mV to 10mV range is amplified by 1000, the 10mV to 100mV range is amplified by 100, the 100mV to 1V range is amplified by 10 and the 1V to 10V range is amplified by 1.

Following the amplifiers the signal paths are split between the positive and negative peak detectors. This



is necessary because the peak detectors are unipolar in operation and the signals are bipolar by nature. These detectors are designed to follow the input signal until the peak is reached and then this peak is held. A large hold capacitor is used and therefore the decay time of the peak detector is slow. This means that if a large signal is followed immediately by a small signal the small signal will not be detected because the peak detector is still charged to the value of the larger discharge.

Because of this it is necessary to incorporate a reset circuit to reset the peak detector which will allow it to detect all signal peaks. This operates so that the peak detector is reset before the next peak is detected. This circuit also generates a signal when the signal peak has been detected which is used both in the reset circuitry, and to operate the sample-and-hold and analogue-to-digital converter.

In this system it is necessary to use two printed circuit boards for the four amplification channels, two channels on each board. The one board carries the 1000 and the 100 amplification channels and the other the 10 and 1 amplification channels.



## 4.2 Operation

### 4.2.1 Amplifier

The full circuit diagram is shown in Figure A3 (Sheets 1,2,3).

First, the signal is buffered by (IC 1) in order to stop the inverting amplifier IC2 and IC3 from loading the resonant circuit of the discharge detector. This also stops spurious signals generated by the peak detector from being fed back into the resonant circuit. Following the buffer, the signal is split to the two amplification channels, times 1000 and times 100 are on the one board and times 10 and time 1 are on the other. Following the amplifier, each channel is duplicated, and identical.

The signal is amplified by a pair of inverting amplifiers (IC2 and IC3). These must be DC coupled, fast slewing, low drift operational amplifiers, with offset correction. The reason for the DC coupling is that the peak from the peak detector is referred to system ground, and this reference must be preserved to obtain the correct peak value. A fast slew rate is required because the rising edge of the signal is very fast, and slew rate limiting is experienced by the amplifiers causing the peak to be reduced and thus reducing the sensitivity. The offset must be



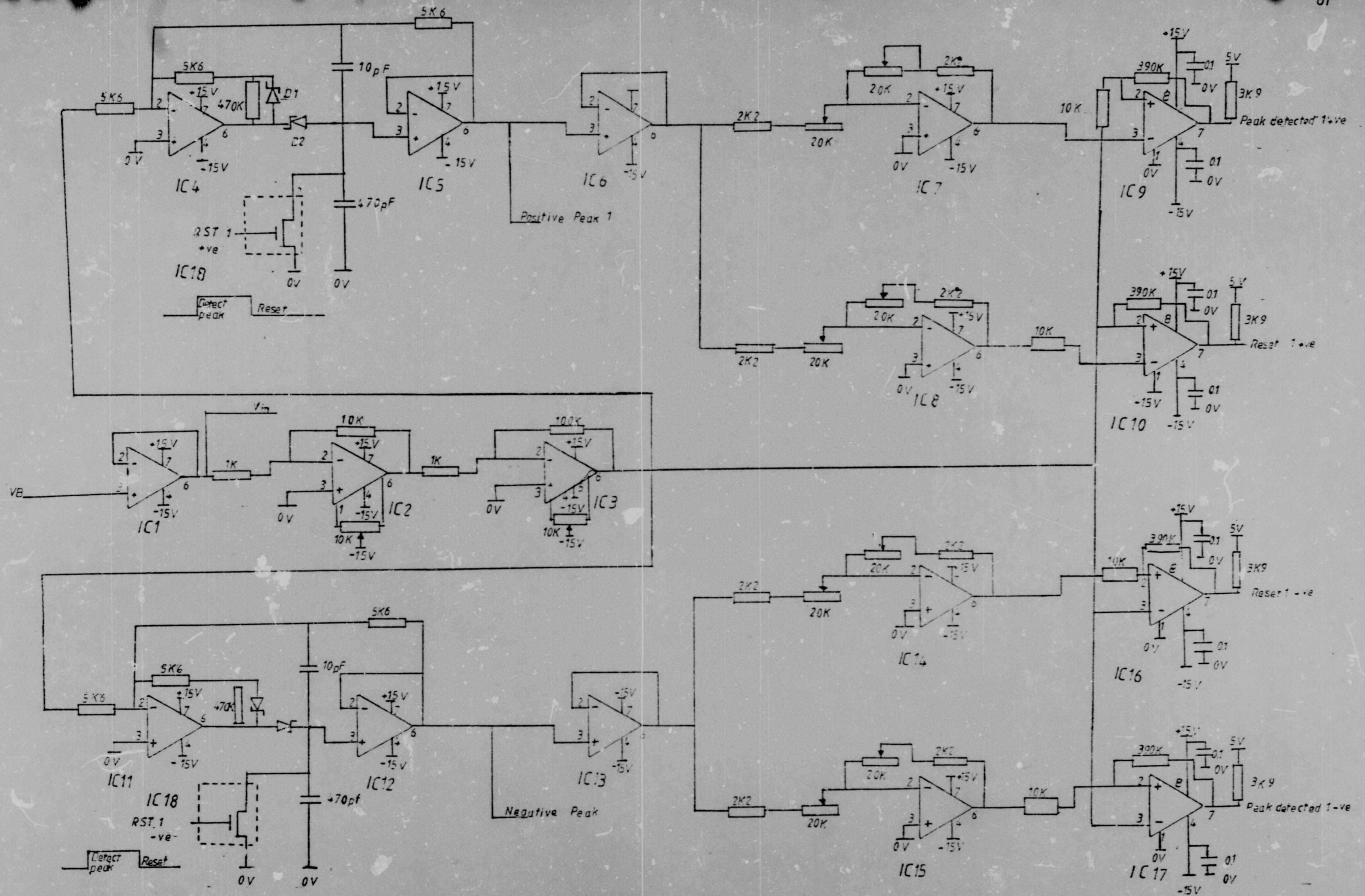
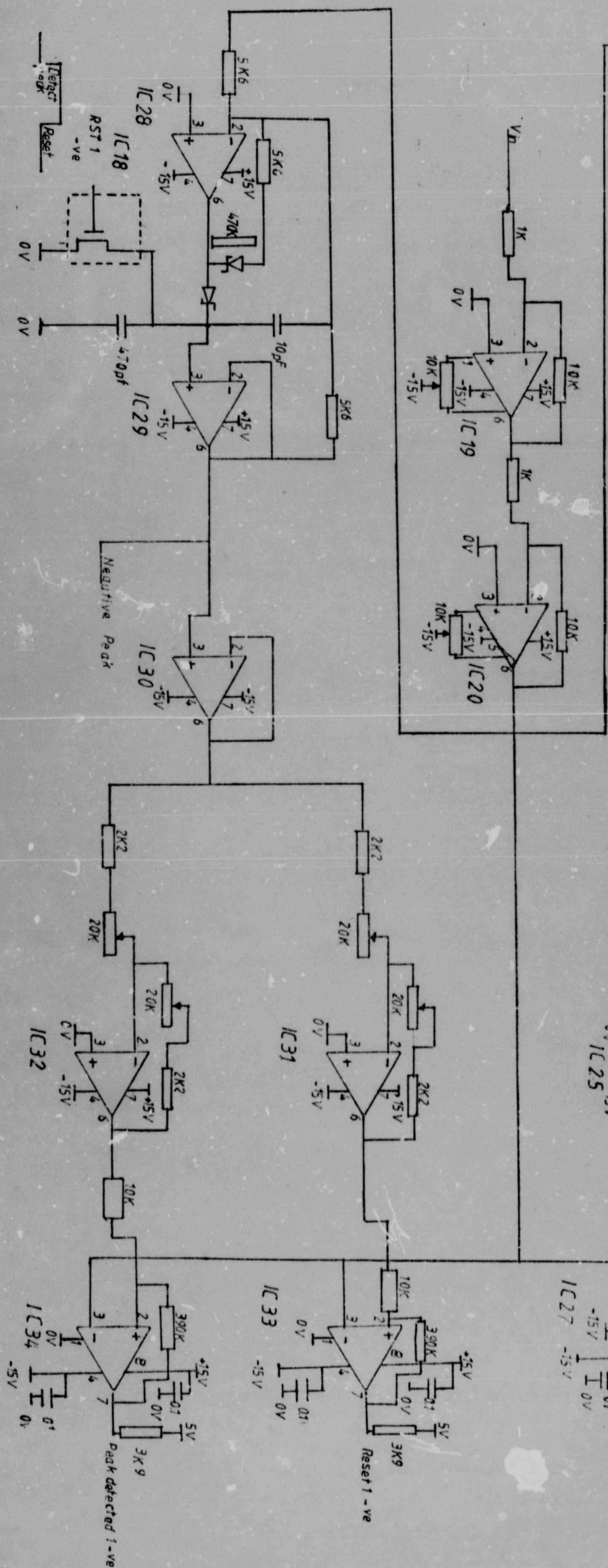
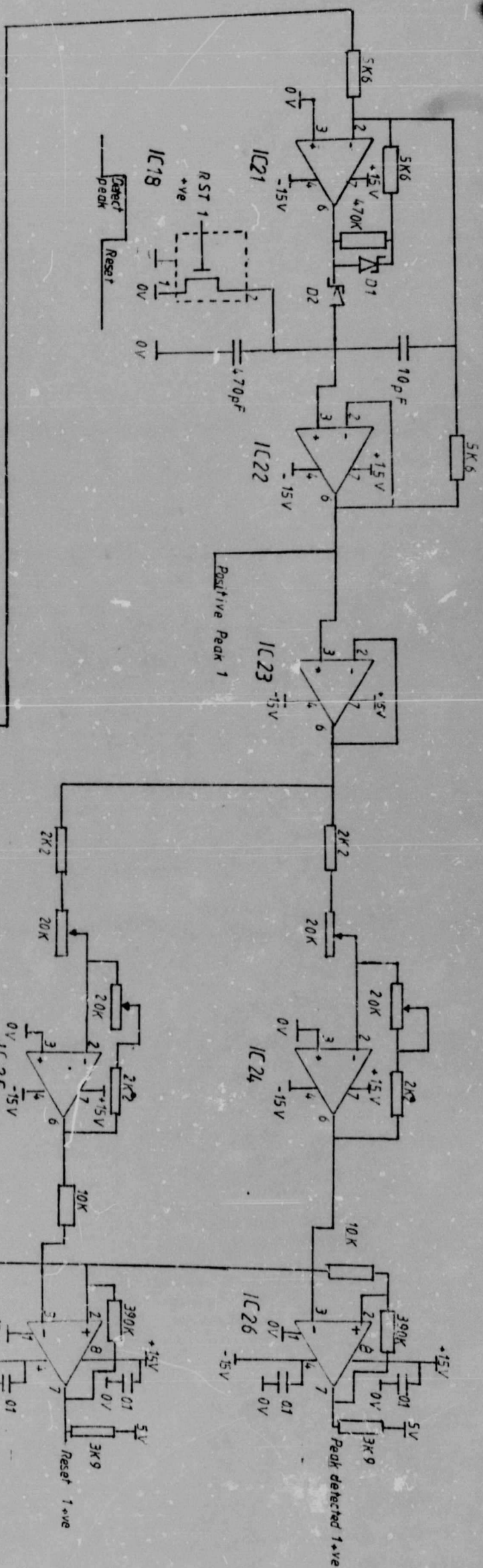
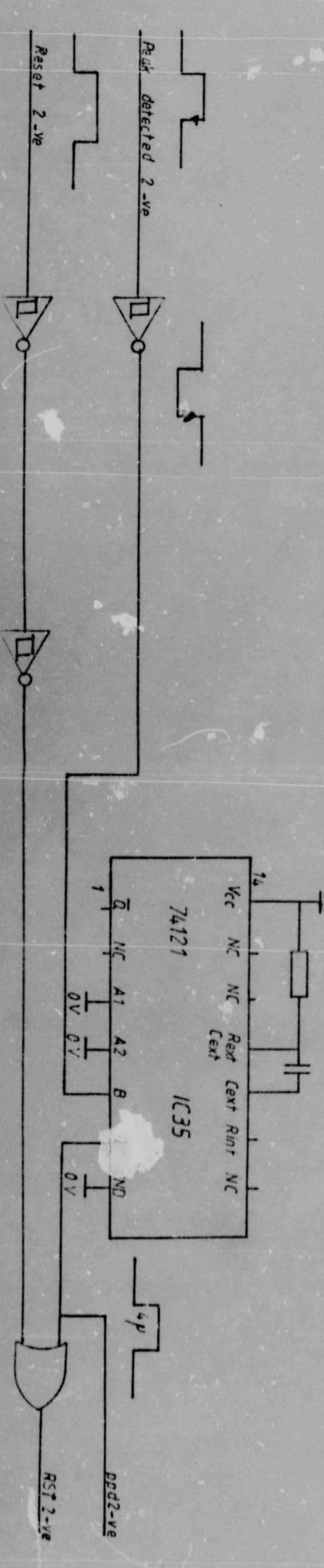
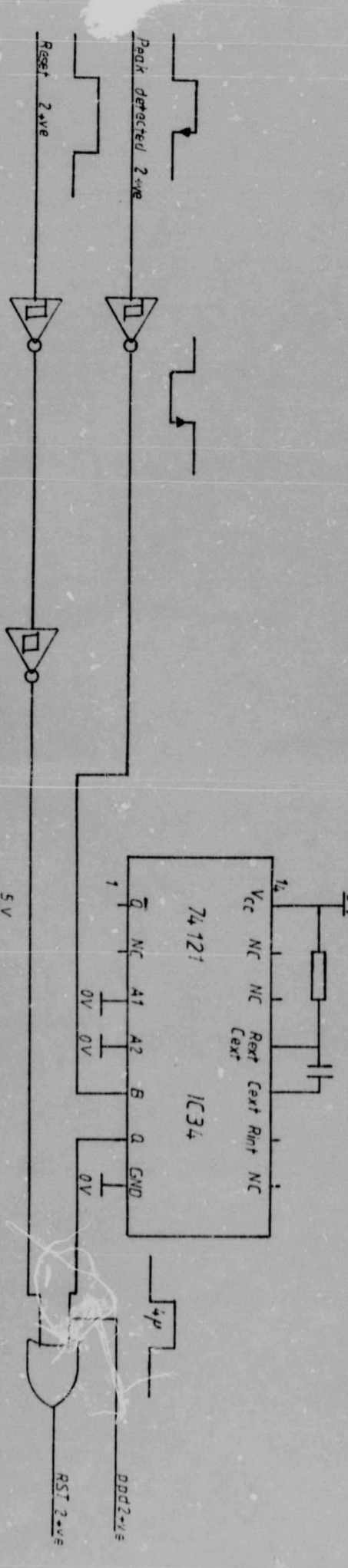
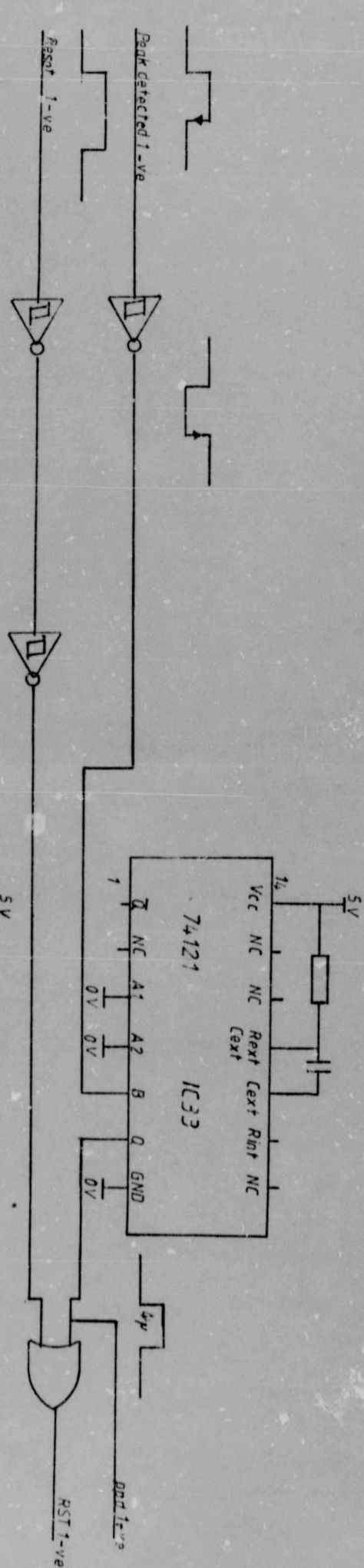
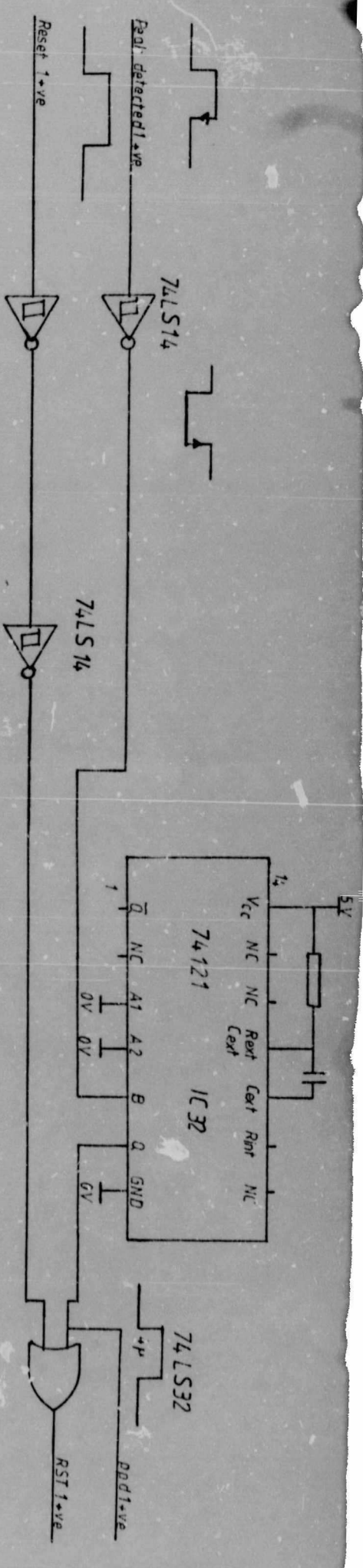


FIGURE A3 SHEET 1 PEAK DETECTOR CIRCUITS









correctable to zero because of the DC coupling, and the drift must be low for the same reason.

The only difference between the amplifiers in each channel is the value of resistance used in the amplification feedback loop. It is only necessary to use a dual amplifier in the times 1000 amplifier, but it was decided to use this configuration throughout because of phaseshift effects caused by the second amplifier. (Other than the 180 degree phaseshift caused by the inverting amplifier configuration) It is essential to minimise the phaseshift effects to allow the timing between signals to be synchronised.

#### 4.2.2 Peak detectors

The circuit is split following the amplifiers between the positive peak detector parts of the circuit and the negative peak detector parts of the circuit. The circuits are identical in topology except that certain components are reversed to allow the processing of positive and negative peaks.

The peak detector consists of an input amplifier and an output buffer (IC4 and IC5) with two peak detecting diodes, one in the negative feedback loop of the input amplifier and the other linking the output of the feedback amplifier to the input of the buffer, and a



hold capacitor between the input of the buffer and ground. There is a reset switch on this hold capacitor which discharges the peak detector once the peak has been sampled by the sample-and-hold, thus allowing the peak detector to detect consecutive peaks, no matter what their values are.

The circuit operates as follows:

The unity gain inverting input amplifier follows the rising edge of the signal. Because it is an inverting amplifier the output is of opposite polarity to the input. While following this rising edge the peak detector diodes are forward biased and hence result in a short circuit. This allows the hold capacitor to be charged, as soon as the signal starts to fall the diodes are reversed biased and appear open circuit. The hold capacitor then has only a very high impedance into which it can discharge and hence it discharges very slowly allowing the peak value to be held.

The switch discharges the capacitor by tying the charge side directly to ground. This switch is open ( high impedance ) when the signal is positive for the positive peak detector and negative for the negative peak detector. Otherwise the switch is closed, and the capacitor shorted to ground.

The peak detector's outputs are passed to a switching circuit which selects the appropriate peak to be processed by the sample-and-hold and analogue-to-digital converter. The peak detector signals are also used to develop the reset and peak detected signals, and this part of the circuitry is buffered from the peak detector.

#### 4.2.3 Reset and peak detected circuitry.

The signal produced by the resonant circuit is complicated and this must be taken into account when designing the reset circuit. The initial peak decays rapidly and the peak value associated with this must be held for long enough to allow the signal to be sampled by the sample-and-hold. The basic operation of the circuit is as follows: the input signal is compared with an attenuated version of the peak detector's output. This operation is shown in Figure A4.

This generates a pulse at the output of the comparator which is used to drive the gate of an analogue switch. This operation ties the hold capacitor to ground at all times except when a peak occurs. This signal is shown in Figure A5.

The peak detector pulse works on the same principle, but the output is less attenuated. This output of the



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