IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 21 February 2024, accepted 3 March 2024, date of publication 11 March 2024, date of current version 18 March 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3375388

RESEARCH ARTICLE

Fundamental Modeling of the Switching Transition in High-Speed Power Electronics

FRANCOIS P. DU TOIT AND IVAN W. HOFSAJER, (Member, IEEE)
School of Electrical and Information Engineering, University of the Witwatersrand, Johannesburg, Johannesburg 2000, South Africa
Corresponding author: Francois P. Du Toit (1270706@students.wits.ac.za)

ABSTRACT Recent advances in semiconductor technology have paved the way for ultra-fast switching capabilities. This increase in switching speed enhances efficiency, power density, and frequency but also increases overvoltage oscillations at the switching node. Existing methods that effectively suppress this overvoltage include slower switching and minimisation of inductance, but unfortunately, these methods become very difficult to implement as the switching speed increases. A new oscillation suppression method, Zero Overvoltage Switching (ZOS), has previously been developed in which the overvoltage is suppressed very effectively by increasing both the switching speed and inductance, contrary to mainstream expectation. This is the only oscillation suppression method that becomes more effective as the switching speed increases and is not constrained by the minimisation of inductance, yet this method has not gained widespread recognition. This is expected because Zero Overvoltage Switching is not explained within the context of existing knowledge, and the argument for implementing it is difficult in the very narrow window where the advantages outweigh the effort. This research develops a generalised fundamental model to better understand Zero Overvoltage Switching by describing the mechanics of fast and slow switching events. The model is also able to provide insights that lead to methods to apply Zero Overvoltage Switching over a broader range of voltages and currents.

INDEX TERMS Wide bandgap (WBG), ultra wide bandgap (UWBG), zero overvoltage switching (ZOS), oscillation suppression methods.

I. INTRODUCTION

Modern wide bandgap (WBG) semiconductor devices offer numerous physical improvements compared to their silicon predecessors, such as higher electron velocity, energy gap, and electric field strength. These characteristics enable them to operate at higher voltages and switch much faster, making them increasingly popular [1], [2], [3].

Faster switching has several advantages, including increased switching frequency, energy density, and efficiency [4], [5], [6], [7]. However, the higher switching speed, represented by higher dv/dt and di/dt, is also responsible for several unwanted oscillations in the circuit [8]. These oscillations are then responsible for several negative consequences, including increased losses, EMI, and component stress, leading to eventual device failure.

Additionally, other characteristics of WBG devices, such as low parasitic capacitance and low on-resistance, can exacerbate these oscillations, presenting a significant hurdle in realising the full potential of WBG technology.

The most prominent type of oscillation that is caused by the fast switching transition is the overvoltage and ringing of the switching node, where the switching node (SN) is the node where the inductor is connected to the switch. An example of the switching node can be seen in the equivalent circuit of a boost converter below in Fig. 1:

In this figure, the parasitic inductance and capacitance components can be seen as well. When the switch in Fig. 1 has been turned on for a long time and then turns off, the simplified plots for the current and voltage during a slow

The associate editor coordinating the review of this manuscript and approving it for publication was Fengjiang Wu.

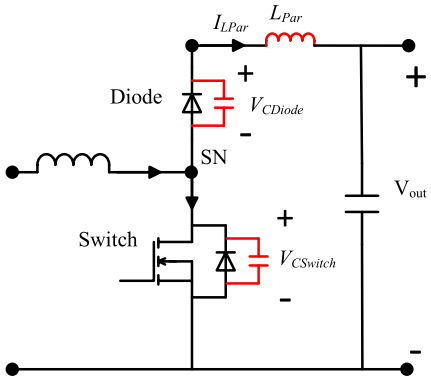

FIGURE 1. Boost converter equivalent circuit with parasitic components.

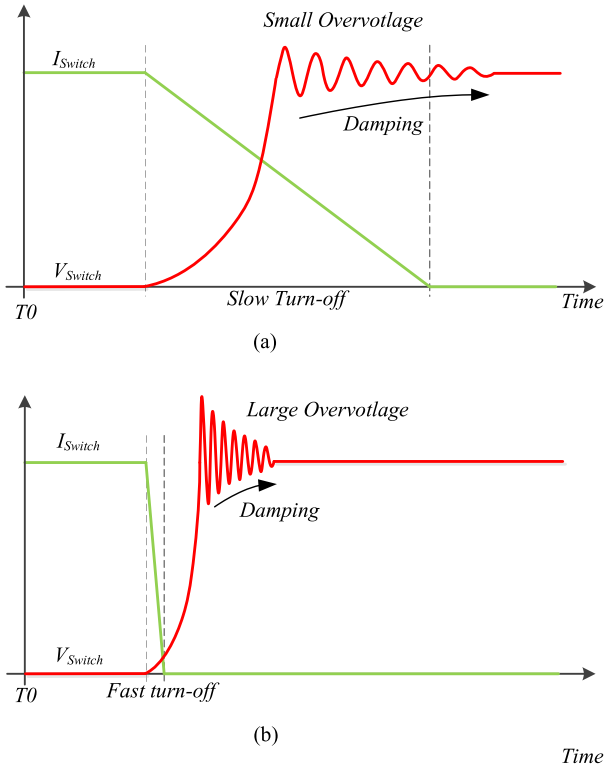

FIGURE 2. Comparison of the voltage overshoot of the switching node when switching (a) Slow and (b) Fast.

turn-off and a fast turn-off switching transition can be seen in Fig. 2.

It can be seen that a voltage oscillation is created on the switching node during the transition, and the faster the turn-off transition of the switch, the larger the voltage overshoot will be. The equivalent circuit resistance will eventually dampen this oscillation.

This overshoot and ringing oscillation of the switching node is caused by the resonance between the parasitic components that are first seen in red in Fig. 1. The fast switching causes these parasitic components to become excited, and the more excited the components are, the larger the overshoot will be. After the switching transition has been completed, the circuit from Fig. 1 will progress to a simplified equivalent

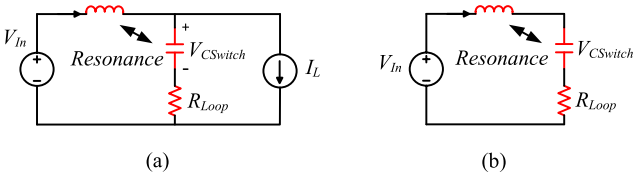

FIGURE 3. Equivalent circuits of the resonance between parasitic components that cause voltage overshoot in the (a) turn-off and (b) turn-on transition.

circuit that is different for the turn-on and turn-off transitions, as can be seen in Fig. 3.

The figure shows the resonance between the parasitic components, and the equivalent resistance eventually damps out the resonance oscillation.

This resonance during the switching event has been a problem in the field of power electronics almost since its inception, and over this time, several different effective methods have emerged to suppress this phenomenon. Even though these solutions have different approaches, in the end, they all address the same resonance problem. Generally, these methods fall into one of the following categories: minimisation of parasitic inductance, switching slower, ferrite beads, Active Gate Drivers (AGD) and RC snubbers, and they are discussed in more detail in Section II.

All of these existing oscillation suppression methods represent improvements based on well-established concepts and extensive research. These interdependent approaches form a comprehensive collection of knowledge, lending credibility to their individual effectiveness.

It is known that materials are the main driver in transistor development, and Ultra Wide Bandgap (UWBG, Eg $>$ 3.4 eV) devices are on the horizon. As semiconductor materials' switching performance parameters increase significantly as the energy gap of a material increases, the rise in energy gap from WBG devices (GaN – 3.4 eV) to UWBG devices (AlGaN 6.2 eV) is expected to enhance switching speed capabilities significantly [9].

Despite being able to accommodate the current switching speed of WBG devices while effectively suppressing oscillations, current solutions become much more challenging to implement effectively as the switching speed increases.

A. ZERO OVERVOLTAGE SWITCHING AS AN OSCILLATION SUPPRESSION METHOD

A new oscillation suppression method, known as "Zero Overvoltage Switching" (ZOS), has recently been described [10]. This solution challenges mainstream assumptions and represents a departure from the two primary approaches of decreasing switching speed and decreasing inductance. Instead, ZOS simultaneously increases switching speed and inductance, leading to surprising and unexpected results, as illustrated in Fig. 4.

Fig. 4 shows the transition period is very small, with no overshoot and ringing, contrary to the expected results. These results were experimentally verified in [11] and [12].

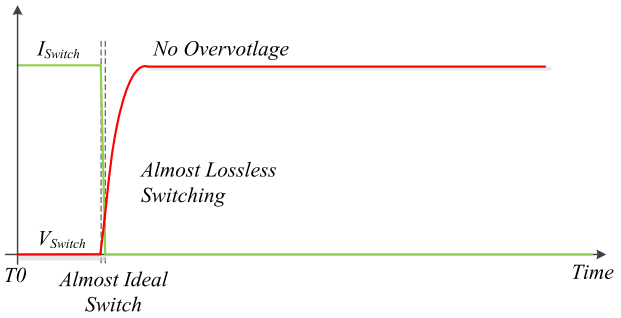

FIGURE 4. Voltage overshoot of optimised ZOS.

When compared to the other suppression methods, this method becomes more effective as the switching speed increases and not less effective as the others do. This approach is also not limited by the physical constraints to minimise the inductance to achieve optimal results, which suggests that this approach holds promise as an effective suppression method.

Despite this potential, ZOS has not gained widespread recognition, as there has not been much work in this area.

It is expected that ZOS has not lived up to its mainstream potential thus far for two main reasons. The first is that ZOS is only possible in a very narrow window, and a small deviation of any of the circuit parameters from the optimal values creates a very large overshoot, making the argument for implementing ZOS difficult.

The second expected reason is the disconnect between the existing, accepted body of knowledge and the theory behind ZOS, as the two are not discussed together. An example of this can be seen specifically in [8] and [13]. These two papers provide a thorough and very deep review of the current position of oscillation suppression methods, fast switching in general, and even future trends, but ZOS is not mentioned.

Additionally, [14] presented the same results as [10] very recently as an optimization strategy but does not refer to it as ZOS, nor does it reference any papers referring to ZOS. This also demonstrates that ZOS is not known to the broader power electronics community.

However, this research aims to bridge these two issues mentioned above by developing a fundamental model that contextualises ZOS within conventional switching assumptions and explores its implications for very fast switching. This model is then able to provide a framework of the fundamental mechanisms and effects of very fast switching so that it can be understood.

This understanding then paves the way for methods to achieve ZOS at non-ideal and realistic switching speeds, as well as broadening the window period of ZOS so that it can be utilised over a larger design range.

This paper is not meant to be a design guide but, rather, a pathway to build upon and provide a fundamental contribution to the work that has already been done in ZOS and fast switching in general. The insights and principles produced by the model in this research are meant to assist the designer in the initial decision-making process when the converter is conceptualised. The model can then inform the designer of the influences that the target parasitic values and switching speed have on the overshoot before experimental results are produced.

The main contributions of this paper are:

- A mathematical model that is able to describe the switching event and is then able to simultaneously explain the results of very fast switching and slow switching.
- An approach that can provide preliminary insights into the switching behaviour of a circuit.
- Insights on the use and application of existing oscillation suppression methods when switching very fast.
- Potential oscillation suppression methods when switching very fast but with a non-ideal switching transition.

The layout of the paper is as follows:

Section II reviews and compares the existing oscillation suppression methods with a focus on methods used for WBG devices. A summary table is presented with high-level advantages and disadvantages for each method.

Section III explains how the actual fundamental model was derived, and alternative equivalent circuit progressions are presented and named *Fast-Mode* and *Slow-Mode*. A discussion is presented on how to apply some of the derived equations to determine the anticipated overshoot of a switching circuit.

Section IV delves into an energy transfer representation through the switching transition and discusses how the energy transfer between the parasitic components can have varying levels of effectiveness, which causes the overshoot and ringing. From this approach, alternative prerequisites for ideal energy transfer are discussed and proposed.

Section V then uses insights from the mathematical model to discuss the implications of when existing oscillation suppression methods are implemented when switching in *Fast-Mode* circuit progressions and which methods will still be relevant.

Section VI then discusses alternative oscillation suppression methods that can be used in *Fast-Mode* to achieve energy balance through the switching transition and their trade-offs.

Section VII discusses the implications of this research on the field of power electronics in general.

Section VII provides the conclusion of the paper.

II. EXISTING OSCILLATION SUPPRESSION METHODS

As discussed above, several accepted oscillation suppression methods already exist to solve the very old problem. These solutions form a well-rounded collection of knowledge and are discussed in this section.

A. MINIMISATION OF PARASITIC INDUCTANCE

The primary cause of overvoltage is the resonance between the parasitic electromagnetic components. When the image in Fig. 3 above is considered, it can be seen that reducing parasitic inductance also reduces the overvoltage.

Minimising parasitic inductance is an obvious and very effective approach and can be achieved mainly in three ways.

TABLE 1. Oscillation suppression methods comparison.

Oscillation Suppression Method	Application	Advantages	Disadvantages	References
Minimisation of parasitic inductance	• Reduction of power loop inductance by: o Power loop layout optimisation o Packaging optimisation o Component selection	• Very Effective • Easy to understand • Component selection is straightforward to implement	• Layout optimisation can become very complicated • The parasitic inductance can never be reduced to zero.	[15], [16], [13], [17], [18], [19], [20], [21], [22]
Slower switching	• A resistor on the gate terminal or slower slew rate of the gate driver	• straightforward to implement	• Not very effective in reducing oscillations • Increase in switching losses	[23], [24]
Ferrite Beads	• Adding a high-frequency dependent resistor	• Simple to implement • cost-effective • passive	• Much better at decreasing oscillation duration than a reduction of maximum voltage • Slightly increased losses	[23], [24], [25]
Active Gate Driver	• Control voltage, current or impedance of the gate terminal of the semiconductor device	• Several papers have been very effective • Very flexible solution	• It can become extremely complex • Higher cost of more components	[26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41]
RC Snubbers	• Adding circuit components to create a critically damped system at the ringing frequency	• Simple to implement • cost-effective • passive • High-order can be very effective	• Lower order has minimal oscillation suppression • Slightly increased losses • Higher order can be complicated to calculate and design	[25], [42], [43], [44], [45], [46], [47], [48], [49], [50]
Zero Overvolatge Switching	• Increase switching speed and inductance according to the optimisation equation.	• The only method that can become better when switching faster	• A very narrow window of operation • A small change in current or voltage creates a large overshoot • This is only possible at very high switching speeds	[10], [11]

The first is device selection. This is an easy approach to simply select a switching device that has the lowest parasitic inductance and this can be read from the datasheet [15], [16].

Second is the layout optimisation to reduce the power loop inductance, which can be achieved by many innovative approaches. Generally, the circuit is optimised by minimising the footprint and by creating lateral power loops, vertical power loops, or optimisation between the two. This approach has reported results of less than 1 nH [13], [17], [18], [19].

And lastly is the approach to optimise the device packaging. In this approach, only the die of the switching device is used, and the package in which the die is placed is designed and implemented. This method has also reported results of less than 1 nH parasitic inductance in experimental results [20], [21], [22].

However, even with a combination of all the approaches mentioned above, the parasitic inductance can only be decreased so much, and further improvements become challenging, especially as *dv/dt* and *di/dt* increase.

B. SLOWER SWITCHING

Lowering the *dv/dt* and *di/dt* by using a gate resistor or implementing a driver that can switch slower can suppress the excitation of parasitic components and increase the stability of the switching event. This is illustrated in Fig. 2, where the overshoot is lower for a slower switching event than for a faster switching event. However, this method leads to increased switching losses [23], [24].

C. FERRITE BEADS

Adding Ferrite beads to the circuit provides a frequency-dependent resistor that can dampen high-frequency oscillations while allowing DC to pass. This method is more

effective in reducing the oscillation duration than the peak but slightly increases conduction losses [23], [24], [25].

D. ACTIVE GATE DRIVER

An Active Gate Driver (AGD) refers to an umbrella term where a specific focus is placed on the gate driving circuit instead of the power loop circuit. With AGDs, the gate driver circuit can adapt the gate voltage, current, or impedance using an auxiliary circuit. The aim of how the switching device is turned on or off can vary greatly, but several different approaches have been effective in reducing the eventual voltage overshoot and ringing.

This research is claimed to be a "research hot-spot" and aims to control the *dv/dt* and *di/dt* of the switch to mitigate overvoltage and ringing [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], crosstalk [38], [39], [40], [41] or false triggering [51]. However, implementing an effective gate driver circuit to suppress overshoot without compromising efficiency becomes highly complex and costly.

E. RC SNUBBERS

Adding an RC snubber is an effective method to suppress switching oscillations, which has been used in power electronics almost since the inception of the research field. This approach involves modelling a simplified RLC circuit for the turn-on and turn-off equivalent circuit and adding an RC bridge to dampen the oscillation, as shown in Fig. 5.

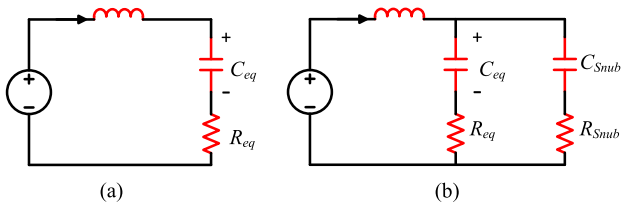

FIGURE 5. Equivalent circuits of a switching node without (a) and with (b) a snubber circuit.

The values of C_{snub} and R_{snub} can be calculated to create a critically damped system at the ringing frequency. Generally, this approach can be categorised into second-, third-, and high-order designs. The second-order design, based on the simplified model, is relatively easy to implement but has limited suppression effects and slightly increased losses [25], [42], [43]. The third-order design involves a more complex circuit to account for additional parasitic parameters and determines the values of R and C using the root locus method of stability. It offers good suppression effects but comes with a slightly more complex design and slightly increased switching losses [44]. High-order design, while more complex and difficult to solve, has similar drawbacks of slightly increased switching losses and complexity but can offer better suppression and stability than lower-order design [45], [46], [47], [48], [49].

In [50], a C-RC snubber is introduced. The calculation for the component values is complicated but effective in the ability to suppress the voltage overshoot.

III. REALISATION OF FUNDAMENTAL MODEL

A single model that is able to explain the results of ZOS and conventional expected results simultaneously is required to bring the two branches together. To achieve this, the switching node of a boost converter is investigated. This node of a boost converter is chosen as it is where the overshoot phenomenon is a major concern, and this node is applicable to other commonly used converter types, like synchronous buck converters. The equivalent circuit is seen in Fig. 1 above.

Several assumptions must be made to the circuit to be able to model the switching transition effectively. The first is the consideration of the intent of the model, which is to investigate the effect of both the parasitic components and the turn-off speed of the switch on the overshoot of the switching node votlage. Thus, the lumped circuit parasitic components and turn off of the switch are modelled explicitly. The turn-off of the switch is modelled by replacing the switch with a decaying current source from I_{in} to zero.

Additionally, the assumption is made that the size of the input inductor and output capacitor is very large compared to the parasitic components and the time period of the investigation is very small, so the input inductor and output capacitor are replaced with a current source and voltage source, respectively. The circuit from Fig. 1 can then be converted into Fig. 6.

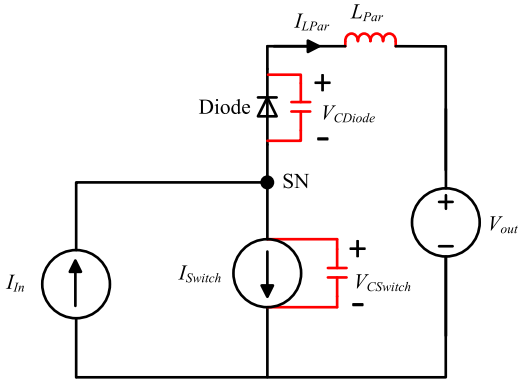

FIGURE 6. Modified Equivalent circuit of a boost converter switching node.

In this circuit, the turn-off current of the switch is assumed to be linear, and the turn-off period can be adjusted as required to model the opening of the switch. An equation that satisfies these requirements can be seen below:

$$I_{Switch}(t) = I_{in} - \frac{I_{in}}{T_{Fall}}(t) \tag{1}$$

In this equation, T_{Fall} refers to the time required for the current through the switch to reach zero and thus is also the current transition period. The assumption that the current through the switch decays linearly is made to show underlying fundamental dynamics without clouding them with the higher-order effects of different semiconductor switching models.

This circuit can be seen to have six degrees of freedom, or variables that can be chosen by the designer, and it must

be noted that the introduction of each additional degree of freedom greatly increases the complexity of the model. These variables are:

1) I_{in} – – Input Current
2) V_{out} – Output Voltage
3) T_{Fall} – Time taken for the switch to turn off fully
4) C_{Diode} – Parasitic Capacitance of Diode
5) C_{Switch} – Parasitic Capacitance of Switch
6) L_{Par} – Cumulative Parasitic Inductance of Power Loop

Together, these variables form a circuit environment, and all the subsequent waveforms are interdependent on all of these variables. The equivalent resistance is not considered at this stage due to the complexity of the model and does not have a big influence on the overshoot magnitude.

To analyse this circuit in Fig. 6, a conventional approach of circuit analysis using Kirchoff's current and voltage laws is used to determine the time domain equations. The Laplace transforms are then used to solve the variables of $V_{Switch}(t)$, $V_{Diode}(t)$ and $I_{LPar}(t)$ and then converted back to the time domain using inverse Laplace transforms. This analysis starts when the switch starts to turn off.

As the voltage and current progress through the time domain, it is seen that the equivalent circuit that is relevant to the specific time period will change. The two events that will change the equivalent circuit and their effects are:

1) Clamping of the diode – As the diode becomes forward-biased, C_{Diode} will be short-circuited and can be ignored in the circuit analysis after the event.
2) The switch turns off fully – when the current through the switch reaches zero, the current source representing the switch becomes an open circuit and can also be removed from the equivalent circuit.

The values at the end of a specific period are then used as the initial conditions for solving the variables in the following period. The math becomes very complicated as the equivalent circuits progress, and the full mathematical results can be seen in the appendix.

The results of this approach can be seen in Fig. 7 below. From the investigation, it is seen that, depending on the combination of choices of the variables mentioned above, either the diode can clamp first or the switch can fully turn off first. This means that depending on the variables, different equivalent circuit progressions will be followed.

The alternative circuit progressions from Period 1 (P1) to Period 3 (P3) are named *Slow-Mode* and *Fast-Mode* circuit progressions for simplicity.

In *Slow-Mode* circuit progressions, the diode clamps before the switch is fully turned off, and this progression is the equivalent circuit progression of mainstream conventional switching.

In *Fast-Mode* circuit progressions, the switch fully turns off and becomes an open circuit before the diode clamps. This is only possible in very fast switching transitions and is the circuit progression when ZOS is presented. A comparison of the switching events of a slow switching event of *Slow-Mode*

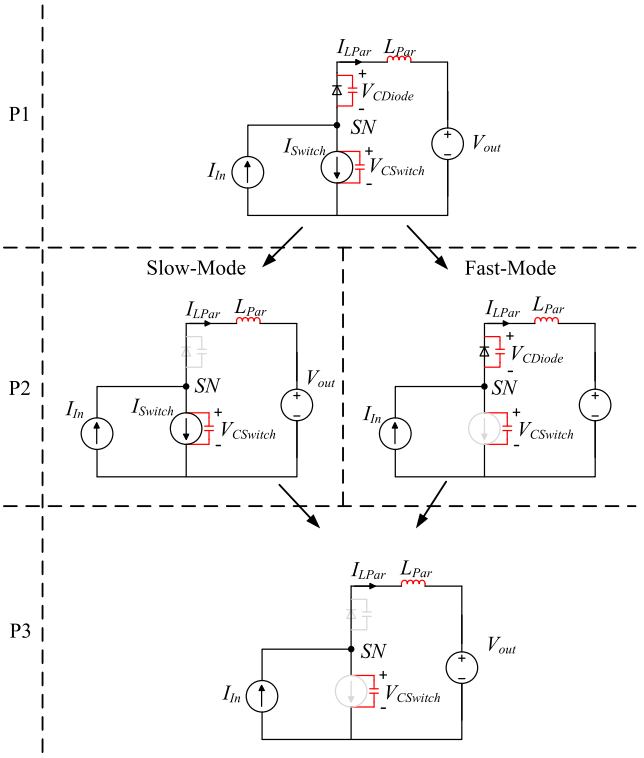

FIGURE 7. Alternative equivalent circuit progression for Slow-Mode and Fast-Mode.

and a very fast switching event of *Fast-Mode* can be seen in Fig. 8 and Fig. 9, respectively.

In these comparisons, it can be seen that the voltage overshoot oscillation will occur when the diode clamps and this happens at different time periods for *Slow-Mode* and *Fast-Mode*.

For *Slow-Mode*, the voltage overshoot will occur in Period 2 (P2), and for *Fast-Mode*, the overshoot will occur in Period 3 (P3). This means that the voltage rise of the switching node is not directly dependent on the turn-off time of the switch but rather dependent on the time it takes for the diode to clamp.

It must be noted that the time it takes for the diode to clamp ($V_{Diode}(t)$ to reach zero) naturally occurs and is a secondary effect of the choice of parasitic components and the turn-off time of the switch, but it is a very important occurrence in the progression. This point in time is referred to as T_{Clamp}.

This overshoot oscillation will be dampened if equivalent resistance is included in the model.

When the turn-off period T_{Fall} (Current switching period) is plotted against the maximum overshoot of a circuit on a logarithmic scale with the same parasitic components as used for the plots in Fig. 8 and Fig. 9, the plot can be seen in Fig. 10.

In Fig. 10, itSlow-Mode on the right-hand side of the plot is an example of conventional switching. In this part of the plot, it is seen that the overshoot decreases as the switching period increases, which is according to mainstream expectations. An example of the waveform of slow switching is seen above in Fig 8. time for the diode to clamp, and this section

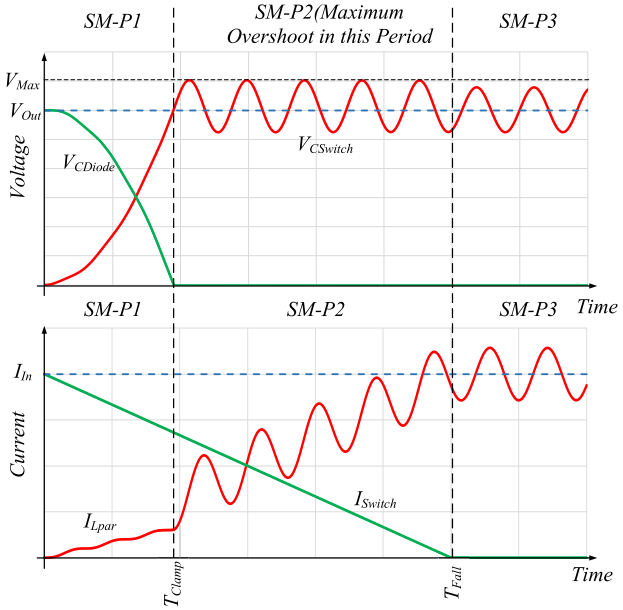

FIGURE 8. Slow-Mode circuit progression waveforms of voltage and current.

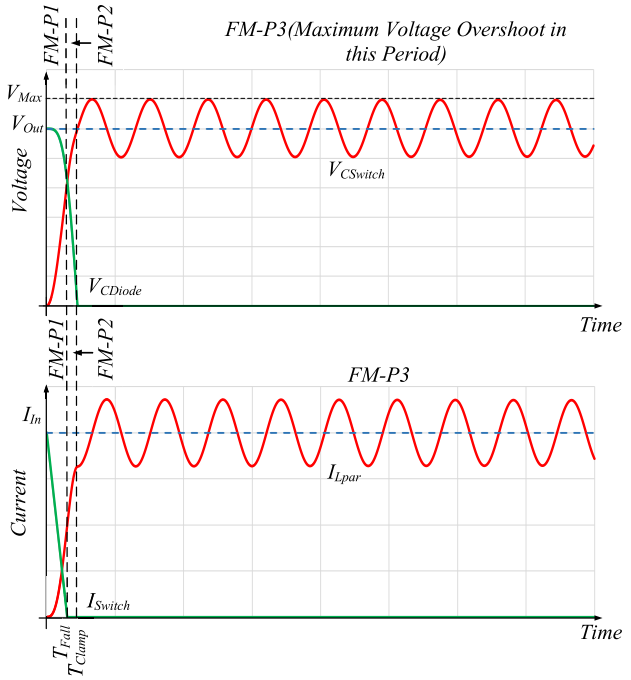

FIGURE 9. Fast-Mode circuit progression waveforms of voltage and current.

generally accounts for the largest overshoot of the entire plot. An example can be seen in Fig. 11:

The left-hand side of the plot in Fig. 10 shows when the circuit is operating in *Fast-Mode*. It can be seen that the overshoot drastically decreases, and this decrease in voltage is against mainstream expectations.

The transition between *Slow-Mode* and *Fast-Mode* will occur when the turn-off time of the switch is equal to the time

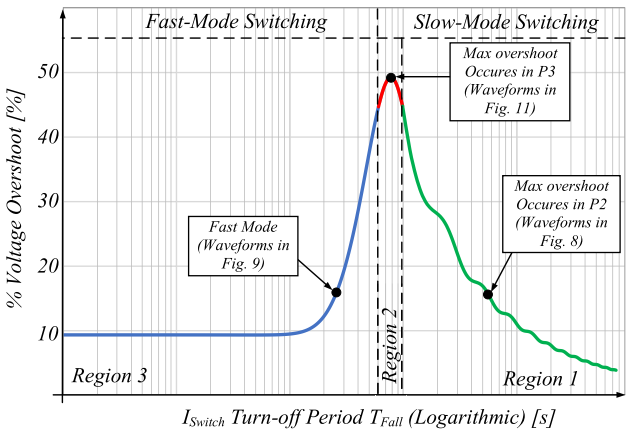

FIGURE 10. Voltage Overshoot Percentage vs. Turn-off period of switch.

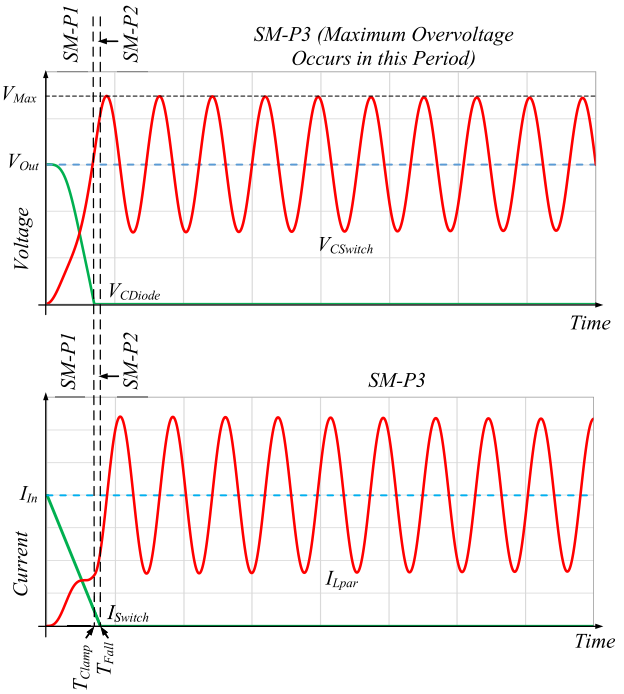

FIGURE 11. Slow-Mode maximum voltage overs hoot waveform.

the diode takes to clamp, or described mathematically below:

$$V_{Diode}\,(T_{Fall}) = 0 \tag{2}$$

This point in time is dependent on all six of the variables described above. This makes this point difficult to derive mathematically, so the roots of the function are solved analytically when all the variables are available.

It is important to note that this transition point between *Slow-Mode* and *Fast-Mode* exists for all combinations and ratios of positive values of the parasitic components. This means that eventually, and independent of the oscillation suppression method that is applied, all switching events will reach the transition point if the speed increases enough. Therefore, given that the switching speed of devices is increasing, a better understanding of *Fast-Mode* is required.

Specifically, it is to fundamentally understand how the circuit parameters and switching speed translate to the overshoot.

These overshoot results of *Fast-Mode* are expected and are also experimentally verified in both [11] and [12]. This difference between the overshoot expectations of *Slow-Mode* and *Fast-Mode* is fundamentally because of the alternative circuit progression, the different circuit conditions, and different stored energy values in the parasitic components when the overshoot occurs.

1) MODEL APPLICATION DISCUSSION

The resulting plot presented in Fig. 10 is a very good preliminary design tool that is able to predict the switching performance of a circuit with the chosen parameters of the designer long before the circuit has been built. The plot will be able to assist with decisions of switching speed or parasitic inductance and the trade-off thereof.

When the six circuit variables mentioned above have been estimated or chosen, the designer can slot the variables into the model equations presented in the appendix, and with the help of mathematical software, some important predictions of the circuit can be calculated.

The first step must always be to calculate if the chosen parameters would have the circuit operating in *Slow-Mode* or *Fast-Mode* to know which set of equations is applicable. This can be done by calculating the time taken for the diode to clamp (T_{Clamp}) under the chosen variables by calculating the roots of (2) using (13) in the appendix.

It is advised that the design must ensure that the switch turn-off time (T_{Fall}) is much faster or slower than the calculated (T_{Clamp}), as this is the largest predictor of the overshoot.

Once T_{Clamp} has been calculated and the determination is made if the set of *Slow-Mode* or *Fast-Mode* equations must be used, the overshoot can be calculated.

When operating in *Slow-Mode*, the variables can be plugged into (16), and the maximum value of the oscillation can be calculated. When operating in *Fast-Mode*, the variables must be plugged in (9). It must be noted that the value of T_{Clamp} must be recalculated if any variable is adjusted.

A similar graph to the one presented in Fig. 10 can be reproduced if desired, and all the model equations can be found in the appendix.

IV. THE UNDERLYING MECHANISM OF THE VOLTAGE OVERSHOOT

When the entire switching transition is considered, including the time before the switching transition and a long time after the switching transition, the waveforms below in Fig. 12 will be applicable in a fast-switching event for a circuit with damping in *Fast-Mode*.

When the period before the switch is considered, P0, it can be seen that the switch has been closed for a long time, and there are no oscillations. P4 is after the switch has been open for a long time and all the oscillations and resonance have been damped out.

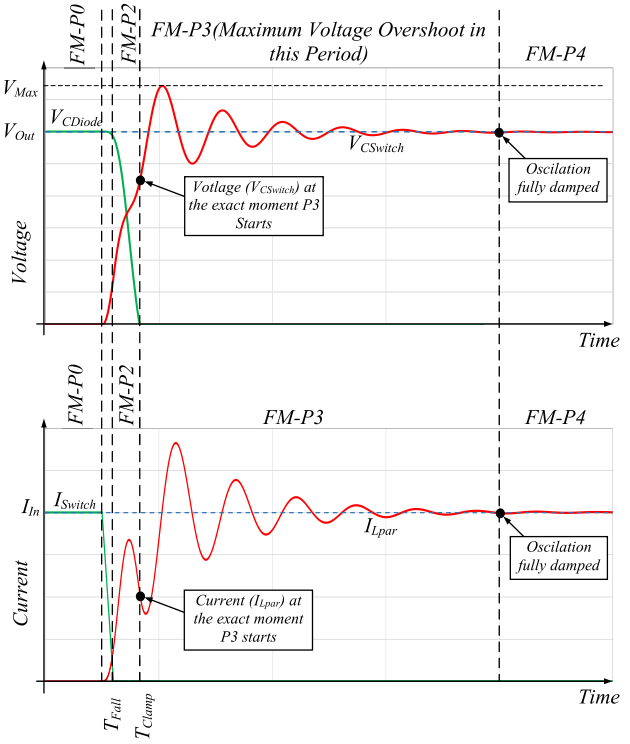

FIGURE 12. Typical Fast-Mode switching transition with damping.

The equivalent circuit transition from P0 to P4 with an emphasis on energy storage of the reactive components can be seen below in Fig. 13.

It can be seen that in P0, only C_{Diode} is storing the energy of the full value of V_{Out}. In P4, C_{Diode} has been short-circuited by the diode, and there is only energy stored in C_{Switch} and L_{Par}.

The investigation into the switching transition can, in essence, be seen as an attempt to effectively manage the process to get the energy stored in the passive components from P0 to P4 as well as possible, where what happens in P1 to P3 can be manipulated.

As the equivalent circuit progressions of *Slow-Mode* and *Fast-Mode* are different, the underlying mechanism of the overshoot and energy transition requirements are also different. These differences are investigated separately below.

A. EFFECTIVE ENERGY TRANSFER FOR IN FAST MODE

When the overshoot of *Fast-Mode* is considered with the relevant equivalent circuit, it can be seen that the overshoot oscillation starts when the diode clamps and the equivalent circuit progresses to a resonance circuit, which can be seen in P3.

When the resonance circuit is considered in isolation, as seen in Fig. 14, it is known that the amplitude of the resonance in a circuit is determined by the initial conditions of the period if the other circuit parameters are fixed.

This then means that if the initial conditions of P3 are such that the voltage over the capacitor is equal to V_{Out}, and the

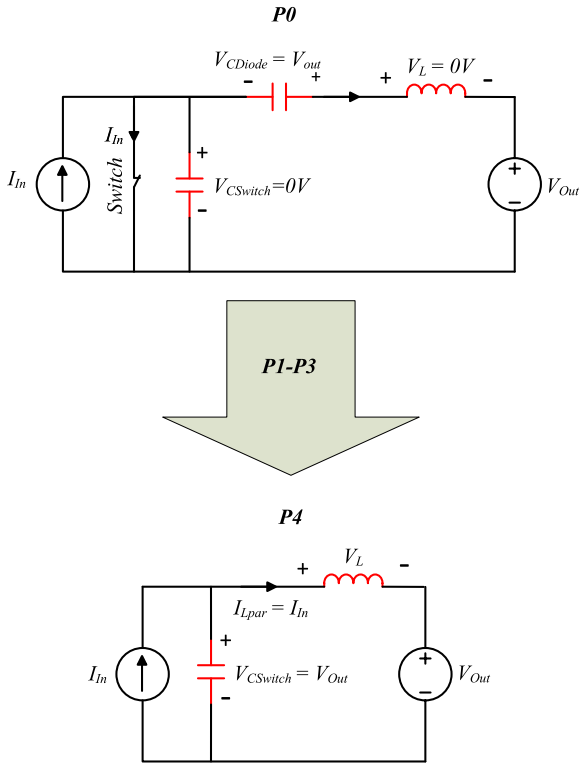

FIGURE 13. Equivalent circuit From P0 to P4 Highlighting energy storage of reactive components.

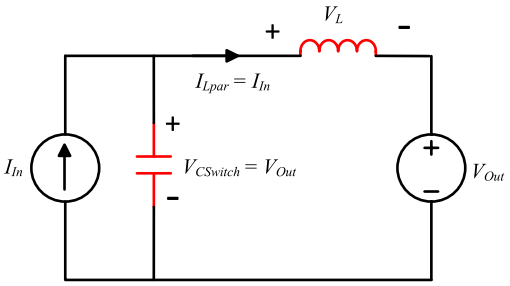

FIGURE 14. Equivalent circuit of oscillation circuit of P3.

current through the inductor is equal to I_{in}, at the exact time the diode clamps, no overshoot will happen. In essence, this means that the energy stored in both C_{Switch} and L_{Par} must be the same as the energy stored in the components in P4 (after oscillation) for no overshoot to occur.

If the assumption is made that the switching period is infinitely small and that the capacitors are equal, the conditions for the optimal energy transfer described above can be derived from the model, and the resulting equation can be seen:

$$I_{in} = V_{Out} - \frac{\sqrt{8\frac{C_{Par}}{L_{Par}}}}{(2n-1)\pi} \tag{3}$$

For this equation to hold, the values of C_{Switch} and C_{Diode} must be the same and is equal to C_{Switch}. The value of n can be any integer larger than one and indicates the optimized point of operation will occur again when one of the variables changes. This equation is similar to those presented in [11] and [12], and when this equation is applied to the parameters of the overshoot plot in Fig. 10 above, with the choice of inductance as the variable, the following plot of Overshoot vs Switching speed can be seen in Fig. 15.

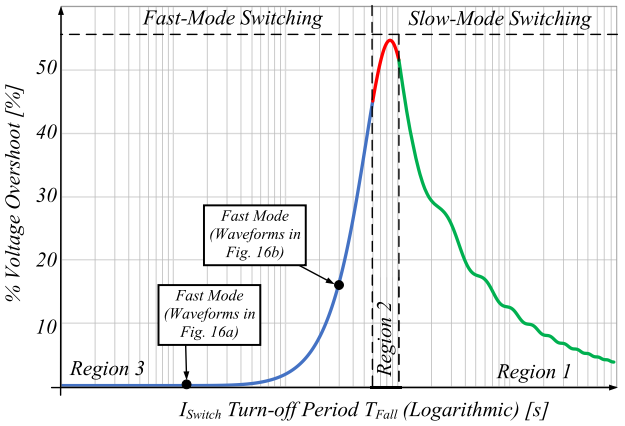

FIGURE 15. Voltage Overshoot vs Switching Speed when Optimisation equation is applied.

When two of the switching waveforms of the different points of operation from the graph above are investigated, the comparison of an ideal and ineffective energy transfer switching event can be seen in Fig. 16.

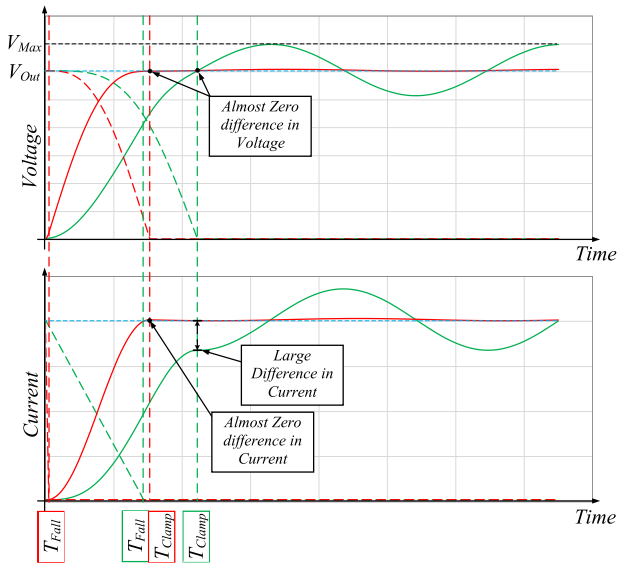

FIGURE 16. Fast-mode comparison of switching node waveforms for optimal energy transfer vs. non-optimal energy transfer.

From these waveforms, it can be seen that the mismatch in energy between the initial conditions of P3 and the required energy conditions of P4 produces the voltage overshoot, and the larger the mismatch, the larger the overshoot will be. As the inductance value is much larger than the capacitance value, the energy mismatch caused by a mismatch in the current of the inductor is punished much more severely than the energy mismatch in the voltage of the capacitor.

1) OPTIMISATION FOR NON-IDEAL SWITCH

An important addition is that this described optimal energy transfer can also be achieved when the turn-off period is not ideal and when the capacitors do not match, but as stated above, the introduction of two more degrees of freedom also introduces very high complexity to the model. Thus, this point of operation also cannot be mathematically derived due to the interdependencies of the variables, but a numerical method of calculation is able to find the combination of parameters that can display this optimised point.

In this numerical method, a solution only exists if all the values are chosen except for the capacitance values. This indicates that the relationship between the capacitance values is also a very important ratio.

Fig. 17 shows the plot comparing the voltage overshoot and the turn-off period of the optimised points for the non-ideal switching transition. These points of operation are found when optimising for three different turn-off periods while keeping the inductance the same as in the plot above and finding the correct capacitance values.

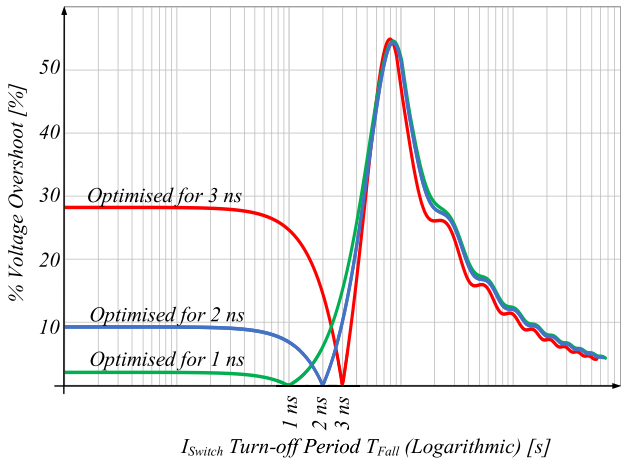

FIGURE 17. Overshoot vs. switching speed when optimised for non-ideal switching event.

In this plot, it can be seen that the longer the turn-off period is optimised for, the greater the overshoot sacrifice is when not switching at exactly this point.

Additionally, the longer the turn-off period point of optimisation, the greater the ratio between the diode and switch capacitor has to be.

B. EFFECTIVE ENERGY MANIPULATION FOR SLOW MODE

When a similar approach is followed for *Slow-Mode*, it is seen that the voltage overshoot happens at the start of P2 and when the diode clamps, but not in P3, like in *Fast-Mode*. This means that the equivalent circuit in Fig. 18 will be applicable when the voltage oscillation starts.

In this circuit, the switch is not yet fully turned off when the oscillation starts, so the energy stored in L_{Par} cannot be the same as in P4. To be able to determine the initial conditions of P2 that the $I_{LPar}(t)$ is supposed to be for no oscillation,

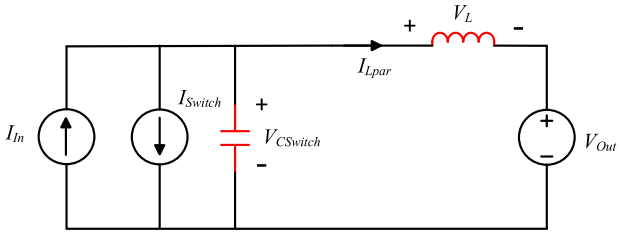

FIGURE 18. Equivalent circuit of Slow-Mode, P2.

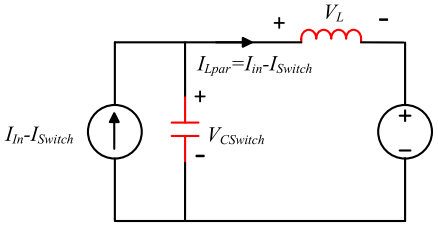

FIGURE 19. Equivalent circuit of Slow-Mode, P2, simplified.

the circuit is simplified. The input current and switch current are combined for a similar circuit, as seen in P3.

This means that for no overshoot to occur, the voltage over the capacitor must be equal to V_{Out}, and the current through the inductor must be $I_{in} - I_{Switch}(t)$ at the exact moment the diode clamps, and the oscillation is supposed to start.

An example can be seen in the waveform comparison below in Fig. 20, where the inductance is lowered.

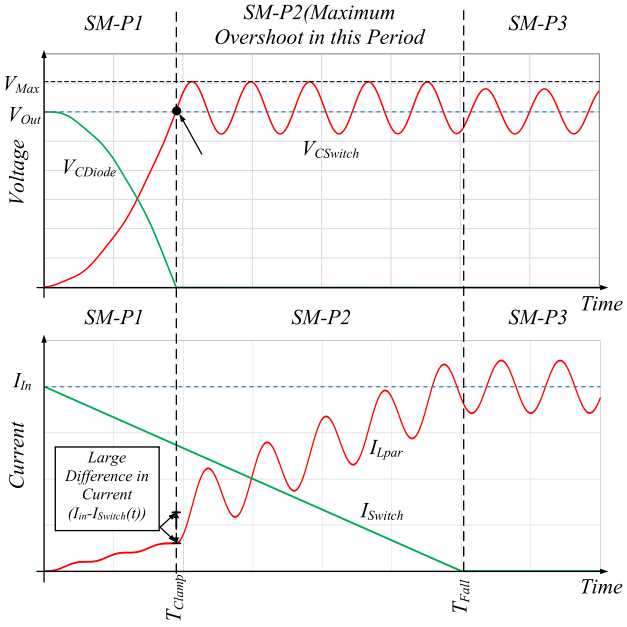

FIGURE 20. Slow-Mode switching node waveforms for non-optimal energy transfer.

It is seen that the smaller the mismatch in current or the smaller the energy mismatch, the smaller the voltage overshoot will be.

From the energy mismatch approach, the inductor current must then be as close as possible to the calculated point when

the diode clamps, and this can be done relatively easily in two ways.

The first is to increase the slope of the inductor current in P1, which can be done by decreasing the inductance as much as possible, and the second is to make P1 longer, which can be done by switching slower.

Decreasing the inductance or decreasing the switching speed are the two most known methods of decreasing the voltage overshoot, which shows that mainstream attempts to minimise overshoot are just a secondary consequence of lowering the energy mismatch at the start of P2.

Unfortunately, the equation can only be satisfied if there is no inductance in the circuit, which in turn means that perfect optimal energy transfer in *Slow-Mode* switching is not possible as the inductance cannot be reduced to zero.

V. APPLICATION OF *SLOW-MODE* OSCILLATION SUPPRESSION METHODS IN *FAST-MODE* SWITCHING

As discussed in Section I, several existing methods have successfully managed and minimised the overshoot when switching to conventional *Slow-Mode*. But as discussed in Section II, all fast-switching devices will eventually transition into *Fast-Mode*, and the equivalent circuit progression and the mechanism underlying the overshoot are different. This means that the mainstream oscillation suppression methods might not be applicable in *Fast-Mode* switching.

This section will re-evaluate the oscillation suppression methods mentioned in Section I to determine if they are still applicable to *Fast-Mode* switching.

A. MINIMISATION OF PARASITIC INDUCTANCE

From the experimental results presented in [10], it is already known that the assumption that lowering the parasitic inductance will lower the overshoot is not true in *Fast-Mode*. To further demonstrate this, a similar graph to that of Fig. 5 is presented, where the circuit model is used to determine the overshoot versus the fall time. In this figure, four inductance values are chosen: 1.) Very low 2.) low 3.) High and 4.) very high.

In the plot, the dot refers to the point where each plot transitions between *Slow-Mode* and *Fast-Mode*. The graph shows that the overshoot increases as the inductance increases, as expected in conventional *Slow-Mode* but not in *Fast-Mode*. When switching to *Fast-Mode*, the goal of minimisation of parasitic inductance must be shifted to that of an optimal energy transition and not minimisation.

When the limitation of minimisation of inductance does not constrain the layout and packaging of a device, more emphasis can be given to other parameters, such as cooling or even just switching speed.

B. SWITCHING SLOWER

As stated in Section II, switching slower while operating in *Fast-Mode* will lead to a large voltage overshoot long before the transition is made to *Slow-Mode*, and the overshoot starts to decrease. This means that Slower switching is not an effective oscillation suppression method in *Fast-Mode*.

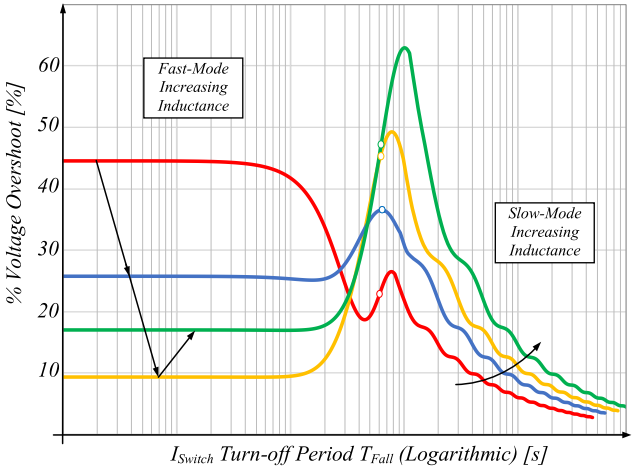

FIGURE 21. Voltage overshoot vs switching speed of four increasing inductance values.

C. FERRITE BEADS

As ferrite beads do not influence the circuit environment of the switch and only provide a high-frequency dependent resistor, this method will still be applicable in *Fast-Mode* switching.

D. ACTIVE GATE DRIVER

As an AGD can actively adapt the gate driver and, in so doing, actively shape the turn-off waveform of the switching current, it is expected that Active Gate Drivers will remain a research sweet spot with *Fast-Mode* and *Slow-Mode*.

When the goal of the AGD is changed to optimal energy transfer, the driver will be able to adapt the turn-off waveform in such a way as to have the correct energy at the required point in time. The successful application of an AGD will then be able to achieve energy balance over a range of inductor currents, shaping the waveform as required.

E. RC SNUBBERS

The applicability of RC snubber in *Fast-Mode* switching is considered to be a whole investigation on its own. The inclusion of an RC snubber would affect the circuit environment of the entire switching circuit, and the effects on the main idea of achieving optimal energy transition would be a very complicated question to answer.

VI. POTENTIAL OSCILLATION SUPPRESSION METHODS OF *FAST MODE*

One of the main hurdles to the implementation of ZOS is that the point of operation where the benefits outweigh the effort is very narrow, and a small difference from the optimisation equation in voltage, current, inductance, or capacitance creates a very large overshoot. This means that, practically, it is not an attractive solution if the load cannot vary in the slightest.

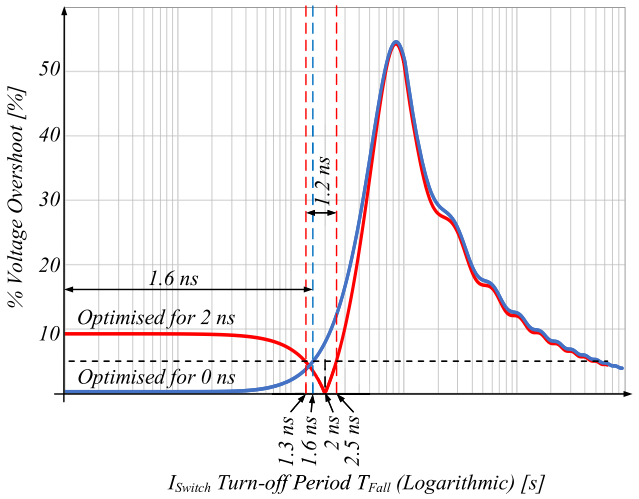

FIGURE 22. Voltage overshoot vs switching speed comparison when optimising for non-ideal switch and ideal switch.

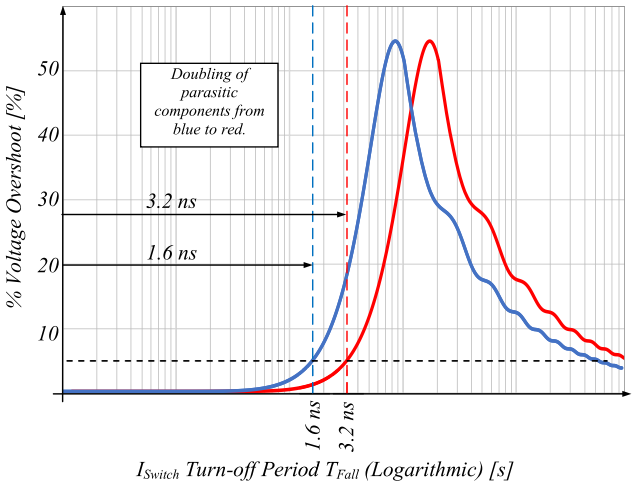

FIGURE 23. Voltage overshoot vs switching speed comparison when parasitic components are doubled.

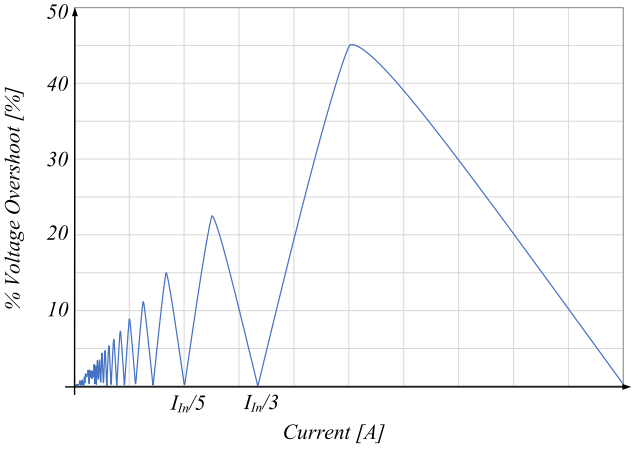

FIGURE 24. Voltage overshoot vs Input Current comparison when current is decreasing.

This point of operation is even narrower when optimised for a non-ideal switching transition. Additionally, it would be very difficult to achieve the designed point of operation practically.

This hurdle can be overcome by widening the area of operation or creating multiple areas of operation, and methods to achieve this are discussed in this section. The widening of the area of operation is also going to be the main research direction in *Fast-Mode* switching research and is also the main goal of [11] and [12].

A. COMPENSATION FOR NON-IDEAL SWITCHING EVENT

As an ideal switching event is not possible, methods to achieve effective energy transition with a non-ideal switching event must be investigated.

In Section IV, Fig. 17, an example of achieving no overshoot with a non-ideal switching event is presented, and in Fig. 15, an optimisation for ideal switch is presented.

When a switching event is considered, and the allowable overshoot is relaxed from 0% to 5%, a window period where the overshoot is below 5% can be measured and compared. In Fig. 22, a comparison can be seen when a circuit is optimised for a non-ideal switching event and for an ideal switching event.

It can be seen that the window period of the ideal switching event is 1.6 ns when the overshoot is below 5%, and the window period is 1.2 ns for the non-ideal switching event. So, if a fast switch is available, optimising for an ideal switch would be better than a non-ideal switch.

Additionally, to minimise the penalty of a slower switching event, one can again return to the optimisation equation (3). In this equation, it can be seen that the equation is dependent on the relationships between the voltage and current and the inductance and capacitance and not on the values themselves.

This means that the overshoot graph, as seen in the figure above, is translatable.

When both the parasitic inductance and capacitance are increased with the same ratio, the overshoot graphs can be translated as seen in Fig.23.

In Fig. 23, the overshoot of a switching transition of 3.2ns is reduced from 18% to 5% by doubling parasitic components, where 3.2ns is considered to be a realistic transition period with WBG technology available.

However, the amount by which the parasitic components are increased must be kept as small as possible, specifically the capacitance. The capacitance will directly influence the speed of the switch, and a better gate driver will have to be employed to keep the transition period very small while increasing the parasitic capacitance. Keeping in mind a faster-than-designed switching transition will have better results.

B. COMPENSATION OF RANGE OF CURRENT

When the optimisation equation (3) is considered again, another important consideration can be seen.

This was mentioned in [12], which discusses how the presence of the n value creates more than one optimisation point.

TABLE 2. Fast mode equations derived from mathematical circuit model.

Time Period	Equation
$I_{LPar,FM,P1}(t)$	$$\frac{C_{Diode}I_{in}(\mathrm{t}-\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}\,\mathrm{Sin}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])}{(C_{Switch}+C_{Diode})T_{Fall}} \quad (4)$$
$I_{LPar,FM,P2}(t)$	$$C_{Diode}I_{in}(\frac{1}{C_{Switch}+C_{Diode}}-\frac{\sqrt{C_{Switch}C_{Diode}L_{Par}}(\mathrm{Sin}[\frac{T_{Fall}-\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]+\mathrm{Sin}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])}{(C_{Switch}+C_{Diode})^{3/2}T_{Fall}}) \quad (5)$$
$I_{LPar,FM,P3}(t)$	$$(2(C_{Switch}+C_{Diode})^2I_{in}\sqrt{L_{Par}}T_{Fall}-2\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}](C_{Diode}{}^{3/2}\sqrt{C_{Switch}(C_{Switch}+C_{Diode})}$$ $$I_{in}L_{Par}\mathrm{Sin}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]+I_{in}\sqrt{L_{Par}}(C_{Switch}(C_{Switch}+C_{Diode})T_{Fall}-C_{Diode}{}^{3/2}$$ $$\sqrt{C_{Switch}(C_{Switch}+C_{Diode})L_{Par}}\mathrm{Sin}[\frac{T_{Clamp}-T_{Fall}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]))+\sqrt{C_{Switch}}((C_{Switch}+C_{Diode})T_{Fall}$$ $$(I_{in}(-2T_{Clamp}+T_{Fall})+2(C_{Switch}+C_{Diode})V_{Out})+2C_{Diode}{}^2I_{in}L_{Par}$$ $$\mathrm{Cos}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]-2C_{Diode}{}^2I_{in}L_{Par}\mathrm{Cos}[\frac{T_{Clamp}-T_{Fall}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]$$ $$\mathrm{Sin}[\frac{T_{Clamp}-\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])/(2(C_{Switch}+C_{Diode})^2\sqrt{L_{Par}}T_{Fall}) \quad (6)$$
$V_{Diode,FM,P1}(t)$	$$(2C_{Switch}C_{Diode}I_{in}L_{Par}-(C_{Switch}+C_{Diode})I_{in}\mathrm{t}^2+2(C_{Switch}+C_{Diode})^2T_{Fall}V_{Out}-$$ $$2C_{Switch}C_{Diode}I_{in}L_{Par}\mathrm{Cos}[\frac{t}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])/(2(C_{Switch}+C_{Diode})^2T_{Fall})$$
$V_{Diode,FM,P2}(t)$	$$((C_{Switch}+C_{Diode})T_{Fall}(I_{in}(T_{Fall}-2\mathrm{t})+2(C_{Switch}+C_{Diode})V_{Out})+2C_{Switch}C_{Diode}I_{in}$$ $$L_{Par}\mathrm{Cos}[\frac{T_{Fall}-\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]-2C_{Switch}C_{Diode}I_{in}L_{Par}\mathrm{Cos}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])/$$ $$(2(C_{Switch}+C_{Diode})^2T_{Fall}) \quad (7)$$

TABLE 2. ***(Continued.)*** **Fast mode equations derived from mathematical circuit model.**

Time Period	Equation
$V_{Switch,FM,P1}(t)$	$$(I_{in}(2{C_{Diode}}^2 L_{Par} + C_{Switch}\mathrm{t}^2 + C_{Diode}\mathrm{t}^2 - 2{C_{Diode}}^2 L_{Par}\mathrm{Cos}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]))/$$ $$(2(C_{Switch}+C_{Diode})^2 T_{Fall})$$
$V_{Switch,FM,P2}(t)$	$$-((I_{in}((C_{Switch}+C_{Diode})T_{Fall}(T_{Fall}-2\mathrm{t}) - 2{C_{Diode}}^2 L_{Par}\mathrm{Cos}[\frac{T_{Fall}-\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]$$ $$+2{C_{Diode}}^2 L_{Par}\mathrm{Cos}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]))/(2(C_{Switch}+C_{Diode})^2 T_{Fall})) \quad (8)$$
$V_{Switch,FM,P3}(t)$	$$V_{Out} - (((C_{Switch}+C_{Diode})T_{Fall}(I_{in}(-2T_{Clamp}+T_{Fall}) + 2(C_{Switch}+C_{Diode})V_{Out})$$ $$+2{C_{Diode}}^2 I_{in}L_{Par}\mathrm{Cos}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}] - 2{C_{Diode}}^2 I_{in}L_{Par}\mathrm{Cos}[\frac{T_{Clamp}-T_{Fall}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])$$ $$\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])/(2(C_{Switch}+C_{Diode})^2 T_{Fall}) + (I_{in}({C_{Switch}}^{3/2}\sqrt{L_{Par}}T_{Fall} +$$ $$C_{Diode}\sqrt{C_{Switch}L_{Par}}T_{Fall} + {C_{Diode}}^{3/2}\sqrt{C_{Switch}+C_{Diode}}L_{Par}\mathrm{Sin}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}] - {C_{Diode}}^{3/2}$$ $$\sqrt{C_{Switch}+C_{Diode}}L_{Par}\mathrm{Sin}[\frac{T_{Clamp}-T_{Fall}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])\,\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])/((C_{Switch}+C_{Diode})^2 T_{Fall}) \quad (9)$$

If a circuit is optimized according to (3), n is chosen as 1, and the switching speed is infinitely fast, the overshoot will be zero. If the current, I_{Lpar}, becomes larger, the overshoot will increase indefinitely, but if the current becomes smaller, the overshoot will increase up to a maximum and then decrease until another optimization point is reached again. This next optimisation point will occur when n is equal to 2 or when I_{Lpar} is equal to $I_{In}/3$. This reoccurring optimisation point will occur closer and closer to each other as the current decreases, as can be seen in Fig. 24.

A plot similar to the one presented in Fig. 24 can be reproduced for any parameter change from (3).

When the inductance is considered, a very similar plot will be reproduced, as another optimized point will reoccur when the inductance is lowered but will not reoccur when the inductance is increased.

The inverse is true for the capacitance and the voltage. If the capacitance or voltage is decreased, the optimised point will not reoccur but will reoccur if the capacitance or voltage is increased.

VII. RESEARCH IMPLICATION DISCUSSION

The main aim of this research is to extend the modelling of a switching event to encompass both the existing well-known behaviour and the behaviour under very fast switching conditions.

The mathematical results show that when the turn-off speed is fast enough, the circuit will respond in a different

TABLE 3. Slow mode equations derived from mathematical circuit model.

Time Period	Equation
$I_{Lpar,SM,P1}(t)$	$$\frac{C_{Diode}I_{in}(\sqrt{C_{Switch}+C_{Diode}}\,\mathrm{t}-\sqrt{C_{Switch}C_{Diode}L_{Par}}\,\mathrm{Sin}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])}{(C_{Switch}+C_{Diode})^{3/2}T_{Fall}} \quad (10)$$
$I_{Lpar,SM,P2}(t)$	$$-\frac{1}{2T_{Fall}}(-2I_{in}\mathrm{t}+\frac{1}{(C_{Switch}+C_{Diode})^2L_{Par}}(2I_{in}L_{Par}\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]$$ $$(C_{Switch}(C_{Switch}+C_{Diode})T_{Clamp}+C_{Diode}\sqrt{C_{Switch}C_{Diode}(C_{Switch}+C_{Diode})L_{Par}}$$ $$\mathrm{Sin}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])+\sqrt{C_{Switch}L_{Par}}(2C_{Switch}(C_{Switch}+2C_{Diode})I_{in}L_{Par}$$ $$-(C_{Switch}+C_{Diode})I_{in}T_{Clamp}{}^2+2(C_{Switch}+C_{Diode})^2T_{Fall}V_{Out}+2C_{Diode}{}^2I_{in}L_{Par}$$ $$\mathrm{Cos}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])) \quad (11)$$
$I_{Lpar,SM,P3}(t)$	$$(2(C_{Switch}+C_{Diode})^2I_{in}\sqrt{L_{Par}}T_{Fall}-C_{Switch}(C_{Switch}+C_{Diode})I_{in}\sqrt{L_{Par}}T_{Clamp}$$ $$\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+\sqrt{C_{Switch}}(C_{Diode}{}^{3/2}\sqrt{C_{Switch}+C_{Diode}}I_{in}L_{Par}$$ $$\mathrm{Sin}[\frac{-\sqrt{C_{Switch}+C_{Diode}}T_{Clamp}+\sqrt{C_{Diode}}(T_{Clamp}-\mathrm{t})}{\sqrt{C_{Switch}C_{Diode}L_{Par}}}]-C_{Diode}{}^{3/2}\sqrt{C_{Switch}+C_{Diode}}I_{in}L_{Par}$$ $$\mathrm{Sin}[\frac{\sqrt{C_{Switch}+C_{Diode}}T_{Clamp}+\sqrt{C_{Diode}}(T_{Clamp}-\mathrm{t})}{\sqrt{C_{Switch}C_{Diode}L_{Par}}}]+(2C_{Switch}(C_{Switch}+2C_{Diode})I_{in}L_{Par}$$ $$-(C_{Switch}+C_{Diode})I_{in}T_{Clamp}{}^2+2(C_{Switch}+C_{Diode})^2T_{Fall}V_{Out})\mathrm{Sin}[\frac{T_{Clamp}-\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]$$ $$-2(C_{Switch}+C_{Diode})^2I_{in}L_{Par}\mathrm{Sin}[\frac{T_{Fall}-\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])-2\sqrt{C_{Switch}}C_{Diode}{}^2I_{in}L_{Par}$$ $$\mathrm{Cos}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])/(2(C_{Switch}+C_{Diode})^2\sqrt{L_{Par}}T_{Fall}) \quad (12)$$

TABLE 3. *(Continued.)* **Slow mode equations derived from mathematical circuit model.**

Time Period	Equation
$V_{Diode,SM,P1}(t)$	$$\frac{1}{2(C_{Switch}+C_{Diode})^2 T_{Fall}}(2C_{Switch}C_{Diode}I_{in}L_{Par}-(C_{Switch}+C_{Diode})I_{in}\mathrm{t}^2+2(C_{Switch}+C_{Diode})^2 T_{Fall}V_{Out}-2C_{Switch}C_{Diode}I_{in}L_{Par}\mathrm{Cos}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])$$ (13)
$V_{Switch,SM,P1}(t)$	$$\frac{I_{in}(2{C_{Diode}}^2 L_{Par}+(C_{Switch}+C_{Diode})\mathrm{T}^2-2{C_{Diode}}^2 L_{Par}\mathrm{Cos}[\frac{\mathrm{t}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}])}{2(C_{Switch}+C_{Diode})^2 T_{Fall}}$$ (14)
$V_{Switch,SM,P2}(t)$	$$\frac{1}{2(C_{Switch}+C_{Diode})^2 T_{Fall}}(-(2C_{Switch}(C_{Switch}+C_{Diode})I_{in}L_{Par}-(C_{Switch}+C_{Diode})I_{in}{T_{Clamp}}^2+2(C_{Switch}+C_{Diode})^2 T_{Fall}V_{Out}+2{C_{Diode}}^2 I_{in}L_{Par}\mathrm{Cos}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+2((C_{Switch}+C_{Diode})^2(I_{in}L_{Par}+T_{Fall}V_{Out})+I_{in}((C_{Switch}+C_{Diode})\sqrt{C_{Switch}L_{Par}}T_{Clamp}+{C_{Diode}}^{3/2}\sqrt{C_{Switch}+C_{Diode}}L_{Par}\mathrm{Sin}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])))$$ (15)
$V_{Switch,SM,P3}(t)$	$$\frac{1}{2(C_{Switch}+C_{Diode})^2 T_{Fall}}(2(C_{Switch}+C_{Diode})^2 T_{Fall}V_{Out}-{C_{Diode}}^2 I_{in}L_{Par}\mathrm{Cos}[\frac{-\sqrt{C_{Switch}+C_{Diode}}T_{Clamp}+\sqrt{C_{Diode}}(T_{Clamp}-\mathrm{t})}{\sqrt{C_{Switch}C_{Diode}L_{Par}}}]-{C_{Diode}}^2 I_{in}L_{Par}\mathrm{Cos}[\frac{\sqrt{C_{Switch}+C_{Diode}}T_{Clamp}+\sqrt{C_{Diode}}(T_{Clamp}-\mathrm{t})}{\sqrt{C_{Switch}C_{Diode}L_{Par}}}]+(-2C_{Switch}(C_{Switch}+2C_{Diode})I_{in}L_{Par}+(C_{Switch}+C_{Diode})I_{in}{T_{Clamp}}^2-2(C_{Switch}+C_{Diode})^2 T_{Fall}V_{Out})\mathrm{Cos}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+2(C_{Switch}+C_{Diode})^2 I_{in}L_{Par}\mathrm{Cos}[\frac{-T_{Fall}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+2C_{Switch}I_{in}\sqrt{C_{Switch}L_{Par}}T_{Clamp}\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+2C_{Diode}I_{in}\sqrt{C_{Switch}L_{Par}}T_{Clamp}\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}]+2{C_{Diode}}^{3/2}\sqrt{C_{Switch}+C_{Diode}}I_{in}L_{Par}\mathrm{Sin}[\frac{T_{Clamp}}{\sqrt{\frac{C_{Switch}C_{Diode}L_{Par}}{C_{Switch}+C_{Diode}}}}]\mathrm{Sin}[\frac{-T_{Clamp}+\mathrm{t}}{\sqrt{C_{Switch}L_{Par}}}])$$ (16)

manner as expected, thus, the existing approaches will have to adapt as well.

This model also shows that the point when the circuit progression will change from *Slow-Mode* to *Fast-Mode* is solvable for all possible values of the variables. Therefore, the *Fast-Mode* equivalent circuit progressions and modelling show great promise for realising the advantages of wide and ultra-wide bandgap devices.

VIII. CONCLUSION

This research presents a fundamental model of the switching node of the turn-off switching transition of a boost converter with parasitic components and an explicitly modelled turn-off transition. From the model, it was found that an alternative equivalent circuit progression is responsible and can explain and predict all the results from ZOS while also explaining the expected results from conventional switching. An optimal energy transition theory is presented to provide a fundamental explanation of why the overshoot exists and how to address the underlying energy mismatch to minimise the eventual voltage overshoot. Lastly, a potential solution to widening the ZOS operation area is suggested by incorporating larger parasitic components. The principles established in this paper can be built upon to eventually become the building blocks to realise the potential of WBG and UWBG technology.

APPENDIX
MATHEMATICAL EQUATIONS

See Tables 2 and 3.

REFERENCES

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[3] T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 402–405, doi: 10.1109/WIPDA.2015.7369328.

[4] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Investigation of gallium nitride devices in high-frequency LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 571–583, Jan. 2017, doi: 10.1109/TPEL.2016.2528291.

[5] Y. Zhang, M. Rodríguez, and D. Maksimovic, "Very high frequency PWM buck converters using monolithic GaN half-bridge power stages with integrated gate drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7926–7942, Nov. 2016, doi: 10.1109/TPEL.2015.2513058.

[6] X. Huang, Z. Liu, F. C. Lee, and Q. Li, "Characterization and enhancement of high-voltage cascode GaN devices," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 270–277, Feb. 2015, doi: 10.1109/TED.2014.2358534.

[7] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401.

[8] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A review of switching oscillations of wide bandgap semiconductor devices," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13182–13199, Dec. 2020, doi: 10.1109/TPEL.2020.2995778.

[9] R. J. Kaplar, A. A. Allerman, A. M. Armstrong, M. H. Crawford, J. R. Dickerson, A. J. Fischer, A. G. Baca, and E. A. Douglas, "Review—Ultra-wide-bandgap AlGaN power electronic devices," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 2, pp. 3061–3066, 2017, doi: 10.1149/2.0111702jss.

[10] S. Matlok, "Zero overvoltage switching 'ZOS'—Breaking the rules of parasitic inductance," Mar. 2018, doi: 10.13140/RG.2.2.11217.63843.

[11] J. Deng, E. Peters, W. Wang, P. Venugopal, J. Popovic, and B. Ferreira, "Turn-off overvoltage characterization and mitigation in wide bandgap power transistors," in *Proc. 23rd Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2021, pp. 1–8.

[12] N. Schmied, S. Matlok, and M. März, "Analysis of the zero overvoltage switching phenomenon," *IEEE Access*, vol. 10, pp. 128263–128275, 2022, doi: 10.1109/ACCESS.2022.3227442.

[13] A. I. Emon, Mustafeez-ul-Hassan, A. B. Mirza, J. Kaplun, S. S. Vala, and F. Luo, "A review of high speed GaN power modules: State of the art, challenges, and solutions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2707–2729, Jun. 2022, doi: 10.1109/JESTPE.2022.3232265.

[14] K. Umetani, K. Tanohara, K. Abe, M. Ishihara, and E. Hiraki, "Power loop inductance optimization strategy for eliminating turn-off switching surge for GaN-HEMT switching device," in *Proc. 25th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2023, pp. 1–9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264302.

[15] H. Li and S. Munk-Nielsen, "Challenges in switching SiC MOSFET without ringing," in *Proc. PCIM Eur., Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2014, pp. 1–6.

[16] A. Lemmon, S. Banerjee, K. Matocha, and L. Gant, "Analysis of packaging impedance on performance of SiC MOSFETs," in *Proc. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2016, pp. 1–8.

[17] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014, doi: 10.1109/TPEL.2013.2266103.

[18] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A multiloop method for minimization of parasitic inductance in GaN-based high-frequency DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4728–4740, Jun. 2017, doi: 10.1109/TPEL.2016.2597183.

[19] Z. Qi, Y. Pei, L. Wang, Q. Yang, and K. Wang, "A highly integrated PCB embedded GaN full-bridge module with ultralow parasitic inductance," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4161–4173, Apr. 2022, doi: 10.1109/TPEL.2021.3128694.

[20] X. Tian, N. Jia, D. B. Chertkovsky, J. Sun, H. Bai, L. M. Tolbert, and H. Cui, "An embedded GaN power module with double-sided cooling and high-density integration," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2022, pp. 1–7, doi: 10.1109/ECCE50734.2022.9947786.

[21] S. Lu, T. Zhao, Z. Zhang, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "Low parasitic-inductance packaging of a 650 V/150 a half-bridge module using enhancement-mode gallium-nitride high electron mobility transistors," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 344–351, Jan. 2023, doi: 10.1109/TIE.2022.3148750.

[22] B. Li, X. Yang, K. Wang, H. Zhu, L. Wang, and W. Chen, "A compact double-sided cooling 650 V/30A GaN power module with low parasitic parameters," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 426–439, Jan. 2022, doi: 10.1109/TPEL.2021.3092367.

[23] H. Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," in *Proc. IEEE 5th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2014, pp. 1–5, doi: 10.1109/PEDG.2014.6878691.

[24] T. Liu, Y. Zhou, Y. Feng, T. T. Y. Wong, and Z. J. Shen, "Experimental and modeling comparison of different damping techniques to suppress switching oscillations of SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 7024–7031, doi: 10.1109/ECCE.2018.8557872.

[25] I. Josifovic, J. Popovic-Gerber, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, Aug. 2012, doi: 10.1109/TPEL.2012.2185951.

[26] P. Nayak and K. Hatua, "Active gate driving technique for a 1200 V SiC MOSFET to minimize detrimental effects of parasitic inductance in the converter layout," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1622–1633, Mar. 2018, doi: 10.1109/TIA.2017.2780175.

[27] P. Nayak and K. Hatua, "Parasitic inductance and capacitance-assisted active gate driving technique to minimize switching loss of SiC MOSFET," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8288–8298, Oct. 2017, doi: 10.1109/TIE.2017.2711512.

[28] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A novel active gate driver for improving SiC MOSFET switching trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, Nov. 2017, doi: 10.1109/TIE.2017.2719603.

[29] Y. Yang, Y. Wen, and Y. Gao, "A novel active gate driver for improving switching performance of high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7775–7787, Aug. 2019, doi: 10.1109/TPEL.2018.2878779.

[30] S. Zhao, A. Dearien, Y. Wu, C. Farnell, A. U. Rashid, F. Luo, and H. A. Mantooth, "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1882–1898, Feb. 2020, doi: 10.1109/TPEL.2019.2922112.

[31] H. C. P. Dymond, J. Wang, D. Liu, J. J. O. Dalton, N. McNeill, D. Pamunuwa, S. J. Hollis, and B. H. Stark, "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, Jan. 2018, doi: 10.1109/TPEL.2017.2669879.

[32] Z. Gao, J. Zhang, Y. Huang, R. Guan, and Y. Zhou, "A closed-loop active gate driver of SiC MOSFET for voltage spike suppression," *IEEE Open J. Power Electron.*, vol. 3, pp. 723–730, 2022, doi: 10.1109/OJPEL.2022.3209334.

[33] A. B. Mirza, A. I. Emon, S. S. Vala, and F. Luo, "Noise immune cascaded gate driver solution for driving high speed GaN power devices," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 5366–5371, doi: 10.1109/ECCE47101.2021.9595515.

[34] H. Takayama, S. Fukunaga, and T. Hikihara, "Switching trajectory control of SiC MOSFET based on I—V characteristics using digital active gate driver," in *Proc. IEEE 12th Energy Convers. Congr. Expo. Asia (ECCE-Asia)*, May 2021, pp. 1338–1343, doi: 10.1109/ECCE-Asia49820.2021.9479118.

[35] W. J. Zhang, J. Yu, W. T. Cui, Y. Leng, J. Liang, Y.-T. Hsieh, H.-H. Tsai, Y.-Z. Juang, W.-K. Yeh, and W. T. Ng, "A smart gate driver IC for GaN power HEMTs with dynamic ringing suppression," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14119–14132, Dec. 2021, doi: 10.1109/TPEL.2021.3089679.

[36] J. Kuhn, T. Zekorn, K. Vohl, R. Wunderlich, and S. Heinen, "An active gate driver for iteratively optimizing the switching characteristics of SiC MOSFETs," in *Proc. 25th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2023, pp. 1–8, doi: 10.23919/EPE23ECCEEurope58414.2023.10264429.

[37] S. Fukunaga, H. Takayama, and T. Hikihara, "A study on digital active gate driving of DC–DC converter for suppressing switching surge voltage," in *Proc. Int. Power Electron. Conf. (IPEC-Himeji ECCE Asia)*, May 2022, pp. 2093–2096, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9806952.

[38] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014, doi: 10.1109/TPEL.2013.2268058.

[39] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017, doi: 10.1109/TPEL.2017.2655496.

[40] F. Gao, Q. Zhou, P. Wang, and C. Zhang, "A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2339–2353, Mar. 2018, doi: 10.1109/TPEL.2017.2690938.

[41] C. Li, Z. Lu, Y. Chen, C. Li, H. Luo, W. Li, and X. He, "High off-state impedance gate driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2999–3011, Mar. 2020, doi: 10.1109/TPEL.2019.2932263.

[42] B. N. Torsæter, S. Tiwari, R. Lund, and O.-M. Midtgård, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module," in *Proc. IEEE 7th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2016, pp. 1–8, doi: 10.1109/PEDG.2016.7527071.

[43] M. Joko, A. Goto, M. Hasegawa, S. Miyahara, and H. Murakami, "Snubber circuit to suppress the voltage ringing for SiC device," in *Proc. PCIM Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2015, pp. 1–6.

[44] K. Yatsugi, K. Nomura, and Y. Hattori, "Analytical technique for designing an RC snubber circuit for ringing suppression in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4736–4745, Jun. 2018, doi: 10.1109/TPEL.2017.2731421.

[45] J. Chen, Q. Luo, J. Huang, Q. He, P. Sun, and X. Du, "Analysis and design of an RC snubber circuit to suppress false triggering oscillation for GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2690–2704, Mar. 2020, doi: 10.1109/TPEL.2019.2927486.

[46] X. Yang, M. Xu, Q. Li, Z. Wang, and M. He, "Analytical method for RC snubber optimization design to eliminate switching oscillations of SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4672–4684, Apr. 2022, doi: 10.1109/TPEL.2021.3127516.

[47] H. Yang, X. Yu, Z. Xu, H. Luo, K. He, H. Cai, P. Jin, and K. Dai, "RC snubber design by multi-objective particle swarm optimization for SiC-MOSFET switching oscillation," in *Proc. IEEE 14th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2023, pp. 1096–1102, doi: 10.1109/PEDG56097.2023.10215135.

[48] Y. Zhou, Y. Jin, H. Xu, H. Luo, W. Li, and X. He, "Heterogeneous integration of silicon-based RC snubber in SiC power module for parasitic oscillation noise reduction," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 6902–6906, Jun. 2023, doi: 10.1109/TPEL.2023.3249798.

[49] L. Che, Y. Dong, and G. Lei, "Design optimization of RC snubber circuit for a SiC power module," in *Proc. 23rd Int. Conf. Electron. Packag. Technol. (ICEPT)*, Aug. 2022, pp. 1–6, doi: 10.1109/ICEPT56209.2022.9873263.

[50] M. Xu, X. Yang, and J. Li, "C-RC snubber optimization design for improving switching characteristics of SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12005–12016, Oct. 2022, doi: 10.1109/TPEL.2022.3180387.

[51] M. Shahverdi, M. Mazzola, R. Schrader, A. Lemmon, C. Parker, and J. Gafford, "Active gate drive solutions for improving SiC JFET switching dynamics," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 2739–2743, doi: 10.1109/APEC.2013.6520683.

FRANCOIS P. DU TOIT received the B.Eng. degree in electrical engineering from the University of Pretoria, South Africa, in 2013, and the M.S. degree in electrical engineering from the University of the Witwatersrand, Johannesburg, South Africa, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering.

IVAN W. HOFSAJER (Member, IEEE) was born in Johannesburg, South Africa. He received the B.Ing. and D.Ing. degrees in electrical engineering from the former Rand Afrikaans University, Johannesburg, in 1991 and 1998, respectively. He worked in the field of electromagnetic interference with South African Atomic Energy Corporation, before joining the Faculty of Rand Afrikaans University. He is currently an Associate Professor with the School of Electrical and Information Engineering, University of the Witwatersrand, Johannesburg. His research interests include power electronics and electromagnetics.