

Modelling and Optimisation of the Turn-Off Switching Transition in Fast-Switching Power Semiconductor Devices



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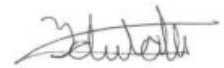
A thesis submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of
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Declaration

I declare that this thesis report is my own original work, submitted to the University of the Witwatersrand for the degree of Doctor of Philosophy. This work has not been submitted to any institute of learning for a degree.

A handwritten signature in dark ink, appearing to read 'F. du Toit', with a stylized flourish extending to the right.

Francois Paulus du Toit
June 2025

Dedicated to *Ingrid*.

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First and foremost, to my wonderful wife, Ingrid, I cannot thank you enough for your love, patience, and the countless ways you've kept me sane while I immersed myself in this PhD. From our daily walks to always making sure I had the space and time to focus, you have been my rock. Your encouragement gave me strength when I doubted myself, and your belief in me made this all possible.

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Abstract

The transition from Silicon to modern wide bandgap semiconductor devices substantially increases the switching speed, enhancing the efficiency and energy density of power electronic converters. However, this increase in switching speed leads to a larger voltage overshoot across devices during turn-off due to the leakage inductance of the commutation path. While minimising the parasitic inductance is effective in solving this problem, it can never be entirely eliminated. This inductance-induced overshoot already restricts the full potential of wide bandgap devices and will become an even greater challenge with the introduction of ultra-wide bandgap devices in the future.

As this overshoot problem has existed almost since the inception of power electronics, several methods for reducing voltage overshoot have been reported in the literature. However, nearly all studies only present the experimental performance of their own results before and after the implementation of the overshoot suppression method and never compare the results to the existing body of results. Even though these experimental results and methods are difficult to compare due to varying testing conditions, not comparing results runs the risk of not being as successful or relevant as it is thought to be. In this work, a framework is developed that enables the comparison of results from the literature. This approach allows us to identify which methods are potentially more effective and should be given priority. Recent results from the literature are analysed using this framework with the conclusion that the emerging method of Zero Overvoltage Switching offers the most future potential for high-speed switching.

In the literature, it has already been demonstrated that Zero Overvoltage Switching can reduce the voltage overshoot across a device as the parasitic inductance and switching speed increase, contrary to convention. However, the literature does not yet offer a sound theoretical foundation for this anomalous result, which limits its application. Additionally, the technique requires ideal switching and a very narrow range of circuit parameters to be implemented successfully, further limiting its application.

This work investigates the underlying mechanisms of Zero Overvoltage Switching to firstly place the technique on a sound theoretical basis and secondly to show how the range of application might be increased to account for non-ideal switching and a wide range of circuit parameters. The turn-off switching transition of a clamped inductive load is investigated, explicitly modelling the adjustable turn-off current of the switch and in the presence of parasitic elements. The adjustable

turn-off current of the switch is able to account for both fast and slow switching conditions. From the resulting model, it is seen that when switching slowly, the clamp diode conducts before the current in the switching device becomes zero, and it is this switching that describes the generally accepted understanding of the switching event. However, when switching very fast, the current in the device becomes zero before the clamp diode conducts, and this alternative order of events accounts for the unexpected results of Zero Overvoltage Switching. It is seen that these fast-switching conditions require the ideal energy at the exact time the diode starts to conduct to eliminate the overvoltage. This is different from conventional soft switching, where there is an energy balance between the load inductor and snubber capacitances.

This work provides the circuit-level analysis and the state progressions of both fast and slow switching by implementing circuit analysis and Laplace transforms to create a mathematical model to compare the two. This allows the mechanism of Zero Overvoltage Switching to become visible while still being able to explain the results of conventional switching. However, Zero Overvoltage Switching can only be implemented with ideal switching and with a very specific ratio and range of voltage and current. It is seen that if the turn-off current of the switch is modelled with two segments instead of one to represent the shaping of the turn-off waveform, the model shows that ideal switching is not required to effectively eliminate the overshoot and range of voltage and current where Zero Overvoltage Switching can take place is greatly expanded.

Beyond addressing the specific problem of voltage overshoot, this research highlights a broader issue in power electronics: the field's fragmented and application-driven nature has limited the development of fundamental, unifying knowledge. The findings of this work suggest that the constraints imposed by parasitic inductance may not be as fundamental as previously assumed. It also underscores a key point that the primary obstacle to realising the full potential of these devices lies in the development of advanced control methods rather than the increasingly challenging task of further reducing parasitic components.

Academic Contribution

Journals:

1. F. P. D. Toit and I. W. Hofsjager, 'Fundamental Modeling of the Switching Transition in High-Speed Power Electronics', *IEEE Access*, vol. 12, pp. 38646–38663, 2024, doi: 10.1109/ACCESS.2024.3375388.
2. F. P. D. Toit and I. W. Hofsjager, 'A Review of the Experimental Performance of Turn-Off Methods in Wide Bandgap Semiconductors', *IEEE Open Journal for Power Electronics*, vol. 5, pp. 1671-1683, 2024, doi: 10.1109/OJPEL.2024.3478178.
3. F. P. D. Toit and I. W. Hofsjager, 'Expanding Zero Overvoltage Switching Range of Power Switches Through Controlled Turn-Off', *IEEE Access*, **Submitted**

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Nomenclature

Acronyms / Abbreviations

BJT Bipolar Junction Transistor

GaN Gallium Nitrate

IGBT Insulated-Gate Bipolar Transistor

MOSFET Metal Oxide Semiconductor Field-Effect Transistor

Si Silicon

SiC Silicon Carbide

UWBG Ultra-Wide Bandgap

WBG Wide Bandgap

ZOS Zero Overvoltage Switching

Chapter 1

Introduction

1.1 Background

Silicon has generally been the semiconductor material used in power electronic devices for most of the lifetime of the field. From the introduction of the thyristor in the 1960s, followed by BJTs, power MOSFETs, and IGBTs, silicon has driven their significant advancements. However, silicon semiconductor technology is now considered mature and has almost reached its full potential [1]–[12].

In contrast, wide bandgap (WBG) semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), have emerged as the preferred materials for new technologies. These WBG devices have become increasingly popular in research due to their superior physical properties compared to Silicon [12]–[28]. A comparison of the physical properties can be seen in Fig. 1.1.

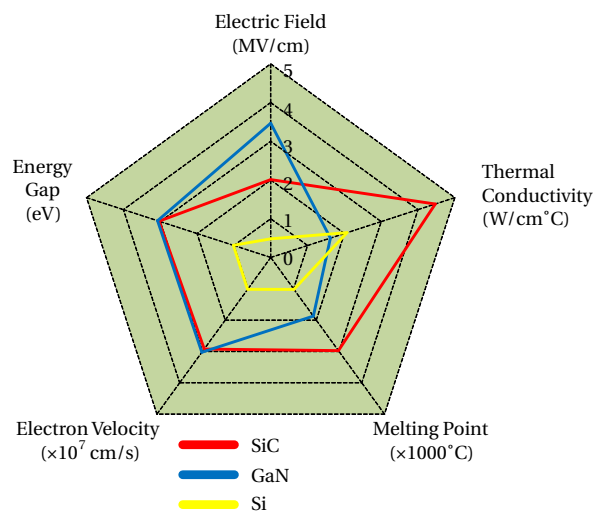


Fig. 1.1 Summary of semiconductor material properties (adapted from: [6], [13])

The figure highlights that WBG devices have higher energy gaps, electric fields, and electron velocities than Silicon devices. As such, they offer several compelling advantages that contribute to their growing popularity in the field.

Some other major advantages are operation at higher temperatures and at higher voltages, which also carry major benefits, however, the most important advantage investigated in this research is the ability of WBG devices to switch much faster than their Silicon predecessors. This ability to switch faster, in turn, has several advantages, including increased efficiency, increased switching frequency, and increased energy density [12], [27]–[29].

Unfortunately, as semiconductor devices switch faster, the overvoltage and ringing in the circuit also increase, which, in turn, has several unwanted side effects. These negative side effects include increased losses, increased EMI, the need for higher-rated components, which are larger and more expensive, and increased device stress, which can lead to eventual device failure [6], [30]–[35].

An example of this voltage overshoot and ringing phenomenon during the switching transition can be seen when a standard phase arm is shown in Fig. 1.2.

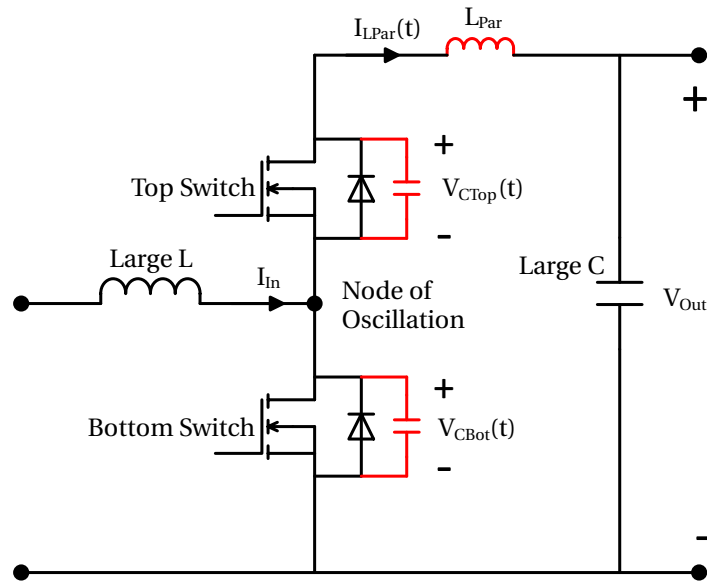


Fig. 1.2 Example of the commutation cell in power electronics

In this image, the parasitic components of the circuit are shown in red. This representation of a phase arm can be applicable to several topologies depending on the modulation and power flow, but the topology investigated in this research is when the device is modelled as a boost converter when the bottom switch turns off.

The turn-off transition of a boost converter is modelled specifically, as this is when the overshoot phenomenon tends to be at its worst. In this representation, the power flows from left to right, and the bottom switch has been turned on for a long time before it starts to turn off. This

means the large inductor is fully charged, the top switch capacitor is fully charged, and the bottom switch capacitor is short-circuited as the switch is fully on.

The switching transition will begin when the bottom switch turns off and the top switch turns on. In this transition, the inductor is assumed to be large enough so that the current stays the same, but the bottom capacitor starts to charge, and the top capacitor starts to discharge. This transition can happen slowly or fast, and the corresponding voltage overshoot of the charging and eventual overshoot and ringing of the bottom capacitor can be seen in Fig. 1.3.

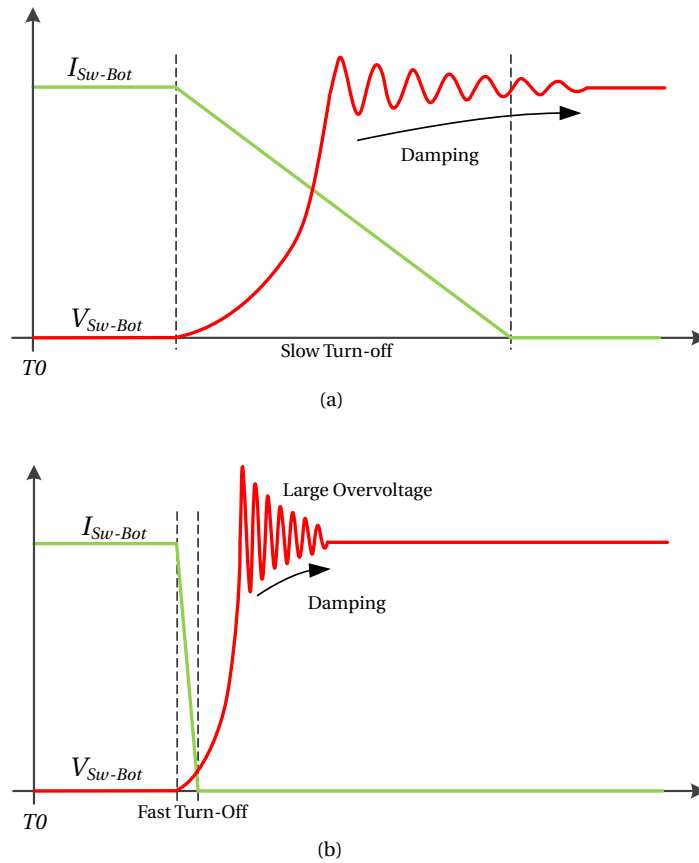


Fig. 1.3 Voltage overshoot comparison of (a) a slow turn-off event, and (b) a fast turn-off event

It can be seen that the voltage overshoot is much larger when the device switches faster. During this switching transition, when the top capacitor has fully discharged, the diode will clamp, shorting the top capacitor, which means it can be ignored. As stated above, the inductor is large enough that the current does not change in the short timeframe under investigation, so it can be represented as a current source. A simplified representation of the circuit mentioned above in Fig. 1.2 when the changes are incorporated can be seen in Fig. 1.4 after the diode clamps and the top capacitor is short-circuited.

This circuit in Fig. 1.4 is simply a resonance circuit where the parasitic components determine the overshoot, and it is this equivalent circuit that is the root cause of the voltage overshoot and

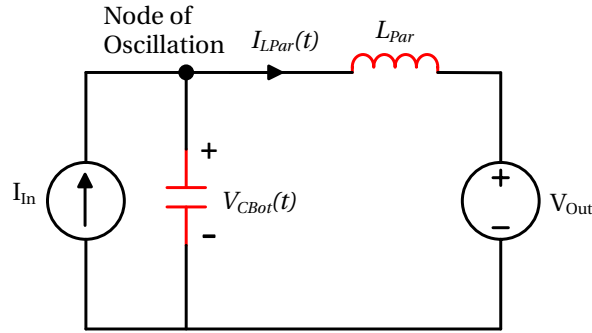


Fig. 1.4 Equivalent resonant circuit after the turn-off transition of the switch has completed

ringing in the switching circuit. When the switch turns off slower, the parasitic elements are not excited as much as when the switch turns off faster, leading to a lower overshoot.

It is important to note that this problem is not a consequence of WBG devices but rather of the intrinsic parasitic components of a circuit in combination with the faster switching speed that devices of the time in question can offer. So, old Si and both SiC and GaN devices can be represented by Fig. 1.2, depending on the size of the parasitic components and the slope of the turn-off current in Fig. 1.3.

Since the inception of power electronics, this overshoot and ringing phenomenon has been a problem. Decades of research have been dedicated to keeping this problem under control while allowing for further increases in switching speed. Although several innovative and functional approaches have been developed that adequately suppress the voltage overshoot for current switching speeds, the two main solutions are to simply switch slower or to decrease the parasitic inductance of the circuit as much as possible [36]–[45].

Generally, if the designer's goal was simply to get a functioning converter and not to optimise the efficiency, speed or converter size, the designer could simply use a gate resistor to switch slower. Although this would increase the converter losses, it is a very effective method of lowering the overshoot.

On the other hand, minimising the parasitic inductance truly solves the overshoot and ringing problem well. This method works so well because the underlying resonance issue is addressed as described above with the simple logic that lower circuit inductance would have a lower voltage overshoot. Minimising the parasitic inductance is generally achieved through circuit layout optimisation and component packaging optimisation. These approaches account for most of the circuit's parasitic inductance and have been the foundation of suppression methods for decades. While all other suppression techniques reduce overshoot for a given circuit, they ultimately rely on parasitic inductance, as it governs the original overshoot. Unfortunately, this method has progressed close to its natural limits, and further improvement past the nano-Henry level that has been achieved [46], [47] is very difficult, and ultimately, the inductance cannot be brought down to zero.

Furthermore, the semiconductor material technology determines the maximum switching speed of the device, and this technology is still progressing very fast. The existing overshoot suppression methods struggle to accommodate the speed of WBG devices, and ultra-wide bandgap (UWBG) devices are already on the horizon. UWBG devices are the next step in semiconductor material technology and have much better physical properties than WBG devices. Typically, WBG devices would have a bandgap between 2 - 4 eV, whereas a UWBG material like Aluminium Nitride (AlN) has a bandgap of 6.2 eV. [48]–[50]. This enhancement in physical properties can enable switching speeds to increase by more than an order of magnitude, significantly complicating the application of overshoot suppression methods that exist today.

So, considering that:

1. Parasitic inductance is already limiting the switching speed of WBG devices,
2. Parasitic inductance cannot be brought down much further or to zero,
3. Semiconductor devices will be able to switch much faster in the near future,

an alternative approach or idea is required to overcome the limitation imposed by the parasitic inductance for future progress and eventual practical application of UWBG devices, even though they do not exist yet.

1.2 Foundational Theory in Power Electronics

Historically, power electronics has evolved by confronting and overcoming a series of practical limitations, each time pivoting and innovating to push the field forward. These pivots have typically occurred when further optimisation became impossible due to some unavoidable constraint, only apparent once engineers had exhausted all available options. This approach has driven much of the field's progress, as each major limitation has required innovation to ensure continued advancement. The problem of overvoltage in fast-switching environments is no different, and given the seriousness of this issue with WBG and, eventually, UWBG devices, it is highly likely that a similar pivot will happen again.

However, this pattern highlights a fundamental trait of the field of power electronics: it is a highly application-driven field. When faced with practical limitations, engineers develop tailored solutions that enable progress within a specific application. Such innovative approaches have repeatedly resolved bottlenecks in various applications of power electronics, allowing for continued improvement. However, while these solutions might address immediate issues, such as a new technique that enables faster switching by suppressing voltage overshoot, as in this case, they often do little to advance the underlying theoretical understanding of the field. The solutions become rules for specific cases: "For fast switching in this particular configuration, follow these steps." This

pattern has produced effective, application-based fixes but has left the field without a clear picture of its true boundaries or theoretical potential.

The consequence is that power electronics, in a sense, operate in the dark. Engineers are working on challenges based on observed practical limits, but it is unclear if they are pushing true physical boundaries or simply encountering limits imposed by current design methods. For example, engineers may devote resources to optimising a parameter that is already near its theoretical limit while other areas that could be significantly improved remain unexplored. Without a clear theoretical map, it is difficult to tell which problems are fundamental and which are situational, meaning resources and research could be misallocated simply because the real opportunities for improvement have not been clearly identified.

This stands in stark contrast to a sister field of energy manipulation, thermodynamics, where theoretical limits are well-defined. In thermodynamics, for instance, no serious pursuit is made toward achieving a 100% efficient steam turbine, as the fundamental laws governing energy conversion are understood to make such efficiency impossible. Thermodynamic principles provide a theoretical framework that defines what is achievable and what is not, ensuring that research and innovation efforts are focused within the bounds of physical reality. This foundational knowledge prevents resources from being wasted on unachievable goals and directs the field toward attainable advancements.

In contrast, each new power electronics design is typically optimised for its specific operating conditions, leading to high-performance solutions that apply only within narrow contexts. While this application-based approach has been effective in solving immediate, practical issues, it has contributed to a fragmented body of knowledge. Optimisations and innovations developed for one application may not transfer effectively to others, meaning each new design often requires a fresh approach to overcome its unique challenges. This lack of a unified theoretical foundation has left power electronics with a patchwork of rules rather than a cohesive understanding of its own principles and limits.

A more fundamental understanding of the theoretical principles governing power electronics would greatly enhance the field, offering a framework within which engineers could work with a clear sense of what is possible. Instead of pursuing isolated solutions to practical problems, research could focus on developing a consistent set of theoretical guidelines that apply across applications. This would not only provide clarity on the real boundaries of power electronics but also allow the field to direct its efforts toward meaningful and impactful advancements, avoiding the pitfalls of application-driven trial and error.

Considering the above-mentioned, this research seeks to address the specific problem of voltage overshoot and ringing caused by parasitic inductance in fast-switching power electronics, not with an application-specific solution but with a fundamental theoretical contribution that can be applied across the field or specifically to UWBG devices when they are introduced.

Recognising the constraints of existing suppression methods, which may soon reach their practical limits and will not be able to suppress the overshoot of future UWBG devices adequately, this thesis provides a foundational theoretical framework that examines the turn-off switching transition. By modelling the interaction between parasitic components and switching dynamics, this work aims to reveal the mechanisms that govern voltage overshoot and offer a basis for understanding its behaviour. The insights derived here lay the groundwork for new, theoretically sound approaches that do not optimise for a specific application but contribute to a broader understanding of the field's capabilities. This framework represents a step toward a more unified foundation in power electronics, guiding future advancements and the feasibility of UWBG technology.

1.3 Research Question and Motivation

The research questions are:

1) **How effective are existing voltage overshoot suppression methods?**

This question is further expanded as follows:

1.1) How can the effectiveness of an overshoot suppression method be fairly measured and compared?

As the voltage overshoot during turn-off is a very old problem in power electronics and a large field of investigation, several methods and techniques exist that are able to suppress the overshoot adequately. Even though all of these methods have their merit, it is not known if there is a specific method that is better than other methods or how to determine objectively which results are best, as these methods and results are never directly compared.

In this research, Chapter 2 analyses the basic mechanisms of existing methods, and Chapter 3 analyses the experimental results of these methods. It is found that in a standard overshoot suppression article, the experimental results *with* a suppression method are only compared to the experimental results *without* a suppression method of the same article, and never to other articles. The framework to be able to extract relevant data from these experimental results has been developed so that the experimental results of different articles can be compared. Several examples are processed, and the extracted data is analysed and compared. It is seen that some of these experimental results look very impressive when considered in isolation, but are not as impressive when compared to the experimental results that others are achieving.

1.2) When do the existing oscillation suppression methods become ineffective, and are there existing oscillation suppression methods that could be used in UWBG devices?

Existing oscillation suppression methods, while effective under current operating conditions, show significant limitations as the switching speed of WBG devices increases. Most methods

rely on minimising parasitic inductance through layout optimisation and packaging improvements. However, as WBG devices push switching speeds higher, the inductance cannot be reduced below nano-Henry levels without encountering physical constraints. Beyond these thresholds, suppression methods fail to adequately manage voltage overshoot, leading to several negative side effects. Additionally, the superior properties of UWBG materials enable even faster switching speeds. Current suppression methods are not designed to cope with the extreme conditions posed by these devices, necessitating new approaches that extend beyond the limits of existing solutions. Chapter 3 of this study critically evaluates where and why existing suppression methods cease to be effective and highlights what technique has the potential to be used in future UWBG devices. From this investigation, it is seen that only a method called Zero Overvoltage Switching (ZOS) is a good candidate for future UWBG devices, as it becomes more effective as the speed increases.

2) Can the fundamental limitation caused by parasitic inductance be overcome in fast-switching devices?

This question is further expanded as follows:

2.1) What is the fundamental interaction between the parasitics components and switching characteristics?

This research question is addressed in Chapter 4, where a fundamental time-domain model of the switching circuit is developed to explicitly account for the non-ideal characteristics of the switching device and the influence of parasitic components. Unlike conventional switching models that assume a fixed progression of circuit states, this work introduces a detailed mathematical framework that captures the dynamic interactions between device turn-off characteristics, parasitic inductances, and capacitances.

From the investigation, it is found that depending on the circuit parameters, the order in which the equivalent circuits progress during the switching event can change. This is particularly significant when the switching speed is high enough that the switching device turns off before the clamp diode conducts, leading to an alternative equivalent circuit progression. These findings provide a theoretical explanation for the unexpected behaviour observed in ZOS, reconciling its unexpected results with a broader understanding of switching dynamics. By explicitly modelling these effects, this work lays the foundation for a more general theoretical framework that accounts for conventional and high-speed switching results simultaneously. This new framework shows that the overshoot can be eliminated when switching very fast and when the parasitic inductance is not minimised.

2.2) If minimisation of parasitic inductance is not the main driver for overshoot, what is it?

Historically, the universal approach to suppressing voltage overshoot has been to minimise parasitic inductance, based on the long-held assumption that lower inductance directly reduces overshoot. This belief has shaped power electronics design for decades, driving advancements in circuit layout optimisation, packaging improvements, and device selection. However, the findings in this thesis provide a different dimension, demonstrating that minimising parasitic inductance is not always the dominant factor in controlling overshoot, particularly in high-speed switching conditions.

This question is addressed in Chapter 5, where the developed energy-based model reveals that the key to suppressing overshoot is not reducing inductance but achieving ideal energy values in the passive components at the moment the diode clamps. The modelling shows that when switching slowly, the system behaves as expected, with parasitic inductance being strongly correlated to the overshoot. However, at very high switching speeds (in excess of approximately 2 MHz of standard converters), a different mechanism emerges, where energy stored in the parasitic components can be balanced in such a way that overshoot is eliminated, regardless of the absolute value of the inductance. It is seen that the ideal energy value explanation is always true and explains why the parasitic inductance is so closely correlated with the overshoot when switching slow and but not when switching very fast.

2.3) Can the limitations of Zero Overvoltage Switching be overcome?

The investigations presented in Chapters 2–5 suggest that ZOS has the potential to overcome the limitations imposed by parasitic inductance, offering a fundamentally different approach to overshoot suppression at high switching speeds. However, despite this promise, ZOS is not a feasible solution in its current form due to two major drawbacks: it only works under ideal switching conditions and is limited to a very narrow set of circuit parameters. These constraints prevent its widespread applicability and make practical implementation challenging.

This issue is addressed in Chapter 6, where the mathematical model is updated to allow for a controlled turn-off of the switch by allowing for two turn-off current segments instead of one, providing greater control over the switching transition. The energy conditions derived in Chapter 5 are reformulated into an optimisation objective, demonstrating that if the turn-off current can be shaped and controlled with sufficient accuracy, the overshoot can be eliminated across a wider range of circuit parameters. This refinement significantly expands the feasibility of ZOS, showing that rather than being confined to ideal conditions, it can be adapted to operate effectively in more practical scenarios. These findings suggest that with further theoretical and technological advancements, ZOS could become a viable suppression method for next-generation high-speed switching devices.

1.4 Thesis Outline

This thesis is divided into chapters that address the research questions in Chapter 1.3.

Chapter 2 provides the background and fundamental workings and mechanisms of the voltage overshoot oscillation suppression methods that are currently being used in the academic literature.

Chapter 3 then further investigates these suppression methods by first providing the framework to extract relevant parameters from existing suppression articles so that the experimental results can be compared. These empirical results are then compared through various scatter plots, and the observations of their comparison are then discussed in detail. Tables containing the results are also presented. In this chapter, a method called ZOS is identified as a potential solution in a fast-switching environment.

Chapter 4 further investigates the unexpected results from ZOS by developing a fundamental circuit model of the turn-off switching transition in power electronics. Using circuit theory and Laplace transforms, a circuit model that explicitly models the parasitic components and the non-ideal turn-off of the switching device is derived. From the investigation, it is seen that alternative models will be applicable for fast-switching devices and slow-switching devices and for clarity, these different events are called *Fast-Mode* and *Slow-Mode*, respectively.

Chapter 5 then uses this model to provide a fundamental, energy-based mechanism of the voltage overshoot. It discusses the implications of having separate models for fast and slow switching and provides more fundamental knowledge and insights into the new understanding of fast-switching events.

Chapter 6 then further develops the model to allow for greater freedom in the turn-off event by allowing two segments in the turn-off event to emulate the controlled turn-off of the switch. This updated model is then able to provide the requirements to overcome the shortcomings of ZOS by allowing non-ideal switching and a wide window of circuit parameters where the overshoot can be eliminated.

Chapter 7 provides the conclusion of the research, which demonstrates that there is a theoretically feasible method to eliminate the voltage overshoot in fast-switching devices of the future, like UWBG devices, by the contribution of a unifying model.

1.5 Academic Contribution

The main contributions of this research are summarised as follows:

- Developed framework for to be able to compare the effectiveness of existing overshoot suppression methods from the literature, enabling objective benchmarking of experimental results across studies.

-
- Proposed a fundamental time-domain mathematical switching model that incorporates parasitic components and non-ideal turn-off characteristics, enabling the theoretical explanation of both conventional and unexpected ZOS switching events.
 - Demonstrated, through the mathematical model, that under very fast switching conditions, voltage overshoot can be eliminated not by minimising parasitic inductance, but by achieving an ideal energy condition at the instant the diode clamps.
 - Introduced a novel controlled turn-off mechanism using a two-segment turn-off current characteristic, which significantly expands the practical window of ZOS beyond the very narrow conditions required for ZOS conditions.

Chapter 2

Background

2.1 Introduction

With the problem of voltage overshoot and ringing of the switching node affecting all converters that attempt to increase the switching speed almost since the inception of the field of power electronics, a whole in-depth and evolving field has developed over the past few decades. In this field, several alternative and innovative oscillation suppression methods have been developed to enable faster-switching devices or lower the overshoot at existing speeds. This section investigates all the overshoot suppression methods that could be found to better understand the current technology and approaches. Investigating all these methods will also provide valuable insights into existing and future trends and will be able to provide the limitations of each method.

2.2 Existing Oscillation Suppression Methods

2.2.1 Minimisation of Parasitic Inductance

The primary cause of overvoltage is the resonance between the parasitic reactive components. Therefore, reducing parasitic inductance also reduces the overvoltage. Minimising the parasitic inductance is a prominent and efficient approach, primarily achieved through circuit layout optimisation, device selection and device packaging optimisation [30], [41], [51], [52].

Selecting devices with small package inductance can reduce the overall inductive effect within the circuit, already reducing the voltage overshoot. Specific examples can be seen in [41], [51]. The TO-263 package, which offers a 32% lower inductance compared to the TO-247 package, is chosen. This reduction in inductance translates to a 29% decrease in total per-cycle switching losses, contributing to enhanced overall efficiency. The advantages of this method lie in its simplicity and

ease of implementation, as no auxiliary circuits are required. However, the primary limitation is its relatively restricted ability to suppress oscillations completely.

Layout optimisation is a critical aspect of minimising parasitic inductance in general as proper PCB layout can significantly reduce the power loop inductance [36], [53], [54]. Examples of the optimisation process include using a double-sided PCB layout in the phase-leg circuit, which can reduce the power loop inductance to 0.1 nH [36]. These layouts often involve careful attention to component placement and trace routing to ensure minimal inductance in critical paths. The double-sided layout enables shorter connections between the power devices and reduces the loop area, further suppressing the parasitic induction [53]. While this method is advantageous in reducing oscillations without the need for additional components, it is not without challenges. Designing such an optimised layout can be complex and time-consuming, and it requires a deep understanding of the power converter's specific operating conditions and parasitic behaviours, but it is still possible. The technique also carries certain limitations, as it may not eliminate all oscillatory behaviours, necessitating the use of supplementary suppression methods in some cases [53].

Finally, the actual packaging of the semiconductor is also optimised by optimising the die design of the semiconductor and can be seen in [55]–[57] and is more modern than the other approaches. In this approach, complicated electromagnetic models of the die and substrate are developed and optimised, and very low inductance could be achieved.

As discussed above, although this method is obvious and has great results, the greatest drawback is that it is very difficult to improve further, and the inductance can never be reduced to zero.

2.2.2 Switching Slower

An effective approach to mitigate switching oscillations is to slow down the switching speed, primarily achieved through the use of gate resistors and gate driver design [58]–[61]. This technique reduces the di/dt and dv/dt stresses on the device, helping to alleviate voltage overshoot, oscillation and electromagnetic interference (EMI) during switching events.

Gate resistors are commonly added in series with the gate terminal of the power device to control the gate charge/discharge process. By introducing a larger gate resistor, the gate charge is delivered more slowly, thereby reducing the sharp transitions that cause oscillations. The trade-off, however, is that increasing the gate resistance can also result in increased switching losses due to the slower turn-on and turn-off times, which impacts the overall efficiency of the converter [53]. Additionally, increased heat would require additional cooling and could decrease the converter energy density. Therefore, selecting an appropriate gate resistor value is critical to balancing oscillation suppression with switching performance and efficiency. A well-designed gate

driver should provide sufficient drive strength to control the device without introducing excessive switching speed that could exacerbate oscillations.

2.2.3 Ferrite Beads

Ferrite beads are also commonly used to mitigate high-frequency oscillations in power electronic circuits. By inserting a frequency-dependent impedance into the circuit, ferrite beads effectively dissipate high-frequency energy, which helps reduce ringing and the associated voltage overshoot during switching events [59].

Their primary advantage lies in their ability to filter out high-frequency oscillations without significantly impacting low-frequency performance, making them well-suited for high-speed switching applications. Studies have shown that ferrite beads can lead to a reduction in peak voltage overshoot by over 25% and a decrease in the duration of ringing by more than 30%, contributing to overall system stability and reduced electromagnetic interference (EMI) [62], [63].

2.2.4 Snubber Circuit

Adding RC snubber circuits to suppress switching oscillations is a widely used method in power electronic systems [19], [43], [44], [62]–[72]. When considering parasitic parameters, the circuit can be simplified to a second-order RLC model to represent the parasitic ringing that occurs during the turn-on and turn-off transients of the switching device [19], [43], [44], [64]. This equivalent RLC circuit is depicted in Fig. 2.1(a). Based on this equivalent circuit, the parasitic ringing can be effectively modelled. To suppress the ringing, an RC snubber [43], [44], [73] or snubber capacitor C [19], [64] is commonly employed. Fig. 2.1(b) shows the equivalent circuit of parasitic ringing suppression with the RC snubber.

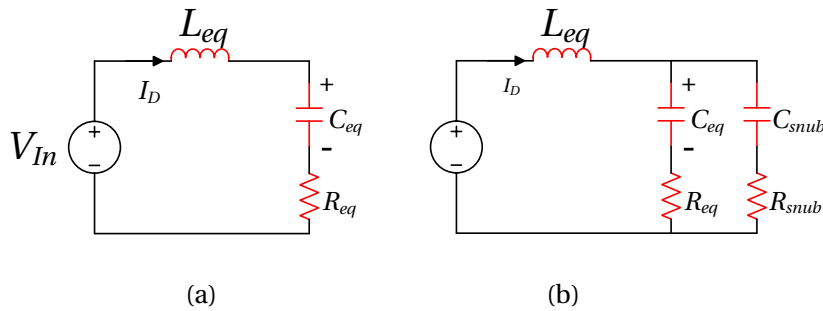


Fig. 2.1 Equivalent circuits of a switching node (a) without and (b) with a snubber circuit

A simple second-order design method for the RC snubber is discussed in [62], [63], [65], [66], where the specific parameters of the snubber can be calculated using the following formulas:

$$R_{\text{snb}}(s) = \frac{1}{2\zeta} \sqrt{\frac{L_p}{C_p}} \quad (2.1)$$

$$C_{\text{snb}}(s) = \frac{1}{2\pi R_{\text{snb}} f_r} \quad (2.2)$$

where ζ is the damping ratio, L_p is the parasitic inductance of the circuit, C_p is the parasitic capacitance of the device, and f_r is the oscillation frequency. However, this second-order design approach has limited effectiveness in fully suppressing parasitic ringing, especially when the circuit cannot be simplified to a second-order form.

When the circuit exceeds second-order behaviour, more advanced techniques are required. The second-order design method [62], [63], [65], [66] does not consider the segmentation of loop inductance caused by the additional current path of the snubber branch. To address this limitation, the root locus method is adopted for parasitic ringing suppression in [69]. In this method, the breakaway point of the characteristic equation is determined. The RC snubber values are designed so that all solutions to the characteristic equation are negative real numbers, effectively damping the oscillations. Simulation and experimental results show that this approach provides better suppression of parasitic ringing compared to the second-order method [69].

For higher-order systems, particularly when the damping ratio exceeds 0.4, the root locus method is still commonly used to analyse how varying C_{snb} affects system stability while keeping the snubber resistance fixed. By selecting an appropriate C_{snb} , the damping effect can be optimised to minimise unwanted oscillations. Experimental results confirm that within this design range, the RC snubber effectively controls oscillations, whereas suppression becomes less effective outside this range.

This design method achieves a satisfactory oscillation suppression effect for circuits up to the sixth order, providing valuable guidance for higher-order circuits. In addition, properly designed RC snubbers can fully suppress sustained oscillations in the drain-source voltage, as demonstrated in [74]. When the RC snubber is optimised for the circuit parameters, sustained oscillations are mitigated, leading to improved device performance and reduced stress during switching.

2.2.5 Active Gate Driver

Active gate drivers have also emerged as an effective suppression method. These designs focus on dynamically adjusting the gate current or voltage to control the dv/dt and di/dt during switching events, reducing oscillations and voltage overshoot. By managing the switching trajectory, active gate drivers help limit the stress placed on the switching devices without significantly increasing power losses. However, the use of active gate drivers introduces complexity to the circuit design and can incur additional costs for the external circuitry required to support the auxiliary circuits.

For instance, the active gate driver design in [75], [76] demonstrates this technique to minimise overshoot in SiC MOSFETs well, demonstrating a significant reduction in ringing amplitude by optimising the gate current during switching transitions. This research also displayed a significant reduction in switching losses, demonstrating the advantages of an active gate driver well.

[77] presents an advanced active gate driver operating at 6.7 GHz specifically developed for GaN FETs, capable of shaping switching waveforms with remarkable precision during sub-10-ns switching transients. Unlike traditional variable gate drivers, which typically alter a single parameter per switching event, this driver achieves a much higher timing resolution and output resistance variability. Utilising a 6.7 GHz update rate, the driver dynamically adjusts gate resistance across a range of 0.12 to 64 Ohm during switching. When tested in a 1 MHz bridge-leg converter with EPC2015 GaN FETs, the driver demonstrated a notable reduction in voltage overshoot, oscillations, and EMI, all while maintaining low switching losses. This design exemplifies how precise resistance modulation at sub-nanosecond intervals can beneficially shape GaN device waveforms, improving switching performance without compromising efficiency.

[78] proposes an active gate driver that utilises an open-loop control system that moderates gate energy by incrementally increasing gate resistance during the Miller plateau region of the gate-source voltage. This approach smooths the turn-on and turn-off transitions, minimising overshoot, oscillations, and switching losses, all without worsening EMI. The driver's design allows for independent control over turn-on and turn-off events, making it well-suited for high-speed SiC applications with asymmetrical power supplies. Experimental validation at high frequencies confirmed the active gate driver's effectiveness, demonstrating that the driver successfully mitigates parasitic effects while supporting high-efficiency, high-density power systems.

[79] presents an active gate driver designed to drive high-power SiC MOSFETs across varying temperatures and load currents. The active gate driver developed reduces the drive voltage during the voltage and current slope intervals, effectively minimising dv/dt and di/dt . Additionally, the optimal drive voltage switching delay time is calculated to strike a balance between switching losses and stresses. Experimental testing on 1.2 kV/300 A and 1.7 kV/300 A SiC MOSFETs confirmed that this active gate driver successfully limits overshoot, oscillations, and switching losses without negatively impacting EMI. The article also includes an EMI and cost analysis, demonstrating that active gate drivers can also work very well for high-power applications.

[80] introduces a three-level active gate driver tailored for SiC power MOSFETs. The active gate driver implements a multi-level approach that adjusts switching losses against dv/dt and di/dt rates in each transient. This design also offers a notably shorter turn-off delay by applying a three-level turn-off profile, which is optimised in real-time using a datasheet-driven model for switching trajectory. Validation through double pulse tests confirmed the performance of the active gate driver in reducing turn-off delays, switching stresses, and overall EMI. The experimental

results underscore its advantages over both conventional and two-stage gate drivers, making it a competitive solution for high-speed SiC applications requiring precision switching control.

Active gate drivers are considered a "research hotspot" because of their effectiveness and flexibility. The full extent to which active gate drivers can be implemented is still unknown, but it is a promising approach. While these active gate driver techniques offer significant benefits in controlling switching speed and suppressing oscillations, they greatly increase the complexity of the circuit in terms of extra components and control. Additionally, even though the gate voltage, current or resistance can be controlled, it is difficult to derive the ideal gate sequence so that the oscillation is minimised, and also what the minimum overshoot actually is. This leaves much uncertainty as to the best solution or if an active gate driver has reached its full potential.

2.2.6 Zero Overvoltage Switching

All the existing oscillation suppression methods mentioned above represent improvements based on well-established concepts and extensive research.

Another oscillation suppression method, known as Zero Overvoltage Switching (ZOS), is outside of this collection of knowledge and was first introduced in [81]. This solution challenges mainstream assumptions and represents a departure from the two primary approaches of decreasing switching speed and decreasing inductance. Instead, ZOS simultaneously increases switching speed and inductance, leading to surprising and unexpected results of voltage overshoot reduction.

When the circuit in Fig. 1.2 is considered, and the assumption is made that the switching event is ideal, the optimisation equation in Eq. (2.3) would lead to the elimination of the overshoot as seen in Fig. 2.2.

$$I_{in} = V_{out} - \frac{\sqrt{\frac{8C}{L_{Par}}}}{(2n-1)\pi} \quad (2.3)$$

In this equation, C is the capacitance of the top switch and bottom switch, assuming they are the same, L_{Par} is the power loop parasitic inductance, I_{in} is the input current, and V_{out} is the output voltage. The overshoot will be eliminated when these four variables are exactly correct according to the equation, and the switching speed is almost ideal. The n in the equation indicates that this ratio will recur at different values of n . It is important to note that the values or the variable must be at the correct values, and not at a minimum, for this method to work, removing the need to minimise the parasitic inductance.

In Fig. 2.2, the transition period is very small (or almost ideal), and it can be seen that no overshoot and ringing occur, which is contrary to the expected results. Additionally, these results were experimentally verified in [82] and [83].

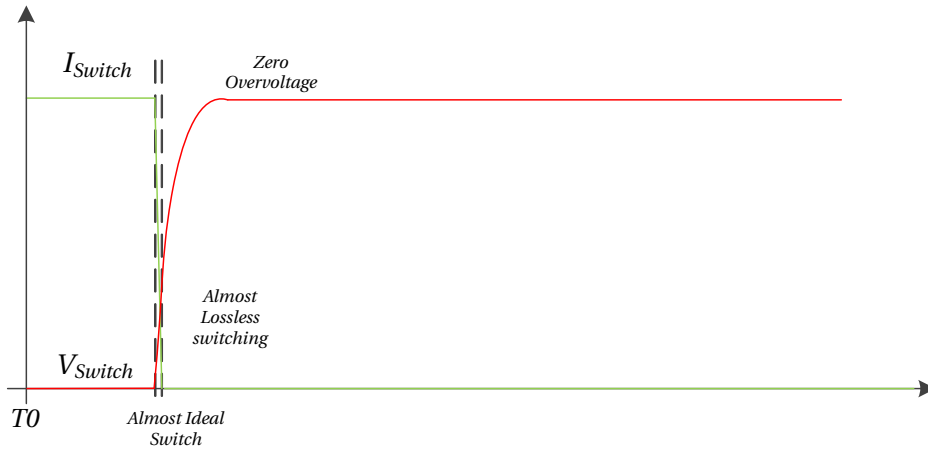


Fig. 2.2 Voltage overshoot of optimised ZOS

Compared to the other suppression methods, this method becomes more effective as the switching speed increases, but not less effective as the others do. As such, this method is not limited by the physical constraints to minimise the inductance to achieve optimal results, but rather the correct values according to the optimisation equation need to be achieved for optimal results. So, even though this method is still sensitive to the values of parasitic components, the values do not have to be minimised, which suggests that it holds promise as an effective suppression method.

Despite this potential, ZOS has not gained widespread recognition, as there has not been much work in this area.

It is expected that ZOS has not lived up to its mainstream potential thus far for two main reasons. The first is that ZOS is only possible in a very narrow window, and a small deviation of any of the circuit parameters from the optimal values calculated from Eq. (2.3) creates a very large overshoot, making the argument for implementing ZOS difficult as seen in [84] and [85]. This equation also assumes an ideal switching event, which is not possible, so implementing ZOS on a slow switching circuit would also cause a very large overshoot.

Secondly, the theoretical underpinnings of ZOS are not well established, making the fundamental understanding of the underlying mechanism difficult to comprehend, even for experts in the field of power electronics. Therefore, even though experts might read about this method, it does not make sense easily unless it is explained very well.

However, the fact that this method is not bound by minimisation of parasitic inductance, no matter how complicated it is, does warrant further investigation, as it might hold the key to a step in the direction of fast-switching beyond WBG devices.

2.2.7 RC Clamping

RC Clamping is also an alternative suppression method that has not gained widespread recognition. This method involves employing passive components such as capacitors, resistors, and diodes to mitigate the parasitic oscillations that occur due to the fast switching characteristics of WBG devices. The fundamental principle behind clamping is the use of a clamping capacitor to clamp the excess voltage during switching transients, preventing voltage spikes that could damage the switching devices.

An example of a simple circuit from derived in [86] can be seen in Fig. 2.3 below:

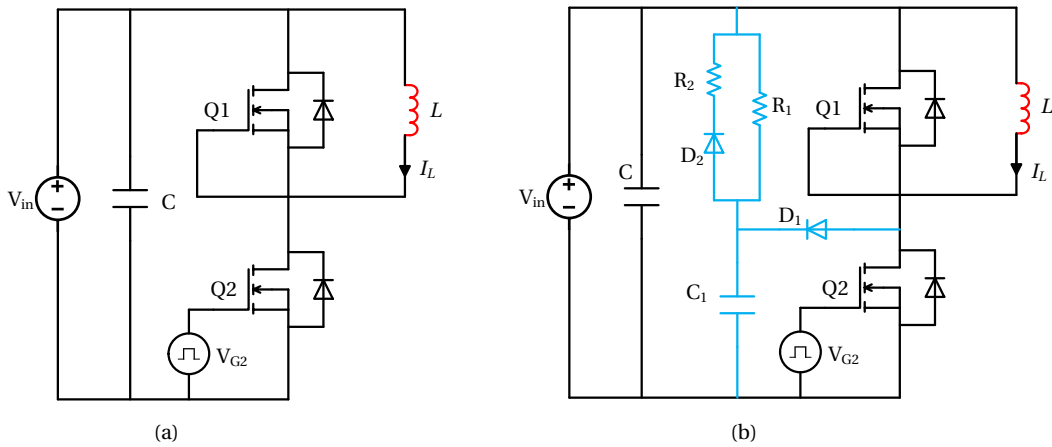


Fig. 2.3 Circuit diagram of (a) double pulse test set-up and (b) simple clamping components added (adapted from [86])

In this image, the additional passive components can be seen in blue. When $Q2$ turns off and the drain-source voltage of $Q2$ begins to rise, the clamping capacitor absorbs the overvoltage caused by parasitic resonance, effectively suppressing the oscillations. This design uses only a few passive components, such as capacitors and diodes, to keep the clamping circuit simple. Experimental results show that this method reduces voltage spikes by 43.3%, all while maintaining efficiency by not introducing additional switching losses, making it a highly effective solution.

The method described in [87] takes the clamping concept a step further by introducing an energy feedback mechanism. In this design, the energy stored in the clamping capacitors during the turn-off transient is fed back into the system after the transient period ends. This circuit operates by turning on a diode when the drain-source voltage exceeds the bus voltage, allowing the clamping capacitor to absorb the overvoltage and store the excess energy. After the turn-off event, this energy is released back into the system, further reducing overall switching losses. In experiments, this clamping method reduced switching losses by 30.3% at 450V compared to conventional circuits and by up to 54% at 150V. This approach ensures a significant reduction in oscillations while improving efficiency.

The method in [86] is simple to implement, relying on basic passive components, which makes it cost-effective and easy to integrate into existing systems. It provides significant oscillation suppression with minimal impact on switching losses, offering a reduction in voltage spikes without compromising the switching speed. The method in [87], while slightly more complex, provides the additional benefit of energy feedback, further enhancing the system's efficiency. This method reduces total switching losses significantly, with experimental results showing reductions of 30.3% to 54%, depending on the operating voltage used in the testing circuits.

However, as with all the methods with passive components, the method will lose effectiveness if the values of the passive components are not chosen effectively, and there is additional complexity with the added components. Additionally, this method is still susceptible to parasitic inductance as the switching speed increases.

2.2.8 External RLC Resonator

External RLC resonators for suppressing switching oscillations in SiC MOSFETs have been explored in [88]. This is the only available article that discusses clamping in detail for SiC devices through the use of a strongly coupled external resonator. The focus of this approach is to suppress parasitic ringing through the use of an RLC resonator coupled magnetically to the main power circuit rather than directly inserting passive components into the switching path, and a simplified circuit diagram indicating the resonator to the power loop can be seen in Fig. 2.4

The resonator is implemented in parallel with the bus bar of the main circuit, allowing strong magnetic coupling to transfer the ringing energy into the external resonator effectively. Using this method, the system can achieve significant ringing suppression without directly impacting the main switching components. The authors demonstrate through both experimental and simulation data that their resonator design can reduce peak voltage ringing to 15% of the original amplitude [88]. This is achieved by tuning the resonator's resistance and inductance values, ensuring the resonant frequency of the external resonator matches that of the parasitic oscillations in the main circuit. Experimental results showed that the resonance frequency stabilises when the resistance value reaches around 5.3 Ohm, which was found to be the optimal value for maximum damping in their setup. Additionally, this method provides minimal impact on switching losses, with measurements indicating that switching loss differences between configurations with and without the external resonator were negligible.

While this method offers significant advantages, particularly in terms of suppression of ringing and minimal interference with the primary circuit, it does have some limitations. The strength of the magnetic coupling between the main circuit and the external resonator must be carefully optimised. If the coupling is too strong, too much energy might be pulled from the main circuit into the resonator, potentially causing over-damping, energy loss, or even new oscillatory behaviours that reduce the effectiveness of the intended suppression. Conversely, if the coupling is too

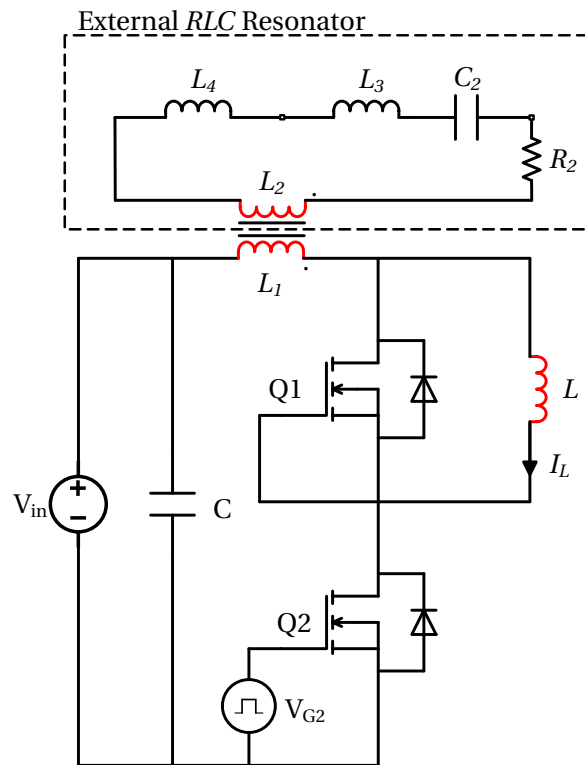


Fig. 2.4 Circuit diagram of double pulse test setup with RLC resonator (adapted from [88])

weak, insufficient energy will be diverted to the resonator, making it ineffective at damping the oscillations. Additionally, the external resonator requires careful design to ensure that its resonance matches the parasitic elements of the main circuit, necessitating additional design complexity.

Chapter 3

Experimental Performance Comparison of Oscillation Suppression Methods

This chapter is adapted from the following publication:

E. P. D. Toit and I. W. Hofsajer, 'A Review of the Experimental Performance of Turn-Off Methods in Wide Bandgap Semiconductors', *IEEE Open Journal for Power Electronics*, vol. 5, pp. 1671-1683, 2024, doi: 10.1109/OJPEL.2024.3478178.

The author of this thesis conceptualised the study, conducted the analysis, developed the models, and wrote the original draft of the paper.

3.1 Introduction

This overvoltage and ringing phenomenon has been a problem in power electronics for a very long time, and as seen in Chapter 2, over the past few decades, much research has gone into almost all aspects of this problem. As such, there is a vast amount of research articles detailing methods to suppress voltage overshoot and ringing. As the academic field of suppression techniques for overvoltage and ringing has evolved over time, a generic structure of a typical article on overvoltage and oscillation suppression methods in the literature has developed. The structure that almost all the historic and modern articles generally follow is outlined in Table 3.1.

Table 3.1 Typical structure of suppression articles

Section	Content of section
1	Introduction
2	Analysis of some new oscillation suppression methods
3	Simulation results
4	Experimental results
5	Comparison of experimental results with and without suppression method
6	The conclusion was that the suppression method implementation was successful as the overshoot decreased from experimental results without the suppression method to the results with a suppression method

In this standard structure of a suppression article, the conclusion is generally made that the research is successful as the experimental results *with* the suppression method have a lower overshoot than the results *without* the suppression method. However, these results are never directly or indirectly compared to other experimental results from other articles using the same or different suppression methods. It is understood that it is very difficult to compare these experimental results to others, as there are several factors that are not accounted for that can skew the comparison. Additionally, the lack of comparison might also be a symptom of the piece-wise and fractured nature of the research of power electronics.

Nonetheless, with the lack of comparison, the actual relevance of the results is unknown, as they are not placed in the context of other experimental results in the field and contribute to the fractured nature of power electronics. Generally, at best, some individual factors like inductance may be compared to a single other article. The experimental results of a suppression method might seem like good results when the overshoot has decreased by a large percentage, but it is possible that even the successful results might still be worse than the results other researchers are achieving, even if their percentage reduction is less. As there is no comparison with other reported results, it is difficult to decide whether to continue to develop and refine a specific method or if some other method offers better performance.

As this research attempts to determine which of the oscillation suppression methods discussed in Chapter 2 holds the most promise in a high-speed switching environment, this chapter develops the framework so that the experimental results of oscillation suppression methods can easily and objectively be compared. It does so by extracting the relevant comparable information from previously reported experimental results. These experimental results are then compiled in a database from which the data can be interpreted from several different viewpoints, and these different viewpoints are discussed in this chapter. Other researchers can also use this database to easily compare their new experimental results with multiple previous experimental results.

3.2 Experimental Results Parameter Extraction Methodology

An article that describes an overvoltage and oscillation suppression method will normally show the waveforms of the switching devices both before and after the implementation of the method. These experimental results contain the information of interest. Unfortunately, the results are normally only presented as oscillograms in the papers, and there is no other access to the waveform data. The relevant information presented in the various waveforms needs to be extracted, and the methodology used to process the published oscillograms is discussed in this chapter.

3.2.1 Research Articles included in this study

The articles included in this study were any and all that could be found that presented an overvoltage and oscillation suppression method, focusing on the past five years. Only well-cited papers older than five years were also included.

Of these articles mentioned above, the main requirement for a paper to be included was that the turn-off voltage waveform had to be presented explicitly to extract the data. This means that the actual turn-off voltage waveform, zoomed in to show only one turn-off event and with division sizes, had to be presented. During this investigation, it was found that several of the oscillation suppression methods articles presented in Chapter 2 do not present the experimental results in this manner. Nonetheless, as many as possible were included.

3.2.2 Extracted Data Points

When the turn-off switching transition of a switch is considered, several characteristics can be extracted, and to ensure fairness and consistency in the comparison, all the results have been extracted in the same way.

The main data relevant to this study that could be extracted and subsequently compared from the experimental results waveform are:

1. **Voltage Overshoot Percentage [%]** - This is the percentage of how much larger the maximum voltage is over settling DC voltage after the oscillation has subsided.
2. **Voltage switching speed or slew rate [V/ns]** – this is the average rate at which the voltage over the switch progresses from 10% to 90% of the full voltage range.
3. **Power loop inductance [nH]** – this is the experimental power loop parasitic inductance measured indirectly from the switching oscillation frequency.

The voltage overshoot percentage is used instead of the actual overshoot to compensate for the differences in DC voltage, and the average switching speed from 10% to 90% is used for the

same reason. These three data points are then compared to each other at the same time to be able to make an objective conclusion on the effectiveness of a specific result.

It must be noted that weighting factors could be added in this comparison step. However, weighting factors could very easily cloud the comparison of the empirical results and are not part of the scope of this research. Other researchers can, in future, add weighting factors to these results and investigate if the results could be improved.

These three data points mentioned above cannot be simply read from the plots provided in the papers, and the published oscillograms needed to be digitised before the values could be calculated. Additionally, the experimental results, both with and without a suppression method, were processed where possible.

3.2.3 Data Extraction Example

The example of the step-by-step methodology is discussed below using [59], where a standard gate resistor is implemented to switch slower and thereby suppress the overshoot and oscillation. Even though the example is presented for a SiC semiconductor, exactly the same process is relevant to GaN devices as well.

Step 1: Digitise the waveform from a high-definition IEEE Xplore image.

In this step, the voltage waveform, presented in as high-definition as possible, is converted to a digital waveform by plotting data points on the graph. Software that can convert multiple points to x and y coordinate values was used to assist in this process. The image of how the experimental results are presented in [59] can be seen in Fig. 3.1 before digitisation, and the image after digitisation can be seen in Fig. 3.2.

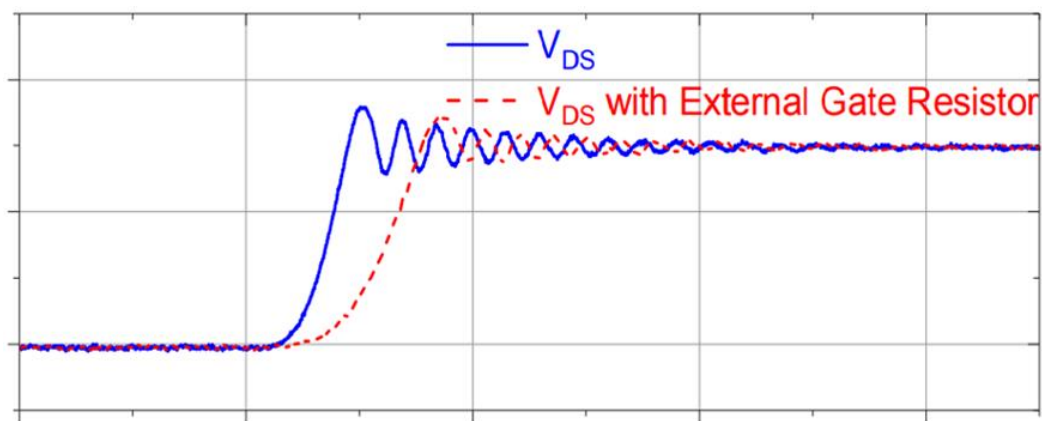


Fig. 3.1 Example of turn-off waveform that can be digitised (Extracted from [59])

A manual data sample check is also performed in this step to verify the integrity of the data. For clarity, only the result without the suppression method will be discussed further.

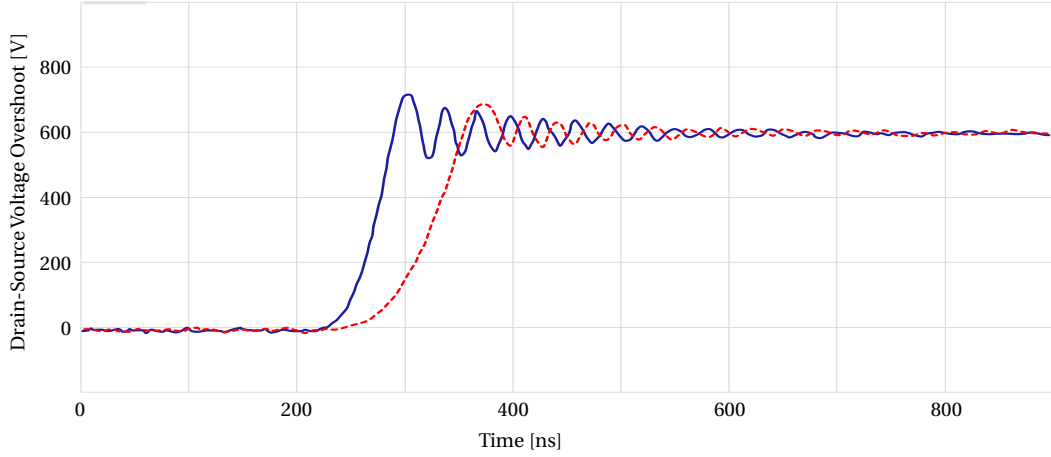


Fig. 3.2 Example of turn-off waveform after digitisation

Step 2: Voltage overshoot percentage calculation

For this step, three new values are defined to be able to calculate the percentage voltage overshoot, and they are as follows:

1. Average Voltage Before Switch - V_{Before}
2. Average DC settling Voltage after Switch - V_{DC}
3. Maximum Voltage - V_{Max}

These values can be seen in Fig. 3.3 and are then used to calculate the percentage voltage overshoot in the equation below:

$$\%OS = \frac{V_{Max} - V_{Before}}{V_{DC} - V_{Before}} \times 100 \quad (3.1)$$

In this equation, the difference between V_{Before} and V_{DC} has to be used to determine the DC voltage instead of simply using V_{DC} . This is because several articles present the voltage plot without the 0V indication directly from an oscilloscope and only with division markers, so the plot has to be compensated for a revised 0V indication.

Step 3: Average switching speed (average slew rate) calculation

After the overshoot has been calculated, the average switching speed or slew rate can be calculated. This is performed from 10% to 90% of the V_{Before} to V_{Max} and is done to calculate the speed of the entire range of the switching event. If the 10% to 90% of V_{Before} to V_{DC} was chosen to calculate the average switching speed, switching events with large overshoots would have seemed to perform better as the slow part of the switch was not included in the assessment area. This step can be seen in Fig. 3.4.

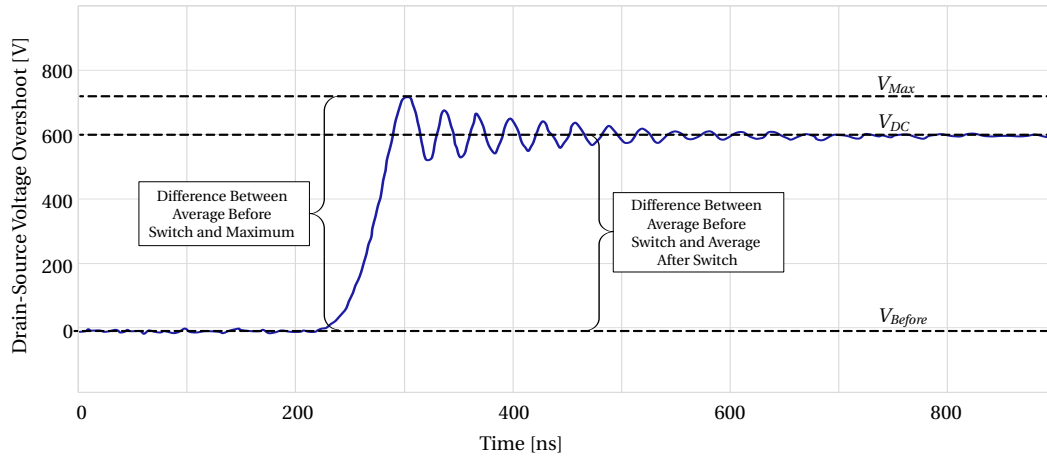


Fig. 3.3 Example of the extraction of relevant parameters to calculate the percentage voltage overshoot (only shown for results without suppression method)

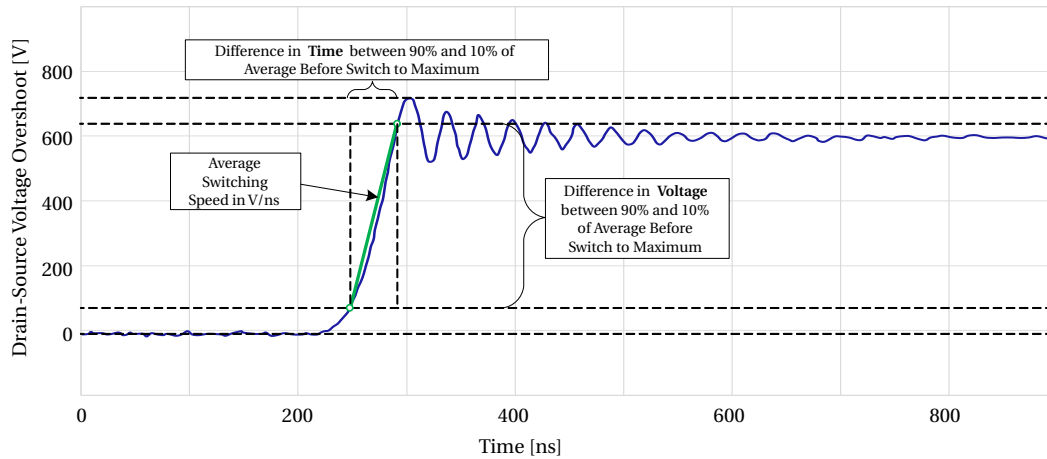


Fig. 3.4 Example of the extraction of relevant parameters to calculate the switching speed

Firstly, voltage values of 10% and 90% need to be calculated. As the calculated voltage would fall between two data points of the digitisation process, the assumption is made that the voltage progresses linearly between these two points as they are close enough together. The slope between the points can be used to calculate the corresponding voltage and time stamp for the 10% and 90% values for both the results with and without a suppression method.

Step 4: Power loop inductance calculation

The power loop inductance can be calculated from the ringing frequency of the voltage waveform if the circuit capacitance is known. For this step, the ringing period is found. This is done by extracting the period from the first trough to the second trough of the voltage waveform, as seen in Fig. 3.5.

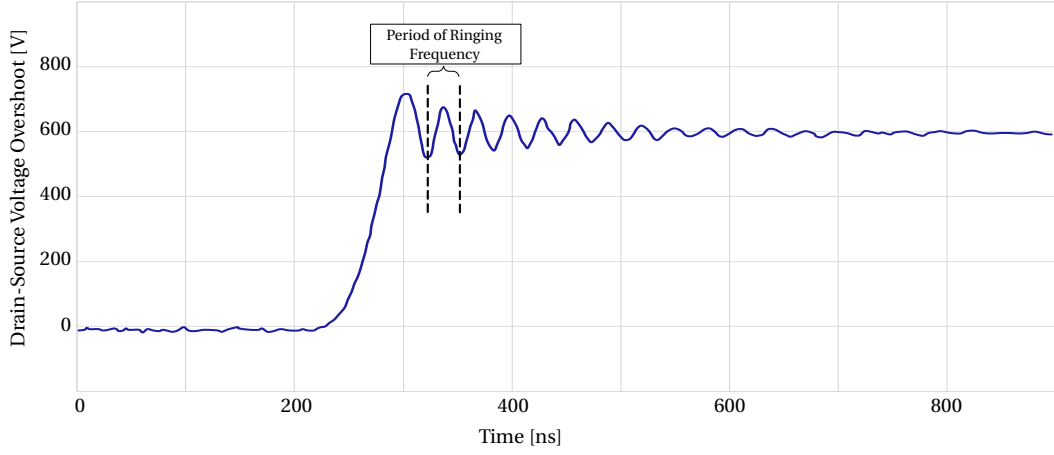


Fig. 3.5 Example of ringing period extraction to calculate parasitic inductance

It was found that using the first and second troughs leads to the most reliable indication of the ringing frequency. Thereafter, the capacitance of the power loop is required. This is the output capacitance (C_{OSS}) of the C_{Bot} value seen in Fig. 1.2, which is part of the resonant circuit. This value can be read from the datasheet of the device used in the experiment. In this case, the SiC MOSFET SCT3040KL is used, and using the settling voltage, the capacitance can be read from the datasheet of the respective manufacturer. For the purposes of extracting the power loop inductance, the device capacitance was considered linear. Other contributing factors to the overall capacitance were neglected, as it was assumed that the device capacitance dominated.

Using the method and equation from [54], the inductance can be calculated with the Equation 3.2 below:

$$L_{Loop} = \frac{T_{Ring}^2}{4\pi^2 \times C_{OSS}} \quad (3.2)$$

where L_{Loop} is the power loop inductance, T_{Ring} is the period of the oscillation frequency, and C_{OSS} is the output capacitance of the switch.

3.3 Experimental Results Presentation

Using the method described in Chapter 3.2, all the articles that met the requirements were processed for both the before and after suppression method implementation. The data points are recorded in Table 3.2.

Additional notes on this table include:

1. Where only results with a suppression method were presented in the research paper, the results without a suppression method section are left blank in the table.

2. In comparison plots in Chapter 3.4, only the final results where the suppression method had been implemented are presented.
3. Where the inductance is measured in the results without a suppression method, it is not repeated in results with a suppression method.
4. Several references present more than one oscillation suppression method result, so more than one data point could be extracted.
5. In [54], no oscillation suppression method is implemented, as this paper only presents a method to calculate and confirm parasitic inductance. However, this article does present an additional data point.

Table 3.2 Oscillation Suppression Methods Comparison

Paper Title	Publication Acceptance Date	Method of Suppression	Transistor Material	Switch Model	Results Without Oscillation Suppression Method					Results With Oscillation Suppression Method					Change in Switching Speed Percentage	Change in Overshoot Percentage
					Settling Voltage [V]	Voltage Overshoot %	Power [W]	Switching Speed [V/ns]	Inductance [nH]	Settling Voltage [V]	Voltage Overshoot %	Power [W]	Switching Speed [V/ns]	Inductance [nH]		
[55]	10/01/2022	Minimisation of Parasitic Inductance (Packaging)	GaN	GS-065-060	-	-	-	-	-	419.2	4.60%	10479.8	44.6	1.2	-	-
[56]	2/01/2022	Minimisation of Parasitic Inductance (Packaging)	GaN	GS-065-150-1-D	-	-	-	-	-	386.8	8.00%	34814.6	43.1	4	-	-
[57]	6/01/2021	Minimisation of Parasitic Inductance (Packaging)	GaN	S66508D	-	-	-	-	-	289.8	9.20%	8113.1	106.4	1	-	-
[36]	4/01/2014	Minimisation of Parasitic Inductance (PCB Layout)	GaN	EPC2015	11.4	105.80%	228.9	10.6	1.5	11.7	23.10%	234.8	9.7	0.3	-82.60%	-8.00%
[53]	8/01/2016	Minimisation of Parasitic Inductance (PCB Layout)	GaN	EPC2015	13.6	55.00%	108.9	6.6	1	13.7	6.50%	109.3	5.3	0.1	-48.50%	-20.30%
[52]	11/01/2021	Minimisation of Parasitic Inductance (PCB Layout)	GaN	GS66508T	-	-	-	-	-	200	2.90%	3880.3	33	0.6	-	-
[59]	9/01/2018	Slower Switching (Driver)	SiC	SCT3040KL	603.6	19.60%	6035.8	12.5	209.4	605.7	13.50%	6056.9	6.2	-	-6.00%	-50.00%
[59]	9/01/2018	Slower Switching (Gate Resistor)	SiC	SCT3040KL	603.6	19.60%	6035.8	12.5	209.4	606.4	14.70%	6064	7.4	-	-4.90%	-40.80%
[61]	10/01/2022	Slower Switching (Gate Resistor)	SiC	C2M0080 120D	299.1	40.20%	3888.3	13.3	438.7	301.3	27.00%	3916.4	4.8	-13.20%	-63.70%	
[59]	9/01/2018	Ferrite Bead	SiC	SCT3040KL	603.6	19.60%	6035.8	12.5	209.4	604.4	16.30%	6044.2	12.3	-3.30%	-1.40%	
[76]	12/01/2017	Active Gate Driver	SiC	SCH2080KE	373.3	48.00%	2241.0	18.1	500.1	373.6	10.00%	2241.6	7.1	-38.00%	-60.70%	

Table 3.3 Oscillation Suppression Methods Comparison (Cont')

Paper Title	Publication Acceptance Date	Method of Suppression	Transistor Material	Switch Model	Results Without Oscillation Suppression Method					Results With Oscillation Suppression Method					Change in Switching Speed Percentage	Change in Overshoot Percentage
					Settling Voltage [V]	Voltage Overshoot %	Power [W]	Switching Speed [V/ns]	Inductance [nH]	Settling Voltage [V]	Voltage Overshoot %	Power [W]	Switching Speed [V/ns]	Inductance [nH]		
[77]	1/03/2017	Active Gate Driver	GaN	EPC2015	11.7	29.40%	58.60%	5.8	0.7	11.9	3.00%	59.6	4.6	-	-26.4	-20.3%
[78]	6/01/2017	Active Gate Driver	SiC	SCT2080KE	414.7	52.40%	3317.6	18.9	420	412.9	11.50%	3303.6	12.9	-	-40.90%	-31.90%
[61]	10/01/2022	Active Gate Driver	SiC	C2M0080 120D	300.2	30.10%	3902.2	13.3	438.7	302.1	24.70%	3927.5	10	-	-15.40%	-24.70%
[59]	9/01/2018	Snubber (RC)	SiC	SCT3040KL	603.6	19.60%	6035.8	12.5	209.4	605.9	19.00%	6059.5	12.3	-	-0.50%	-1.60%
[73]	11/01/2021	Snubber (RC)	SiC	C2M0080 120D	406.9	58.80%	7730.7	29.9	220.2	405.1	53.30%	7696	30	-	-5.40%	0.30%
[72]	6/01/2022	Snubber (CRC)	SiC	C2M0025 120D	415.1	40.80%	8302.7	40.7	232.4	413.9	23.70%	8278	22.7	-	-37.30%	-44.20%
[81]	12/01/2018	Zero Overvoltage Switching	SiC	C2M0025 120D	401.7	23.40%	19283.8	11.3	43.6	399.2	8.70%	27144.9	19.8	-	-15.60%	75.90%
[83]	12/01/2022	Zero Overvoltage Switching	SiC	FS03MR12 A6MA1B	801.9	23.30%	157969.8	20.3	25.8	793.5	4.10%	156328.2	46.8	-	-19.20%	130.90%
[86]	12/01/2023	Clamping (RC)	SiC	C2M0080 120D	306.3	52.90%	9188.6	26	88.5	304.9	16.70%	9147.6	23	-	-36.20%	-11.40%
[87]	8/01/2021	Clamping (RC)	SiC	IMW120R 45M1	572.4	45.30%	22896.6	45.3	179.9	565.8	16.70%	22630	42.6	-	-39.70%	-6.10%
[88]	8/01/2020	External RLC Resonator (RC)	SiC	CAS120M12 BM2	404.8	23.50%	16193.7	4.9	103.8	405.8	23.70%	16230.6	4.8	-	0.20%	-1.30%
[54]	4/01/2018	None - Determination of Parasitic Components	GaN	EPC2010C	-	-	-	-	-	51.2	54.40%	512.5	21.9	1.4	-	-

3.4 Experimental Results Discussion

This section analyses, interprets and discusses the data extracted from all the articles in Table 3.2.

When interpreting the values from the table, it is important to keep in mind that the experimental results represented in the table were done under different circumstances, with different applications, different operating conditions and varying engineering rigour. This means that the data must be interpreted very carefully. However, viewing a sufficient number of data points gives insight into the trend of progress in the field.

In this chapter, the data from the table are analysed in three ways: Firstly, to show the influence of different suppression methods on the overshoot and device switching speed. Then, the influence of the operational characteristics such as the switching voltage and parasitic inductance, and then lastly, the trend towards faster switching speeds over the past decade. Scatter plots of all of the data points are presented so that the investigation can be viewed holistically.

Unfortunately, when large amounts of data in varying comparisons are viewed, it might become confusing to interpret, so special attention is given to presenting the results in as easy to understand way as possible. So, for each of the data points plotted in this section, the colour and marker shapes show the suppression method, and each of the axes is labelled. Each data point is labelled with the reference from which it was extracted and the y-axis variable. No distinction is made between GaN and SiC results. A simplified key to reading the scatter plots can be seen in Fig. 3.6.

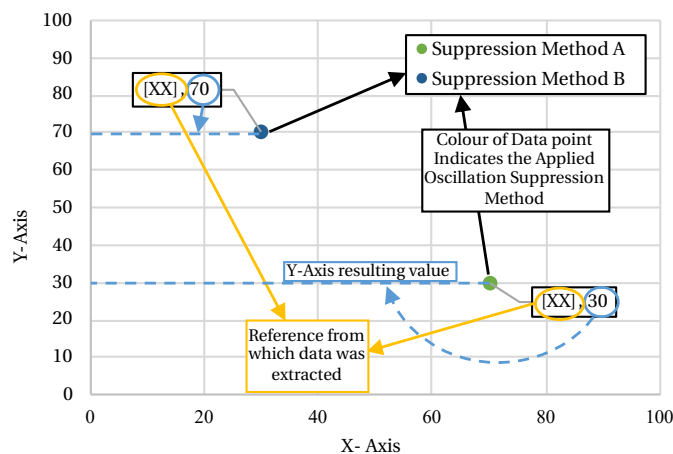


Fig. 3.6 Example of the presentation of the experimental results scatter plots

3.4.1 Comparison of Oscillation Suppression Methods

Percentage Overshoot versus Switching Speed

The first section is the direct comparison of the voltage overshoot percentage and the switching speed in V/ns. This comparison allows the results of a single article to be compared with all the other articles. This is shown in Fig. 3.7.

The voltage overshoot percentage is used instead of the actual overshoot to compensate for the differences in DC voltage, and the average switching speed from 10% to 90% is used for the same reason. This comparison could be thought of as the simplest and fairest.

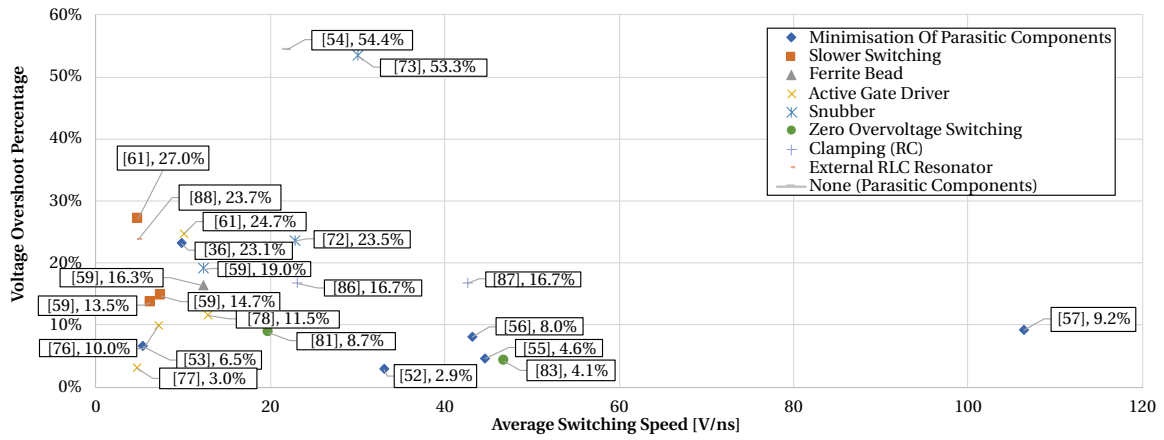


Fig. 3.7 Scatter plot of voltage overshoot percentage versus average switching speed

It is generally accepted that fast switching speeds lead to large overshoots. Therefore, a fast switching speed with a low overshoot is seen as a more successful implementation of a suppression method. This is seen in the outlier of [57] in Fig. 3.7. Conversely, the outlier of [73] shows a less effective suppression method as the switching speed is relatively slow and the overshoot percentage is substantial.

It can be seen that some of the suppression methods cluster together. For example, the active gate driver [76], [78], [77], [61] and the slower switch of [59], [61] and the parasitic reduction methods of [52], [55], [56]. While there is no definitive pattern emerging, the parasitic reduction methods show good performance in this view of the results. In particular, the apparent exceptional performance of [57] bears closer scrutiny. However, it is not within the scope of the current paper to delve into possible reasons for this high performance. The data presented in Fig. 3.7 allows new suppression methods to be compared to the existing ones. In this way new results can be more readily interpreted as to their effectiveness.

Change in Overshoot versus Change in Switching Speed.

In many articles, the implementation of a suppression method is contrasted against the same circuit without the suppression method present. In all cases the suppression method is shown to increase the performance of the circuit. To capture this type of result, the percentage change in overshoot is plotted against the percentage change in switching speed, shown in Fig. 3.8. To interpret this plot, consider first the three orange clustered points of [59] and [61], representing the suppression method of slower switching. As is known, slower switching speeds lead to lower overshoots. As almost all suppression methods sacrifice switching speed to reduce the overshoot, the other method's results can be compared to the slower switching method to determine their relative success.

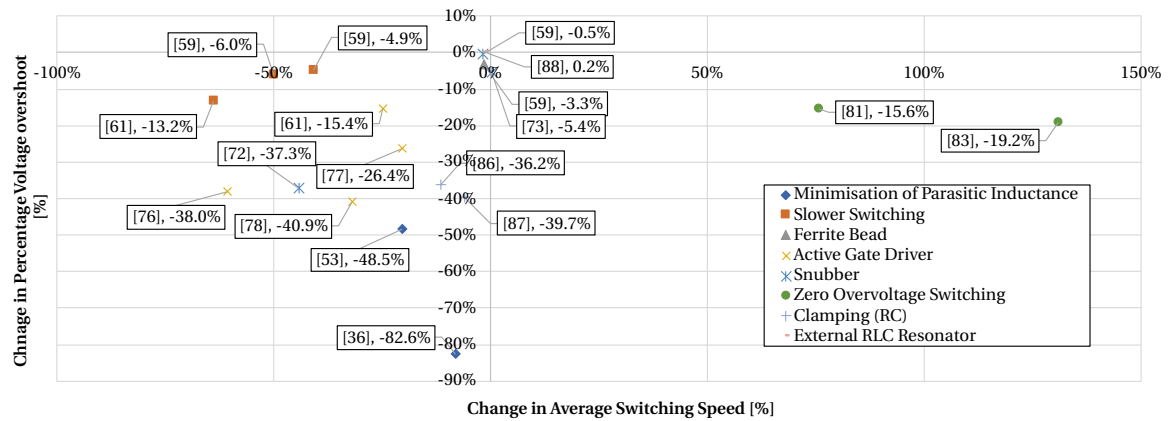


Fig. 3.8 Scatter plot of change in percentage voltage overshoot versus change in switching speed from results without suppression method to results with a suppression method

However it can be seen that the ZOS method has the characteristic that it increases the switching speed and reduces the overshoot, against conventional expectations. This indicates that this method might be well-suited to handle future fast-switching devices.

One of the main findings of the comparison plots of Fig. 3.7 and Fig. 3.8 shows that scoring well in the change measurement Fig. 3.8 does not automatically imply that the result compares well overall, as was discussed in Chapter 3.1. Even though a given experimental setup might benefit greatly from a suppression method, the overall result still might not compare well with other methods.

An example of this can be seen in [36], where the inductance is minimised. In this result, when only the overshoot reduction percentage is compared to the sacrifice in switching speed in Fig. 3.8, an overshoot reduction of 82.6% is achieved, and only 8% switching speed is sacrificed, which could be considered a very good result. However, when the resulting actual switching speed is compared to the actual overshoot of [36] as in Fig. 3.7, and is compared to other results, it has a

relatively slow switching speed and a relatively large overshoot, making the final result within the context of other results much less impressive.

Conversely, if a result like [57], which is switching very fast with a low overshoot, as compared to others, can be improved only marginally, the improvement itself would be unimpressive if measured in the "change in percentage overshoot versus change in percentage speed" metric, but the actual result would be exceptional, as the actual boundaries of the field are being pushed.

3.4.2 Influence of Circuit Parameters

Influence of inductance on overshoot and switching speed.

It is well known that the parasitic inductance in the power loop has a major influence on the voltage overshoot and, therefore, the allowable switching speed. This has logically led to the suppression method, which minimises parasitic inductance to decrease the overshoot.

To verify this concept, the percentage voltage overshoot is plotted against the parasitic inductance in Fig. 3.9 and the switching speed against the parasitic inductance in Fig. 3.10.

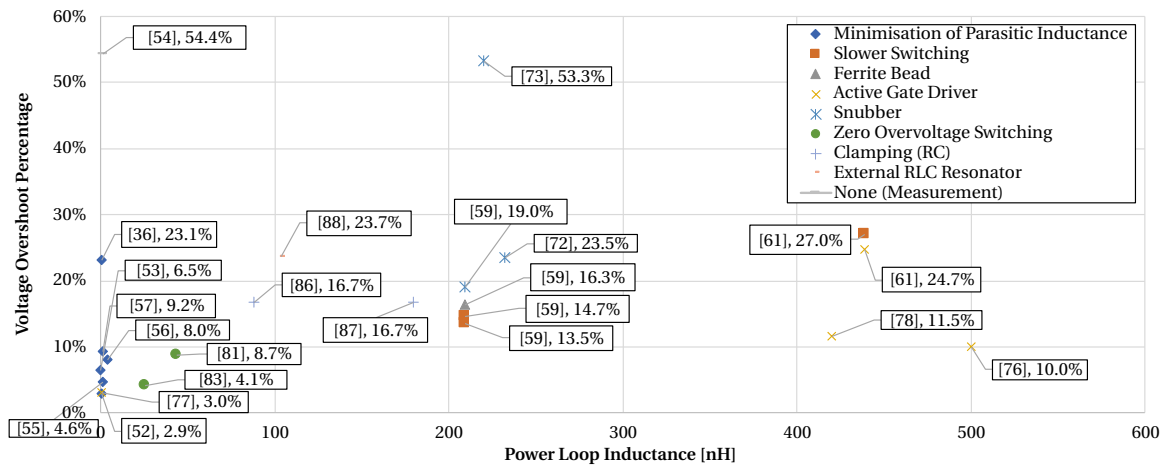


Fig. 3.9 Scatter plot of voltage overshoot percentage versus power loop inductance

When Fig. 3.9 is considered, it is expected that the data points should lean heavily to the right-hand side of the plot to represent a higher percentage overshoot when the inductance is higher. However this is seen not to be the case. It appears that there are several data points where the inductance is very low, but the overshoot is still very high, and there are cases where the parasitic inductance is very high, but the overshoot is not. Therefore, even though lowering parasitic inductance for a given circuit will reduce the overshoot, low parasitic inductance in isolation does not predict a high or a low overshoot. In Fig. 3.10, it can be seen that data points with high inductance tend to switch slower, and data points with lower inductance seem to switch faster, in general.

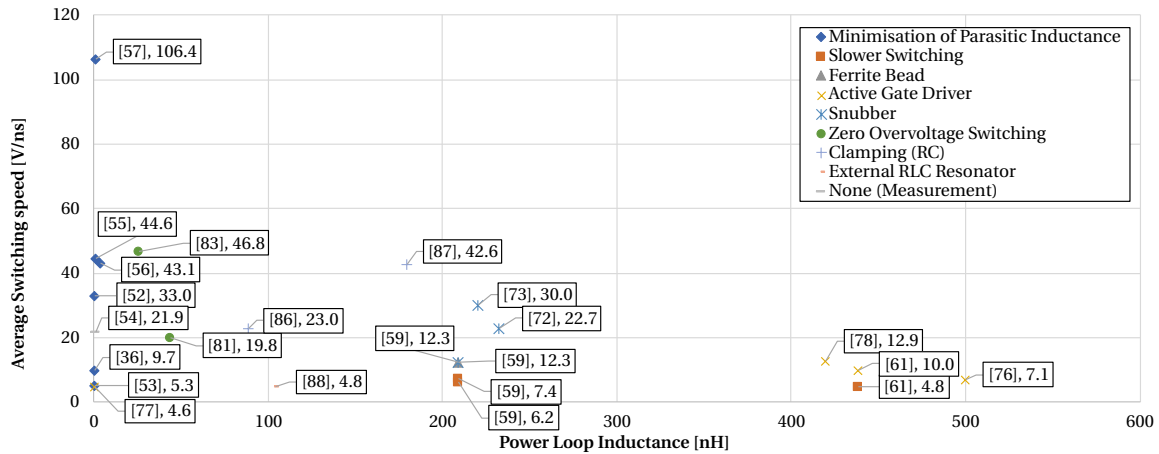


Fig. 3.10 Scatter plot of average switching speed versus power loop inductance

Influence of voltage and power on the overshoot

In this section, the view that the overshoot would generally be higher in converters that have a higher DC voltage or power is investigated. This section tests this view by first plotting the voltage overshoot against the settling voltage in Fig. 3.11 and then plotting the voltage overshoot percentage against the converter's power in Fig. 3.12.

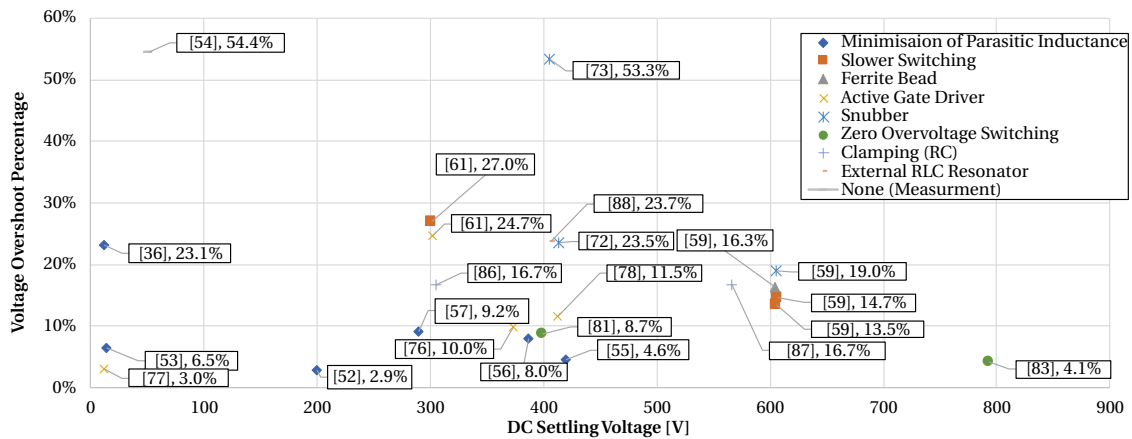


Fig. 3.11 Scatter plot of voltage overshoot percentage versus DC settling voltage

In these plots, it can be seen that there are several low DC voltage data points with high and low overshoots, as well as several high power data points with high and low overshoots.

This indicates that there is a very weak correlation between the overshoot and the voltage or power of a converter, and the general expectation that higher DC voltages or higher power could cause higher overvoltages does not seem to be true in general.

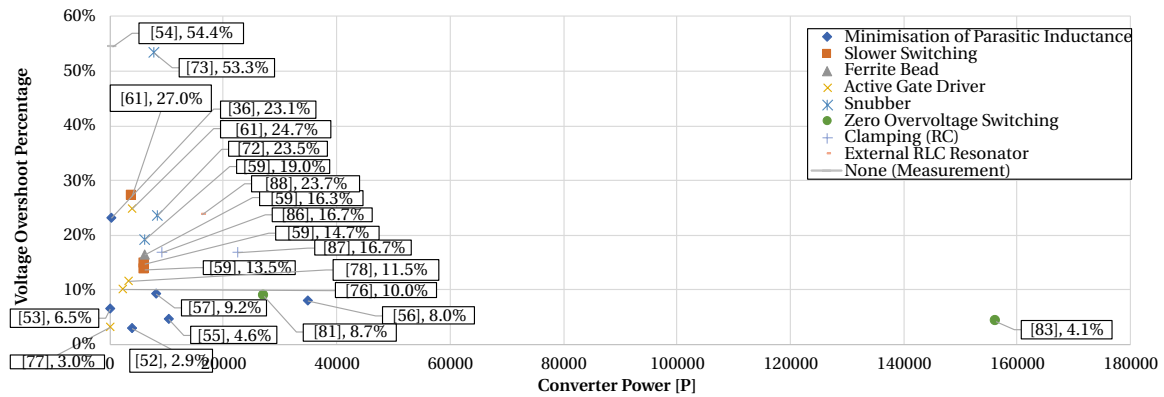


Fig. 3.12 Scatter plot of voltage overshoot percentage versus power

3.4.3 Future Direction of High-Speed Power Electronics

The switching speed is plotted versus the date the research was accepted for publication in Fig. 3.13. It is easy to see that the general trend over the past decade has been towards technology that enables higher switching speed. This is already well known. However, most of the articles used to extract the data from this work were based on real applications. Therefore, the trend shown in Fig. 3.13 is not only an idealised version of the pure devices but includes the complexities of the actual circuit.

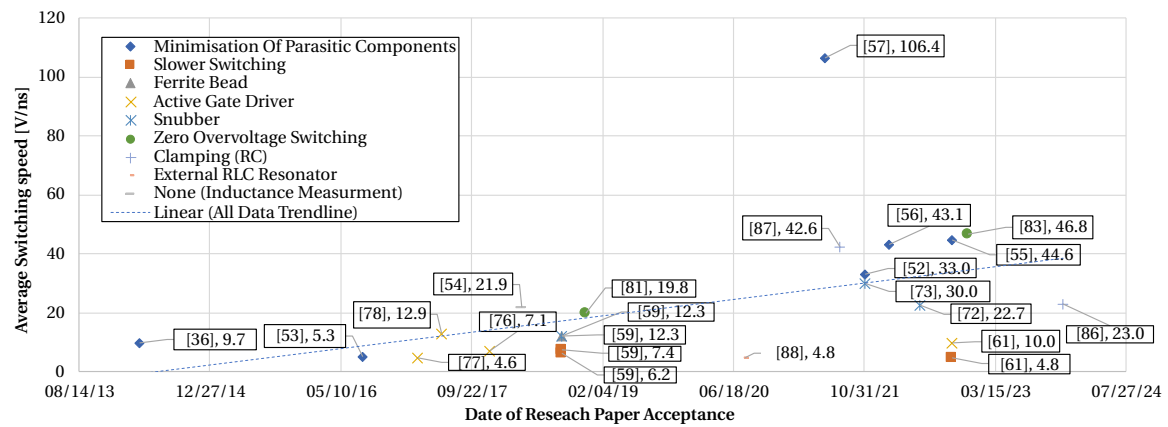


Fig. 3.13 Scatter plot of average switching speed versus the date the article was accepted for publishing

Fig. 3.13 includes a trendline that shows an increase in switching speed of approximately 4V/ns per year. This implies that if the trend continues, switching speeds may increase to between 50V/ns and 100V/ns over the next decade. Such a prediction is fraught with uncertainties, and the continuous increase in switch speeds may very well be countered by the associated increase in EMI. It may be that the switching speed plateaus over the next decade.

However, if the trend does continue to increase, it is questionable whether or not the current suppression methods would still be appropriate. From the graph of Fig. 3.13, the only suppression method amenable to increasing switching frequency is the ZOS method of [81], [83].

3.4.4 GaN versus SiC Discussion

Even though this research does not focus on the differences between SiC and GaN, the raw results in the appendix could be used for an in-depth comparison.

However, it can be seen that the average switching speed of SiC devices is 16.7 V/ns versus 37.7 V/ns of GaN, and the average DC voltage of SiC is 444.5 V versus 196.1 V of GaN. These results are as expected as GaN can switch faster than SiC and is generally used at lower voltage.

When the average overshoot is considered, it is seen that the SiC devices have an average overshoot of 18% and GaN has an overshoot of 14%, which is considered too small a difference to be relevant.

The data shown does not explicitly differentiate between GaN and SiC. These two materials generally have different areas of application, but both suffer from overvoltage problems due to fast switching. From the data, there is no indication that a certain type of overvoltage suppression method is more favourable for either GaN or SiC.

The semiconductor material does not directly influence the overshoot other than possibly introducing a change in the parasitic switch inductance and capacitance. The overshoot is a consequence of the electromagnetic environment around the switch coupled with its fast speed. Therefore, it is not expected that the material will influence the overshoot or the suppression methods.

Indeed, while this paper did not focus on older Si devices, it is expected that similar clustering of suppression methods could be expected.

The generality of the suppression methods implies that a given method could equally well be implemented on either GaN or SiC materials and, by extension, also on other materials.

3.5 Discussion and Recommendations

From the results, it can be seen that the minimisation of parasitic inductance yields the best results by far at the moment. This result makes sense as it directly addresses the root cause of the problem, but as mentioned, the main drawback of this method is that it will reach a natural limit.

The active gate driver method also has promising results, as the overshoot could be lowered substantially without sacrificing too much of the switching speed. This method has been described as a “research hotspot” and is expected to remain a heavily researched area.

It is anticipated that any significant progress can be divided into a medium-term future and a long-term future. For the medium-term future of five to ten years, it is expected that significant progress will lie in the hybrid application of minimisation of parasitic inductance with other methods, like Active Gate Driver. This will enable step-wise progression, but the parasitic inductance will still remain the major hurdle.

It is expected that the long-term future (more than ten years, in devices like UWBG) will be in the application of a method where parasitic inductance is not the main obstacle. The only known method at the moment where parasitic inductance is not the main hurdle is ZOS. Methods like this will also enable the full potential of future faster-switching devices like ultra-wide bandgap devices. However, this method is still in its infancy, and much work is needed to demonstrate its full potential both theoretically and practically.

3.6 Conclusion

This chapter reviews and compares the experimental results of several methods used to suppress the overvoltage and ringing of the switching node in WBG devices. A method to extract the relevant information from images of the turn-off voltage transition is presented and applied to all the resources that meet the requirements. A database of the results is included so that new methods can compare themselves against existing performance. The results in the database were plotted against each other, and the observations are summarised below:

1. Research articles that do not compare their experimental results to other experimental results in the field run the risk of not actually being as relevant as they expect. The single comparison of a waveform with and without a suppression method could be misleading as there is no common baseline between different methods.
2. Even though in a given switching circuit, when the parasitic inductance is lowered, the overshoot generally decreases, the parasitic inductance in isolation does not point to higher or lower overshoots.
3. Generally, the voltage and power of a converter, on their own, do not correlate with a higher overshoot.
4. If the achieved switching speed is used as a metric for the progress of power electronics, it can be seen that the field has progressed very well in the past ten years.

As mentioned above, it is seen that the method called ZOS seems to have the most potential in fast-switching applications, especially since it becomes better as the switching speed increases and is not bound by the parasitic inductance. However, this method will only be viable if the two

main drawbacks of operation only with an ideal switching event and in a very narrow margin of circuit parameter can be overcome.

Chapter 4

Fundamental Turn-off Switching Model

This chapter is adapted from the following publication:

F. P. D. Toit and I. W. Hofsajer, 'Fundamental Modeling of the Switching Transition in High-Speed Power Electronics', *IEEE Access*, vol. 12, pp. 38646–38663, 2024, doi: 10.1109/ACCESS.2024.3375388.

The author of this thesis conceptualised the study, conducted the analysis, developed the models, and wrote the original draft of the paper.

4.1 Introduction

From Chapter 2 and Chapter 3, it was seen that the suppression method called Zero Overvoltage Switching showed encouraging signs of potential to overcome the limitation imposed by parasitic inductance. However, this method is still in its infancy and is not yet adequately explained by some fundamental knowledge. Even though the high-level explanation of ZOS was given in [81]–[83] and the experimental results have now been placed within the context of other results, the fundamental theory explaining the unexpected results are still never explained within the context of the expected results.

Additionally, the basis of ZOS, the optimisation equation, Eq. (2.3), assumes 1.) ideal switching, which is impossible, and 2.) that all of the values of the inductance, capacitance, voltage and current are exactly as in the equation. Any straying from these values would cause a significant overshoot, making the argument to implement ZOS in a practical environment where voltage or current can change very difficult.

This chapter introduces a model based on circuit theory that investigates the switching transition in power electronics from a fundamental point of view to better understand the fundamentals working of ZOS and to create the underlying knowledge that can solve the issues introduced by parasitic inductance in fast switching environments. This theoretical knowledge is meant to increase

the fundamental understanding of the switching event that is applicable to all power electronic converters.

4.2 Introduction To Switching Model

4.2.1 Development of Model

The switching node of a commutation cell operation in boost mode is investigated, as seen and discussed in Chapter 1. This representation is chosen as it is where the overshoot phenomenon is a major concern, and this topology is applicable to other commonly used converter types, like synchronous buck converters. The equivalent circuit of a commutation cell from Fig. 1.2 is shown again below in Fig. 4.1.

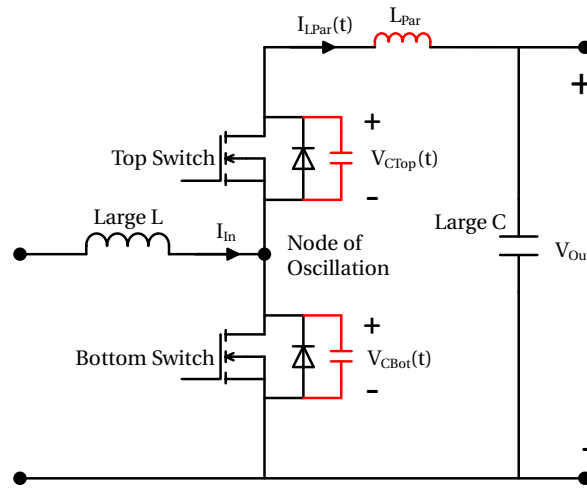


Fig. 4.1 Equivalent circuit of a commutation cell in boost mode

Several assumptions must be made to the circuit in Fig. 4.1 to be able to model the switching transition effectively. The first is the consideration of the intent of the model, which is to investigate the effect of both the parasitic components and the turn-off speed of the switch on the overshoot of the switching node voltage. Thus, the lumped circuit parasitic components and turn-off of the switch are modelled explicitly. The turn-off of the switch is modelled by replacing the switch with a linearly decaying current source from I_{In} to zero. As only the diode of the top switch will take part in the turn-off transition of the bottom switch, the transistor representation can also be removed.

Additionally, the assumption is made that the size of the input inductor and output capacitor is very large compared to the parasitic components and the time period of the investigation is very small, so the input inductor and output capacitor are replaced with a current source and voltage source, respectively. The circuit from Fig. 4.1 can then be converted into Fig. 4.2.

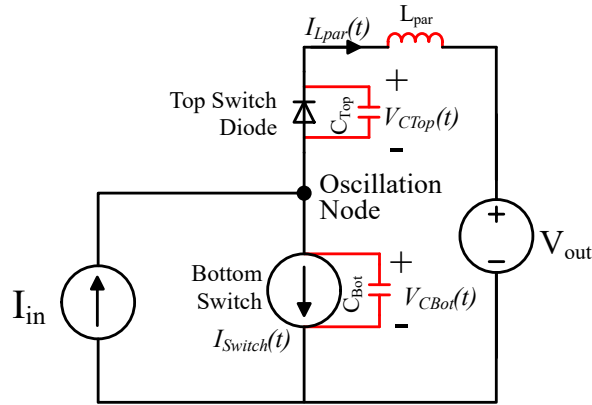


Fig. 4.2 Modified equivalent circuit of a commutation cell in boost mode

In this circuit, the turn-off current of the switch is assumed to be linear, and the turn-off period can be adjusted as required to model the opening of the switch at different switching speeds. An equation that satisfies these requirements can be seen below:

$$I_{Switch}(t) = I_{In} - \frac{I_{In}}{T_{Fall}} \cdot t \quad (4.1)$$

In this equation, T_{Fall} refers to the time required for the current through the switch to reach zero and thus is also the current transition period from I_{In} to zero. The assumption that the current through the switch decays linearly is made to make the resulting mathematics solvable, and to show underlying fundamental dynamics without clouding them with the higher-order effects of different semiconductor switching models.

This circuit can be seen to have six degrees of freedom, or variables that can be chosen by the designer, and it must be noted that the introduction of each additional degree of freedom greatly increases the complexity of the model. These variables are:

1. I_{In} – Input Current
2. V_{Out} - Output Voltage
3. T_{Fall} - Time taken for the switch to turn off fully
4. C_{Top} - Parasitic Capacitance of Diode (Top)
5. C_{Bot} - Parasitic Capacitance of Switch (Bottom)
6. L_{Par} - Cumulative Parasitic Inductance of Power Loop

Together, these variables form a circuit environment, and all the subsequent waveforms are interdependent on all of these variables. The equivalent resistance is not considered due to the complexity of the model and does not have a big influence on the first peak of the overshoot.

To analyse this circuit in Fig. 4.2, a conventional approach of circuit analysis using Kirchoff's current and voltage laws is used to determine the time domain equations. The Laplace transforms are then used to solve the variables of $V_{CBot}(t)$, $V_{CTop}(t)$ and $I_{LPar}(t)$ and then converted back to the time domain using inverse Laplace transforms. This analysis starts when the switch starts to turn off. In the equivalent circuit illustrations, the diode is indicated only when it is blocking, and is not shown when it has clamped.

As the voltage and current progress through the time domain, it is seen that the equivalent circuit that is relevant to the specific time period will change. The two events that will change the equivalent circuit and their effects are:

1. **Clamping of the diode** – As the diode becomes forward-biased, C_{Diode} will be short-circuited, and both the diode and capacitor can be ignored in the circuit analysis after the event.
2. **The switch fully turns off** – when the current through the switch, $I_{Switch}(t)$, reaches zero, the current source representing the switch becomes an open circuit and can also be removed from the equivalent circuit.

The values at the end of a specific period are then used as the initial conditions for solving the variables in the following period. The math becomes very complicated as the equivalent circuits progress, and the full analysis and mathematical results can be seen in Appendix A.

From the investigation, it is seen that, depending on the combination of choices of the variables mentioned above, either the diode can clamp first or the switch can fully turn off first. This means that depending on the variables, different equivalent circuit progressions will be followed. The simplified comparison of slow and fast switching waveforms from Fig. 1.3 is reinvestigated and annotated as seen in Fig. 4.3 below.

In this simplified illustration, an example of a slow-switching and fast-switching waveform can be seen, and the different time periods are indicated explicitly. Period 0 (P0) is before the switch starts to close, and Period (P3) is after both the diode has clamped and the switch has fully turned off. It can be seen that in-between P0 and P3, the order of events can differ between a fast switching transition and a slow switching transition.

The alternative circuit progressions from Period 1 (P1) to Period 3 (P3) are named *Slow-Mode* and *Fast-Mode* circuit progressions for simplicity, and the corresponding equivalent circuits progression can be seen in be seen in Fig. 4.4, and must be viewed in conjunction with Fig. 4.3.

In *Slow-Mode* circuit progressions, as seen in Fig. 4.3(a), the diode clamps before the switch is fully turned off, and this progression is the equivalent circuit progression of mainstream conventional switching and can be seen in Fig. 4.4.

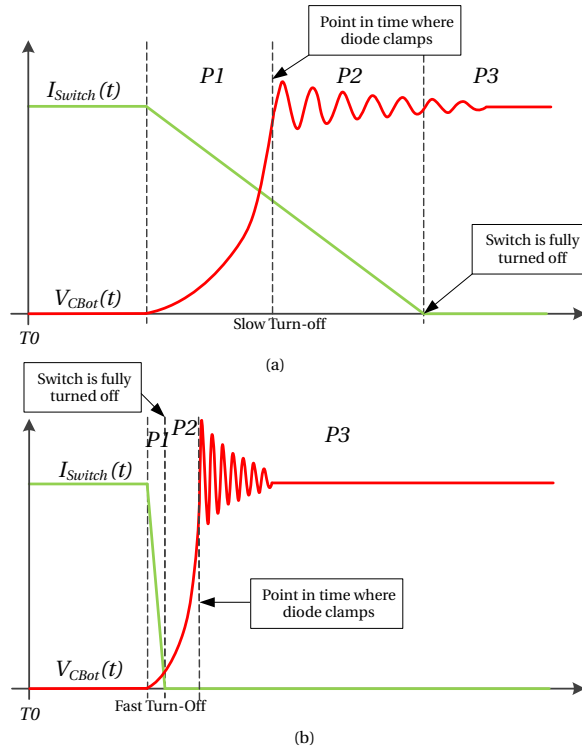


Fig. 4.3 Overshoot comparison of (a) a slow turn-off event, and (b) a fast turn-off event with annotations

In *Fast-Mode* circuit progressions, as seen in Fig. 4.3(b), the switch fully turns off and becomes an open circuit before the diode clamps. This is only possible in very fast switching transitions and is the circuit progression when ZOS is presented.

4.2.2 Mathematical Model Preliminary Results

After both the circuit progressions of *Slow-Mode* and *Fast-Mode* have been analysed and solved using circuit analysis and Laplace transforms, the variables in the equations are populated using arbitrary realistic values so that the model can be illustrated. These values will be used for the rest of the thesis unless explicitly stated otherwise, and they are as seen in Table 4.1.

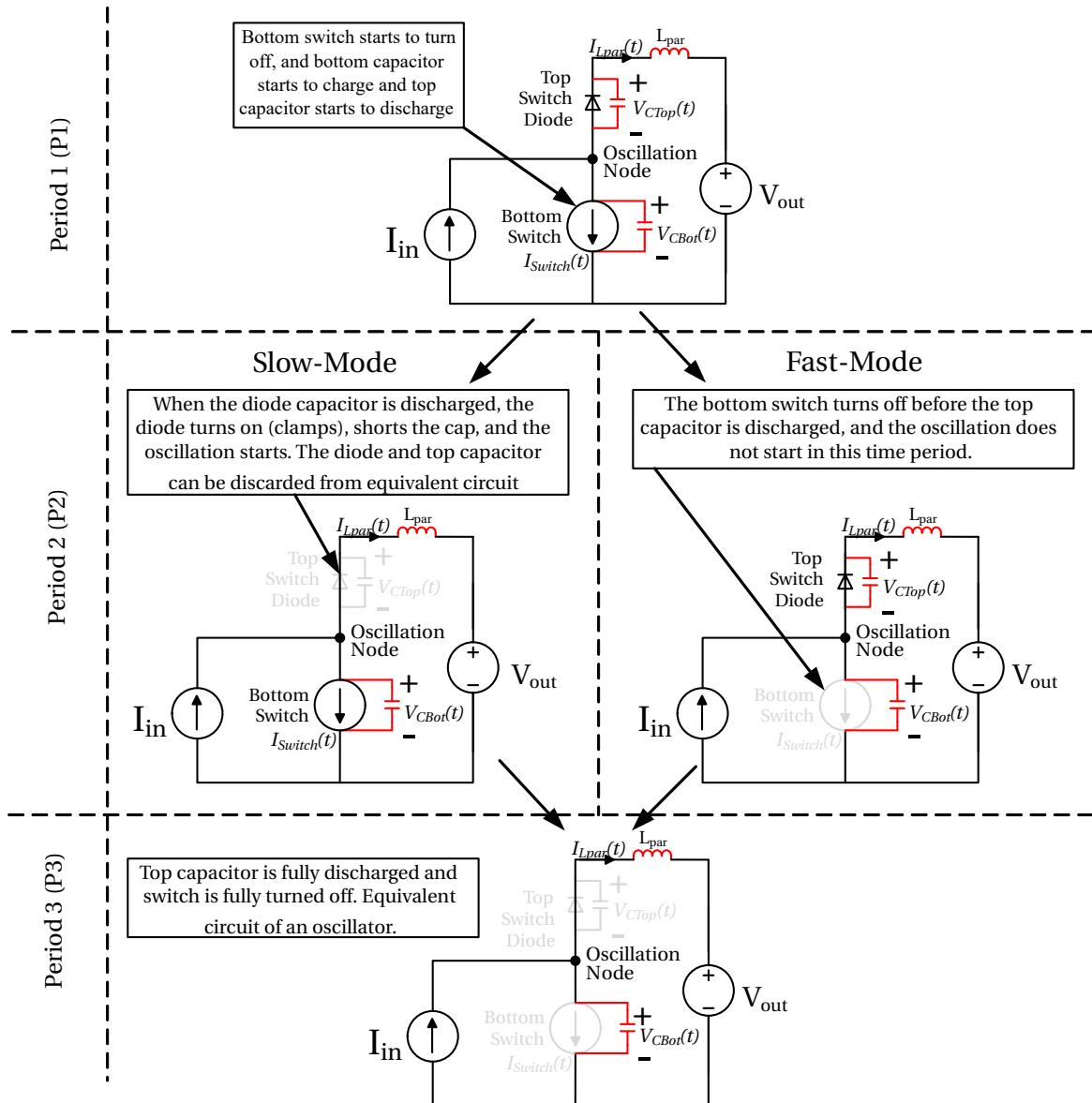


Fig. 4.4 Alternative equivalent circuit progression for Slow-Mode versus Fast-Mode

Table 4.1 Circuit Model Variable Values

Variable	Value
I_{In}	20A
V_{Out}	300V
C_{Diode}	100pF
C_{Switch}	100pF
L_{Par}	15nH

When the mathematical model from Appendix A is populated with the values above, and together with a slow switching transition illustrated by $T_{Fall} = 60ns$, and fast switching transition illustrated by $T_{Fall} = 3ns$, the following waveforms can be seen in Fig. 4.5 and Fig. 4.6, respectively. It must be noted that the scale of these plots is the same to emphasise the difference in switching speed.

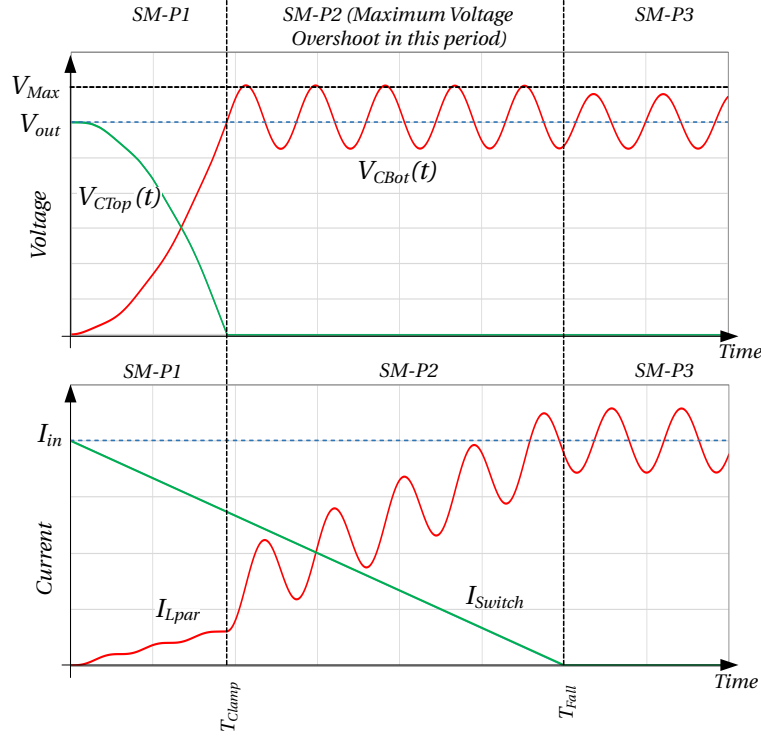


Fig. 4.5 Slow-Mode circuit progression waveforms of voltage and current

In these figures, the scale of the time-axis is kept the same to illustrate the differences in turn-off time, and it must be noted that these waveforms were simulated as well to verify the integrity of the underlying maths. It must also be noted that the oscillation will be damped if the equivalent resistance is included.

For *Slow-Mode* in Fig. 4.5, the voltage overshoot will occur in Period 2 (P2) when the equivalent circuit of a resonating circuit has been achieved, and it can be seen that the current oscillation starts as well, even though it has not reached I_{In} yet. The current oscillation will also be damped out if the equivalent resistance is modelled.

For *Fast-Mode* in Fig. 4.6, the overshoot will occur in Period 3 (P3). It can be seen that P2 is very small in *Fast-Mode* as the diode clamps quicker and that P3 will be reached much faster.

When the two plots of *Slow-Mode* and *Fast-Mode*, it can be seen that the oscillation will always start after the diode clamps. This means that the voltage rise of the oscillation node is not directly

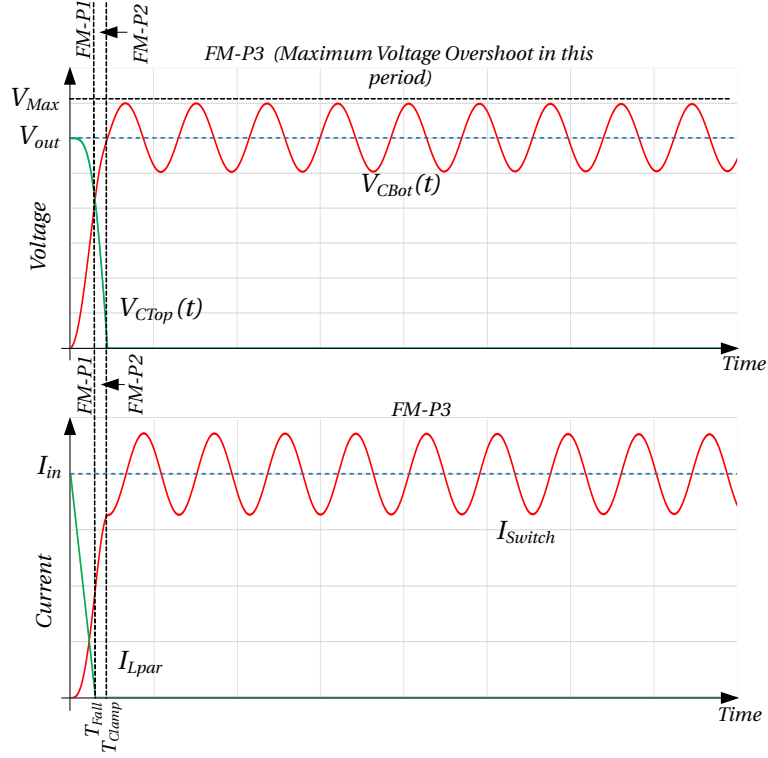


Fig. 4.6 Fast-Mode circuit progression waveforms of voltage and current

dependent on the turn-off time of the switch but rather dependent on the time it takes for the diode to clamp.

It must be noted that the time it takes for the diode to clamp ($V_{CTop}(t)$ to reach zero) naturally occurs and is a secondary effect of the choice of parasitic components and the turn-off time of the switch, but it is a very important occurrence in the progression. This point in time is referred to as T_{Clamp} , and this value will become lower as the switching time T_{Fall} becomes smaller.

If T_{Fall} starts large (slow switching event) as seen in Fig. 4.5, and then becomes smaller and smaller, it will eventually become equal to, and then smaller than T_{Clamp} . It is at this equal point (when T_{Fall} is chosen as such) where $T_{Fall} = T_{Clamp}$ where the transition happens between *Slow-Mode* and *Fast-Mode* and can be described mathematically as seen below in Eq. 4.2.

$$V_{CTop}(T_{Fall}) = 0 \quad (4.2)$$

This point in time is dependent on all six of the variables described above. This makes this point difficult to derive mathematically, so the roots of the function are solved analytically when all the variables are available.

It is important to note that this transition point between *Slow-Mode* and *Fast-Mode* exists for all combinations and ratios of positive values of the parasitic components. This means that eventually,

and independent of the oscillation suppression method that is applied, all switching events will reach the transition point if the speed increases enough. Therefore, given that the switching speed of devices is increasing, a better understanding of *Fast-Mode* is required. Specifically, to fundamentally understand how the circuit parameters and switching speed translate to the overshoot when switching in *Fast-Mode*.

Influence of Turn-off Period On Voltage Overshoot in Fast-Mode

When the maximum voltage overshoot in Fig. 4.5 and Fig. 4.6 are investigated, it can be seen that the overshoot is very similar, even though the switching period is 20 times faster in the *Fast-Mode* example than in the *Slow-Mode* example, which is not according to mainstream expectations, but is predicted according to ZOS.

So to get a better understanding of the voltage overshoot for all different values of the turn-off period T_{Fall} (time for switch to fully turn-off), an iterative method is followed where T_{Fall} is swept from 0 (ideal switch) to a very high value, but the rest of the circuit parameters are kept as in Table 4.1, and the resulting voltage overshoot versus switching speed can be seen in Fig. 4.7.

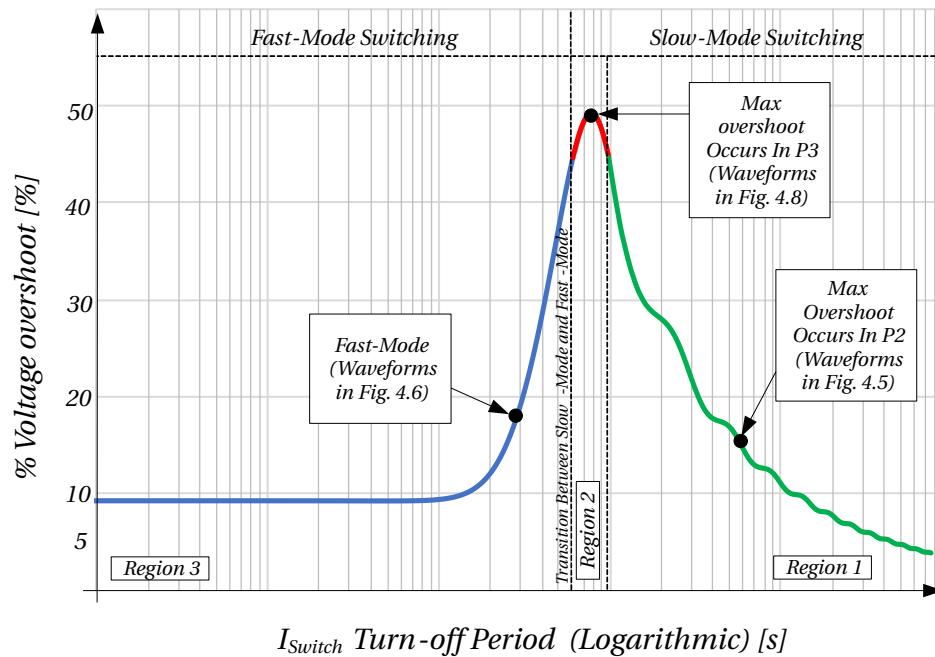


Fig. 4.7 Overshoot percentage versus turn-off period of switch

In Fig. 4.7, *Slow-Mode* on the right-hand side of the plot is an example of conventional switching. In this part of the plot, it is seen that the overshoot decreases as the switching period increases, which is according to mainstream expectations. An example of the waveform of slow switching is seen above in Fig. 4.5.

The left-hand side of the plot in Fig. 4.7 shows when the circuit is operating in *Fast-Mode*. It can be seen that the overshoot drastically decreases, and this decrease in voltage overshoot is against mainstream expectations. It is seen that when in *Fast-Mode*, one of the main rules of switching, that the overshoot increases as the speed increases, no longer holds.

Indications of the maximum voltage overshoots of the plots in Fig. 4.5 and Fig. 4.6 are also shown, and it can be seen that they have a similar value but with a very large peak in between. It can be seen that this peak occurs in *Slow-Mode* part of the plot.

This very large peak occurs when 1.) the switching transition is in *Slow-Mode*, and 2.) the maximum overshoot is in P3 and not in P2. This can only occur in a very limited space, as the switch must fully turn off within a quarter-cycle of the oscillation starting. This section generally accounts for the largest overshoot of the entire plot. An example of the switching waveform when this occurs can be seen in Fig. 4.8.

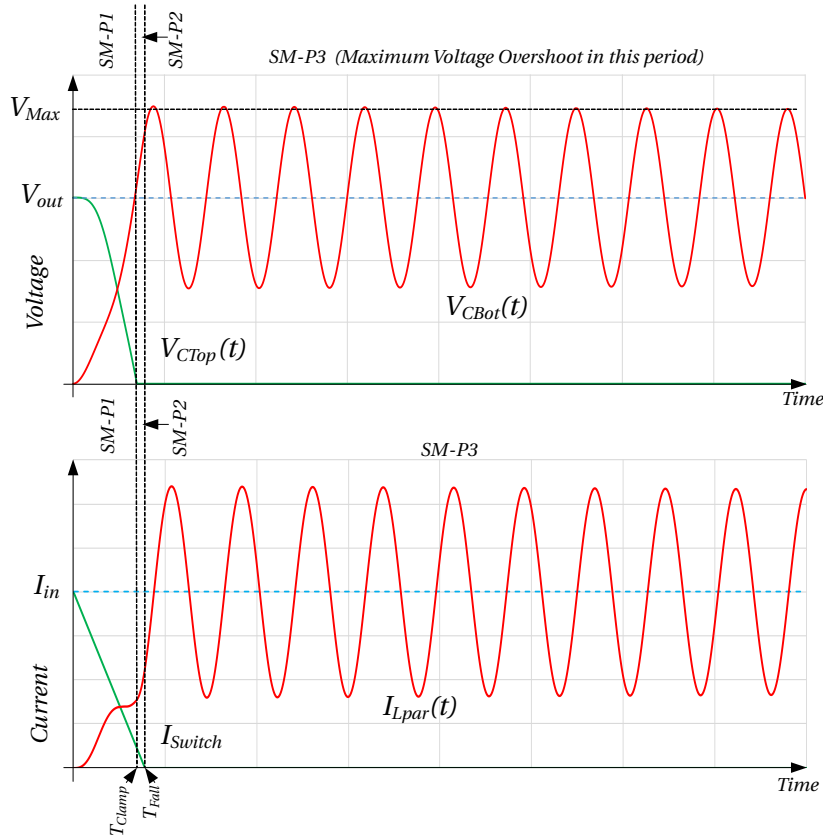


Fig. 4.8 Slow-Mode maximum voltage overshoot waveforms

In the figure, the voltage overshoot is at a maximum given the chosen parameters. It can be seen that this absolute maximum occurs when T_{Fall} is half of a quarter cycle of the oscillation after the diode clamps, and it can be seen that the difference between T_{Fall} and T_{Clamp} is very small.

Influence of Inductance On Voltage Overshoot in Fast-Mode

As discussed above, it was seen that when switching in *Fast-Mode*, one can no longer expect the voltage overshoot to increase as the speed increases. This section investigates the other main accepted rule in power electronics, that overshoot must decrease as the parasitic inductance decreases.

To demonstrate this, a similar graph to that of Fig. 4.7 is presented in Fig. 4.9, where the circuit model is used to determine the overshoot versus the fall time. In this figure, four inductance values are chosen: 1.) very low 2.) low 3.) high and 4.) very high.

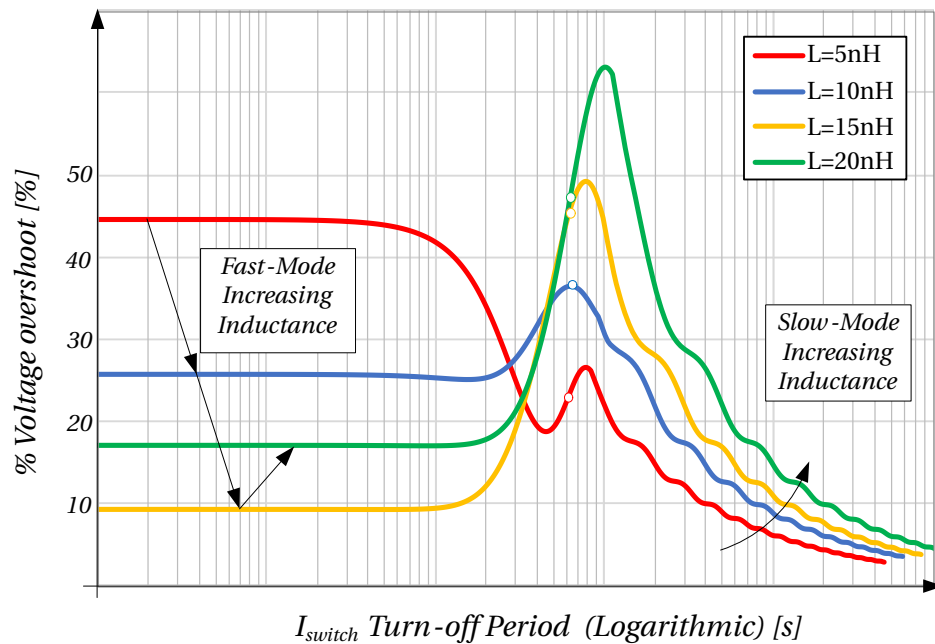


Fig. 4.9 Voltage overshoot versus switching speed of four increasing inductance values

In the plot, the dot on each of the plots refers to the point where each plot transitions between *Slow-Mode* and *Fast-Mode*.

On the right-hand side, the graph shows that the overshoot increases as the inductance increases for a given switching speed, as expected in conventional *Slow-Mode*. On the left-hand side of the plot that represents *Fast-Mode*, it can be seen that the overshoot does not behave as expected and that the inductance does not correlate with the voltage overshoot at all. It can be seen some of the overshoots at ideal switching are less than the local maximum at the transition point, and some are more. From this plot, it can be seen that the assumption that the inductance exacerbates the overshoot is not true in *Fast-Mode* and that there is no correlation between inductance and overshoot.

An additional observation is the point where all four of the plot's transitions between *Slow-Mode* and *Fast-Mode* are almost exactly for the same switching speed. This indicates that the inductance does not heavily influence this point but rather the capacitance of the diode.

4.3 Conclusion

This section provides the development of a mathematical model that can be seen in Appendix A of the generic switching transition in power electronics. This model is then able to account for the unexpected results of ZOS as well as the expected conventional results always expected in power electronics. The model also mathematically proves that any switching circuit, if switched fast enough, will transition from *Slow-Mode* and *Fast-Mode*, which means that eventually all switching transitions will be *Fast-Mode*.

Additionally, the model also shows that when switching in *Fast-Mode*, most of the historically accepted assumptions in power electronics, like faster-switching leads to larger overshoot, become false. So, knowing that eventually, all switching transitions will be in *Fast-Mode* and that all accepted assumptions break down, a much deeper understanding and foundation of fast switching is required.

As it is seen that the main approaches to minimise the overshoot in conventional switching do not apply to very fast switching scenarios, the logical follow-up question then becomes: "What must the main approach be when switching very fast?" is answered in the following chapter.

Chapter 5

Fundamental Energy-based Mechanism of Voltage Overshoot

This chapter is adapted from the following publication:

F. P. D. Toit and I. W. Hofsjager, 'Fundamental Modeling of the Switching Transition in High Speed Power Electronics', *IEEE Access*, vol. 12, pp. 38646–38663, 2024, doi: 10.1109/ACCESS.2024.3375388.

The author of this thesis conceptualised the study, conducted the analysis, developed the models, and wrote the original draft of the paper.

5.1 Introduction

The previous chapter provides insight into alternative equivalent circuit switching progression but does not explain how it is possible to eliminate the overshoot in the correct conditions when having *Fast-Mode* circuit progression but not in *Slow-Mode*. Therefore, this chapter utilises the model to provide an energy-based explanation of the mechanics of the overshoot and describes what the underlying intention of the design must be to eliminate the overshoot.

5.2 Energy-Based Underlying Mechanism of Voltage overshoot

When the entire switching transition is considered, including the time before the switching transition and a long time after the switching transition, the waveforms below in Fig. 5.1 will be applicable in a fast-switching event for a circuit with damping in *Fast-Mode*.

When the period before the switch is considered, P0, it can be seen that the switch has been closed for a long time, and there are no oscillations. P4 is after the switch has been open for a long time and all the oscillations and resonance have been damped out.

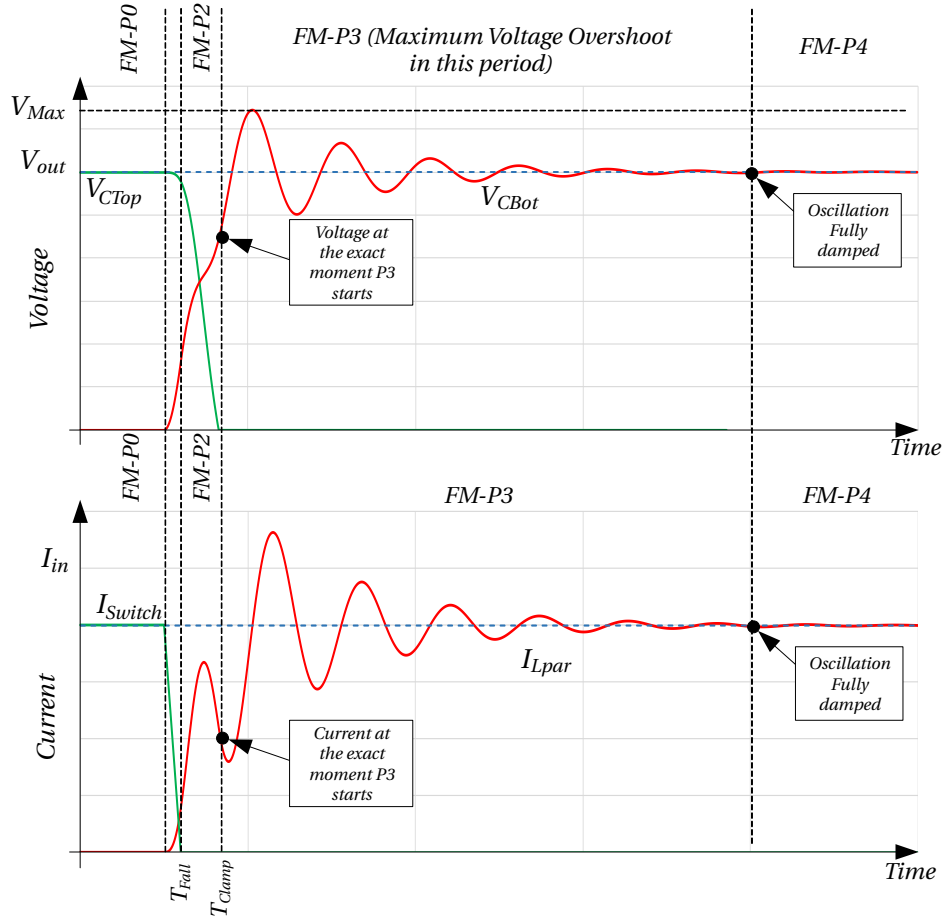


Fig. 5.1 Typical Fast-Mode switching transition with damping

The equivalent circuit transition from P0 to P4 with an emphasis on energy storage of the reactive components can be seen in Fig. 5.2.

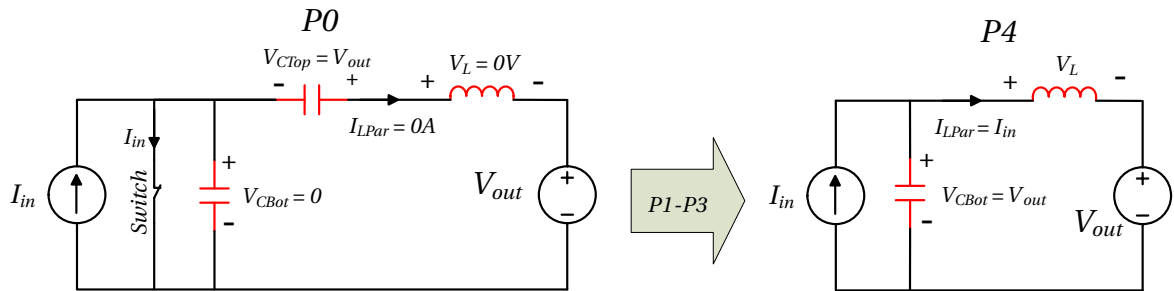


Fig. 5.2 Equivalent circuit From P0 to P4 highlighting energy of reactive components

It can be seen that in P0, only C_{Top} is storing the energy of the full value of V_{Out} . In P4, C_{Top} has been short-circuited by the diode, and there is only energy stored in C_{Bot} and L_{Par} . Basically, the investigation into the switching transition is an attempt to effectively manage the process to

get the energy stored in the passive components from P0 to P4 as well as possible, where what happens in P1 to P3 can be manipulated.

As the equivalent circuit progressions of *Slow-Mode* and *Fast-Mode* are different, the underlying mechanism of the overshoot and energy transition requirements are also different. These differences are investigated separately below.

5.2.1 Ideal Energy for Fast-Mode

As discussed in Chapter 4, when the overshoot of *Fast-Mode* in Fig. 4.6 is considered with the *Fast-Mode* equivalent circuit from Fig. 4.4, it can be seen that the overshoot oscillation starts when the diode clamps and the equivalent circuit progresses to a resonance circuit, which happens in P3. This is the same circuit as the resonance circuit in P4 of Fig. 5.2, just with the oscillation damped out.

When the resonance circuit is considered in isolation, as seen in P4 of Fig. 5.2, it is known that the amplitude of the resonance in a circuit is determined by the initial conditions of the period if the other circuit parameters are fixed.

This then means that if the initial conditions of P3 are such that the voltage over the capacitor is equal to V_{Out} , and the current through the inductor is equal to I_{In} , at the exact time the diode clamps, no overshoot will happen. In essence, this means that the energy stored in both C_{Bot} and L_{Par} must be the same as the energy stored in the components in P4 (after oscillation) for no overshoot to occur. This scenario is referred to as the ideal energy at T_{Clamp} further in this research.

Since the energy stored in an inductor is determined by its current ($E_L = \frac{1}{2}LI^2$) and the energy stored in a capacitor is determined by its voltage ($E_C = \frac{1}{2}CV^2$), these quantities inherently represent the system's energy state. Therefore, rather than separately referring to the inductor current or capacitor voltage, this explanation adopts an energy-based perspective, as it provides a unified and comprehensive description of the circuit conditions.

Additionally, as will be discussed in Chapter 6, the energy stored in these components will directly determine the eventual voltage overshoot in the circuit.

Derivation of Ideal Energy Requirements

To be able to determine the requirements for ideal energy at T_{Clamp} , the switching event is assumed to be ideal, eliminating one of the system's degrees of freedom, meaning $T_{Fall}(t)$ can be removed. So, the assumption is made that P0 (steady state before the switch) will progress directly to P2 when the switch becomes a short circuit, and P2 will naturally progress to P3 once the diode clamps.

This means that in P2, the voltage over the capacitor will increase, and the current in the inductor will increase as with the natural response of the system. However, if the energy values are at the ideal values, as discussed above, at the exact time the diode clamps, no overshoot will occur because the system is already in its steady state. Mathematically, this requirement of the ideal energy at T_{Clamp} translates to the following equations:

$$V_{C_{Bot}}(T_{Clamp}) = V_{Out} \quad (5.1)$$

And

$$I_{L_{Par}}(T_{Clamp}) = I_{In} \quad (5.2)$$

When this requirement is investigated using circuit analysis and Laplace transforms, the resulting equation could be produced:

$$I_{in} = V_{out} - \frac{\sqrt{\frac{8C_{Par}}{L_{Par}}}}{(2n-1)\pi} \quad (5.3)$$

For this equation to hold, the values of C_{Bot} and C_{Top} must be the same. The value of n can be any integer larger than one. The presence of this n indicates that the optimised point of operation will occur again when one of the variables changes.

This equation is similar to those presented in [81] and [83]. This equation also summarised the main drawbacks of the current understanding of ZOS, namely, that it assumes ideal switching and that change of any variable will cause a large overshoot at the equation is not satisfied any more.

Ideal versus Non-Ideal Energy Example

As the optimisation equation indicated where ideal energy at T_{Clamp} would be possible and eliminate the overshoot, it is applied to the system described in Chapter 4, and the inductance is recalculated to be 18.15 nH, up from 15nH. The resulting plot of overshoot versus switching speed can be seen in Fig. 5.3.

In this graph, it can be seen that there is effectively no overshoot when switching at very high speeds and a major sacrifice in overshoot when the switching speeds slow down. It can also again be seen that the actual peak occurs when switching in *Slow-Mode*, and this graph can also be used as a good illustration for an example of a fast switching event with ideal energy transfer and one without, so two dots are indicated on the plot. The corresponding time domain waveforms of these two dots can be seen in red and green in Fig. 5.4.

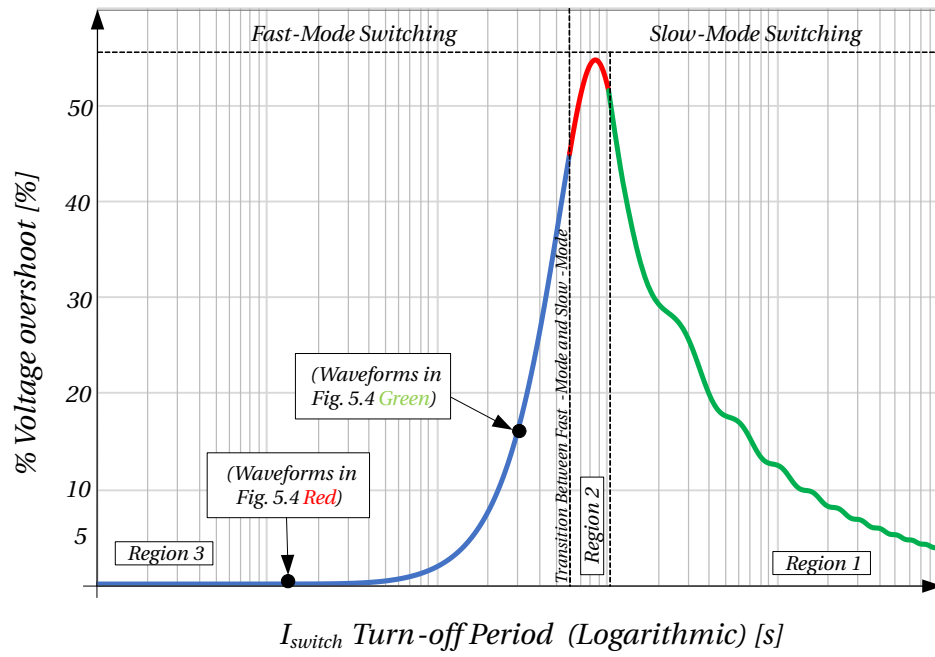


Fig. 5.3 Voltage overshoot versus switching speed when optimisation equation is applied

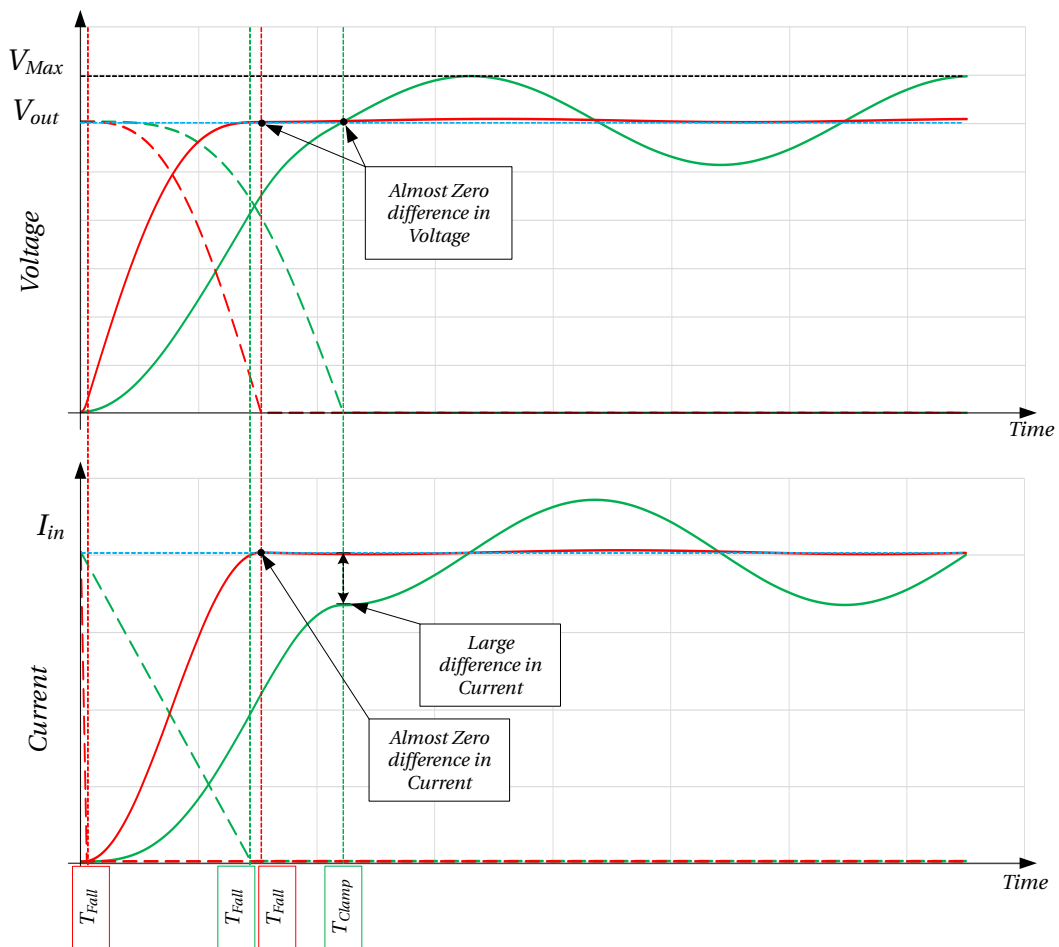


Fig. 5.4 Fast-Mode comparison of switching node waveforms for optimal energy transfer versus non-optimal energy transfer

In this plot, the red is an example of ideal energy at T_{Clamp} , and the green is an example of the same system switching slower and consequently having non-ideal energy at T_{Clamp} .

For the ideal example in red, it can be seen that both the inductor current and the capacitor voltage are at ideal values the moment the diode clamps (start of P3), and no overshoot follows.

For the non-ideal example in green, it can be seen that the capacitor voltage is at the ideal value the moment the diode clamps (start of P3), but the inductor current is far from the ideal value, leading to a large overshoot in P3. It can be seen that the mismatch in energy between the initial conditions of P3 and the required energy conditions of P4 produces the voltage overshoot. And the larger the mismatch, the larger the overshoot will be. As the inductance value is much larger than the capacitance value, the energy mismatch caused by a mismatch in the current of the inductor is punished much more severely than the energy mismatch in the voltage of the capacitor.

Further Interpretation of ZOS Optimisation Equation

From the optimisation equation of ZOS in Eq. (5.3), it can also be seen that the ideal point of operation is dependent on the relationship between the parameters and not the parameters themselves. This means the plot presented in Fig. 5.3 is translatable. When the parasitic inductance values are doubled from 18.15nH to 36.3nH, and both the capacitors are doubled from 100pF to 200pF, the updated plot in Fig. 5.5 will be applicable.

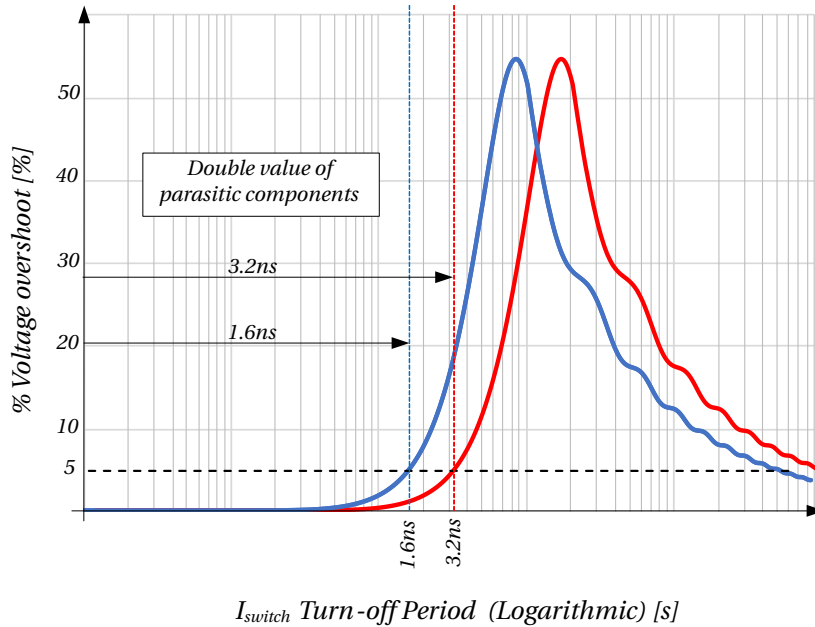


Fig. 5.5 Voltage overshoot versus switching speed comparison when parasitic components are doubled

From the plot, it can be seen that the allowable turn-off period for a 5% overshoot is doubled if the parasitic components are also doubled. Unfortunately, even though this allows for larger inductance, the larger capacitance would directly influence the switching speed, and may require a better gate driver still to achieve the fast switching speed with the larger capacitance.

An important addition is that this described ideal energy at T_{Clamp} can also be achieved when the turn-off period is not ideal, but this can only be achieved when the capacitors do not match and the diode capacitor is larger than the switch capacitor, but as stated above, the introduction of two more degrees of freedom also introduces very high complexity to the model. Thus, this point of operation also cannot be mathematically derived in closed form due to the interdependencies of the variables, but a numerical method of calculation is able to find the combination of parameters that can display this optimised point.

In this numerical method, values are given to the parasitic inductance, voltage, current and chosen turn-off period, and the corresponding capacitance values for the diode and switch capacitors are calculated. It must be noted that this is the only method in which values for the non-ideal switching event could be calculated. For example, if values were chosen for all but the inductance, a solution did not exist. This indicates that the relationship between the capacitance values is also a very important ratio.

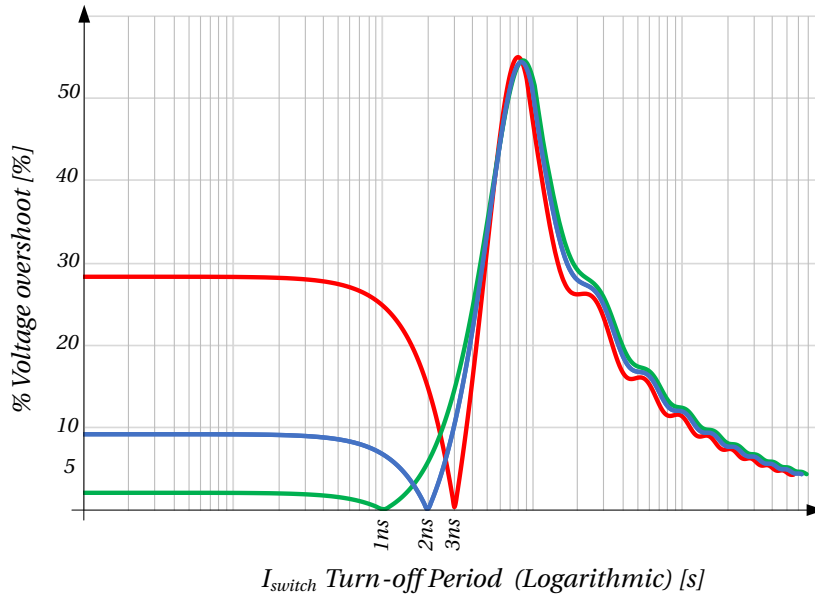


Fig. 5.6 Overshoot versus switching speed when optimised for non-ideal switching event

Fig. 5.6 shows the plot comparing the voltage overshoot and the turn-off period of the optimised points for the non-ideal switching transition. These points of operation are found when optimising for three different turn-off periods while keeping the inductance the same as in the plot above and finding the correct capacitance values. In this plot, it can be seen that the longer the turn-off

period is optimised for, the greater the overshoot sacrifice is when not switching at exactly this point.

Additionally, the longer the turn-off period point of optimisation, the greater the ratio between the diode and switch capacitor has to be.

Even though these methods attempt to solve one of the major drawbacks of ZOS, that an ideal switch is required, the other problem of it still only having a single point of operation is still applicable. This drawback will be addressed in the following chapter.

5.2.2 Ideal Energy for Slow-Mode

When a similar approach is followed for *Slow-Mode* as seen in the analysis above, we now know that the energy in the parasitic components needs to be at the correct values at T_{Clamp} , but in *Slow-Mode*, the diode clamps at the start of P2, and not at the start of P3. This means that the values need to be at the ideal values in a different equivalent circuit. So, to determine what the ideal energy values are, the equivalent circuit of P2 for *Slow-Mode* is re-evaluated and simplified as seen in Fig. 5.7.

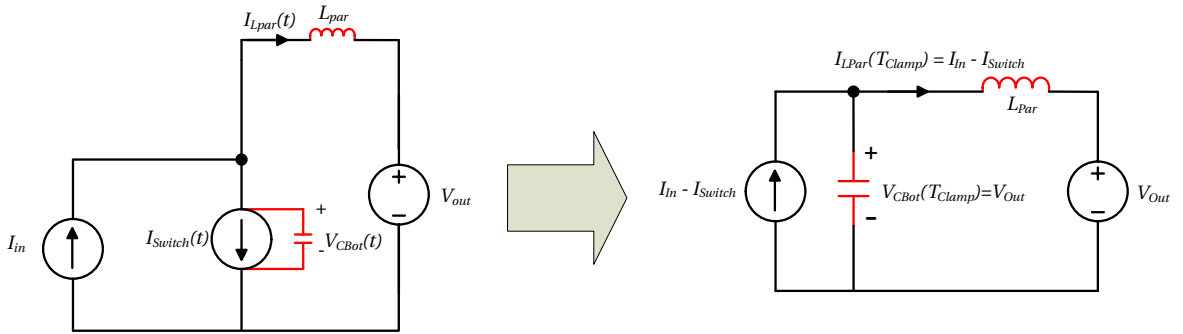


Fig. 5.7 Equivalent circuit of Slow-Mode, P2, simplified

It can be seen that the input current and the switch current can be combined so that the equivalent circuits of P2 and P3 are similar. In this representation, we know the ideal values are when the inductor current is equal to the current source and the capacitor voltage is equal to the voltage source, So the ideal values for *Slow-Mode* can be revised as:

$$V_{CBot}(T_{Clamp}) = V_{Out} \quad (5.4)$$

And

$$I_{LPar}(T_{Clamp}) = I_{In} - I_{Switch} \quad (5.5)$$

This means that for no overshoot to occur, the voltage over the capacitor must be equal to V_{Out} , and the current through the inductor must be $I_{In} - I_{Switch}(t)$ at the exact moment the diode clamps, and the oscillation is supposed to start. An example can be seen in the waveform comparison below in Fig. 5.8.

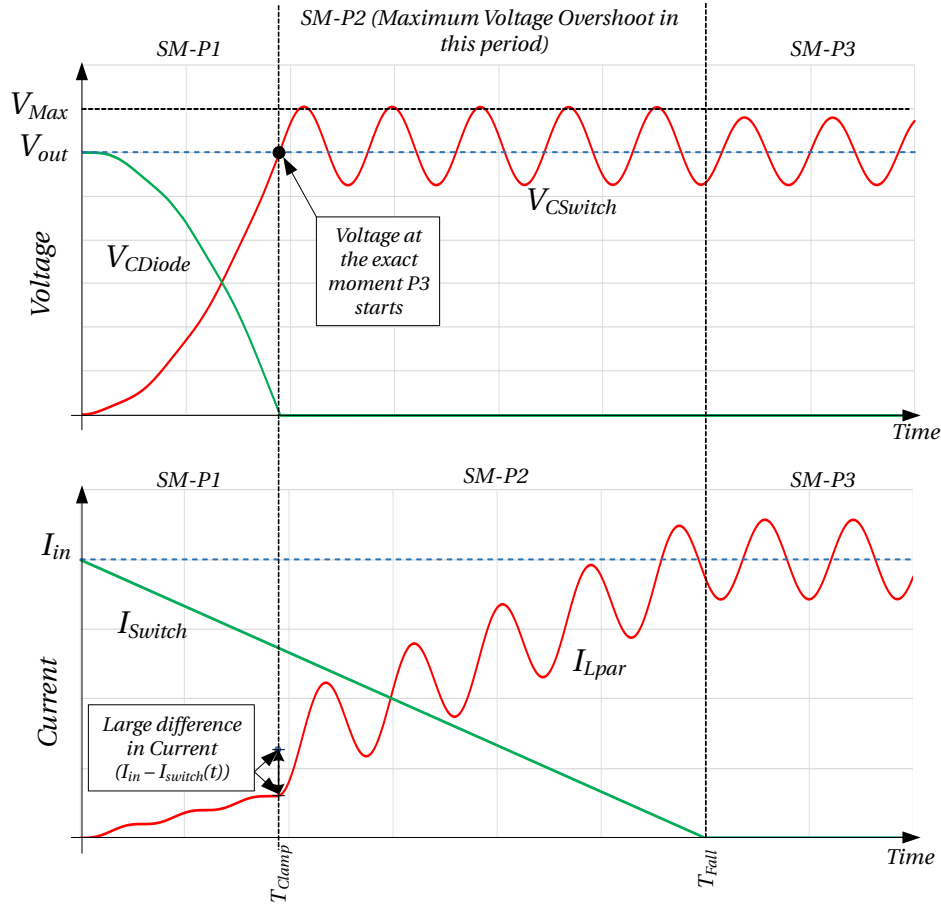


Fig. 5.8 Slow-Mode switching node waveforms for non-optimal energy values

It is seen that the smaller the mismatch in current or the smaller the energy mismatch, the smaller the voltage overshoot will be. From the energy mismatch approach, the inductor current must then be as close as possible to the calculated point when the diode clamps and this can be done relatively easily in two ways.

The first is to increase the slope of the inductor current in P1, which can be done by decreasing the inductance as much as possible, and the second is to make P1 longer, which can be done by switching slower.

Decreasing the inductance or decreasing the switching speed are the two most known methods of decreasing the voltage overshoot, which shows that mainstream attempts to minimise overshoot are just a secondary consequence of lowering the energy mismatch at the start of P2.

Unfortunately, the equation can only be satisfied if there is no inductance in the circuit, which in turn means that ideal energy at T_{Clamp} in *Slow-Mode* switching is not possible as the inductance cannot be reduced to zero.

5.3 Conclusion

This chapter demonstrates an energy-based understanding of the overshoot mechanism in the turn-off event. It is seen that ideal energy at T_{Clamp} is not possible in *Slow-Mode* because of the order of events in the circuit progression.

The main aim of this section is to show that the idea of minimisation of parasitic inductance or switching slower to reduce overshoot must be changed to the idea of ideal energy at T_{Clamp} , especially in fast switching conditions. It is seen that if the inductor current and capacitor voltage are at exactly the correct values at the exact moment, the overshoot can be eliminated. It is then also seen that this cannot happen in *Slow-Mode* because of the order of the equivalent circuit progression, but it is possible in *Fast-Mode*. However, ideal overshoot elimination is only possible at ideal switching speeds and in a very narrow margin, and these concerns are addressed in the following chapter.

Chapter 6

Expanding Zero Overvoltage Switching Range of Power Switches Through Controlled Turn-Off

This chapter is adapted from the following publication:

E. P. D. Toit and I. W. Hofsjager, 'Expanding Zero Overvoltage Switching Range of Power Switches Through Controlled Turn-Off', *IEEE Access*

Submitted

The author of this thesis conceptualised the study, conducted the analysis, developed the models, and wrote the original draft of the paper.

6.1 Introduction

In the previous chapters, ZOS emerged as a promising candidate for oscillation suppression in next-generation UWBG devices. However, its practicality remains limited due to two significant drawbacks: it relies on ideal switching conditions and operates effectively only within a highly restricted range of variables. These limitations currently render the method unviable. Additionally, we have seen that the only main requirement for overshoot elimination is simply to achieve ideal energy in the parasitic components at T_{Clamp} .

This chapter investigates and overcomes the main drawbacks of ZOS to allow for voltage overshoot elimination over a large range of circuit parameters and at non-ideal switching by updating the mathematical model to allow for controlled turn-off of the switch. The turn-off switch current, $I_{Switch}(t)$, in the model, is updated to be a linear decaying current source with two adjustable segments instead of one. This two-segment turn-off current is able to emulate much

more complicated functions while still being simple enough so that a few variables can describe the function, and it can still be described and solved mathematically.

6.2 Optimisation of Controlled Turn-Off

The first step is to describe the new two-segment turn-off switching current mathematically. The period P1 is broken up into P1A and P1B to represent the different current functions. This representation of the current is a very important part of being able to describe the system as a whole mathematically. This derivation can be seen in Fig. 6.1 below:

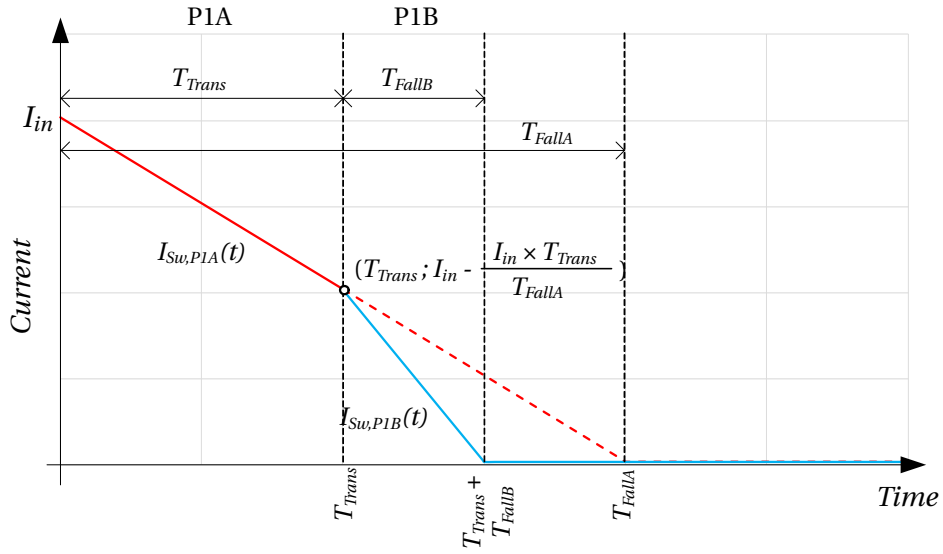


Fig. 6.1 Adjustable current turn-off waveform through the switch

The function for the first segment is still the same as in previous chapters, as described below:

$$I_{Sw,P1A}(t) = I_{In} - \frac{I_{In}}{T_{FallA}(t)} \quad (6.1)$$

The function for the second segment can be derived by substituting two known points into the line equation and solving the unknowns. The following equation is then derived and will always be applicable to describe to second part of the current turn-off:

$$I_{Sw,P1B}(t) = \frac{I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans})}{T_{FallA}}(t - T_{Trans}) + I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans}) \quad (6.2)$$

In these equations, T_{FallA} is the time taken from $t = 0$ to where $I_{Sw,P1A}(t)$ would have crossed the x-axis, T_{Trans} is the time taken from $t = 0$ to where the switching current transitions from

$I_{Sw,P1A}(t)$ to $I_{Sw,P1B}(t)$ and T_{FallB} is the time taken from $t = T_{Trans}$ to $t = T_{FallB}$. The only constraint is that $T_{Trans} < T_{FallA}$.

This representation can approximate almost all turn-off characteristics. The use of linear equations also keeps the eventual math as simple as possible without introducing higher-order events to the equations, as the intent of this research is to provide fundamental knowledge, not real-world scenarios.

This circuit with adjustable current turn-off can be modelled by applying classical circuit theory, where the equivalent circuit of each period is analysed independently by applying KCL and KVL to solve the circuit variables of the Fast-turn-off equivalent circuits in *Fast-Mode* circuit progressions of Fig. 4.4.

The functions of $I_{LPar}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$ can then be solved from P1A to P2 by performing the Laplace transforms on the differential equations of a given period, solving the functions, and performing the inverse Laplace transform to convert the functions back to the time domain, exactly like completed in Chapter 4. The equations are made particularly complicated by the inclusion of the initial conditions of the previous time period and keeping the equations in a closed form. The corresponding time domain equations for each period can be found in Appendix B.

These equations are then the mathematical description of the time domain representation of the system as a whole. When the equations from the appendix are populated with typical values from Table 4.1 with corresponding fast turn-off time, an example of the resulting waveforms can be seen in Fig. 6.2. These waveforms were also simulated to verify the integrity of the equations.

T_{Clamp} is the moment the diode turns on, and it can be seen that the values of $I_{LPar}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$ at T_{Clamp} are the initial conditions for P3, and define what the eventual overshoot will be. From the waveforms in Fig. 6.2, it can be seen that with the chosen turn-off current, the overshoot of the turn-off switching event will be 10%.

The main idea of this representation of the current turn-off is to accurately control the energy in the passive components while still achieving a fast turn-off. This representation is then able to display any fast or slow start of the transition and fast or slow end to the transition, and the results can be observed. It is very quickly seen that this manipulation of the turn-off current has a very large influence on the resulting overshoot, and this influence is discussed and observed in the next section.

It must also be said that the derivation of such a model can become very complicated, so all the results were also verified in simulation software.

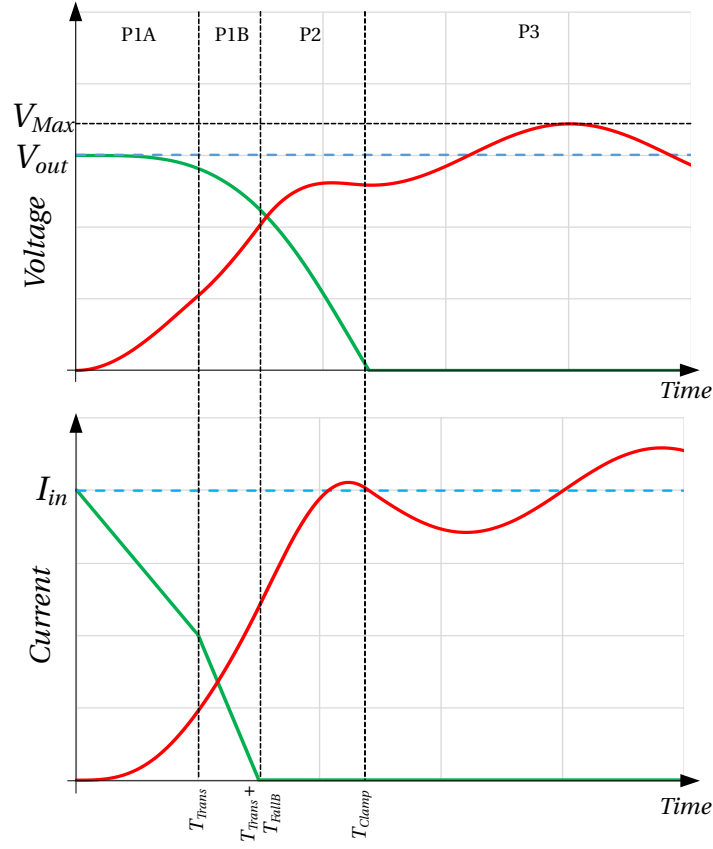


Fig. 6.2 Resulting voltage and current waveforms produced by the circuit model equations

6.2.1 Observation of the Influence of Turn-off Current Waveform on the Voltage Overshoot

This section investigates the direct influence of adjusting the individual parameters of the turn-off current on $I_{LPAr}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$, and specifically on when T_{Clamp} occurs, which in turn defines the initial conditions for the overshoot period.

As there are three variables that define the turn-off current described above and seen in Fig. 6.1, the influence of these variables is investigated separately by illustrating the effect of when a specific variable changes and all other variables are kept the same. Firstly, the influences of changing the individual variables will be discussed, and thereafter, a holistic view will be discussed.

Influence of T_{FallA}

The variable of T_{FallA} will define the slope of the first segment of the turn-off current waveform, $I_{Sw,P1A}(t)$. The higher the value of T_{FallA} , the higher the slope of the turn-off current will be for the first segment, and the lower the value, the lower the slope will be. The example of the waveforms presented in Fig. 6.2 above is reinvestigated, but with a higher and lower value of T_{FallA} where the

red plot serves as the reference, the blue plot serves as a higher value for T_{FallA} and the green plot serves as a lower value for T_{FallA} .

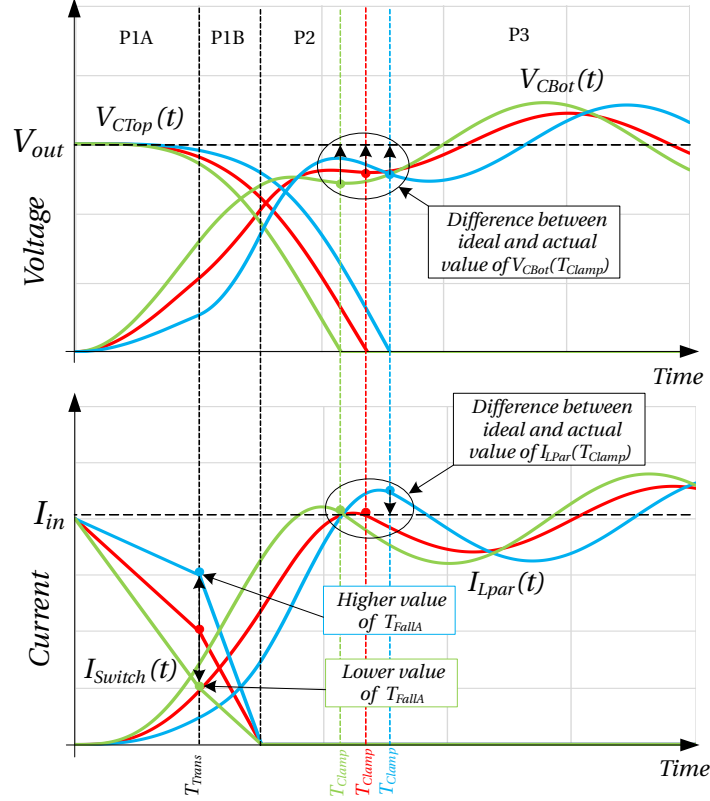


Fig. 6.3 Voltage and current waveforms when T_{FallA} is adjusted higher (blue) and lower (green)

The first observation is that when T_{FallA} is selected higher, T_{Clamp} will occur later so that P2 will last longer, and if T_{FallA} is selected lower, T_{Clamp} will occur earlier, so P2 will be shorter but by the same amount of time.

It can be seen that the difference in current between the actual and ideal steady-state values is very similar for the current at T_{Clamp} for all three plots, and the voltage difference between the actual and ideal steady-state values is significantly different only on the blue plot.

From the observation, it can already be seen that a change in T_{FallA} has a significant influence on $I_{Lpar}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$, but the interaction is too complicated to observe.

Influence of T_{Trans}

The variable of T_{Trans} is the x-axis value of where the applicable period changes from P1A to P1B and the function changes from the turn-off function changes $I_{Sw,P1A}(t)$ to $I_{Sw,P1B}(t)$. In the waveforms presented in Fig. 6.4, the red plot serves as the reference again, the blue plot serves as a higher value for T_{Trans} , and the green plot serves as a lower value for T_{Trans} .

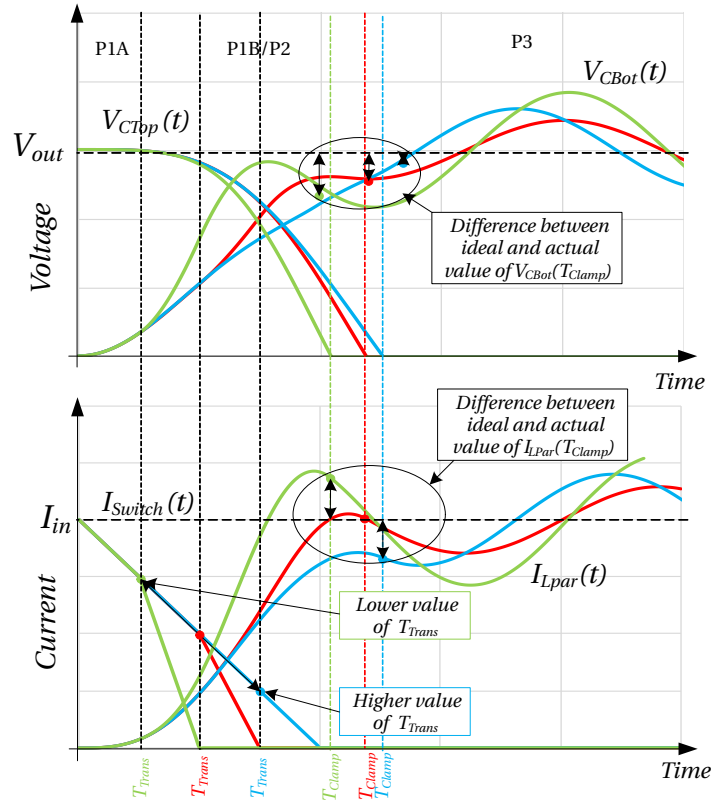


Fig. 6.4 Voltage and current waveforms when T_{Trans} is adjusted higher (blue) and lower (green)

As with the change in when T_{FallA} , T_{Clamp} also changes the same amount based on the same change of T_{Trans} . When T_{Trans} is selected smaller, T_{Clamp} will be smaller by the same amount as when T_{Trans} is selected larger.

As with the change in T_{FallA} , it can also be seen that a change in T_{Clamp} has a significant influence on $I_{LPar}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$, but the interaction is too complicated to observe.

Influence of T_{FallB}

The variable T_{FallB} is the time from T_{Trans} to where the switch fully opens and also defines the slope and duration of $I_{Sw,P1B}(t)$. The illustration of this change can be seen in Fig. 6.5 below. In the waveforms presented in Fig. 6.5, the red plot serves as the reference again, the blue plot serves as a higher value for T_{FallB} , and the green plot serves as a lower value for T_{FallB} .

For this change in T_{FallB} , it can be seen that the $V_{CBot}(T_{Clamp})$ increases slightly as T_{FallB} increases, but the $I_{LPar}(T_{Clamp})$ drops quite significantly. The change in T_{FallB} also has a small influence on when T_{Clamp} occurs. It must be noted that the effect of the change in T_{FallB} would be much smaller if T_{Trans} is large, and vice versa.

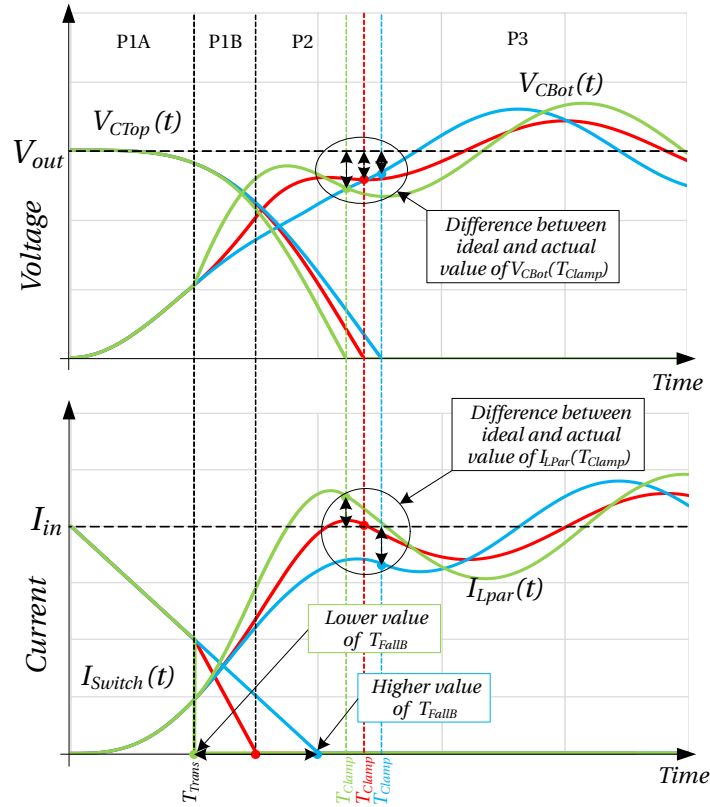


Fig. 6.5 Voltage and current waveforms when T_{FallB} is adjusted higher (blue) and lower (green)

Summary of influence of variables

The most significant finding from the comparison is that the interaction is very complex, and changing a single variable has several side effects, and a correlation between the change of any single and a specific waveform could not be observed. It can be seen that the reactive components determine the frequency of the oscillation.

To get a better idea of the influence of the change of variables and more of a holistic view of the results, a summarised table of all the waveform results can be seen below in Table 6.1. In this table, the changes in T_{Clamp} and the mismatch of $I_{LPar}(T_{Clamp})$ and $V_{Switch}(T_{Clamp})$ between the base case and the variations are documented and can then be directly compared, and from these results, the actual mismatch in energy can be calculated.

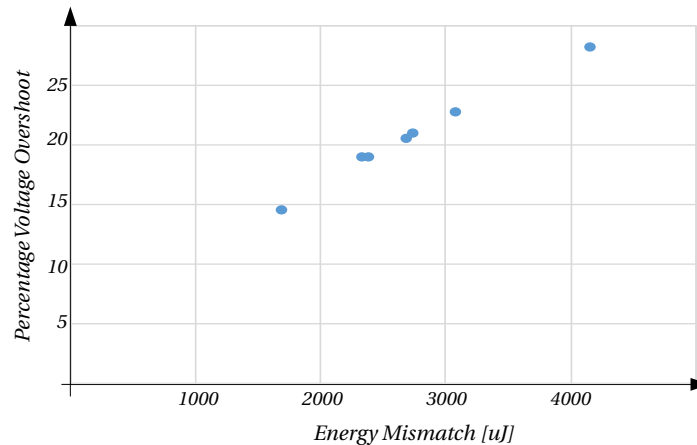
From the table, it can be seen that the area under the curve of the turn-off current function is directly correlated with the change in T_{Clamp} . It can also be seen that the voltage at T_{Clamp} was lower for every combination of the turn-off current variables, indicating that this would be an important but difficult goal to achieve.

In Chapter 5, the argument is made that the energy mismatch of $I_{LPar}(T_{Clamp})$ and $V_{CBot}(T_{Clamp})$ both together would define the overshoot, and this argument can be further investigated with

Table 6.1 Comparison of results when changing single variables of the current turn-off waveform

Case	Reference	Change of T_{Clamp}	$I_L(t)$ mismatch @ T_{Clamp}			$V_{Switch}(t)$ mismatch @ T_{Clamp}			Total energy Mis-match	Voltage overshoot Percent-age
			Current	Percentage	Energy (nJ)	Voltage	Percentage	Energy (nJ)		
Base-case	Fig. 6.2	N/A	0.16 A	1%	49.20	-41.87	-14%	1,635.82	1,685.03	15%
Higher T_{FallA}	Fig. 6.3 (Blue)	8%	2.20	11%	696.27	-43.98	-15%	1982.37	2678.64	21%
Lower T_{FallA}	Fig. 6.3 (Green)	-9%	0.36	2%	109.53	-57.12	-19%	2627.51	2739.66	21%
Higher T_{Trans}	Fig. 6.4 (Blue)	5%	-3.25	-11%	-895.78	-33.41	-11%	1481.36	2377.14	19%
Lower T_{Trans}	Fig. 6.4 (Green)	-12%	3.69	15%	1209.12	-63.28	-21%	2938.07	4147.19	28%
Higher T_{FallB}	Fig. 6.5 (Blue)	6%	-3.31	-17%	-909.83	-32.07	-11%	1419.00	2328.83	19%
Lower T_{FallB}	Fig. 6.5 (Green)	-6%	2.05	10%	646.52	-52.98	-18%	2421.66	3068.18	23%

these results. So, a plot comparing the sum of the energy differences with the observed overshoot further emphasises this point, as seen in Fig. 6.6.

Fig. 6.6 Percentage voltage overshoot comparison with energy mismatch at T_{Clamp}

In this plot, it can be seen that the overshoot correlates almost linearly with the mismatch in energy. So, this greatly supports the idea that to minimise overshoot when switching to the progression where the diode clamps first, the aim must change from minimising the overshoot to minimising the sum of the difference in energy.

6.3 Turn-off Current Control for Voltage Overshoot Elimination

To be able to totally eliminate the voltage overshoot when switching in *Fast-Mode*, the current and voltage values must be at exactly the correct values at exactly the correct time. It was seen that this could be achieved with an ideal switch and picking the voltage, current, inductance

and capacitance at exactly the correct values so that this occurs naturally. However, this is a very impractical approach. It was then discussed that if the ideal switching is modelled as non-ideal with a linear decaying current, a single solution exists if the diode capacitor is larger than the switch capacitor, but this is also an impractical solution as only one point exists. However, these results do show that under some special cases, there exists a solution that is determined by the turn-off characteristics.

This must then mean that if the turn-off current can be manipulated, a window of solutions can be opened, and this theory is discussed in this chapter.

Therefore, if the requirements of overvoltage elimination are articulated again, as in Chapter 5, the equations below must be true simultaneously:

$$V_{CBot}(T_{Clamp}) = V_{Out} \quad (6.3)$$

And

$$I_{LPar}(T_{Clamp}) = I_{In} \quad (6.4)$$

This set of equations sets up an environment that cannot be solved mathematically in closed form, and the roots cannot be calculated, but they can serve as an objective function that can be optimised.

So if these equations are both set equal to zero and all the variables or the turn-off current (T_{FallA} , T_{FallB} , T_{Trans}) are included as unknowns in the environment, the following optimisation equation can be set up:

$$(I_L(T_{Clamp}, T_{FallA}, T_{FallB}, T_{Trans}) - I_{In}) + (V_{Switch}(T_{Clamp}, T_{FallA}, T_{FallB}, T_{Trans}) - V_{Out}) \quad (6.5)$$

The objective function can be minimised using the differential evolution method. While various optimisation techniques can be applied, differential evolution is chosen for its effectiveness in handling complex environments and non-linearities, as present in this scenario [89].

The primary goal of this optimisation is to demonstrate that adjusting turn-off current parameters can eliminate voltage overshoot across a broad range of voltage and current conditions.

Furthermore, the objective function can be extended to incorporate additional constraints, such as limiting the maximum slope of a specific semiconductor device.

The following section explores the concept of a "solution window". This refers to the conditions under which the objective function can be minimised to zero, given a specific combination of circuit parasitics, voltage, and current. If values for T_{FallA} , T_{FallB} , T_{Trans} exist that result in a zero-

value objective function, then a solution is feasible, ensuring that the resulting voltage waveform exhibits no overshoot.

This approach identifies the range of possible solutions where a solution exists.

6.3.1 Solution Window for change in current

When a practical converter is considered, the operating range is always a very important consideration as the load requirements vary, even if it is just a small amount. If a converter does not have an operating range but only an operation point, it would not be very practical, independent of how well it works at that one point.

This section first investigates the converter's current range with the parameters as specified in Table 4.1, with the only difference that the two-segment turn-off current is applied. So the values specified in Table 4.1 fed into the objective function, and this is repeated for a current value of 25% higher (25A) and 25% lower (15A), and it was found that an objection function could be minimised for al three of there current examples as seen below.

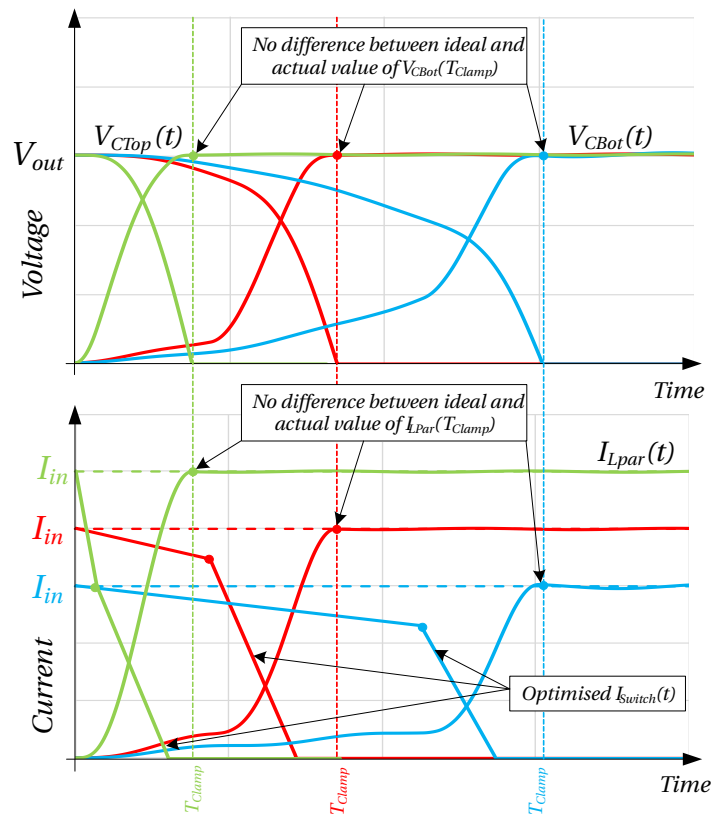


Fig. 6.7 Voltage and current waveforms when turn-off current has been optimised for three different current values

In these plots, the output voltage stays the same, even though the input current changes and the overshoot is still eliminated for all three scenarios by adapting the turn-off current, as was not possible before.

The most important observation of the resulting waveforms is that the value of T_{Trans} (indicated by the dot on the turn-off current) becomes smaller as the input current increases but larger as the input current decreases. This means that there is a lower limit to T_{Trans} but not an upper limit. This, in turn, means that for a given set of circuit variables, the implementation of an adjusting waveform has a current range from 0A to some upper limit and that the value of T_{Trans} determines the limits of the solution window. It can be seen that T_{Trans} of the 25A green example is very close to the y-axis, indicating that the chosen value of 25A is close to the upper current limit of the solution window.

The influence of the inductance and diode capacitance is investigated further to investigate the solution window of the input current. To achieve this, the objective function is optimised for a matrix of the input current and inductance value, with all other values kept the same, and thereafter, a matrix of the input current and diode capacitance, again with all other values kept the same. This matrix of points where solutions were possible and not possible could then be converted into a grid with the simplified results below in Fig. 6.8 and Fig. 6.9.

It must be noted that only the diode capacitance is varied in this exercise. This is done to specifically investigate the difference in the ratio between the diode capacitance and switch capacitance.

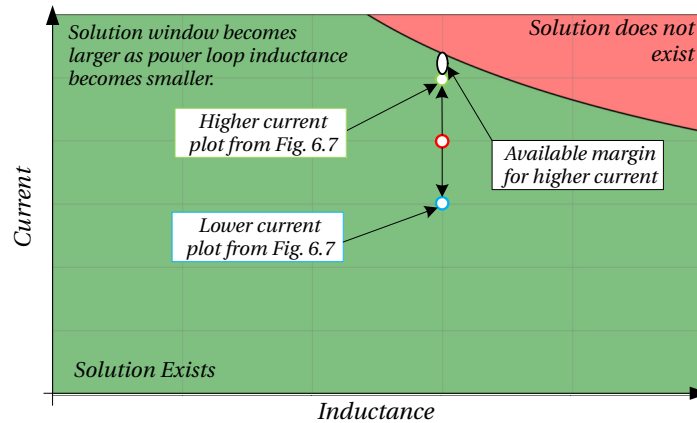


Fig. 6.8 Current solution window when parasitic inductance can be changed

Firstly, to interpret these diagrams, the three points representing the three waveforms in Fig. 6.7 can be seen in the solution window in 6.8 and 6.9 indicated by the red, blue and green points. In 6.8 it can then be seen that the range increases as the inductance lowers, but in 6.9, the range increases as the diode capacitance increases. This means that a smaller inductance when controlled turn-off is applied is also a good goal to attempt, as the possible solution window would be larger.

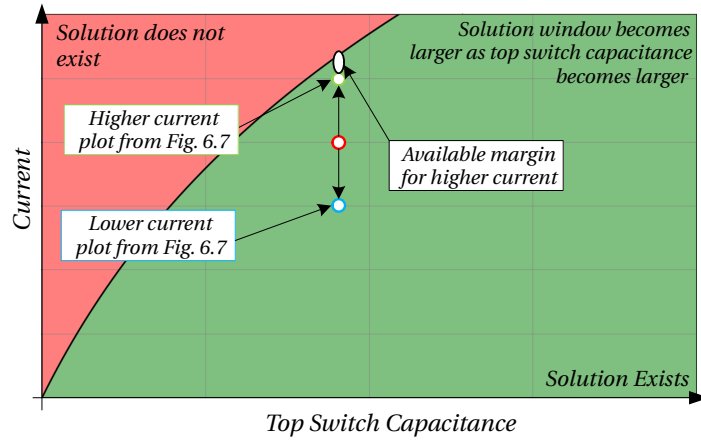


Fig. 6.9 Current solution window when diode capacitance can be changed

It can also be seen that T_{Trans} in the green plot in Fig. 6.7 still has a small amount of margin to become smaller. This translates to an upper current limit that is a bit higher than the current value of the green plot.

This leads to the conclusion that to increase the current range of a given circuit, the inductance can be minimised, and the diode capacitance can be increased.

6.3.2 Solution Window for change in voltage

This section follows the same approach as the current investigation in the previous section but applies the principles to investigate the voltage range and solution window.

As with the current solution, the objective function is first applied to determine the turn-off waveforms for three different voltages, and it is seen that solutions exist for the three different chosen voltage values. These values are 50V higher than the original 300V and 50V lower. The resulting waveforms can be seen in Fig. 6.10.

Fig. 6.10 shows voltage and current waveforms when the turn-off current has been optimised for three different voltage values. It can be seen that the opposite of the current is true for the voltage. An increase in voltage requires an increase in T_{Trans} , and a decrease in voltage requires a decrease in T_{Trans} . This means that the voltage has a lower limit for the given set of circuit variables but not an upper limit.

The objective function is then optimised to determine the influence the inductance and diode capacitance have on the voltage range of the solution, and the figures in Fig. 6.11 and Fig. 6.12 are produced.

Firstly, the three plots of Fig. 6.10 can be seen as the three data points on the solution window in 6.11 and Fig. 6.12. When the green plot in Fig. 6.10 is investigated, it is seen that T_{Trans} is on the minimum limit. This translates to the green plot being on the lower limit in both 6.11 and Fig. 6.12.

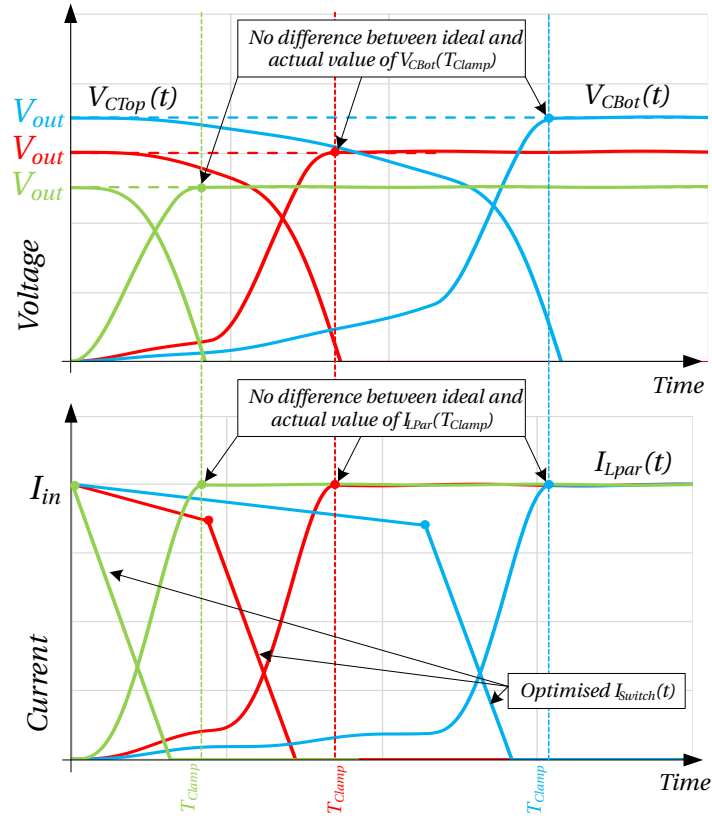


Fig. 6.10 Voltage and current waveforms when turn-off current has been optimised for three different voltage values

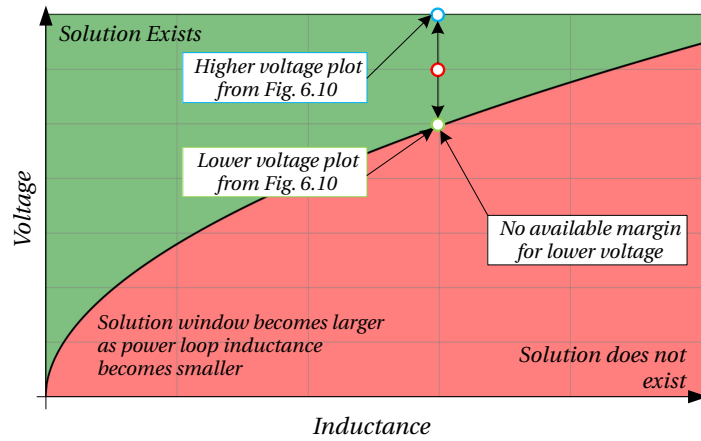


Fig. 6.11 Voltage solution window when parasitic inductance can be changed

Similar to the current, it can be seen that the voltage range will increase when the inductance is lowered, and the voltage range will also increase when the diode capacitance is increased.

It is seen that the switching speed is at a maximum when T_{Trans} (indicated by the dot on the turn-off current plots) is at a minimum. This is also when the current is close to the maximum

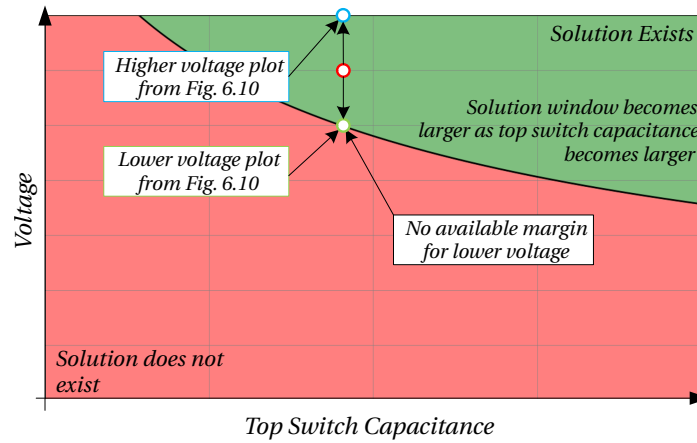


Fig. 6.12 Voltage solution window when parasitic diode capacitance can be changed

limit and the voltage is close to the minimum limit. So even though the current has a lower limit of zero, and the voltage has no upper limit, it is not advisable to switch in this region, as the switching speed would be slow, and thus, the losses would be high.

6.4 Conclusion

This chapter explored the role of controlled turn-off techniques in overcoming the limitations of ZOS, demonstrating that parasitic components are not necessarily the fundamental barrier to achieving faster switching. Through the development of a generalised mathematical model and an objective function that can be optimised, it was shown that shaping the switching current waveform allows for voltage overshoot elimination across a wide range of circuit parameters. The findings further show that lowering parasitic inductance and increasing diode capacitance can expand the range within which no overshoot occurs.

More importantly, this research does not aim to provide a design tool for specific applications but instead establishes a theoretical foundation for understanding the feasibility of applying UWBG devices in high-speed switching environments. The results identify solution windows where overshoot elimination is possible. These insights reinforce the broader objective of this thesis to contribute to the fundamental understanding of high-speed switching dynamics rather than presenting an application-based optimisation framework.

Chapter 7

Conclusions And Future Work

7.1 Conclusions

WBG semiconductor technology offers the ability to switch much faster than traditional devices, unlocking significant advantages such as higher efficiency and greater energy density. However, this increased switching speed also introduces challenges, particularly in the form of overvoltage and ringing at the switching node, which, in turn, has several negative side effects that limit the performance of the converter. These overshoots are primarily caused by the resonance of inherent parasitic components within the circuit. Minimising parasitic inductance has been the primary method to address this issue, and while it has been effective, it is becoming increasingly difficult to achieve further improvements, and complete elimination of parasitic inductance is impossible, creating a natural barrier that limits further increases in switching speed. However, the material development research field in semiconductor technology is in the process of developing UWBG materials that will be able to switch much faster than the existing WBG devices.

Most of the research in this field of suppressing the voltage overshoot has achieved sufficient suppression capabilities as the switching speed increases, but most of this research was done in isolation, not in the context of others that are attempting the same thing, as tends to happen in the greater field of power electronics.

This research aimed to provide a deeper understanding of this specific issue of voltage overshoot as well as the basic mechanisms of the switching transition, in general, to create a fundamental piece of new knowledge and bridge some of the gaps between these methods.

The first part of the unifying knowledge was developed in Chapter 3, where the framework was provided so that the experimental results of a switching transition could be compared to other switching events. This extraction and comparison was completed for several different suppression methods, and a database of the extracted data was presented. The comparison of this data revealed that it is important to compare the experimental switching results with others to ensure that those

results are indeed as relevant as initially assumed by their designers. Other conclusions of the investigation were that parasitic components in isolation do not predict the overshoot, higher voltage or power does not correlate with larger overshoot, and that the field of power electronics has progressed well in the last decade.

The comparison also identified a new method, Zero Overvoltage Switching, as a potential solution to overcoming the limitations imposed by parasitic inductance, with the possibility of improved performance as switching speeds increase. However, this method has two major drawbacks: (1) it relies on ideal switching conditions, and (2) even a slight deviation in any circuit parameter results in a significant overshoot, making practical implementation challenging and not feasible.

Although ZOS was not yet feasible in its current form, it presented a potential pathway for making UWBG devices viable. Furthermore, its unexpected results suggested the presence of an underlying phenomenon that required deeper investigation to be fully understood and addressed. To explore this, a fundamental model of the turn-off switching transition was developed using circuit theory in Chapter 4 to analyse the switching transition, particularly under very fast switching conditions. This investigation revealed that at very high switching speeds, the switching device could turn off before the diode clamps, resulting in an alternative equivalent circuit progression to conventional switching. This new insight provided a clear theoretical basis for the unexpected behaviour observed with ZOS while simultaneously reconciling it with conventional switching expectations. It also demonstrated that many conventional assumptions and expectations about switching transitions no longer hold at these extreme speeds.

Chapter 5 introduced an energy-based explanation for the fundamental mechanism of the voltage overshoots, demonstrating that achieving ideal energy values at the precise moment of the diode clamping can prevent overshoot entirely. Using this energy-based explanation, it was seen that ideal energy at the correct time is possible when switching very fast but not when switching conventionally.

As the fundamentals of switching transition were now understood, the new knowledge could be used to further develop ZOS into a solution that would be used on a wide range of parameters and without ideal switching. Driven by the requirement of ideal energy at the correct time for overshoot elimination, the mathematical model was further refined to accommodate two segments in the switch's turn-off current waveform. By adjusting the turn-off current, it was possible to create an objective function for eliminating overshoot. The objective function could then be optimised to determine the required turn-off characteristics so that the overshoot would be eliminated. If the objective function could not be minimised, it would be indicated that a solution is not possible and that the overshoot cannot be eliminated for that set of circuit parameters. This analysis revealed that a solution window exists where an adjustable turn-off current can eliminate overshoot, even under non-ideal switching conditions. As a result, the major drawback of ZOS—its reliance

on narrow, ideal conditions—could be addressed, offering a wider solution window, making the technique more practical for real-world applications, and ultimately providing a feasible oscillation suppression method for devices like UWBG.

Although this research is not intended as a practical design guide, it is meant to serve as a fundamental and unifying contribution, where the principles would be used to overcome the limitations of parasitic inductance and provide future devices with a possible switching solution.

7.2 Future Work

The research conducted in this thesis opens several avenues for further development, particularly in advancing the foundational understanding of *Fast-Mode* switching and in establishing a more unified theoretical framework for power electronics. While this work has provided key insights into ZOS and its potential in high-speed switching, further theoretical exploration is needed to fully integrate these findings into a broader understanding of switching transitions. The field of power electronics remains fragmented, with many advancements being driven by isolated, application-specific solutions rather than a cohesive theoretical foundation. Future research should focus on bridging these gaps, developing a comprehensive theory that unifies the interactions between switching dynamics, parasitic effects, and energy at high speeds. This would provide a stronger basis for guiding future developments in high-performance power electronics, ensuring that advancements are built on a well-defined theoretical structure rather than empirical observations alone.

A key aspect of this effort is deepening the understanding of *Fast-Mode* switching. The behaviours observed at extremely high speeds, as detailed in Chapters 4 and 5, challenge many conventional assumptions about switching transitions. Future work should focus on refining and extending the models presented in this thesis to account for a wider range of operating conditions. The fundamental energy mechanisms that enable ZOS must also be further explored to determine whether they represent a distinct shift in switching behaviour or a special case within a broader theoretical framework. By solidifying the theoretical foundation of *Fast-Mode*, researchers can better define the boundaries of high-speed switching and develop a more general set of principles that govern device operation beyond the limits of conventional power electronics theory.

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Appendix A

Mathematical Derivation of Circuit Model with Single Segment

To be able to understand what happens in the circuit of a common switching node when the switch is turned off, the switch characteristics that have the largest influence must be modelled while still keeping the circuit simple enough to analyse mathematically.

In this case, the parasitic components and the current turn-off characteristics must be explicitly modelled. The circuit from Fig. 1.2 can be adjusted to include a current source with a linear current decay to model the current turn-off waveform of the transistor, as shown below in Fig. A.1. (This is a duplicate of Fig. 4.2 for clarity.)

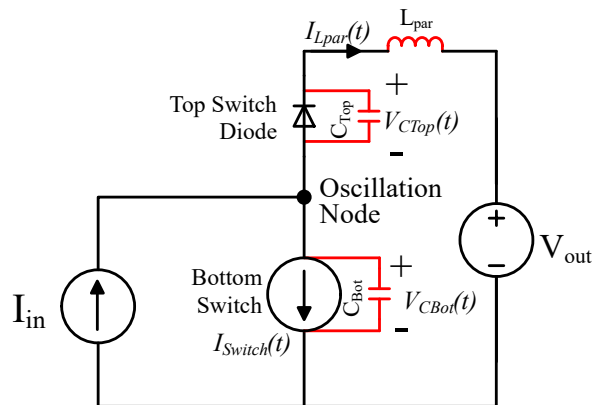


Fig. A.1 Modified Equivalent circuit of a commutation cell in boost mode (duplicate)

As the investigation focuses only on a very short time period, several assumptions are made to avoid excessive complexity in the calculations. These assumptions are as follows:

- I_{in} is constant.
- V_{out} is constant.

- The transistor's turn-off current is linear.
- Equivalent resistance is not modelled.
- The parasitic capacitances of the transistor and the diode are not equal.

In this analysis, the transistor current, $I_{Switch}(t)$, is the only dynamic variable.

As the transistor current $I_{Switch}(t)$ changes, the following variables must be explicitly calculated as secondary effects:

- The voltage across the top capacitor, $V_{CTop}(t)$.
- The voltage across the bottom capacitor, $V_{CBot}(t)$.
- The inductor current, $I_{LPar}(t)$.

To determine the time-domain analysis of the circuit, circuit theory is applied to determine the waveform of the three variables above. The circuit progresses through three equivalent circuits until a steady state is achieved.

Depending on the choice of transistor current, the progression of the circuit to a steady state will not be the same, and thus, two modes of operation are analysed, as seen in the Fig. A.2. (This is a duplicate of Fig. 4.4 for clarity.)

A.1 *Fast-Mode* Operation

In *Fast-Mode*, the transistor current $I_{Switch}(t)$ reaches 0 A before the top capacitor voltage $V_{CTop,FM,P1}(t)$ reaches 0 V. The circuit can then be modelled in three associated time periods:

- *Fast-Mode* Period 1 (FM,P1) is applicable for $0 < t < T_{Fall}$.
- *Fast-Mode* Period 2 (FM,P2) is applicable for $T_{Fall} < t < T_{Clamp}$.
- *Fast-Mode* Period 3 (FM,P3) is applicable for $T_{Clamp} < t < \infty$.

Where T_{Fall} refers to when the bottom switch current reaches 0 A, and T_{Clamp} refers to when the top capacitor reaches 0 V.

To determine the time-domain equations of the variables for each time period, the following classical approach is used:

- Step 1: Convert each differential equation to its corresponding Laplace Transform.

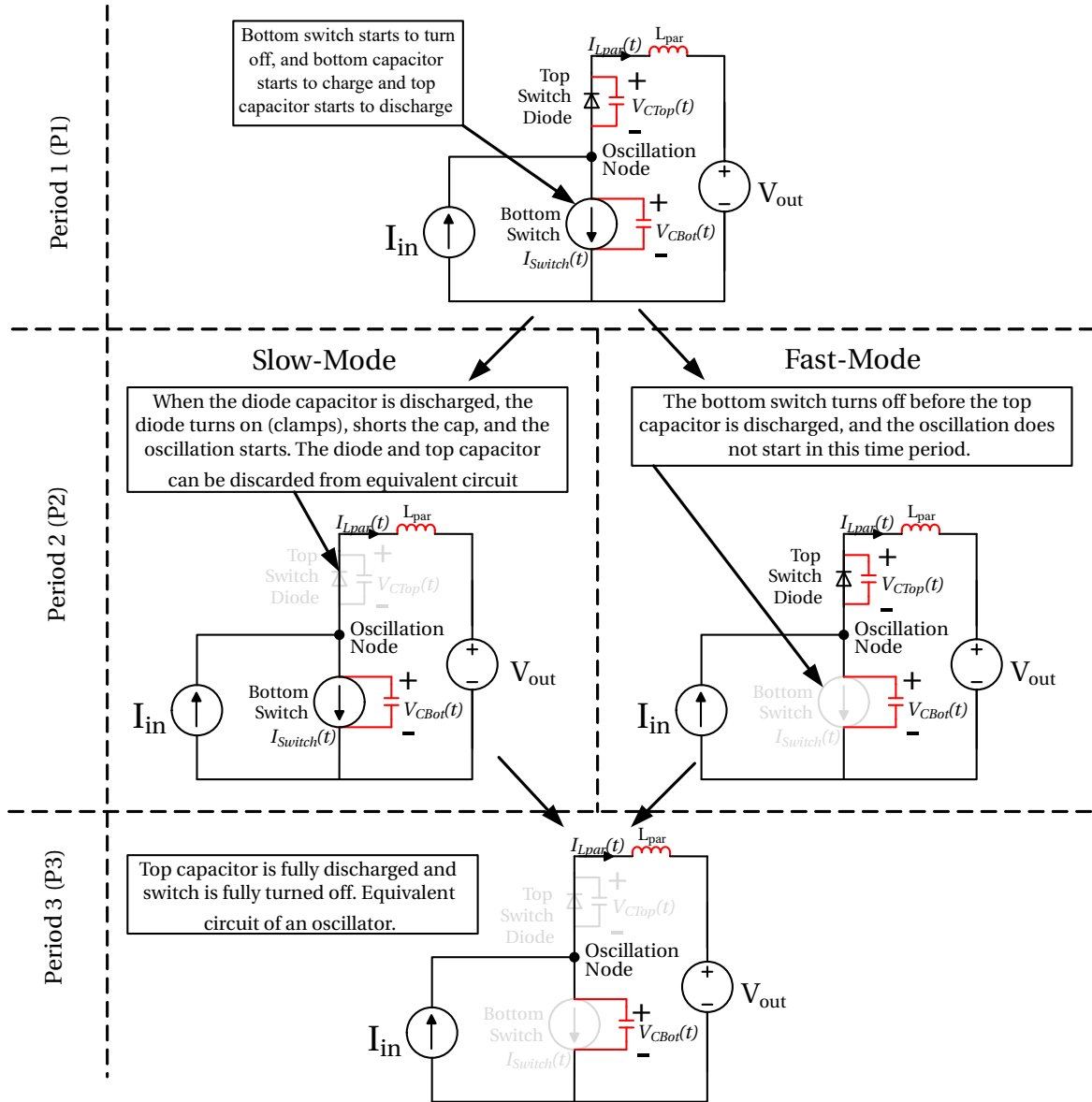


Fig. A.2 Alternative equivalent circuit progression for Slow-Mode

- Step 2: Solve the Laplace transform mathematically.
- Step 3: Find the inverse Laplace Transform to get the time-domain solution.

The results from each period are used as the initial values for the next period. Due to this, the math becomes quite complex, even though assumptions such as linear transistor current and no damping resistance are used.

To minimise errors in the model, software packages such as Java and Mathematica are used to solve the differential equations and compute the inverse Laplace transforms. These results are later verified through simulation and will be discussed in the following sections.

Special attention was given to keeping the model in mathematical form to extract as much information as possible.

Since the resulting equations for $V_{CTop}(t)$, $V_{CBot}(t)$, and $I_{LPar}(t)$ will differ for each time period, these variables will have a subscript referring to the specific mode and time period.

A.1.1 Fast-Mode – Period 1 circuit analysis

The applicable circuit for the time period $0 < t < T_{Fall}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{CTop,FM,P1}(t) + I_{CBot,FM,P1}(t) + I_{Switch}(t) \quad (A.1)$$

Where $I_{Switch} = I_{in} - \frac{I_{in}}{T_{Fall}}(t)$ for linear decay of the transistor current. Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,FM,P1}(t)}{dt} + C_{Bot} \frac{dV_{CBot,FM,P1}(t)}{dt} + I_{in} - \frac{I_{in}}{T_{Fall}}(t) \quad (A.2)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,FM,P1}(s) - V_{CTop,FM,P1}(0)) + C_{Bot} (sV_{CBot,FM,P1}(s) - V_{CBot,FM,P1}(0)) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} \quad (A.3)$$

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,FM,P1}(s) - V_{out}) + C_{Bot} (sV_{CBot,FM,P1}(s) - 0) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} \quad (A.4)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar}(t) = I_{CTop,FM,P1}(t) \quad (A.5)$$

Thus:

$$I_{LPar}(t) = -C_{Top} \frac{dV_{CTop,FM,P1}(t)}{dt} \quad (A.6)$$

The Laplace transform of this equation can be written as:

$$I_{LPar}(t) = -C_{Top} (sV_{CTop,FM,P1}(s) - V_{CTop,FM,P1}(0)) \quad (A.7)$$

$$I_{LPar}(t) = -C_{Top}(sV_{CTop,FM,P1}(s) - V_{out}) \quad (A.8)$$

The initial condition for this time period is simply the initial conditions as seen in the original circuit.

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,FM,P1}(t) + V_{CBot,FM,P1}(t) - V_{L,FM,P1}(t) \quad (A.9)$$

Thus:

$$V_{out} = V_{CTop,FM,P1}(t) + V_{CBot,FM,P1}(t) - L \frac{dI_{LPar,FM,P1}(t)}{dt} \quad (A.10)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,FM,P1}(s) + V_{CBot,FM,P1}(s) - L(sI_{LPar,FM,P1}(s) - I_{LPar,FM,P1}(0)) \quad (A.11)$$

$$\frac{V_{out}}{s} = V_{CTop,FM,P1}(s) + V_{CBot,FM,P1}(s) - L(sI_{LPar,FM,P1}(s) - 0) \quad (A.12)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$I_{LPar,FM,P1}(t) = \frac{C_{Top}I_{in} \left(t - \sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}} \sin \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}} \right) \right)}{(C_{Bot} + C_{Top})T_{Fall}} \quad (A.13)$$

$$V_{CTop,FM,P1}(t) = \left(2C_{Bot}C_{Top}I_{in}L_{Par} - (C_{Bot} + C_{Top})I_{in}t^2 + 2(C_{Bot} + C_{Top})^2T_{Fall}V_{out} \right. \\ \left. - 2C_{Bot}C_{Top}I_{in}L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}} \right) \right) / 2(C_{Bot} + C_{Top})^2T_{Fall} \quad (A.14)$$

$$V_{CBot,FM,P1}(t) = \frac{I_{in}(2C_{Top}^2 L_{Par} + C_{Bot}t^2 + C_{Top}t^2 - 2C_{Top}^2 L_{Par} \cos\left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}}\right))}{2(C_{Bot} + C_{Top})^2 T_{Fall}} \quad (A.15)$$

A.1.2 Fast-Mode – Period 2 circuit analysis

The applicable circuit for the time period $T_{Fall} < t < T_{Clamp}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

As the current source has reached 0A in the previous time frame, the current source is simply removed for the analysis of this circuit. As stated above, in this time period, it is important to remember that the initial conditions for this time period are the final conditions for the previous time period. From this diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found:

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{CTop,FM,P2}(t) + I_{CBot,FM,P2}(t) \quad (A.16)$$

Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,FM,P2}(t)}{dt} + C_{Bot} \frac{dV_{CBot,FM,P2}(t)}{dt} \quad (A.17)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,FM,P2}(s) - V_{CTop,FM,P2}(0)) + C_{Bot} (sV_{CBot,FM,P2}(s) - V_{CBot,FM,P2}(0)) \quad (A.18)$$

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,FM,P2}(s) - V_{CTop,FM,P1}(T_{Fall})) + C_{Bot} (sV_{CBot,FM,P2}(s) - V_{CBot,FM,P1}(T_{Fall})) \quad (A.19)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar,FM,P2}(t) = I_{CTop,FM,P2}(t) \quad (A.20)$$

Thus:

$$I_{LPar,FM,P2}(t) = -C_{Top} \frac{dV_{CTop,FM,P2}(t)}{dt} \quad (A.21)$$

The Laplace transform of this equation can be written as:

$$I_{LPar,FM,P2}(t) = -C_{Top} (sV_{CTop,FM,P2}(s) - V_{CTop,FM,P2}(0)) \quad (A.22)$$

$$I_{LPar,FM,P2}(t) = -C_{Top} (sV_{CTop,FM,P2}(s) - V_{CTop,FM,P1}(T_{Fall})) \quad (A.23)$$

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,FM,P2}(t) + V_{CBot,FM,P2}(t) - V_{LPar,FM,P2}(t) \quad (A.24)$$

Thus:

$$V_{out} = V_{CTop,FM,P2}(t) + V_{CBot,FM,P2}(t) - L \frac{dI_{LPar,FM,P2}(t)}{dt} \quad (A.25)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,FM,P2}(s) + V_{CBot,FM,P2}(s) - L (sI_{LPar,FM,P2}(s) - I_{LPar,FM,P2}(0)) \quad (A.26)$$

$$\frac{V_{out}}{s} = V_{CTop,FM,P2}(s) + V_{CBot,FM,P2}(s) - L (sI_{LPar,FM,P2}(s) - I_{LPar,FM,P1}(T_{Fall})) \quad (A.27)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$I_{LPar,FM,P2}(t) = C_{Top} I_{in} \left(\frac{1}{C_{Bot} + C_{Top}} - \frac{\sqrt{C_{Bot} C_{Top} L_{Par}} \left(\sin \left(\frac{T_{Fall} - t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) + \sin \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \right)}{(C_{Bot} + C_{Top})^{3/2} T_{Fall}} \right) \quad (A.28)$$

$$\begin{aligned}
V_{CTop,FM,P2}(t) = & ((C_{Bot} + C_{Top})^2 T_{Fall} (I_{in}(T_{Fall} - 2t) + 2(C_{Bot} + C_{Top})V_{out}) + 2C_{Bot}C_{Top}I_{in} \\
& + L_{Par} \cos \left[\frac{T_{Fall} - t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right] - 2C_{Bot}C_{Top}I_{in}L_{Par} \cos \left[\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right]) / \\
& (2(C_{Bot} + C_{Top})^2 T_{Fall}) \quad (A.29)
\end{aligned}$$

$$\begin{aligned}
V_{CBot,FM,P2}(t) = & -((I_{in}((C_{Bot} + C_{Top})T_{Fall}(T_{Fall} - 2t) - 2C_{Top}^2 L_{Par} \cos \left(\frac{T_{Fall} - t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& + 2C_{Top}^2 L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right))) / (2(C_{Bot} + C_{Top})^2 T_{Fall}) \quad (A.30)
\end{aligned}$$

A.1.3 Fast-Mode – Period 3 circuit analysis

The applicable circuit for the time period $T_{Clamp} < t < \infty$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

From this diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{CTop,FM,P3}(t) + I_{CBot,FM,P3}(t) \quad (A.31)$$

Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,FM,P3}(t)}{dt} + C_{Bot} \frac{dV_{CBot,FM,P3}(t)}{dt} \quad (A.32)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,FM,P3}(s) - V_{CTop,FM,P3}(0)) + C_{Bot} (sV_{CBot,FM,P3}(s) - V_{CBot,FM,P3}(0)) \quad (A.33)$$

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top} (sV_{CTop,FM,P3}(s) - V_{CTop,FM,P2}(T_{Clamp} - T_{Fall})) \\ & + C_{Bot} (sV_{CBot,FM,P3}(s) - V_{CBot,FM,P2}(T_{Clamp} - T_{Fall})) \end{aligned} \quad (A.34)$$

Kirchhoff's Voltage Law

$$V_{out} = V_{CBot,FM,P3}(t) - V_{LPar,FM,P3}(t) \quad (A.35)$$

Thus:

$$V_{out} = V_{CBot,FM,P3}(t) - L \frac{dI_{LPar,FM,P3}(t)}{dt} \quad (A.36)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CBot,FM,P3}(s) - L (sI_{LPar,FM,P3}(s) - I_{LPar,FM,P3}(0)) \quad (A.37)$$

$$\frac{V_{out}}{s} = V_{CBot,FM,P3}(s) - L (sI_{LPar,FM,P3}(s) - I_{LPar,FM,P2}(T_{Clamp} - T_{Fall})) \quad (A.38)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$\begin{aligned}
I_{LPar,FM,P3}(t) = & (2(C_{Bot} + C_{Top})^2 I_{in} \sqrt{L_{Par}} T_{Fall} - 2 \cos \left[\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}} \right] (C_{Top}^{3/2} \sqrt{C_{Bot}(C_{Bot} + C_{Top})} \\
& I_{in} L_{Par} \sin \left[\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] + I_{in} \sqrt{L_{Par}} (C_{Bot}(C_{Bot} + C_{Top}) T_{Fall}) - C_{Top}^{3/2} \\
& \sqrt{C_{Bot}(C_{Bot} + C_{Top}) L_{Par}} \sin \left[\frac{T_{Clamp} - T_{Fall}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] + \sqrt{C_{Bot}} ((C_{Bot} + C_{Top}) T_{Fall} \\
& (I_{in}(-2T_{Clamp} + T_{Fall}) + 2(C_{Bot} + C_{Top}) V_{out}) + 2C_{Top}^2 I_{in} L_{Par} \\
& \cos \left[\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] - 2C_{Top}^2 I_{in} L_{Par} \cos \left[\frac{T_{Clamp} - T_{Fall}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right]) \\
& \sin \left[\frac{T_{Clamp} - t}{\sqrt{C_{Bot} L_{Par}}} \right] / \left(2(C_{Bot} + C_{Top})^2 \sqrt{L_{Par}} T_{Fall} \right) \quad (A.39)
\end{aligned}$$

$$\begin{aligned}
V_{CBot,FM,P3}(t) = & V_{out} - (((C_{Bot} + C_{Top})^2 T_{Fall} (I_{in}(-2T_{Clamp} + T_{Fall}) + 2(C_{Bot} + C_{Top}) V_{out}) \\
& + 2C_{Top}^2 I_{in} L_{Par} \cos \left[\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] - 2C_{Top}^2 I_{in} L_{Par} \cos \left[\frac{T_{Clamp} - T_{Fall}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right]) \\
& \cos \left[\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}} \right] / \left(2(C_{Bot} + C_{Top})^2 T_{Fall} \right) + I_{in} (C_{Bot}^{3/2} \sqrt{L_{Par}} T_{Fall} + \\
& C_{Top} \sqrt{C_{Bot} L_{Par}} T_{Fall} + C_{Top}^{3/2} \sqrt{C_{Bot} + C_{Top}} L_{Par} \sin \left[\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] - C_{Top}^{3/2} \\
& \sqrt{C_{Bot} + C_{Top}} L_{Par} \sin \left[\frac{T_{Clamp} - T_{Fall}}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right] \sin \left[\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}} \right] / ((C_{Bot} + C_{Top})^2 T_{Fall}) \quad (A.40)
\end{aligned}$$

A.2 Slow-Mode Operation

In *Slow-Mode*, the capacitor voltage $V_{CTop,FM,P1}(t)$ reaches 0 V before the transistor current $I_{Switch}(t)$ reaches 0 A. The circuit can then be modelled in three associated time periods:

- *Slow-Mode* Period 1 (SM,P1) is applicable for $0 < t < T_{Clamp}$.
- *Slow-Mode* Period 2 (SM,P2) is applicable for $T_{Clamp} < t < T_{Fall}$.
- *Slow-Mode* Period 3 (SM,P3) is applicable for $T_{Fall} < t < \infty$.

Where T_{Fall} refers to when the bottom switch current reaches 0 A, and T_{Clamp} refers to when the top capacitor, as seen in the previous section, reaches 0 V.

To determine the time-domain equations of the variables for each time period, the following classical approach is used:

- Step 1: Convert each differential equation to its corresponding Laplace Transform.
- Step 2: Solve the Laplace transform mathematically.
- Step 3: Find the inverse Laplace Transform to get the time-domain solution.

Since the resulting equations for $V_{CTop}(t)$, $V_{CBot}(t)$, and $I_{LPar}(t)$ will differ for each time period, these variables will have a subscript referring to the specific mode and time period.

A.2.1 Slow-Mode – Period 1 circuit analysis

The applicable circuit for the time period $0 < t < T_{Clamp}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

It must be noted that this section is the same as *Fast-Mode* Period 1, but is repeated for consistency.

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{CTop,SM,P1}(t) + I_{CBot,SM,P1}(t) + I_{Switch}(t) \quad (A.41)$$

Where $I_{Switch} = I_{in} - \frac{I_{in}}{T_{Fall}}(t)$ for linear decay of the transistor current. Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,SM,P1}(t)}{dt} + C_{Bot} \frac{dV_{CBot,SM,P1}(t)}{dt} + I_{in} - \frac{I_{in}}{T_{Fall}}(t) \quad (A.42)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,SM,P1}(s) - V_{CTop,SM,P1}(0)) + C_{Bot} (sV_{CBot,SM,P1}(s) - V_{CBot,SM,P1}(0)) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} \quad (A.43)$$

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,SM,P1}(s) - V_{out}) + C_{Bot} (sV_{CBot,SM,P1}(s) - 0) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} \quad (A.44)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar}(t) = I_{CTop,SM,P1}(t) \quad (A.45)$$

Thus:

$$I_{LPar}(t) = -C_{Top} \frac{dV_{CTop,SM,P1}(t)}{dt} \quad (A.46)$$

The Laplace transform of this equation can be written as:

$$I_{LPar}(t) = -C_{Top} (sV_{CTop,SM,P1}(s) - V_{CTop,SM,P1}(0)) \quad (A.47)$$

$$I_{LPar}(t) = -C_{Top} (sV_{CTop,SM,P1}(s) - V_{out}) \quad (A.48)$$

The initial condition for this time period is simply the initial conditions as seen in the original circuit.

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,SM,P1}(t) + V_{CBot,SM,P1}(t) - V_{LPar,SM,P1}(t) \quad (A.49)$$

Thus:

$$V_{out} = V_{CTop,SM,P1}(t) + V_{CBot,SM,P1}(t) - L \frac{dI_{LPar,SM,P1}(t)}{dt} \quad (A.50)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,SM,P1}(s) + V_{CBot,SM,P1}(s) - L (sI_{LPar,SM,P1}(s) - I_{LPar,SM,P1}(0)) \quad (A.51)$$

$$\frac{V_{out}}{s} = V_{CTop,SM,P1}(s) + V_{CBot,SM,P1}(s) - L(sI_{LPar,SM,P1}(s) - 0) \quad (A.52)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$I_{LPar,SM,P1}(t) = \frac{C_{Top}I_{in} \left(t - \sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}} \sin \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}} \right) \right)}{(C_{Bot} + C_{Top})T_{Fall}} \quad (A.53)$$

$$V_{CTop,SM,P1}(t) = \left(2C_{Bot}C_{Top}I_{in}L_{Par} - (C_{Bot} + C_{Top})I_{in}t^2 + 2(C_{Bot} + C_{Top})^2T_{Fall}V_{out} - 2C_{Bot}C_{Top}I_{in}L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}} \right) \right) / 2(C_{Bot} + C_{Top})^2T_{Fall} \quad (A.54)$$

$$V_{CBot,SM,P1}(t) = \frac{I_{in}(2C_{Top}^2L_{Par} + C_{Bot}t^2 + C_{Top}t^2 - 2C_{Top}^2L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}} \right))}{2(C_{Bot} + C_{Top})^2T_{Fall}} \quad (A.55)$$

A.2.2 Slow-Mode – Period 2 circuit analysis

The applicable circuit for the time period $T_{Clamp} < t < T_{Fall}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{CTop,SM,P2}(t) + I_{CBot,SM,P2}(t) + I_{Switch}(t) \quad (A.56)$$

$$I_{in} = -C_{Top} \frac{dV_{CTop,SM,P2}(t)}{dt} + C_{Bot} \frac{dV_{CBot,SM,P2}(t)}{dt} + I_{in} - \frac{I_{in}}{T_{Fall}}(t - T_{Clamp}) \quad (A.57)$$

The Laplace transform of this equation can be written as:

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top} (sV_{CTop,SM,P2}(s) - V_{CTop,SM,P2}(0)) + C_{Bot} (sV_{CBot,SM,P2}(s) - V_{CBot,SM,P2}(0)) \\ & + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} - \frac{I_{in} T_{Clamp}}{s T_{Fall}} \end{aligned} \quad (A.58)$$

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top} (sV_{CTop,SM,P2}(s) - V_{CTop,FM,P1}(T_{Clamp})) + C_{Bot} (sV_{CBot,SM,P2}(s) - V_{CBot,FM,P1}(T_{Clamp})) \\ & + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{Fall}} - \frac{I_{in} T_{Clamp}}{s T_{Fall}} \end{aligned} \quad (A.59)$$

Kirchhoff's Voltage Law

$$V_{out} = V_{CBot,SM,P2}(t) + V_{CTop,SM,P2}(t) - V_{LPar,SM,P2}(t) \quad (A.60)$$

Thus:

$$V_{out} = V_{CBot,SM,P2}(t) + V_{CTop,SM,P2}(t) - L \frac{dI_{LPar,SM,P2}(t)}{dt} \quad (A.61)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CBot,SM,P2}(s) + C_{Top,SM,P2}(s) - L (sI_{LPar,SM,P2}(s) - I_{LPar,SM,P2}(0)) \quad (A.62)$$

$$\frac{V_{out}}{s} = V_{CBot,SM,P2}(s) + C_{Top,SM,P2}(s) - L (sI_{LPar,SM,P2}(s) - I_{LPar,SM,P1}(T_{Clamp})) \quad (A.63)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$\begin{aligned}
I_{LPar,SM,P2}(t) = & -\frac{1}{2T_{Fall}}(-2I_{in}t + \frac{1}{(C_{Bot} + C_{Top})^2 L_{Par}}(2I_{in}L_{Par} \cos\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot}L_{Par}}}\right) \\
& (C_{Bot}(C_{Bot} + C_{Top})T_{Clamp} + C_{Top}\sqrt{C_{Bot}C_{Top}(C_{Bot} + C_{Top})L_{Par}} \\
& \sin\left(\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}}\right) + \sqrt{C_{Bot}L_{Par}}(2C_{Bot}(C_{Bot} + 2C_{Top})I_{in}L_{Par} \\
& - (C_{Bot} + C_{Top})I_{in}T_{Clamp}^2 + 2(C_{Bot} + C_{Top})^2 T_{Fall}V_{out} + 2C_{Top}^2 I_{in}L_{Par} \\
& \cos\left(\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}}\right) \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot}L_{Par}}}\right)) \quad (A.64)
\end{aligned}$$

$$\begin{aligned}
V_{C_{Bot},SM,P2}(t) = & \frac{1}{2(C_{Bot} + C_{Top})^2 T_{Fall}}(- (2C_{Bot}(C_{Bot} + C_{Top})I_{in}L_{Par}) - (C_{Bot} + C_{Top})I_{in}T_{Clamp}^2 \\
& + 2(C_{Bot} + C_{Top})^2 T_{Fall}V_{out} + 2C_{Top}^2 I_{in}L_{Par} \cos\left(\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}}\right) \\
& \cos\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot}L_{Par}}}\right) + 2((C_{Bot} + C_{Top})^2 (I_{in}L_{Par} + T_{Fall}V_{out}) \\
& + I_{in}((C_{Bot} + C_{Top})\sqrt{C_{Bot}L_{Par}}T_{Clamp}) + C_{Top}^{3/2}\sqrt{C_{Bot} + C_{Top}}L_{Par} \\
& \sin\left(\frac{T_{Clamp}}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot}+C_{Top}}}}\right) \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot}L_{Par}}}\right)) \quad (A.65)
\end{aligned}$$

A.2.3 Slow-Mode – Period 3 circuit analysis

The applicable circuit for the time period $T_{Clamp} < t < \infty$ can be seen in Fig. A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Oscillation Node

$$I_{in} = I_{C_{Top},SM,P3}(t) + I_{C_{Bot},SM,P3}(t) \quad (A.66)$$

$$I_{ph} = -C_{Top} \frac{dV_{CTop,SM,P3}(t)}{dt} + C_{Bot} \frac{dV_{CBot,SM,P3}(t)}{dt} \quad (A.67)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top}(sV_{CTop,SM,P3}(s) - V_{CTop,SM,P3}(0)) + C_{Bot}(sV_{CBot,SM,P3}(s) - V_{CBot,SM,P3}(0)) \quad (A.68)$$

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top}(sV_{CTop,SM,P3}(s) - V_{CTop,SM,P2}(T_{Clamp} - T_{Fall})) \\ & + C_{Bot}(sV_{CBot,SM,P3}(s) - V_{CBot,SM,P2}(T_{Clamp} - T_{Fall})) \end{aligned} \quad (A.69)$$

Kirchhoff's Voltage Law

$$V_{out} = V_{CBot,SM,P3}(t) - V_{LPar,SM,P3}(t) \quad (A.70)$$

Thus:

$$V_{out} = V_{CBot,SM,P3}(t) - L \frac{dI_{LPar,SM,P3}(t)}{dt} \quad (A.71)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CBot,SM,P3}(s) - L(sI_{LPar,SM,P3}(s) - I_{LPar,SM,P3}(0)) \quad (A.72)$$

$$\frac{V_{out}}{s} = V_{CBot,SM,P3}(s) - L(sI_{LPar,SM,P3}(s) - I_{LPar,SM,P2}(T_{Clamp} - T_{Fall})) \quad (A.73)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$\begin{aligned}
I_{LPar,SM,P3}(t) = & (2(C_{Bot} + C_{Top})^2 I_{in} \sqrt{L_{Par}} T_{Fall} - C_{Bot}(C_{Bot} + C_{Top}) I_{in} \sqrt{L_{Par}} T_{Clamp} \\
& \cos\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}}\right) + \sqrt{C_{Bot}}(C_{Top}^{\frac{3}{2}} \sqrt{C_{Bot} + C_{Top}} I_{in} L_{Par} \\
& \sin\left(\frac{-\sqrt{C_{Bot} + C_{Top}} T_{Clamp} + \sqrt{C_{Top}}(T_{Clamp} - t)}{\sqrt{C_{Bot} C_{Top} L_{Par}}}\right) - C_{Top}^{\frac{3}{2}} \sqrt{C_{Bot} + C_{Top}} I_{in} L_{Par} \\
& \sin\left(\frac{\sqrt{C_{Bot} + C_{Top}} T_{Clamp} + \sqrt{C_{Top}}(T_{Clamp} - t)}{\sqrt{C_{Bot} C_{Top} L_{Par}}}\right) + 2C_{Bot}(C_{Bot} + 2C_{Top}) I_{in} L_{Par} \\
& - (C_{Bot} + C_{Top}) I_{in} T_{Clamp}^2 + 2(C_{Bot} + C_{Top})^2 T_{Fall} V_{out} \sin\left(\frac{T_{Clamp} - t}{\sqrt{C_{Bot} L_{Par}}}\right) \\
& - 2(C_{Bot} + C_{Top})^2 I_{in} L_{Par} \sin\left(\frac{T_{Fall} - t}{\sqrt{C_{Bot} L_{Par}}}\right) - 2\sqrt{C_{Bot}} C_{Top}^2 I_{in} L_{Par} \\
& \cos\left(\frac{T_{Clamp}}{\sqrt{C_{Bot} C_{Top} L_{Par}}}\right) \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}}\right) / \left(2(C_{Bot} + C_{Top})^2 \sqrt{L_{Par}} T_{Fall}\right) \quad (A.74)
\end{aligned}$$

$$\begin{aligned}
V_{CBot,SM,P3}(t) = & \frac{1}{2(C_{Bot} + C_{Top})^2 T_{Fall}} (2(C_{Bot} + C_{Top})^2 T_{Fall} V_{out} - C_{Top}^2 I_{in} L_{Par} \\
& \cos\left(\frac{-\sqrt{C_{Bot} + C_{Top}} T_{Clamp} + \sqrt{C_{Top}}(T_{Clamp} - t)}{\sqrt{C_{Bot} C_{Top} L_{Par}}}\right) - C_{Top}^2 I_{in} L_{Par} \\
& \cos\left(\frac{\sqrt{C_{Bot} + C_{Top}} T_{Clamp} + \sqrt{C_{Top}}(T_{Clamp} - t)}{\sqrt{C_{Bot} C_{Top} L_{Par}}}\right) + (-2C_{Bot}(C_{Bot} + 2C_{Top}) I_{in} L_{Par} \\
& + (C_{Switch} + C_{Diode}) I_{in} T_{clamp}^2 - 2(C_{Switch} + C_{Diode})^2 T_{Fall} V_{out}) \cos\left(\frac{-T_{clamp} + t}{\sqrt{C_{Switch} L_{par}}}\right) \\
& + 2(C_{Bot} + C_{Top})^2 I_{in} L_{Par} \cos\left(\frac{-T_{Fall} + t}{\sqrt{C_{Bot} L_{Par}}}\right) + 2C_{Bot} I_{in} \sqrt{C_{Bot} L_{Par}} T_{Clamp} \\
& \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}}\right) + 2C_{Top} I_{in} \sqrt{C_{Bot} L_{Par}} T_{Clamp} \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}}\right) + 2C_{Top}^{3/2} \\
& \sqrt{C_{Bot} + C_{Top}} I_{in} L_{Par} \sin\left(\frac{T_{Clamp}}{\sqrt{C_{Bot} C_{Top} L_{Par}}} \sin\left(\frac{-T_{Clamp} + t}{\sqrt{C_{Bot} L_{Par}}}\right)\right) \quad (A.75)
\end{aligned}$$

Appendix B

Mathematical Derivation of Circuit Model with Double Segment

The turn-off switch current $I_{Switch}(t)$ is modelled as a linear decaying current source but with two adjustable segments instead of one. The corresponding period is then also broken up into P1A and P1B to represent the different current functions. This representation of the current is a very important part of being able to describe the system as a whole mathematically. This example can be seen in Fig. B.1 below:

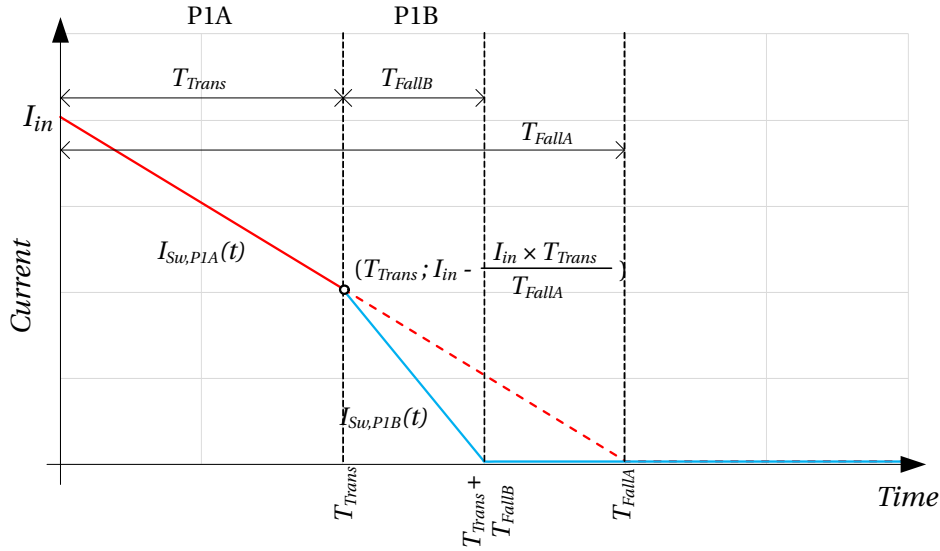


Fig. B.1 Adjustable Current turn-off waveform through the switch

The functions for the segments are:

$$I_{Sw,P1A}(t) = I_{In} - \frac{I_{In}}{T_{FallA}(t)} \quad (B.1)$$

The function for the second segment can be derived by substituting two known points into the line equation and solving the unknowns. The following equation is then derived and will always be applicable to describe to second part of the current turn-off:

$$I_{Sw,P1B}(t) = \frac{I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans})}{T_{FallA}}(t - T_{Trans}) + I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans}) \quad (B.2)$$

In these equations, T_{FallA} is the time taken from $t = 0$ to where $I_{Sw,P1A}(t)$ would have crossed the x-axis, T_{Trans} is the time taken from $t = 0$ to where the switching current transitions from $I_{Sw,P1A}(t)$ to $I_{Sw,P1B}(t)$ and T_{FallB} is the time taken from $t = T_{Trans}$ to $t = T_{FallB}$. The only constraint is that $T_{Trans} < T_{FallA}$. These values individually are arbitrary, but collectively, they are very important to the system. This representation can approximate almost all turn-off characteristics. The use of linear equations also keeps the eventual math as simple as possible without introducing higher-order events to the equations.

This circuit with adjustable current turn-off can be modelled by applying classical circuit theory, where the equivalent circuit of each period is analysed independently by applying Kirchhoff's Current Law and Kirchhoff's Voltage Law to solve the circuit variables of the Fast-turn-off equivalent circuits in *Fast-Mode* circuit progressions of Fig. A.2.

The functions of $I_{LPar}(t)$, $V_{CBot}(t)$ and $V_{CTop}(t)$ can then be solved from P1A to P3 by performing the Laplace transforms on the differential equations of a given period, solving the functions, and performing the inverse Laplace transform to convert the functions back to the time domain, exactly like completed in Chapter 4. The equations are made particularly complicated by the inclusion of the initial conditions of the previous time period and keeping the equations in a representation form. The corresponding time domain equations for each period can be found in this section and are only completed for *Fast-Mode*

The circuit can then be modelled in three associated time periods:

- *Fast-Mode* P1A is applicable for $0 < t < T_{Trans}$.
- *Fast-Mode* P1B is applicable for $T_{Trans} < t < T_{Trans} + T_{FallB}$.
- *Fast-Mode* P2 is applicable for $T_{Trans} + T_{FallB} < t < T_{Clamp}$.

B.1 Model Equation Derivations

To determine the time-domain equations of the variables for each time period, the following classical approach is used:

- Step 1: Convert each differential equation to its corresponding Laplace Transform.

- Step 2: Solve the Laplace transform mathematically.
- Step 3: Find the inverse Laplace Transform to get the time-domain solution.

The results from each period are used as the initial values for the next period. Due to this, the math becomes quite complex, even though assumptions such as linear transistor current and no damping resistance are used.

To minimise errors in the model, software packages such as Java and Mathematica are used to solve the differential equations and compute the inverse Laplace transforms. These results are later verified through simulation and will be discussed in the following sections.

Special attention was given to keeping the model in mathematical form to extract as much information as possible.

Since the resulting equations for $V_{CTop}(t)$, $V_{CBot}(t)$, and $I_{LPAr}(t)$ will differ for each time period, these variables will have a subscript referring to the specific mode and time period.

B.1.1 Double Segment – Period 1A circuit analysis

The applicable circuit for the time period $0 < t < T_{Trans}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Switching Node

$$I_{in} = I_{CTop,P1A}(t) + I_{CTop,P1A}(t) + I_{SW,P1A}(t) \quad (B.3)$$

Where $I_{SW,P1A} = I_{in} - \frac{I_{in}}{T_{FallA}}(t)$ for linear decay of the transistor current. Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,P1A}(t)}{dt} + C_{Bot} \frac{dV_{CBot,P1A}(t)}{dt} + I_{in} - \frac{I_{in}}{T_{FallA}}(t) \quad (B.4)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,P1A}(s) - V_{CTop,P1A}(0)) + C_{Bot} (sV_{CBot,P1A}(s) - V_{CBot,P1A}(0)) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{FallA}} \quad (B.5)$$

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,P1A}(s) - V_{out}) + C_{Bot} (sV_{CBot,P1A}(s) - 0) + \frac{I_{in}}{s} - \frac{I_{in}}{s^2 T_{FallA}} \quad (B.6)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar}(t) = I_{CTop,P1A}(t) \quad (B.7)$$

Thus:

$$I_{LPar}(t) = -C_{Top} \frac{dV_{CTop,P1A}(t)}{dt} \quad (B.8)$$

The Laplace transform of this equation can be written as:

$$I_{LPar}(t) = -C_{Top} (sV_{CTop,P1A}(s) - V_{CTop,P1A}(0)) \quad (B.9)$$

$$I_{LPar}(t) = -C_{Top} (sV_{CTop,P1A}(s) - V_{out}) \quad (B.10)$$

The initial condition for this time period is simply the initial conditions as seen in the original circuit.

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,P1A}(t) + V_{CBot,P1A}(t) - V_{L,P1A}(t) \quad (B.11)$$

Thus:

$$V_{out} = V_{CTop,P1A}(t) + V_{CBot,P1A}(t) - L \frac{dI_{LPar,P1A}(t)}{dt} \quad (B.12)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,P1A}(s) + V_{CBot,P1A}(s) - L (sI_{LPar,P1A}(s) - I_{LPar,P1A}(0)) \quad (B.13)$$

$$\frac{V_{out}}{s} = V_{CTop,P1A}(s) + V_{CBot,P1A}(s) - L (sI_{LPar,P1A}(s) - 0) \quad (B.14)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$I_{Lpar,P1A}(t) = \frac{C_{Top} I_{in} \left(t - \sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}} \sin \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \right)}{(C_{Bot} + C_{Top}) T_{FallA}} \quad (B.15)$$

$$V_{Top,P1A}(t) = (2C_{Bot} C_{Top} I_{in} L_{Par} - (C_{Bot} + C_{Top}) I_{in} t^2 + 2(C_{Bot} + C_{Top})^2 T_{FallA} V_{out} - 2C_{Bot} C_{Top} I_{in} L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right)) / 2(C_{Bot} + C_{Top})^2 T_{FallA} \quad (B.16)$$

$$V_{Bot,P1A}(t) = \frac{I_{in} (2C_{Top}^2 L_{Par} + C_{Bot} t^2 + C_{Top} t^2 - 2C_{Top}^2 L_{Par} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right))}{2(C_{Bot} + C_{Top})^2 T_{FallA}} \quad (B.17)$$

B.1.2 Double Segment – Period 1B circuit analysis

The applicable circuit for the time period $T_{Trans} < t < T_{Trans} + T_{FallB}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

Kirchhoff's Current Law at Switching Node

$$I_{in} = I_{CTop,P1B}(t) + I_{CBot,P1B}(t) + I_{SW,P1B}(t) \quad (B.18)$$

Where:

$$I_{SW,P1B}(t) = \frac{I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans})}{T_{FallA}}(t - T_{Trans}) + I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans}) \quad (B.19)$$

for the second segment of the switch turn-off the current. Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,P1B}(t)}{dt} + C_{Bot} \frac{dV_{CBot,P1B}(t)}{dt} + \frac{I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans})}{T_{FallA}}(t - T_{Trans}) + I_{In} - \frac{I_{In}}{T_{FallA}}(T_{Trans}) \quad (B.20)$$

The Laplace transform of this equation can be written as:

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top} (sV_{CTop,P1B}(s) - V_{CTop,P1B}(0)) + C_{Bot} (sV_{CBot,P1B}(s) - V_{CBot,P1B}(0)) \\ & + \frac{I_{in}}{T_{FallA}} \cdot \frac{e^{-sT_{Trans}}}{s^2} + \frac{I_{in}}{s} - \frac{I_{in}T_{Trans}}{T_{FallA}s} \end{aligned} \quad (B.21)$$

$$\begin{aligned} \frac{I_{in}}{s} = & -C_{Top} (sV_{CTop,P1B}(s) - V_{CTop,P1A}(T_{Trans})) + C_{Bot} (sV_{CBot,P1B}(s) - V_{CBot,P1A}(T_{Trans})) \\ & + \frac{I_{in}}{T_{FallA}} \cdot \frac{e^{-sT_{Trans}}}{s^2} + \frac{I_{in}}{s} - \frac{I_{in}T_{Trans}}{T_{FallA}s} \end{aligned} \quad (B.22)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar,P1B}(t) = I_{CTop,P1B}(t) \quad (B.23)$$

Thus:

$$I_{LPar,P1B}(t) = -C_{Top} \frac{dV_{CTop,P1B}(t)}{dt} \quad (B.24)$$

The Laplace transform of this equation can be written as:

$$I_{LPar,P1B}(t) = -C_{Top} (sV_{CTop,P1B}(s) - V_{CTop,P1B}(0)) \quad (B.25)$$

$$I_{LPar,P1B}(t) = -C_{Top} (sV_{CTop,P1B}(s) - V_{CTop,P1B}(T_{Trans})) \quad (B.26)$$

The initial condition for this time period is simply the initial conditions as seen in the original circuit.

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,P1B}(t) + V_{CBot,P1B}(t) - V_{L,P1B}(t) \quad (B.27)$$

Thus:

$$V_{out} = V_{CTop,P1B}(t) + V_{CBot,P1B}(t) - L \frac{dI_{LPar,P1B}(t)}{dt} \quad (B.28)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,P1B}(s) + V_{CBot,P1B}(s) - L(sI_{LPar,P1B}(s) - I_{LPar,P1B}(0)) \quad (B.29)$$

$$\frac{V_{out}}{s} = V_{CTop,P1B}(s) + V_{CBot,P1B}(s) - L(sI_{LPar,P1B}(s) - I_{LPar,P1B}(T_{Trans})) \quad (B.30)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$I_{LPar,P1B}(t) = \frac{(C_{Top}I_{in}(T_{FallB}T_{Trans} + (T_{FallA} - T_{Trans})(-T_{Trans} + t) + \sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}})}{(C_{Bot} + C_{Top})T_{FallA}T_{FallB}} \left(-T_{FallB} \sin\left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}}\right) + (-T_{FallA} + T_{FallB} + T_{Trans}) \sin\left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}}\right) \right) \quad (B.31)$$

$$V_{Top,P1B}(t) = \frac{(I_{in}(2C_{Bot}C_{Top}L_{Par}T_{FallA} - 2C_{Bot}C_{Top}L_{Par}T_{Trans} - C_{Bot}T_{FallB}T_{Trans}^2 - C_{Top}T_{FallB}T_{Trans}^2 - 2(C_{Bot} + C_{Top})T_{FallB}T_{Trans}(-T_{Trans} + t) - (C_{Bot} + C_{Top})(T_{FallA} - T_{Trans})(-T_{Trans} + t)^2) + 2(C_{Bot} + C_{Top})^2T_{FallA}T_{FallB}V_{out} + 2C_{Bot}C_{Top}I_{in}L_{Par}(-T_{FallB} \cos\left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}}\right) + (-T_{FallA} + T_{FallB} + T_{Trans}) \cos\left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}}\right)))/2(C_{Bot} + C_{Top})^2T_{FallA}T_{FallB}} \quad (B.32)$$

$$\begin{aligned}
V_{Bot,P1B}(t) = & (I_{in}(2C_{Top}^2 L_{Par} T_{FallA} - 2C_{Top}^2 L_{Par} T_{Trans} + C_{Bot} T_{FallB} T_{Trans}^2 + C_{Top} T_{FallB} T_{Trans}^2 \\
& + 2(C_{Bot} + C_{Top}) T_{FallB} T_{Trans} (-T_{Trans} + t) + (C_{Bot} + C_{Top}) (T_{FallA} - T_{Trans}) \\
& (-T_{Trans} + t)^2 + 2C_{Top}^2 L_{Par} (-T_{FallB} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& + (-T_{FallA} + T_{FallB} + T_{Trans}) \cos \left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right))) / 2(C_{Bot} + C_{Top})^2 T_{FallA} T_{FallB} \quad (B.33)
\end{aligned}$$

B.1.3 Double Segment – Period 2 circuit analysis

The applicable circuit for the time period $T_{Trans} + T_{FallB} < t < T_{Clamp} + T_{FallB}$ can be seen in Fig A.2. From his diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found.

As stated above, in this time period, it is important to remember that the initial conditions for this time period are the final conditions for the previous time period. From this diagram, applying Kirchhoff's voltage law and current law, the following Differential equations can be found:

Kirchhoff's Current Law at Switching Node

$$I_{in} = I_{CTop,P2}(t) + I_{CBot,P2}(t) \quad (B.34)$$

Thus:

$$I_{in} = -C_{Top} \frac{dV_{CTop,P2}(t)}{dt} + C_{Bot} \frac{dV_{CBot,P2}(t)}{dt} \quad (B.35)$$

The Laplace transform of this equation can be written as:

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,P2}(s) - V_{CTop,P2}(0)) + C_{Bot} (sV_{CBot,P2}(s) - V_{CBot,P2}(0)) \quad (B.36)$$

$$\frac{I_{in}}{s} = -C_{Top} (sV_{CTop,P2}(s) - V_{CTop,P1B}(T_{FallB})) + C_{Bot} (sV_{CBot,P2}(s) - V_{CBot,P1B}(T_{FallB})) \quad (B.37)$$

Kirchhoff's Current Law at Parasitic Inductor

$$I_{LPar,P2}(t) = I_{CTop,P2}(t) \quad (B.38)$$

Thus:

$$I_{LPar,P2}(t) = -C_{Top} \frac{dV_{CTop,P2}(t)}{dt} \quad (B.39)$$

The Laplace transform of this equation can be written as:

$$I_{LPar,P2}(t) = -C_{Top} (sV_{CTop,P2}(s) - V_{CTop,P2}(0)) \quad (B.40)$$

$$I_{LPar,P2}(t) = -C_{Top} (sV_{CTop,P2}(s) - V_{CTop,P1B}(T_{FallB})) \quad (B.41)$$

Kirchhoff's Voltage Law

$$V_{out} = V_{CTop,P2}(t) + V_{CBot,P2}(t) - V_{L,P2}(t) \quad (B.42)$$

Thus:

$$V_{out} = V_{CTop,P2}(t) + V_{CBot,P2}(t) - L \frac{dI_{LPar,P2}(t)}{dt} \quad (B.43)$$

The Laplace transform of this equation can be written as:

$$\frac{V_{out}}{s} = V_{CTop,P2}(s) + V_{CBot,P2}(s) - L (sI_{LPar,P2}(s) - I_{LPar,P2}(0)) \quad (B.44)$$

$$\frac{V_{out}}{s} = V_{CTop,P2}(s) + V_{CBot,P2}(s) - L (sI_{LPar,P2}(s) - I_{LPar,P1B}(T_{FallB})) \quad (B.45)$$

Resulting Time-Domain Equations

When the Laplace transforms derived above are solved, the corresponding Inverse Laplace Transforms, so the solved time-domain equations can be seen below:

$$\begin{aligned}
V_{CTop, P2}(t) = & -((C_{Bot} + C_{Top})T_{FallB}(I_{in}T_{Trans}(T_{FallB} + T_{Trans}) + I_{in}T_{FallA}(T_{FallB} + 2(-T_{FallB} \\
& - T_{Trans} + t)) - 2(C_{Bot} + C_{Top})T_{FallA}V_{out}) + 2C_{Bot}C_{Top}I_{in}L_{Par} \\
& (T_{FallB} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right) + (T_{FallA} - T_{FallB} - T_{Trans}) \cos \left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& + (-T_{FallA} + T_{Trans}) \cos \left(\frac{-T_{FallB} - T_{Trans} + t}{\sqrt{\frac{C_{Bot}C_{Top}L_{Par}}{C_{Bot} + C_{Top}}}} \right)) / 2(C_{Bot} + C_{Top})^2 T_{FallA} T_{FallB} \quad (B.47)
\end{aligned}$$

$$\begin{aligned}
V_{CBot,P2}(t) = & (I_{In}((C_{Bot} + C_{Top}) T_{FallB} (T_{Trans} (T_{FallB} + T_{Trans}) + T_{FallA} (T_{FallB} + 2(-T_{FallB} - T_{Trans} + t))) \\
& + 2C_{Top}^2 L_{Par} (-T_{FallB} \cos \left(\frac{t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& + (-T_{FallA} + T_{FallB} + T_{Trans}) \cos \left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& + (T_{FallA} - T_{Trans} + T_{FallB} - T_{Trans}) \cos \left(\frac{-T_{Trans} + t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right) \\
& (T_{FallA} - T_{Trans}) \cos \left(\frac{-T_{FallB} - T_{Trans} + t}{\sqrt{\frac{C_{Bot} C_{Top} L_{Par}}{C_{Bot} + C_{Top}}}} \right))) / 2 (C_{Bot} + C_{Top})^2 T_{FallA} T_{FallB} \quad (B.48)
\end{aligned}$$