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# Implementation of the Stopless removal software for the level-1 tile-muon trigger system of the LHC atlas tilecal

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# Implementation of the Stopless removal software for the Level-1 Tile-Muon Trigger system of the LHC ATLAS TileCal

by

**Sijiye Humphry Tlou**

*A Dissertation submitted to the Faculty of Science, University of the Witwatersrand in fulfillment of the requirements for the degree of: Master of Science in Physics*

**Supervised by**
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School of Physics

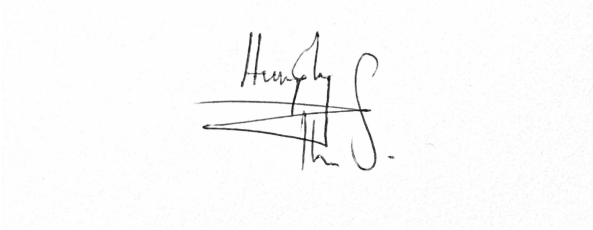
**2019**

# Declaration

I declare that this Dissertation is a result of my own work, except where explicit reference is made to the work of others. It is being submitted for the Degree of Master of Science at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any qualification or examination at any other University.

Related research output:

- H. Tlou. The Level-1 Tile-Muon trigger system in the ATLAS detector of the Large Hadron Collider. To appear in the book of proceedings of HEPP2018, High Energy Particle Physics, February 2018; Stellenbosch, South Africa [1]



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Sijiye Humphry Tlou, **$20^{th}$ of May 2019 in Johannesburg.**

# Abstract

The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider. The TileCal is essential for providing highly-segmented energy measurements for incident particles. The Tile-Muon trigger system is used for the detection of interesting muon events using the outermost radial layers (D5 and D6 cells) of the TileCal system in coincidence with the ATLAS muon chambers. The main source of the Level-1 Muon-Trigger background in the end-cap region is low momentum protons scattering off magnets and shielding in the forward region. They produce correlated hits leading to coincidences in the trigger muon chambers up to the highest transverse momentum muon threshold. Requiring a coincidence with some other detectors lying inside the toroid magnets and shielding lowers the fake event trigger rate. The Tile Muon Digitizer Board (TMDB) was designed and is responsible for digitizing the analogue muon trigger output from the D5 and D6 cells. Hardware or firmware failures of the TMDB can lead to a permanent busy assertion. The Tile-Muon trigger system requires functionalities that will aid in detecting changes in the conditions of an asserted permanent busy. This dissertation presents the hardware and the implementation of the stopless removal software for the Level-1 Tile-Muon Trigger system of the TileCal.

# Acknowledgements

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# Nomenclature

| | |
|---|---|
| **ACR** | ATLAS Control Room |
| **ADC** | Analog to Digital Converter |
| **AFS** | Andrew File System |
| **ALEPH** | Apparatus for LEP PHysics |
| **ALICE** | A Large Ion Collider Experiment |
| **AM** | Access Management |
| **API** | Application Programming Interface |
| **ATLAS** | A Toroidal LHC ApparatuS |
| **B175** | Building 175 laboratory in Meyrin site, CERN |
| **BE** | Back-End |
| **BC** | Bunch-Crossing |
| **BCId** | Bunch-Crossing Identifiier |
| **BW** | Big Wheel |
| **CAEN** | Construzioni Apparecchiature Elletroniche Nucleari S.p.A |
| **CCC** | CERN Control Centre |
| **CERN** | European Organization for Nuclear Research |
| **CIS** | Charge Injection Scan |
| **CMS** | Compact Muon Solenoid |
| **CMT** | Configuration Management Tool |
| **COOL** | ATLAS-wide conditions database, also: CLIPS Object Oriented Language |
| **CRC** | Cyclic Redundancy Check |
| **CTP** | Central Trigger Processor (L1 trigger) |
| **DAL** | Data Access Library |
| **DAQ** | Data AcQuisition system |
| **DB** | DataBase |
| **DCS** | Detector Control System |
| **DELPHI** | DEtector with Lepton, Photon and Hadron Identification |
| **DMU** | Data Management Unit |
| **DQM** | Data Quality Monitoring |
| **DSP** | Digital Signal Processor |
| **DVS** | Diagnostic and Verification System |

| | |
|---|---|
| **EB** | Extended Barrel |
| **EBA** | Extended Barrel A-side |
| **EBC** | Extended Barrel C-side |
| **ERS** | Error Reporting Service |
| **EF** | Event Filter |
| **EIL4** | End-cap Inner Large 4 |
| **EM** | ElectroMagnetic |
| **ECal** | EM Calorimeter |
| **FCal** | Forward Calorimeter |
| **FE** | Front-End |
| **FIFO** | First-In First-Out memory or strategy |
| **FPGA** | Field-Programmable Gate Array |
| **FSM** | Finite State Machine |
| **GeV** | Giga electron Volt |
| **G-LINK** | Gigabit LINK |
| **GUI** | Graphical User Interface |
| **HCal** | Hadronic Calorimeter |
| **HEC** | Hadronic End-cap Calorimeter |
| **HL-HLC** | High Luminosity LHC |
| **HLT** | High Level Trigger |
| **HOLA** | High speed Optical Link for ATLAS |
| **HVPS** | High Voltage Power Supply |
| **IBL** | Insertable B-Layer |
| **ID** | Inner Detector |
| **IGUI** | Integrated Graphical User Interface |
| **IP** | Internet Protocol |
| **IPC** | Inter-Process Communication |
| **IPMI** | Intelligent Platform Management Interface |
| **I/O** | Input/Output |
| **IS** | Information Service |
| **LAr** | Liquid Argon |
| **L1A** | L1 Accept |
| **L1Calo** | LVL1 Calorimeter Trigger |
| **LEP** | Large Electron-Positron |
| **LHCb** | Large Hadron Collider beauty |
| **LINAC2** | Linear accelerator 2 |
| **LB** | Long Barrel |
| **LBA** | Long Barrel A-side |
| **LBC** | Long Barrel C-side |
| **LCG** | LHC Computing Grid |
| **LHC** | Large Hadron Collider |

| | |
|---|---|
| **LHCf** | Large Hadron Collider forward |
| **LS1** | Long Shutdown 1 |
| **LS2** | Long Shutdown 2 |
| **LS3** | Long Shutdown 3 |
| **LTP** | Local Trigger Processor |
| **LTPi** | Local Trigger Processor interface |
| **LVDS** | Low Voltage Differential Signal |
| **LVL1** | First level trigger |
| **LVL2** | Second level trigger |
| **LVPS** | Low Voltage Power Supply |
| **MDT** | Monitored Drift Tubes |
| **MeV** | Mega electron Volt |
| **MF** | Matched Filter |
| **MoEDAL** | Monopole and Exotics Detector At the LHC |
| **MPU** | Module Processing Unit |
| **MUCTPI** | L1_MUon to Central Trigger Processor Interface |
| **NSW** | New Small Wheel |
| **OKS** | Object Kernel Support |
| **OPAL** | Omni-Purpose Apparatus for LEP |
| **PMG** | Process ManaGer |
| **PMT** | PhotoMultiplier Tube |
| **PS** | Proton Synchrotron |
| **PSB** | Proton Synchrotron Booster |
| **PU** | Processor Unit |
| **QCD** | Quantum ChromoDynamics |
| **ROB** | Read Out Buffer |
| **ROD** | Read Out Driver |
| **RoI** | Region of Interest |
| **ROL** | Read Out Link |
| **ROS** | Read Out System |
| **RC** | Run Control |
| **RCD** | ROD Crate DAQ |
| **SBC** | Single Board Computer |
| **SCT** | SemiConductor Tracker |
| **SFP** | Small Form-factor Pluggable |
| **SLC** | Scientific Linux CERN |
| **S-L** | Sector-Logic |
| **S-LINK** | Simple LINK |
| **SM** | Standard Model |
| **SNR** | Signal-to-Noise Ratio |
| **SPS** | Super Proton Synchrotron |

| | |
|---|---|
| **SVN** | SubVersioN revision control system |
| **TBM** | Trigger and Busy Module |
| **TDAQ** | Trigger and Data AcQuisition |
| **TCP** | Transmission Communication Protocol |
| **TeV** | Tera electron Volt |
| **TGC** | Thin Gap Chamber |
| **TileCal** | Tile Calorimeter |
| **TM** | Transition Module |
| **TMDB** | Tile Muon Digitizer Board |
| **TOTEM** | TOTal Elastic and diffractive cross section Measurement |
| **TRT** | Transition Radiation Tracker |
| **TTC** | Timing, Trigger, and Control |
| **TTCDec** | TTC Decoder |
| **TTCoc** | Timing, Trigger, and Control optical coupler |
| **TTCpr** | TTC receiver in PMC Form Factor |
| **TTCex** | Trigger, Timing, and Control laser transmitter |
| **TTCRx** | Trigger, Timing, and Control Receiver ASIC |
| **TTCvi** | Timing, Trigger, and Control VME interface module |
| **TTL** | Transistor-Transistor Logic |
| **TType** | Trigger Type |
| **VME** | Versa Module Eurocard |
| **XOFF** | Message or signal indicating that data transmission has to be halted |
| **UA1** | Underground Area 1 |
| **UA2** | Underground Area 2 |
| **UN** | United Nations |
| **UNESCO** | United Nations Educational, Scientific and Cultural Organization |
| **USA15** | Underground counting room |
| **WLS** | WaveLength Shifting |
| **XML** | Extensible Markup Language |

# Chapter 1

# Introduction

Modern high energy physics experiments are dependent on innovative tools, simulation, computation and technological advancements of other research fields. The particle accelerators utilize the sophisticated computing techniques and technological tools in the collection, organization and distribution of data. The World Wide Web was invented at CERN, a European organization for nuclear research, which will be discussed in Chapter 2. The World Wide Web was invented to address the needs of particle physics collaborations and was further extended to the general public.

The Large Hadron Collider (LHC) is a complex experimental facility, built by CERN and consists of several experiments, designed to investigate the fundamental structure of the universe. The ATLAS (A Toroidal LHC ApparatuS) experiment is the largest of the four major experiments at the LHC at CERN, Geneva, Switzerland. It is a general purpose detector with a specific design for the precision Standard Model (SM) measurements and to conduct physics research beyond the SM. The Tile Calorimeter (TileCal) is one of the ATLAS experiment sub-detectors, it is the Hadronic calorimeter that covers the most central region of the ATLAS experiment. The TileCal is mechanically divided into three cylinders along the beam direction. Each cylinder is segmented azimuthally into 64 modules. The TileCal is based on a sampling technique where plastic scintillating tiles are embedded in steel absorber plates. Each tile is read-out on both sides by wavelength shifting fibers. Groups of tiles are bundled together into cells, each of them is read-out by two photo-multiplier tubes (PMTs). The PMTs and the Front-End electronics are located in the super-drawers in the outermost part of the modules.

The TileCal Online System is a set of Trigger and Data Acquisition (TDAQ) System, and its main purpose is to readout, transport and store physics data originating from collisions at the LHC. The TDAQ software is built up of CMake packages, which are stored in Gitlab. The TileCal online software is an extension

of the ATLAS TDAQ software, which provides TileCal detector specific software. The detector specific software is for the Back-End electronics, infrastructure for calibration systems, monitoring (including hardware), and the diagnostic and verification systems tests. One of the core components of the TileCal Online Software elements is the Back-End electronics ROD Crate DAQ. It is supported by the ATLAS Data Flow policy for which the TileCal online software provides plug-ins. This keeps the programming efforts focused on specific hardware handling since the core software is centrally managed.

The Tile-Muon trigger system is part of the Level-1 trigger system and it is used for the detection of interesting muon events using the outermost radial layers (D5 and D6 cells) of the TileCal system. The Tile Muon Digitizer Board (TMDB) is a Read Out Driver (ROD) that receives, digitizes and transfers signals to the Read Out System (ROS). The TMDB provides a busy signal to regulate the trigger rate within the bandwidth limitations. The main source of the Level-1 Muon-Trigger background in the end-cap region is low momentum protons emerging from magnets and shielding in the forward region [2]. They produce correlated muon hits leading to coincidences in the muon trigger chambers up to the highest transverse momentum threshold. Requiring a coincidence with some other detectors lying inside the toroid magnets and shielding, lowers the fake event trigger rate.

This manuscript is based on the ATLAS experiment Level-1 Tile-Muon Trigger system, paying particular attention to the TMDB system. This work was carried out within the TileCal group of the ATLAS experiment collaboration. There is always a possibility to result in a permanent busy assertion by the TMDB boards due to hardware or firmware failures. The ROS can indefinitely fail to transfer events further due to hardware or firmware failures. The ROS then sends an "Xoff" signal indicating that data transmission has to be halted. When events are halted in the TMDB, the TMDB sends an xoff signal, also reffered to as the busy signal, to the TTC RODBusy module. The busy signal remains active (permanent busy assertion) until the TMDB is disabled or the problem fixed.

The Tile-Muon trigger system requires functionalities that will aid in detecting changes in conditions of an asserted permanent busy and send the stopless removal (recovery commands) to instruct the TDAQ system to remove the corresponding TMDB from the acquisition. This ensures that the corresponding input is ignored, allowing the triggers to flow again. The manuscript presents the hardware and the implementation of firmware and the stopless removal software for the Level-1 Tile-Muon Trigger system of the TileCal.

## 1.1 Manuscript organization

The manuscript organization is as follows: Chapter 2 introduces CERN, the LHC and the ATLAS experiment. The chapter covers the sub-detectors with particular focus on the hadronic Tile Calorimeter. It further discusses the Trigger and Data Acquisition System, and the Level-1 trigger system. Chapter 3 introduces the Read Out Driver (ROD)/TMDB lab test bench used for the Tile-Muon project. The test bench is located in building 175, Meyrin site, at CERN. This chapter gives the description of the Front-End and Back-End electronics in detail. Chapter 4 discusses the online software necessary for the implementation of the stopless removal. The chapter covers the ROD Crate DAQ, stopless recovery, DCS-to-DAQ connection, software release, versioning, organization and the build systems. Chapter 5 discusses the muon trigger detectors and the Level-1 Tile-Muon Trigger system. The chapter describes the Tile Muon Digitizer Board working principle and its implementation on the Level-1 trigger system. Chapter 6 discusses the handling of the busy signal. It describes the busy signal occurrence, busy signal handling, hardware, firmware and the software for the busy module. Finally, Chapter 7 summarizes and concludes the entire manuscript.

# Chapter 2

# CERN, LHC and the ATLAS experiment

Chapter 2 introduces CERN, the LHC accelerator, and the ATLAS experiment. It shortly discusses the ATLAS subsystems, with focus on the Tile Calorimeter.

## 2.1 CERN

CERN is the European Organization for Nuclear Research, responsible for operating the world's largest particle physics laboratory. The idea of CERN (French: Conseil Européen pour la Recherche Nucléaire), which translates to the European Council for Nuclear Research, came into place during the end of the Second World War. The idea was to revive European science, by creating a European atomic laboratory, where European nuclear physicists would unite, share ideas and also share building and operational costs of the nuclear physics facilities. The first official proposal was brought forward by Louis de Broglie, the French physicist at the European Cultural Conference. The European laboratory was opened in Lausanne on the $9^{th}$ of December 1949.

In December 1951, the first resolution concerning the establishment of a European Council for Nuclear Research was adopted at an Intergovernmental meeting of UNESCO,[1] (United Nations Educational, Scientific and Cultural Organization) in Paris. After two months, eleven countries signed an agreement establishing the provisional council. In 1952, Geneva was selected as the suitable site to build the CERN laboratory. In 1953, the convention establishing the organization was signed and ratified by the 12 founding member states. In 1954, the European Organization for Nuclear Research officially came into existence. The provisional CERN was dissolved but the acronym remains unchanged.

[1] A United Nations (UN) division devoted to contributing to peace and security by promoting international collaboration. This is done through educational, scientific, and cultural reforms in order to increase universal respect for justice, the rule of law, and human rights along with fundamental freedom proclaimed in the United Nations Charter.

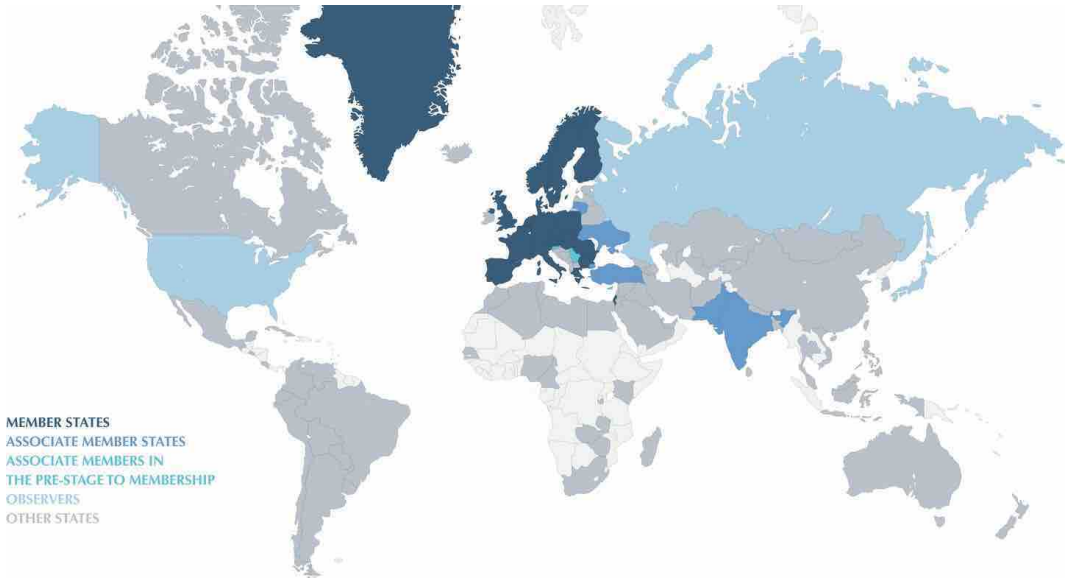



Figure 2.1: Global contribution at CERN

Today, CERN is run by 22 member states and many non-European countries. Figure 2.1 depicts the global contribution. Over 600 institutes and universities around the world use CERN's facilities. The responsibility for financing, construction and operation of the experiments, falls on the members and non-member states. CERN employs approximately 2500 people. The scientific and technical staff are responsible for designing, building and ensuring smooth operation of the particle accelerators. Currently, CERN has about 12 000 visiting research scientists from more than 70 countries and with 105 different nationalities. It is globally becoming more popular with science and technology advancement.
To date, CERN has paved way to a number of discoveries, predicted by the Standard Model (SM). The Standard Model is the name first coined in 1975 by Sam Treiman and Abraham Pais, making reference to the electroweak theory, a theory of fundamental particles and how they interact. The theory describes three of the four known fundamental forces (the electromagnetic, weak, and strong interactions, with the exclusion of the gravitational force) in the universe. It incorporated all that was known about subatomic particles at the time and predicted the existence of additional particles as well. There are seventeen named particles in the SM, organized into the chart shown in Figure 2.2. The $W$ and $Z$ bosons (1983), the top quark (1995), the tau neutrino (2000), and the Higgs boson (2012) were the last particles to be discovered. The SM has been highly successful in yielding experimental predictions. It however does not explain some phenomena, thereby proving in-adequate for the complete theory of fundamental interactions. It falls short in explaining baryon asymmetry, does not incorporate the gravitation theory, as detailed in general relativity or to explain the universe's accelerating expansion as described by dark energy. It is also difficult to fit dark

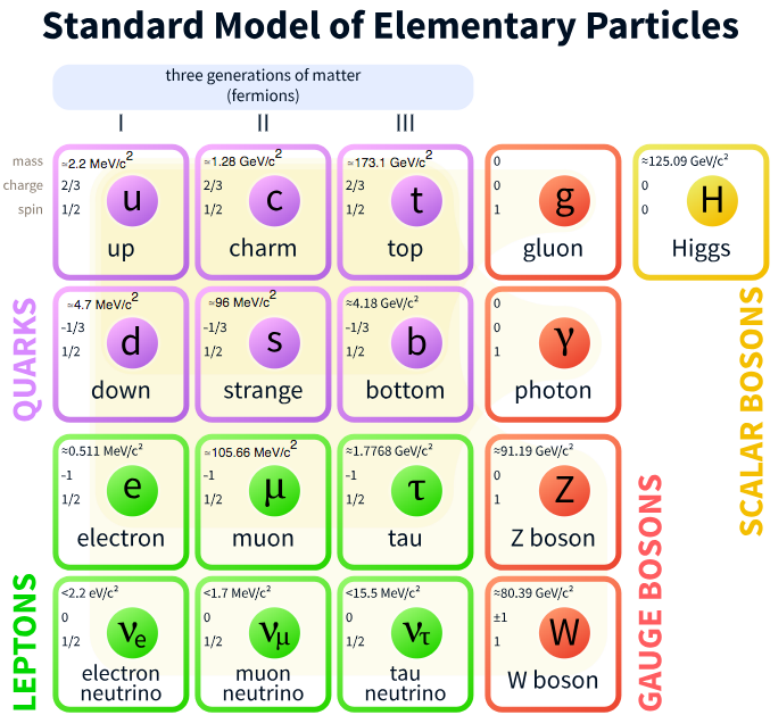



Figure 2.2: Standard model of elementary particles.

matter and the origin of the mass of the neutrino in the SM.

Predicted by the SM, the discoveries include the weak neutral currents by the Gargamelle,[2] experiments in 1974, which was the first experimental indication of the existence of the $Z^0$ boson, and consequently a major step towards the verification of the electroweak theory. Steven Weinberg, Sheldon Glashow and Abdus Salam shared the 1979 Nobel Prize in Physics for their theory, which predicted the existence of the $W^{\pm}$ and $Z^0$ bosons as propagators of the weak force.

The discovery of the $W^{\pm}$ and $Z^0$ bosons by the UA1 and UA2 experiments,[3] in 1983 led to Carlo Rubbia and Simon van der Meer being awarded the 1984 Nobel Prize in Physics, for their work leading to the discovery of these bosons at CERN. The accurate measurements of the $Z^0$ boson took place in 1989, which indicated that in nature there are only three conventional quark-lepton families of particles in the standard particle table. The discovery of the Higgs boson by the LHC's experiments ATLAS and CMS experiments in 2012, led to a Nobel Prize

[2]Gargamelle was a heavy liquid bubble chamber detector in operation at CERN between 1970 and 1979. It was designed to detect neutrinos and antineutrinos before being decommissioned. It is currently part of the microcosm exhibition at CERN, open to the public.

[3]The Underground Area (UA1 and UA2) experiments were high-energy physics experiments at the Proton-Antiproton Collider (SppS), a modification of the Super Proton Synchrotron (SPS) at CERN. The experiments ran from 1981 until 1990, jointly discovering the $W^{\pm}$ and $Z^0$ bosons.

in Physics 2013, which was awarded jointly to Peter Higgs and François Englert for their work in the theoretical discovery of a mechanism that contributes to our understanding of the origin of mass of subatomic particles. The Discovery of the Higgs boson completed the missing piece of the puzzle in the SM of elementary particles. Currently in 2018, physicists continue to investigate the nature and properties of the Higgs field, using data collected at the LHC and in-depth research shows the discovered Higgs boson continues to be in line with the predicted SM Higgs boson.

## 2.2 The Large Hadron Collider

The Large Hadron Collider (LHC) shown in Figure 2.4, is the most powerful and largest particle collider to be ever built worldwide. It is a complex experimental facility, built by CERN from 1998 to 2008. The LHC lies in a 27 km circular tunnel, that runs 100 metres deep under the France-Switzerland border near Geneva. The 27 km tunnel was initially built for the Large Electron-Positron (LEP) collider shown in Figure 2.3, which was commissioned in 1989. The LEP collider's energy was initially set at 91 GeV, suitable for the of $Z$ bosons and eventually reached 209 GeV in year 2000 after the upgrades. The upgrades enabled the pair production of $W$ bosons, each having a mass of 80.4 GeV. LEP's experiments ran for 11 years and collisions were observed by four large detectors, ALEPH,[4] DELPHI,[5] L3[6] and OPAL.[7]

During this period, detailed research of the electroweak interaction was conducted and the LEP conducted measurements, proved the existence of three generations of light neutrinos. In November 2000, after the successful critical test of the SM, the LEP was shut down to pave way for the construction of the LHC. The LHC was built with intentions to investigate and hopefully find answers to some of the fundamental questions in physics, with focus on the governing basic laws of interactions and forces within elementary objects.

The 27 km LHC ring is built of superconducting magnets with a number of accelerating systems to boost the energy of the particles along the way. As shown in Figure 2.3, a number of systems are arranged in series, in order to successively increase the energy of the particles. In filling the LHC, the linear particle accelerator LINAC 2 is the first system and it accelerates 50-MeV protons

[4]ALEPH (Apparatus for LEP PHysics) at CERN. It determined the $W$ boson and $Z$ boson masses to a greater accuracy of one part in a thousand.

[5]DELPHI (DEtector with Lepton, Photon and Hadron Identification).

[6]L3, one of the LEP experiments. Its huge octagonal magnet return yoke, remained in the same cavern position and became part of the LHC ALICE detector.

[7]OPAL (Omni-Purpose Apparatus for LEP) OPAL, was designed as a general-purpose detector for a broad range of data collection and it enabled high precision measurements of the Z boson lineshape.

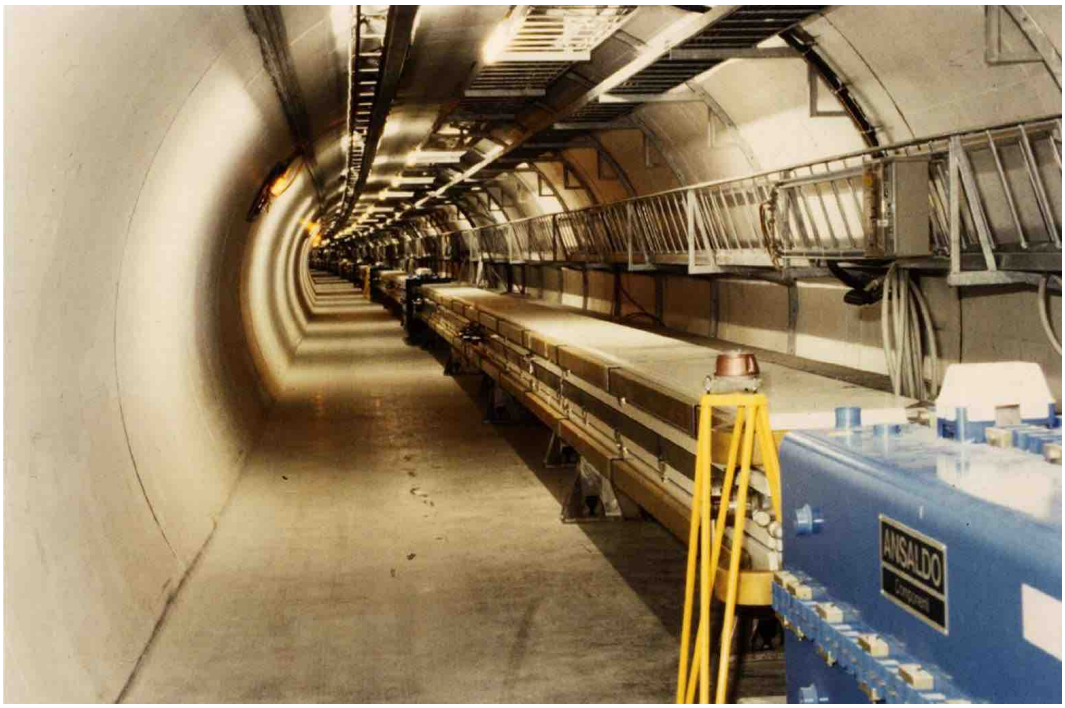



Figure 2.3: The underground LEP was in operation from year 1989 to 2000 [3].

from the proton source.[8] The protons are fed to the Proton Synchrotron Booster (PSB), which accelerates the protons to 1.4 GeV. After reaching 1.4 GeV, the protons are injected into the Proton Synchrotron (PS) and are accelerated to 26 GeV. After reaching 26 GeV, they are injected into the Super Proton Synchrotron (SPS), which accelerates the protons to 450 GeV. Lastly the 450 GeV protons are injected into the LHC ring in bunches and accelerated to their peak energy, which is currently 6.5 TeV per beam.

The two 6.5 TeV proton beams are accelerated close to the speed of light before head-on collisions. The beams travel in opposite directions inside separate beam pipes, two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. The electro-magnets are built from coils of special electric cable that operates in a superconducting state, efficiently conducting electricity without resistance or loss of energy. This requires lowering the temperature of the magnets to -271.3°C, a temperature lower than outer space. In order to achieve this, most parts of accelerator are connected to a liquid helium distribution system, which cools the magnets.

Thousands of different kinds of magnets are used for beam direction around

[8]Within a single bottle of hydrogen gas, an electric field strips hydrogen nuclei of their electrons, remaining with protons. Electric fields along the accelerator switch from positive to negative at a given frequency, pulling the charged protons forward in the accelerator.

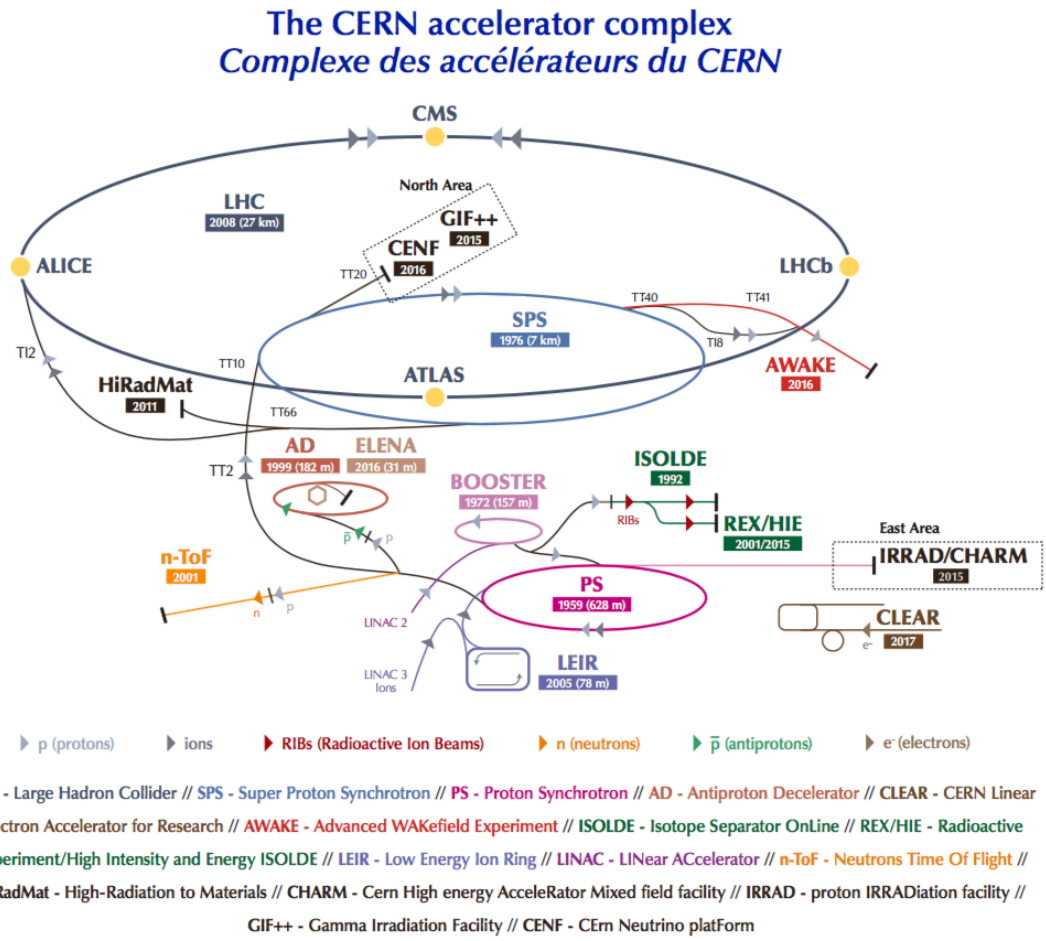



Figure 2.4: A diagrammatic representation of the CERN's accelerator complex [4].

the LHC. These include 1232 15 metre long dipole magnets shown in Figure 2.6, which are responsible for bending the beams, and 858 main quadrupoles to keep the beam in focus. The LHC has 6000 corrector magnets for preserving the beam quality.

Just before collisions, a different type of magnet is used to "squeeze" the particles closer together in order to increase the probability of collisions. The proton bunches are so thin that the mission of making them collide is comparable to firing 2 needles a few kilometres apart with such precision that they meet halfway. The LHC services and technical infrastructure are housed in different buildings and are controlled from the CERN Control Centre (CCC). The collisions of the beams in the LHC takes place at 4 points and are controlled from the CCC. These 4 points (as seen in Figure 2.4) correspond to the 4 particle detectors - ATLAS, CMS, ALICE and LHCb.

The LHC was successfully commissioned in 2010 for proton–proton collisions with a centre-of-mass ($\sqrt{s}$) energy of 6.5 TeV and sometimes collides beams of lead

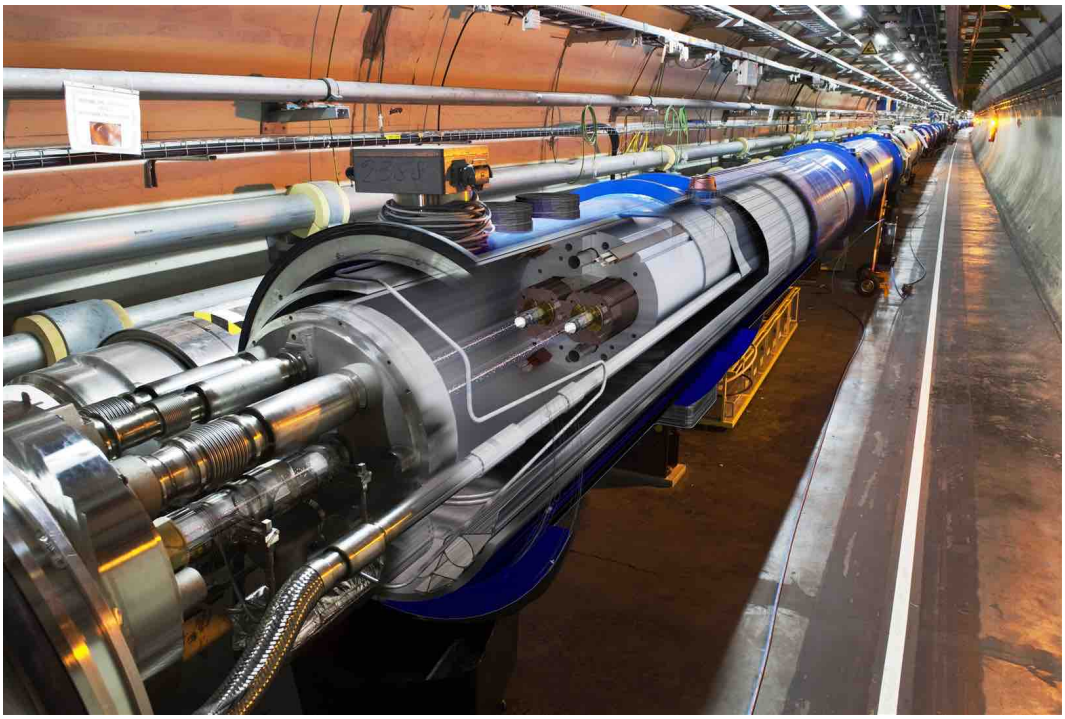


Figure 2.5: The current underground LHC tunnel [5].

nuclei (Pb). It delivered a $\sqrt{s} = 8$ TeV proton collisions from 2012 till the end of Run 1,[9] in 2013, with 50 ns between bunch crossings (bunch spacing). Following LS1,[10] in 2013-2014, it operated with $\sqrt{s} = 13$ TeV proton collisions during Run 2 from 2015 to date. In 2017, the LHC accelerated and collided fully stripped Xenon (Xe) nuclei for the first time at $\sqrt{s} = 5.44$ TeV per colliding nucleon pair. Table 2.1 shows the LHC parameters achieved in 2018.

| Parameter | Design | 2018 |
|---|---|---|
| Energy (TeV) | 7.0 | 6.5 |
| Number of bunches | 2808 | 2556 |
| Maximum stored energy per beam (MJ) | 362 | 312 |
| $\beta^*$(cm) | 55 | 30 |
| Protons/bunch (typical value of $10^{11}$) | 1.15 | 1.1 |
| Typical normalised emittance ($\mu$m) | 3.75 | 1.8 |
| Peak luminosity($10^{34}$ cm$^{-2}$s$^{-1}$) | 1.0 | 2.1 |

Table 2.1: LHC parameters achieved in 2018.

The bunch spacing has been reduced to a nominal value of 25 ns and with

[9]Runs refer to ATLAS data-taking period operations before and between long shutdowns.
[10]LS refers to the LHC machine's long shutdown periods.

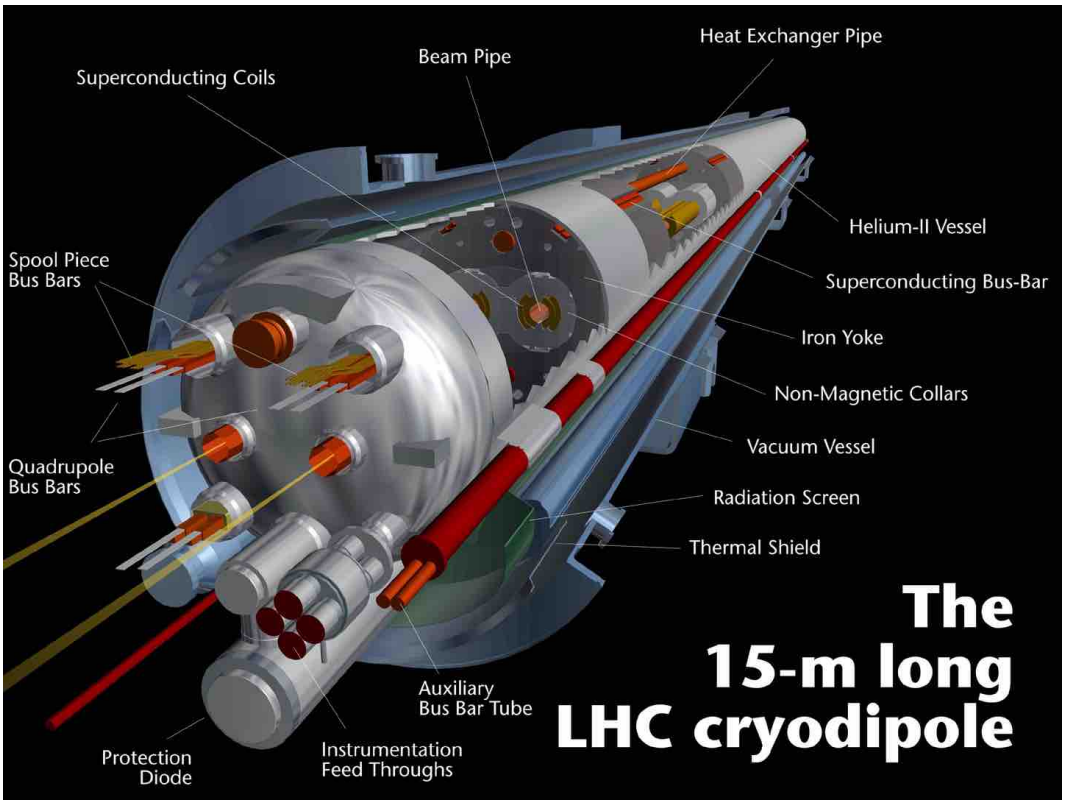



Figure 2.6: 1232 LHC cryodipoles are responsible for bending the beam around the 27 km circumference.

an increase in peak luminosity[11] reaching 1.7 x $10^{34}$ $cm^{-2}s^{-1}$. LS2 (2019-2020) is scheduled to prepare for peak luminosity of approximately 3 x $10^{34}$ $cm^{-2}s^{-1}$ in Run 3 (2021-2023) and increase the energy to the design value of 7 TeV.

LS3 (2024-2025) is foreseen for the HL-LHC (High Luminosity LHC) upgrade, after which the peak luminosity will increase by a factor of 10 and reach a constant level of about 7 x $10^{34}$ $cm^{-2}s^{-1}$. The HL-HLC aims to reach a total integrated luminosity of 3000 $fb^{-1}$ beyond 2026 as seen in Figure 2.7. This will boost the accelerator's potential for new discoveries in physics and also provide a better chance to see rare processes and improve the marginal measurements statistically.

[11]Luminosity is an important parameter in the accelerator and it determines the number of collisions generated in an interaction point per $cm^2$ and per second.

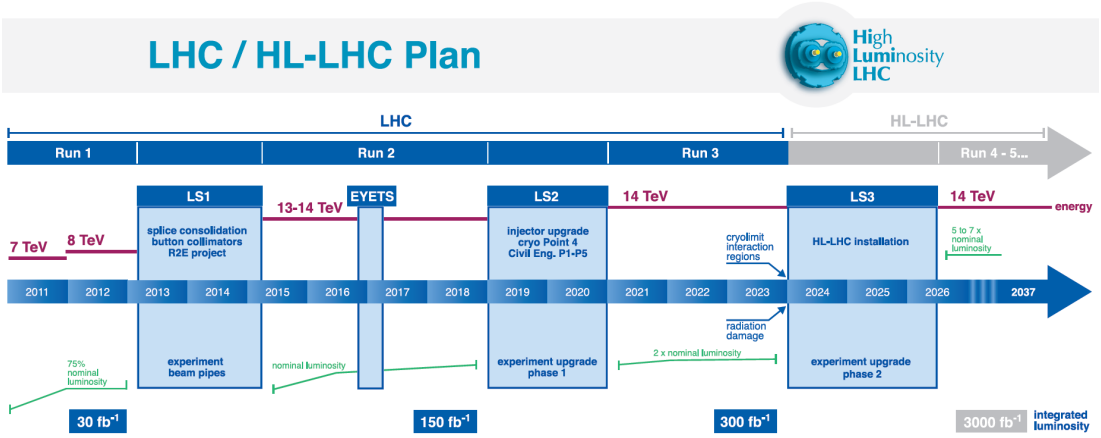



Figure 2.7: The LHC foresees three long shutdowns before constant nominal luminosity [6].

### 2.2.1 Particle production rate

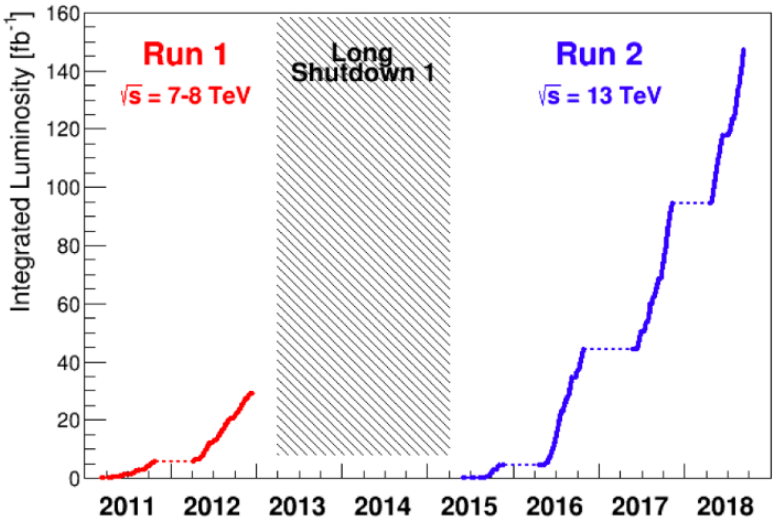



Figure 2.8: Integrated luminosities for Run 1 and Run 2. The Run 2 total was just below 150 fb$^{-1}$ in September 2018 [7].

The particle production rate ($R$) in the LHC is driven by two parameters, the ($\sqrt{s}$), which sets the cross-section,[12]($\sigma$) and the total integrated luminosity ($L$). The integrated production rate is given by equation 2.1.

$$R = \sigma(\sqrt{s})L \tag{2.1}$$

[12]Cross-section is the probability of interaction

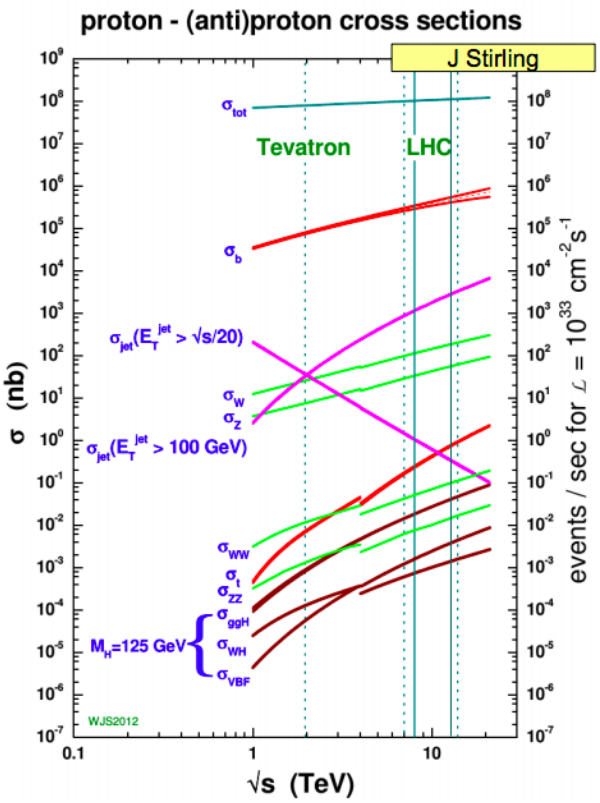



Figure 2.9: Cross sections as function of $\sqrt{s}$ at the Tevatron and LHC colliders [8].

The integrated luminosity is the integral of the delivered luminosity over time and it is an important value in characterizing the performance of the accelerator. The total integrated luminosity is obtained from the integral $\int L_{inst}dt$; where $L_{inst}$ is the instantaneous luminosity. $L_{inst}$ is obtained from equation 2.2, by the measurement of beam parameters during van der Meer (vdM) scans.[13]

$$L_{inst} = \frac{1}{4\pi}\frac{N^2 f}{\sigma_x \sigma_y t} \tag{2.2}$$

$N$ gives the number of protons per bunch, $f$ gives the fraction of bunch positions containing protons, $\sigma_x$ and $\sigma_y$ are the transverse dimensions of the Gaussian beam profiles and $t$ is the time between bunches. The LHC Run 2 produced five times more data than during Run 1. In October 2018, Run 2 reached a target of 150 fb$^{-1}$ delivered to both ATLAS and CMS as seen in Figure 2.8.

Quantum Chromodynamics (QCD) is critical to understanding the scattering processes at high energy hadron colliders and these scattering processes can be classified as hard or soft. The two cases are approached differently. With reference

[13]Provide a measurement of the beam-overlap area, which is proportional to the transverse beam size, needed to solve the luminosity equation.

to Figure 2.9, the rates and event properties of hard processes e.g high jet transverse energy ($E_T^{jet}$) production, can be predicted with some precision, using the perturbation theory. The rates and event properties of soft processes, e.g $\sigma_{tot}$ or diffractive processes, are dominated by the much less understood non-perturbative QCD effects.

### 2.2.2 LHC experiments

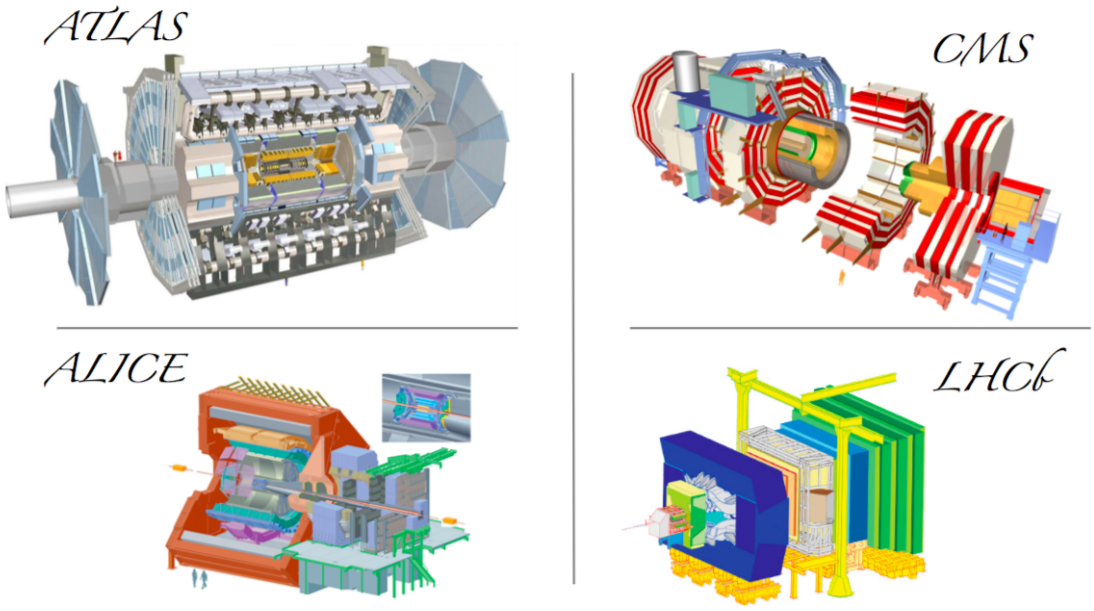



Figure 2.10: LHC's four main experiments.

The LHC makes use of seven experiments, to analyse an extremely great number of particles, produced by collisions in the four strategic points of the accelerator. The LHC has four main experiments, all designed for specific purposes. These four detectors are all located in huge caverns, 100 metres underground on the LHC ring.

1. **ATLAS** (*A Toroidal LHC ApparatuS*)

One of the two general purpose detectors, optimized to study the largest range of physics at a TeV scale, this includes the Higgs boson, heavy ion physics and supersymmetric particles. A detailed description of the ATLAS detector is given in section 2.3.

2. **CMS** (*Compact Muon Solenoid*)

It is a general purpose detector, built for the same purpose as the ATLAS detector. Two independently designed detectors are crucial for cross-confirmation of any new discoveries made. The discovery of the Higgs boson in 2012, was cross-confirmed by both, ATLAS and CMS detectors.

3. **ALICE** (*A Large Ion Collider Experiment*)

A detector dedicated to heavy ions collisions. ALICE specialises in unveiling the properties of a phase of matter called quark-gluon plasma.

4. **LHCb** (*Large Hadron Collider beauty*)

A detector dedicated to the investigation of minor differences between matter and antimatter the in the universe.

The other three LHC experiments are small scale detectors. TOTEM (TOTal Elastic and diffractive cross section Measurement) has the purpose of taking measurements of the total cross section, elastic scattering and diffraction dissociation. The detector is located near the CMS detector. The LHCf (LHC forward) studies particles generated in the forward region of collisions, almost in line with the $p$-$p$ beams. It measures the energy and the number of neutral pions, produced in collisions. This might aid in explaining the origin of the ultra-high-energy cosmic rays. The experiment has two detectors which are located 140 metres on either side of the interaction point. The ATLAS detector is located in the middle of these two detectors. MoEDAL (Monopole and Exotics Detector At the LHC) directly searches for the magnetic monopole and highly ionising stable massive particles. The detector is attached to the walls of the cavern of the LHCb experiment. It was upgraded in 2015 and still has not found any magnetic monopoles. It continues to search for the magnetic monopoles and new limits on the production cross section have been set to improve the search.

## 2.3 The ATLAS experiment

The ATLAS [9, 10] collaboration consists of 38 nations across the globe, with about 3000 physicists including more than 1000 students from more than 181 institutions. The ATLAS detector, seen in Figure 2.11, is a general purpose detector with a specific design for precision SM measurements and to conduct physics research beyond the SM [11]. It is the largest of the four major experiments at the LHC. Figure 2.11 [12] presents an overview of the ATLAS detector, displaying its proportions in comparison to a human being.

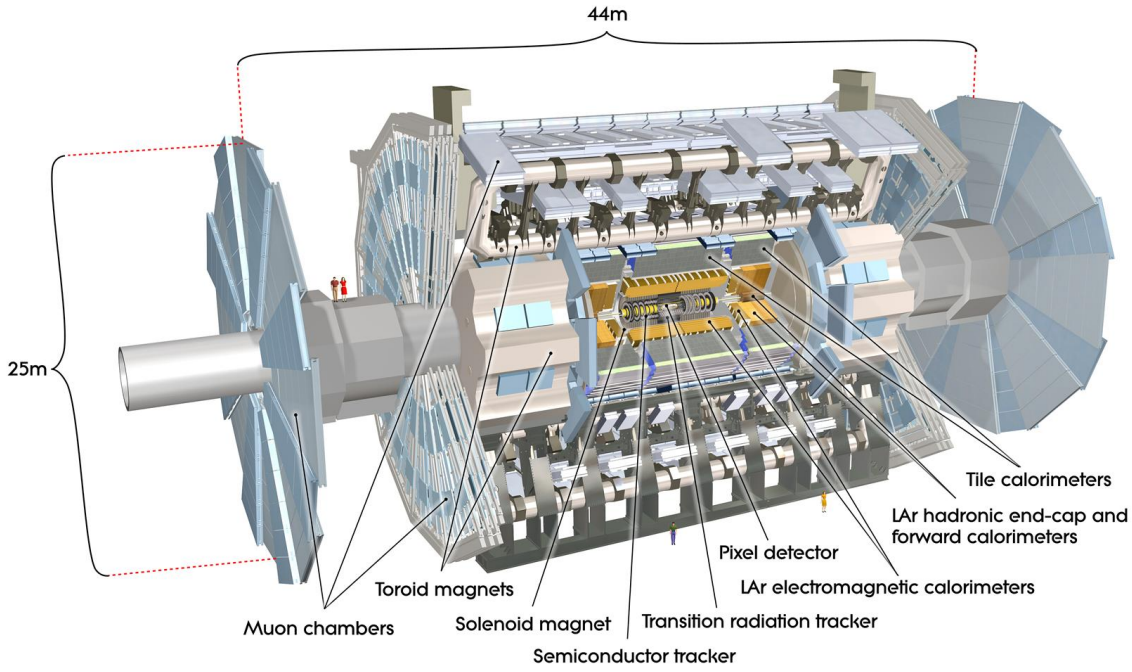



Figure 2.11: Overview of the ATLAS experiment. The collision of high speed particles, occurs in the centre of the experiment. The resulting particles are recorded by the tracking detectors which are dark grey, the calorimeters which are grey and orange, and the muon system shown in blue. Surrounding the tracking detectors is a solenoid magnet. The solenoid magnet and the toroid magnets, provide magnetic fields which are critical for the charged particle momenta measurements. Image is from [13].

Particles produced in the collisions emerge from the center of the detector in all directions as seen in Figure 2.12. The design of the detector is in various layers and this is important for the identification of all particles created during collisions. The ATLAS detector is comprised of four major components, the Magnet System, Muon Spectrometers, Inner Detector, and the Calorimeters. The major components are made up of contrasting subdetectors designed to detect distinct particles. The different tracks left behind by the particles in each subdetector allow for the identification of particles and the energy and momentum measurements. Details of the subdetectors are discussed in the following subsections. The ATLAS detector has a symmetric forward-backward and cylindrical geometry, it is approximately 45 metres long, with a diameter of 25 metres and weighs about 7000 tons. The ATLAS detector is specified under the right-handed Cartesian coordinates. The origin of the interaction point is at the centre of the detector, the $x$-axis pointing towards the centre of the LHC ring, $y$-axis pointing upwards and the $z$-axis, also referred to as the beam axis, travelling through the beam pipe.

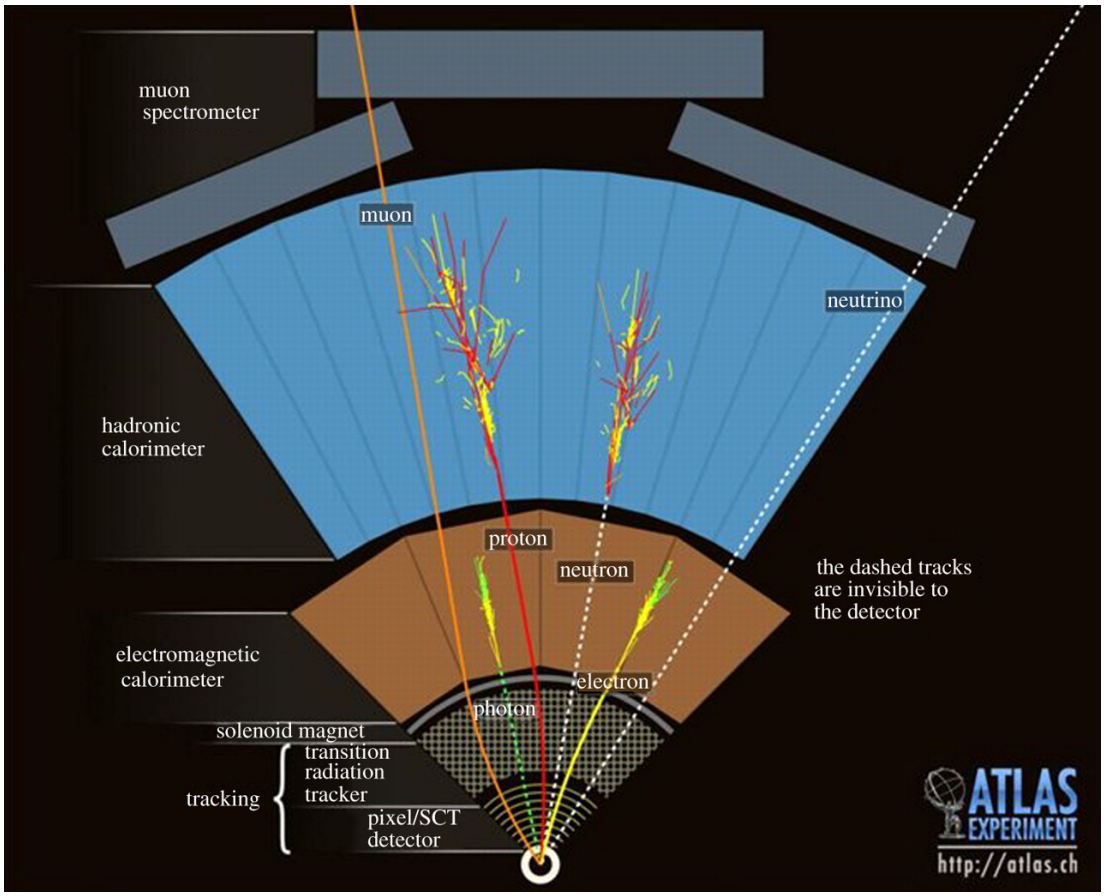



Figure 2.12: Transverse view of the ATLAS detector, showing particle detection in each subdetector.

The polar angle ($\theta$) is the positive angle of elevation from the axis of the beam. Cylindrical coordinates are used in the $xy$-plane, also called the transverse plane, with the radial distance (r) and the azimuthal angle ($\phi \in [-\pi, \pi]$) surrounding the beam axis. Figure 2.13 shows the orientation of the detector with respect to these coordinates.

The rapidity of a particle is defined in particle physics as

$$y = \frac{1}{2} \ln(\frac{E + p_z}{E - p_z}) \tag{2.3}$$

where $p_z$ is the magnitude of the momentum component along the beam axis. Conversely, the transverse momentum ($p_T$) of a particle is the magnitude of the momentum projected onto the $xy$-plane orthogonal to the beam axis. In the relativistic limit, the rapidity converges to a spatial coordinate measuring the angle of the particle with respect to the beam axis, called pseudorapidity ($\eta$):

$$\eta = -\ln(\tan(\frac{\theta}{2})) \tag{2.4}$$

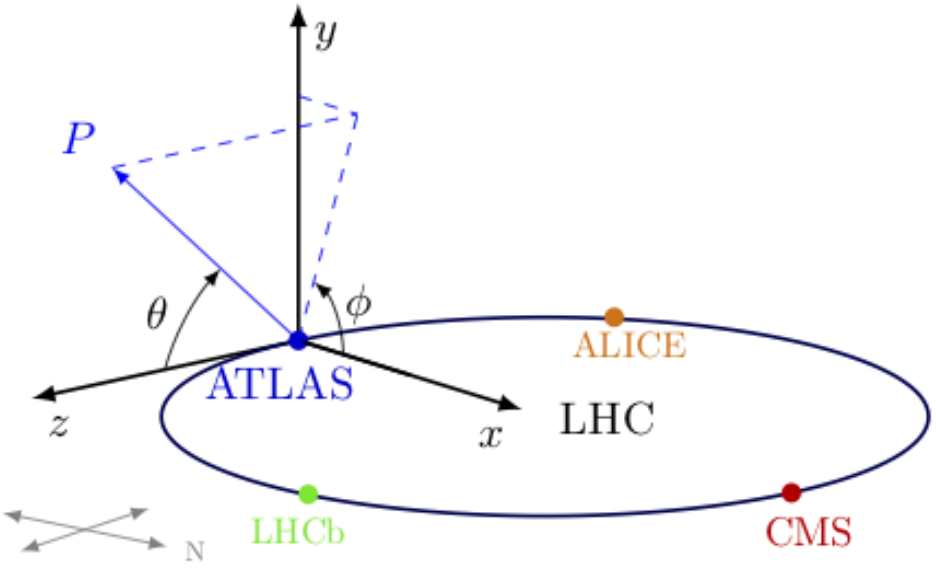



Figure 2.13: The right handed ATLAS coordinate system.

This cylindrical detector covers an angle of 2.5 for the trackers and 4.9 for the calorimeters given in $\eta$. For massless particles, $\eta$ remains invariant under boosts along the $z$-axis . For reasonably light, high-energy particles, pseudorapidity is a good approximation of the true rapidity. The detector pseudorapidity ($\eta_{det}$), measured at the detector centre,[14] marks the angular position of different detector regions, as shown in Figure 2.14. Central regions correspond to $\eta_{det}$ close to zero, and forward regions to high $|\eta_{det}|$ values.

[14]It is assumed that the pseudorapidity of an object is defined with respect to the object's origin point, i.e. jet pseudorapidity to the interaction point and detector pseudorapidity to the detector centre. In cases of ambiguity, $\eta_{det}$ is used to explicitly denote the detector pseudorapidity.

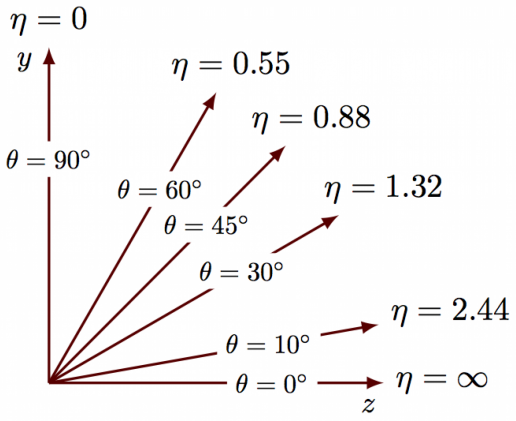



Figure 2.14: This is the symmetric half representation where the detector pseudorapidity marks different detector regions. Central regions approach $\eta_{det} = 0$, while $|\eta_{det}| \gg 0$ for forward regions.

### 2.3.1 Inner Detector

The tracking detectors, responsible for the measurements of direction, momenta and charge of electrically-charged particles after collisions, will be discussed in the following sections. The tracking detectors are the innermost layers of the ATLAS experiment. The beam pipe is surrounded by the tracking detectors, which cover the range of -2.5 $< \eta <$ 2.5, with full coverage in $\phi$. These tracking detectors are the pixel detector, Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT). The decay products of collisions propagate through the tracking detectors, inducing electric charges. The induced electric charges are collected and digitized. This produces "hits", [15] which are joined by the reconstruction software, producing trajectories of the charged particles. Figure 2.15 and Figure 2.16 show the organization of the tracking detectors.

#### Pixel detector

The pixel detector is made up of 3 barrel layers and 3 discs in each end-cap, situated in the forward direction. These pixel sensors and discs host 80 million silicon pixels, which are 50 x 400 $\mu$m$^2$ in size. They are spread out over a 1.7 m$^2$ surface. The hit information yielded by the pixels has a position resolution of 14 $\mu$m in transverse and 115 $\mu$m in the direction of the beam. Closer to the beam pipe, high spatial resolution is very important for the extrapolation of the trajectories of particles into the collision region, where sub-detectors cannot be installed. If hits occur in all layers, the pixel detector yields 3 high resolution points for particle trajectories. The pixel layers are shown as green surfaces, labelled "Pixels" in Figure 2.16. It also shows a fourth layer installed in LS1,

[15] Information about the parts of the sub-dectors where charged particles have traversed.

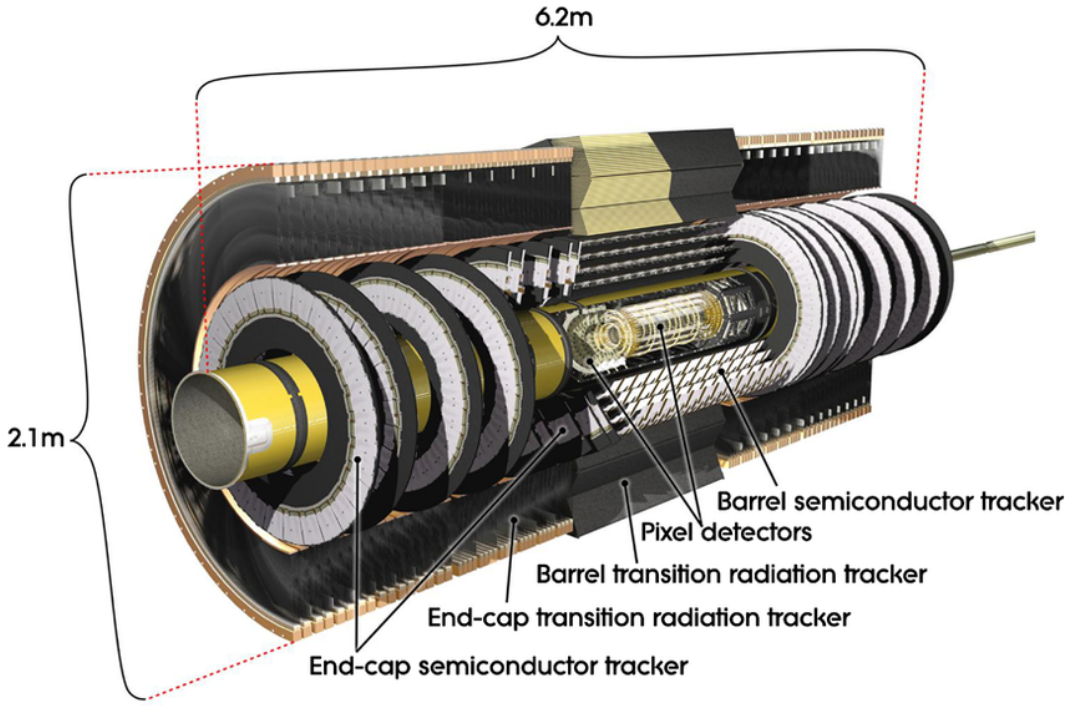



Figure 2.15: The Inner detector (ID) of the ATLAS experiment. SCT modules and pixel discs are for the extension of the acceptance of the tracking detectors up to $|\eta| = 2.5$, in the forward direction. [14]

Insertable B-Layer (IBL), placed 3.3 cm from the point of interaction.

### Semiconductor Tracker

The SCT is made up of 4 barrel module layers and 18 endcap discs, which accommodate 60 $m^2$ of silicon sensors. The sensors' readout strips are spaced at about 80 $\mu$m, to allow for a position resolution of 17 $\mu$m transverse to the strips. Small crossing angles are used for the installed layers, in order to provide position information in the readout strips direction, with about 600 $\mu$m of resolution. Double-sided barrel module layers yield up to 8 points for the particle trajectory. Figure 2.15 shows the barrel module layers and endcap discs.

### Transition Radiation Tracker

The TRT is the furthest tracking detector from the centre. It consists of 300 000, 4 mm diameter straw tubes. In the middle of each straw, ther is a tungsten wire, responsible for the detection of the charges produced in gas-filled tubes. The TRT provides $\gg 10$ hits with 170 $\mu$m in transverse position resolution. Electrons traversing the TRT, generate transition radiation, i.e. radiating photons. More charges are generated compared to heavier particles and this is useful in

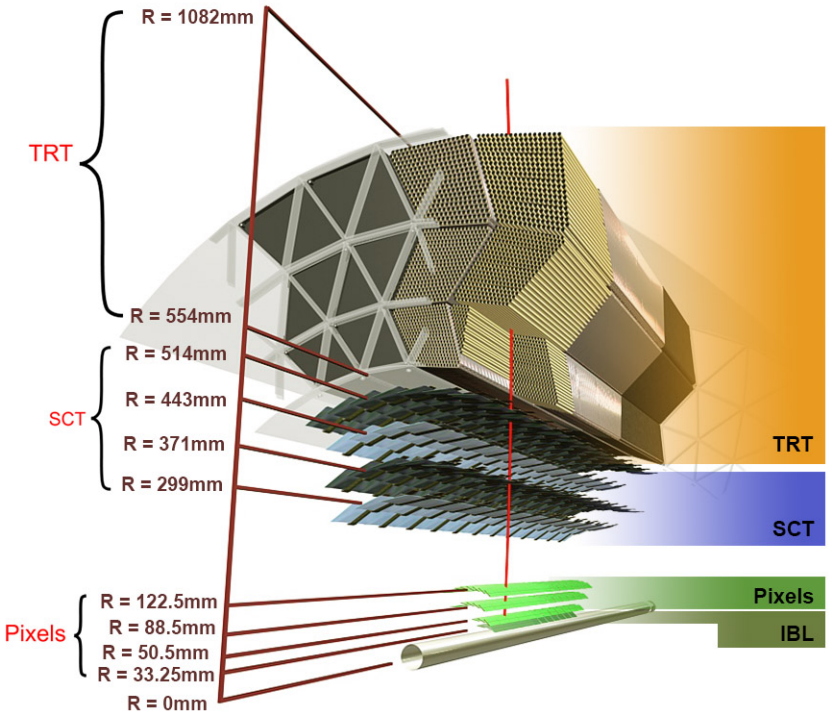



Figure 2.16: An exploded view of the sub-dectors, organized in layers. [15]. The IBL, 3 layers of pixel detectors, 4 for the SCT and TRT. The red line indicates the charged particle track.

the isolation of electrons from other particles. A solenoid magnet surrounds the inner detector, providing a 2 T uniform magnetic field along the beam line. The magnetic field bends the charged particle tracks in the transverse plane. The momentum,[16] in the transverse plane is determined from a curvature of the track, by applying the Lorentz force. The resolution of the transverse momentum measurements is given by [16]:

$$\frac{\sigma_{p_T}}{p_T} \approx 5 \times 10^{-4} \cdot \frac{p_T}{\text{GeV}} + 0.01 \tag{2.5}$$

High-momentum tracks have lower resolution as determined by equation (2.5). This is due to the straightness of the high-momentum tracks, which lowers the bending radius measurement. The transverse momentum resolution of an electron with $p_T = 100$ GeV, is expected to be approximately 6% and for $p_T = 25\,\text{GeV}$, is expected to be approximately 2%.

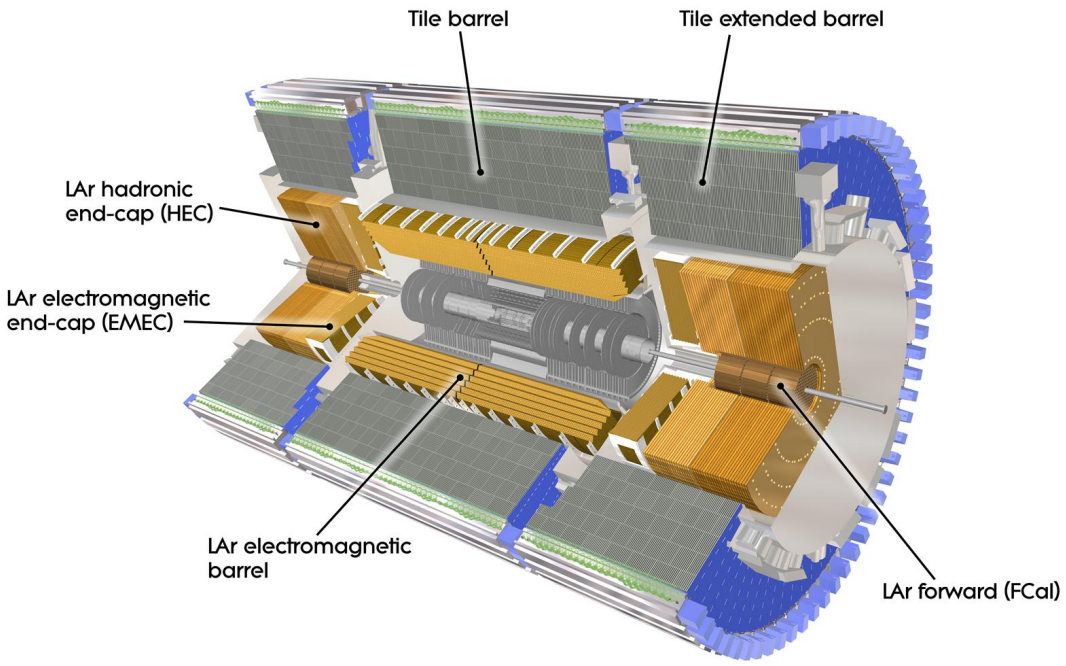



Figure 2.17: The ATLAS detector calorimeters [17]. The inner calorimeter (orange) is the liquid argon electromagnetic calorimeter. It is responsible for the detection of photons, electrons and positrons. It is surrounded by the tile calorimeter, responsible for the detection of hadrons. A number of forward calorimeters enclose the beam pipe, covering a range of -5 $< \eta <$ 5 (angular distance of approximately 0.8° from the beam axis).

### 2.3.2 Calorimeters

The Calorimetry measures the energy of particles and jets. It is essential for the detection of the traversing neutral particles which are not detected by the ID. Figure 2.17 shows the ATLAS ID enclosed by the calorimeters.

#### Liquid Argon EM Calorimeter

Liquid Argon EM Calorimeter (LAr ECal) is located inside the TileCal. It is an electromagnetic calorimeter, see Figure 2.18. EM calorimeters only measure the energy of the particles that interact electromagnetically. These particles are photons, electrons and positrons.[17] During the interaction with the material in the EM calorimeter, photons are converted to electron/positron pairs and they

[16]It is $p_T.q$ measured by ATLAS, where $q$ is a single elementary charge.

[17]There exists other particles that are not observed in the EM calorimeter but interact electromagnetically.

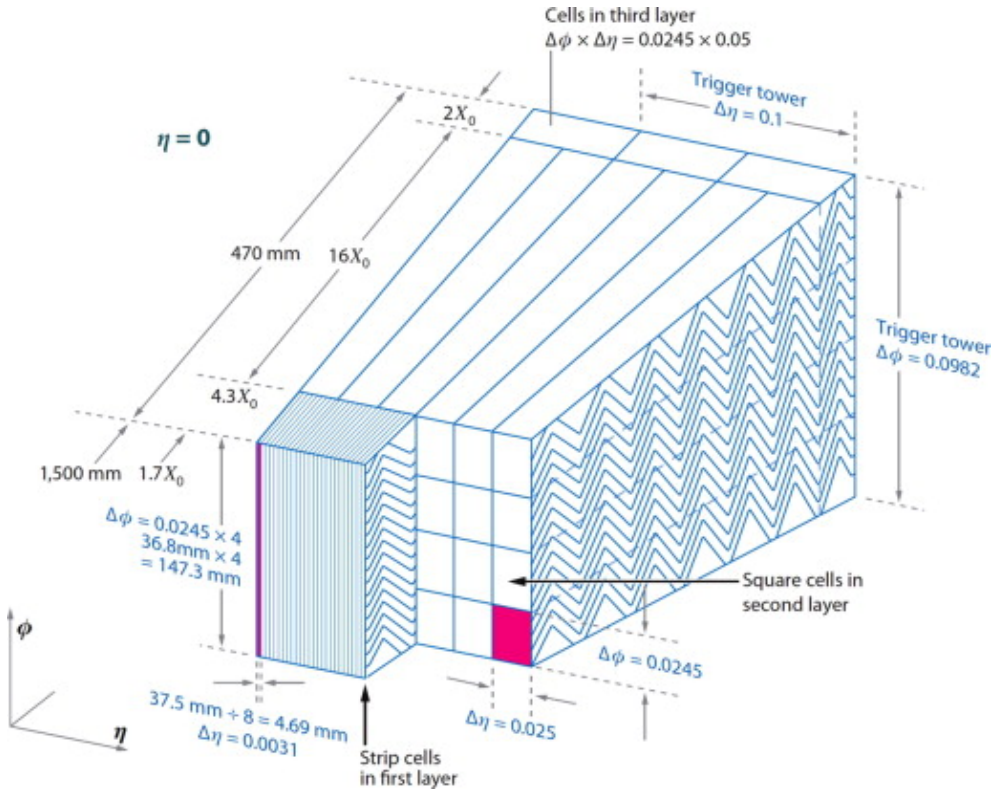



Figure 2.18: The ATLAS EM calorimeter is made up of liquid argon cells, which are kept apart by lead that is inserted between them. The liquid argon cells measure the deposited charge from EM showers. [19].

radiate photons when traversing the LAr ECal. The $e^+e^-$ pairs are produced by photons and this further produces particle showers in the LAr ECal [18]. The LAr ECal has a barrel segment (-1.475 $< \eta <$ 1.475) and 2 endcap segments, which cover the range of $1.375 < |\eta| < 2.5$ and $2.5 < |\eta| < 3.2$.

### Tile Calorimeter (TileCal)

The TileCal surrounds the LAr ECal and it is made up of the central hadronic section of the ATLAS experiment. TileCal covers a range of $|\eta| < 1.7$. Hadrons traverse the EM calorimeter with less impedance due to lack of Bremsstrahlung emission. Bremsstrahlung emission does not occur due to higher masses or missing electric charge. Hadrons can hadronically interact with the nuclei of the hadronic calorimeter. TileCal is made up of steel absorbers and plastic scintillators, in order to detect hadronic showers. The plastic scintillators emit light when excited by charged shower particles. Neutral pions decay to photon pairs, in turn producing EM showers and they can be detected. The light from the plastic scintillators is guided to photomultipliers by wavelength shifting (WLS) fibers (see Figure 2.21) [21]. The amount of light collected by the photomultipliers, is a measure of

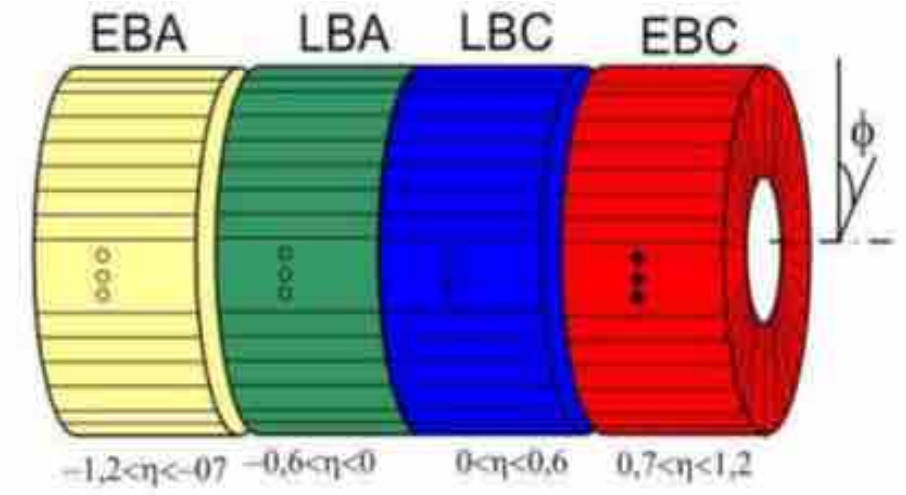



Figure 2.19: TileCal detector is divided into three barrels and four partitions.

the incoming hadrons or jets energy.

The TileCal is mechanically partitioned into three barrels, two extended barrels and one central barrel. Operationally, the system is split into four partitions, which are labeled as LBA and LBC for the long barrel A or C side, and EBA and EBC for the extended barrel A or C side as shown in Figure 2.19. Each barrel is assembled out of 64 wedge-shaped modules staggered in the $\phi$ direction as seen in Figure 2.20. The 64 modules have granularity of $\triangle\phi \cdot \triangle\eta = 0.1 \cdot 0.1$ (see Figure 2.21). For each module, the scintillating tiles are grouped into cells which are read out on both sides by a photomultiplier located along with the rest of the Front-End (FE) electronics in the super-drawers located at the outermost part of the barrels.

The TileCal readout electronics are divided into the FE electronics which are those mounted on the detector, and the BE which are installed in the counting rooms of the ATLAS cavern in a low radiation environment. The FE electronics are contained in mobile drawer units located in the radius beam back region of the calorimeter. Two drawers form a super-drawer which is inside of the two sides of the Long Barrel and on one side in each of the two Extended Barrels. The main FE components are the: PMTs, 3-in-1 cards, mother-boards, digitizer boards and the interface boards [21] and the BE electronics consist of various components in the TTC crate, ROD crate and TMDB crate. The functionally of each of these components will be discussed in Chapter 3.

The FE electronics are powered by low-voltage power supplies (LVPS). The data from the FE electronics is transferred to the Back-End (BE) electronics for further processing and if selected by the trigger, it is readout to permanent storage. The communication between the FE and BE electronics is done via redundant

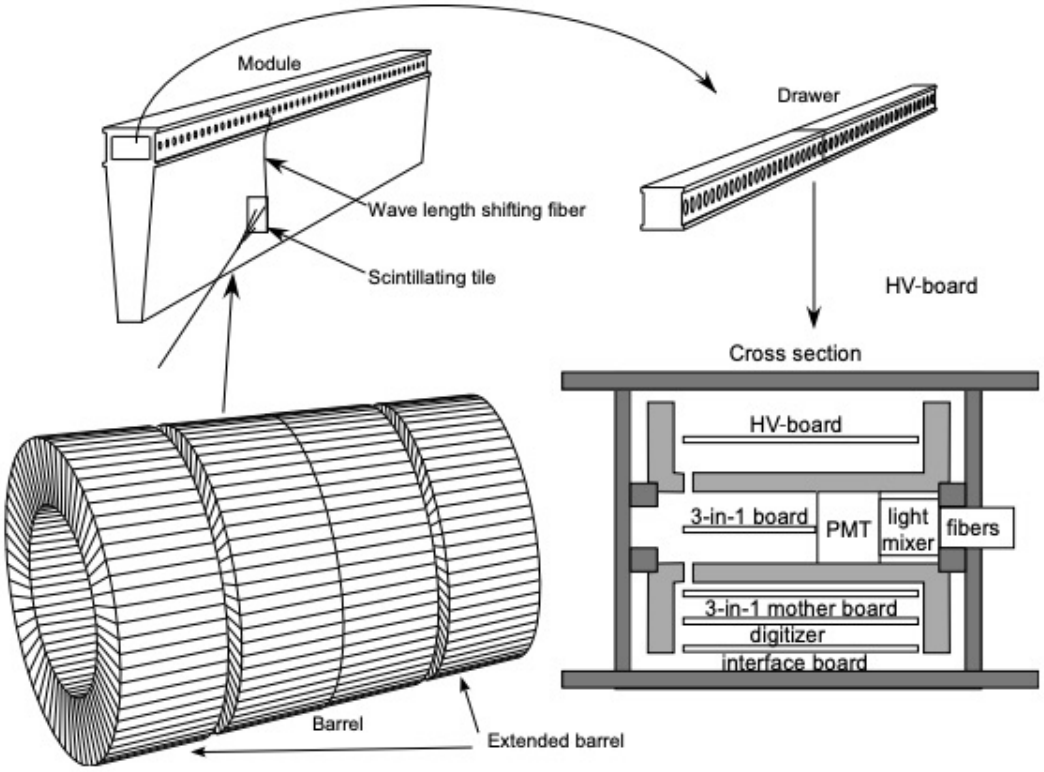



Figure 2.20: Tile Calorimeter has 3 barrels, each with 64 modules, housing the drawers that contain the FE electronics. The cross section shows the electronics housed in the drawer. The tiles are connected to photomultiplier tubes through wave length shifting fibers for light transmission [20].

optical links, which are of two types: The TTC from BE to FE and G-link from FE to BE. Finally, TileCal is instrumented with three detector calibration systems viz. charge injection scan (CIS) system, laser system and a $^{137}$Cs radioactive source [23], to be discussed in Chapter 3. Together these systems are used to calibrate the signals to the electromagnetic scale with very good precision.

### 2.3.3 Muon Spectrometer

The muon spectrometer is responsible for the measurement of the momenta of muons. It is the largest and furthest detector from the interaction region of the ATLAS experiment. It is shown by the grey and light-blue components in Figure 2.11. The muon system has a pseudorapidity covering range of $|\mu| < 2.7$, which is moderately greater in acceptance compared to the ID. It detects muons, since the calorimeters absorb all other particles with the exception of muons and neutrinos. Muons deposit small sums of energy when traversing the calorimeters since they are much heavier than electrons. The muon spectrometer

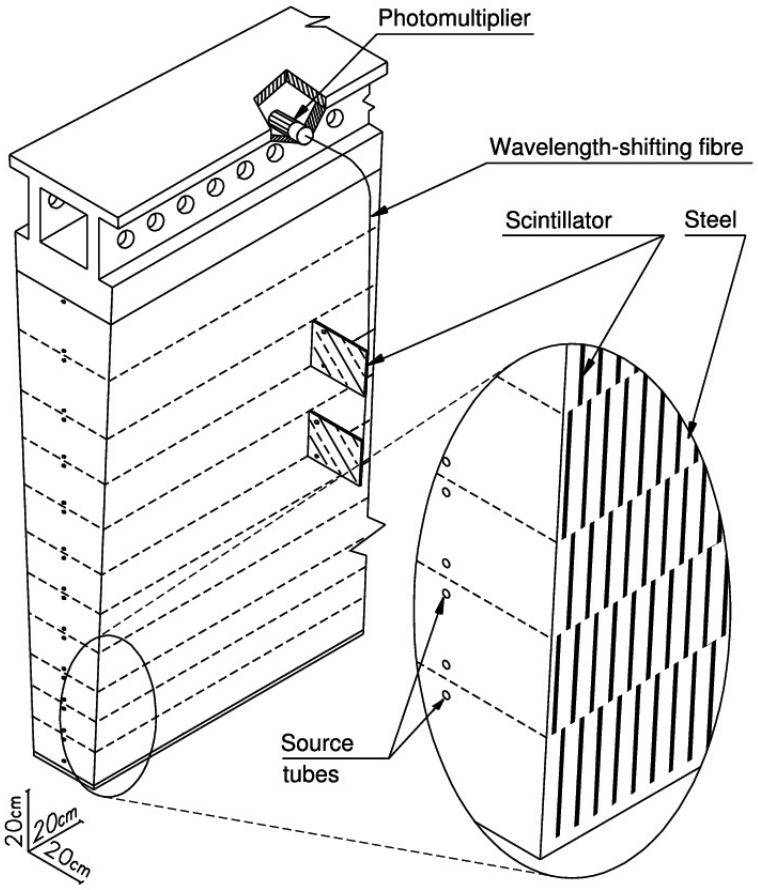



Figure 2.21: Schematic diagram of the TileCal wedge. It is made up of steel as absorber and plastic scintillating tiles. [22].

acts as a tracking detector, with a magnetic field ranging from 0.5 to 4 T, for measuring track curvatures and momenta. In the barrel region, there are 8 large coils which create the magnetic field and its range depends on the distance to the coils. The endcaps also have 16 small toroid coils with the same range of the magnetic field as the muon spectrometer. The muon system consists of 3 layers of tracking detectors, situated in the barrel and forward regions. They make use of a combination of low position resolution fast detectors and high position resolution slow detectors. This is essential for accurate timing and precision in position, or measurements in momentum. The muon system's momentum resolution ranges from 1.7 % at low $|\eta|$ for $p_T \approx 10$ GeV, to 4% at large $|\eta|$ for $p_T \approx 100$ GeV [24]. The muon system momentum measurements can be merged with the ID momentum measurements, to better the resolution. A detailed description of the Muon spectrometer will be given in Chapter 5.

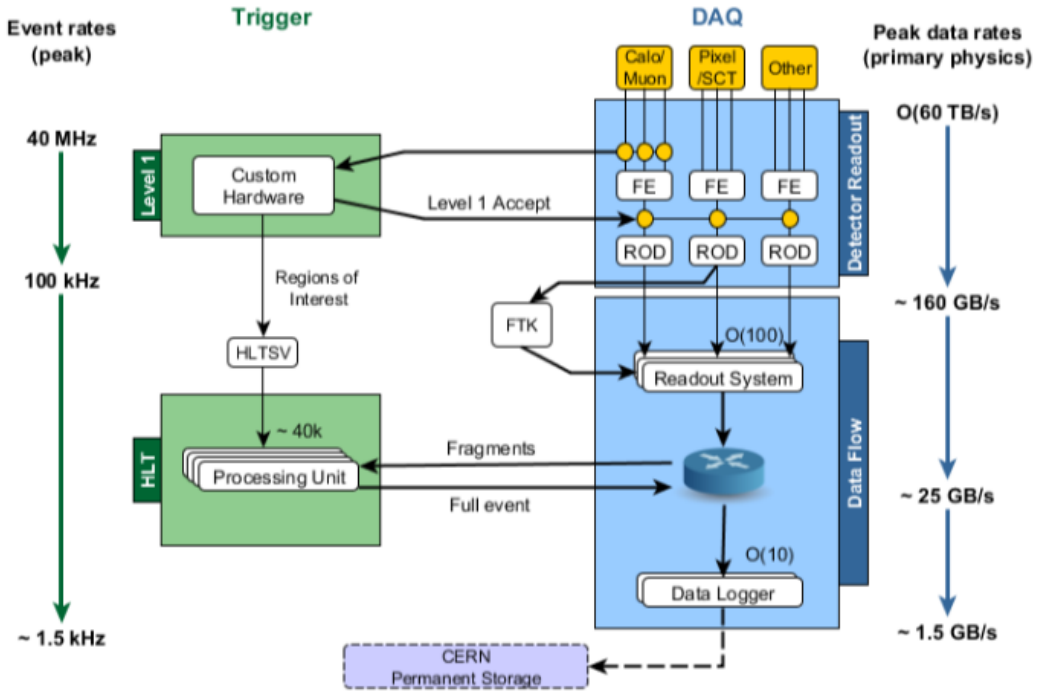



Figure 2.22: Overview of the TDAQ system.

### 2.3.4 The Trigger and Data Acquisition System

The ATLAS detector has a special design driven by technological limitations. The design has the capability to probe up to a billion $p$-$p$ collisions per second, with an integrated data volume greater than 60 million MB/s. Nonetheless, only a small fraction of the events will have interesting characteristics that may in a way, lead to new discoveries and measurements. In order to minimise the flow of data to levels that are manageable, the ATLAS experiment uses a specialised multi-level computing system, known as the Trigger System. The trigger system selects events with distinguishing characteristics that might be interesting for physics analyses. The trigger system selects 100 interesting events per second out of a billion total. The data is channeled by the Data Acquisition System (DAQ) from the detectors to storage.

The Trigger and Data Acquisition (TDAQ) System of ATLAS, shown in Figure 2.22 [25], is structured in a 2-level architecture. The levels are essential for the event rate reduction, from a collision rate of 1.7 GHz to about 1 kHz, for which the events are recorded in a permanent repository. The first level (LVL1) trigger is carried out with custom electronics to reduce the rate of accepted events from an input rate of 40 MHz (25 ns) to 100 kHz [26, 29]. In Run 2, the Run 1 second level (LVL2) trigger has been merged with the third level (event builder), to form

the High Level Trigger (HLT) [27, 28], which is made up of custom software, network switches and commercial computers. The HLT further reduces the rate of recorded events from 100 kHz to 1 kHz [26].

The event data from read-out electronics is received and buffered by the DAQ system at the LVL1 trigger accept rate. The LVL1 trigger lowers the rate to 100 kHz, operating at a maximum of 2.5 $\mu$s in latency budget [29]. LVL1 trigger merges the calorimeter data with the muon trigger processors data, before taking the last Level-1-Accept (L1A) resolution. Time in-between interaction and L1A arrival in the sub-systems is known as the LVL1 latency [30].

LVL1 trigger also provides details on the Region-of-Interest,[18] (RoI) to the HLT. Each sub-system keeps data of an event for a set period of time, to ensure the event data is read out as soon as L1A arrives. The fixed time is dependent on LVL1 latency and the event data arrival time in the read-out electronics. The pipeline memories located in the detector FE electronics are essential for the storage of the data pending the arrival of the L1A. Data related to each and every event, is only read out for the entire detector components after the LVL1 trigger has accepted an event.

The Read Out Driver (ROD) receives data about the event from pipeline memories, it then executes data compression and zero suppression. A detailed description of the ROD is given in Chapter 3. The data is transferred from the ROD to the Read Out System (ROS) through the Readout Links (ROLs), making use of the S-LINK protocol [31]. After receiving the data, the ROS sends the RoI fragments to the HLT and keeps data of the event in a customized memory buffer [25,32] for a full HLT period of latency. The HLT further executes additional selection criteria, which is dependent on LVL1 RoI data and full-granularity data. This is achieved by the implementation of software algorithms, that are significant for early rejection. Upon the acceptance of an event by the HLT, the event builder reads out the event fragments from all the ROSs and combines the fragments of the event into complete ones. The complete events further reach the Event Filter (EF) farm and they are handled by the use of offline-type algorithms, with accessible information of the full calibration and alignment. Events determined by the EF in the HLT are permanently stored at a CERN computer center [33].

### 2.3.5 The Level-1 trigger system

The LVL1 trigger system [34] executes quick selection of events, by using data from Tile and LAr calorimeters, and the muon detectors. The LVL1 trigger system outline is shown in Figure 2.23 [35].

The event selection in the calorimeter is dependent on the electromagnetic and hadronic calorimeter information, which is grouped into one subsystem, known as the LVL1 Calorimeter Trigger (L1Calo). The L1Calo trigger system makes use

[18]The location of the object when it passes the trigger threshold in the detector.

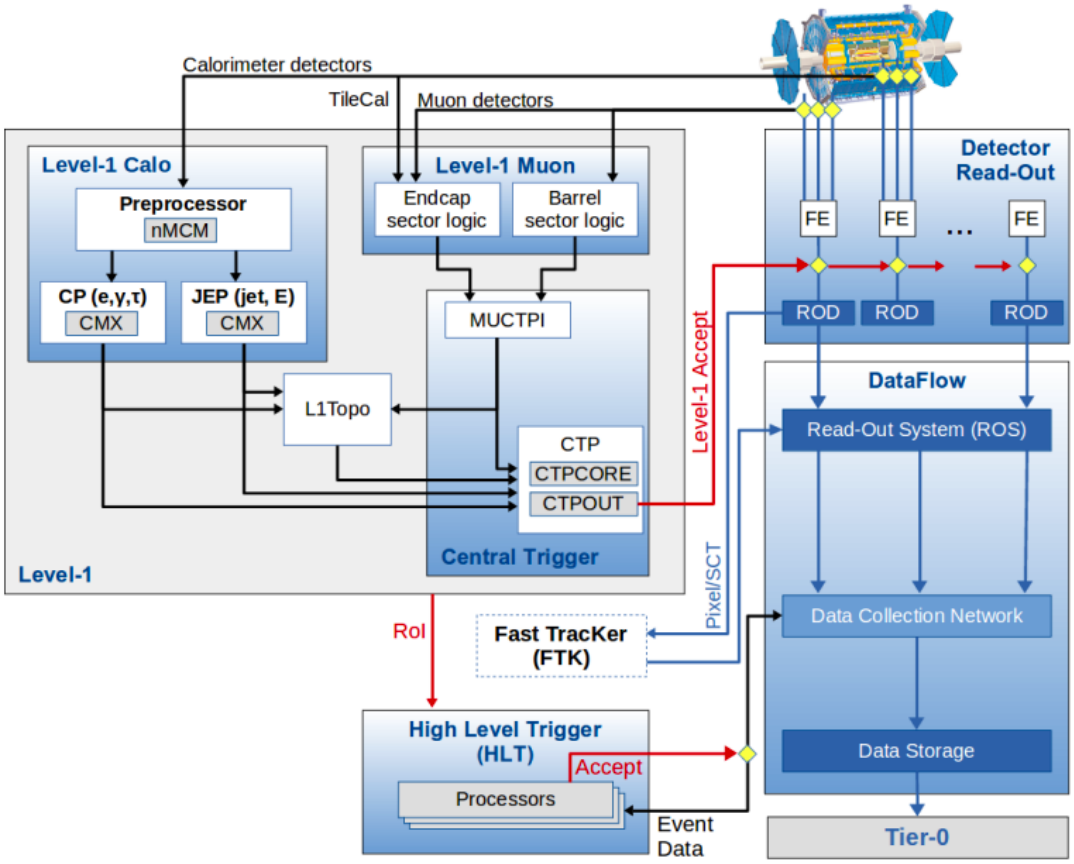



Figure 2.23: Level-1 trigger system outline [36].

of configurable algorithms to trigger on electrons, photons, muons, jets, $E_T{}^{miss}$,[19] and hadronically decaying $\tau$-leptons. The LVL1 trigger decision uses data from the calorimeter. This data is a multiplicity of hits for each $E_T$ threshold. The LVL1 Muon Trigger (L1Muon) system looks for hits with certain patterns, which are consistent with the high $p_T$,[20] muon originating from the collision point. The LVL1 trigger decision, uses muon data, which is a multiplicity of muons for $p_T$ thresholds. The Central Trigger Processor (CTP) [37] generates the L1A signal. It merges data coming from L1Calo and L1Muon systems. It further executes the selection of event by relying on the physics signatures seen in an event [38]. The L1A signal, simultaneously with the bunch clock, is distributed to the detector FE electronics at a set time after the interaction through the TTC system. The data about the position of trigger objects is obtainable from muon and calorimeter

[19]It is the energy that is not detected by the ATLAS detector, however anticipated due to the law of energy conservation and the law of momentum conservation. The difference in energy is due to different factors such as particles that escape detection, physics processes that haven't been accounted for and certain detector aspects such as noise and dead cells.)

[20]The transverse momentum $p_T$ represents the component of momentum in the $xy$-plane.

trigger processors. For each and every event that has been accepted by the LVL1 trigger, the data from the RoI is transferred and utilized in the HLT selection. The LVL1 latency must be kept to minimum due to the limited storage of the FE pipeline memory. The design of the FE electronics has the LVL1 latency being below 2.5 $\mu$s as per requirements. The experiment dimensions, the drift time in the Muon Drift Tubes (MDTs) and the cable length to the counting rooms have an effect on the latency budget. The cable length gives a delay of approximately 1 $\mu$s of latency, having 0.5 $\mu$s left for contingency. This leaves 1 $\mu$s in latency budget, which is to be split into LVL1 trigger subsystems, for data processing and transfer.

# Chapter 3

# The ROD/TMDB lab test bench in Building 175

This chapter entails a description of the ROD/TMDB laboratory test bench, describing the Front-End and the Back-End read-out electronics. The ROD/TMDB lab test bench read-out electronics are a replica of the ones used for the Tile Calorimeter in the ATLAS detector.

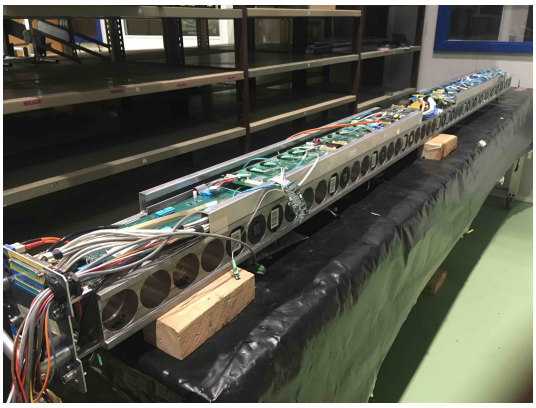
The TileCal read-out electronics are divided into two, the FE electronics and the BE electronics. The FE electronics are mounted on the detector and BE electronics reside in the ATLAS cavern counting room (USA15), which is a low radiation environment. In building 175 (B175), the FE electronics and the BE electronics are located under one roof but in different areas. Throughout the chapter, the FE and BE electronics in B175 will be discussed in relation to the ones currently used in the ATLAS detector.

## 3.1 Front-End Electronics

The FE electronics are located inside drawers that are inserted in the outer edges of the TileCal modules, see Figure 2.21. B175 currently has one module (see Figure 3.1a) that includes a super-drawer (see Figure 3.1b), set up in the lab. All the FE electronics on the super-drawer are powered by low voltage power supply (LVPS). The main FE electronic devices are PMTs, mother-boards, digitizer boards and the interface boards. [21]. The signal chain through the FE electronic devices is depicted in Figure 3.2 and Figure 3.3 gives a detailed overview of the signal chain.



(a) Module located in the Cesium lab.



(b) The super-drawer that holds FE elctronics and inserted into the module.

Figure 3.1: A pictorial view of B175, showing the module in the Cesium lab and the ROD/TMDB lab that houses the BE electronics.

### 3.1.1 Photomultiplier tube block

A particle traversing the scintillating tiles emits light that is transferred to the PMT by the WLS. The main function of the PMT block is to convert the light from the scintillating tiles into analogue signals, which are then digitized by two separate analogue-to-digital converters (ADCs) with a 1:64 gain ratio. Mechanically, it is assembled as a mu-metal,[1] shield for magnetic shielding and a steel cylinder. Its main components are: a light mixer, a PMT, a voltage divider and the 3-in-1 card [23].

#### Mixer

The light mixer is an optical plastic device that provides the interface between the PMT and the bundle of fibers which collect light produced in the plastic scintillators of the TileCal [23]. Its main functionality is to mix the light from all the readout fibers ensuring consistent lighting of the photo-cathode.

[1] A soft ferromagnetic alloy of nickel and iron, used for shielding sensitive electronic devices against static or low-frequency magnetic fields.

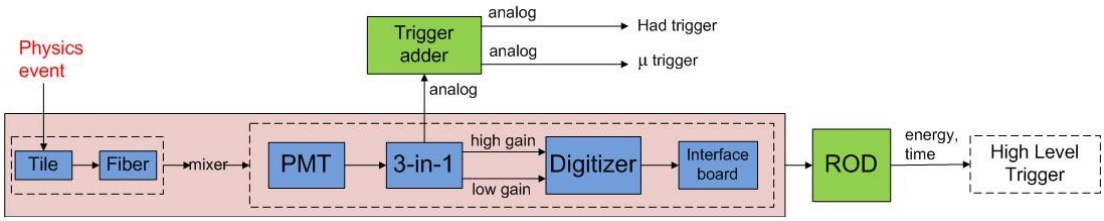



Figure 3.2: TileCal BE electronics signal chain [39].

#### PMT

The PMT is a compact 8-dynode device which measures light from the plastic scintillators. It is responsible for converting the light pulses from the fiber bundles into an electrical charge [41].

#### Divider

The Divider is a printed circuit device with surface mounted components. It is attached onto the 3-in-1 board. The divider is used for partitioning the high voltage between the dynodes of the PMTs since the PMTs require high voltage for operation. This voltage is supplied to the PMTs by external high voltage power supplies (HVPS) that deliver 800 V from USA15.

#### 3-in-1 card

The 3-in-1 card receives an electrical pulse that has been detected and amplified by the PMT. The electrical pulse is transmitted through the pre-amplifier in the 3-in-1 card. The main functionalities of the 3-in-1 card, are to provide a high and a low gain shaped pulse for the digitizer boards, slow integrator readout signals used for monitoring and calibration, and the Charge Injection Scan (CIS) system. The 3-in-1 card also provides a third analog trigger signal output to the LVL1 trigger summation board.

### 3.1.2 Mother-board

The mother-board serves as the base element that holds all the drawer electronics together, as shown in Figure 3.3. It provides power and TTC commands to the 3-in-1 boards and also accommodates four digitizer boards and a single interface board. There are two mother-boards contained in each super-drawer.

### 3.1.3 Digitizer board

The digitizer board receives bi-gain (low and high) signals from the PMT 3-in-1 cards as input to its ADCs. Each PMT is readout by two separate ADCs. The digitized data from six ADCs (3 PMTs) is sent to one data management unit (DMU)

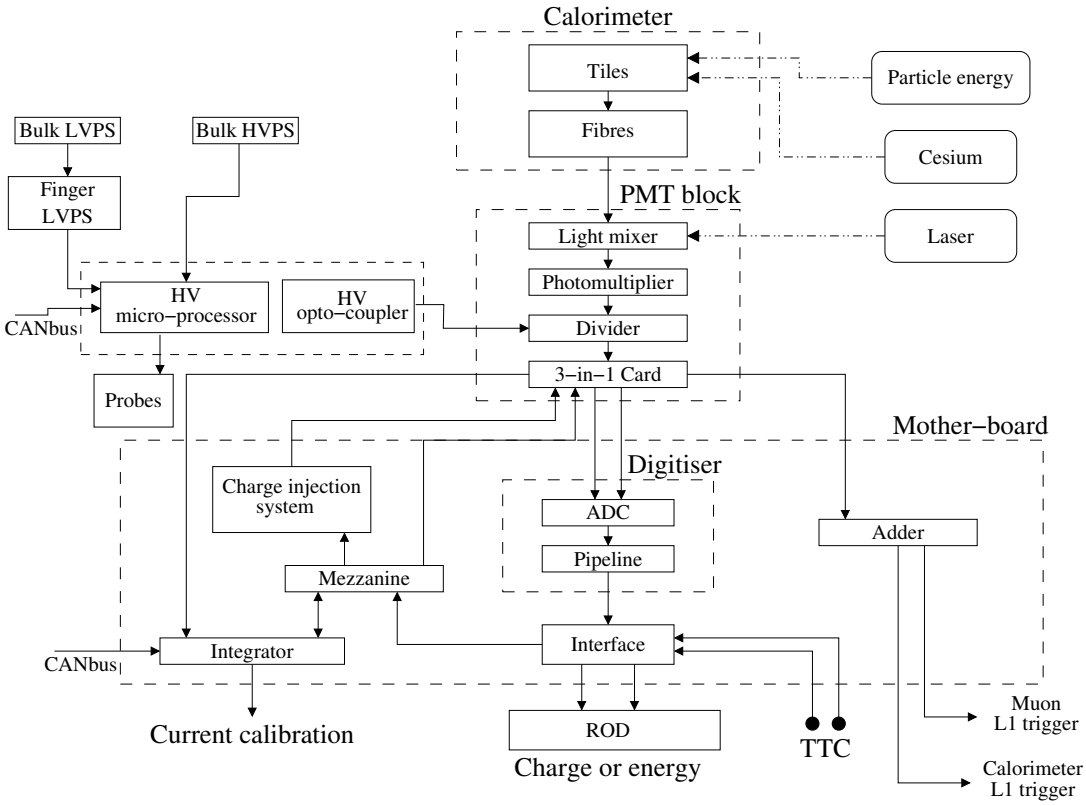



Figure 3.3: The Tile Calorimeter read-out FE electronics overview [40].

ASIC chip which implements specific circuitry for the required pipeline and buffer memories, cyclic redundancy check (CRC), memory parity checking, bunch crossing identification (BCID) and gain logical selection computations. Each board is equipped with 12 ADCs for reading 6 PMTs, 2 DMU chips, and one TTC receiver (TTCrx) chip for the control and distribution of ATLAS clock. There are 8 digitizer boards in each Long Barrel super-drawer that readout 45 PMT blocks, and 6 digitizer boards in each Extended Barrel super-drawer that readout 32 PMT blocks.

### 3.1.4 Interface card

The Interface card receives digitized data from the digitizer board upon the reception of a L1A signal from the LVL1. Each super-drawer is equipped with one interface card. The interface card encodes and transmits the data through dedicated fiber-optical links to the BE electronics and receives TTC commands from it as seen in Figure 3.3. The entire readout section for the interface board has been replicated with two dedicated output optical fibers for redundancy and to reduce single event upset errors. The interface board also computes the Check Sum (CRC) on the input and output data streams which are used in the BE elec-

tronics not to process data affected by single event upset errors and to perform online data quality checks [42].

### 3.1.5 Trigger summation boards

The trigger summation board sits on the mother board and its purpose is to merge low gain analogue signals from the 3-in-1 boards up to a maximum of six in order to form the analogue trigger-tower sums which are required by the LVL1 trigger.

## 3.2 Back-End Electronics

The BE electronics are organized into four TTC partitions, as mentioned in the Chapter 2, section 2.3.2, under the TileCal detector. Each partition consists of 64x2 TTC links to write and 64x2 ROD links to read from the detector. The TTC links are connected to TTC modules in a 6U Versa Module Eurocard (VME) crate and the ROD links are connected to ROD modules in a 9U VME crate. In the TileCal, these crates are known as the TTC and ROD crates (see Figures 3.4a and 3.4b), in order to easily specify the type of electronic boards they contain. In each of the crates is a Single Board Computer (SBC) that controls the VME crate. DCS and monitoring of the crate is done by the fan-tray and read-out by DCS through CANbus. Figure 3.5 shows a schematic diagram of the VME crate modules. In B175, the TTC crate contains the SBC, ATLAS Local Trigger Processor (LTP) module, Local Trigger Processor Interface (LTPi) module, TTC VME bus interface (TTCvi) module, TTC emitter (TTCex) module, TTC receiver in PMC Form Factor (TTCpr) module, ROD Busy module and the Shaft module.

### 3.2.1 TTC crate

#### Single Board Computer

The TTC crate is controlled by a SBC. The SBC is equipped with VME bus interface that allows mapping of all modules connected to the crate. It is a Concurrent Technologies (CCT) VP-917/919, Intel Core i7, 4/8 GB RAM, dual Ethernet PC and 64-bit. It is remotely booted and loads a Scientific Linux CERN (SLC) version specifically tuned for ATLAS. The TDAQ drivers and specific services are loaded at start up. The SBC communicates with the other boards in the crate, through VME bus. The B175 SBCs in the crates are named as follows:

- TTC crate: sbctil-ttc-01
- ROD crate: sbctil-rod-01
- TMDB crate: sbctil-trg-01



(a) The TileCal BE read-out electronics in USA15.



(b) TileCal B175 ROD/TMDB BE read-out electronics

Figure 3.4: The TileCal BE read-out electronics in Point 1 consist of four partitions, while B175 consists of one partition. The colours of the four crates, correspond to the TileCal detector barrels shown in Figure 2.19.

### Local Trigger Processor Module

The ATLAS Local Trigger Processor (LTP) receives timing and trigger signals from the CTP through the Link-in cable and distributes them into the TTC system of the sub-detector through NIM outputs. This module can also be used in stand-alone mode by using local timing and trigger signal sources or by internal signal generation via a pattern generator.

### Local Trigger Processor Interface module

The ATLAS LTP interface (LTPi) module provides an interface between the CTP and LTP to allow combined parallel running between various sub-detectors as opposed to the ATLAS global run.

### TTC VME bus interface module

The ATLAS TTC VME bus interface (TTCvi) module serves the purpose of configuring the FE electronics and interface the local TTC system to the global TTC system. The TTCex provides A and B channel signals to the TTC distributors for optical conversion, encoding, multiplexing and distribution to the TTCrx chips

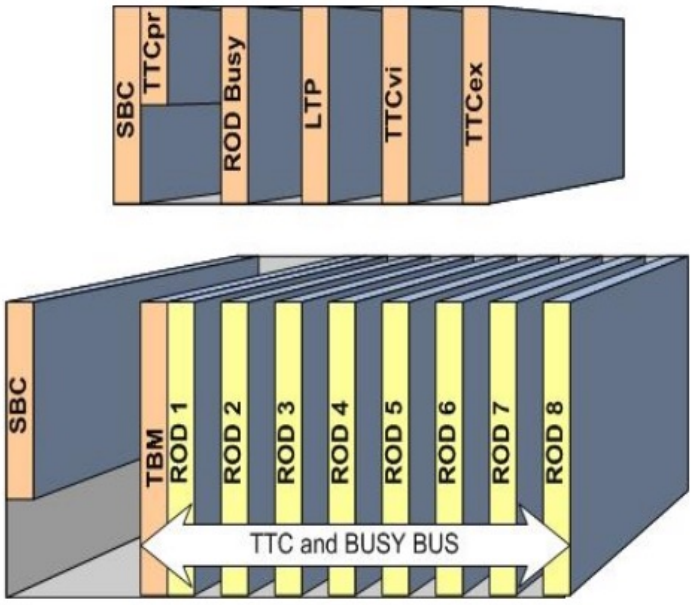



Figure 3.5: Diagrammatic representation of the TileCal TTC and ROD VME modules in the crates.

for the corresponding FE and BE electronics controllers. The TTC channel A is used for the distribution of the L1A signal to the TTCvi. The TTC channel B is used for the transmission of formated and framed commands and LHC clock synchronous or asynchronous data.

### TTC emitter module

The TTC emitter (TTCex) is a laser based module which converts TTCvi commands into optical signals that arrive to the FE and BE electronics. It provides 10 optical outputs at a level of approximately 0 dBm. The optical outputs of the TTCex are fanned out by a 1:32 TTC optical coupler (TTCoc) to broadcast to a total of 320 destinations. The TTCoc is a 1 to 8 splitter to distribute the signals to all the drawers in a sector, where a sector covers 8 modules in 1 ROD.

### TTC receiver in PMC Form Factor module

The TTC receiver and PMC Form Factor (TTCpr) [43] module is a mezzanine card plugged into the SBC of the TTC crate. It is used to make available the Tile TTC information in the TDAQ framework for calibration runs. The TTCpr buffers the EventID, BCID, and trigger type (TType) associated with each L1Accept. It asserts a busy signal that is propagated to the ROD Busy module after a TTC event has been received. The busy signal is cleared after the EventID, BCID, and TType have been read out from the TTCpr.

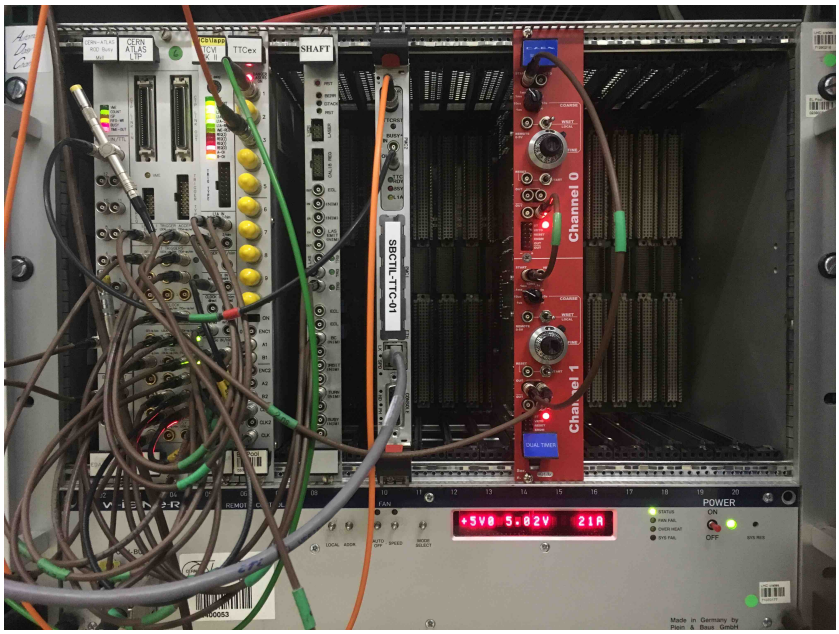



Figure 3.6: B175 TTC crate housing different modules.

#### Read Out Driver Busy module

The RODBusy module is used to monitor the busy signal. It measures the busy in bunch crossing units and produces the sum of each of its 16 busy input lines which can be conveniently masked. This module generates a VME interrupt signal after a programmed time-out, which is used for monitoring the busy states. In the TileCal, this module sums the busy signal from the ROD crate Trigger and Busy Module (TBM) and the TTCpr card. The busy output is sent to the LTP busy input.

#### Shaft module

The Shaft is a TileCal specific module responsible for controlling different calibration trigger requests. It is a specific VME board module that is able to share calibration requests during physics runs. Each calibration request can be enabled and its firing timed with respect to the TTC signal that clocks the turn of the LHC beam.

### 3.2.2 Laser Read Out Driver

This module is a 6U VME module that provides information from the Laser calibration system into the data-flow and furnishes TTC signals to the Laser system. It is equipped with a High-speed Optical Link (HOLA) card which provides data fragments to a Readout Buffer (ROB) of the LBC partition ROS through a dedi-

cated readout link (ROL).

### 3.2.3 Read Out Driver crate



Figure 3.7: B175 ROD crate housing one ROD module, TBM and SBC.

The B175 ROD crate shown in Figure 3.7, houses the ROD which is controlled and monitored through the VME bus by the SBC named sbctil-rod-01. In Point 1, there are four ROD crates corresponding to four partitions and each ROD crate houses 8 RODs installed in the slots 6, 8, 10, 12, 14, 16, 18, 20. For all the 4 partitions, there are 32 RODs in total and each ROD is connected to 8 super-drawers. In B175, only one ROD is installed in the ROD crate and it is connected to one super-drawer.

#### Read Out Driver module

The ROD [44] is located between the FE electronics and the ROS of the LVL2 trigger. The data from the FE electronics is transmitted in and out of the ROD through optical links on the board for each super-drawer. The ROD board supports 4 Processing Units (PUs) for computing the energy and time for each readout channel, as seen in Figure 3.8. The PU is a mezzanine card with utmost importance to the ROD, it is instrumented with two input FPGAs, two Digital Signal Processors (DSPs) and one output FPGA. The output FPGA provides interface with the rest of the ROD. The Input FPGA receives data from two FE links which are checked and formatted for DSP processing. The ROD is coupled to a Transition Module (TM) located behind it, which receives the data fragments

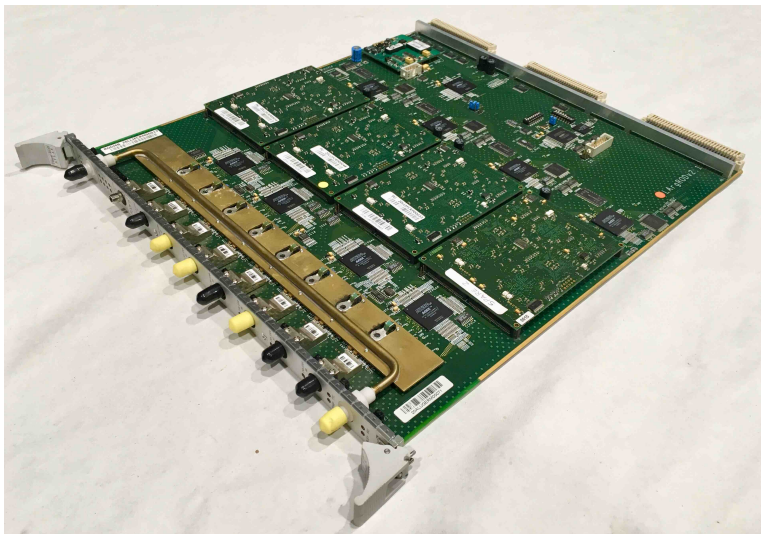


Figure 3.8: ROD module equipped with four PUs.

through the connectors of the VME crate back plane.

The ROD has been using two PUs until early 2017 and the four PU design is now being fully utilized. The number of PUs, ROS, ROLs and HOLA cards have been doubled to increase the readout bandwidth. The TM was also upgraded during the ROD upgrades, it is now equipped with four HOLA cards that transmit data fragments to the ROS through the ROLs. The author's contributions to this ROD upgrades was to modify the TileCal Online software to accommodate the doubled number of HOLA cards, PUs, fiber connections and the ROLs. Details of the current B175 TileCal Online software modified by the author will be presented in Section 3.3.

#### Trigger and Busy Module

The TBM is a 9U VME module. It receives TTC signals through optical links from the local TTC system. The signal is propagated to every ROD module through P3/J3 connectors using the CP3 backplane in the ROD crate. The TBM also gathers busy signals through the CP3 plane from the eight RODs in a VME crate and provides a busy signal to the ROD Busy module.

### 3.2.4 Tile Muon Digitizer Board crate

The B175 TMDB crate houses the TMDBs which are controlled and monitored through the VME bus by the SBC named sbctil-trg-01. In Point 1, there are 2 TMDB crates, corresponding to the extended and long barrel. The EB crate, contains 16 TMDBs and the LB crate contains 6 TMDBs for reading a small



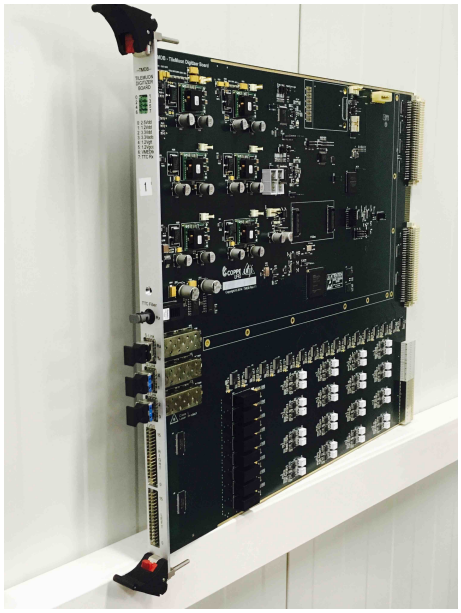

Figure 3.9: TMDB crate housing the 4 TMDBs (2 currently in use), TMDB busy module and a SBC.

fraction of the LB for noise studies. In B175, two TMDBs are installed in the TMDB crate and they are connected to the one super-drawer, the TTC, the ROS and the TMDB busy module.

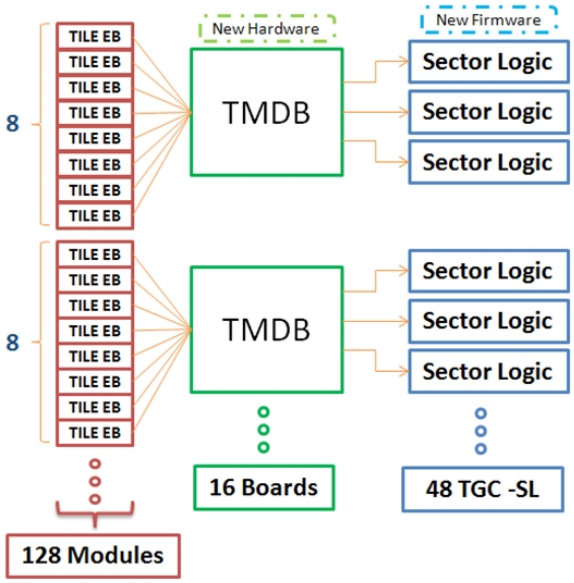
### Tile Muon Digitizer Board module

The TMDB is a ROD that receives, digitizes and transfers the signals to the ROS. The analog signals come from the TileCal D5 and D6 channels of the extended barrel module. The TMDB estimates the energy using the Match Filter approach [46], applies a threshold and the digitized signal is transferred to the Thin Gap Chamber (TGC) Sector-Logic (S-L) Boards, as illustrated in Figure 3.10b. Each TileCal cell in a module consists of a double readout and the TMDB processes 512 signals in total, coming from the D5 and D6 cells. 48 TGC S-L Boards receive the output signals from the TMDB and process the final decision. Based on those requirements, the system was designed with 16 TMDB's (8 per partition) with 32 channels (i.e. 8 TileCal modules) and 3 optical links to interface with the TGC S-L Boards. The TMDB hardware and specifications will be fully discussed in Chapter 5.

On the TGC side, 48 S-L Boards receive the TMDB output signal to process the final decision. Based on those requirements, the system was designed with 16 TMDB's (8 per partition) with 32 channels (i.e. 8 TileCal modules) and 3



(a) A pictorial view of the TMDB.




(b) Schematic view of TMDB to sector logic system architecture [45].

Figure 3.10: In USA15, there are 16 TMDBs installed for EBs and 6 for LBs.

optical links to interface with the TGC S-L Boards. The TMDB hardware and specifications will be fully discussed in Chapter 5.

### Tile Muon Digitizer Board Busy module



Figure 3.11: TMDB busy module

TMDBs are originally designed to send their busy or memory full/nearly full, signals in a Low Voltage Differential Signal (LVDS) format. This format is incompatible with the Transistor-Transistor Logic (TTL) input format that the ROD busy module accepts. The TMDB busy module acts as an interface between the TMDB and the ROD busy module. The TMDB busy module details on the busy module hardware and the busy handling will be fully discussed in Chapter 6.

### 3.2.5 Read Out System

The ROS is a server class PC which accommodates up to 12 Read-Out Buffers (ROB). It receives event data from the RODs through the optical fibre ROLs. Each ROB buffers data from a distinct $\theta$,$\phi$ region at the Level 1 Trigger rate.

### 3.2.6 Calibration System

TileCal construction has been augmented for good energy resolution achieved by the use of highly accurate and precise system calibrations. There is three main tests and calibration systems that work together to provide accurate jet energy measurements. These are the Cesium system, Laser system and CIS. Each system tests a seperate element of the readout electronics chain and the combination of the three provides the overall calibration of each readout channel as shown in Figure 3.3 and Figure 3.12.

#### Cesium

The Cesium calibration consists of circulating sources of $^{137}$Cs isotope that emits 662 keV photons in the detector. These photons interact with the plastic scintillator tiles which then emit photons to the WLS. This allows for the test of stability and uniformity of the optical response of the cells. In a Cesium scan, the radioactive source is circulated around TileCal using a hydraulic system.

#### Laser

The Laser calibration involves sending laser pulses into the base of the PMTs, allowing for calibration with respect to each PMT's response. This allows for the calculation of corrections to the optical gain of the PMT and a test for the stability of each PMT over time.

#### Charge Injection Scan

This calibration system consists of the simulation of physics signals through the injection of known charge values into the readout electronics. This is achieved by using dedicated capacitors (5 pF and 100 pF) plus a 4096 DAC controlled by the ADC. The relation of the peak amplitude in the response of the electronics

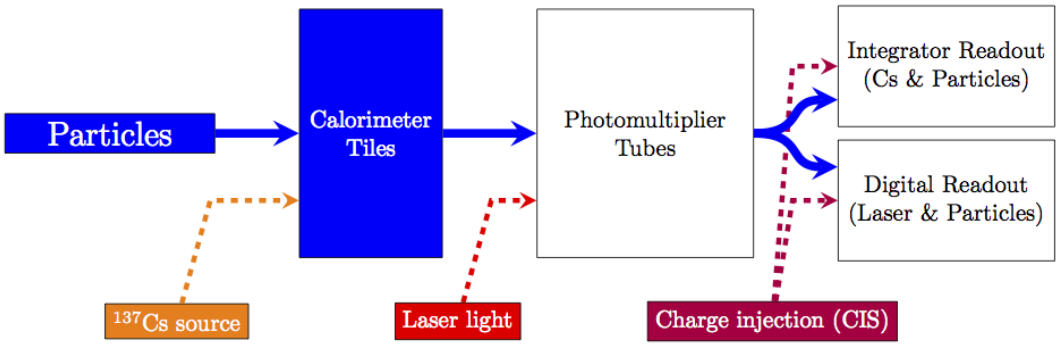



Figure 3.12: Schematic flow diagram of the signal readout chain of different calibration systems in TileCal [47].

(measured in ADC counts) to the value of charge injected (in pC) gives the calibration of each ADC in units of ADC counts/pC. This enables verification and identification of errors with the readout chains and allows for calibration of single ADC outputs of every PMT for every 3-in-1.

### 3.2.7 Detector Control System

The DCS architecture is implemented as a distributed BE system that runs on computer nodes,[2] and various FE systems. The BE software functionality is two-fold such that it requires data from the FE components and offers supervisory control functionality, like data processing and analysis, storage and display. The system also provides handling of alarms, messages and commands. To provide the needed functionality, the BE system of the ATLAS DCS is organized in three layers as depicted in Figure 3.13. The main DCS systems for the TileCal monitor and control the LVPS, the HVPS and the cooling of the electronics. The HV system is needed to operate the PMTs, the low voltage system is required for powering the entire on detector readout electronics and for HV regulation. The cooling system is required to keep all the electronics within the correct temperature range. There are other dedicated control systems specifically for the calibration related systems that are independent of the DCS. They however interface with the TileCal DCS for data and command exchange [48].

[2] A node is a device with an IP address. It has the ability to transmit data along distributed network routes.

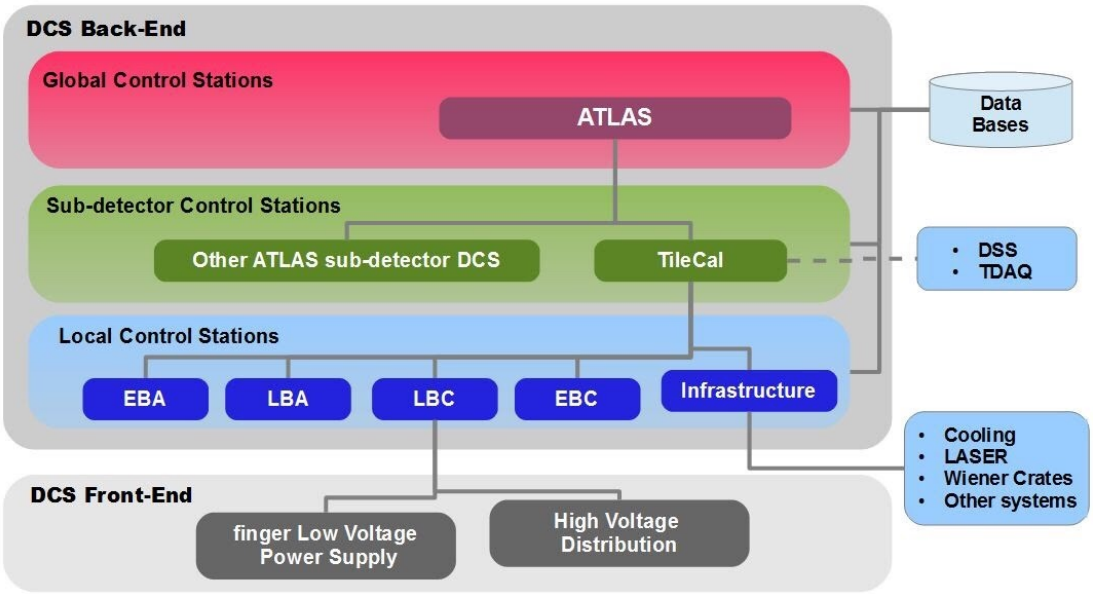



Figure 3.13: Diagrammatic representation of TileCal DCS hierarchal system used in Run 2 [48].

# Chapter 4

# Online Software

Chapter 4 introduces the online software necessary for the implementation of the stopless removal. The Tile online software covers the ROD Crate DAQ, Stopless recovery and DCS-to-DAQ connection. The chapter further discusses the TDAQ software release and its versioning. Lastly, the TDAQ software organisation and build systems are discussed.

The online software, which is part of the TDAQ system, incorporates the software responsible for the configuration, control and monitoring of the TDAQ, with the exclusion of physics data processing and transportation. The online software holds the different sub-systems together and does not have any elements that are specific to the detector as it is to be used by required configurations of the DAQ and the instrumentation of the detector. It co-exists and coordinates with other sub-systems. The online software includes various components, which are basic services needed to run a partition. These components are:

- Configuration databases: Contains all the necessary information for running the DAQ software. The application of the database system is essential in the description of the DAQ system configuration.
- Process Manager (PMG): The PMG is responsible for the execution of applications on the nodes.
- Resource Manager: The Resource Manager is responsible for keeping records of allocated resources. In the configuration database, the utilization of the available hardware and software resources is managed by this service.
- Access Manager (AM): The AM is responsible for access to resources and nodes for a user with authorization, based on the user's expertise and experiment status at a given time.
- Inter Process Communication: The core communication service that relies on the underlaying TCP/IP message passing.
- Information Services (IS): The service that allows sharing of any kind of user defined information between applications.

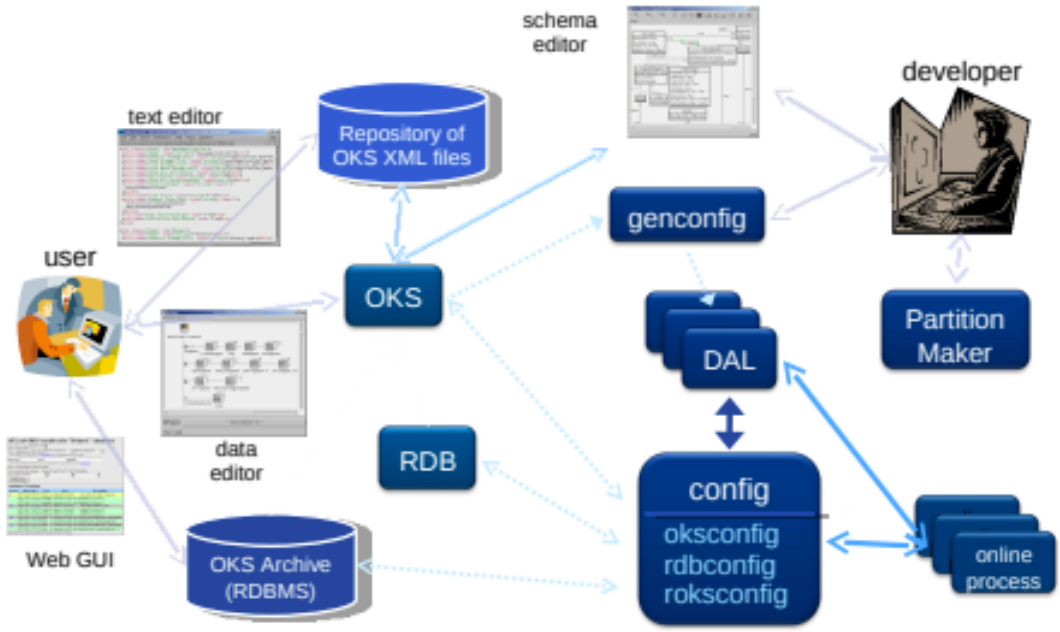



Figure 4.1: A schematic diagram of the Configuration Databases: architecture, management and access [29].

- Run control (RC): The RC is the core Finite State Machine (FSM) service responsible for the structure of controlled applications.
- Monitoring infrastructure: ATLAS online monitoring system which is organized as a distributed framework.
- Integrated Graphical User Interface (IGUI): The friendly user interface with the RC.
- Expert System: The service that supervises the recovery actions.

The Online Software doesn't hold any specific sub-system components, as it is developed as a customizable framework with strong requirements on distribution, robustness, flexibility, scalability and modularity. The TDAQ is defined from the control point of view as a collection of applications running on a set of hosts. It is modelled around a common FSM that specifies a few well defined states and transitions. The FSM conceals the complexity of the individual components. The overall TDAQ status is kept in a coherent state by the RC service which implements a hierarchical tree with a Root Controller acting as the root. The TDAQ is best described by the configuration database service [49].

The configuration database is a service containing the TDAQ system description and detector specific information including software, hardware, partitions and run parameters. This information description is gathered in form of configuration for distinct run types (calibration, physics, debug, etc...). This service is used by

sub-detector experts to develop their own configuration parts and to write the code configuring their applications using common configuration service tools. Its implementation is based on the Object Kernel System (OKS), a persistent in-memory object manager. The primary storage for this OKS is XML files, which consists of two types; the schema files which define classes, and the data files to store database objects.

Well structured XML files can be included in the OKS database, to build a complete database and they can be shared with other OKS databases. The configurations database can be accessed via API provided by the config package based on two layers; the first config layer provides an abstract interface to access configuration schema description objects and to work with databases, and the second Data Access Libraries (DAL) layer uses the above abstract config to instantiate database data as appropriate objects of such classes and to map the database schema on C++, Java and Python classes [49].

## 4.1 Partition

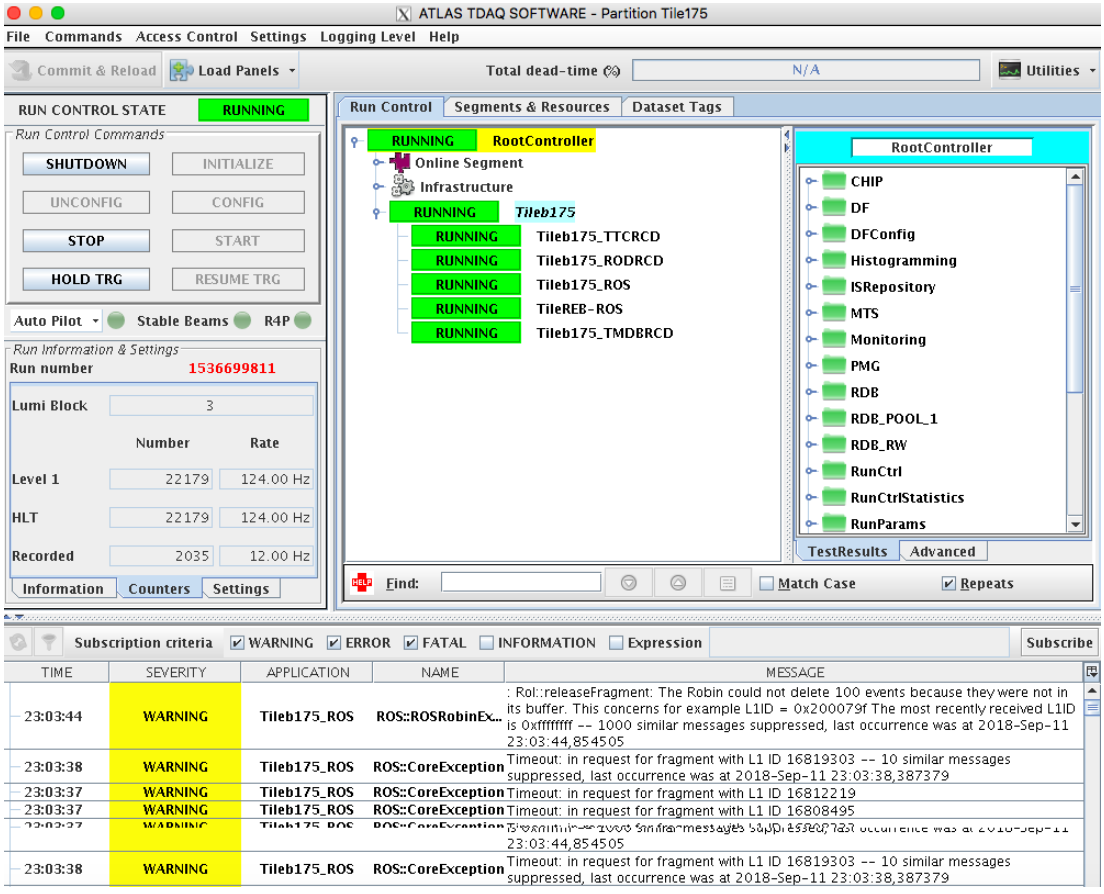



Figure 4.2: A screen shot of the IGUI of the Tile175 partition.

The TDAQ configuration is firstly defined in the partition. In ATLAS, a partition is a synonym for a data taking configuration, it is basically an object of the configuration database from which all the configuration of the hardware and software elements which are included in the readout is spanned. Several partitions can be defined, i.e the Tile partition for TileCal, which is used for taking calibration runs and the ATLAS partition, which groups all sub-systems together. In B175 ROD/TMDB lab, there exists Tile175 partition, which has been tirelessly used throughout this project. Figure 4.2 shows the IGUI of the Tile175 partition with the RC in the RUNNING state. There are several specific functionalities in the TDAQ system, these include the TTC partition, Resources, Segments and the TDAQ partition.

**TTC partition**

A TTC partition consists of a part of the TTC system and an analogous part of the busy feedback chain. A TTC partition corresponds to a single TTCvi module. As outlined in Chapter 3, there are four TTC partitions in the Tile Calorimeter, two in the Long Barrel (LBA and LBC) and one in each Extended Barrel (EBA and EBC). The ATLAS TTC partitions are fully described in [50].

**Resource**

A resource is one of the TDAQ system parts, it can be enabled or disabled (masked) individually, without stopping the data taking process. A ROL in the Tile Calorimeter is an example of a resource.

**Segment**

A segment is interpreted as a set of TDAQ system elements which can be configured and controlled independently from the rest of the TDAQ system. A segment can be included or removed from an active TDAQ partition without stopping the run. Each of the four TTC partitions of the Tile Calorimeter is represented as a TDAQ segment.

**TDAQ partition**

The TDAQ partition is a subset of the TDAQ system, which is responsible for data taking. The full TDAQ functionality is available to a subset of the detector. A TDAQ partition corresponds to one or more TTC partitions.

TDAQ partitions can be operated at the same time, depending on the maximum number of instances allowed for the used resources. Some resources are designed to have a unique instance across all partitions. This is the case of the

detector instrumentation resources. A super-drawer cannot be in two contradictory states of the FSM at the same time. Two super-drawers from two different TTC partitions can be in two contradictory states. There is one TDAQ partition that describes each TTC partition of the Tile Calorimeter in the configuration database. Yet another TDAQ partition includes the four TTC partitions, each one described in a different segment. This way, easy swapping between configurations may be achieved. In ATLAS data-taking, each sub-detector is included into the ATLAS TDAQ partition as a different segment. These top level segments are organized into further segments which describe the different TTC partitions and other overall sub-detector segments, such as monitoring segments.

## 4.2 Tile Online software

The Tile online software is a set of TDAQ software used for the operation of the Tile Calorimeter. It is built up of CMake packages which are stored in Gitlab (atlas-tile-online). The Tile online software is basically an extension of the ATLAS TDAQ software which provides TileCal detector specific software for the BE electronics, infrastructure for calibration systems, monitoring (including hardware), and the diagnostic and verification systems tests (DVS). One of the core components of the TileCal Online Software elements is the BE electronics ROD Crate DAQ (RCD). It is supported by the ATLAS Data Flow policy for which the TileCal Online software provides plug-ins. This keeps the programming efforts focused on specific hardware handling since the core software is centrally managed.

### 4.2.1 ROD Crate DAQ

The RCD framework is an addition of the ROS software that allows an integration of the custom hardware into the general TDAQ software. The RCD is based on a multi-threaded read-out application core, which loads specific plug-ins at runtime, in order to adapt its behaviour to the detector specific needs. There are different plug-ins for different purposes. A schematic overview of the read-out application with its plug-ins, is shown in Figure 4.3. These plug-ins are:

- Configuration plug-in: Loads the information from the configuration database and passes it to the RCD core application.
- Trigger plug-in: Handles the trigger requests for data fragments. It runs as a separate thread that queues requests on a request list. A number of request handlers from the RCD dequeues them by executing the data requests that push the output information to the output plug-in.
- Module plug-in: A controlled resource which receives transition commands from the RCD. In ATLAS operation mode it does not send data out to the output plug-in.

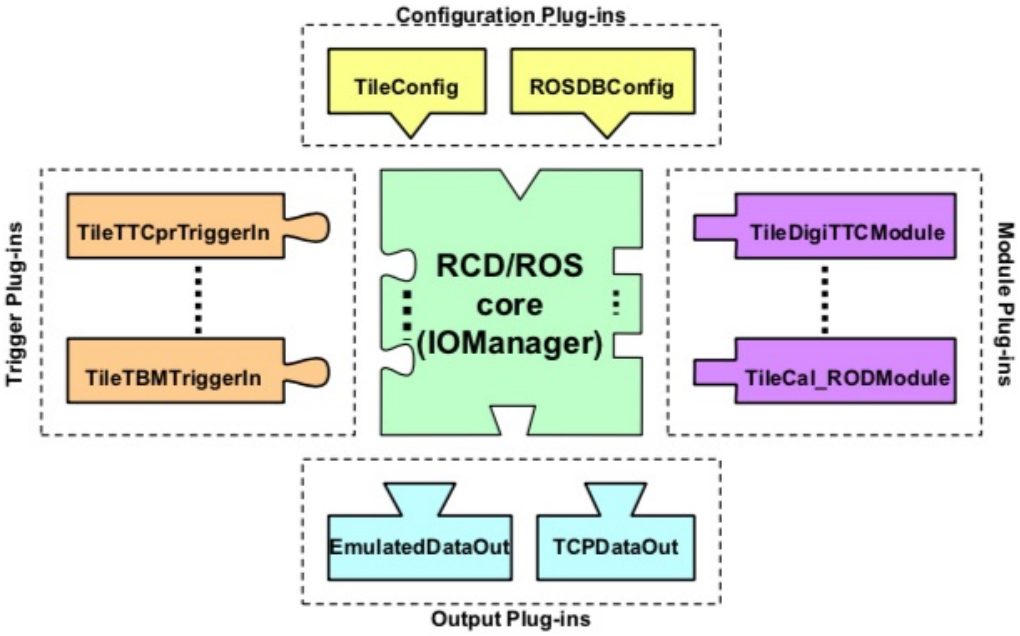



Figure 4.3: A diagrammatic view of the ROD Crate DAQ. The RCD basically handles the BE hardware operation for Tile. There is one RCD application running in each TTC and ROD crate [51].

- Output plug-in: Manages the output of the data which can be sent elsewhere through ethernet or written down to a file.

The RCD application is commanded by the RC service. When a state RC transition command is sent by the user through the IGUI, a request for a state transition is sent to the RCD. The RCD reacts to the request and operates the controlled hardware according to the detector specific code. The configuraton required by the RCD is stored in the configuration database, which is an object oriented database which allows relationships between objects. To add an object in the configuration database, it must belong to a class defined in the schema. The schema allows the mapping of objects in the OKS database and C++ objects in the running software. The base schema is extended to describe the specific Tile Calorimeter classes. All hardware objects are described in the configuration database.

An RCD application is represented in the configuration database by the RCD object. It loads the different plug-ins based on its attributes and relationships. The RCD retrieves the class name of the objects linked to it and dynamically loads the plug-in library with the same name through DAL.

### Configuration

A generic configuration plug-in called ROSDBConfig is available for its use with the RCD. In addition, there is a Tile Calorimeter specific configuration plug-in, TileConfig, exceptionally the TileDigiTTCModule plug-in uses TileConfig to retrieve the configuration of the super-drawers, instead of the generic one. In particular, the trigger and module RCD plugins for the Tile Calorimeter implement mechanisms to retrieve any configuration information using the generic plug-in.

This plug-in retrieves all the attributes from a given object of the database and populates the corresponding keys. It is also possible to retrieve the configuration database pointer from the RCD code; this allows the RCD code to access the configuration database directly. Consequently, any object from the configuration database can be retrieved from the RCD code.

### Trigger

Specific trigger plug-ins are available for both TTC and ROD crates. These make use of sub-detector hardware such as TTCpr and the TBM.

### TileTTCprTriggerIn

The TileTTCprTriggerIn is a trigger plug-in used in calibration runs. It waits for a L1A in the TTCpr input link and reacts to it. The TTCpr buffers the EventID, BCID, and trigger type associated to the L1A. When a L1A is received, the TileTTCprTriggerIn creates a data request and schedules it on the requested data fragments queue. The request handlers in the RCD retrieve the request from the queue and execute it. The executed request builds the data fragment which contains calibration information and pushes it to the data output plug-in. The busy is raised at the first event in and it is removed once the data has been moved out from the request queue.

The ROD busy module retrieves the busy status of the TTCpr, publishes it to the IS and it is displayed in the Crate panel of the Tile Calorimeter specific IGUI panel, as shown in Figure 4.4.

### TileTBMTriggerIn

As discussed in Chapter 3, section 3.2.3, the TBM distributes TTC signals through the VME backplane of the crate and handles the busy from the eight RODs. The TBM trigger plug-in is a trigger plug-in to the RCD that does not queue data requests. It gathers the active RODs for the run at configuration time and configures the busy mask accordingly. On every probe command, every 5 s, the busy information is published into the IS and displayed as the colour of each ROD in the Crate panel of the Tile Calorimeter specific IGUI panel, as shown in Figure 4.4.

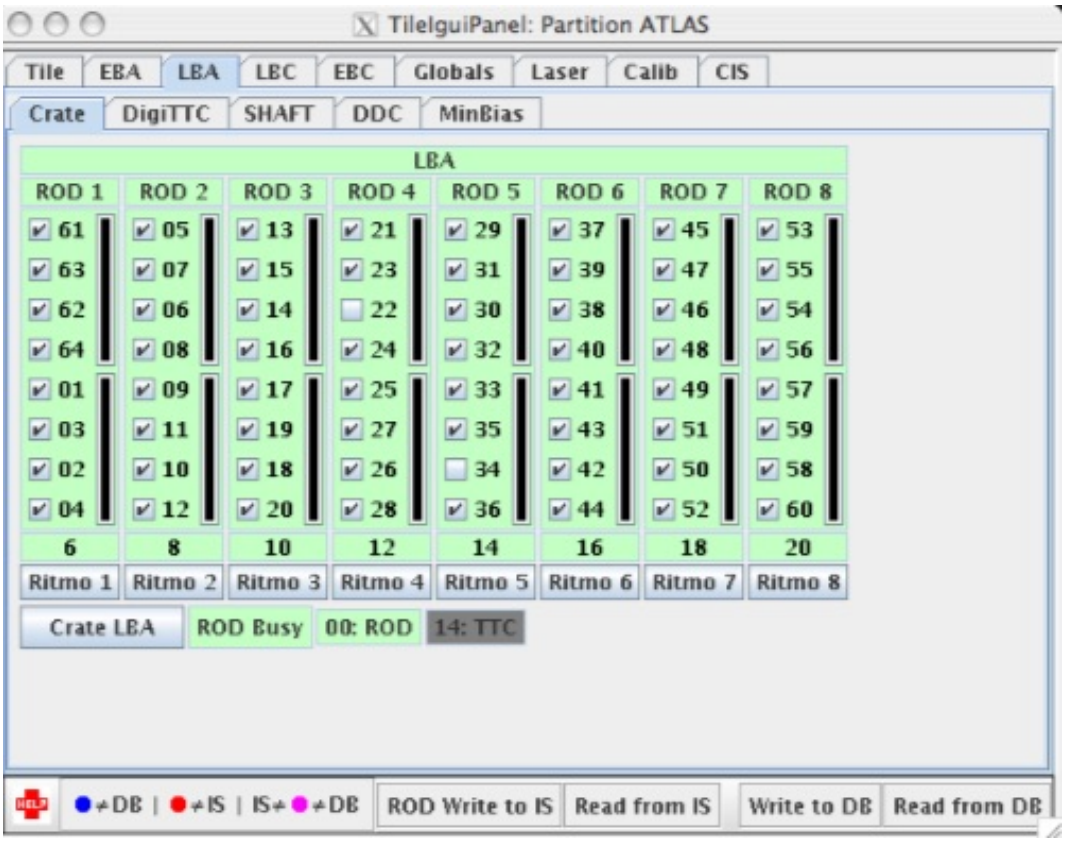



Figure 4.4: Crate sub-panel in the Tile IGUI panel.

### Modules

A module plug-in describes a hardware or software component that is controlled by the RCD. It can extend any of the methods of the ReadoutModule class which represent a RC transition command. The RCD module plug-in can be used in ROD emulation or ROD hardware manipulation. TileCal specific module plug-ins for their use in the RCD framework are TileDigiTTCModule, TileVMEReadoutModule, TileCal RODModule, TileOfcShameModule, TileShaftModule and TileLaserModule.

### TileDigiTTCModule

The TileDigiTTCModule is a double purpose module. It controls the FE electronics through 3-in-1 TTC commands and the BE electronics needed for TTC. It is the steering wheel of the calibration run. It provides the charge injection settings to the FE and, coupled with the TileVMEReadoutModule, provides data fragments containing the same settings to the data flow. The configuration of the TileDigiTTCModule may be done through the TTC sub-panel of the Tile IGUI panel, as seen in Figure 4.4.

### TileVMEReadoutModule

The TileVMEReadoutModule is a general purpose module. In calibration runs it is configured to read-out data from the shared memory region of the crate controller and provide data fragments to the output plug-in.

### TileCal RODModule

The TileCal RODModule controls the ROD motherboard. It configures the motherboard and the processing units according to the run type. For physics runs, ROD is configured as a dataflow element between the FE electronics and the read-out system. It takes data in from the FE links and sends data out through the Read-out Links. Monitoring quantities computed inside the boards are accessed from the SBC and made available to the TDAQ monitoring service.

Eight instances of the TileCal RODModule are needed by the RCD application in the ROD crate. Each one controls a different motherboard independently. Masking of individual input links to the motherboard may be done through the Crate panel of the Tile Calorimeter specific IGUI panel, as shown in Figure 4.4. The online processing algorithm may be configured through the Globals sub-panel of the Tile IGUI panel, shown in Figure 4.4. The conditions settings are retrieved accordingly at configuration time, in the "prepare-for-run" transition, from the shared memory region of the crate controller.

### TileOfcShameModule

The TileOfcShameModule is a module plug-in that doesn't control any hardware module. It is used as the conditions data cache for the whole crate. In order to avoid eight connections to the conditions database, one per ROD module, this module is used to gather conditions settings and store it in the shared memory region of the crate controller. In order to avoid unnecessary time consumption, this module checks the input link status of the RODs. If an input link is set to be masked, the corresponding conditions data will not be retrieved for it. The same will occur for pedestal calibration runs, where conditions settings are not necessary.

### TileShaftModule

The TileShaftModule is a module plug-in to control the Shaft board, which is a specific VME board to share the calibration requests in empty bunches, as mentioned above. This module controls the different calibration trigger requests foreseen in the Tile Calorimeter. Each calibration request can be enabled and its firing timed with respect to the TTC signal that clocks the turn of the LHC beam. There is one shaft board per partition. The information about the calibration

requests is placed in IS for the Laser ROD to retrieve. The configuration of the Shaft board may be done through the Shaft sub-panel of the Tile IGUI panel.

#### TileLaserModule

The TileLaserModule is a module plug-in that controls the Laser ROD. This is a ROD which does not read-out data from the FE but from the BE. It is used in physics runs to insert calibration information into the data-flow. Its read-out link is connected to the LBC partition read-out system. It receives TTC information from the shafts and the calibration information of the current event is read-out from IS. The Laser calibration system provides a Laser pulse to all the PMTs. The intensity of the pulse can be regulated via a digital to analog converter and an attenuation filter which is placed in front of the source. The response of the detector PMTs is compared to the response of an internal PMT of the system. This PMT is calibrated via an internal $\alpha$-source run. The configuration of the Laser run parameters can be done through the Laser panel in the Tile specific IGUI panel.

### 4.2.2 Stopless recovery

The stopless recovery mechanism is the automatic procedure through which a hardware resource, responsible for raising the busy signal for a fixed amount of time is disabled and possibly re-enabled without stopping the data-taking process. The stopless recovery is supervised by the expert system. Since 2008, the ROD has been the only element to raise the busy signal, within the busy chain of the ATLAS detector. The TMDB was commissioned in 2015 under the TileCal detector and it became the second element to raise the busy signal during data-taking.

#### Stopless Removal

On each RCD probe, approximately every 5 s, each ROD performs a check to see whether there is any busy. If there is a busy inside a PU that lasted 100% of the time, a hardware failure message is issued on a ROL. The expert system reacts on this message and suggests that RC removes the faulty hardware. If RC accepts the removal, ROD and ROS are notified and the hardware is disabled. The TMDB stopless removal follows a similar procedure, it is implemented differently based on the design of the hardware and firmware by the author.

#### Recovery After Removal

Once the faulty hardware has been removed, there is a RC command that can be issued to re-synchronize the hardware. The recovered hardware issues a message that is processed by the expert system and the hardware at both sides of the ROL is reset and enabled back.

### 4.2.3 DCS-to-DAQ connection

The DCS-to-DAQ Connection (DDC) is the connection between the DAQ and the DCS, where messages and information are exchanged both ways. The exchange of information during the run, provides better understanding of each system when looking at only one source of data, either DAQ or DCS. On the DAQ side, the DDC system is made up of three components, the DDC controller, message transfer application, and the data transfer application. The DDC controller launches a DCS action defined for a TDAQ RC transition in DDC configuration. The message transfer application, passes text messages (defined in configuration) to TDAQ via ERS. The data transfer application, passes data from DCS to IS and from IS to DCS as defined in configuration.The DDC controller is defined together with the message transfer application for every TTC partition of a sub-detector and the data transfer application is optional.

## 4.3 TDAQ Software release and versioning

TileCal employs software that is grouped together as packages in the TileCal Online software release for its operation. The software is distributed in releases. The release follows the ATLAS TDAQ software policies and release, meaning that it is updated simultaneously following ATLAS TDAQ updates and policies. It is built up of CMake packages which are stored in a Gitlab repository (https://gitlab.cern.ch/atlas-tile-online). The list of packages included in the release is referenced by a packages.txt file inside the release build area. For every new release built, the packages are checked out into an Andrew File System (AFS) account and compiled at once.

All packages that are ready for a new release build are, and should always be tagged using the Git so-called annotated lightweight version tags which require a specific message. Such tags are never deleted once pushed to the Gitlab remote repository. The tags follow the guideline of 3 groups of letters and digits specifying the major, minor and patch version, e.g. v2r1p0. The latest tag for every package is used for building the release. The versioning of the TileCal Online release (tile-X.Y.Z.U) follows the TDAQ versioning (tdaq- X-Y-Z) adding additional enumeration for the number of times the release has been rebuilt due to updates. External software is used by the TileCal Online release. This includes offline TileCalibBlobObjs (used to access the information stored in COOL DB) and other specific software which resides in offline SVN/Git repository [52]. The TileCalibBlobObjs remains the only offline package used by the online software, and it is now however compiled together with the other online packages as a TDAQ package.

After the compilation process, the binaries are transferred to Point 1 and in-

stalled in the detector area. No write permissions are given to the release files once installed. In fact, a patches folder is provided for a given release with full access for developers to test their code. If a specific patch has to be applied to the release, it has to be copied from the patches to the installed directory.

ATLAS has been utilizing Apache Sub-version (SVN) for software conversioning and revision control. The software revision control,[1] is to be upgraded to Git, in preparation for Run 3. Git is already being utilized in most of the sub-detectors alongside SVN. Git is a modern distributed version control system, it is widely adopted in open source community and allows a more decentralized approach to software version control. Git is fully supported by CERN as the recommended VCS tool for all software projects, and this has rendered migration from SVN to git almost inevitable as a non-git solution would require dedicated ATLAS support. Although git is a fully distributed service, the Gitlab server plays a similar role to the Subversion server: it contains the official version of the code and this is employed in building releases. In the following section, the TDAQ software is described according to its organization and build systems.

## 4.4 TDAQ software organization and build systems

The TDAQ software is organized in three projects: the tdaq-common, dqm-common and tdaq. It provides access to a large number of external software packages, that are maintained by the SFT (SoFTware Development for Experiments) group at CERN, and this is shared with offline and other experiments. Figure 4.5 shows a diagramatic representation of the hierarchy in the sub-detector software project and Figure 4.6 shows the list of TileCal Online software release packages with their dependencies.

- tdaq-common: This is the most basic project used by both TDAQ and offline software. Examples of the packages that it contains are the raw event format and storage, and the ERS. All other TDAQ projects are built against this project.
- dqm-common: This projects contains packages that are used for data quality monitoring (DQM) for both TDAQ and offline DQM. It is built against the tdaq-common project.
- tdaq: This is the TDAQ projects itself and contains all the rest of the packages used by sub-detectors and the HLT. This project is built against both the tdaq-common and dqm-common projects. TileCal Online software is compiled against this TDAQ project.

[1] A part of software responsible for recording different versions of code in a persistent and recoverable way.

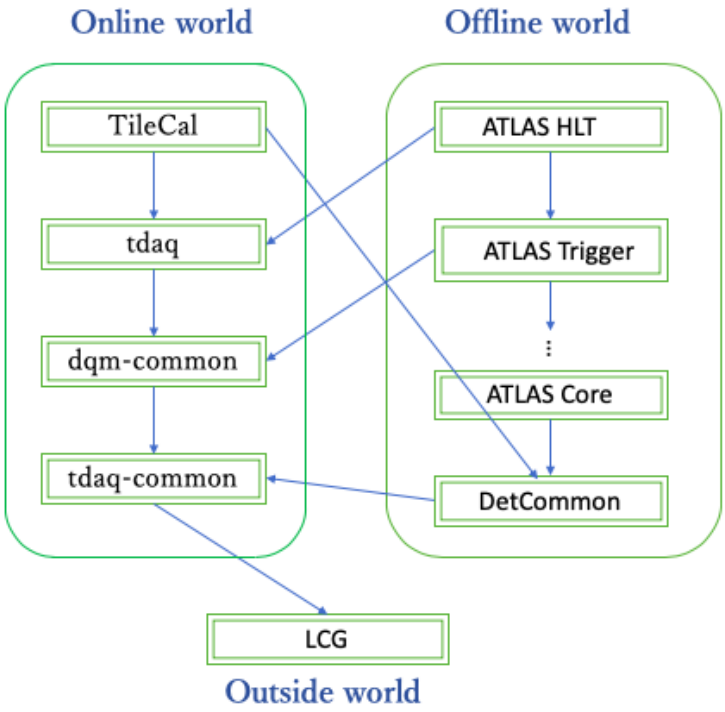



Figure 4.5: A diagrammatic representation of the organization of TDAQ software. TileCal and other sub-detector software projects are built against the tdaq project, which is built against the dqm-common and tdaq-common projects.

The TDAQ software (same as offline software) has for many years depended on the CMT[2] build system. However, the ATLAS code base has now evolved beyond CMT capabilities and this has resulted in replacing CMT with CMake in favour of modern software development tools and procedures.

The TDAQ software has been migrated, and now uses the CMake tool to build, test and package software. TDAQ software is built and distributed as packages. A Package is the smallest manageable unit of a software. It is the primary development unit and can have dependencies against other packages. TDAQ provides several CMake specific commands to replace CMT. TileCal Online software has also been migrated and rebuilt with CMake following TDAQ. The migration to CMake has provided greater similarity and better integration between the offline and online worlds as seen in Figure 4.5. CMake was developed to build, test and package software by Kitware Inc. CMake is used for controlling software compilation processes, making use of simple platform and compiler independent

[2]It is a configuration management environment based on some management conventions and comprises several shell-based utilities. It was developed as an open-source academic project aimed at providing support to software developments in the context of large physics experiments by LAL (Laboratoire de l'Acc'lerateur Lin'eaire - CNRS)

configuration files [53]. CMake is very much similar to CMT but provides better performance, maintainability and multi-platform support. One of the reasons for the migration was the maintenance of CMT by itself, which was at an end of life stage while CMake is community developed and supported

Several programming languages are employed in the TileCal Online software. C++ is the main programming language for TDAQ software with a share of 97%, almost all services and libraries are used from C++. Java is used for the IGUI that controls the TDAQ sessions, it is 2.3% of the Tile Online software. Java is also used for various web based services on the BE side and most interfaces make use of Java. Python is the preferred scripting language and most services have a Python binding for ease of use and quick solution implementations. Python is used when speed is not of utmost importance. The officially supported architecture is 64 Bit, the operating system is SLC and the compiler is GCC.

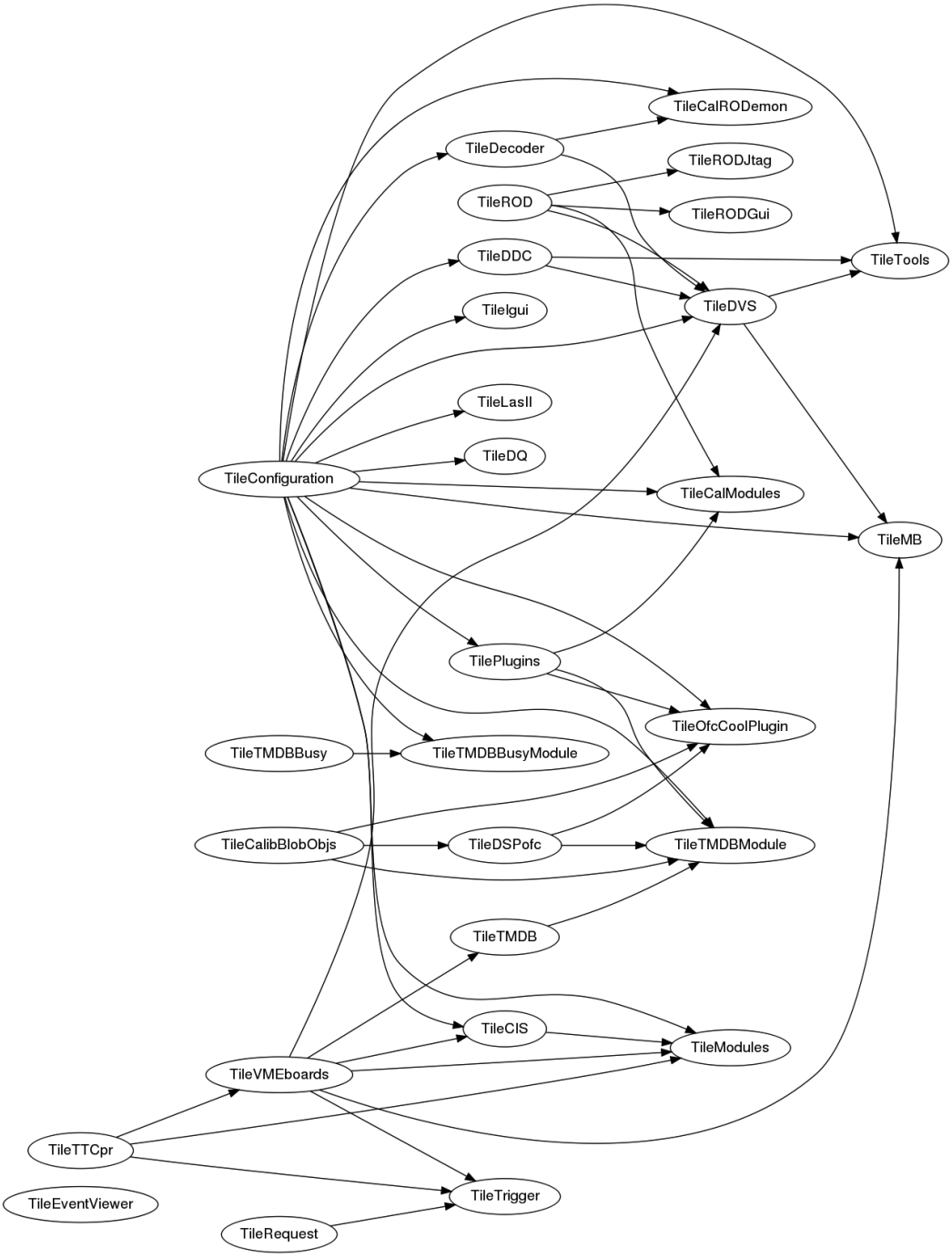



Figure 4.6: A diagrammatic representation of the currently available packages in the TileCal Online software release. There are twenty nine packages and most of them are dependent on the TileConfiguration package.

# Chapter 5

# The Level-1 Tile-Muon Trigger system

Chapter 5 discusses the muon trigger detectors and the Level-1 Tile-Muon Trigger system. The chapter describes the Tile Muon Digitizer Board working principle and its implementation on the Level-1 trigger system.

## 5.1 Motivation of the Level-1 Tile-Muon Trigger project

The LVL1 muon endcap trigger currently in use, is based on the Thin Gap Chambers (TGCs) of the middle endcap stations. These middle endcap stations are referred to as the Big Wheel (BW), i.e. the BW-TGCs, which are covering a pseudo-rapidity ($\eta$) range of $1.0 < |\eta| < 2.4$. Over the Phase-I,[1] (2019-2020) upgrade, muon chambers located at the endcap inner station, called the muon Small Wheel, will be replaced by new chambers, sTGC and MicroMegas detectors with high-rate tolerance and improved resolution [54]. Together, these are referred to as the New Small Wheel (NSW). The NSW has the coverage $1.3 < |\eta| < 2.7$, as shown in Figure 5.1. New chambers were designed to improve the muon tracking performance and also improve the rejection of fake muons in the LVL1 muon trigger by integrating the track-vector data from the NSW. To further improve the rejection of fake triggers in the full $\eta$ coverage of the current BW-TGC, hit information of the End-cap Inner Large (EIL4) TGC chambers and energy-loss in the Tile-calorimeter D-layer cells (D5, D6) in the range $1.0 < |\eta| < 1.3$ will be used (see Figure 5.1). In the absence of the proposed improvements, the trigger rate above a $p_T$ threshold of 20 GeV would be 51 kHz, whereas the introduction of information from the EIL4-TGC and Tile calorimeter D-layer cells in Long Shutdown 1 was expected to lower the rate to 32 kHz. Additional rate reduction to

[1] Refers to the LHC machine and detector upgrades anticipated to be completed by 2020

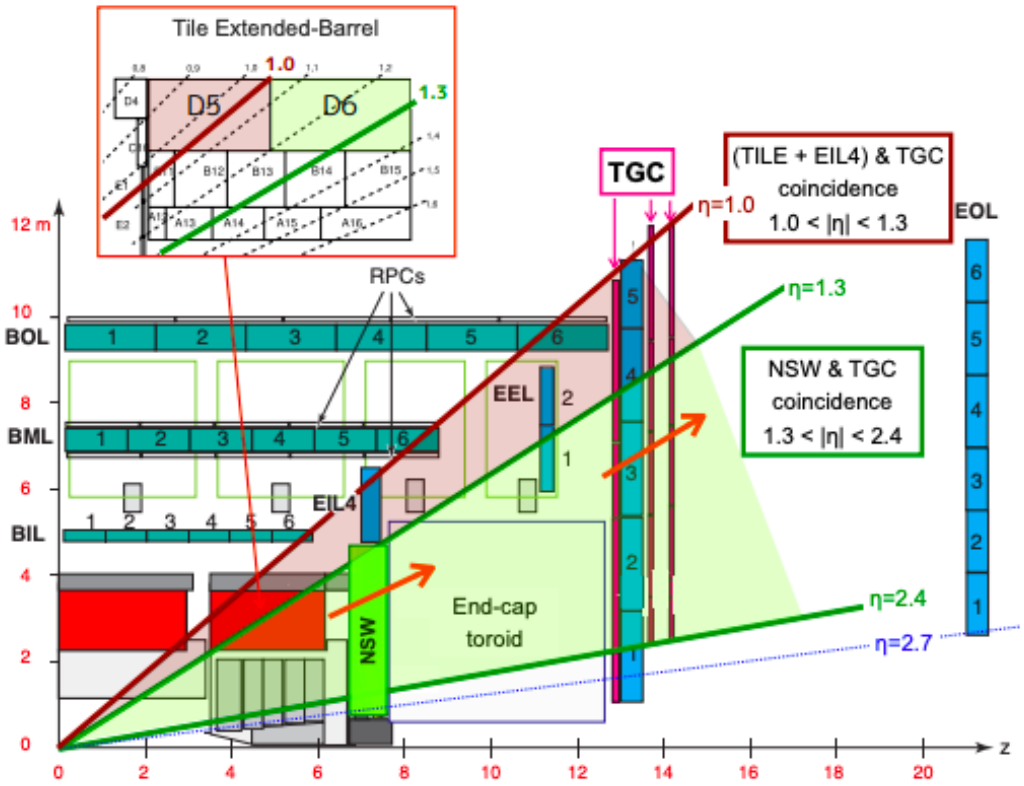



Figure 5.1: A diagrammatic representation for half of the detector, illustrating the coincidence between TileCal D5 and D6 cells of the extended barrel and the endcap muon chamber [54].

15 kHz will be achieved in Phase-I, where the NSW is introduced into the LVL1 muon trigger logic. Reducing the fake LVL1 muon rate will allow to keep a low $p_T$ trigger threshold for single muons at 20 GeV, thus maintaining the physics acceptance of the ATLAS experiment [54].

### 5.1.1 Level-1 Muon Trigger system

#### Level-1 Muon Endcap Trigger

The track vector data from the NSW is merged with the results obtained from the current LVL1 muon trigger (based on the BW-TGC [50]) at the new S-L board. Figure 5.2 gives an outline of the LVL1 muon endcap trigger system. The diagram inside the dotted blue box represents the part of the current trigger system which is based on the BW-TGC. It will continuously be used after the Phase-I upgrade without any changes. The BW-TGC covers the range $1.0 < |\eta| < 2.4$ and consists of three stations, the TGC1, TGC2 and TGC3. The TGC1 station consists of three layers and the outer two stations (TGC2 and TGC3) consist of two layers

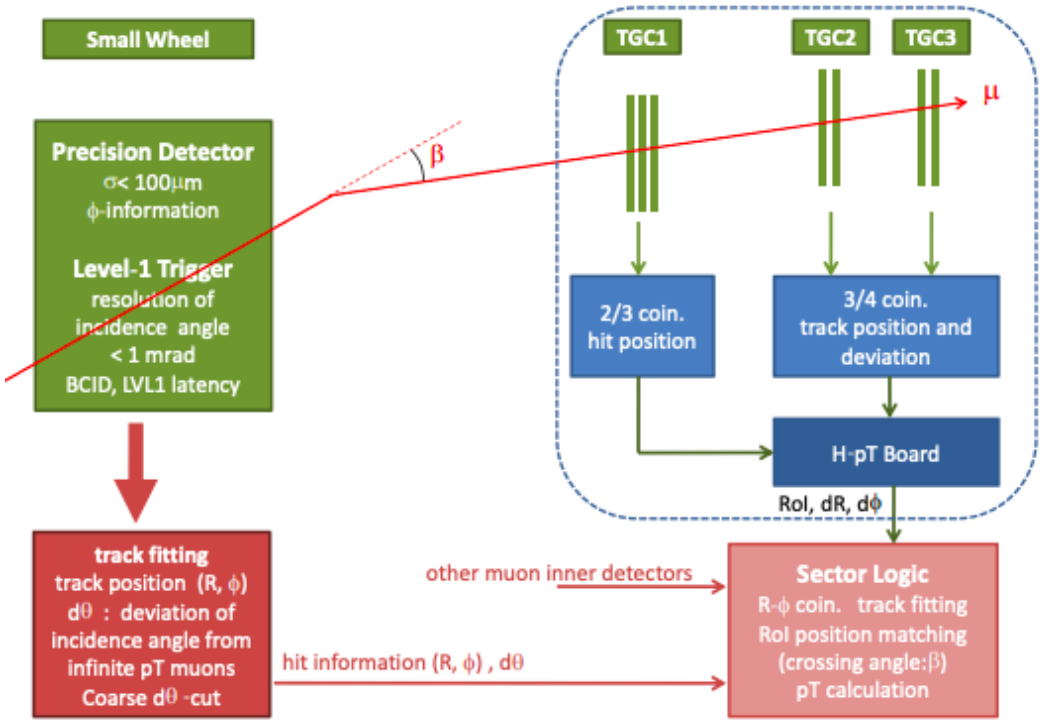



Figure 5.2: An outline of the LVL1 muon endcap trigger [55].

each. This makes it seven layers in total. The TGC3 is referred to as the pivot plane and the trigger algorithm extrapolates pivot plane hits to the IP, in order to construct roads following the infinite-momentum (straight) path for a track. The deviations $\delta R$ and $\delta\phi$ from the track position ($R$, $\phi$) of hits in the trigger planes are related to the momentum of the track [56]. Coincidence signals are independently generated for $R$ and $\phi$ [9]. The information from the hit position, together with the granularity of ROIs and deviations, is sent to the S-L board located in USA15. The NSW consists of two detector technologies, the sTGC and the MicroMegas. Both detectors measure the positions and incidence angles of muon tracks. Information on the candidate muon tracks, which are pointing to the IP within $\pm$ 15 mrad deviations, is provided to the Endcap S-L. This information consists of the track position and $\delta\theta$, which is the deviation of the incidence angle from a straight line to the IP. The final trigger decision is done by merging the $R$ - $\phi$ coincidence of signals from the BW-TGC and the information from the NSW.

Shown in Figure 5.3 is the pivot plane formed by the TGC doublet plane (TGC3) furthest from the IP. Two regions, the Endcap ($|\eta| < 1.9$) and the Forward ($|\eta| > 1.9$), make up the pivot plane. The Endcap region is separated into 48 trigger sectors in $\phi$, where a trigger sector is a logical unit with independent

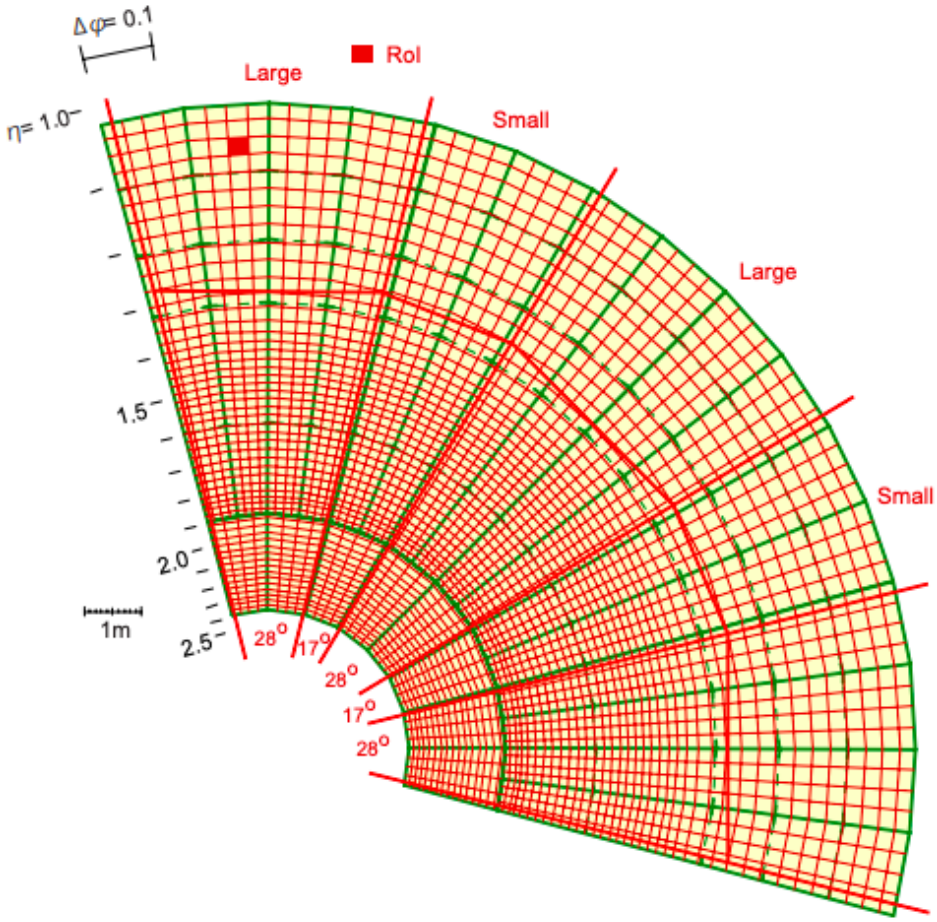



Figure 5.3: A schematic diagram of the Trigger Sector Segmentation and mapping [55].

treatment in the trigger. The Forward region is also divided into 24 trigger sectors. The segmentation of trigger sectors projectively corresponds to the layout of the TGCs in the Big Wheels. The red lines in Figure 5.3 show projective boundaries on the NSW detector, which covers $1.3 < |\eta| < 2.4$ and whose structure has octant symmetry. Each octant has a Large NSW sector and a Small NSW sector. The boundaries of the NSW do not coincide with the segmentation of the trigger sectors. The segmentation of the trigger sectors and granularity of the RoI (indicated by a red box labelled RoI in Figure 5.3) for the Phase-I upgrade still remain similar to the ones of the present system. The sizes of the RoIs are approximately $0.025 \times 0.030$ in $\eta$ - $\phi$. Two types of S-L boards have been developed and these are, the "Endcap S-L" board and the "Forward S-L board for the endcap and forward regions respectively. A single S-L board serves two adjacent trigger sectors, therefore 24 Endcap and 12 Forward S-L boards per side are required.

### Level-1 Muon Barrel Trigger

The ATLAS LVL1 Muon Barrel Trigger is one of the important elements in the early stage of event selection of the ATLAS experiment. During LS1, the LVL1 muon barrel trigger coverage was extended by about 3% in the toroid feet and elevator regions through the addition of RPC chambers. In LS2, the upgrade of the inputs to the Muon-to-Central-Trigger-Processor Interface (MUCTPI) from electrical to optical will need to be matched by the upgrade of the electronics boards used to send trigger data from the muon barrel trigger to the MUCTPI. Sectors 12, 13 and 14 of the barrel spectrometer have a trigger coverage about 20% lower compared to the other sectors as there are no RPC trigger detectors in the areas occupied by the toroid feet support structure (sectors 12 and 14) and by the elevator shaft (sector 13). The trigger coverage increased after LS1 with the installation of new RPCs outside the toroid feet support and the elevator structures, placed in the projective area of the trigger holes. The new trigger towers were integrated in the barrel LVL1 system and read out by the same S-L boards used for the feet and the elevator sectors before LS1.

The barrel LVL1 muon trigger system uses programmable coincidences of three concentric layers of RPC detectors to detect the muons generated at the collision point [57]. The on-detector LVL1 trigger electronics receives the RPC FE signals and executes the trigger coincidence algorithm, while the S-L boards, located in USA15, collect the trigger results coming from the on-detector electronics related to the same trigger sector.

### Level-1 Tile Muon Trigger

The Tile-Muon trigger system is part of the LVL1 trigger system and is used for the detection of interesting muon events using the outermost radial layers (D5 and D6 cells) of the TileCal extended barrels [1]. The Tile-Muon trigger project will reduce the fake muon triggers by using the coincidence between the TileCal D5 and D6 cells and the endcap muon chambers. The muon trigger rates are reduced whilst maintaining good muon efficiency of about 98%.

The main source of the trigger background in the LVL1 muon endcap region are protons with low-momentum. These protons emerge from the toroid magnets of the endcap and the beam shielding in the forward region [2]. The low-momentum protons produce correlated hits leading to coincidences in the trigger muon chambers up to the highest transverse momentum muon threshold. Figure 5.4 shows the distribution of LVL1 trigger muons as a function of $\eta$ above an online $p_T$ threshold of 20 GeV.

To improve the rejection of fake triggers in the range of $1.0 < |\eta| < 1.3$, i.e. the region of the Big Wheel-Thin Gap Chamber (BW-TGC) not covered by the NSW, as seen in Figure 5.1, energy-loss in the outermost layer of the Tile hadronic

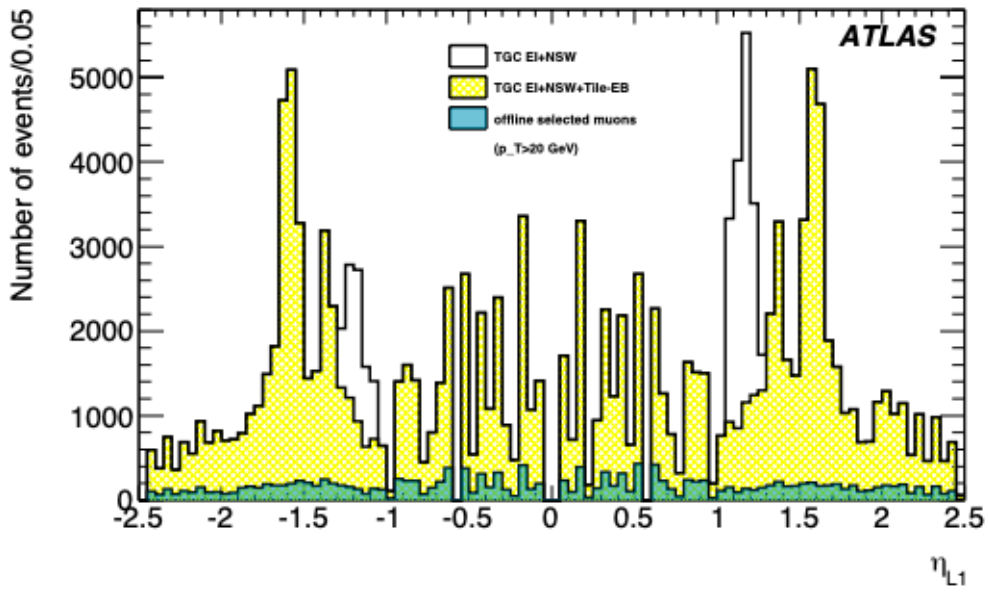
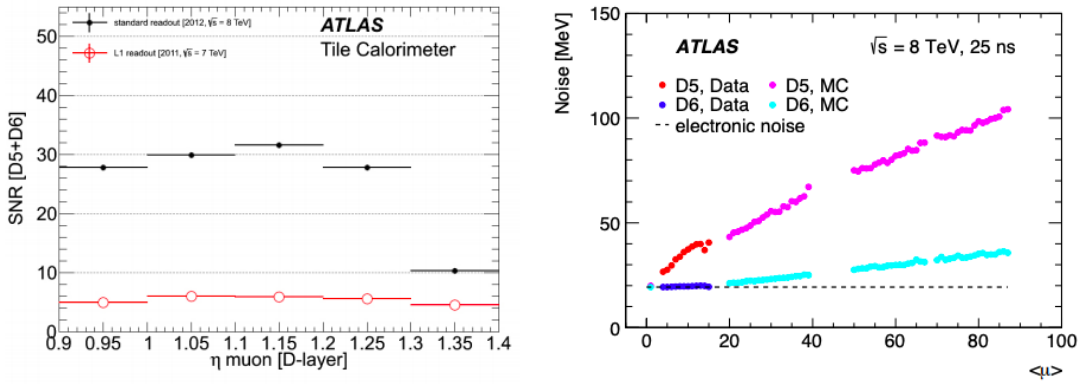



Figure 5.4: Distribution of LVL1 trigger muons as a function of $\eta$ and for a $p_T$ threshold of 20 GeV. The NSW is included in the combined yellow and white distribution, for the LVL1 muon endcap decision. The stand-alone distribution in yellow, displays the outcome of incorporating the TileCal extended barrel D5 and D6 cells, in the LVL1 muon endcap decision. The green distribution displays the muons reconstructed offline with a $p_T > 25\,\text{GeV}$ cut [55].

calorimeter extended barrel (D-layer cells D5 and D6) will be used in combination with the BW-TGC [2, 55]. The NSW is a set of precision tracking detectors that are fast, capable of performing bunch crossing identification at rates up to 15 kHz/cm$^2$ and have spatial resolution of less than 100 $\mu$m per detection plane. The NSW detectors can therefore provide the muon trigger system with re-constructed track segments of good angular resolution (<1 mrad). The re-constructed track segments can clearly indicate the origin of the triggered muons in the range of 1.3 $< |\eta| <$ 2.4 [55].

The TMDB digitizes the analogue muon trigger output from the D5 and D6 cells shown in Figure 5.1. The TMDB is also a ROD that sends outputs to the ROS, just like most RODs and it provides a busy signal to regulate the trigger rate due to bandwidth limitations [1]. The author was responsible for setting up the test bench in B175 and the programming of the busy module hardware, in order to conduct software upgrades.



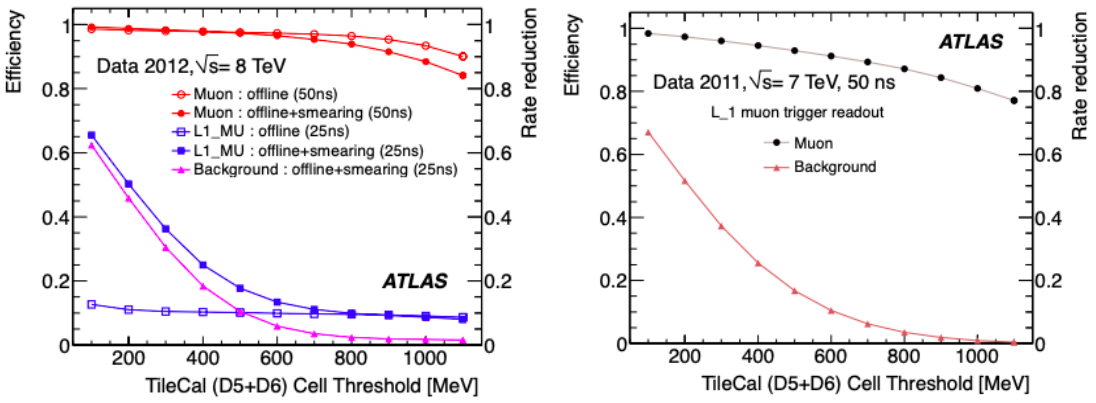

(a) (b)

Figure 5.5: (a) Graphical representation of the Signal-to-Noise ratios of D5 and D6 muon signals, as a function of the muon track $\eta$. The SNR values were measured during the 2011 operation for both, the standard read-out path shown in black circles and the LVL1 read-out path shown in red circles. (b) Noise in D5 and D6 cells against $\mu$ with the standard read-out path [58].

### 5.1.2 Hadronic TileCal Muon identification

There are two read-out paths for the TileCal signals, one responsible for transmitting the trigger tower energy signals to the LVL1 trigger and the other being the standard ATLAS read-out path, via read-out drivers to the DAQ system. A prototype LVL1 trigger receiver module for the TileCal D-layer muon signals was developed [58] and used to receive data for a small number of D-layer trigger cells during ATLAS running in 2010 and 2011.
The 2010 and 2011 data was used to establish the signal-to-noise ratio (SNR) between the most probable value of the estimated energy distribution of the muon signals and noise. This is defined as the RMS of energy depositions in cells, using zero-bias data samples. Figure 5.5a shows the measured SNR values in cells D5+D6 as a function of the $\eta$ position of the muons. The variation in the SNR value is due to the different path lengths of muons through these cells (see Figure 5.1). For the LVL1 read-out path, SNR values of $\approx 6$ have been measured in the $\eta$ range of interest. The electronic noise of this read-out path is measured to be $\approx$ 200 MeV and is the largest contribution to the RMS. Also shown in Figure 5.5a is the SNR obtained by using the standard ATLAS read-out path for analogue signals digitized on the detector. SNR values of $\approx 30$ have been measured with a total noise of $\approx 45$ MeV at a $\mu$ of 20.
Figure 5.5b shows the measured noise in the standard read-out path, in cells D5 and D6 up to a $\mu$ value of 20 using 2012 data. Also shown are the noise values obtained from simulation for larger values of $\mu$. It can be seen that the expected contribution of pile-up to the noise at a $\mu$ value of 80 is $\approx 105$ MeV.

### 5.1.3 Muon efficiency and fake rate reduction




(a) (b)

Figure 5.6: (a) Muon detection efficiency and L1_MU20 rate reduction as a function of the TileCal (D5+D6) cell summed up energy threshold. The rate reduction is also represented and it is the probability that in each bunch crossing the energy summation deposited in the D5 and D6 cells, will be above the threshold, in the absence of offline combined muon. The standard offline read-out data was used to obtain the results. The introduction of 200 MeV smearing was carried out in each cell's response, to simulate the noise in the electronics of the LVL1 read-out. (b) Muon detection efficiency and background reduction with the use of a prototype receiver module, which is coupled to the trigger electronics of the LVL1 calorimeter . In 2012 data, 50 ns bunch spacing runs were used for the accumulation of good muon tracks and 25 ns bunch spacing runs were used in the calculation of the fake trigger rate [59].

Each extended barrel in TileCal consists of 64 modules in $\phi$, while the LVL1 muon trigger, located in the endcap region is split up into 48 trigger sectors. For a signal in a muon trigger sector, it is expected to have a high-$p_T$ muon to traverse one of the two TileCal modules in front of the LVL1 muon endcap trigger sector. In the region $1.0 < |\eta| < 1.3$, an analysis was carried out with data taken during 2012, requiring that for each L1_MU20 at least one of the modules, mapped in $\phi$ to the associated trigger sector, an energy summation deposit in the D5 and D6 cells that is greater than a pre-set energy threshold.

Figure 5.6a shows a comparison of the reconstruction efficiency for combined muons, with an offline $p_T > 25\,\text{GeV}$ (open red circles), and for events triggered by L1_MU20 (open blue squares), as a function of the TileCal cell energy threshold. In this analysis, the analogue signals are digitized on the FE electronics. To emulate the energy resolution measured in the LVL1 trigger read-out path, the

energy of each D5 and D6 cell has been smeared by 200 MeV (1 $\sigma$). The efficiencies obtained with this correction to the data are shown by the full red circles in Figure 5.6a. Smearing reduces the muon efficiency above a threshold of 500 MeV, and the rejection power below a similar threshold (full blue squares). For a TileCal cell energy threshold of 500 MeV, the efficiency for signal muons is 97%, while the L1_MU20 trigger rate is reduced by 82%. In the same figure is shown (by the solid triangles) the probability that the combined energy deposited in the D5 and D6 cells is above threshold when there is no (offline) combined muon. These studies assume that unambiguous bunch crossing identification and energy calibration will be performed in the digital filter before summation, similarly to that performed in the LVL1 calorimeter trigger.

Additional studies have been performed that measure the muon efficiency, using the prototype receiver module used for data-taking in 2010-2011, and connecting the TileCal D-layer signals to the LVL1 calorimeter trigger [46]. In this case, the real D-layer cell noise of $\approx$ 200 MeV was used. As shown in Figure 5.6b, using the D5+D6 cell information and a 500 MeV threshold cut, a detection efficiency of 93% is attained. For the same energy threshold, this analysis confirms the 17% of fake muons found by the LVL1 muon endcap trigger. The computed efficiency is less than the one presented in Figure 5.6a, which is most likely due to the selection taken on the raw D5 and D6 summation of analogue signals instead of the summation of individually calibrated cell energies.

## 5.2 Tile Muon Digitizer Board

In order to provide the best possible matching in $\phi$ between the TileCal extended barrel modules and the LVL1 muon endcap S-L, the receiver board is required to process the D5 and D6 signals from eight TileCal modules and interface with three LVL1 muon endcap S-L blocks. Covering the entire detector therefore, requires 16 TMDBs. The TMDB is a 9U VMEbus slave module. The main functions of the TMDB are to:

- receive and digitize the TileCal Muon signals (D5 and D6) from eight modules (Analogue Stage)
- provide the correct calibration for each signal (VME FPGA)
- perform signal detection for each cell (Core FPGA)
- provide the BCID information for each cell (Core FPGA using timing information from TTCRx)
- transmit the $\eta$, $\phi$, and bunch number from the detected cells to the three muon S-L blocks (G-LINK)

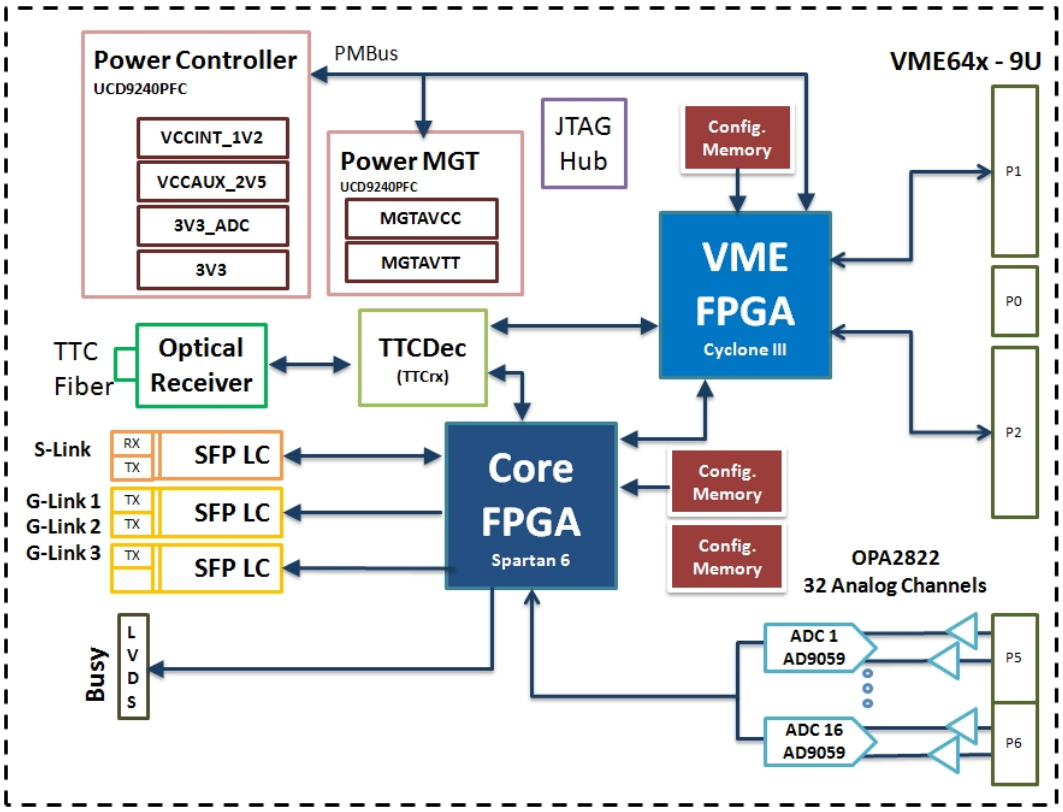



Figure 5.7: Schematic diagram of the TMDB system design [45].

- connect to neighbour receiver boards to accommodate the non-perfect matching between the eight TileCal modules and the three muon S-L blocks (LVDS)
- provide ROD data fragments to the DAQ system (ROD)

The 16 boards have been housed in two VMEbus crates in USA15, and the VMEbus is being used for configuration, control, monitoring and the distribution of the LHC clock. TTC signals are received optically by a TTC module in the VMEbus crate and re-transmitted to each TMDB.

### 5.2.1 TMDB system architecture

The TMDB receives the analog signals through the Analog channels and they are converted into digital signals. The Core FPGA has functionalities that aid in the estimation of the energy, using the Match Filter (MF) approach [60]. A threshold is applied and the resulting digitized signal is transferred to the TGC S-L boards through the G-LINKS, as seen in Figure 5.7.

The TMDB processes 512 signals in total, due to the double read-out of the TileCal D5 and D6 cells. There are 48 Sector-Logic (S-L) boards on the TGC side.

The S-L boards accepts the TMDB output signal and process the final decision. Based on these requirements, the system was designed with 16 TMDBs (8 per partition) with 32 channels (i.e. 8 Tile modules) and 3 optical links to interface with the TGC S-L boards. The VME interface of the TMDB is controlled by a customized FPGA (Cyclone III from Altera). 16 TileCal cells send 32 analogue signals to each TMDB and signal digitization is performed by the 8-bit flash ADCs. The digitized 32 signals are transferred to the core FPGA (Spartan-6 from Xilinx). In the core FPGA, the estimation of energy and the detection of the signal is performed. In order to monitor and debug with less complications, the TMDB transmits the ADC information, reconstructed energy and decisions from the trigger at a maximum LVL1 Trigger rate of 100 kHz. The TMDB transmits it to the ATLAS ROS via a Simple Link Interface (S-LINK) defined at CERN. There is one S-LINK (2.0 Gbps) used in the Core FPGA [61]. The TTC signal is transferred to the optical receiver and decoded in the TTCDec mezzanine. The optical communication with the muon TGC S-L is through the G-LINK protocol. There are 3 G-LINKS (800 Mbps) implemented in the Core FPGA, and they use the Small Form-factor Pluggable (SFP) connectors. TMDB trigger decision is provided to the TGC S-L boards for the processing of the final decision.

### 5.2.2 TMDB core firmware

Analogue signals are digitized at 40 MHz and the read-out pulse is sampled seven times. For each and every event, time samples are transferred to the Core FPGA. The Core FPGA estimates the energy and performs trigger decision assignments within the Module Processing Unit (MPU). The MPU block diagram is shown in Figure 5.8. The implementation of the MPU is in VHSIC,[2] hardware description language (VHDL). The energy reconstruction in the TMDB is executed by a 7-coefficient Finite Impulse Response (FIR) filter, with co-efficients based on MF approach [60]. In each read-out channel, the computation of MF co-efficients is carried out with the use of the respective reference pulse-shape and noise covariience matrix.

The output of the TMDB matches the value of energy which is determined by taking the inner product of the time samples received in the ADC counts and the MF coefficients. The TMDB output is utilized in providing four TMDB decision triggers, which are based on thresholds. The D6 cell provides two decision triggers and the D5+D6 cells provide the other two. A peak detector algorithm is used to trigger the right event, since the LHC has collisions every 25 ns and the read-out pulse remains in the read-out window.

The ATLAS conditions database contains the thresholds and MF coefficients

[2]Very High Speed Integrated Circuit

to be loaded into the TMDB. The trigger decision is acquired through the AND logic between "Peak detector" and "Thresholds" algorithms. The acquired latency

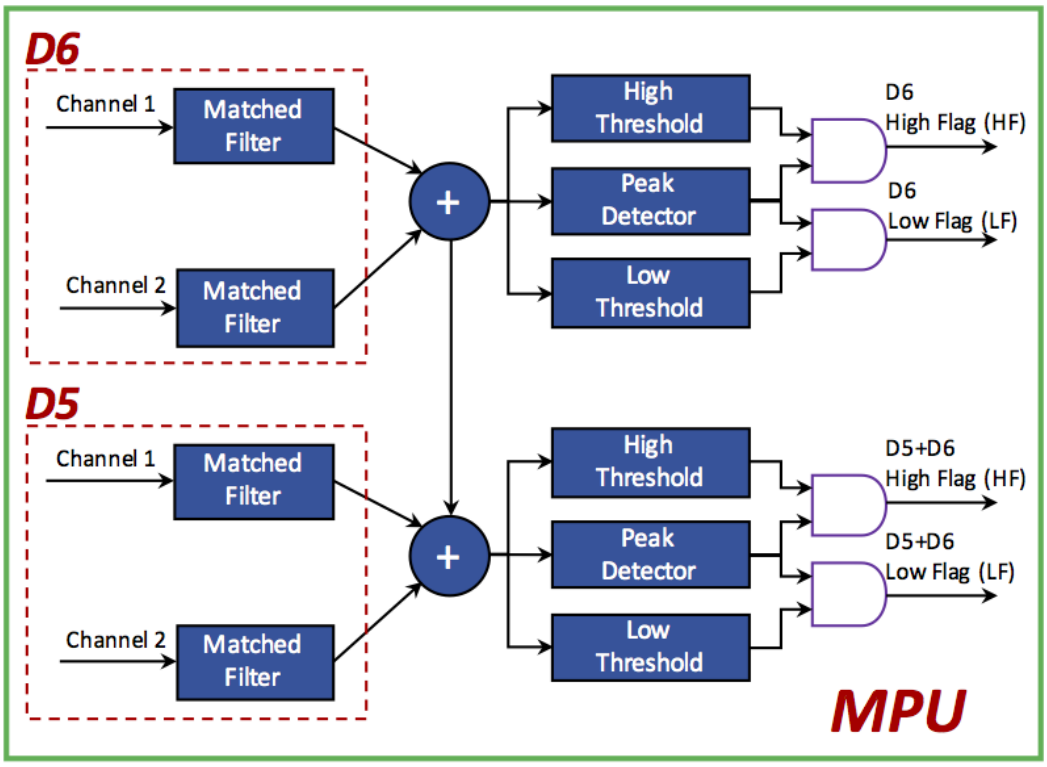



Figure 5.8: Diagramatic representation of the MPU [45].

of the MPU from the simulation is below 0.5 $\mu$s, which meets the requirements of the specification. The MF operation provides the TMDB output in arbitrary units and the output is converted to MeVs, using calibration parameters acquired ahead of time. Calibration constants are determined through a linear fit based on the TileCal offline reconstructed energy. The thresholds are given in arbitrary units and loaded into the TMDB for comparison with the MF output and to determine a TMDB decision.

The LVL1 Tile-Muon trigger system was commissioned before physics data taking in 2015. The project required the development of new simulation and DAQ software, and new firmware for the LVL1 muon endcap S-L. The upgrades will be implemented during the Phase-1 period.

# Chapter 6

# The handling of the busy signal in the TMDB

As discussed in Section 3.2.4, TMDBs were not only designed to process the data emerging the TileCal D5 and D6 cells of the extended barrels, but they were also designed to send their busy signals in a Low Voltage Differential Signaling,[1] (LVDS) format. The LVDS format is completely incompatible with the Transistor-Transistor Logic (TTL) input format that the RODBusy module accepts. The TMDB busy module was introduced to act as an interface between the TMDB and the RODBusy module. The following sections cover the busy signal occurrence, busy signal handling, hardware, firmware and software for the busy module.

## 6.1 Busy signal occurrence

The busy signal is a low-level notifier of when the data cannot be written, resulting in further events, which causes a traffic jam in the data flow. This appears to be a full memory issue, but it can indeed be caused by other factors. These factors are:

- First-In, First-Out (FIFO) Memory buffers become full.
- Bandwidth in S-LINK narrows (requires $\approx$ 160MB/s for 32-bit word at 40 MHz clock).
- ROS systems cannot ship events further, this is known as "Xoff".
- Bandwidth between TMDB MPU and S-LINK output device narrows.

The first factor is a bit outdated, in the latest revision of the TMDB firmware, the busy signal will actually be transmitted when the memories are close to being full and released when enough space has been cleared. This essentially introduces

[1] LVDS is a signaling method that operates at low power and is used for high speed binary data transmission, over inexpensive copper cables.

threshold levels, which can be adapted on the fly via VME registers. Furthermore, the FIFO memory was increased to a massive 512-bit size to reduce the occurrence of busy signals from the first factor. These new implementations were applied after installing the hardware in USA15 and observing a significant number of busy signals at around 100 kHz L1A frequency. This was unexpected since in B175, the busy occurrence was only observed above 180 kHz, and our operational frequency aims at 100 kHz. This new firmware change solved this issue, therefore a busy signal is now far more likely to be indicative of a physical hardware issue such as a broken data distribution line.

## 6.2 Busy signal handling

Following the TMDB system outline in section 5.2, the design and system requirements for the correct busy signal handling are as follows:

- accept LVDS input signals a total of 16 needed for EB project.
- output TTL signals, a total of 2 needed for EB project.
- fit in a 6U VME slot and communicate through the VME.
- have a user programmable chip for logic implementation.

## 6.3 Busy module hardware

The CAEN v1495 module described in Chapter 3, section 3.2.4, offers direct user customization. The module was evaluated against the busy signal system hardware requirements. It met all the fundamental requirements for the correct busy signal handling. It fulfilled the following requirements:

- equipped with a total of 64 LVDS input channels split evenly in port A and B.
- includes two TTL I/O, labelled port G.
- designed for VME communication.
- includes two FPGAs, one for user programmable logic and another one for VME communication.
- it is 6U in length and 1U wide.

Figure 6.1 provides an overview of the CAEN v1495 module. It comprises several input ports, form A to G, of which D, E, F are allocated for mezzanine expansion by using up to 3 mezzanine boards. The limitation of the number of channels to be expanded is up to 194. Ports A, B and G are the only ports utilized for this project. Port A is utilized for the EBC LVDS input and port B is utilized

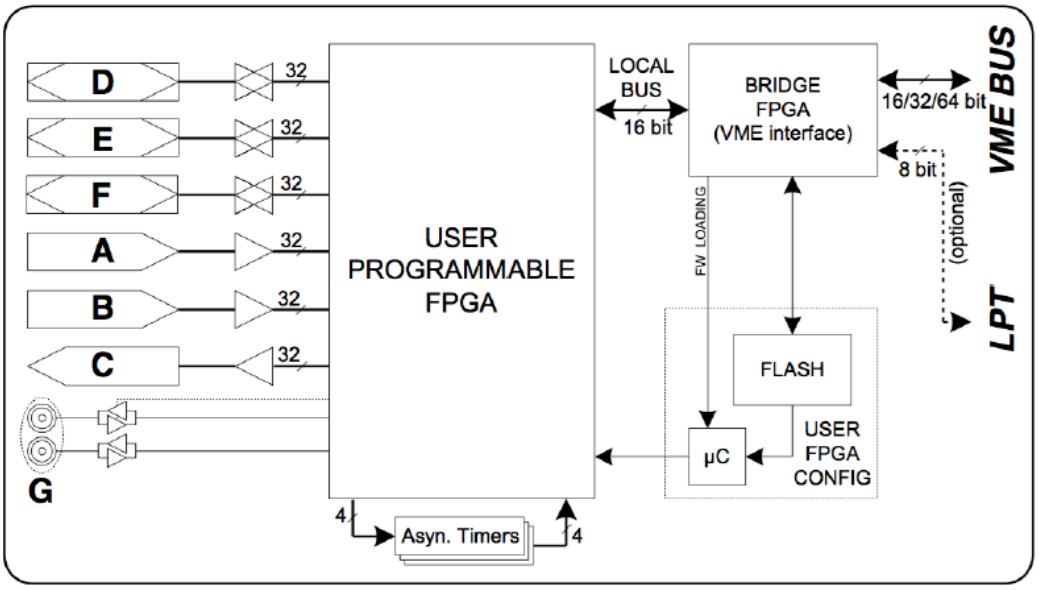



Figure 6.1: Block diagram of Module v1495 [62].

for the EBA LVDS input. The module is controlled by two FPGAs, which share a common clock of 40 MHz [62].

The "Bridge" FPGA is utilized for the VME interface and also connects the VME to the "User programmable" FPGA through a 16-bit local bus. The "Bridge" FPGA is also responsible for managing the programming through the VME of the "User programmable" FPGA. The VME bus communicates with the "Bridge" FPGA via a 16/32/64 bit.

The "User programmable" FPGA (Cyclone EP1C20) controls the I/O channels in the front panel and it is empty at its initial state. The user can program it according to a desired logic functionality and it can be programmed "on the fly" through the VME. This can be done in the absence of external hardware tools and without disconnecting or resetting the module, or turning the crate off.

The module has an embedded flash memory for storing the programming file to be loaded on the "User programmable" FPGA at any point in time. The module also consists of four timers for Gate/Trigger applications.

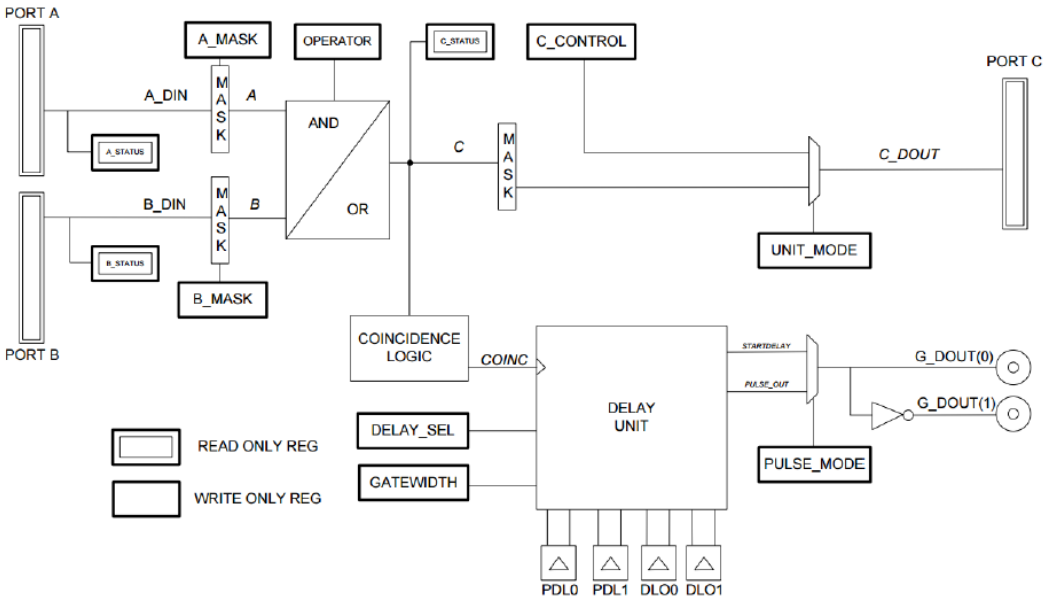



Figure 6.2: CAEN v1495 firmware reference design [62].

## 6.4 Busy module firmware

The firmware employed in the v1495 module is compiled using the Altera's Quartus II 13.0 (sp),[2] software and the Cyclone I family library. The latest version of Altera's Quartus II software supports Cyclone III families and later, it is not compatible with the Cyclone I family FPGA used in the v1495 module.

The preloaded reference design in the "User programmable" FPGA is specified as a design guide. The reference design gives access to ports A, B, C, G, and to use this design, does not require any mezzanine expansion cards. The reference design shown in Figure 6.2, closely resembles the TMDB busy module intended design. The TMDB busy module design does not require any use of delay units, coincidence logics and pulse delay lines. The most important attributes are the Port mapping, VME read and write operations , and masking bits.

The main difference between the reference design and the TMDB busy module design is, the TMDB busy module design requires each input port A or B to be treated individually and port C has no signal connected to it. Appendix A contains a detailed list of declared ports for the TMDB busy module and Appendix B contains a table of the local signals, declared within the architecture of the firmware. The firmware can be found in the CAEN website under the name

[2]Service Pack, it contains fixes and enhancements to the Quartus II software, that were not included in the Quartus II software versions.

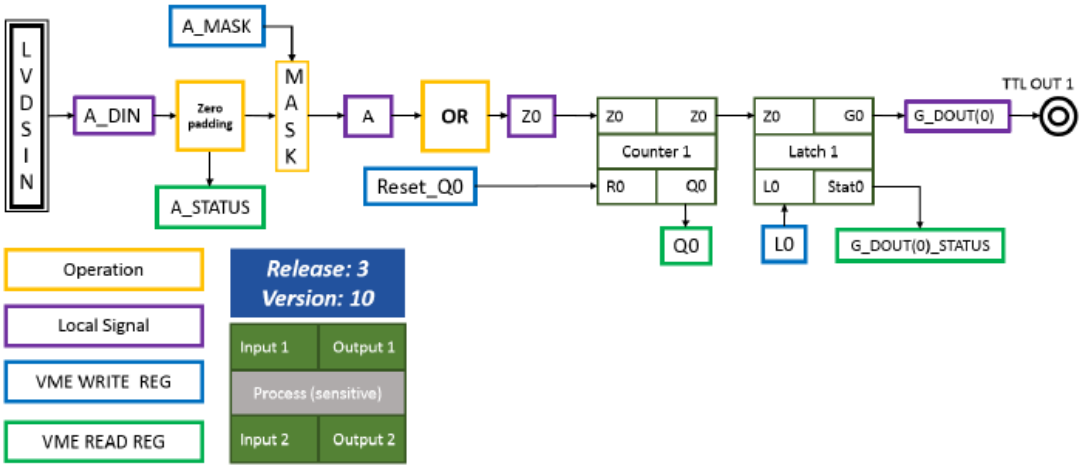



Figure 6.3: The schematic diagram of the firmware data flow for port A side, which is similar to port B dataflow.

"V1495 User Demo Firmware". The downloaded firmware project can be opened with Quartus, by opening the "v1495usr_demo.qpf" file in the FIT,[3] folder (qpf is quartus project file). The "Bridge" FPGA (i.e VME FPGA) and the "User programmable" FPGA firmware can be upgraded via VME, by writing the Flash. CAEN provides the CAEN Upgrader software tool which can be found on the CAEN web site.[4]

Figure 6.3 shows a detailed schematic diagram of how the data flows in the firmware from input to output. Local signals are contained within the architecture on the firmware and they are only used as temporary placeholders. Operations are not to be confused with processes. Zero-padding is the operation of zeroing the unused bits in the 32-bit signal, the masking operation combines the A_DIN signal with A_MASK by passing them through an AND gate. Thus, when a bit in A_MASK is '1' the signal is unmasked, and when it is '0' it is masked. The OR operation is what puts together the 8 signals or bits from a TMDB partition, into a single std_logic signal. The processes are used for counting the rising edges of the concatenated signal and pass onto the output port or latch on a state. These processes are sensitive to the input signals, i.e. they will only be called upon when an event in the input signal has occurred. Furthermore, the inverter needed for the correct logic communication with the RODBusy module is contained within the Latch processes. The inverter is essential since the TTL reception logic levels are flipped on the RODBusy module.

[3]Framework for Integrated Tests
[4]www.caen.it

### 6.4.1 Release and version specific information

Unnecessary VME registers migrated from the reference design, were removed and proprietary registers were added by Henric Wilkens and the author. The proprietary registers are of essence for the functionality of the target design and state machine implementation. The VME_FORCE register has been added to force on or off state from VME interface to G_DOUT port. VME registers for release number: 3 and version number: 10, have also been added. OUTPUTG0 and OUTPUTG1 processes have been added to select the desired output through port G, which is now dependent on the VME_FORCE register. The table with register addresses can be found in Appendix C.

The structure contains three sections, the first, which occupies registers from 0x1000-0x1050 (inclusive) are used for header registers that contain general information. The next set of registers begin from 0x1052, which contains all of the registers needed for side A while the next section contains addresses from 0x2052, which contains the registers needed for side B. This re-organization was done to simplify things at the state machine level. The access level of all these registers can be modified, so if need be a write only, can be easily changed to read and write and vice-versa. Default values can also be easily modified. As well as the VME address, provided it is not taking the space of a pre-existing one. The only variable to be maintained is the data sizing. Otherwise there will be errors when communicating with the VME FPGA.

## 6.5 Online busy module software

The online software is to behave as a state machine that has the ability to react to the inputs coming from the TMDB busy module. This state machine is to exist within the current TDAQ framework, just like the TMDBs online software is implemented. Also the state machine will need to be able to gather information from the OKS database to obtain things like VME base address. Functions from the RODBusy and RODBusyModule packages for the RODBusy module in the TTC crate, were modified in the development of the TMDB busy software by Henric Wilkens, Lucas Borgna and the author. These packages correspond to the lower and higher level software packages, respectively. The author further added the stopless removal functionalities in both libraries.

### 6.5.1 Busy module software and firmware synergy

The online software needs to be as simple as possible and to have a reduction in the number of functions taken from the RODBusy packages. Simplicity reduces bugs in the software. This can be accomplished by having a synergy between the FPGA firmware and the online software. As seen in Figure 6.4, the firmware has




Figure 6.4: FPGA registers layout for synergy with online software.

setup virtual spaces for the registers needed and organized them into a space that is specific for each use. Headers occupy the space from 0x1000 to 0x1050. Headers in this case refers to general information registers in the firmware, e.g. there are two headers which contain the firmware release and version numbers. Another header example is the scratch register which is simply used as 16-bit read & write test of VME operations without having any effect on the firmware.

The next set of registers named Side 'A' registers are given the space between 0x1052 to 0x2050. This space is reserved for the registers that belong to the operations on the LVDS Port A input signals. This can be the MASK, STATUS, COUNTER, etc... signals, but they will only belong to the first '8' TMDBs in the crate. These first 8 TMDBs on the left side of the crate actually correspond to the EBC, so the names are mismatched. Similarly the Side 'B' space registers, 0x2052 to 0x3050, belong to all the input signals going into LVDS port B.

The implications of this approach means that there are two virtual instances of the software for a single physical board. One of the virtual instance pulls the needed header register and its respective 'side' registers; the other instance simply pulls the next set of 'side' registers. In the software, the switch between sides is done by a simple addition in each applicable function. The original register address, for which the information is stored in the header file, gets a modifier of + VME_SIZE*SIDE. The VME_SIZE is chosen to be 0x1000 and the side can alternate between 0 and 1. Here the value of side = 0 is for EBC and side = 1 is for EBA.

### 6.5.2 Low level library

The low level library is the TMDBBusy package. It makes use of the vme rcc API package which allows for simple VME read and write operations by using ReadSafe(reg, &data) and WriteSafe(reg,data) respectively. There are a total of 10 main parts of the low level library, these are summarized below:

- **VME communication**: Handles the opening and closing of the VME connection by using mastermap/unmap. This is where the details of VME connections are important, such as the windows size for which in the busy module 24-bits was chosen.
- **Framework functions**: These are responsible for being able to read or write or mask individual bits in specific registers.
- **Software busy**: Contains the functions that can determine, assert, release and check whether a software busy has been asserted. A software busy is a terminology inherited from the framework, what it really means in the context of the busy module is a latching operation
- **Set/get limits**: Sets and gets limits, and reset intervals for higher software to use.
- **Busy & mask operations**: Directly retrieves the status information from the FPGA registers in binary or hexadecimal format. Has the ability to also set the mask, unfortunately busy status is read only. Lastly it also has the ability to enable and disable specific channels
- **VME pipeline testing**: can read and write the main header scratch function to test the passage of data through the VME bus onto the user FPGA in the busy module. It can also read the side scratch register to determine on which side registers we are reading.
- **Miscellaneous**: contains the functions to set the side variable '0' or '1', as well as the function which retrieves the firmware release and version number.
- **FPGA functionality**: has the core functionality to read & reset the FPGA 32-bit counters and read the port G output.
- **Busy output latches**: Functions which can force the latches in the firmware to output a constant '0' or '1', not busy or busy, respectively.
- **FPGA Reset/ Configuring**: Can return the state of the FPGA to its default values determined in the firmware. This can be done either all at once or per side or header. It also contains a "do nothing" function, which is used for avoiding a bug in the higher level software, where the first VME read or write operations returns a 0x205 (slave address not found) error, yet the operation is perform adequately. Any subsequent VME operations will not yield this issue. In the future, this is where one could implement a script which uploads the firmware.

The low-level library also contains a script called “menuTMDBBusy”, which can be used to swiftly test the operation of any function or any future implementations. It is a very simple command window menu, which allows verification of the low-level library without having to start the TDAQ GUI.

### 6.5.3 High level library

The higher level library is the TMDBBusyModule package. This library mostly concerns itself with the running of the software within the TDAQ GUI and is, therefore, very similar to the RODBusy software. Here the software first resets all the applicable FPGA registers to their default values. It then performs some tests using the latches and if successful, will then pass onto the next step and prepare for a run. The ”do nothing” function is implemented in this instance. It catches this odd first read/write VME error 0x205 and logs it in the ERS_LOG, so that it does not show up on the shifter panel, while other errors are reported. The reason why the resolution for this bug was to ‘sweep it under the rug’, is because the error in the code does not logically follow from the previous statement. If one was to replace the ”do nothing” function with the one that actually does something, such as defaulting the FPGA, one will realise that the action has taken place and the master was indeed able to find a slave with the given address. This is definitely something that should be investigated later on. In previous experience it seems that when there are VME requests too close to each other, it spits out this error.

Another important aspect of the higher level software is the polling action package. This is the responsible member for producing the real time sampling of the data. In fact it has been set to a polling rate of 5 seconds for current testing. It is also the member responsible for applying the control conditions. This condition is known as a permanent busy. If a TMDB has had a state of constant busy, the software will sample the state and counters once, and if upon the next sample the counter and state has not changed it will then apply a permanent busy condition. The permanent busy condition is a state for which the software disables that specific TMDB channel and will also alert the ATLAS Control Room (ACR) shifter about this error. Reinstating the normal operational mode requires manual intervention.

# Chapter 7

# Conclusions and future work

## 7.1 Conclusions

The implementation of the stopless removal consists of two parts: firmware and software, which are both essential for success in this project. A CAEN v1495 board was chosen by TileCal members and implemented into the TileCal BE electronics test bench in B175 by the author.

The CAEN v1495 board acts as a TMDB busy module. It was introduced to act as an interface between the TMDBs and the ROD busy module, since the TMDBs were designed to send their busy signals in a LVDS format. The LVDS format is completely incompatible with the TTL input format, that the ROD busy module accepts. The test bench in B175 required upgrades in firmware and software, in order to have similar operational environment as the ATLAS detector. The latest modified version of the firmware was uploaded in the CAEN v1495 and tested successfully. The CAEN v1495 is a suitable solution for the TMDB busy signal handling, as it allows plenty scalability and flexibility.

The B175 TileCal Online software packages have been migrated by the author following ATLAS new code management tools. The online busy module software necessary for the stopless removal, needed to be able to react to the inputs from the TMDB busy module and to gather information from the OKS database. Certain functions from the RODBusy and the RODBusyModule packages were modified according to the TMDB busy module specifications. The packages correspond to the low level (TMDBBusy) and the high level (TMDBBusyModule) libraries.

## 7.2 Future work

FPGA development keeps evolving, hence the need to improve robustness without altering the core functionality of the TMDB busy module. There were several

complications with the correct fabrication of the busy cable which interfaces the v1495 module with the TMDBs. The cable was made in a non-standard way and it is not as robust as intended. It is worth investigating a better, standardized way of manufacturing the cables with the proper crimping tools. Most of the functions have been tested successfully and the failed ones, still need to be modified. Upon completion of the modifications and tests, during the author's PhD studies, the stopless removal will be implemented in the ATLAS control room.

Online software additional features can be added, with the most important one being the integration of the script responsible for writing the firmware from the VME bus into the FPGA. It would be worthwhile to spend some time integrating this as a function on the low level part and higher level part of the software to be called upon during the configuration step. This should not significantly increase the configuration time of the systems, as it takes roughly 30 seconds for configuration. However, the first problem that will be encountered is that the higher level software will actually configure the FPGA twice. This is because of the 2 sides of the software, but there is however only 1 target FPGA/physical board.

# Appendix A

# Entity list

The list of ports found in the entity list of the firmware is detailed in the following table. The reference design includes all of these ports and most of these ports are not useful in the TMDB busy module design. In this project, they have been declared and it is a more stable design to have them declared and routed. The table below provides an outline of the usage of each signal.

| *Port Name* | *Direction* | *Width* | *Description* |
|---|---|---|---|
| | | *GLOBAL SIGNALS* | |
| NLBRES | IN | 1 | Async Reset (active low) |
| LCLK | IN | 1 | Local Bus Clock (40 MHz) |
| REGISTER INTERFACE | | | |
| REG_WREN | IN | 1 | Write pulse (active high) |
| REG_RDEN | IN | 1 | Read pulse (active high) |
| REG_ADDR | IN | 16 | Register Address |
| REG_DIN | IN | 16 | Data from CAEN Local Bus |
| REG_DOUT | OUT | 16 | Data to CAEN Local Bus |
| USR_ACCESS | IN | 1 | Current register access is at user address space<br>(Active high) |
| *V1495 Front Panel Ports (PORT A, B, C, G) INTERFACE* | | | |
| A_DIN | IN | 32 | In A (32 x LVDS/ECL) |
| B_DIN | IN | 32 | In B (32 x LVDS/ECL) |
| C_DOUT | OUT | 32 | Out C (32 x LVDS) |
| G_LEV | OUT | 1 | Output Level select (0=> TTL; 1=>NIM) |
| G_DIR | OUT | 1 | Output Enable (0=>Output, 1=>Input) |
| G_DOUT | OUT | 2 | Out G – LEMO (2 x NIM/TTL) |
| G_DIN | IN | 2 | In G – LEMO (2 x NIM/TTL) |
| *V1495* | *Mezzanine* | *Expansion* | *Ports (PORT D, E, F) INTERFACE* |
| D_IDCODE | IN | 3 | D slot mezzanine Identifier |
| D_LEV | OUT | 1 | D slot Port Signal Level Select |
| D_DIR | OUT | 1 | D slot Port Direction |
| D_DIN | IN | 32 | D Slot Data In Bus |
| D_DOUT | OUT | 32 | D slot Data Out Bus |
| E_IDCODE | IN | 3 | E slot mezzanine identifier |
| E_LEV | OUT | 1 | E port signal level select |
| E_DIR | OUT | 1 | E slot Direction |
| E_DIN | IN | 32 | E slot Data In bus |
| E_DOUT | OUT | 32 | E slot data Out bus |
| F_IDCODE | IN | 3 | F slot mezzanine Identifier |
| F_LEV | OUT | 1 | F slot port signal level select |
| F_DIR | OUT | 1 | F slot Port Direction |
| F_DIN | IN | 32 | F slot data in bus |
| F_DOUT | OUT | 32 | F slot data out bus |
| | | *PDL CONFIGURATION INTERFACE* | |
| PDL_WR | OUT | 1 | Write Enable |
| PDL_SEL | OUT | 1 | PDL Selection (0=>PDL0, 1=>PDL1) |
| PDL_READ | IN | 8 | Read Data |
| PDL_WRITE | OUT | 8 | Write Data |
| PDL_DIRE | OUT | 1 | Direction (0=> Write, 1 =>Read) |
| | *DELAY* | *LINES AND OSCILLATORS I/O* | |
| PDL0_OUT | IN | 1 | Signal from PDL0 Output |

| | | | |
|---|---|---|---|
| PDL1_OUT | IN | 1 | Signal from PDL1 Output |
| DLO0_OUT | IN | 1 | Signal from DLO0 Output |
| DLO1_OUT | IN | 1 | Signal from DLO1 Output |
| PDL0_IN | OUT | 1 | Signal to PDL0 |
| PDL1_IN | OUT | 1 | Signal to PDL1 Input |
| DLO0_GATE | OUT | 1 | Signal to DLO0 Input |
| DLO1_GATE | OUT | 1 | Signal to DLO1 Input |
| | | | *SPARE INTERFACE* |
| SPARE_OUT | OUT | 12 | SPARE Data Out |
| SPARE_IN | IN | 12 | SPARE Data In |
| SPARE_DIR | OUT | 1 | SPARE Direction |
| | | | *LED INTERFACE* |
| RED_PULSE | OUT | 1 | RED Led Pulse (active high) |
| GREEN_PULSE | OUT | 1 | GREEN Led Pulse (active high) |

# Appendix B

# Architecture signal declaration

The names, sizes and descriptions of the local signals declared within the firmware architecture, are listed in the following table.

| *Name* | *Size(bits)* | *Description* |
|---|---|---|
| *A_STATUS* | 32 | Contains port A status |
| *B_STATUS* | 32 | Contains port B status |
| *A_MASK* | 32 | Masks port A input |
| *B_MASK* | 32 | Masks port B input |
| *SCRATCH* | 16 | Empty read and write register |
| *A* | 32 | A input signal after masking |
| *B* | 32 | B input signal after masking |
| *Z0* | 1 | First 8 bits of A input logically OR |
| *Z1* | 1 | First 8 bits of B input logically OR |
| *Q0b* | 32 | Counter of Z0 rising-edges |
| *Q1b* | 32 | Counter of Z1 rising-edges |
| *ResetCount_G0* | 16 | Resets counter Q0b |
| *ResetCount_G1* | 16 | Resets counter Q1b |
| *VME_FORCE1G0* | 16 | Forces '1' on G0 |
| *VME_FORCE0G0* | 16 | Forces '0' on G0 |
| *VME_FORCE0G1* | 16 | Forces '0' on G1 |
| *VME_FORCE1G1* | 16 | Forces '1' on G1 |
| *RELEASE* | 16 | Major changes number |
| *VERSION* | 16 | Minor changes number |
| *G_DOUT_STATUS0* | 16 | Port G0 Status |
| *G_DOUT_STATUS1* | 16 | Port G1 Status |
| *DEFAULT_HEAD* | 16 | Reset Headers to default |
| *DEFAULT_DUMMY* | 16 | Does Nothing |
| *DEFAULT_A* | 16 | Reset A-side to default |
| *DEFAULT_B* | 16 | Reset B-side to default |
| *SIDE_ASCRATCH* | 16 | Side A scratch test register |
| *SIDE_BSCRATCH* | 16 | Side B scratch test register |

# Appendix C

# CAEN v1495 VME addresses and useful information for busy signal handling.

Table Colour scheme:

| | |
|---|---|
| | Header Registers, useful key information regarding firmware and VME R/W test |
| | Registers for Side A |
| | Registers for Side B |

| *Name* | *Address* | *Access* | *Notes* | *Default* |
|---|---|---|---|---|
| RELEASE | 0x1000 | RO | Proprietary firmware release number, corresponding to major changes and strategy shifts | X"0003" |
| VERSION | 0x1002 | RO | Proprietary firmware version number, corresponding to small incremental changes. | X"0010" |
| SCRATCH* | 0x1004 | RW | For testing R/W operation from VME. | X"DEAD" |
| DEFAULT_ALL | 0x1006 | RW | Forces applicable registers to default values | X"0000" |
| DEFAULT_HEAD | 0x1008 | RW | Forces header registers to default value | X"0000" |
| A_STATUS_L | 0x1052 | RO | Port A status. Reflects only on A[15:0]; | N/A |
| A_STATUS_H | 0x1054 | RO | Port A status. Reflects only on A[31:16]; | N/A |
| A_MASK_L | 0x1056 | RW | Port A mask. This register masks A[15:0], active low | X"00FF" |
| A_MASK_H | 0x1058 | RW | Port A mask. This register masks A[31:16], active low | X"0000" |
| Q0b_L | 0x105A | RO | First part of 32-bit counter 0, makes up Q0b[15:0]; | N/A |
| Q0b_H | 0x105C | RO | Second part of 32-bit counter 0, makes up Q0b[31:16]; | N/A |
| GDOUT_STAT0 | 0x105E | RO | Outputs the status of G_DOUT0 on first bit only | N/A |
| ResetCount_G0 | 0x1060 | WO | Used to reset counter G0 back to zero | X"0000" |
| VMEFORCE1_G0 | 0x1062 | RW | Forces a true output on G(0) port | X"0000" |
| VMEFORCE0_G0 | 0x1064 | RW | Forces a constant false output on G(0) port | X"0000" |
| SIDE_ASCRATCH | 0x106A | RW | Scratch to test if we are writing to this side | X"AAAA" |

| | | | | |
|---|---|---|---|---|
| A_DEFAULT_A | 0x106C | RW | Defaults all registers on side A and itself | X"0000" |
| B_STATUS_L | 0x2052 | RO | Port B status. Reflects only on B[15:0]; | N/A |
| B_STATUS_H | 0x2054 | RO | Port B status. Reflects only on B[31:16]; | N/A |
| B_MASK_L | 0x2056 | RW | Port B mask. This register masks B[15:0], active low | X"00FF" |
| *B_MASK_H* | *0x2058* | *RW* | *Port B mask. This register masks B[31:16], active low* | *X"0000"* |
| Q1b_L | 0x205A | RO | First part of 32-bit counter 1, makes up Q1b[15:0]; | N/A |
| Q1b_H | 0x205C | RO | Second part of 32-bit counter 0, makes up Q1b[31:16]; | N/A |
| GDOUT_STAT1 | 0x205E | RO | Outputs the status of G_DOUT1 on first bit only | N/A |
| ResetCount_G1 | 0x2060 | WO | Resets counter G1 back to zero | X"0000" |
| VMEFORCE1_G1 | 0x2062 | RW | Forces a true output on G(1) | X"0000" |
| VMEFORCE0_G0 | 0x2064 | RW | Forces a false output on G(1) | X"0000" |
| SIDE_BSCRATCH | 0x206A | RW | Scratch  to test if we are writing to this side | X"BBBB" |
| A_DEFAULT_B | 0x206C | RW | Defaults all registers on side B and itself | X"0000" |

## C.1 Detailed Description of registers

- **RELEASE**: Register used to keep track of which release of the firmware is being used. The release number corresponds to major structural changes in the firmware.
- **VERSION**: Version number register that is used, together with the release number, to determine which minor changes in the firmware have been made within the same release.
- **SCRATCH***: A simple register that is only used to test the read and write operations of the VME bus. In this specific version this register has had its default value changed depending on which v1495, the firmware is written on. This is to verify which board has been accessed. Thus if it is on the first board (VME address 0x020000), its default value is X"DEAD" and if it is on the second board, its default value is X"CAFE". This is simply for debugging purposes and to convince us which board has been accessed. The permissions and address are still the same. However the first board firmware is now R3V6-A and the second board is R3V6-B.
- **DEFAULT_ALL**: 16-bit logic vector of which only the first bit is used. If the first bit is set to '1' it will force all of the applicable registers to their default state from the FPGA firmware.
- **DEFAULT_HEAD**: Similar to DEFAULT_ALL but now only the header registers are reset to their default values.
- **A_STATUS_L & A_STATUS_H**: Simply reads the status of the input signals fed into the LVDS port A of the v1495 board. It has been split into 2 registers (low and high), to accommodate for the 16-bit bus width to the VME and FPGA Bridge.
- **A_MASK_L & A_MASK_H**: These are the write registers, which are used to individually mask the signals from the incoming port A, defaulted to fully unmasked. In this case the masking is done by writing a value of '0' from the VME bus into the register, a value of '1' corresponds to unmasked. The arrays are 16-bit each when passed through the bridge but are concatenated in the "User programmable" FPGA. The first or lowest element of this array corresponds to the first input signal from port A. So A_MASK (0) masks A_DIN (0).
- **Q0b_L & Q0b_H**: These are 2 16-bits registers that make up the 32-bit counter Q0b in the firmware design. Q0b_L makes up the lower 16 bits of the counter and Q0b_H makes up the higher 16 bits of this counter. In order to correctly read the number counted these two registers should be concatenated first and then read as whole, provided that the 16-bit threshold has been surpassed. Similar concept to the status and masking registers.
- **A_GDOUT_STAT0 & A_GDOUT_STAT1**: Registers used to read the output of the port G both G_DOUT(0) and G_DOUT(1) for passing on to

the state machine to determine the busy status.

- **ResetCount_G0 & ResetCount_G1**: VME write register that is used to reset the counter registers back to zero. This reset action is a not asynchronous and will reset the counter only on the next clock cycle of the counters. It is a 16-bit register but only the first 2 bits are used. The first bit, if '1', resets the Q0b register and the second, if '1' resets the Q1b register. If any of the bits are '0' they will simply allow their respective registers to continue counting.
- **VMEFORCE1_G0/G1 & VMEFORCE0_G0/G1**: Registers used to latch the output of either G ports independently to, either a True or False signal, which remains as such until turned off. VMEFORCE1_G0 sets the output of port G(0) as '1', and VMEFORCE0_G0 sets the output of the same port to '0'. VMEFORCE1_G1 and VMEFORCE0_G1 are identical to the previous two except that they are now applied to port G(1).
- **B_STATUS_L & B_STATUS_H**: Similar to the A_STATUS ports, however this now reads directly the signal that is being fed into the LVDS port B of the v1495 board. The original 32-bit signal has been again split up into 2 16-bit registers to accommodate for the bus width.
- **B_MASK_L & B_MASK_L**: Similar to A_MASK registers, but they now mask the LVDS signals coming into port B.
- **Q1b_L & Q1b_H**: These are 2 16-bits registers that make up the 32-bit counter Q1b in the firmware design. Q1b_L makes up the lower 16 bits of the counter and Q1b_H makes up the higher 16 bits of this counter. In order to correctly read the number counted these two registers should be concatenated first and then read as whole, provided that the 16-bit threshold has been surpassed. Identical to the Q0b counter except that this is used for the second output signal.
- **A_DUMMYA_L/H & A_DUMMYB_L/H**: A register implemented solely to achieve the read and write access level for the A/B_STATUS registers. These registers are directly driven by the input port A_DIN, hence adding an additional driver from the VME IS explicitly prohibited. Thus these dummy variables were created to simply pass on the status states, but can also be overwritten from the VME to test downstream effects from the state machine software. These registers should be removed on final revision, unless they can offer additional functionality.
- **SIDE_(A/B) SCRATCH**: Similar scratch variable that has now been implemented to determine and test which side of the v1495 we are accessing, since the low-level access software considers one physical board as 2 virtual boards. This is to avoid having repeated instances of functions that specifically address port G0 or G1 of the v1495 board.
- **DEFAULT_A/B**: Same concept as the all default and header default, except this now defaults only the selected side either A or B.

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