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Light yield studies of neutron irradiated plastic scintillators and the testing of the front-end readout system of the Atlas tile calorimeter

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University of the Witwatersrand

School of Physics

Light Yield Studies of Neutron irradiated plastic scintillators and The Testing of the Front-End readout system of the ATLAS Tile Calorimeter.

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A dissertation submitted to the Faculty of Science, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Master of Science

2020

Declaration

I declare that this dissertation is my own, except where explicit reference is made to the work of others. It is being submitted for the Degree of Master of Science at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination at any other University.



Thabo Clearance Masuku 2^{nd} day of September 2020 at University of the Witwatersrand, Johannesburg

Abstract

The CERN's Large Hadron Collider (LHC) is the largest particle accelerator in the World. This comprises a variety of experiments to investigate the basic structure of matter in the universe. A Toroidal LHC Apparatus (ATLAS) is one of the experiments at CERN that is used to detect particles that result from the proton-proton collisions. The ATLAS detector is a general-purpose detector. During the maintenance periods, the ATLAS Tile Calorimeter (TileCal) detector modules are repaired/fixed. The Front-End (FE) electronics of these TileCal modules are tested and maintained using the MobiDICK system and if they are faulty they are repaired or replaced. The FE readout system, which is housed in the super-drawers, is tested and verified using the MobiDICK system.

The upgrade of the LHC to the High-Luminosity LHC (HL-LHC) will provide great opportunities to explore new physics beyond the Standard Model. This poses significant challenges to the detector and the Trigger and data acquisition system (TDAQ). The TileCal readout electronics will be replaced during the Phase-II upgrade to cope with the HL-LHC's increased luminosity. In this study we focus on the certification of the Demonstrator at the particle test beams. The Demonstrator's latest electronics are being commissioned to be integrated into ATLAS during the LS2. This study presents the early readout certification of the Demonstrator.

Due to their properties, such as fast time response and high optical transmission, plastic scintillators are used in particle detectors. The fast pulse generation allows for fast readout, and the intensity of the light is proportional to the energy deposit. Scintillators are used to measure energies and to reconstruct the particles' path through the luminescence process due to ionizing radiation. However, long exposure to ionizing radiation can cause permanent damage to the scintillators. In this study we focus on the effects of neutron irradiation of plastic scintillators similar to that of the lifetime of the HL-LHC. The plastic scintillator being investigated are the

UPS-923A blue scintillators and green scintillators. The optical properties of the irradiated samples are studied using the techniques of light yield measurements.

Acknowledgements

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Related research outputs

Published Journal Article:

- G. Mokgatitwane, B. Mellado, E. Sideras-Haddad, R. Erasmus, T. Masuku, J.E Mdhuli, N. Lekalakala, C.O Kureba, Yu.I Dauydov, V. Baronov, I. Vasilyev, and P.N Zhmurime, "*Effect of the neutron radiation on the optical and structural properties of blue and green emitting plastic scintillators*", Nuclear Inst. and Methods in Physics Research B vol 436, December 2018.

Published Proceedings:

- G. Mokgatitwane, B. Mellado, E. Sideras-Haddad, R. Erasmus, T. Masuku, J.E Mdhuli, N. Lekalakala, C.O Kureba, L. Mashishi, G. Peters, T. Sechogela", *A systematic study of the properties of proton induced damage in plastic scintillators for the upgrade of the Tile Calorimeter of the ATLAS detector*", To appear in the book of Proceedings of HEPP2018, the High Energy Particle Physics workshop, February 2018; Port Elizabeth, South Africa.

- T. Masuku, N. Lekalakala, H. Tlou, B. Mellado, "*ATLAS Tile Calorimeter Online Software configuration and performance study of the super-drawer components*", To appear in the book of Proceedings of SAIP2018, 63^{rd} Annual Conference of the South African Institute of Physics, June 2018; Bloemfontein, South Africa.

- N. Lekalakala, T. Masuku, B. Mellado, "*Overview of test beam campaigns for readout electronics of the upgrade Tile Calorimeter of the ATLAS Detector*", To appear in the book of Proceedings of HEPP2019, the High Energy Particle Physics workshop, February 2019; Port Elizaberth, South Africa.

- N. Lekalakala, T. Masuku, B. Mellado, "*The Diagnostic and Verification System for the Tile Calorimeter Trigger and Data Acquisition framework of the ATLAS Detector*", Submitted to Proceedings of SAIP2019, 64^{th} Annual Con-

ference of the South African Institute of Physics, July 2019; Polokwane, South Africa.

Chapter 1

Introduction

The CERN's Large Hadron Collider (LHC) is the world's largest particle accelerator. It comprises a wide variety of experiments to investigate the basic structure of matter in the universe. There are four main experiments of the LHC, namely: A Toroidal LHC Apparatus (ATLAS), the Compact Muon Solenoid (CMS), A Large Ion Collider Experiment (ALICE), and the Large Hadron Collider Beauty (LHCb). The first two experiments (ATLAS and CMS) are general-purpose experiments and the remaining two experiments (ALICE and LHCb) are designed to study specific phenomena. Our main focus in this study is on the ATLAS detector. The ATLAS detector consists of several layers of separate sub-systems that work in synergy to detect the various particles and measure their properties. The Hadronic Tile Calorimeter (TileCal) is an ATLAS sub-detector system used to detect and measure the energy and direction of hadrons and jets.

During the maintenance periods of the ATLAS detector, several Front-End modules of the TileCal detector that became faulty during the operation of the detector were extracted, tested and fixed. The components of the super-drawers which forms the FE readout systems, were tested and repaired before being inserted back to the detector. The super-drawer is the FE system reading the signals in the TileCal that occur from the collisions of proton-proton at the ATLAS detector of the LHC. The main components of the super-drawers are the PMT blocks, Motherboards, digitizer

boards and the interface boards. In each super-drawer, there are two Motherboards, 8 digitizer boards, and one interface board. Each super-drawer can house 48 PMT blocks, but for the Long Barrel (LB) only 45 PMTs are used and on the Extended Barrels only 32 PMTs are used. There are 9 summation cards for the LB and 7 summation cards for the EB. The super-drawer has 8 digitizer boards for the LB and 6 digitizers for the EB. The components of the super-drawers are tested using the mobile test-bench integrity check (MobiDICK), and components that were not in good working conditions were repaired/replaced. Those that were in a good working condition are to be used again on the detector.

Another aspect of this study is the characterization of the Demonstrator of the TileCal upgraded FE electronics for the HL-LHC. The HL-LHC will provide a lot of opportunities to explore the fundamental constituents of nature. The readout architecture of the current system needs to be upgraded to cope with the increase in luminosity. The Demonstrator is a prototype that has been designed to evaluate and to qualify new concepts of readout and trigger in full ATLAS operation and data acquisition. The Demonstrator is based on the 3-in-1 FE option and is designed to be fully compatible with the current system, offering both analogue trigger sums for the current Level 1 (LVL1) trigger as well as full digital readout to the PreProcessor (PPr) prototype Phase-II trigger. The PPr prototype is the core component of the off-detector electronics of the Demonstrator system. It has an interface to the Timing, Trigger and Control (TTC) network, and can emulate the current FE electronics in legacy mode, by providing properly formatted data to the current back-end ReadOut Drivers (ROD), or full flavour data to the FELIX, which is the read-out system sought for Phase-II upgrade.

The last part of this study will be dedicated to the study of irradiated of plastic scintillators. These are organic materials that in interaction with ionizing radiation

exhibit the effect of scintillation. Electronic excitations in scintillating material are caused by incident radiation which then relaxes to the ground state via a fluorescence process when light emission occurs. The amount of light emitted can be used to identify particles and thus play a significant role in the field of detector physics, because it is dependent upon the energy of the exciting particle. In this study we investigate the effects of neutron irradiation and we study how they affect the optical properties of the organic plastic scintillator. Neutron irradiation is known to allow bulk probing of the material since they are penetrating particles. In this study light yield techniques are used to evaluate the optical properties of the neutron-irradiated plastic scintillators.

The objectives of this study are to:

- Test the super-drawer components during maintenance and reviewing their quality to make sure that during data collection no information is lost or corrupted.
- Assemble and certify new electronics on the Demonstrator during the LS2 before insertion at ATLAS.
- Study the effects of neutron irradiation on plastic scintillators by using light yield techniques to study their optical properties.

1.1 Chapter presentation

Chapter 2 provides an overview of the history and main achievements of the CERN laboratory; it also describes the LHC accelerators, experiments and the ATLAS detector in more detail. Finally, it includes a description of the basic design concepts of the sub-detectors and the ATLAS TDAQ. Chapter 3 describes the sub-detector of the ATLAS detector, the TileCal, and in particular, the FE instrumentation and readout electronics. The testing of the FE readout system is described in chapter 4 with emphasis on the use of the MobiDICK for testing of the FE components. The

description of the old and current MobiDICKs are discussed in this chapter and also the tests performed by the current MobiDICK are discussed. Chapter 5 discusses the TileCal Phase-II upgrades electronics and focuses more on the work done on the Demonstrator during the beginning of the LS2, with more focus on the certification of the Demonstrator before the insertion on the ATLAS detector. Chapter 6 deals with the light yield studies of the neutron-irradiated plastic scintillators. In this chapter the effects of radiation damage on the optical properties of the samples are studied using light yield measurements. Lastly, Chapter 7 is the summary and the conclusions of the work being presented.

Chapter 2

The ATLAS Experiment at the CERN Large Hadron Collider

2.1 CERN

CERN is the European Organisation of Nuclear Research, and the name CERN is derived from the French acronym Conseil European pour la Research Nucleaire, which translates to European Council for Nuclear Research. It was a provisional council to set up the laboratory in 1952 with the mandate of establishing a fundamental physics research organization in Europe [1]. CERN became official in 1954 and with the title European Organization for Nuclear Research. The main area of research at CERN is particle physics, which is the study of fundamental constituents of matter and the forces acting between them.

Many achievements can be attributed to CERN, like the discovery of the direct CP violation in the NA48 experiment, the neutral currents in the Gargamelle bubble chamber in 1974, Higgs boson in 2012, the observation of the $W^{\pm}$ and Z particles in 1983 by the UA1 and UA2 experiments, and the accurate measurements of the Z particle that showed that there are only three families of particles in nature. The above few examples are among a long list of important physics achievements made

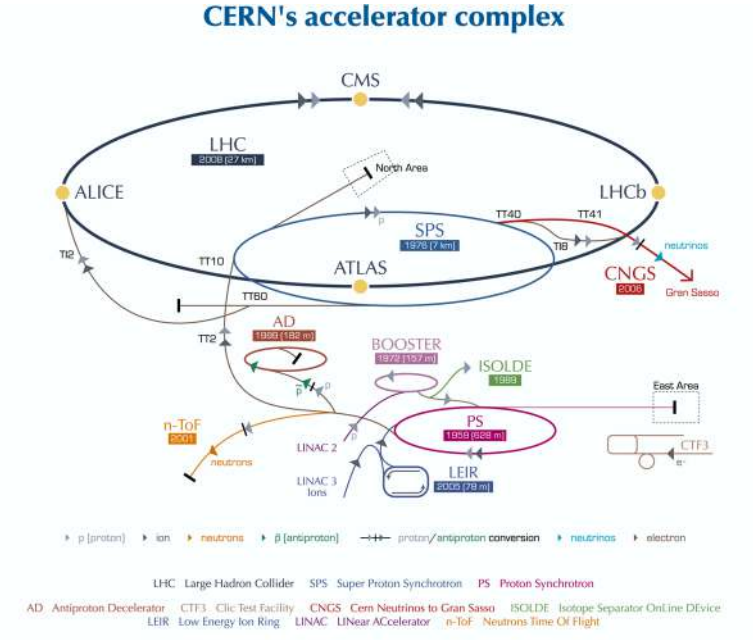


Figure 2.1: CERN LHC's Accelerator Complex. [2]

at CERN. CERN is also an excellent environment for the development of new technologies in other fields like Computing and Electronics.

Figure 2.1 shows the CERN's Large Hadron Collider (LHC) accelerator complex.

2.2 The Large Hadron Collider

The LHC is the world's largest and most powerful particle accelerator (see Figure 2.1). Inside the LHC two-particle beams are accelerated and collided head-on. The LHC was built in the tunnel where the Large Electron-Positron (LEP) collider operated from 1989 to the end of 2000. The LEP was a circular collider with a circumference of 27 km on the border of France and Switzerland. Inside the LHC's 27 km ring, protons are accelerated and formed into beams in four large detectors before being injected with an energy of 450 GeV. The beams are then accelerated in the ring until their energy is increased by a factor of 15, to an energy of 7 TeV. When this energy is reached, the beams collide in the centre of the LHC's main experiments. The proton beams in the LHC collide at a centre of mass energy of 14 TeV and a design luminosity of 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The LHC beam parameters are

Table 2.1: LHC Beam parameters.

Parameters	**Values**
Injection Energy	450 GeV
Collision Energy	7 TeV
Primary Fluor	1.5×10^{11}
Number of bunches per fill	2808
Nominal Luminosity	10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Inelastic cross section	60 mb
Total cross section	100 mb
Revolution Frequency	11.245 kHz
Bunch Frequency	40.08 MHz
Circumference Length	26.66 km
Radius	4.25 km
Number of Dipole magnets	1232
Number of quadrupole magnets	392
Nominal Magnetic field strength	8.33 Tesla

shown in Table 2.1.

2.3 The ATLAS Experiment

At CERN, the ATLAS detector is the general-purpose proton-proton collider designed to exploit the full discovery potential of the LHC [3]. The ATLAS detector is about 45 meters long, more than 25 meters high and has an overall weight of approximately 7 000 tones, see Figure 2.2. The four main detector components that play an important role in the reconstruction of the original collision in the observation of new physics. These components are The Inner detector, the Calorimeters, the Muon Spectrometer, and the Magnetic system.

The inner detector is isolated in the innermost part of the ATLAS detector. It is built around the beamline and specifically designed for tracking and vertexing and is used to measure tracks of charged particles resulting from collisions. The Transition Radiation Tracker (TRT), the Pixel detector and the Semi-Conductor Tracker (SCT) are all sub-detectors of the inner detector. A superconducting solenoid magnet which gives a magnetic field of two Telsa surrounds this internal detector. Surrounding the Inner detector are the electromagnetic and the hadronic (Tile) calorimeters, hadronic

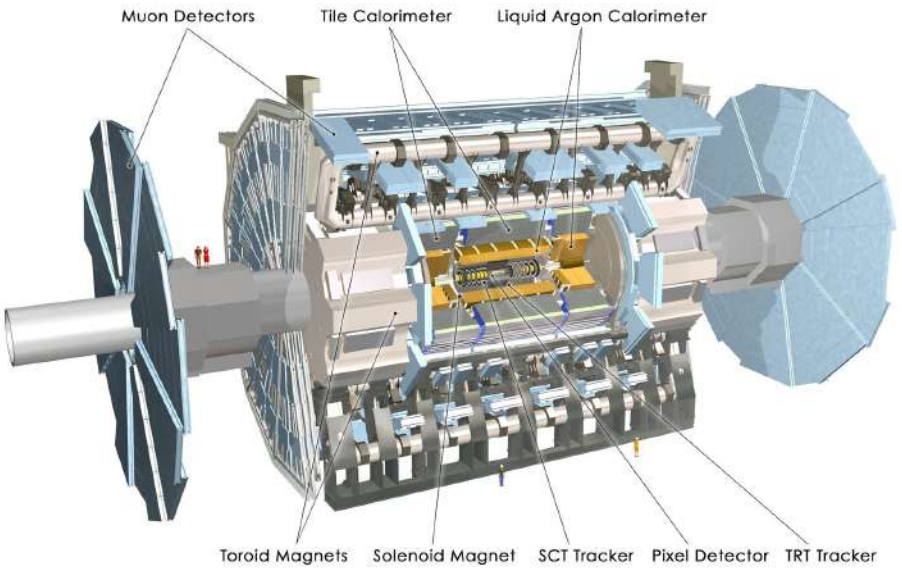


Figure 2.2: The ATLAS Detector [3].

end-cap, and forward calorimeters. All electromagnetic and hadronic calorimeters have been designed to contain the showers and only neutrinos and muons can escape from these layers. The layer after the calorimeters is formed by the muon spectrometer and a toroidal magnet. The magnetic field from the toroidal magnets bends the muons and the muon tracking system measures the trajectories of these particles and any charged particles leaving the calorimeters. The neutrinos are the only particles that pass the detector undetected.

2.3.1 Inner Detector

The inner detector has been designed for highly efficient reconstruction of tracks and decay vertices [4]. The inner detector also contributes to the detection of electrons, photons and muons, as in calorimeters and muon systems. The inner detector also supplies extra signatures for short-lived particles decay vertices. The following are the important physics consideration for the design of the inner detector:

- Excellent momentum and impact parameter resolution for tracks with $p_T > 0.5$ GeV up to very high momentum,

- tracking coverage over the range $|\eta| < 2.5$,

- high efficiency with equally high noise rejection,
- identification of the charge of high-p_T tracks,
- tagging of jets originating from b-quarks (b-jets),
- reconstruction of soft electrons and secondary vertices from b and tau decays,
- identification of the primary vertex,
- electron identification capability,
- identification of a high-p_T track to reduce the Level 1 electromagnetic cluster trigger rate from jet events

Figure 2.3 shows a sectional view of the inner detector.

2.3.2 Calorimeters

Fast detector response and fine granularity are required to minimize the impact of the pileup on the physics performance. The calorimetry part of the ATLAS detector consists of an Electromagnetic (EM) calorimeter covering the pseudorapidity region $\eta < 3.2$ for all the EM calorimetry, a hadronic calorimeter covering $|\eta| < 1.7$, hadronic endcap calorimeter covering $1.4 < |\eta| < 3.2$, and the forward calorimeters covering $3.2 < |\eta| < 4.9$. The EM calorimeter is lead/Liquid-Argon (LAr) detector with accordion geometry. The hadronic calorimeter is based on a sampling technique with plastic scintillating plates (Tiles) embedded in a steel absorber. The radiation-hard LAr technologies are used for all the calorimeters where higher radiation resistance is needed. This is the section where you have the Hadronic Endcap Calorimeter (HEC) and the Forward calorimeter (FCal). Figure 2.4 shows the scheme with all the calorimeters of the ATLAS detectors.

Electromagnetic Calorimetry

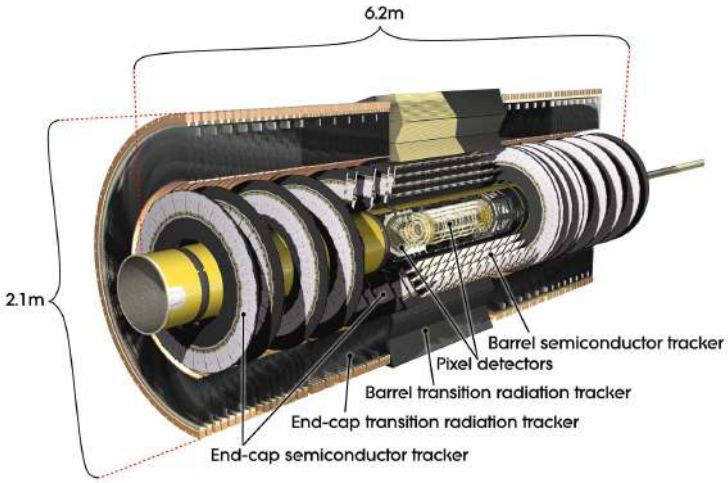


Figure 2.3: The Inner Detector [3].

The electromagnetic calorimeter consists of two identical half-barrels that cover the rapidity of range $|\eta| < 1.4$. Each half-barrel is divided into 16 modules and for each half-barrel, the calorimeter is made of 1024 accordion-shaped absorbers alternating with 1024 readout electrodes, and they are arranged with a complete ϕ symmetry around the beam axis.

Inside the endcap cryostat, we have the Electromagnetic EndCap (EMEC), the HEC, and FCal calorimeters. The EMEC uses the same technique as in the barrel part and it covers the range $1.375 < |\eta| < 3.2$. The HEC uses copper plates as an absorber and it covers the range $1.5 < |\eta| < 3.2$ region. The FCal covers the range $3.2 < |\eta| < 4.9$ region, it provides EM coverage by using copper as an absorber and provides hadronic showers by using tungsten as an absorber.

Hadronic Calorimeter

As mentioned above the Hadronic calorimeter covers the range $|\eta| < 1.7$. In this calorimeter the technique of sampling is used, where plastic scintillators (tiles) are embedded in a steel absorber structure. The tiles are each readout by the Wavelength Shifting (WLS) fibres on both sides. These tiles are grouped into bundles to form cells and each of these cells is readout by two Photo-multiplier Tubes (PMTs). Figure 2.5 shows the TileCal module components and structure. The TileCal has a

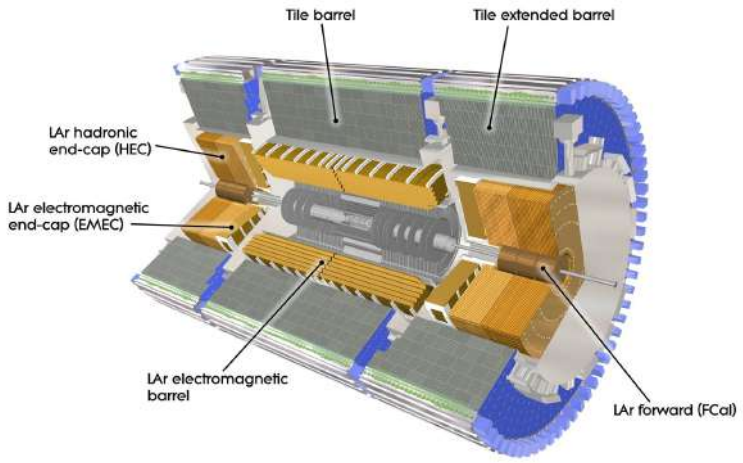


Figure 2.4: The Calorimeter system of the ATLAS detector [3].

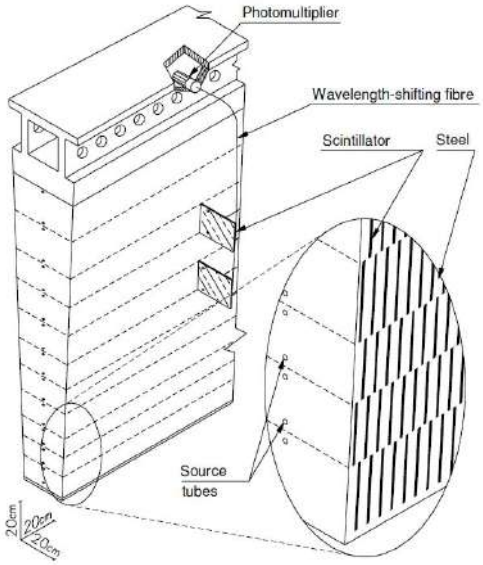


Figure 2.5: TileCal module components and structure [3].

hollow cylinder that has an inner and outer radius of 2.28 m and 4.23 m respectively. The central Long Barrel (LB) has a length of 5.56 m and covers the range $|\eta| < 1$, and the Extended Barrels (EBs) have a length of 2.91 m with each covering the range of $0.8 < |\eta| < 1$. Each barrel consists of 64 wedge-shaped modules staggered in a ϕ direction. There is a 0.6 m gap between the LB and the EB that is needed for ID and LAr calorimeter services.

The TileCal is divided into three layers (A, BC, and D). The cell segmentation for layers A and BC in $\Delta\eta \times \Delta\phi$ is 0.1×0.1 and for the D layer cells is 0.2×0.1. The FE electronics with the PMTs are in the outer radius back-beam region of the

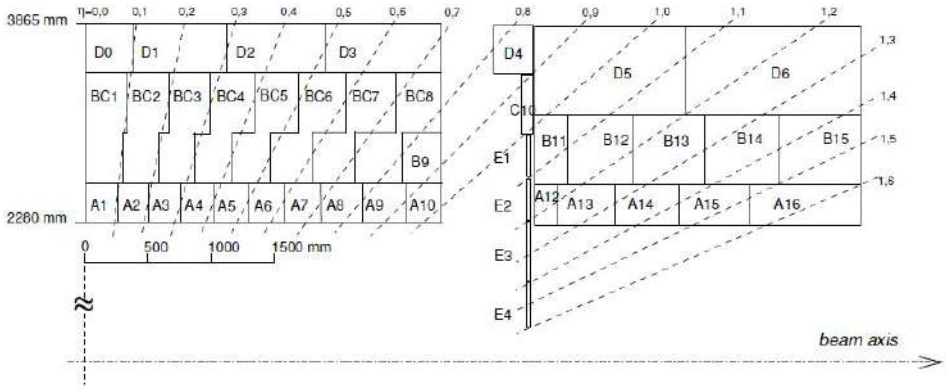


Figure 2.6: TileCal cell distribution scheme for half of a long barrel module (on the left) and an extended barrel module (on the right) showing the projective distribution of pseudo-rapidity [3].

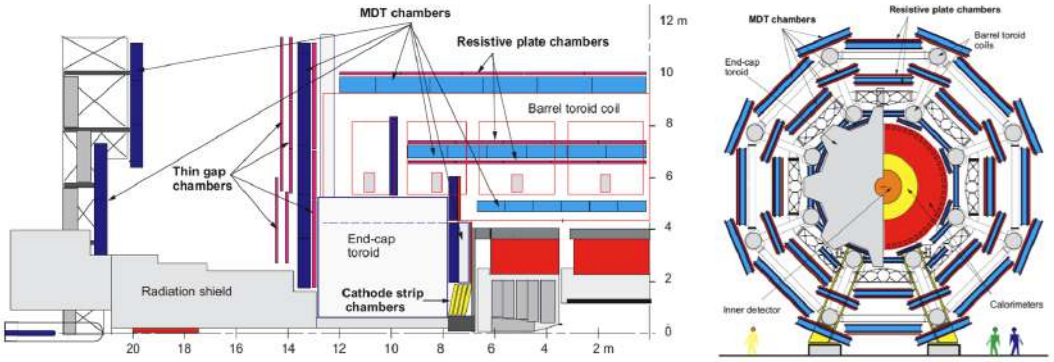


Figure 2.7: The ATLAS muon spectrometer in the rz (left) and xy view (right) [3].

calorimeter, placed in moveable drawers that are 1.5 m long. A super-drawer is made up of two drawers that are sequentially mounted from both sides of the LB and one side of the EB. The whole calorimeter needs 512 identical drawers. The super-drawers can each house 48 PMTs, but only 45 are needed for each side of the LB and 38 PMTs needed for the EBs. It contains approximately 10 000 readout channels and it weighs around 2 300 tonnes. The Scheme of the Cell Distribution is displayed in Figure 2.6 for the half long and extended barrel modules.

2.3.3 The Muon Spectrometer

The ATLAS muon spectrometer has been used to make efficient use of the magnetic bending power with a coverage of $|\eta| < 2.7$. The spectrometer consists of practical chamber dimensions for production, transport and installation, and also includes

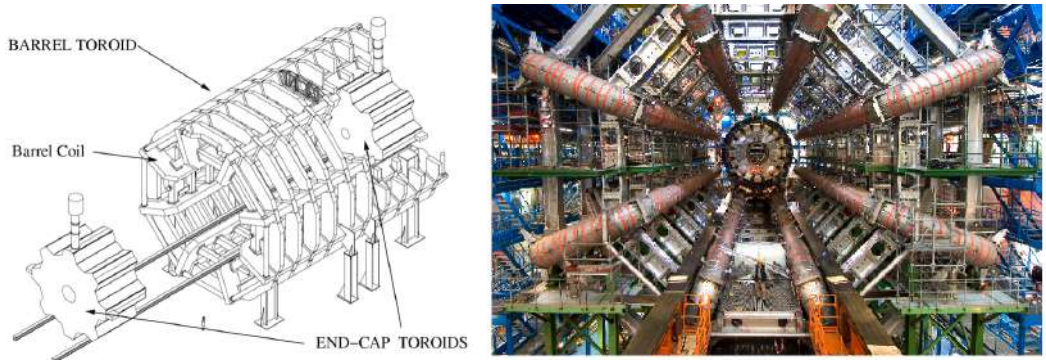


Figure 2.8: ATLAS superconducting air-core toroid magnet system (left) and the barrel toroid (right) [3].

projective towers η and ϕ directions [5]. The spectrometer is divided into three regions, the barrel regions ($|\eta| < 1.05$), the transition region ($1.05 < |\eta| < 1.4$), and the end-cap region ($|\eta| > 1.4$). Figure 2.7 shows the position of the muon chambers.

2.3.4 Magnetic Field

The ATLAS magnetic field system is optimized to increase the identification power of the sub-detectors in a lightweight and open structure, which minimizes scattering effects [6]. The magnetic system consists of a central solenoid serving the inner detector with an axial magnetic field surrounded by eight large scale air-core coils generating a toroidal magnetic field for the muon spectrometer. The magnetic system weighs 1300 tons and is cooled by liquid helium at 4.5 K. In this case, the Nb-Ti superconductor in a copper matrix technology is used. Figure 2.8 shows ATLAS superconducting air-core magnet system the barrel toroid.

2.4 The ATLAS Trigger and Data Acquisition System

The trigger and data acquisition system is organized in layers. A first rejection system (LVL1 trigger) reduces 40MHz to around 100 kHz. The LVL1 trigger is fully implemented in 2.5 microseconds, using custom components, as it accepts or rejects events. When they are accepted, the fragments of the on-detector electronic

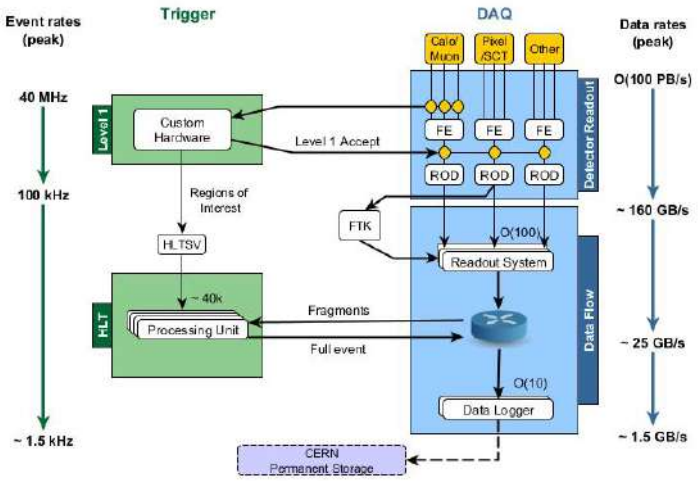


Figure 2.9: The ATLAS DAQ System in LHC Run 2. [7]

FE are forwarded via customized point-to-point detector links to the BE electronics ReadOut Drivers (ROD) in the separate service cavern. The RODs perform data manipulation tasks like aggregation or compression before pushing the data to the circa 100 ReadOut System (ROS) PCs over 1800 point-to-point optical links (S-Link) [8]. ROS PCs buffer event fragments to a computer farm consisting of 1500 servers on request to the High-Level Trigger (HLT). Here, the event rate is further reduced to the target event rate of about 1 kHz.

The main features to be discussed will be the upgrades of the ROS, Region of Interest Builder (RoIB), High-Level Trigger (HLT) and Data Logger (Sub-Farm Output, or SFO). An overview of the upgraded system is presented in Figure 2.9.

2.4.1 Schedule of the HL-LHC

Figure 2.10 shows the schedule for the HL-LHC. Recently the LS2 was prolonged by 6 months and the Run3 extended by one year. Thus the start of the HL-LHC is now planned for 2025.

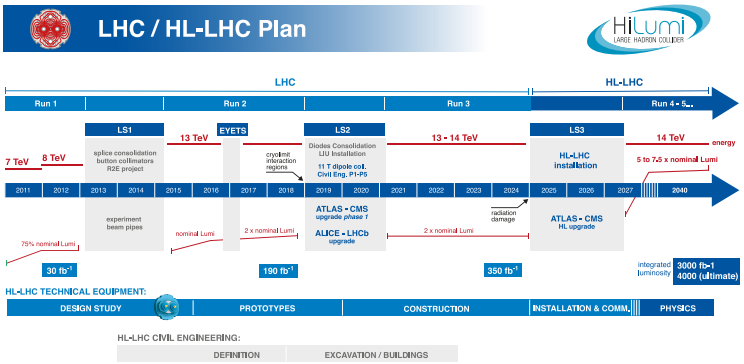


Figure 2.10: Schedule of the HL-LHC [9]

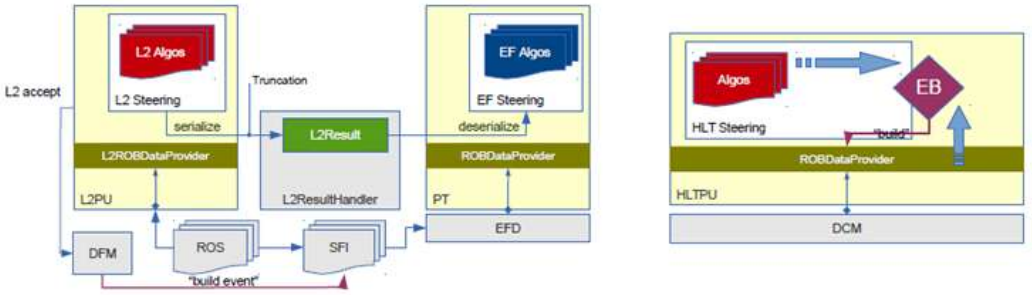


Figure 2.11: Conceptual diagram showing the merger of logical blocks within the combined High Level Trigger. The old architecture is shown on the left and the new one on the right. [7].

2.4.2 High-Level Trigger

The upgrade of the HLT was designed to significantly improve efficiency by a major conceptual change. There is also a separate processing capability program in place to replace older servers in the farm with new models in late operation. The number of motherboards has increased to about 2000 by the end of 2016 in the hardware replacement programme. The newest machines, making up 50 % of the farm, are based on modern Intel Haswell [10] architecture-based CPUs. More significantly, the structure of the farm has been simplified. What were previously two separate farms [11] handling Regions of Interest and full event filtering were merged into one system. The merger of the two HLT steps was achieved through a complete rewrite of many of the individual algorithms that previously ran on the two farms, with functionality combined, as demonstrated schematically in Figure 2.11. A single 'data collection manager' (DCM) process running on each HLT node orchestrates

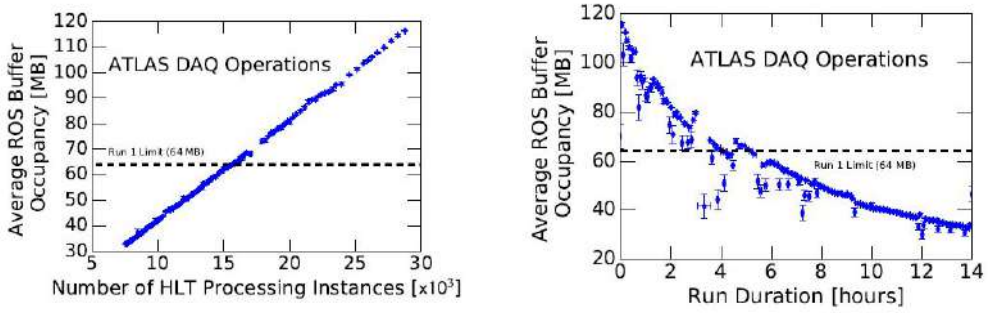


Figure 2.12: Average ROS buffer occupancy for a single readout channel plotted against number of HLT application instances in use in the HLT farm (Left). The evolution of buffer occupancy for a typical single readout channel during an ATLAS run (Right). [7]

the data flow from the ROS through to the HLT processing units, event building processes and finally the SFOs.

There are several areas where the benefits of the merger can be felt. Firstly, data throughput requirements are reduced as there is no longer a need to transfer event data from one farm to another, or re-request the data from the ROS. Secondly, whereas the split system resulted in particular cores in the farms only ever being tasked with given processing types, potentially leading to under-utilisation, the new system allows all cores to perform all HLT processes. This enables much more efficient resource distribution and load balancing. The increased capacity and exibility of the system also makes it possible to build events gradually by requesting data during processing, rather than having a dedicated event building step. With the old architecture, such a step was necessary and was implemented with dedicated machines. The performance of these systems limited the event building rate to 7 kHz. With the new architecture limitations may come from readout or network bandwidth, but at a much higher threshold than the previous system. No saturation has yet been observed in regular operations.

2.4.3 ReadOut System

The ROS is responsible for buffering event data passing LVL1 trigger selection for the period taken for the HLT to perform its more detailed processing. The ROS consists of a series of server commodity machines that host personalized I/O cards. These receive data from detector FE electronics over one of approximately 1850 optical links and store them in internal memory buffers. During processing the HLT will request data from the ROS as needed before either accepting an event, and sending it to the SFOs for permanent storage, or requesting its deletion from the ROS buffers. The upgrade of the ROS [12] focused on increasing the density of the system (i.e., the number of links that can be handled in the same amount of server space) as well as increasing the data rates and volumes to be processed. Furthermore, the overall buffering capacity was upgraded to allow for future increases in requirements due to the expansion of the HLT farm size. The new system allows the data input to be buffered by 100 kHz, to an average size of 1,6 kB per connection input, and 50% of the data can be sent to HLT without any loss of performance. This is to be compared to a 75 kHz input rate with 10-15 % readout in Run 1 up to the same event size.

The primary element of the ROS upgrade, installed for the start of Run 2, was the design and implementation of an upgraded version of the custom I/O board, known as the RobinNP. The new component consists of ATLAS-specific firmware installed on a PCIe board originally developed by the ALICE Collaboration [13]. The hardware features a high-performance Xilinx Virtex 6 series FPGA and 8 GB of onboard DDR3 RAM. The current PCIe bus implementation allows an in-practice maximum output bandwidth of 1.6 GB/s, potentially upgradable to 3.2 GB/s should requirements evolve.

To accommodate evolving conditions towards LHC Run 3, the performance of an upgraded ROS has comfortably satisfied the ATLAS requirements for Run 2. Fig-

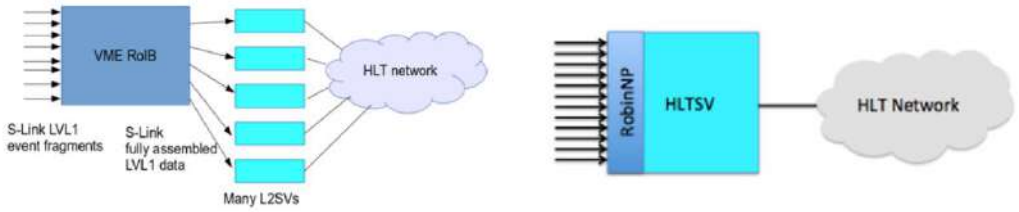


Figure 2.13: Schematics of RoIB system in Run 1 (Left). Schematics of RoIB system in Run 2 (Right). [7]

ure 2.12 demonstrates the impact of the increased memory capacity by comparing the limits imposed by the Run 1 system on HLT farm size (left), as well as the evolution of buffer occupancy throughout a run (Right).

2.4.4 Region of Interest Builder

ATLAS HLT event processing is driven by the RoI detector study flagged with the LVL1 trigger system. RoI information from the different LVL1 trigger system components is then assembled into one entity via a special system before an FLT processing system assigns it to a free HLT node. This RoIB system was implemented in Run 1 in custom-designed hardware based on VMEbus technology with multiple supervisor nodes. Experience has indicated that the performance limitation of this system would be the complexity of RoI information used in run 2 and would also be subject to maintenance and obsolescence problems in view of the age of custom hardware.

In Run 2 the RoIB system was replaced with an integrated design based on ROS technology [15]. RoI data from the LVL1 trigger system components are now received by a RobinNP card hosted in a standard ROS server PC and automatically transferred to the host for further processing. RoI's are then built completely on software before being transferred for assignment to an HLT node to a single farm supervisor process now running on the same host. The evolution of the system is presented in Figure 2.13. The updated RoIB has been successfully deployed in

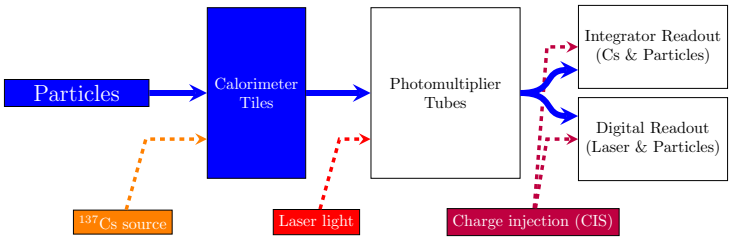


Figure 2.14: Flow diagram of the readout signal paths of the different TileCal calibration systems.[14].

early 2016, enabling further information on the RoI to be handled at a high rate, as well as expanding monitoring and downstream reporting capability. The design also provides adequate replacement capacity to meet any real performance changes.

2.4.5 Data Logger

The data logger, referred to for historical reasons as SFO, is responsible for aggregating large volumes of event data accepted by the HLT for further processing into a standardised file format for transfer to the ATLAS Tier0 processing centre for further analysis and permanent storage using the EOS standard [16]. For Run 2, a state-of-the-art CPU storage and a revamped multi-threading processing model was added to the SFO system. The new system contains six specially selected nodes with a total buffer capacity of 340 TB, which allows for the local storage of up to 24 hours of collision data before transfer to EOS. The system is extendable and new nodes can be integrated to increase efficiency if necessary, but the new installation already works beyond 1.5 GB/s in design.

2.5 Calibration Systems

In general the readout chain of the signal can be separated into three stages. Each stage can change its behaviour with time and therefore has to be monitored and in some cases corrected see Figure 2.14. The three stages and possible effects are:

- Production of light in the scintillating tiles and propagation through the WLS fibres. Radiation damage and ageing of fibres and scintillators can change

their light yield. Such changes are typically slow and can be monitored by inducing light of know characteristics with the help of a radioactive source. In the TileCal a Cesium-137 source is used to calibrate the response of the scintillator tiles.

- Conversion of the light into a current at the PMT. Due to gain drift and deterioration of gain and quantum efficiency, the photo-multiplier response may change. The injection of a well known light pulse at this stage can be used to monitor such processes. A Laser system is used to induce a light pulse to the PMTs to monitor their response.

- Readout and processing of the calorimeter signal. Ageing of electronic components can result in non-linearity. This can be monitored by injecting a defined charge into the electronics and comparing it with the signal given at the end of the readout chain. The 3-in-1 cards include a Charge Injection System to inject a programmable charge into the shaping and amplification circuit.

Therefore the TileCal inter-calibration and monitoring strategy is based on several calibration systems. The final channel reconstructed energy calibrated to GeV units can be expressed as:

$$E[GeV] = A[ADC] \times K_{ADC \to pC} \times K_{laser} \times K_{Cs} \times K_{pC \to GeV}$$

Where $A[ADC]$ is the reconstructed amplitude of the pulse in ADC-counts. The term $K_{pC \to GeV}$ represents the conversion factor from the charge (pC) to the electromagnetic scale energy (GeV) which was measured during the 2001-2003 test beam using electrons and muons. The other three constants in the above equation are periodically monitored and determined with the TileCal calibration systems. They provide corrections to the response of the scintillator and fibres, the PMTs and the electronics.

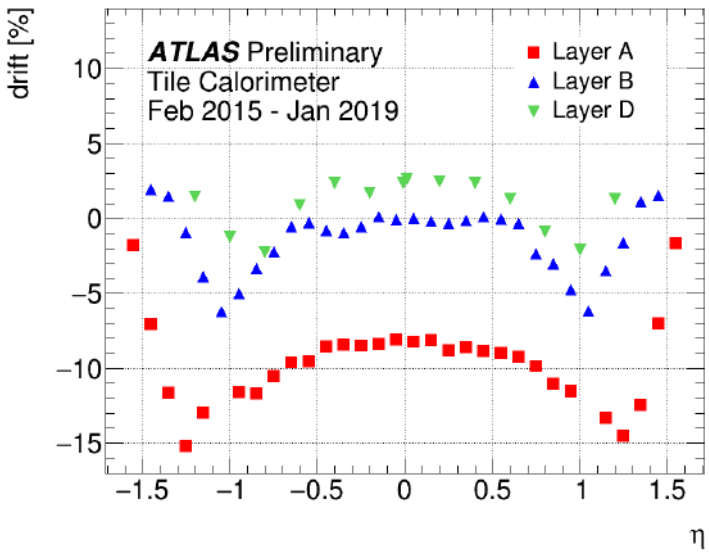


Figure 2.15: Down-drift in different cells in three longitudinal layers as a function of cell position in η between February 2015 (start of Run 2) and January 2019 (start of LS2) [14].

2.5.1 The Cesium-137 Calibration System

A radioactive source of Cesium-137 is circulated through a system of steel tubes crossing each cell in Tile. This calibration is done every month with dedicated runs for about 6 hours when no beam is circulating in the accelerator. The cesium source induces light with 662 keV γ-rays with an activity of around 330 MBq. The integrator circuit in the 3-in-1 cards measures the current from the PMT which is normalized to the cell size. The cesium system is the only calibration system that allows determining the response of the entire readout chain. This system is used to monitor the response of the optical elements and to measure the response of each cell and also to equalize the response of the calorimeter cells at the electromagnetic scale. The cesium calibration system determines the response of the optical chain with a precision better than 0.3 %. Figure 2.15 shows the maximum signal change measured with the cesium calibration system during the 2015 data taking period as a function of the pseudo-rapidity in three longitudinal cell layers. Every point represents an average of 64 cells (over ϕ).

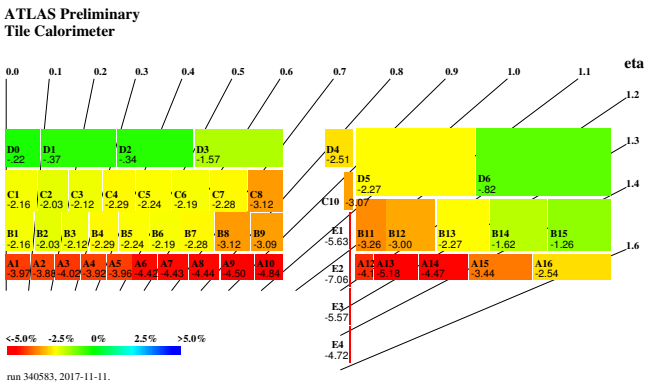


Figure 2.16: Mean PMT gain variation per cell type measured with the laser system between two cesium runs in April 2017. [14].

2.5.2 The Laser System

The Laser system is used to monitor and calibrate the gain and linearity of the PMTs as well as the timing. The laser calibration is done twice per week using dedicated runs between beam fills and during physics runs in the LHC gaps dedicated to the calibration. The dedicated runs are used to equalize the response of the PMTs in time between two consecutive cesium runs whereas the laser pulses in empty bunches are used to monitor the stability of the timing. The laser emits a pulse of light of 532 nm to each PMT. This wavelength corresponds to the typical wavelength of the light produced by particles crossing the detector. The light produced is split and distributed to all the TileCal PMTs. Furthermore, the amplitude of the produced light pulses is monitored inside the Laser system using a set of photo-diodes.

Figure 2.16 shows the mean gain variation (in %) in the ATLAS Tile calorimeter photo-multipliers that read the signal deposited in each channel, as a function of η and radius, between the 6 March and 11 November 2017 (covering the entire 2017 proton collisions period). The gain in each PMT is measured using a laser calibration system that sends a controlled amount of light in the photocathode of each PMT in the absence of collisions. The mean gain variation of the 10000 TileCal channels is computed cell by cell using the Combined method, and calculated for a set of reference runs taken before the initial date (all laser runs within 10 days

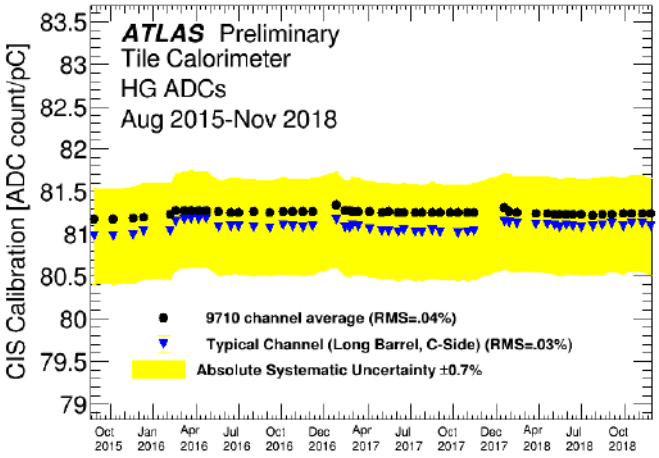


Figure 2.17: High gain CIS calibration stability during the 2015 data taking period. [14].

of March 6th 2017). For each cell, the gain variation is defined as the mean of the Gaussian function that fits the gain variation distribution of the channels associated with this cell. A total of 64 modules in ϕ are used for each cell while known pathological channels were excluded, and only laser runs taken with high gain readout are used (position 8 of the filter wheel in the laser system). The observed down-drift mostly affects cells at inner radius, that are the cells with higher current. The mean gain variation is corrected for changes in high voltage (HV). The HV correction affects mostly E3 and E4 cells since their HV was significantly decreased in 26th July 2017, from 750 to 700 V and from 750 to 650 V, respectively.

2.5.3 The Charge Injection System

The Charge Injection System (CIS) is designed to calibrate the relative response of the pulse readout electronics for all calorimeter PMTs and to monitor the variations with time. Each PMT channel has two analogue paths, the high and low gain (designed for a conversion factor of 82 counts/pC and 1.3 counts/pC, respectively), digitized by a 10-bit ADC, covering a range of 800 pC (corresponding to an energy deposition of about 700 GeV). Each channel is equipped with calibration capacitors, charged from a voltage source and discharged into the input electronics. The resul-

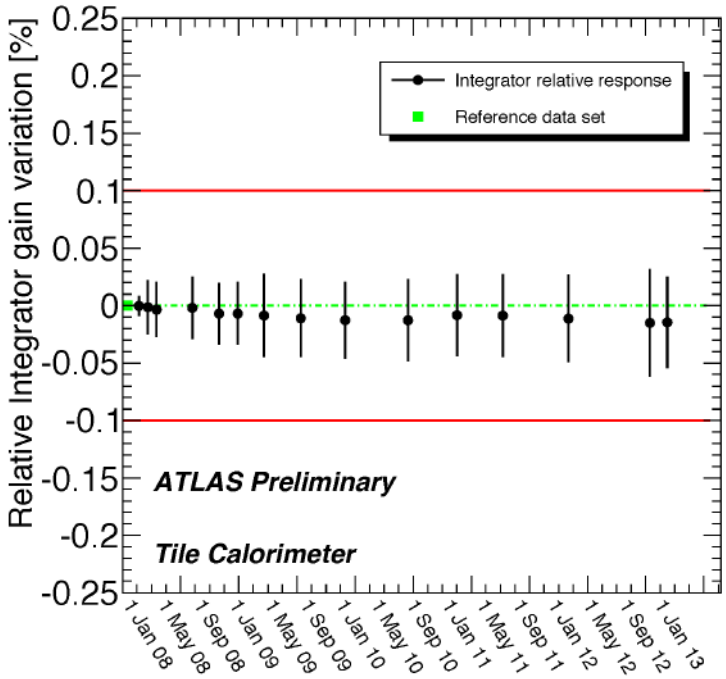


Figure 2.18: Relative variation of the integrator gain used by the Cesium calibration system as a function of time obtained by comparing the gains of all the channels of Tile. [14].

tant waveform is similar to the one produced by the PMT for a given charge, except for an amplitude 10 % larger and a Full Width at Half Maximum (FWHM) 10 % smaller. Dedicated CIS runs are taken twice per week when the beam is absent, scanning the full range of charges for both gains, allowing for the determination of the ADC-counts/pC ratio for each channel. Figure 2.17 represents the evolution of the high gain CIS calibration constants for the 2015 data taking period. The stability of the calibration constant is within the 0.7 % channel systematic uncertainty in the whole period.

2.5.4 The Integrator System

The Minimum Bias (MB) events in ATLAS are inelastic proton-proton collisions with low momentum transfer, whose rate is proportional to the LHC luminosity. These events produce a non-negligible occupancy of the TileCal cells, with rates uniform in the azimuthal angle and moderately dependent on the pseudo-rapidity. Since the MB current, averaged over milliseconds, is almost constant and propor-

tional to the interaction rate, it can be used to monitor the calorimeter response, the relative luminosity and the beam quality during physics runs. Dead and hot channels are also identified in MB data. For each PMT channel the anode output is DC coupled to an integrator circuit based in an operational amplifier. This has a configurable time constant between 10-20 ms and a gain selectable from six predefined values (as the MB current changes with the position of the cell on the calorimeter, as well as with the luminosity). All integrator outputs, multiplexed to a 12-bit ADC, are readout every 2 ms through a dedicated Controller Area Network (CAN) bus. This integrator system is also used to readout the cesium calibration data. The stability of individual channels in the system is better than 0.05 % whereas the average stability better than 0.01 % as presented in Figure 2.18.

Chapter 3

The ATLAS Tile Calorimeter

3.1 Detector overview

As discussed in Section 2.3.2, the ATLAS Tile calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS. The TileCal detector is a sampling calorimeter which uses steel as an absorber medium and the tiles of the scintillator as the active absorber. This calorimeter was designed to contain all the hadronic showers developing from the proton-proton collision and also to measure the energy of hadron, taus, and jets. It also contributes to the reconstruction of missing transverse momentum. The calorimeter covers the region $|\eta| < 1.7$ and is placed around the liquid argon EM calorimeter and as one barrel (LB) and two extended barrels (EB) parts. The LB is 5.8 m in length and the two EBs are 2.6 m each and they have an inner radius of 2.28 m and an outer radius of 4.25 m. Each barrel is divided into 64 wedged-shaped modules [17].

The scintillator tiles are placed radially and staggered in-depth and the structure is periodic along the z-direction. The tiles are 3 mm thick and the thickness of the iron plates is 14 mm. Wavelength Shifting (WLS) fibres readout the two sides of the scintillators tiles in two separate PMTs. In the mechanical structure of the calorimeter, the electronic and readout systems of the TileCal are well integrated, see Figure 3.1. All the Front-End (FE) electronics and the PMTs are mounted on aluminium units

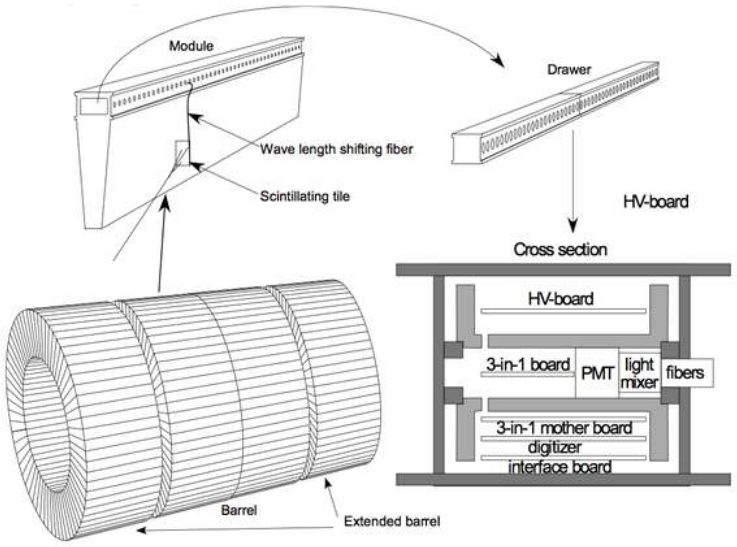


Figure 3.1: Mechanical structure of the TileCal [18].

called super-drawers and are located at the girder on the rear-end of each module. The FE electronics are powered by the low voltage power supply (LVPS) mounted on a separate steel box, also inserted inside the girder. The LVPS box has the same cross-section as the girder and it also contains the external connection for power and other services. The TileCal also contains three calibration systems namely the charge injection, laser, and a Cesium-137 radioactive source and such systems are used with good precision for calibrating signals on an electromagnetic scale.

3.2 Front-End Electronics

In this section we will briefly describe the components of the Front-End electronics, namely The Photo-Multiplier Tube (PMT) block, motherboards, digitizer boards, and interface board.

3.2.1 Photo-Multiplier Tube Block

The PMT block's main function is to transform the light signals from the scintillators into electrical signals. These electrical signals are then digitized by two separate analogue-to-digital converters (ADCs) with a gain ratio of 1:64. The PMT block has

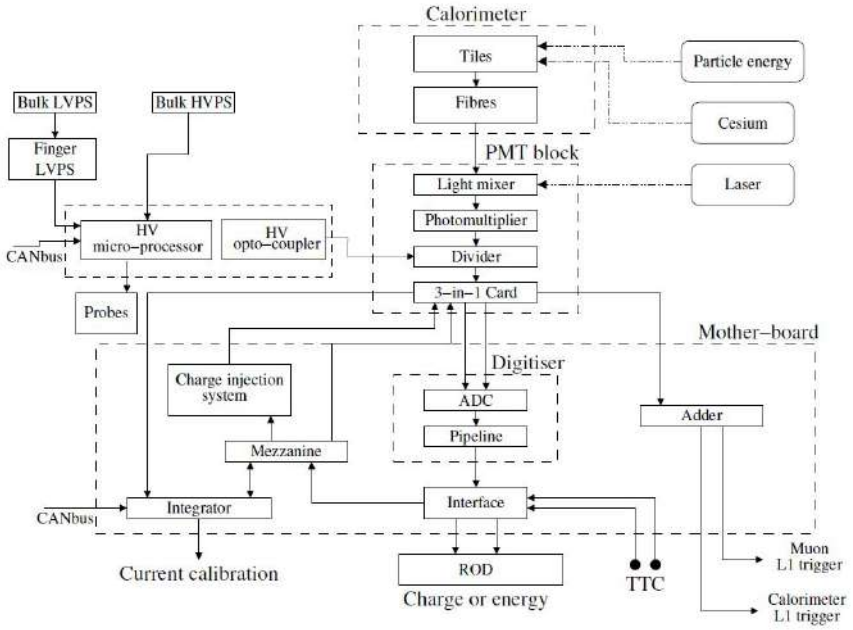


Figure 3.2: Schematic of the TileCal readout electronics [3].

a mechanical structure that comprises a steel cylinder made out of μ-metal shield for magnetic shielding. The main components of the PMT block are a light mixer, the actual photo-multiplier, a High Voltage (HV) divider, and the 3-in-1 cards, see Figure 3.3 [19]. The light mixer is an optical plastic insert and its main function is to uniform the light from all the readout fibres ensuring consistent illumination of the photocathode [20]. The photo-multiplier is a Hamamatsu model R7877 with an 8-dynode structure and is used to measure the light from the scintillators. The PMT also converts the light pulse from the fibre bundles into an electric charge. The light mixer is supported mechanically by a plastic element, which also isolates the PMT metallic package (connected to the HV). This support piece is made of high electrical resistant material (NORYL).

The HV divider is a device that is used to partition the high voltage between the dynodes of the PMT. The HV divider is a circular printed circuit board which is attached to the 3-in-1 card. The HV divider also serves as a socket allowing connection of the PMT to the FE electronics without any interconnecting wires. The advantage of this design is that the capacitance between the PMT and the rest of

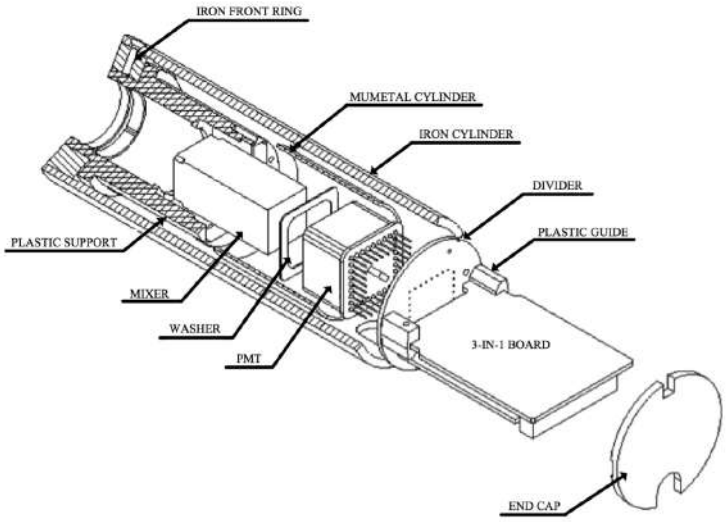


Figure 3.3: PMT block [18].

the electronics is minimized and this reduces noise and unreliable connections. The 3-in-1 card is a 7 cm by 4.7 cm printed circuit, which has the main functions to provide a high and low gain shaped pulse for the digitizer boards, the charge injection calibration system, and slow integration of the PMT signals for monitoring and calibration. The connector to the divider is a 90 degrees header. The connector for the digital control signals and power from the motherboards is a flat 34-position ribbon cable. The fast analogue output signal is brought out to the digitizing system using a different shielded twisted pair.

3.2.2 Motherboard

All the electronics in a drawer are held together by the motherboard. In a super-drawer, there are two motherboards. The motherboard provides power and TTC commands to the 3-in-1 cards, and each motherboard can host up to 4 digitizer boards and one interface card see Figure 3.2.

3.2.3 Digitizer System

The PMT blocks provide the signals to the digitizer boards. These signals from the PMT blocks are shaped and amplified by the 3-in-1 cards and these 3-in-1 cards

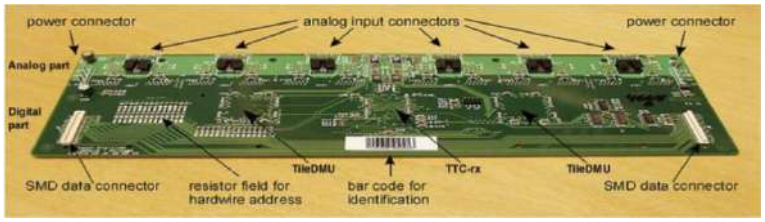


Figure 3.4: Digitizer board [22].

provide this system with two output signals, high and low gains with a gain ratio of 64. The digitizer boards digitizes the input signals every 25 ns through means of a 10-bit ADC, it does so by using a sample clock that can be adjusted collectively for all the ADC in steps of 106 ps. Each digitizer is equipped with two Tile Data Management Units (DMUs), which are a custom ASIC chips which temporarily stores the data in the pipeline memories. In each digitizer board, there are 12 ADC, that will read 6 PMTs, meaning that the digitized data from 6 ADC (3 PMTs) are sent to one DMU. The DMUs implements specific circuitry for the required pipeline with buffer memories, cyclic redundancy check (CRC), memory parity check, BCID and logical selection computations. There are 8 digitizer boards in each LB super-drawer that readout 45 PMTs and 6 digitizer boards in each EB super-drawer that readout 32 PMTs. The digitizer board is also equipped with a TTCrx chip that is responsible for system timing and programming. Figure 3.4 shows the digitizer board with its components. The motherboards are the base element for power distribution from the LVPS to the digitizer boards, the 3-in-1 cards, and the interface board.

3.2.4 Interface Board

The interface board is placed in the middle of the super-drawer and it receives the TTC optical signals and distributes them to the rest of the components inside the drawer. After receiving the L1A signal from the LVL1, the interface board receives digitized data from the digitizer boards. In each super-drawer, there's one interface board. The interface board encodes and transmit data through dedicated fibre-optical links to the Back-End (BE) electronics and receive TTC commands. This board also computes the CRC on input and output data streams that are used in BE



Figure 3.5: The Daughterboard version no 4. [23].

electronics to process data that is not affected by single event error and to perform online data quality checks [21, 22].

3.2.5 Trigger Board

The trigger boards are special trigger summation cards also called adder boards and are mounted on the motherboards of the super-drawers. The purpose of this board is to perform an analogue sum of the signals and sends two output signals (tower signal and muon output) to the LVL1 trigger system. Each board receives signals from up to 6 3-in-1 boards, grouped in projections of eta, that define so-called trigger towers. The tower signals comprise of the sum of all cells and the muon output contains only the last layer cell. The trigger boards also provide the sum of the signal in all four of the gap and crack scintillators. The muon output provides the signal from the scintillators and covers the region $1.2 < |\eta| < 1.4$.

3.3 Phase-II Daughterboard and Mainboard

The Tile on-detector electronics for Phase-II are housed inside the mini-drawers. Each mini-drawer contains up to 12 PMT blocks, each with a light mixer, a PMT, its active HV divider base and an amplifier/shaper card (3-in-1 card). These are then connected to a Mainboard that provides low voltage and controls to the 3-in-1 cards, digitizes their signals, and routes the data to the link Daughterboard, which handles all high-speed communication with the BE electronics PPr. The mini-

drawer also contains high voltage (HV) distribution cards that receive individual HV levels for each PMT via separate cables from a multi-channel off-detector HV supply.

The overall design emphasises reliability through redundancy and simplicity. In addition to the implicit redundancy facilitated by reading out each cell by two PMT channels, redundancy in the low voltage supply is facilitated by partitioning each mini-drawer into small independent units (half mini-drawers, sides A and B) to limit the impact of potential failures.

The 3-in-1 FE card amplifies the PMT signals with high and low gain (with a gain ratio of 32), sets gains, and provides charge injection calibrations. Another function is to integrate and digitize the current from minimum bias events or from a Cesium source calibration capsule that can be moved through the Tile cells using a hydraulic tube system. All raw data from each PMT will be digitized with an effective 17-bit dynamic range and sent to the off-detector electronics for both trigger processing and data acquisition. The 3-in-1 cards are built with discrete components and are a modified version of the present design with improved performance to linearity and noise level.

While most of the electronics drawer is shielded by the calorimeter steel, the services gap between the barrel modules has higher exposure, primarily from low energy neutrons. This presents a challenge for the design of the LV power supplies located in this region. Other electronics sensitive to radiation effects are located on the Mainboard and Daughterboard deeper into the mini-drawer where the radiation dose is lower. The on-detector FPGAs must be radiation tolerant and supported by efficient error mitigation strategies. Persistent data errors will be interpreted as a corruption of the configuration of the corresponding FPGA and thus force a reconfiguration either locally from an on-board flash memory or remotely from off-detector configuration source.

The off-detector PPr, sends Detector Control (DCS) and run-control data via two 4.8 Gbps optical links to GigaBit Transceiver protocol chips (GBTx) on the Daughterboards, which also extract and distribute the low jitter system clock. The Daughterboard, in turn, sends readout and DCS data back to the PPr over two duplicated (i.e. total 4) optical links running at 9.6 Gbps. Four electro-optic service (SFP+) modules provide the electro-optic translation. The fact that the duplicated uplinks are both connected to the PPr allows a failed link to be compensated immediately. The redundancy and the GBT protocol with Forward Error Control (FEC) helps to guarantee a high level of transmission reliability

3.3.1 Daughterboard

The Daughterboard is the on-detector interface between the FE and the counting room. It is connected via multi-gigabit optical links with the off-detector PPr, which sends DCS and run configuration data to the Daughterboard over 4.8 Gbps links. The Daughterboard, in turn, transmits detector readout and DCS data to the PPr over 9.6 Gbps links. Redundant optical fibres and electro-optic modules are used for protection against single link failures, and like the Mainboard, the Daughterboard is also divided into independent sides for additional redundancy.

The Daughterboard [23] has undergone several revisions and adapted to evolving specifications and component choices. The present version, version 5 is a modification of version 4 [24], which has already satisfied all functional and performance requirements for the Tile upgrade and was adapted to serve all three FEB alternative solutions. Version 5 includes a more modern FPGA technology (Xilinx Ultrascale+), which offers improved link performance margins and higher radiation tolerance than the earlier Kintex7 devices. The new version also replaces the two QSFP+ modules in previous versions to four SFP+ modules with multi-mode optical fibres. Apart from these and a few other new components, the version 5 design uses as many



Figure 3.6: View of both sides of the prototype Mainboard for the 3-in-1 FE system. [25].

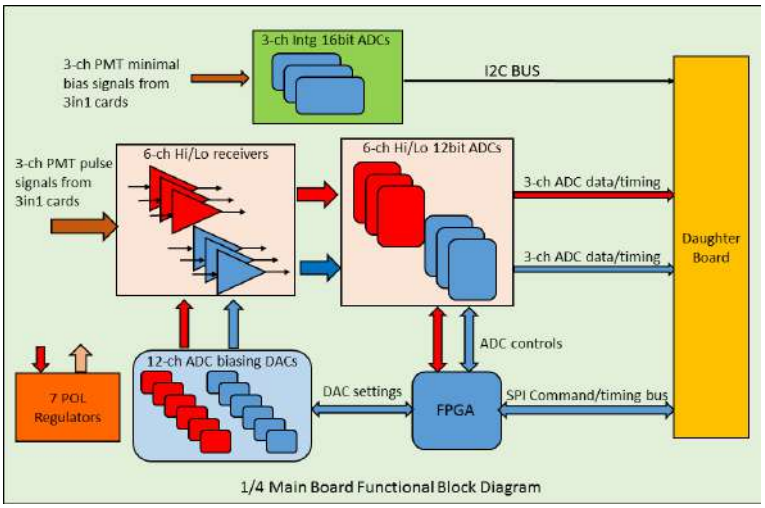


Figure 3.7: Functionality diagram of the Mainboard. [25].

components and schematic features from revision 4 as possible.

The Daughterboard version 4 (Figure 3.5) uses a 16 layer PCB of the size 280 mm x 100 mm. All six signal layers are adjacent to ground planes on both sides, and the high-speed signals are routed in the inner layers. The power planes are grouped in the middle of the stack. The two sides are independently powered by redundant 10V from the Mainboard. The power distribution network with local Point-Of-Load regulators eliminates power drop problems. To decrease the jitter of the FPGA internal clock nets to the lowest possible level additional power supply filtering were implemented. This was especially important for the 1 V core supply to the transceivers. Much effort has been spent to route related signals to same I/O banks.

3.3.2 Mainboard

A prototype Mainboard [25] is shown in Figure 3.6. The Mainboard measures 690 mm by 100 mm. Since 6 PMT signals are routed in from each side, Mainboard layout is physically divided into two sections called the A-side and B-side. The two sides' electronics are completely independent, with each side having its own +10V LVPS supply brick to power the electronics. To prevent failures caused by LVPS brick trips or total failure, the two sides are "Diode-Or"'ed to make a redundant power supply.

The Mainboard electronics is grouped into 4 sections served by each FPGA. The logic diagram of the electronics in one of these sections is shown in Figure 3.7. To support the 3 PMTs in a section there are 6 channels of 40 Msps 12-bit ADCs and 3 channels of 50 KHz 16-bit ADCs for the slow integrators. An Altera Cyclone EP4CE10F17 FPGA controls low gain and high gain ADCs, including input bias voltage levels. The FPGA can also generate ADC test patterns for better data alignment.

The other functionality of the FPGA is to serve as a communication hub between FE cards and Daughterboard. The FPGA in a section on a Mainboard communicates to the Daughterboard with a dedicated SPI port. Two timing signals (TPH and TPL) that initiate the low gain and high gain CIS calibrations are also provided. The digitized data from the low gain and high gain channel are sent to the Daughterboard on a dedicated serial bus without FPGA's involvement. The integrator ADC data is readout directly by the Daughterboard via a standard I2C bus. Note that the serialised data is not routed through the FPGAs; the design strategy is to minimise the use of FPGA control in normal operation, thereby making the system more robust against single event upset (SEU). In the event of SEU, the FPGA is used to reconfigure and clear the soft errors.

3.4 Back-End Electronics

The Back-End (BE) electronics is organized in four partitions, two servicing the readout of the LB (LBA and LBC) and the other two servicing the readout of the EBs (EBA and EBC), see Figure 3.8 (a). The TTC and ReadOut Driver (ROD) units are equipped on each BE partition. These units are physically split into a 6U Versa Module Eurocard (VME) TTC crate and a 9U VME and readout crate called the ROD crate. The TileCal BE electronics racks are shown Figure 3.8 (b). The TTC and ROD for side A of the detector are contained on the left rack with LBA on top and EBA on the bottom and the TTC and ROD for side C are contained on the right rack with EBC on the top and LBC on the bottom. In the centre rack we have the TTC Optical Coupler (TTCoc) that splits the TTC optical signals from 1 to 32 links [26]. The BE electronics racks also house the FE optical links, and all TTC and readout links from the detector are connected to the back of the patch panel. The Single Board Computer (SBC) controls each of the creates and they are powered and monitored by the DCS.

In the Tile HL-LHC data acquisition architecture the PMT digital samples are transferred to the PPrs for every bunch crossing. The data in the PPr is stored in pipeline buffers waiting for the trigger decision. Parallel to the trigger system, the PPr provides reconstructed data at 40 MHz. According to trigger system, the reconstructed information includes calibrated energy per cell or group of cells. The PPr system provides multiple copies of the data for those parts of the detector where the area used in the trigger algorithms overlap. After the trigger decision, the selected data events are transferred to the FELIX system which is the core element of the central ATLAS DAQ system.

In order to have more flexibility and reduce the complexity of the designs, the communication with the FE and the trigger and data acquisition functionalities are located in different electronics modules. The interface with the FE electronics,

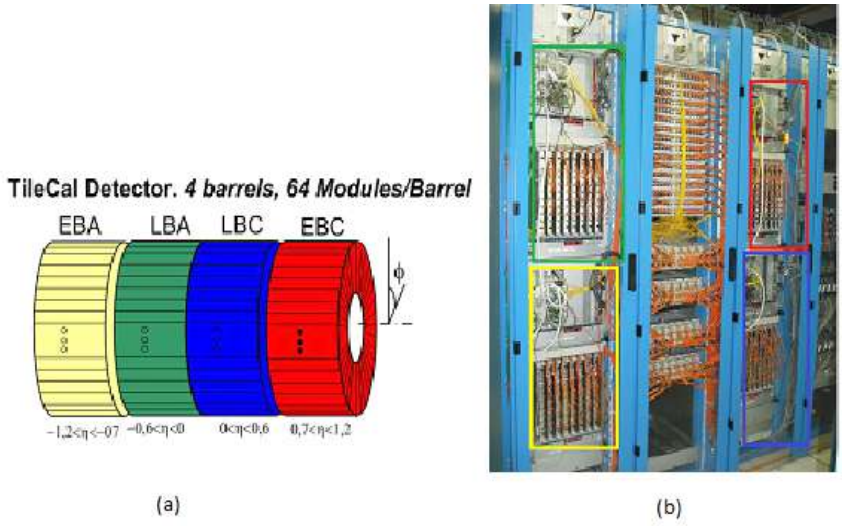


Figure 3.8: (a) Partitions of the TileCal. (b) Back-End electronics rack.

pipeline buffering and signal reconstruction are implemented in the PPr Advanced Telecommunications Computing Architecture (ATCA) blade, while construction of the trigger primitives and the interfaces with the trigger and FELIX systems are performed in the Trigger and DAQ interface (TDAQi) system.

3.4.1 Tigger, Timing and Control Modules

There are 9 TTC modules for the BE electronics, see Figure 3.9. The TTCvi, TTCprr, and the Laser ReadOut modules are described next.

The ATLAS Trigger, Timing and control VME bus Interface Module

The ATLAS Trigger, Timing and control VME bus Interface (TTCvi) module is used to configure the FE electronics and interfaces the local TTC system to the global TTC system. The TTCvi provides A and B channels signals to the TTC transmitters for multiplexing, encoding, optical conversion and distribution to the TTCrx chips associated with the FE controllers [26]. The channel A is used to transmit the Level 1 Accept (L1A) signal. A programmable L1A source selector and an internal trigger emulator are Incorporated by the TTCvi. This internal trigger emulator is used for tests purposes. The channel B is used to transmit framed and formatted commands and data, which can be synchronous or asynchronous concerning the LHC clock [27].

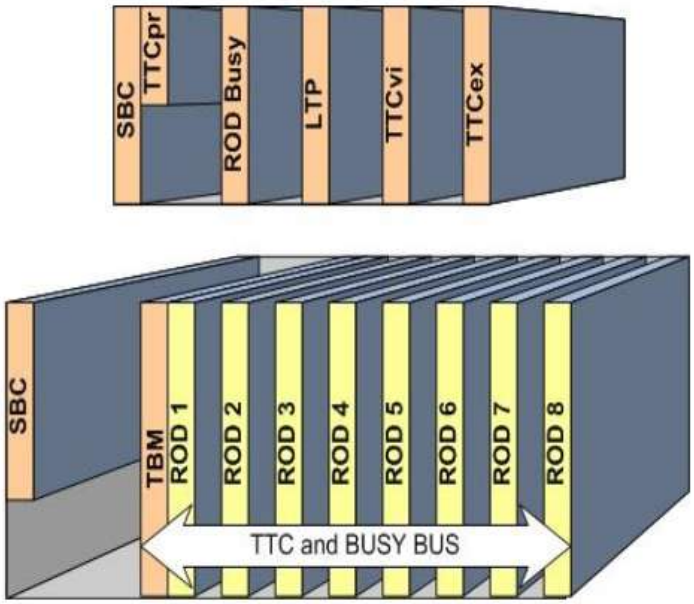


Figure 3.9: TTC and ROD VME crate modules of TileCal BE electronics partitions.

The ATLAS Trigger, Timing and control Reciever in PMC form factor

The ATLAS Trigger, Timing and control Reciever (TTCprr) card is plugged into the SBC of the TTC crate and is used to make available the TTC information in the TDAQ framework for calibration runs. The TTCpr provides event ID, bunch crossing ID, and Trigger Type for each event in the data records. The busy signal which is connected to the ROD Busy module as mention above is provided by this specific card.

Laser ReadOut Driver Module

The Laser ReadOut Driver module is also a 6U VME module used to provide information from the Laser calibration system into the data-flow and furnishes the TTC signals to the Laser system. The Laser ReadOut Driver driver is equipped with a High-speed Optical Link (HOLA) card [28]. The HOLA card is used to provide data fragments to a ReadOut Buffers of the ReadOut System of the LBC partition through a ReadOut Link [29]

3.4.2 ReadOut Modules

This section gives a brief description of the ReadOut modules.

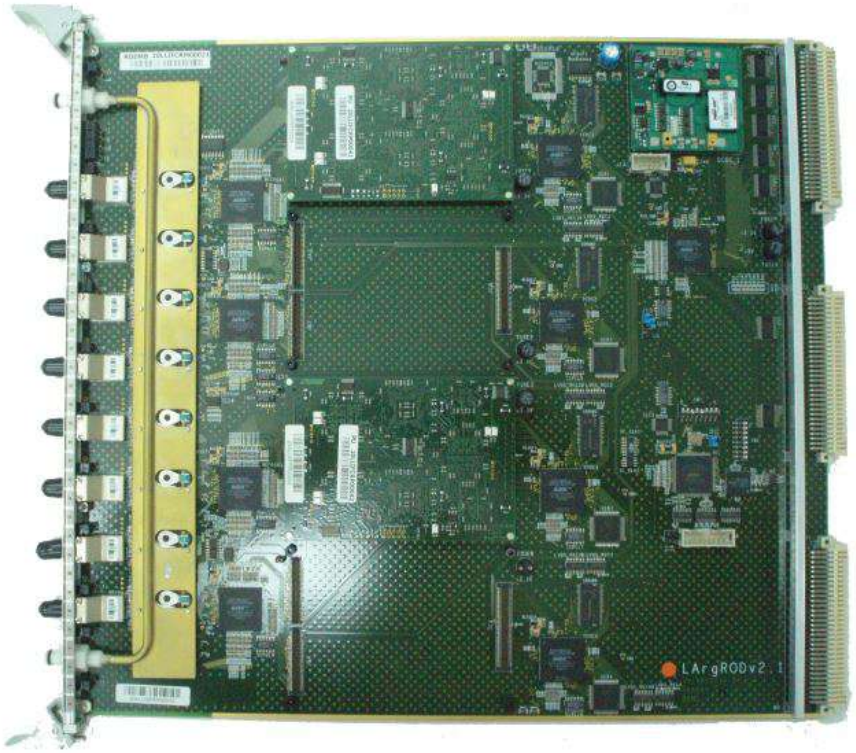


Figure 3.10: ROD Module [18].

Trigger and Busy Module

The Trigger and Busy Module (TBM) is a 9U VME module for the ReadOut Driver (ROD) crate and it is received TTC signals from the local TTC system using an optical link [30]. The signal received by the TBM is propagated to each ROD module via the P3/J3 connector, using the CP3 plane in the ROD crate. The TBM module also provides a busy signal to the ROD Busy module as well as to gather the busy signals through the CP3 from the eight RODs in the crate.

The ReadOut Driver Module

The ReadOut Driver (ROD) module is a 9U VME module that receives data from the super-drawers. The data from the super-drawers is received through eight FE links, with each corresponding to one super-drawer, see Figure 3.10. The ROD module is equipped with four Processing Units (PUs) that are used to compute the

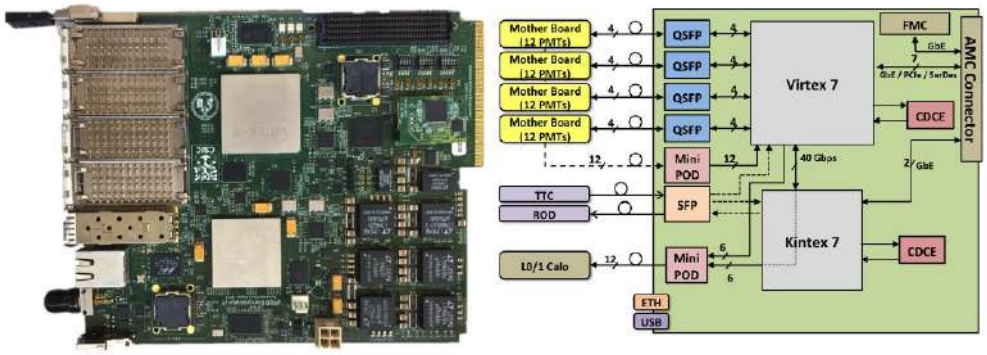


Figure 3.11: Picture and block diagram of the PPr demonstrator module. [34].

time and energy of each readout channels, and its coupled to a Transition Module (TM) [31]. The TM is placed behind the ROD, and it receives data fragments through the P2 and P3 connectors of the VME crate. The TM is also equipped with two HOLA cards which transmit data fragments to the ReadOut System (ROS) through the ReadOut Links (ROL). In the ROD crate, eight RODs are installed.

Optical Multiplexer Board Module

The Optical Multiplexer Board (OMB) module is a 9U VME module used to provide the correct data to the ROD input in case there is an error in one of the output links. The OMB corrects data to the ROD input by analysing the CRC of the data packets on both fibres coming from the FE. This 9U VME module selects data from one of the two outputs links and transfers it to the ROD. The OMB module is also used to inject data to the ROD for test purposes.

3.4.3 PreProcessor System

The Phase-II PreProcessor module is implemented in a full-size ATCA blade format. The basic interfaces with the ATCA backplane and the power distribution are located in a Carrier Base Board with up to four slots to host Compact Processing Modules (CPM). The single wide Advanced Mezzanine Card (AMC) CPMs includes high speed optical connections to communicate with the FE electronics, one FPGA

and interconnections through the Base Board to communicate with the TDAQi implemented as an ATCA Rear Transition Module (RTM). Each CPM can process the data from 8 mini-drawer (2 Tile modules), thus 32 PPr systems are needed to readout the entire detector. The Zone 3 ATCA connector provides point to point connections to Quad Small Form-factor Pluggable (QSFP) connectors in the TDAQi to communicate with the FELIX system and to the Trigger FPGA. The data received from the detector is processed in real-time and calibrated energy and time per cell for every bunch crossing are transferred to the Trigger FPGA in the TDAQi. In parallel, the data are stored in pipeline memories in the CPM FPGAs. The data corresponding to the events selected by the trigger (LVL0 or LVL1 depending on the final ATLAS trigger structure) are extracted from the pipelines and transmitted to the FELIX through the TDAQi module.

One key issue is the selection of the FPGA model according to the resources required to implement all these functionalities. A total of 46 Multi-gigabit transceivers are needed to communicate the PPr with the FE, FELIX, TDAQi and the ATCA backplane. A total of 3 Mbit of internal memory blocks are required for the implementation of pipeline memories in the worst-case scenario of a single pipeline with a length of 35 μs. The low latency trigger signal reconstruction algorithms require a total of 1152 Digital Signal Processing (DSP) blocks (12 per channel). Besides, roughly 200,000 logic cells are needed for all the other functionalities of the FPGA. These estimations have been made using the results from the demonstrator PPr module and represent the minimum resources only for the main functionalities. Except for the number of transceivers that are fixed, a factor of 2 is applied for the required DSP, memory and logic cells resources. One candidate for the CPM FPGA is the Xilinx Kintex Ultrascale (XCKU115) which includes up to 52 Multigigabit Transceivers, 1.4 Million of logic cells, 75.9 Mb of internal memory and more than 5,000 DSP slices. The ATCA backplane (Zone 1 and Zone 2 connectors) is used for power distribution, control and board health management, remote FPGA program-

ming, system configuration and data monitoring.

The ATCA standard [32] has been selected by the ATLAS collaboration to replace the VME standard [33] as the basis for modular electronics for the upgrade. In the final system the PPr module has an ATCA blade form factor and it is installed in different ATCA shelves. The baseline is to keep the current partitioning with four shelves (two for the central barrel and two for the extended barrels) housing 8 PPr blades each. The ATCA framework allows intelligent monitoring and control while offering high-speed connectivity via a 40 Gbps backplane. The CPMs and TDAQi include a Modular Management Controller (MMC) that provides the operation of the basic services when connected to the ATCA system using the Intelligent Platform Management Interface (IPMI) protocol. The MMC manages the power connection of the CPMs with the Base Board and monitors the temperature sensors on the board. The Base Board provides the final connection to the ATCA IPM-Bus through an IPM-Controller (IPMC) which is implemented using a common solution for all the ATLAS ATCA blades.

The PPr demonstrator represents a reduced version of the final PPr system including the Base Board, CPM and TDAQi functionalities in a double mid-size AMC as shown in Figure 3.11. This board can be operated in an ATCA carrier or a Micro Telecommunications Computing Architecture (mTCA) crate. The stack-up has been designed to fulfil the high-speed design specifications and constraints. The Printed Circuit Board (PCB) is formed by16 layers, divided into 8 layers for power and ground planes and 8 layers for signals with a total thickness of the PCB of 1.6 mm, compliant with the AMC standard. The core processing of the PPr prototype is composed of two Xilinx series 7 FPGAs: one Virtex 7 (XC7VX485T) and one Kintex 7 (XC7K420T). These FPGAs provide high connectivity bandwidth, high-density logic resources and dedicated DSP slices resources for the implementation of signal processing algorithms. A third FPGA, a Xilinx Spartan 6, is used for slow

control and monitoring of the jitter cleaners, clock management units, QSFP and MiniPOD modules and supervisory power chips.

The Virtex 7 operates the Tile module through four QSFPs using 16 asymmetric GigaBit Transceiver (GBT) [35] running at 4.8 Gbps for the downlink (PPr to FE) and 9.6 Gbps for the uplink (FE to PPr). Detector Control System (DCS) commands and Trigger, Timing and Control (TTC) information are encoded and transmitted to the downlink at a data rate of 4.8 Gbps using the standard GBT protocol with Forward Error Correction (FEC). In the front-end electronics the Daughterboard decodes and executes the received commands, sending an acknowledgement receipt to the PPr. The PPr demonstrator module consumes a maximum of 60 W with the default firmware running on both FPGAs. This is compliant with the ATCA standard in terms of power distribution and cooling. Nevertheless, a heat sink is mounted in the FPGAs when the PPr is operated in the ATCA chassis. A fan is attached to the heat sink when the PPr is operated with no external air cooling.

3.5 The ATLAS Online Software

Online software is in charge of the overall experimental configuration, control, including run-control, and the monitoring of TDAQ systems and management of data taking configuration. Online Software is implemented such that it allows several types of users that can be grouped into two categories, one being the TDAQ operator and the other the TDAQ developer/expert. In the Online Software, several user interfaces are provided for both operational levels. The Online Software is considered to be the glue that holds the various sub-systems together, and also provides a uniform control interface, and the ability to easily hide the specifics of those sub-systems so that they can be provided with control services. It was developed with strong distribution, scalability, flexibility and modularity need as a customizable framework, hence it does not contain any specific sub-systems components. The TDAQ system is defined as a collection of applications running on a set of

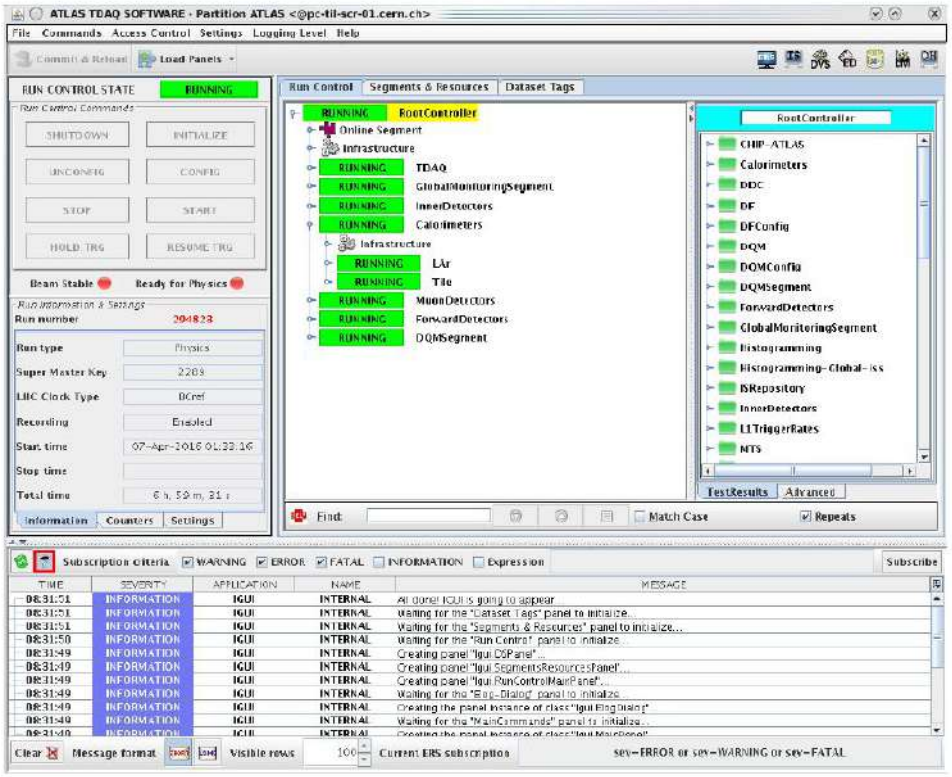


Figure 3.12: The Graphical User Interface (GUI) of the ATLAS TDAQ Partition in the state running.

hosts and it is modelled around a common Finite State Machine (FSM) that defines well-defined states and transition and also hides the complexity of the individual components. The TDAQ is best described through the services of the configuration database.

The configuration database is a service that includes the overview of the TDAQ system and information about the detector which include run parameters, software, hardware and partitions. The TDAQ description information is collected in a form of configuration for different run types which include calibration, physics, debug, etc. This configuration database service is employed by the sub-detector experts to develop their configuration parts and to write the code configuring their applications using a common configuration service tool. Also this configuration database service has implementations based on the Object Kernel System (OKS) [36]. The OKS is an object manager that is persistent in-memory and its primary storage is

an XML file. For this configuration database services, there are two types of XML files being used, one being the data file used to store database objects and the other is the schema files that define classes. In ATLAS the starting point that describes a TDAQ configuration is the Partition, which is the synonym for data taking configuration and it is essentially an object of the configuration database where all the configuration of the software and hardware elements is spanned. Two or more partitions can run in parallel provided that they use distinct or sharable resources. A Partition contains several Segments. Segments are the modular parts of the TDAQ system which can be included or excluded as a whole from one or more Partitions. In ATLAS there is one Segment for each sub-detector see Figure 3.12. A Segment can be divided into as many segments as there are TTC partitions. In TileCal there are four TTC partitions (EBA, LBA, LBC, and EBC). Starting from the Partition, we thus have a nested tree of segments and this tree matches one-to-one to the Run Control (RC) tree, i.e. every Segment is controlled by one controller application. A Segment is associated with a set of hardware components and software application and a Segment can contain other segments. The four TTC partitions are defined as segments inside the TileCal Partition which itself is referenced as a Segment in the main ATLAS Partition. The Partition can be ran using the following basic services which are: Resource Manager (RM), Access Manager (AM), Process Manager (PMG), Inter-Process Communication (IPC), Information Service (IS), Online Histogramming (OH), Error Reporting System (ERS), and the Integrated Graphical User Interface (IGUI). Detailed information for each service is described in the ATLAS TDAQ monitoring working group website accessible from [37].

3.5.1 Tile Calorimeter Online Software

The TileCal Online software is the set of TDAQ software used for the operation of TileCal which is not provided by the ATLAS TDAQ online software. It is basically an extension of the ATLAS TDAQ software which provides TileCal detector specific software for the BE electronics, infrastructure for calibration systems, monitoring

(including hardware), and the diagnostic and verification systems tests (DVS). One of the core components of the TileCal Online Software elements is the BE electronics ROD Crate DAQ (RCD). It is supported by the ATLAS Data Flow policy for which the TileCal Online software provides plug-ins. This keeps the programming efforts focused on specific hardware handling since the core software is centrally managed [44, 39].

The RCD is an extension of the ROS software that provides a complete framework for implementing DAQ functionality between ATLAS system specific electronics and the DAQ system common parts boundary. It allows the use of common services (such as data output and monitoring channels) together with dedicated libraries for control, monitoring, event building, DAQ and emulation of detector specific electronics. The application employs four specific runtime (dynamic) plug-in types to implement the different I/O protocols [40]. The RCD is an RC application and it reacts to the FSM transition commands initiated by TDAQ user through the GUI.

3.5.2 Tile Calorimeter Online Software run types

In TileCal there are six different runs; five are calibration runs, the last being the physics run. A brief description of the run types is presented next. For physics and calibration runs the detector configuration is different. The type of calibration runs requires the storage charge value that is sent to the FE electronics, together with the data from the RODs.This calls for additional elements to be included in a readout that slows down the acquisition rate. Therefore, the calibration configuration is not feasible for physics runs. All run types are taken using the 7 samples window at a readout window of 25 ns * 7 = 175 ns. The runs are either bi-gain: both ADC gains are readout for each channel, or mono-gain: only one ADC gain is read-out per channel. The gain is chosen automatically by the DMU based on the 2 following criteria:

- High Gain overflow: if the number of ADC counts in HG is 1023 for at least 1 of the samples, then the gain is switched to LG.

- High Gain underflow: if the number of ADC counts in HG is 0, then the gain is switched to LG.

In ATLAS, the DAQ-Experts or the shifters in the sub-detector take calibration runs which must be examined offline before physics analysis to validate data quality. The TileCal standalone offline frameworks automate this process, though shifters are necessary to evaluate the results. The Data Quality Validator (DQV) and the Data Quality Leader (DQL) are the shifters responsible for performing this analysis and recording the results.

Calibration runs:

- Pedestal: This is a bi-gain calibration to monitor noise without a signal for the electronics. It is used to check the detector noise level and the integrity of the data.

- Charge Injection Scan (CIS): This is a bi-gain calibration run that yields the ADC count/pC conversion for each channel. A DAQ ramp is performed for each of the two capacitors (5 pF and 100 pF). For each DAQ step the timing is varied. This run scans the entire TileCal electronics range, checking the correct ADC linearity, DAC settings control, and finding stuck bits and data integrity problems.

- Mono CIS: This is a mono-gain calibration run in which a constant charge is injected to monitor electronics stability. This run is aimed at checking the correct response to ADC, find gain switching, the timing of the motherboard and problems with data integrity.

- CIS ramp: CIS is fired with a configurable pattern and data is read-out in physics mode for Optimal Filtering reconstruction validation.

- Laser: This is another mono-gain calibration run in which a Laser light is injected into the laser fibers to make sure there are no dead PMTs/fibres and to calculate PMT gain and timing. The purpose of this run is to verify the correct response of the PMT, find gain switching, digitizers timing, and data integrity problems.

Physics runs:

This a mono-gain run with ATLAS setup and TileCal included as a segment running in the combined partition. The L1A is obtained from the CTP through the LTP. During commissioning, it is used to take cosmic data. The response of the cells to muon energy deposition is measured. Various offline controls may be carried out by cell and track reconstruction through the TileCal detector concerning energy deposition.

Chapter 4

Testing of the Front-End readout system

During LS2, the Front-End electronics of the TileCal have to be serviced, due to failures and non-performant components. In some cases these damages can be associated with radiation damage (neutron displacement) but in other cases, they are just spontaneous failures. This could be related to the non-compliant specifications of the components used in the electronics, or to the lack of better alternatives. Every single TileCal super-drawer is extracted from its position and inspected in-situ with MobiDICK [41] during the LS2. Defective components replaced and inspected in the surface laboratory at CERN. The author is responsible for testing all the components that came out from ATLAS between 2018 and 2019.

4.1 The MobiDICK System

The MobiDICK system is designed to check the integrity of the TileCal super-drawer during the CERN maintenance periods. The first version of the MobiDICK was ready in May 2003 for the delivery of the first production of super-drawers. The second or upgraded version of the MobiDICK system was delivered in March 2005, and this upgraded version included a new system to provide a high voltage input to the super-drawer and an LED driver to be able to study the response of the super-



Figure 4.1: A picture of the old version of the MobiDICK.

drawer to light pulses. The third version of the MobiDICK was delivered in 2007, and this version was able to test all the functionalities of the super-drawer. This version was fully contained in a custom aluminium box which had a width of 50 cm, a depth of 33 cm and a height of 41 cm. It also had three fans for cooling, a custom VME crate and a laptop, see Figure 4.1. The total weight of the box including the crate and the electronics boards is approximately 20 kg. The box can be connected to the super-drawer via single custom multi-connector cable and an optical fibre. The system is controlled by software running on the embedded laptop which acts as the user interface. The current MobiDICK system, the MobiDICK-4 system, is used as a substitution to the VME system (crate and modules) and it contains programmable logic. The embedded system together with the programmable logic and custom made PCBs emulates the functionality of the VME modules. For the simplicity of the design, a Field Programmable Gate Array (FPGA) evaluation board has been preferred to be used as the core of the system rather than designing from scratch a custom FPGA-based board. In the new system, the weight the MobiDICK is about 20% of the weight of the previous MobiDICK and the volume has been halved. This



Figure 4.2: A picture of the current version of the MobiDICK.

system is still mounted on a custom aluminium box which provides a robust tool suitable for use during maintenance periods. This box has a height of 20 cm, a width of 40 cm, and a depth of 35 cm, see Figure 4.2. The embedded system has a total weight of 4 kg. The new system contains a forced-air cooling system that reduces the possibility of thermal failures of the electronics.

4.1.1 The MobiDICK Hardware

The hardware part of the current MobiDICK system can be divided into four parts namely: the motherboard, ADC board, High Voltage and LED driver board, and the CAN bus. A brief description of each component is given:

Motherboard

The MobiDICK-4 system uses the Xilinx ML507 evaluation board as the motherboard of the system. The Virtex-5 FPGA with a PowerPC 440, built-in gigabit transceivers and programmable logic, is eligible for the Xilinx ML507 evaluation board. This evaluation board includes a 10/100/1000 Ethernet port, a DDR2 memory slot and a compact-Flash configuration for the configuration of the embedded

system. This module incorporates all the Back-End electronics of TileCal described in Section 3.4 in a single board. In particular it implements the Hamilton encoding of the TTC, at firmware level

ADC board

The analogue trigger and muon outputs of the FE electronics are digitized by the ADC board. This custom ADC board includes two Texas Instruments ADC 12-bit ADC chips that digitize 16 input channels at a 40 Mbps sampling rate. This board's digitized data is sent to the ML507 using the expansion ports at 480 Mbps each via the 16 LVDS channel.

High Voltage and LED driver boards

We have two different custom boards revamped from the old high voltage and LED VME card in this version of the MobiDICK, and they are the HV power supply board and the LED driver board. During testing, the HV power supply board used to supply the HV to the PMTs and the LED driver is used to generate the 20 ns wide LED excitation pulse during testing.

CAN bus

The HVmicro board, which set high voltage for feeding PMTs and the ADC-I board that provides current PMT integration data, uses two commercial CAN-bus dongles. The two serial ports of the ML507 board control these CAN-bus dongles.

4.1.1.1 The Embedded system

In the embedded system, the PowerPC 440 processor is the core of the system and is built into the Virtex-5 FPGA. The Virtex-5's logic resources are used to implement the various IP cores connected to the PowerPC processor. These IP cores

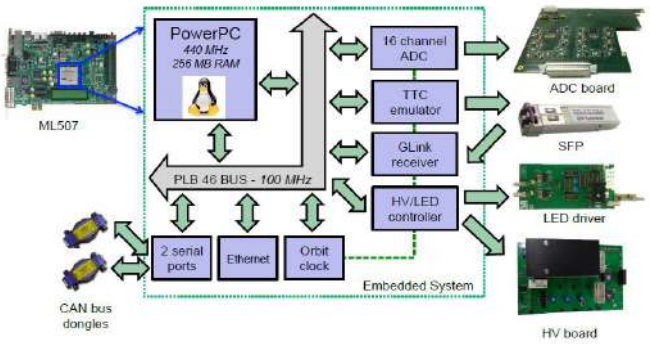


Figure 4.3: Sketch of the embedded system of the MobiDICK-4 test-bench [42].

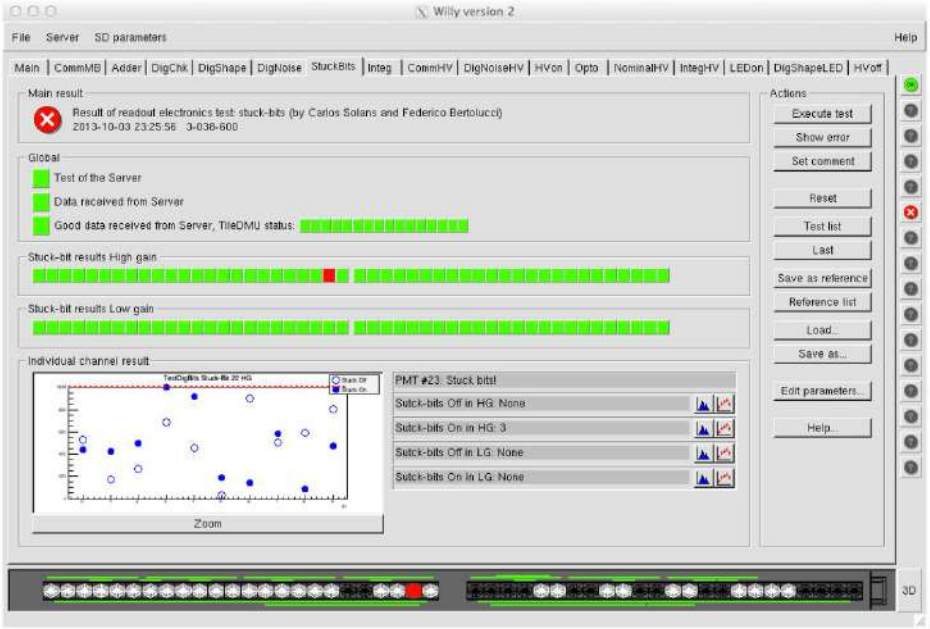


Figure 4.4: The Willy GUI showing the Stuck bits test [44]

are connected via a 32-bit Local Bus Processor (PLB) to the PowerPC processor as a slave device. The embedded system was developed with the version 13.1 of XIlinx ISE and EDK. Figure 4.3 shows a diagram of the complete embedded system. For more description of the IP cores check [42].

4.1.1.2 The MobiDICK Software

The same architecture from the previous system has been maintained on the new version of the MobiDICK and it has the ML507 as the server and the embedded laptop as the client. The Willy software is a custom ROOT [43] based GUI appli-

cation from the previous MobiDICK was used to handle the various tests required to send commands to the server, which checks the rest of the hardware, the certification, extracts and processes data and transmits the data back to Willy. The tests are implemented as tabs to the main panel and the results are stored in a local database.

4.1.2 Tests Performed by the MobiDICK

Seventeen tests can be performed by the current version of MobiDICK and these tests provide the functionality to certify the FE electronics. A brief description of the tests performed by the MobiDICK is given below:

Communication with Motherboard (CommMB) test

This is the first and most basic test of the super-drawer readout side performed by MobiDICK. The purpose of this test is to check the communication with the ADC-I card, the 3-in-1 card and the motherboard TTCrx (mezzanine card). This test also checks the serial number of the different boards and compares it with the ones stored in the Willy database for the corresponding super-drawer. The Willy database contains information of super-drawers. This database contains information about the serial numbers of different boards for each super-drawer.

Adder test

The purpose of this test is to manage the readout of analogue signals coming from the adder boards using the ADC board. It does so by using the Charge Injection System (CIS) which generates analogue signals.

Digitizer check (DigChk) test

This test has the purpose to validate from the digitizer to the optical links the complete digital readout chain. Digitizers are configured to transmit various data patterns in this test, and this data is received by the interface board and sent via the SFP fibre using the G-Link protocol.

Digitizer pulse shape test (DigShape)

The purpose of this test is to check the digitizer's functionalities and the data readout using the CIS in the 3-in-1 cards. A capacitor in the PMT output is charged with a programmable charge, and the resulting signal is then digitized and transmitted via the optical fiber to verify the electronics ' proper response.

The Digitizer Noise (DigNoise) and The Digitizer Noise with HV (DigNoiseHV)

The purpose of these tests is to measure the digital noise and also to check the data integrity. In the DigNoise test the signals of the non-powered PMTs are digitized and read out using the SFP fibre through the interface board. In the DigNoiseHV test, the noise levels are measured with the HV power supply supplying the PMTs. In this case there is an increase in the noise levels from the PMTs and this increase is taken into account when the check is performed.

Fast test

In this test the MobiDICK sends to the FE electronics L1A triggers with a data rate of 100 kHz checking the validity of incoming data with the G-Link IP core CRC module in real-time.

Digitizer stuck bit test

The purpose of this test is to configure the digitizers to transmit various patterns of data to detect stuck bits at high and low logic values, then produced data is checked.

Integrator readout test (Integ) and Integrator readout test with HV (IntegHV)

The purpose of these tests is to check the linearity and noise levels of the ADC-I and of the CIS in the 3-in-1 cards. In the Integ test, the CIS transmits a pre-programmed signal to the ADC-I board which is read out using the CAN bus interface. Then in

the IntegHV the Integ test is performed with the HV feeding the PMTs switched on. Also in this test the increase in noise is expected and considered in the performed checks.

Communication with HV (CommHV)

In this test the status and the communication with the HVmicro board is checked. It does so using the CAN bus interface.

HV regulator test (NominalHV)

During this test the voltage set stored in EEPROM of the HVmicro board is checked with the database on Willy. The EEPROM is read out using the CAN bus interface. In this test, the status and the communication with the HVmicro board is checked. It does so using the CAN bus interface.

Communication with HVOpt test (Opt)

The purpose of these tests is to check the functionalities of the high voltage distribution electronics in the FE electrons using the CAN bus interface.

LED test

The aim of the LED test is to test a light pulse with a known shape for complete read-out chain injection through a dedicated fibre into the PMTs. The digitized data is read using the SFP module and its integrity is checked.

4.2 Tested Components and Results

For this study the tests that were performed during the maintenance period by the author are CommMB, Adder, DigChk, DigShape, DigNoise, and fast test. Figure 4.5 shows a picture of the MobiDICK connected to the super-drawer during testing. For this study only one super-drawer was used, but components from other super-drawers were used.



Figure 4.5: The MobiDICK system connected to the super-drawer during testing of the components

The first test that is performed is to check if there is communication between the MobiDICK and the super-drawer being tested. This is achieved by using the CommMB test on the embedded laptop connected to the MobiDICK. In this test the communication with the ADC-I card is established, through the CAN bus, using the IDALLOC DEFID command. In case of success the serial number of this card is read back and the parameters of the tested super-drawer are extracted from the super-drawer database using its ADC-I serial number, which is unique among all super-drawers. Then the communication with every single 3-in-1 card through the ADC-I card is also verified. All the control bits of these cards are flipped and the status register is read back to check if the commands were successful. All the operations are done with the CAN bus. Also, the communication with every 3-in-1 card through the motherboard's TTCrx is verified. During this all the control bits of these cards also flipped, sending commands through the TTC system. Then the status register is read back the CAN bus to check if the commands were successful. The motherboard TTCrx address is also verified and this is done by having the 3-in-1 card being selected and checked three times with the previous sub-test, using the expected motherboard TTCrx address, the expected address minus the one and the expected address plus one. In the last two tests the communication with the



Figure 4.6: A screenshot of the Willy after performing the CommMB test.

3-in-1 card should fail if everything is working fine.

Figure 4.6 shows the results of the CommMB performed to check if there is communication between the MobiDICK and the super-drawer. From the Figure we see that the test was successful as the overall result of the test is 'OK' and everything is green (the blue ones means there are no PMTs on those channels). This means that there is communication between the MobiDICK and the super-drawer and the serial number of the motherboard TTCrx and ADC-I correspond to the one on the database of the Willy. This test is performed every time a new component to be tested is connected.

Adder test

The adders are checked if they are performing an analogue sum of the outputs of up to six 3-in-1 cards by injecting a known charge on the adders one by one, verifying at each step that the increase in the adder output is consistent with what is expected. Therefore, this test is a loop on all the channels where all the 3-in-1 cards are configured to disable the charge injection input. Then, the signals coming out of the trigger cables are digitized using the trigger ADC set of cards in the MobiDICK. The charge injection input is then enabled on one 3-in-1 card with a charge of 7 pC and the trigger signals are digitized and the differences between these signals and

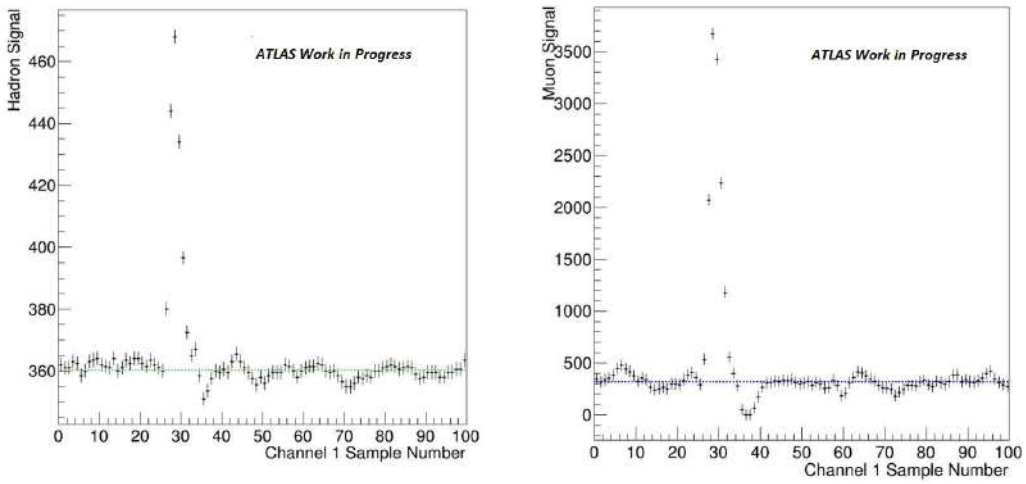


Figure 4.7: Adder's response: left (Hadron trigger output), and right (Muon trigger output).

the pedestals are computed and compared.

As mentioned above, the adder signal is an analogue sum of up to six 3-in-1 cards. The adder signal will give fast information about the energy deposited in a trigger tower (as described in Section 2).

For every channel of the tested super-drawer, an adder signal has been measured by MobiDICK for both the hadron and muon triggers. The idea of this test is to estimate the total spread of the adder signal. This will require the identity and the separation of the spread introduced by the MobiDICK due to the drawers themselves. Distribution of the adder's response from one the tested set is shown in Figure 4.7. The difference between the hadron and muon trigger output is that the muon trigger output in the figure above has signals higher than that of the hadron signal. This is the case because the MobiDICK tests were performed in a laboratory. During the maintenance period, several adder cards were tested and those that were not in a good condition were repaired and tested again if they still showed performances issues they were then replaced but if they worked after the repairs they were marked and are to be used again.

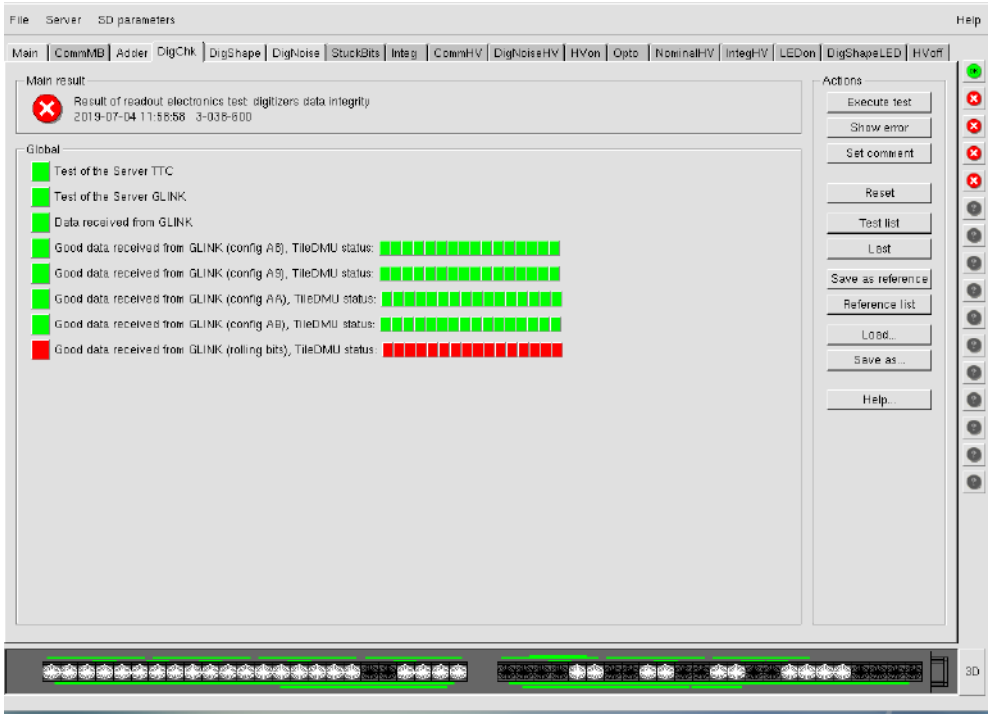


Figure 4.8: Result of the DigChk test. Here we see one of the DMU in the digitizer is not working properly

DigChk test

As mentioned above in this test the digitizers are configured to transmit different data patterns. Figure 4.8 shows the result of the DigChk test where we see that one of the checks fails in one of the digitizer's DMU. In a case like this we normally repeat the test and if we still get the same results it means that the is a problem with the digitizer's DMU this issue is further investigated by performing the digitizer's pulse shape test (Digshape).

Figure 4.9 shows a successful test of the DigChk, from this result we note that the digital readout chain is from the digitizer to the optical links is validated and everything works well. This means the integrity of the data is validated.

DigShape test

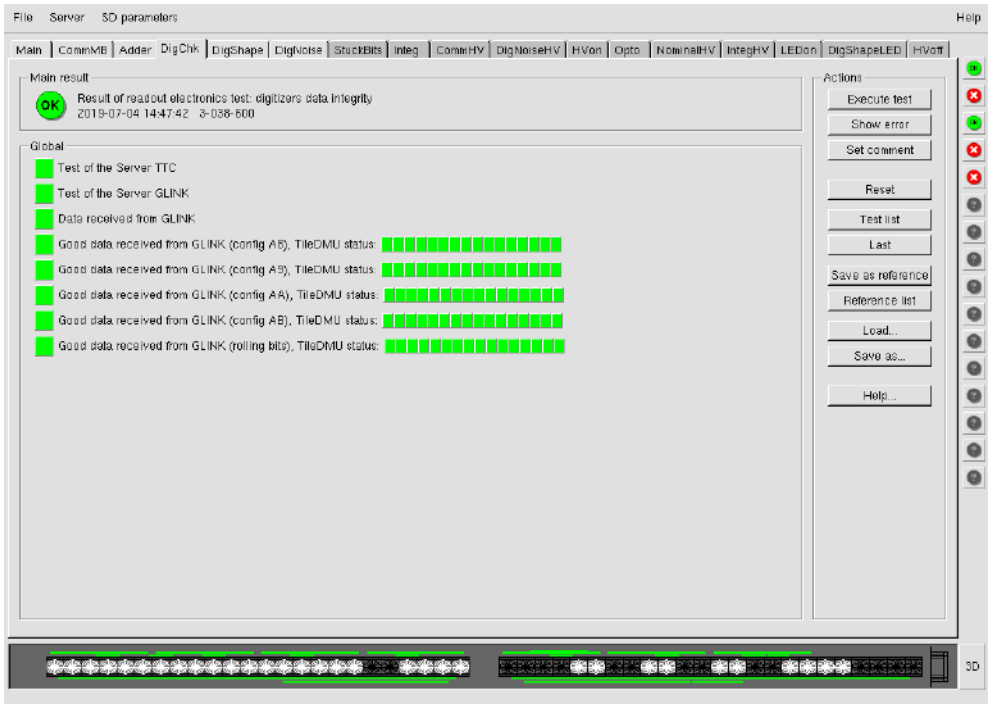


Figure 4.9: Result of the DigChk test. Here we see that everything is working properly.

The motherboard and all digitizers are first configured using their TTCrx addresses. The 3-in-1 cards are configured to enable the charge injection input. Finally, the data are read out and analyzed, including a fit of the digitized pulse.

In this test two steps are performed:

- A small charge of 10 pC using a 5.2 pF capacitor is injected to test the high gain circuits. This charge is injected on all 3-in-1 cards at the same time, allowing to detect faulty digitizers very quickly. This test is done a second time with a big charge (800 pC using a 100 pF capacitor) in order to test the low gain circuits;

- A big charge of 800 pC is injected, in order to test the low gain circuits. This charge is injected on a single 3-in-1 card, and no charge is injected on the others, to check the connectivity with the digitizers, in order to find 3-in-1 cards which would have been connected to a wrong digitizer channel.

The stability of the fit parameters of the digitized pulse shape is checked over all

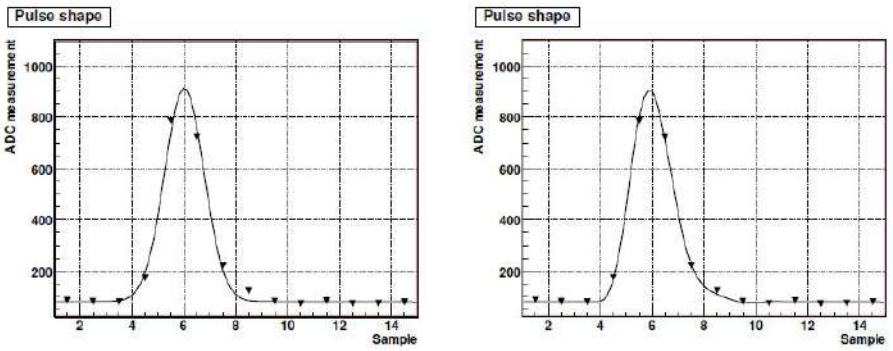


Figure 4.10: Digitized signal from a given channel (high gain signal) on the left : fit with a gaussian function, on the right : fit using the normalized pulse shape.

the available channels. During the test and validation procedure, the digitized pulse shape is fitted to a Gaussian function and the ADC measurements are plotted against the sample number.

For the analysis of the global DigShape test results, a procedure has been used, that has been fitted by the expression:

$$s(t) = p + h \times f(\alpha t - \tau)$$

where $s(t)$ is the digitized pulse shape, p and h are the free parameters, $f(t)$ is a normalized pulse shape which corresponds to the measured response of the 3-in-1 card for a given injected charge, α is a fixed conversion factor between ns and sample number (one sample corresponds to 25 ns), and τ corresponding to the time where the pulse is the highest. Figure 4.10 shows the digitized signal corresponding to a given channel. On the left, a Gaussian fit has been applied. On the right, the fit has been performed using the above equation.

Figure 4.11 shows the results of the digitized pulse shape generated by the CIS. In this Figure the shape is coloured green (digital/soft copy), meaning that the digitizers on the tested super-drawer work perfectly. After getting this result from

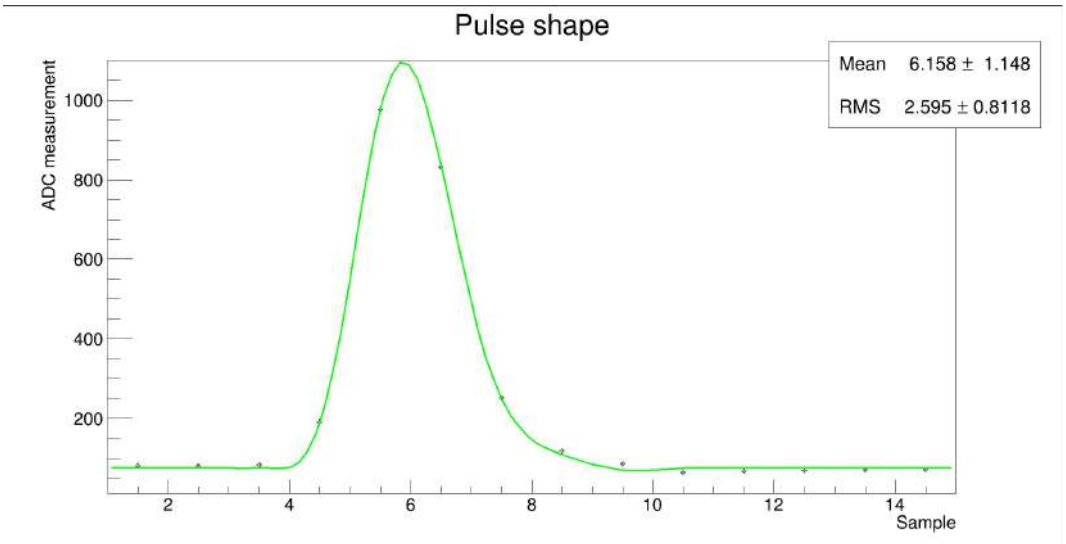


Figure 4.11: Results from the DigShape test for the Low gain configuration.

the first test, the digitizers were marked as being good, then one of the digitizers is replaced with a digitizer that has not been tested and the test is performed again. If the results change with this new digitizer, say the pulse shape becomes red, it would mean that there is something wrong with the digitizer that has been connected. That digitizer will be removed and marked as bad and will be repaired and tested again.

DigNoise test

To have a reasonable statistic, one thousand events are read out at a maximum trigger rate, without charge injection to have pedestal information only. The digitizers are put in calibration mode to read both high and low gain data. In this test the BCIDs of all the TileDMU, all CRCs and the pedestal average and RMS (digitizer noise) for each channel are computed and checked.

In the DigNoise test, the noise level for each channel in the super-drawer is measured. This has been determined for both the high and low gain configurations.

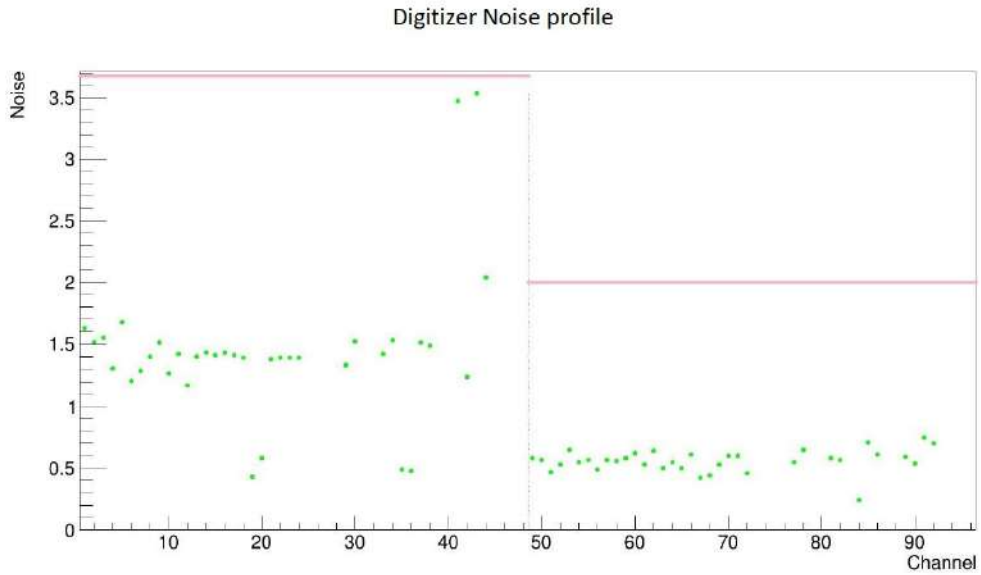


Figure 4.12: Results from the DigNoise test.

Figure 4.12 shows the noise profile of the digitizers in the super-drawer that is being tested. With the first 45 channels (left side) showing the high gain results and the rest (right side) showing the low gain, the same channels are used for both modes. These results show that the digitizer pedestals, noise and data integrity are all good.

The author tested all the super-drawer components that were brought back from the installation location in ATLAS to the surface. In 90 % of the cases, the components could be fixed and installed back in ATLAS. In the rest of the cases, new components had to be procured and assembled onto spare boards, or old boards. By the time of writing, almost 100 % of the TileCal super-drawers that had a problem at the end of Run 2 have been serviced and the expected performance of the electronics is close to 100 %

Chapter 5

ATLAS Tile Calorimeter Phase-II upgrades and Test beam campaigns

The upgrade of the Large Hadron Collider to the High-Luminosity LHC (HL-LHC) [18] will provide a unique opportunity to search for physics beyond the Standard Model (SM), to observe new details of the electro-weak symmetry breaking, and to measure more precisely the properties of the Higgs boson [45]. The LHC was designed to deliver proton-proton collisions at a centre-of-mass energy of 14 TeV and a instantaneous luminosity of 1×10^{34} cm^{-2}s^{-1}. An upgrade of the luminosity of up to 7.5×10^{34} cm^{-2}s^{-1} is planned to fully exploit the physics potential of the LHC. This upgrade corresponds to an average of up to 200 simultaneous proton-proton interactions per bunch crossing. During Long Shutdown 2 (LS2), from 2019 until 2020, the injectors will be upgraded to allow the LHC to deliver a luminosity of up to 2×10^{34} cm^{-2}s^{-1}. The luminosity increase of almost an order of magnitude above the original design will lead to a corresponding increase of particle fluxes in the detector and necessitates a major upgrade of virtually all ATLAS detector system. The performance of ATLAS will degrade as the number of collision per crossing is increased. Among other measures, this can be avoided by having the calorimeters and the muon spectrometer readout systems upgraded in order to cope with the increased occupancy and trigger rates. To improve the event selection a new trigger

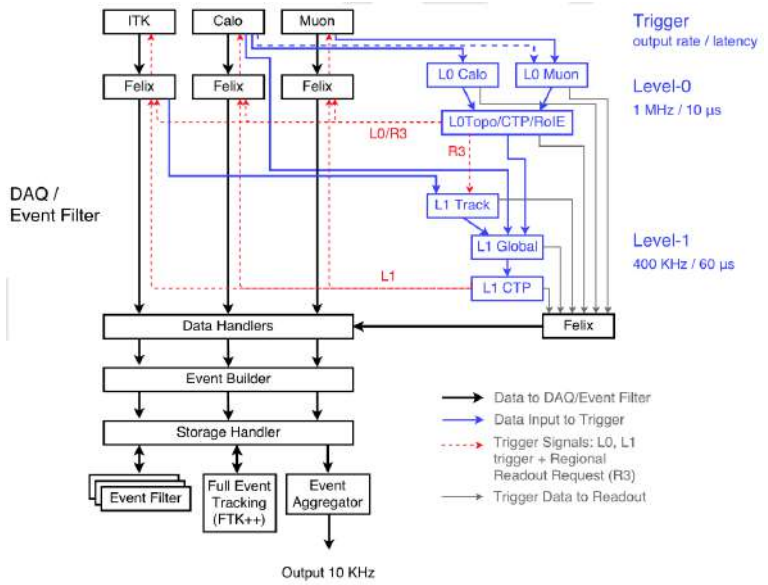


Figure 5.1: High-level description of the trigger and readout architecture in the dual Level-0/Level-1 (LVL0/LVL1) ATLAS trigger system scheme for HL-LHC [18].

architecture is needed, and this will be possible by exploiting the detector readout upgrades.

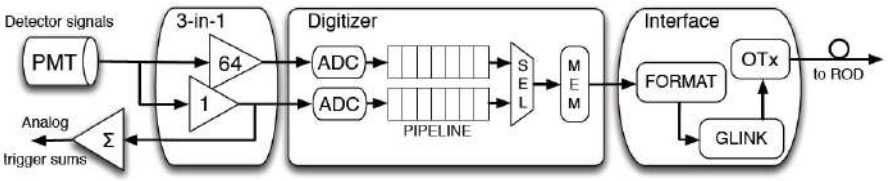
This chapter summarises the plans for the upgrade of the ATLAS Tile Calorimeter for the operation of the HL-LHC and also the test beam campaigns, and some of the details of the LS2 where the author participated on.

5.1 Motivation

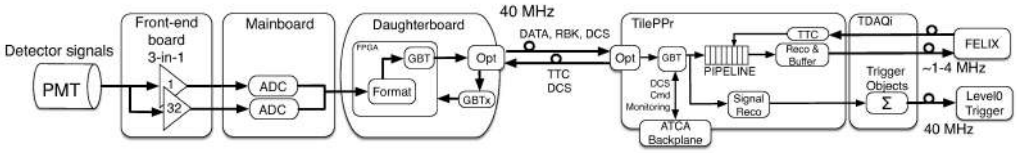
5.1.1 Requirements for the HL-LHC

5.1.1.1 TileCal Trigger and Data Acquisition Architecture

The ATLAS Phase-II TDAQ architecture compared to the current system foresees a fully digital calorimeter trigger with higher granularity and precision. The first-level calorimeter trigger (L1Calo) in the current scheme uses analogue signals, corresponding to pseudo-projective towers of 0.1×0.1 in $\Delta\eta \times \Delta\phi$. Figure 5.2 shows the current TDAQ and the Phase-II architecture. In the Tile calorimeter these towers signals are built by summing up PMT signals using analogue summing boards



(a) Current TDAQ Architecture



(b) Phase-II upgrade TDAQ Architecture

Figure 5.2: TileCal TDAQ Architecture [18].

(Adders). The PMT signals are roughly adjusted in time using delay lines but not calibrated to take into account differences in the gain in the electronics. The outputs from the summing boards are then sent off-detector to the trigger PreProcessor system using 30 to 60 m long cables. In the Phase-II design the analogue system will be replaced, and all the information from the TileCal cells, corresponding to a granularity of $\Delta\eta = 0.1 \times \Delta\phi = 0.05 \times \Delta R = [1, 3]$ λ, will be sent with a maximum latency of about 1.7 μs at 40 MHz to the trigger system that will sum the energy of the cells. To send all of this information will require an increase in the system data bandwidth, as shown in Table 5.1 that compares the current system with the Phase-II upgrade.

5.1.1.2 Radiation Hardness

As already described in Section 3.2 the FE electronics are located at the outer radius of the calorimeter and thus are shielded from radiation by the body of the calorimeter. The radiation dosage received by these electronics is not as critical as in other ATLAS sub-detector system. However, the current FE electronics need to be replaced because they have reached their end of life by 2024. The replacement of the current on-detector electronics is necessary because these components will not survive the planned radiation dose of the HL-LHC. Over the 10 years of the

Table 5.1: Comparison between the Tile Back-End (BE) readout systems in the present (ROD) and Phase-II (PPr) architectures. The data links used for redundancy and backup are omitted. The total number of fibres in the system is twice the number shown here.

Down-Links	**Present**	**Upgrade**
Number of fibres	256	1024
Link bandwidth	80 Mbps	4 Gbps
Up-Links	**Present**	**Upgrade**
Number of fibres	256	2048
Link bandwidth	800 Mbps	9.6 Gbps
BE readout modules	32	32
BE crates	4 (VME)	4 (ATCA)
BE Input bandwidth	6.4 Gbps	625 Gbps
BE output bandwidth to DAQ	3.2 Gbps	40 Gbps
BE output bandwidth to Trigger	Analogue Front-End	$\sim$ 500 Gbps

operation of the HL-LHC, a maximum integrated total dose (TID) of 244 Gy is estimated in the most critical areas, and 100Gy (10kRad) in the FE electronics of TileCal as shown in Figure 5.3

5.1.1.3 Accessibility of the Front-End electronics during maintenance periods

For the Phase-II upgrade the super-drawer body will be split into four parts, called the mini-drawers. The reason for this is to simplify the manipulation, installation and maintenance operations. The accessibility to the FE electronics will be improved, and the maintenance and installation operations in all scenarios of the detector openings will be allowed. This will help to avoid the current situation in the standard small-opening, where the current super-drawers in the extended barrels module cannot be fully extracted. Figure 5.4 shows the ATLAS detector in open configuration.

5.1.2 Reliability and Redundancy

As mentioned before, the super-drawer is the basic readout unit and in the current system it is serviced with an independent data link, TTC link, power lines, cooling and monitoring services. During the operation of the detector in Run 1, the observed

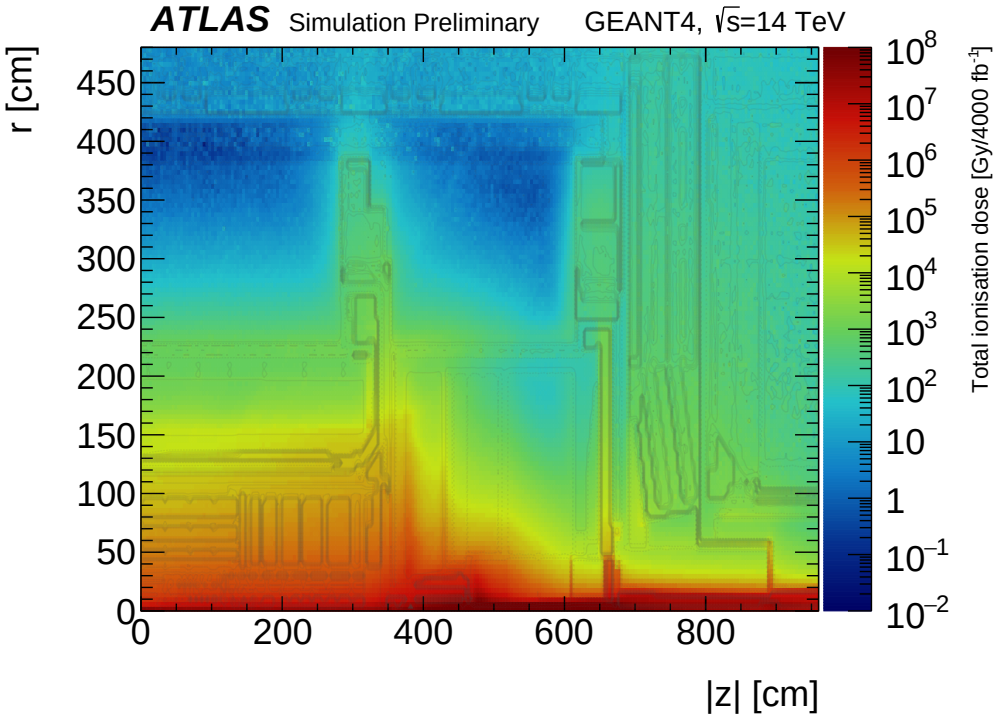


Figure 5.3: FLUKA simulation plot with Tile at 10 krad [46].

failure was mostly due to power distribution. These include failures of the LVPS, the DC/AC converter stage installed in on-detector and these failures in the power distribution interconnects with the motherboards, digitizers, and interface cards [45]. Failures were observed also in the High Voltage distribution to the PMTs realised through long distribution bus cards and flexible interconnections [45]. These failures were migrated by consolidation campaigns held during LS1 in 2013-2014, and ongoing LS2 in 2018-2019, using the MobiDICK system explained in Chapter 4.

The Phase-II system will be partitioned in smaller independent readout units to limit the impact of such failures. The overall structure of the new super-drawer is comprised of four independent readout elements, the mini-drawers. Each mini-drawer can house up to 12 PMTs, with FE amplifier/shaper cards, a Mainboard that receives the PMT signal and routes them to high-speed Daughterboards that handles all the communication with the BE electronics, this is further discussed in section 5.2. Looking at Figure 5.5 and 5.6 one can see the differences between the

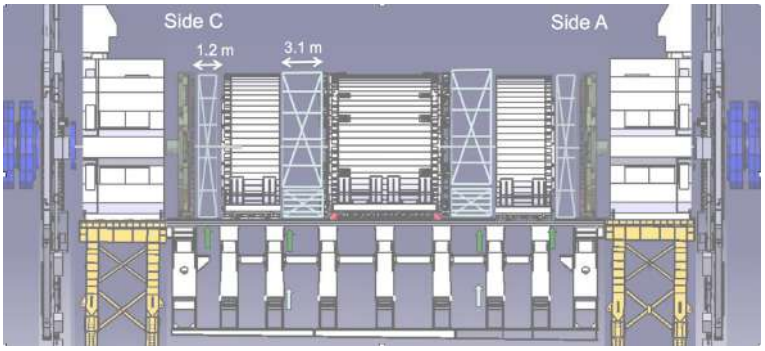


Figure 5.4: ATLAS standard opening configuration. The space between the extended barrel calorimeter and the end-cap cryostats is insufficient for the extraction of the currently used super-drawers [18].

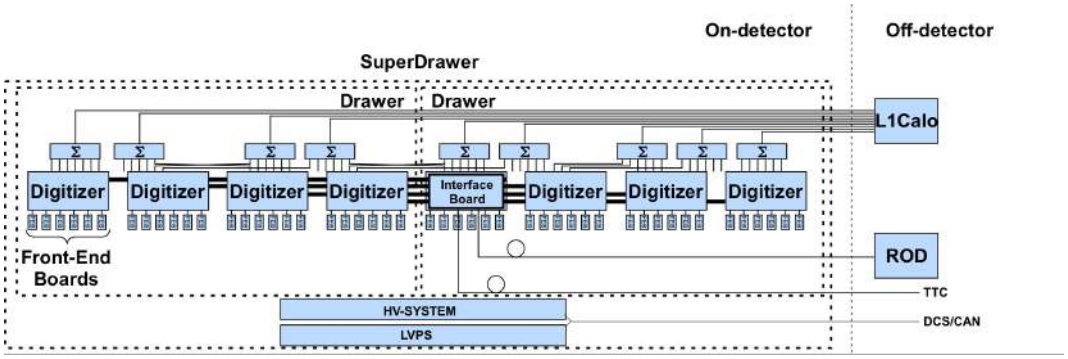


Figure 5.5: Organisation of the readout electronics in the current (Run 1) super-drawer [18].

current and the updated electronics that will be further explained in Section 5.2.

5.1.3 Optical Robustness

Currently, it is not planned to have the sampling elements, such as the scintillating tiles, WLS fibres or the PMTs changed. This decision followed a detailed study of their ageing and radiation sensitivity. The study that leads to reaching this decision was performed by analysing the evolution over time of the performance of these active elements during normal operation and it is confirmed by the irradiation tests of the scintillators [47]. The study predicted that would be a light loss of 5% (10%) after 300 fb^{-1} (4000 fb^{-1}) for the scintillators equipping the most exposed cells in the extended barrels. These variations can be easily corrected by using the calibration systems. Therefore, based on these results, there is no strong concern for the light loss of the scintillator equipping the regular TileCal cells with increased radiation.

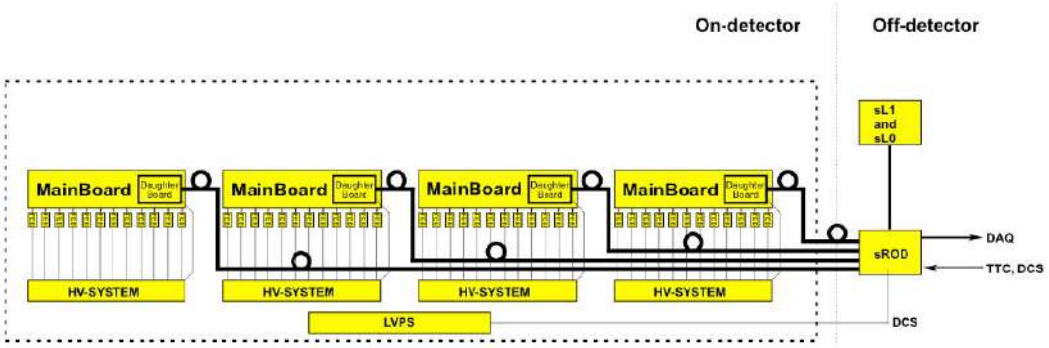


Figure 5.6: Organisation of the read-out electronics in four independent HL-LHC mini-drawers [18].

5.2 Proposed upgrades and options

The readout depends on a continuous digitization of every PMT in the FE electronics and transfer of the samples registered for every bunch crossing in the center of the detector with a frequency of 40.08 MHz as shown in Table 5.1, to the off-detector TileCal specific PPr, that will replace the current TileCal ROD. The model puts equal focus on redundant optical data transmission, which means that there will be no gain choice logic in FE electronics and the digitized signals of both gains will be transmitted. The PPr boards will be located in a very low radiation environment will implement the pipelines and the de-randomizer. The PPr will also apply calibrations of the energy scale as in the current RODs and prepare the trigger information for the LVL0/LVL1.

5.2.1 Front-End Electronics

The Front-End readout design is based on the use of highly reliable components with a strong focus on radiation sensitivity that meets the 10 krad HL-LHC requirement over 10 years. It has also been redesigned to optimize the reliability of the interconnection and sub-assemblies in the drawers, taking into account the experience of the current detector as mentioned above. In the Phase-II upgrades, four mini-drawers comprise a super-drawer, in contrast to the current configuration of 2 drawers, and 256 super-drawers form a full detector in 4 barrels of 64 wedges each. As mentioned

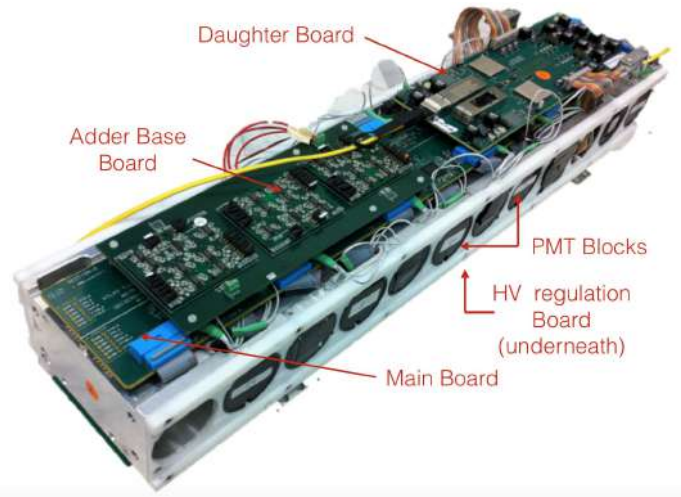


Figure 5.7: TileCal mini-drawer and the components it comprises [48].

in the previous section this particular stacking was done to improve the reliability of the interconnections and, in particular, to avoid single-point failures due to power distribution. Each mini-drawer contains a total of 12 PMTs with FE amplifier cards for pulse conditioning and calibration, a Mainboard that receives PMT signals and forwards them to the Daughterboard [49] that handles all communication with BE electronics and the HV regulation board to deliver the correct HV to the PMTs. The Daughterboard is an on-detector communication interface between the TileCal FE and BE electronics PPr located in a radiation save counting room. The Daughterboard is equipped with a GBTx chip that replaces the TTCrx, that runs at 4.8 Gpbs from the PPr for TTC and slow control (DCS), and at 9.8 Gpbs to the PPr for data and DCS transmission Figure 5.7 shows the mini-drawer with its components.

Three options of redesigned FE cards have been proposed and studied for Phase-II upgrades. One of them is an optimized redesign of the current 3-in-1 cards developed by the University of Chicago, USA, that uses state-of-the-art discreet commercially off-the-shelf integrated circuits. The 3-in-1 signal processing approach uses the shaper circuit to transform the PMT pulse into an easy-to-digitize waveform/pulse, the amplitude of which is proportional to the total charge of the original PMT pulse. The shaped signal is then amplified into two separate ranges and sent to the 12-bit ADCs on the Motherboard. This technology also provides a system

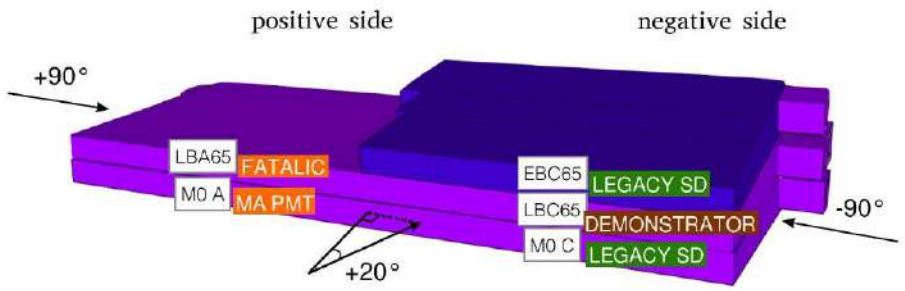


Figure 5.8: Tile Calorimeter module configuration at test beam [18].

with lower electronic noise compared to the current system. The new 3-in-1 system is compatible with the analogue trigger and can be installed in TileCal before the HL-LHC upgrade. This option was chosen as the main baseline option. Another approach is the FATALIC developed by LPC in Clermont Ferrand, France, which uses 3-in-1 shape, but with a different pulse. This ASIC chip is a new technology for TileCal and aims to integrate a large part of the 3-in-1 functionality into the FATALIC chip, including signal digitization. The ASIC design is based on a 130 nm CMOS process which has already been certified in ATLAS for uses in other subsystems with much higher doses of radiation [50]. The third option is the QIE ASIC developed by ANL, USA. The QIE circuit does not shape the PMT pulse to be digitized at bunch crossing rate. Instead, it explicitly integrates the current of the PMT anode with the same frequency. This chip was designed to meet TileCal's radiation specifications. QIE provides a unique opportunity to reduce the effect of TileCal out-of-time pile-up measurements. All signal processing (integration and digitization) is performed inside the circuitry of the card [27].

The distribution of voltage power (LV and HV) has also been revamped to tackle space constraints, performance and heat issues. To improve efficiency, the current LVPS will be based on a three-step control, where the last phase consists of discrete DC/DC linear regulators with the required radiation hardness. In terms of HV supply, 2 types of solutions were considered, remote HV and HV Opto. The

remote HV is fitted with off-detector control and monitoring circuitry. It requires many high voltage cable to each PMT from the counting room. This design significantly reduces issues with radiation sensitivity since the devices are mounted off-detector. And the HV Opto solution has a single high voltage delivered to the mini-drawer, and the control and monitoring of the 48 PMTs are carried out in the on-detector electronics. This reduces considerably the number of long high voltage cables, but the problems with radiation tolerance become more serious. For even more redundancy, it was decided to equip the mini-drawers with the two options.

5.3 The Demonstrator Program

The objective of the Demonstrator program is to test the long-term performance of the upgrade system without compromising the current data. This is achieved by developing an early version of the new BE electronics that is compatible with the current analogue trigger, DAQ, DCS and TTC. The TileCal Demonstrator is a Phase-II super-drawer prototype with an additional output trigger provided by Adder boards, that sum the analog signal from the 3-in-1 cards for the LVL1 Trigger system. It was tested to perform according to specifications during test beams. In one of the end-of-year maintenance cycles, more Demonstrator drawers could be inserted into ATLAS if desired. This will allow the major functionality of a Phase-II system to be thoroughly tested before full Phase-II installation [51]. The demonstrator's data readout strategy is as follows: data is read through the PPr board formatting and transmitting it to the legacy RODs for backward compatibility.

Between 2015 and 2018, a series of measurement campaigns with particle beams were undertaken to assess the Phase-II upgrade of electronic prototypes and to help estimate the requirements for potential commissioning of efforts. The primary objective is to determine the status of the Demonstrator based on the updated 3-in-1 FEB baseline alternative and to pay some attention to QIE and FATALIC. Several TileCal drawer modules are fitted with upgrade-specific electronics, and as shown in

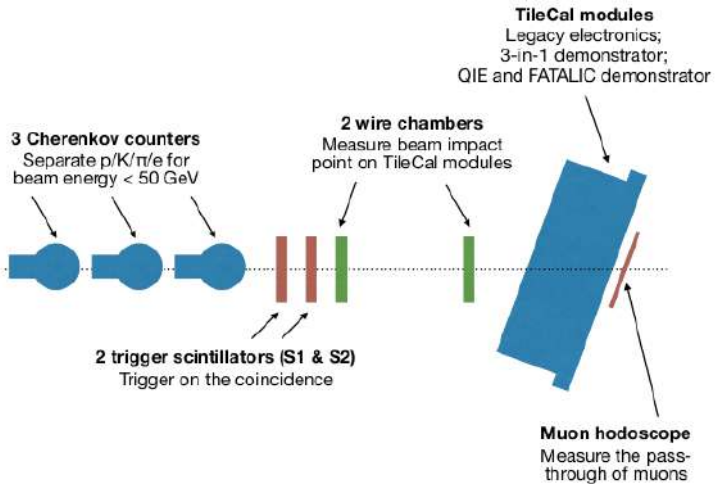


Figure 5.9: Diagram of the beam elements at the TileCal test with beam setup [18].

Figure 5.8, two other modules are fitted with existing legacy electronics. Also, the mini-drawer prototype equipped with the 2 HV regulation options were produced during these campaigns to evaluate performance and functionality in stand-alone operation was integrated with the other parts of the system. During the test beam campaigns, these modules were subjected to muons, electrons and hadrons to determine their output at different energies. The electron beam helps with the studies of the EM scale, the muons are used to study the tomography of the calorimeter and the hadrons for performance studies of the jet/$E_T{}^{miss}$. Instrumentation of the beam as shown in Figure 5.9, to identify different particles, to measure the position of the beam and to trigger synchronous data acquisition with the beam. As of 2016, 3 Cherenkov counters have been used to identify protons, electrons and muons for energy below 50 GeV, and a muon hodoscope (muon wall) behind the modules has been used to detect muons. The wire chambers are used to deduce the exact beam location in real-time, and the coincidences of two scintillators were used to produce triggers.

During these campaigns, the prototype PPr was used as it can be used in both legacy and upgrade modes. In legacy mode, by processing data samples at 40 MHz, the PPr emulates the legacy FE electronics and stores them in pipeline memories and packs them together with the computed CRC into an event fragment [52] when

a L1A signal is received that is transmitted to the RODs through optical links. The ROD processes further the event, and transmits the data to the ROS and finally to the Event Builder that saves the data on the disk. The PPr syncs the processing to the rest of the system through the TTC, and sends data fragments at LVL0 rate to the FELIX. In the current setup, this data is available later for offline analysis. The 3-in-1 Demonstrator was read using both update and legacy readings, while QIE and FATALIC were read-only using the upgrade-specific FELIX readout [27].

As of the 2016 test-beams, new hardware components were available, including Daughterboard version 4 using the new GBTx (GigaBit Transceiver) chip [53] instead of the CDCE chip for clock recovery and remote FPGA programming [54, 55]. Daughterboard version 4 has encountered a few issues related to the reliability of the high-speed data links and the clock control circuitry. Daughterboard version 5 was designed to address these issues and uses new FPGAs, and was evaluated in the 2017 test beam campaign. There is also a new Motherboard version 2 which includes an ADC de-serialization frame and bit clock, proper channel orientation, and new 3-in-1 cards were produced for this test-beam campaign. There is a new PPr version with no auxiliary boards and operates with optimized firmware versions at 40.08 MHz. Furthermore, the FELIX software was available to read the data through PCIe into local storage. Eventually, a new mobile Cesium-137 calibration system is available is available to conduct Cesium calibrations. For the entire test-beam period the three FE options under evaluation were used in parallel.

New TDAQ and DCS software to improve communication with PPr via IPBus has been developed and provides improved reliability of PPr memory for multiple application access, monitoring of connection status and configuration of FE options at the beginning of reach run. The DCS software has been updated to work with the centrally developed IPBUS OPC server [56] providing better monitoring of HV and temperature. Calibration runs (CIS, CIS mono, Pedestal and LED) have also been

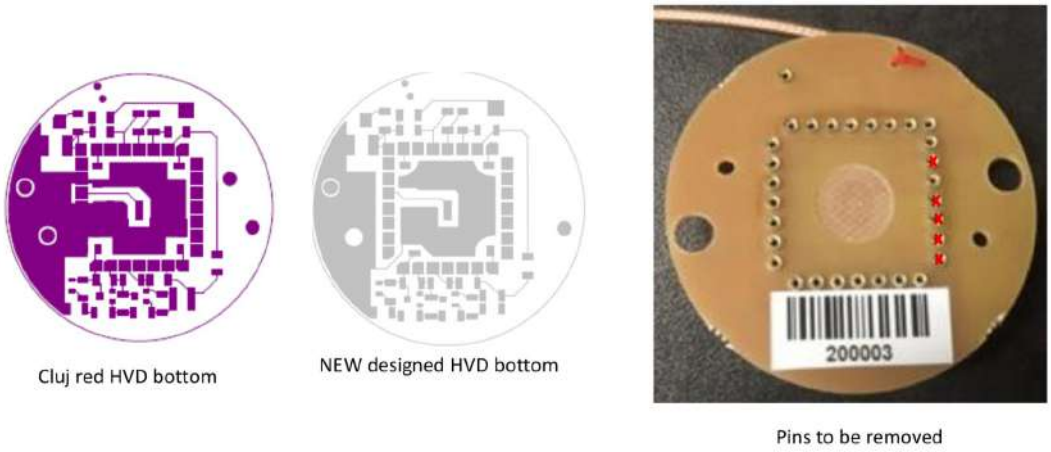


Figure 5.10: Active Divider with marked ground pins to be removed.

successfully integrated into the TDAQ system [57].

5.4 The Demonstrator Certification

An assembly of a new demonstrator to be installed in ATLAS by the LS2 was carried out in 2019. The Demonstrator with the new electronics had to be certified before insertion into ATLAS. The Demonstrator is planned to be inserted and operated in the position LBA14. It will be kept in the actual detector until early summer 2020. The Mainboards on the Demonstrator with version 2 had to be replaced and this required that all the mini-drawers of the Demonstrator and that of the Demonstrator Extended Barrel be extracted because the extended barrel contained the version 3. The PMT blocks of the Demonstrator were dissembled to replace the HV dividers with the new active dividers. Some pins connected to the ground from these new active dividers had to be removed, see Figure 5.10. Some problems were detected during the exchange, like broken capacitors on Motherboard Version 3. The reason for this damage is mechanical stress. These damaged Motherboards were repaired on site and then they were inserted back to the mini-drawers. For the readout tests, Daughterboard version 4 was used in the mini-drawers. Also, the HV Opto in the mini-drawer 2 and mini-drawer 3 of the Demonstrator Extended Barrel were with HV remote. The readout of the mini-drawers as tested can be seen of section 5.4.1 to 5.4.4. Before insertion, the testing of the HV system was performed. In a few cases,

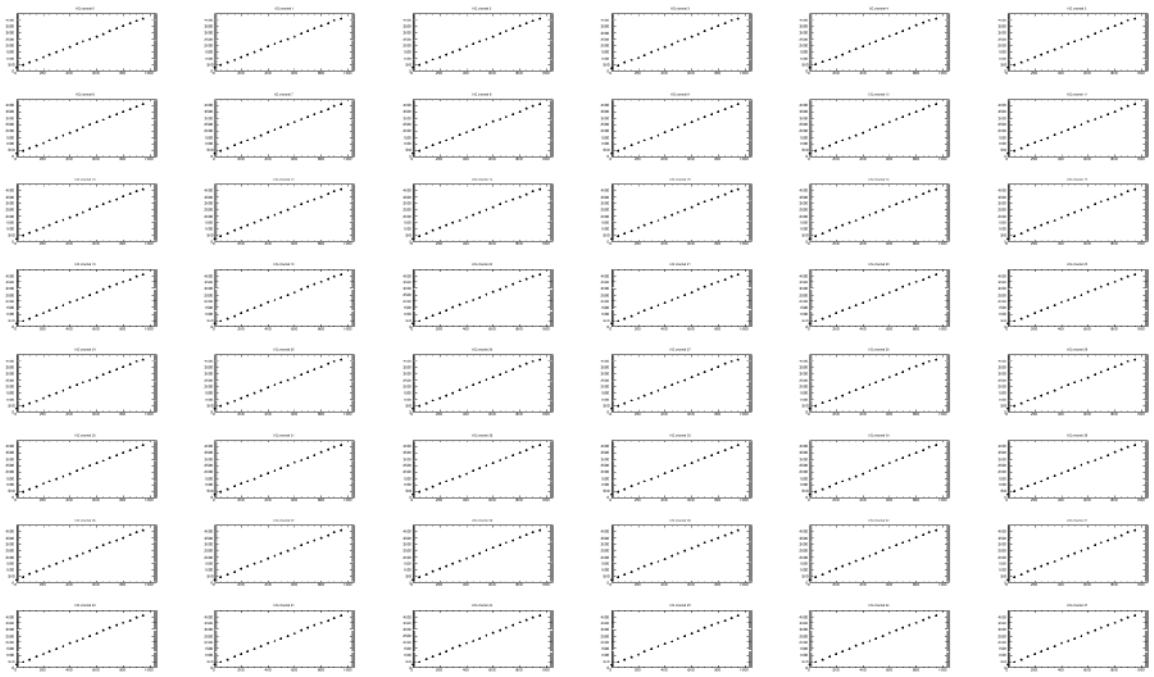
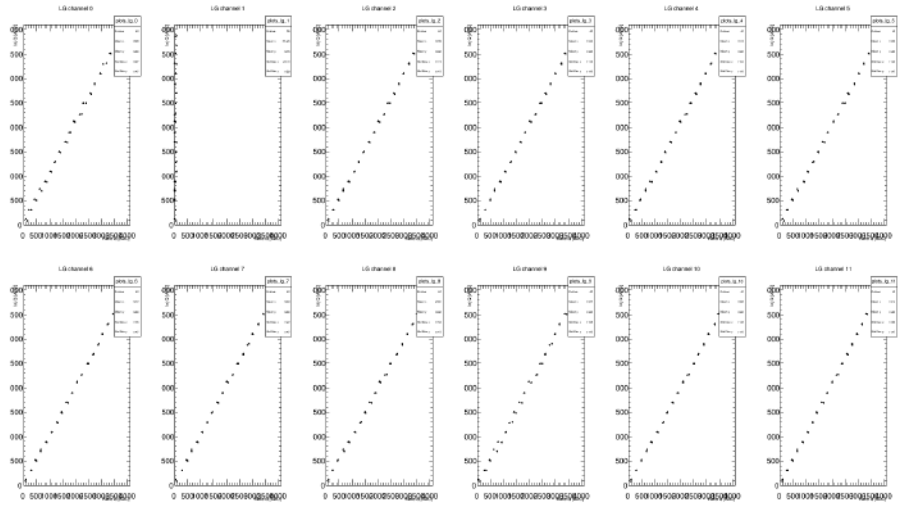


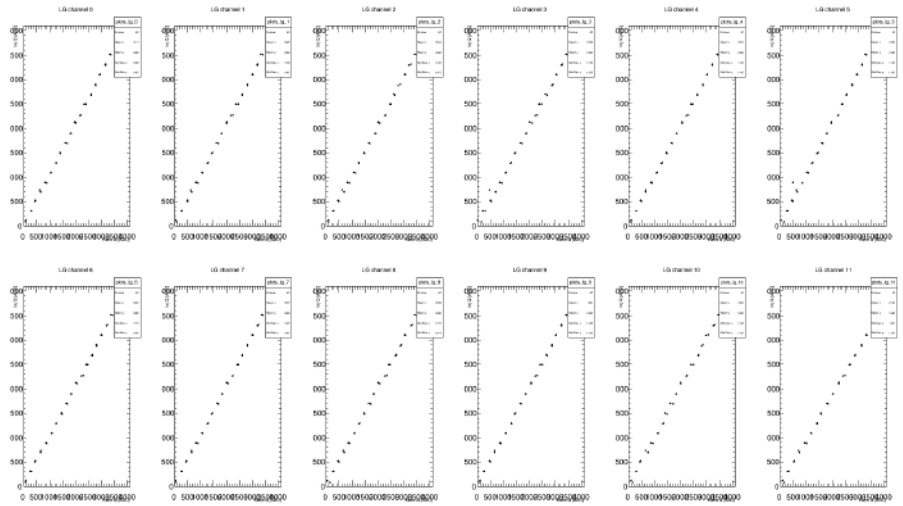
Figure 5.11: ADC linearity of the Demonstrator, showing results for the low gain

we found shorts between the ground pin of 3-in-1 cards and the PMT block causing the HV to trip. This was resolved by placing an insulating tape on the inside walls of PMT blocks. The mini-drawers were inserted back to the module on the test beam scanning table (Figure 5.9 with Daughterboard version 4, without mounting the trigger output and tested with the full readout chain for standard calibration runs.

In this study, we will show the results of the mini-drawers before being inserted in the ATLAS detector. After the testing, the mini-drawers will be extracted to replace the Daughterboard version 4 with Daughterboard version 5. Then the other next step is to install the temperature sensors (DC-DC converters on MB and Daughterboard, ADC under the Daughterboard, and DAC on the MB close to the PMT's 3-in-1 connection). Then mini-drawers will be ready for insertion in ATLAS. Trigger wires will be assembled there. On the other hand, the mini-drawers of the the Demonstrator in the extended barrel will be equipped with the Draughtboard version 5 for development work.



(a) mini-drawer 1

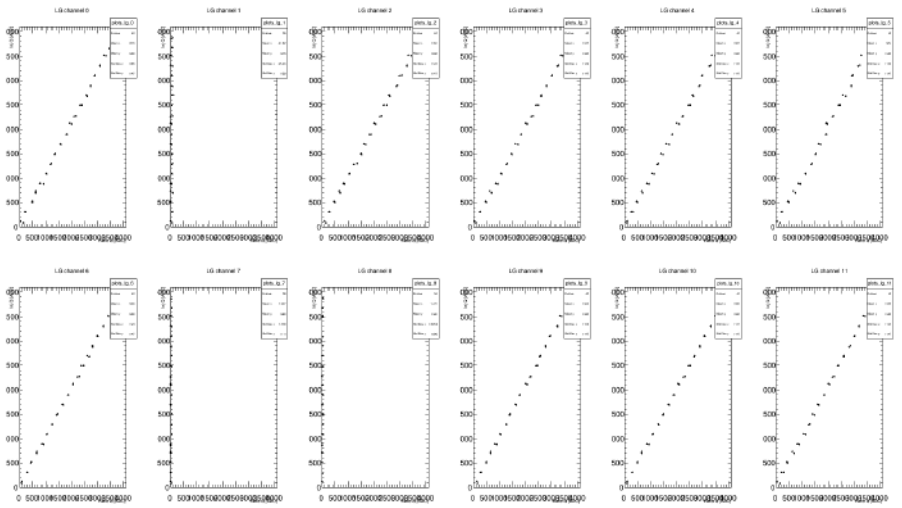


(b) mini-drawer 2

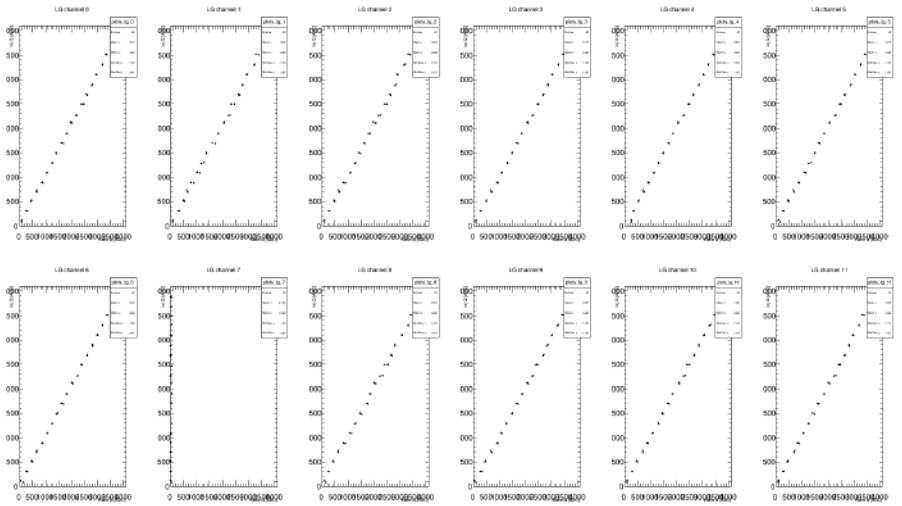
Figure 5.12: CIS linearity test of the Demonstrator for the low gain.

5.4.1 Link Tests

The link tests are performed on the Draughtboard with the aim of detecting bit-flips due to mis-alignment of the data, or CRC errors that could indicate that the link is faulty. Tests are executed on the PPr, and the variables to check from the Draughtboard are the Gigabit transceivers and the ready status of the GBTX. This test has to be executed on each mini-drawer.



(a) mini-drawer 3



(b) mini-drawer 4

Figure 5.13: CIS linearity test of the Demonstrator for the low gain.

5.4.2 ADC Linearity test

This test makes use of the script linTestv2_4QSFPs.py to the ADC linearity of the Mainboard only. Figure 5.11 shows the results for the Mainboard's ADC linearity for all the mini-drawers of the Demonstrator. In the Figure, we see that all the ADCs for each channel of the mini-drawers are working perfectly fine. Note on the plot that the 1st 12 channels represent the 1st mini-drawer then the following 12 represents the 2nd mini-drawer and so on.

5.4.3 Charge Injection System linearity test

This test is executed by running the script CIS_linearity_fromDaughterboard2.py or by using the TDAQ. The charge injection system is a feature of the TileCal front-end electronics that simulates physics signals in the TileCal channels by injecting a known charge and measuring the electronic response. This test checks the fast readout of the path using the PMT's 3-in-1 cards and plots the ADC count against the injected charge for each channel. This test is done in two modes (high and low gains), so it is done twice for each mode. Figure 5.12 and 5.13 shows the low gain CIS linearity test performed on the mini-drawers of the Demonstrator. From the Figure, it is noted that all the channels for the Demonstrator are working fine except for channel 47 (PMT 48) which has a problem with the low gain. To fix this, the 3-in-1 card on this PMT has to be changed and replaced with a new one that is working properly and should be tested again. Channel 31, 32 and 42 have close to zero signals since on those PMT slots there is nothing.

5.4.4 Integrator tests

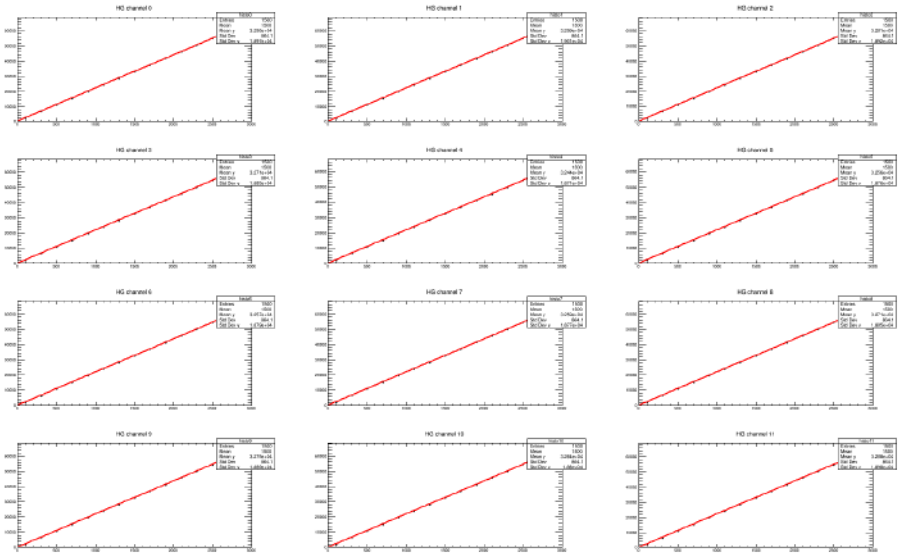
This test is also executed using the script Integrator_readout_All_del.py, but for this test additional options have to be added to specify what integrator value to be used. The Demonstrator had to be checked for all the integrator gain which are 6. This test checks the slow readout path using the PMT's 3-in-1 cards. For this test one mode (low or high) needs to be selected. Figure 5.15 the Integrator linear test results of the Demonstrator for gain 1 in the indicated mode on the plot. In the Figure, we see that the charge integrator circuitry for gain 1 in all the channels of the Demonstrator is working perfectly. For channel 31 and 32 of mini-drawer 3 and channel 43 of mini-drawer 4, there is no plot, this is the case because in these channels there are no PMTs in these slots so we do not expect to see any signals.

Figure 5.16 and 5.17 shows the integrator linearity for gain 2. Figure 5.18 and 5.19

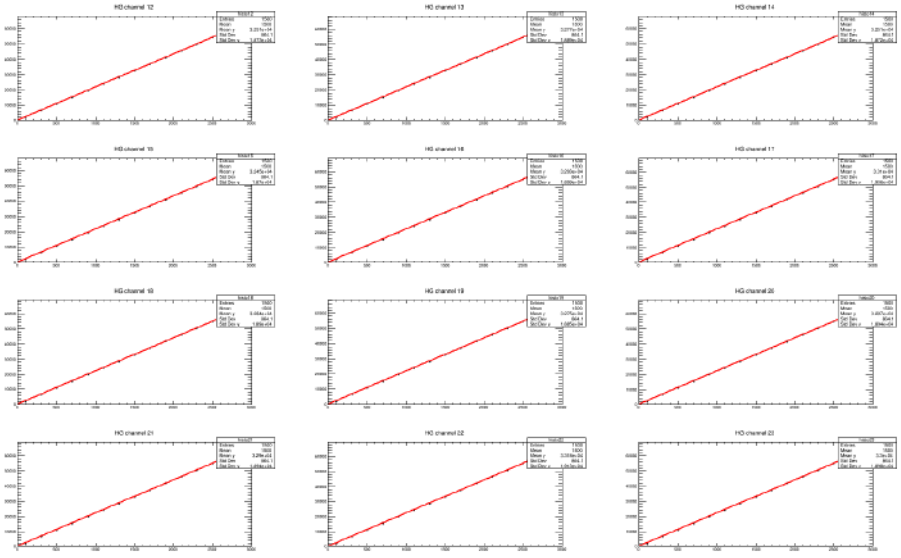
shows the integrator linearity results for gain 3. In these Figures it is noted that the linearity of channel 33 for these gains is not consistent with the rest of the other channels, meaning that for this channel there is a problem for higher gains. This problem is rectified by replacing the 3-in-1 card of this channel and this test is repeated to see if the new 3-in-1 card is working properly.

5.5 Conclusions

All these tests were performed at the test beam site at CERN and the problems encountered for all the channels will be fixed before the Demonstrator can be inserted in ATLAS. As soon as the problems are fixed, the Demonstrator will be taken to ATLAS and these tests and more will be performed, and the Demonstrator will be studied carefully during the LS2. The author contributed to this study by doing the assembly of the components needed for the Demonstrator and also by performing the tests for the certification of the Demonstrator.

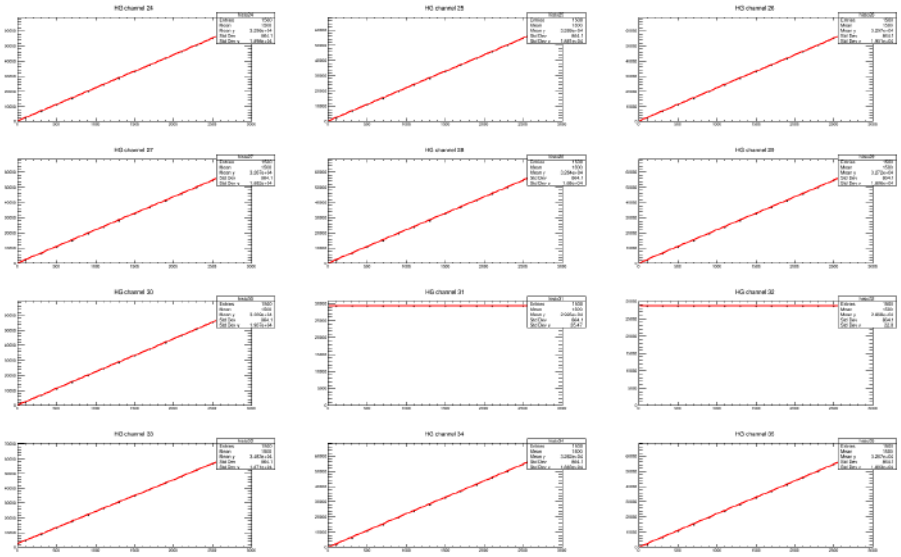


(a) mini-drawer 1

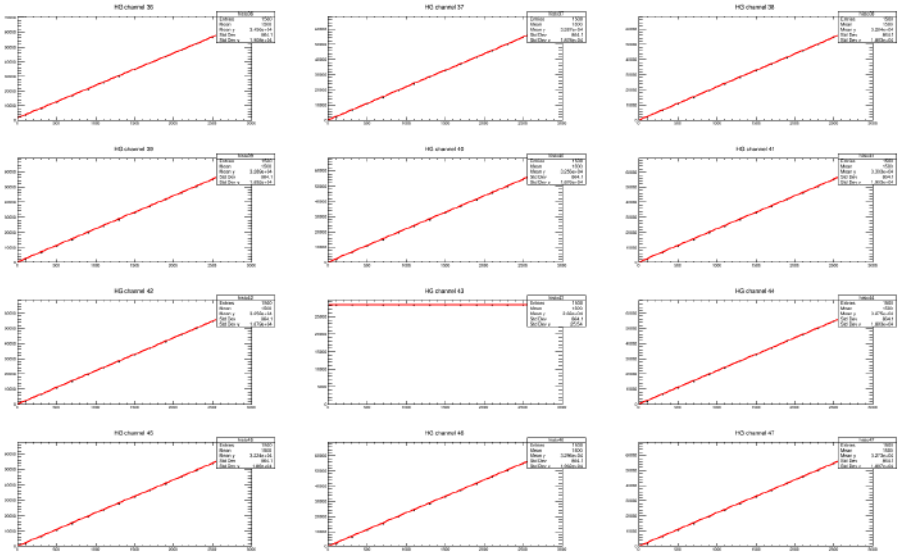


(b) mini-drawer 2

Figure 5.14: Integrator linearity results of the Demonstrator for Gain 1 (mini-drawer 1 and 2).

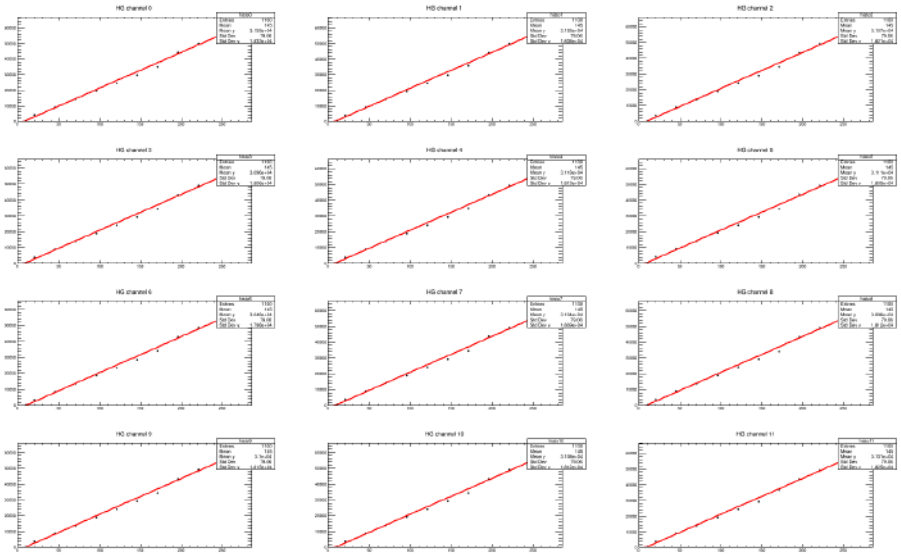


(a) mini-drawer 3

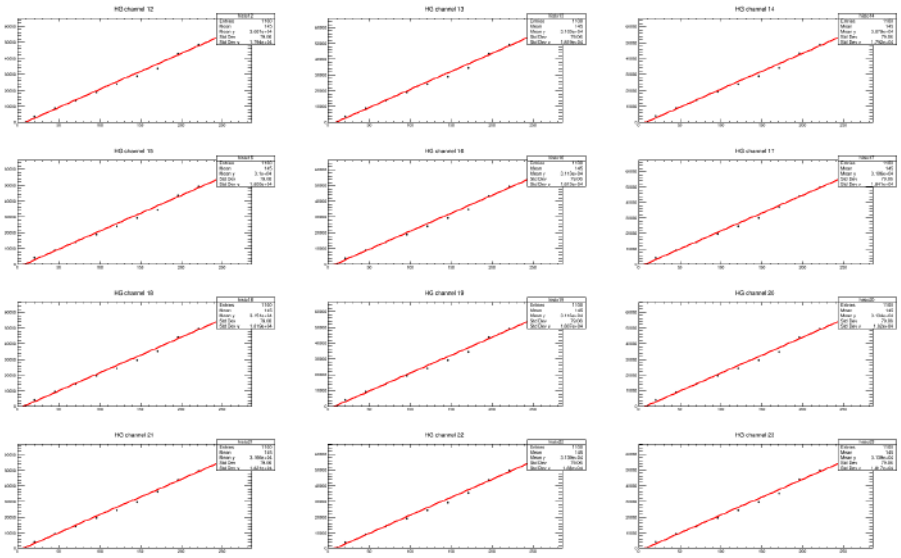


(b) mini-drawer 4

Figure 5.15: Integrator linearity results of the Demonstrator for Gain 1 (mini-drawer 3 and 4).

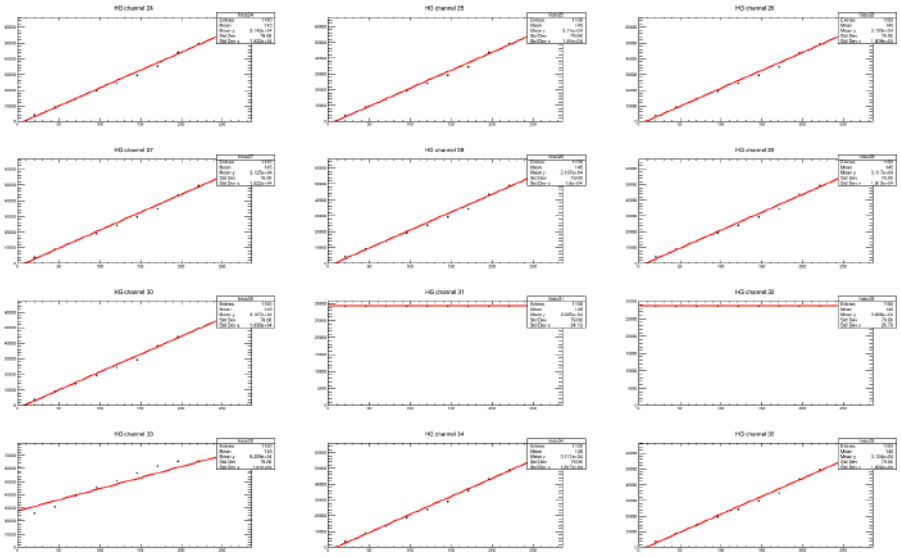


(a) mini-drawer 1

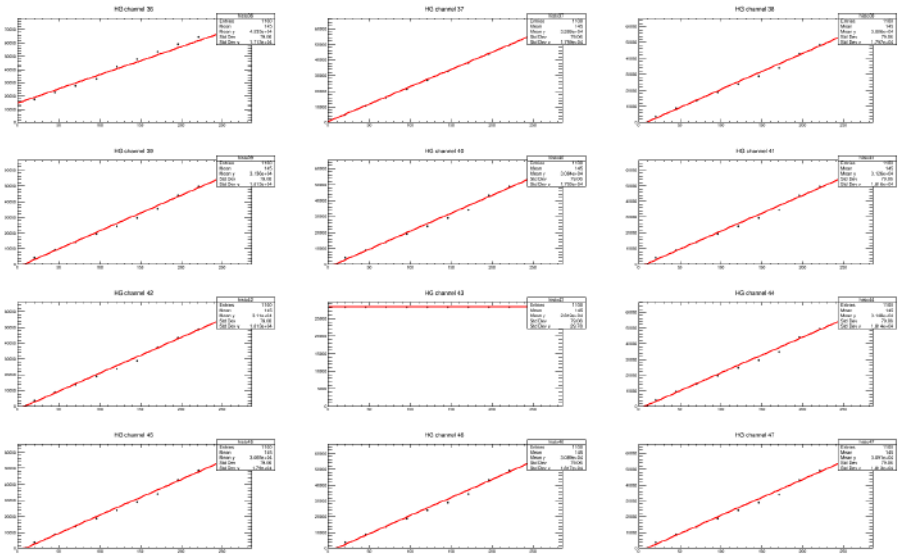


(b) mini-drawer 2

Figure 5.16: Integrator linearity results of the Demonstrator for Gain 2 (mini-drawer 1 and 2).

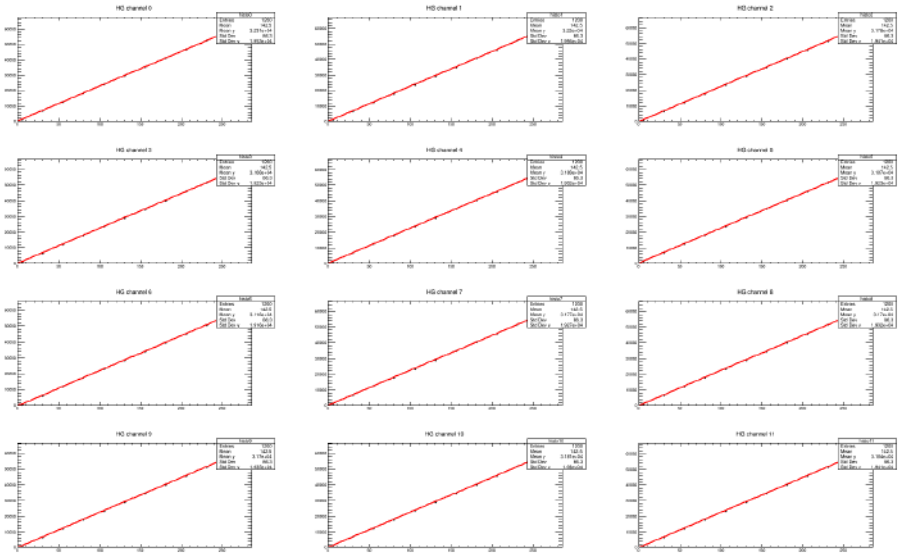


(a) mini-drawer 3

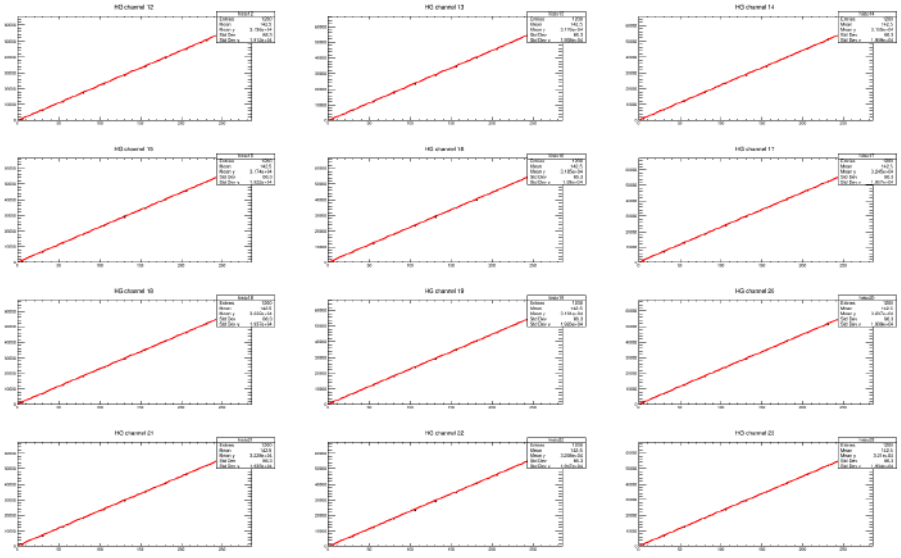


(b) mini-drawer 4

Figure 5.17: Integrator linearity results of the Demonstrator for Gain 2 (mini-drawer 3 and 4).

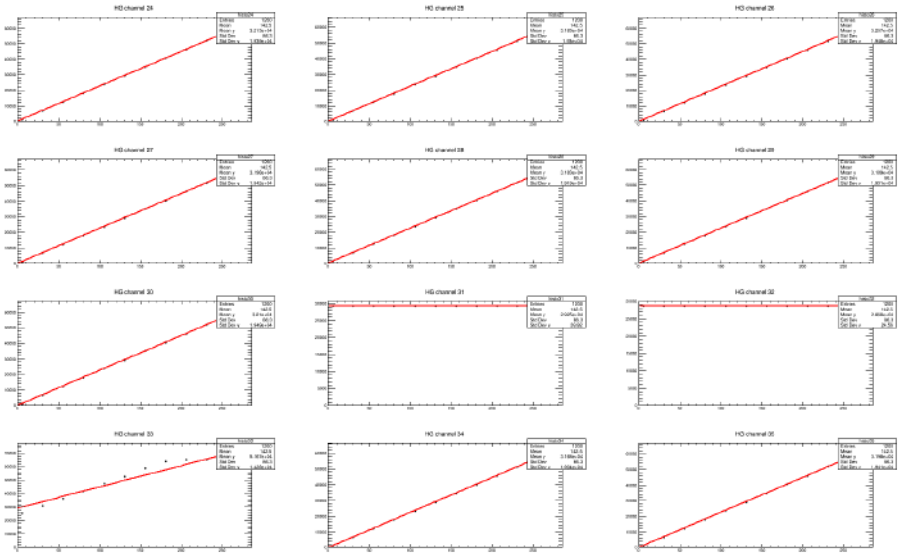


(a) mini-drawer 1

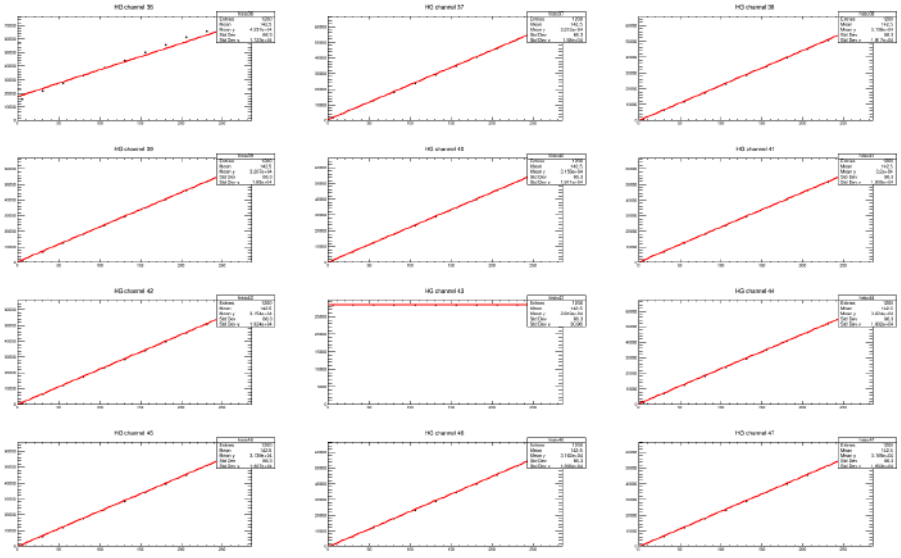


(b) mini-drawer 2

Figure 5.18: Integrator linearity results of the Demonstrator for Gain 3 (mini-drawer 1 and 2).



(a) mini-drawer 3



(b) mini-drawer 4

Figure 5.19: Integrator linearity results of the Demonstrator for Gain 3 (mini-drawer 3 and 4).

Chapter 6

Light Yield Studies of Neutron irradiated plastic scintillators

In this chapter we discuss the effects of neutron irradiated plastic scintillator by checking the optical properties of the samples using the techniques of light yield.

6.1 The Scintillation Mechanism

Plastic scintillators are mainly composed of organic fluors suspended in a polymer base. The polymer base contains an aromatic ring structure that results in the molecule being dislocated to the π-electron structure. If ionizing radiation hits the scintillator. These de-localized π-electron will absorb part of its energy, leading to the molecules to be excited. Usually, the absorption is shown in the visible and ultraviolet wavelengths that lead to the excitation of the singlet π-electron state. An excited π-electron may return to its ground state via multiple types of deactivation processes, resulting in the shortest lifetime of the excited state being the preferred process.

Excitation with additional vibrational energy can also lose energy by vibrational relaxation by dissipating heat and reaching thermal equilibrium in the molecule. The fluorescence process occurs where energy is emitted as a photon of a character-

istic wavelength from the lowest vibrational first excited state to the ground state. In organic plastic scintillators, this process forms the primary scintillation mechanism. Fluorescence occurs within nanoseconds, giving fast response capability to plastic scintillators.

6.1.1 Radiation damage in plastic scintillators by neutron irradiation

As ionizing particles pass through the scintillator medium, they leave a collection of excited particles behind, some of which are exposed to fluorescence, providing light. At high incident doses, this radiation may break the chemical bonds of the material, therefore modifying the polymer properties. This kind of damage on the scintillator is complicated and can be due to several factors, which include: the rate of irradiation, the amount of dose absorbed, the nature of the incident particle the structural properties of the polymer and the environment where radiation occurs.

The greatest effect of radiation damage is that it changes the scintillator's optical properties. This normally occurs in two ways: the first is the decrease in the actual light output of the scintillation due to damage to the fluorescent component in the material, and the second is the degradation in its transmission character due to the formation of optical absorption centres. The change in transmission character also affects the scintillator's light attenuation length [58] and the amount of light collected by a PMT in TileCal.

The study here focuses on the effects of non-ionizing radiation (i.e neutrons). Compared to the interaction of ionizing radiation, the non-ionizing radiation indirectly interacts with matter. Once materials are bombarded with neutrons, inside the material collision cascades are produced which result in point defects and dislocations. When the kinetic energy from the collision is transferred to the displaced lattice atom, a Primary Knock-on Atoms (PKA) is formed. The Knock-on atoms lose

Table 6.1: Properties of the Plastic scintillators under study

Scintillator	**Blue UPS-923A**	**Green**
Manufac	ISMA	ISMA
Base	Polystyrene	Polystyrene
Primary Fluor	2% PTP	3HF
Light output (% Anthracene)	60	
Wavelength of max. Emission (nm)	425	530
Rise Time (ns)	0.9	0.9
Decay Time (ns)	3.3	7.6

energy during these collisions, and that energy, in turn, ionizes the material [59]. Neutron irradiation allows bulk sampling of materials, as these are particles with high penetration.

6.2 Experimental Details and Setup

In this study commercial blue scintillators (UPS-923A) [60] and synthesized green scintillators [61, 62] are investigated and the properties of these scintillators can be found on Table 6.1. The samples were prepared at the Institute for Scintillation Materials (ISMA, Kharkov). They were cut and polished with a thickness of 6 mm to dimensions 2 by 2 cm. Channel number 3 of the reactor IBR-2, as shown in Figure 6.1, was used to irradiate samples at the FLNP at JINR in Dubna Russia [63, 64].

The samples were exposed to a 432-hour beam of neutrons, which was the duration of the October 2017 reactor cycle. The reactor operated at an average power of 1875 kW with samples positioned at different positions away from the centre of the reactor to achieve different neutron fluences [65]. The neutron fluence was ranged between 10^{13} to 10^{17} n/cm^2. As shown in Figure 6.2, the samples were discoloured as the evidence of irradiation. The only neutrons we are concerned about are those with $E > 1$ MeV. These neutrons represent approximately one-quarter of the total flux. Hereafter, we refer to the number of fast neutrons with $E > 1$ MeV, although the actual number of neutrons is a factor of four higher.

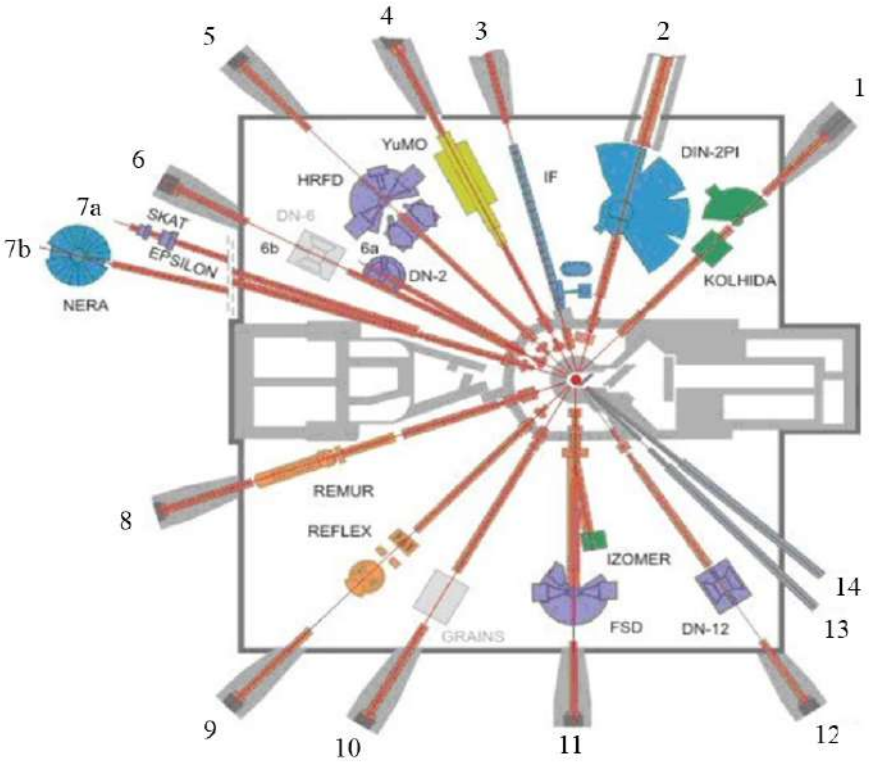


Figure 6.1: IBR-2 reactor.

To characterize the effects of radiation damage on optical and structural properties of the samples, measurements of light yield, light transmission, light fluorescence and Raman spectroscopy is performed. The Varian Cary 500 spectro-photometer at the University of the Witwatersrand was used for transmission spectroscopy studies. The spectro-photometer consists of a source of lamp and diffraction grating to produce a light spectrum of variable wavelength. In this study, the radiation damage effects are characterized by measurements of the light yield on the optical properties of the samples.

The light yield measurements were conducted at CERN using a light-tight box setup. This setup is shown in Figure 6.3. The plastic scintillators were exposed to a Sr-90 source of electrons with average energy levels of 0.54 and 2.28 MeV. The position of the Sr-90 source was moved in the direction x-y across the sample and emitted radiation in the direction of z. The PMT was used to detect the light

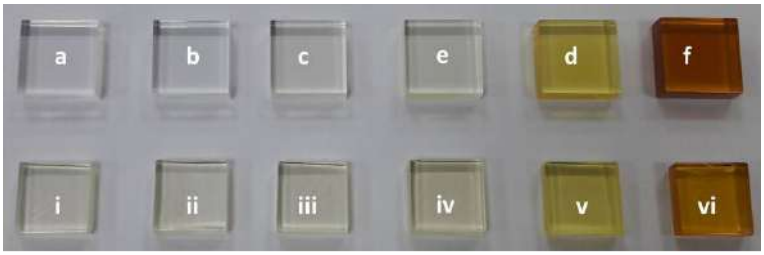


Figure 6.2: Neutron irradiated samples, Green scintillators (a–f) and Blue scintillators (i–vi) UPS-923A. From the left column to right column: non-irradiated, 10^{13} , 10^{14}, 10^{15}, 10^{16}, and 10^{17} n/cm^2.

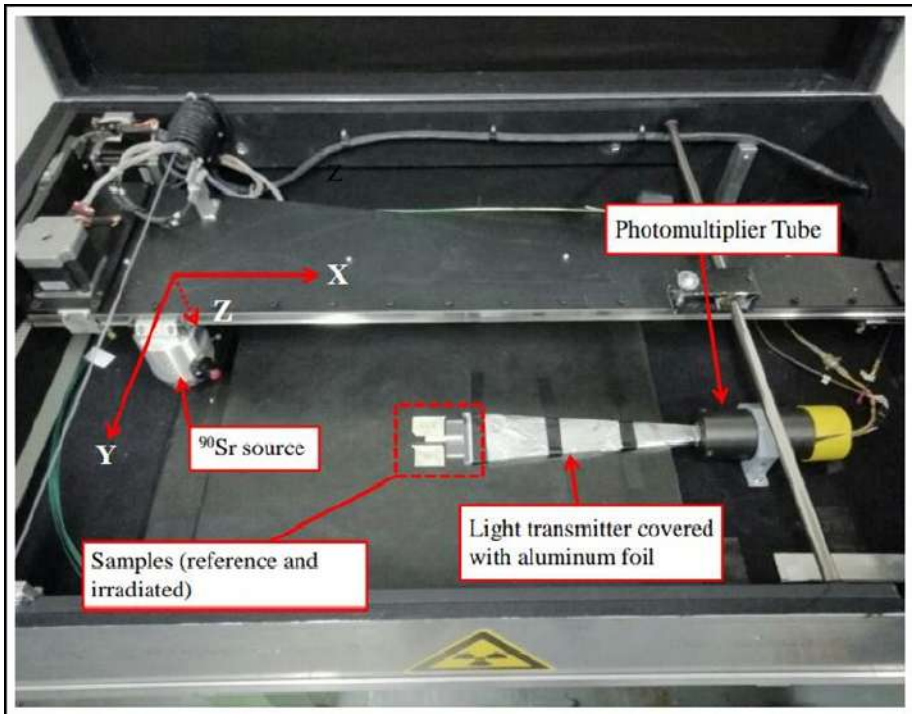


Figure 6.3: The Black Box setup at CERN.

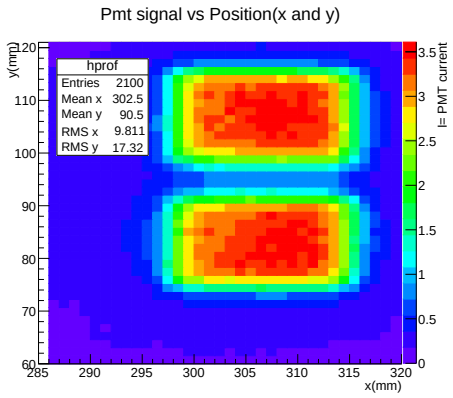
emitted by the scintillators under study. The PMT signal was further processed and digitized using a simple ADC. Background signals like the electrons interacting with PMT were reduced by a light transmitter to transport the scintillator's light to the PMT cathode. To prevent electrons from the source to interact with the light transmitter, the light transmitter was covered with an aluminium foil. The above table Table 6.1 shows some of the important properties of the plastics scintillators under study. For more details see [65].

6.3 Results and Discussions

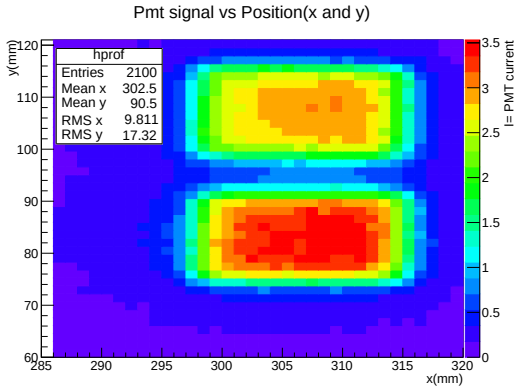
The evaluation of the light produced by the irradiated plastic scintillator samples was carried out by testing their response to the Sr-90 source of electrons. The PMT signal was measured in terms of the position of the source. A 2D mapping of the signal measured in x and y direction over two blue samples are shown in Figure 6.4. In the mapping the first pair is the 10^{13} n/cm^2 irradiated blue samples (top) and the unirradiated blue sample (bottom). The next pair consists of the 10^{14} n/cm^2 also with an unirradiated reference sample. The green samples are also shown in Figure 6.5, where the pair of 10^{13} n/cm^2 and the unirradiated green is also mapped and the rest follows until 10^{17} n/cm^2. In the Figures we see that for the blue samples as the light detected by the PMT decreases the neutron fluence increases. This is the same as for the green samples, but the green samples are affected more by the neutron fluence as compared to the blue samples.

A 2D map of the signal measured at x and a y pair of samples is shown in the Figure 6.6. Samples are approximated by the black and yellow boxes, which show both irradiated and irradiated samples. The background had been subtracted from the rest of the mappings before analysis. The background region marked with a red box on Figure 6.6(a) was selected on one of the 2D mapping surfaces with the signal not contaminated by the signal from the samples. As a background value, the mean signal value of 0.1309 mean/entry was used over the selected area. The area cuts plots shown in Figure 6.6(b) were selected from the 2D mappings with entries of high signal values. In order to analyze the light yield loss based on neutron fluence, the ratio of corrected signals from the reference and test samples was calculated and reported against the neutron fluence as shown in Figures 6.7. As expected, neutron fluence increases, the light yield loss in all irradiated samples is observed. It is prominent at a fluence of 10^{17} n/cm^2. In Figure 6.7 we note that as the neutron fluence increase the light yielded by the samples decreases, but the light yield for the green samples is lower in comparison with the blue samples. The reason for this is

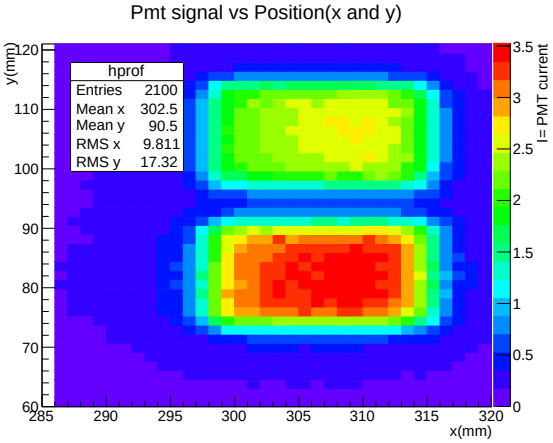
that the green sample appear to be sensitive to radiation and die out as the neutron fluence increases as compared to blue samples.



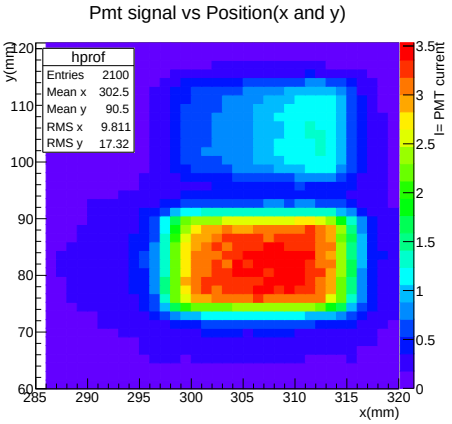
(a) 10^{13} n/cm^2 (Top: irradiated, Bottom: unirradiated)



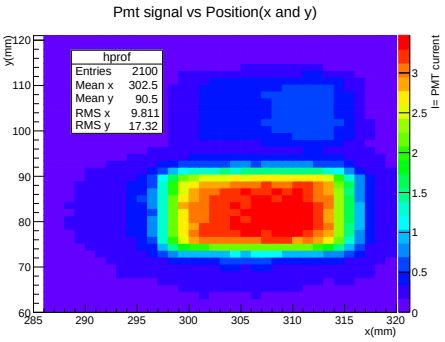
(b) 10^{14} n/cm^2 (Top: irradiated, Bottom: unirradiated)



(c) 10^{15} n/cm^2 (Top: irradiated, Bottom: unirradiated)

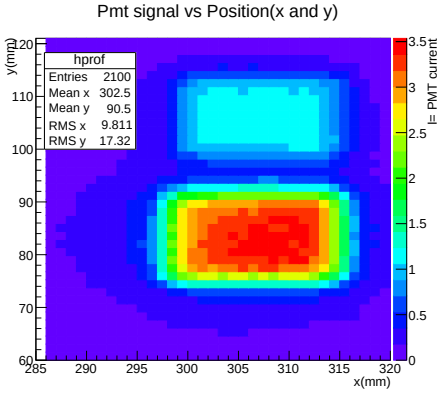


(d) 10^{16} n/cm^2 (Top: irradiated, Bottom: unirradiated)

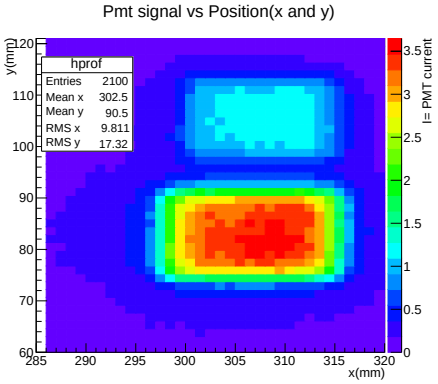


(e) 10^{17} n/cm^2 (Top: irradiated, Bottom: unirradiated)

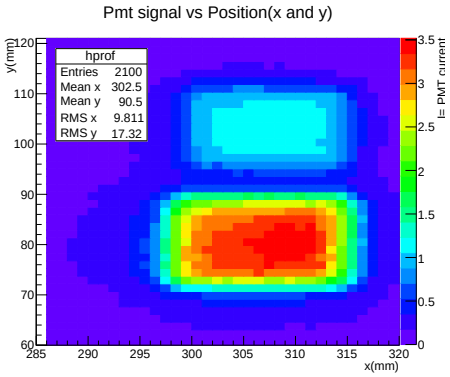
Figure 6.4: 2D mapping of the Blue samples



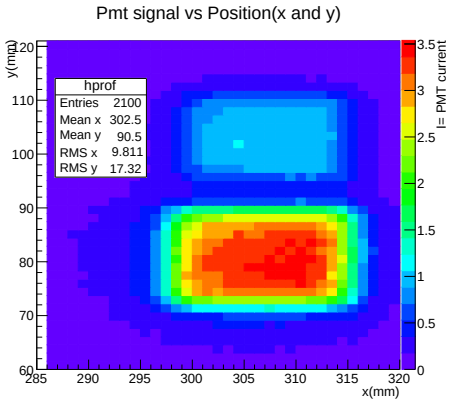
(a) 10^{13} n/cm^2 (Top: irradiated, Bottom: unirradiated)



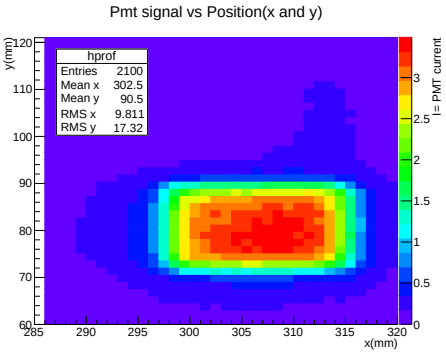
(b) 10^{14} n/cm^2 (Top: irradiated, Bottom: unirradiated)



(c) 10^{15} n/cm^2 (Top: irradiated, Bottom: unirradiated)



(d) 10^{16} n/cm^2 (Top: irradiated, Bottom: unirradiated)



(e) 10^{17} n/cm^2 (Top: irradiated, Bottom: unirradiated)

Figure 6.5: 2D Mapping of the Green samples.

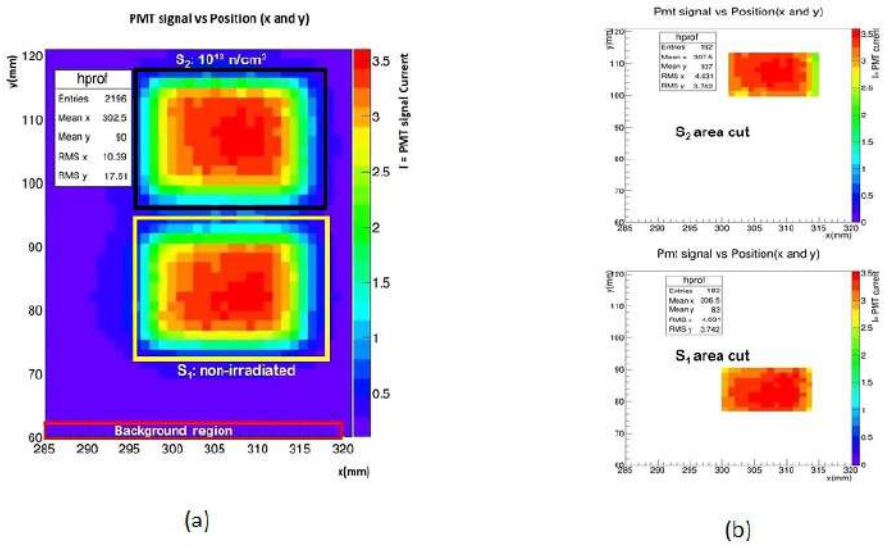


Figure 6.6: (a) 2D mapping of the PMT signal at the Sr-90 source position, indicating the signal regions corresponding to the regions on the experimental set-up. (b) And plots of area cut with entries of high signal values.

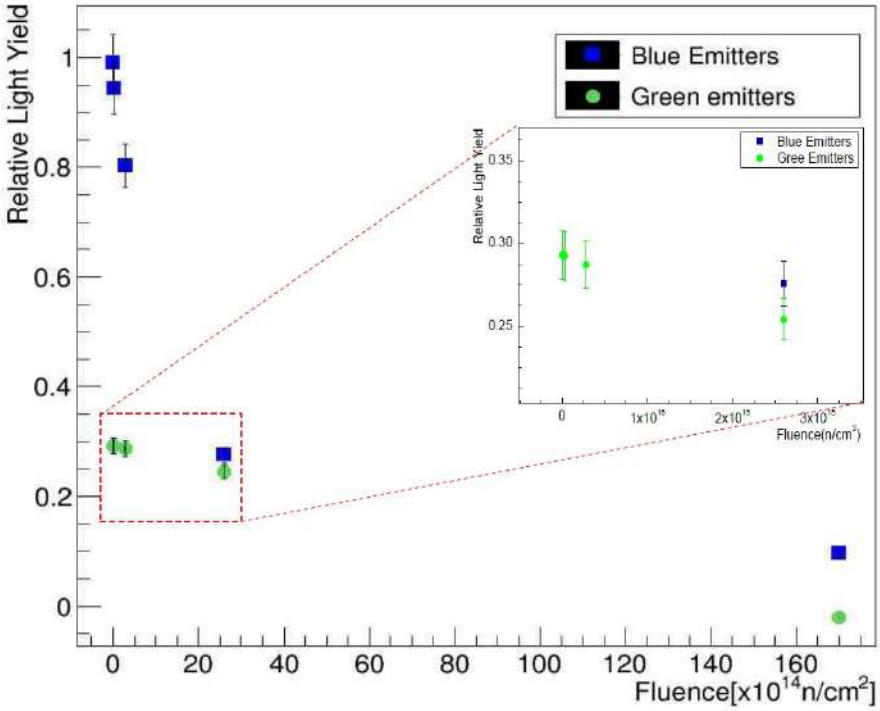


Figure 6.7: Light yield for the blue UPS-293A scintillator and green scintillator against neutron fluence.

Chapter 7

Conclusion

This thesis is divided into two parts. The first part is the testing of the current FE readout system and the Demonstrator certification which houses the ATLAS Phase-II upgrade readout system of TileCal. The second part features the light yield study of the neutron-irradiated plastic scintillators.

The first part is devoted to introducing the ATLAS experiment with an emphasis on the TileCal detector. This includes a detailed explanation of the detector elements and focuses on the FE readout system. The FE readout electronics play an important part in data taking. During the maintenance periods at CERN, the different components of the FE electronics undergo serious testing and maintenance to improve their functionality during detector operations. The MobiDICK system is the mobile test bench that is used to certify the electronics in stand-alone mode or when are inserted on the detector. The Phase-II upgrade FE system is also important. A prototype FE electronics demonstrator has been developed in the context of the Phase-II upgrade of the LHC, and has been certified before insertion into ATLAS during LS2.

In this study early certification of the Demonstrator has been performed and with positive results as compared to previous test beam campaigns. It has been confirmed that the Demonstrator is ready for insertion in ATLAS. During LS2, the Demon-

strator will be tested alongside the current system in preparation for the LHC's Run 3. During the maintenance periods between 2018 and 2019, the components of the super-drawers from different modules have been tested and debugged for better performance of the detector. In chapter 4 of this study, components of the super-drawer, such as the PMT blocks, Motherboards, digitizer boards, interface boards, and summation cards have been tested. In this study several components of the super-drawers from different modules were tested to asses their performance and it was noted that components that are faulty or not working properly compromised the granularity of the data during data taking. Such components were replaced/fixed to improve the FE readout system. In chapter 4 we see the result of the components tested. Faulty components were repaired and tested again and if the issues persist, they will be replaced. In chapter 5 we see the early certification results of the Demonstrator, which are positive, meaning that the Demonstrator is ready for insertion in ATLAS. In the certification process of the Demonstrator, several issues rose with most verified to be misbehaving channels. This problem for most of the readout was fixed by replacing the misbehaving component, which was the 3-in-1 cards.

In the last section, the optical properties of the neutron-irradiated plastic scintillators (blue and green light-emitting scintillators) have been studied. This study was conducted by measuring the light yield at CERN. This study is important as it would help understand how the light yielded by the scintillators affected by neutron irradiation. The neutron fluence used in this study ranged from 10^{13} n/cm^2 to 10^{17} n/cm^2 and this range the optical properties of the samples were studied. According to the results from chapter 6, it was found that as the neutron fluence increases, the light yielded by both samples decreased. This is first shown by the 2D scan plots, where the scan of the unirradiated sample is compared to those that have been irradiated with neutrons. In the 2D scans it is noted that as the neutron fluence is increased, the light signals detected by the PMT decreased. Comparing both

the blue and green samples, it is seen that the green samples tend to lose the light transmitted faster than the blue samples. The relative light yield of both samples is also plotted. In the plot for relative light yield against fluence, it is seen that for both samples the relative light yield decreases as the neutron fluence increases with of cause the green samples having a low relative light yield compared to the blue samples. The same neutron influences were applied for both blue and green samples. The scintillators currently being used at the TileCal will not be effected that much during the HL-LHC.

The TileCal's performance will be affected by the HL-LHC as more data will be generated and the current TileCal system will not be able to keep up. The Phase-II upgrades of the TileCal will enable the TileCal system to keep up with the flow of data since the trigger architecture is redesigned.

For future work, the Demonstrator still needs to be tested after insertion into ATLAS. This will require implementation of several diagnostic tests available in MobiDICK into the certification procedures for the upgraded electronics, in order to allow for fast and reliable diagnosis. This includes the stuck bits test. Furthermore, the study of the irradiation of plastic scintillators is important in order to identify new materials for the construction of new experiments beyond the HL-LHC.

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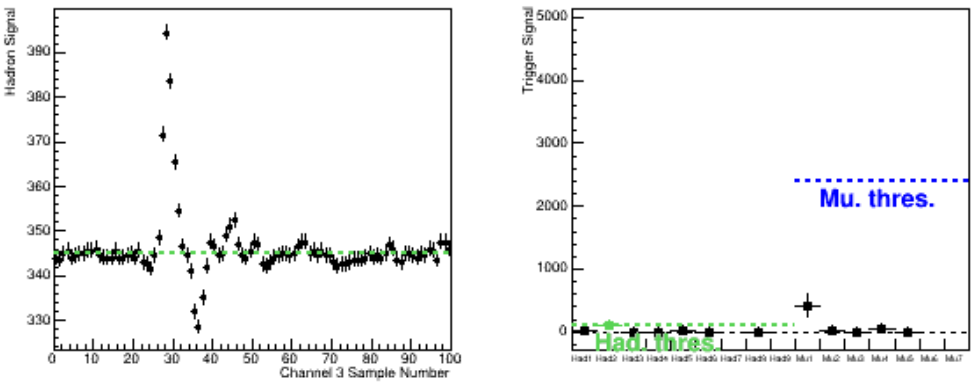
[65] V. Baranov et al, *Effects of neutron radiation on the optical and structural properties of blue and green emitting plastic scintillators*, 2018 Nuclear Instruments and Methods B 436 p236-243.

Appendix A

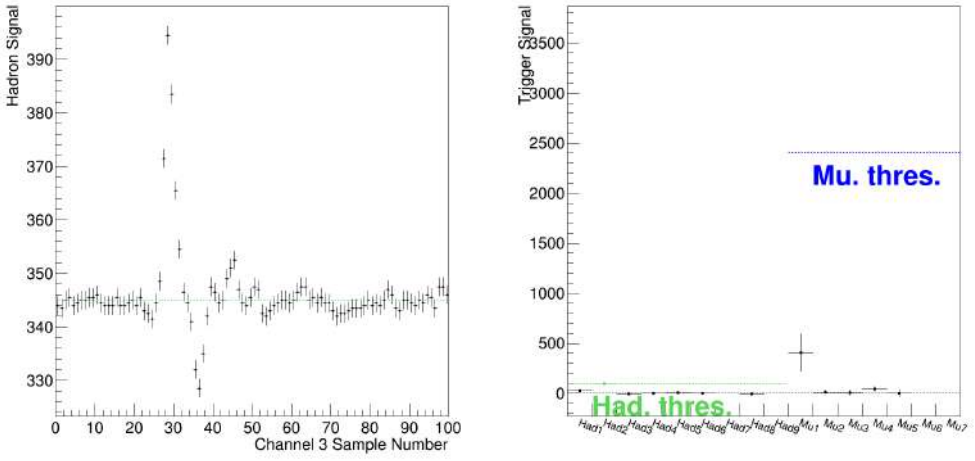
Tests performed on the FE system

Figure A.1 and A.2 shows more results of the tests that were performed on the super-drawer. Figure A.1(a) shows results of the adder tests that failed. In the figure, we see that there is no signal from the 3-in-1 card on the hadron adder for channel 3. This means that an analogue sum has not been performed by the adder card. Figure A.1(b) also shows a bad adder signal for the hadron trigger tower. For empty channels we do not expect to get any signals on the adders, this is seen Figure A.2(a). On the figure we see that there are no hadron signals for the trigger, so the adder cannot perform an analogue sum on empty channels

Figure A.3 shows results from the tests that were performed on the digitizers that were not working properly. On the Figure A.3(a) we see how a pulse shape looks like for a digitizer is not working properly and on Figure A.3(b) we see how a bad pulse shape looks likes when the digitizer has a problem with the low gain.

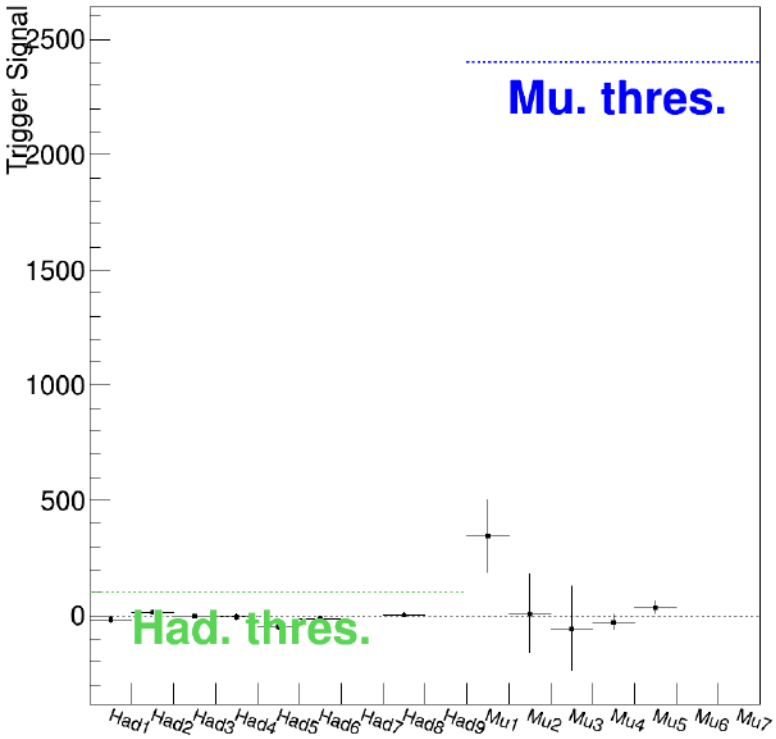


(a) Bad adder signal for channel 3

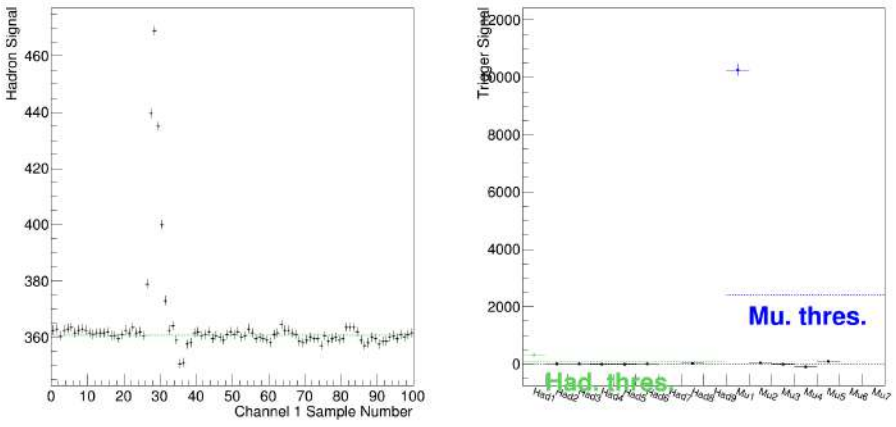


(b) Bad adder signal for the hadron side of the trigger

Figure A.1: More results on the test performed.

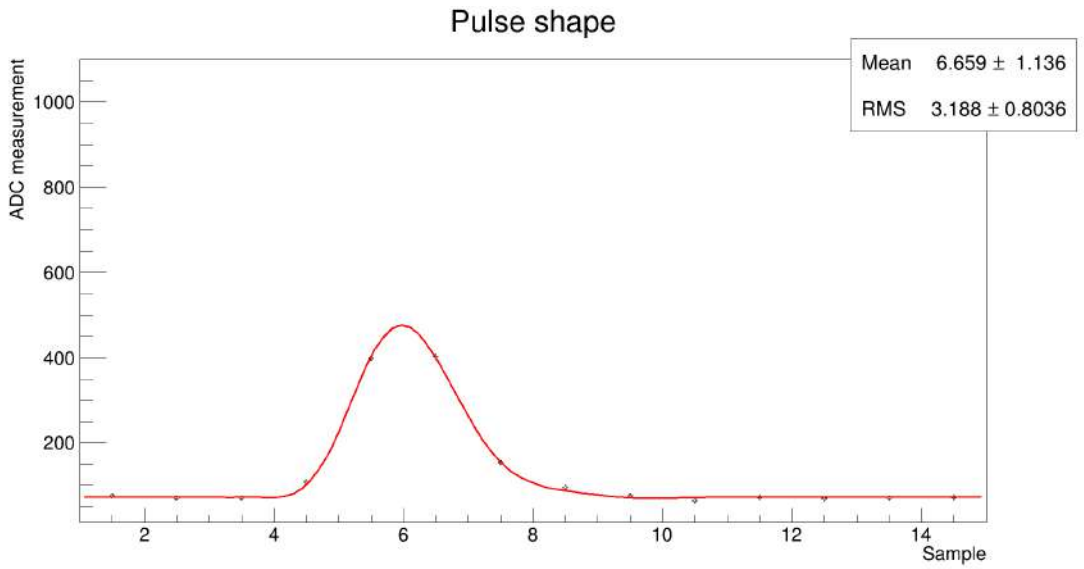


(a) Adder response for empty channel

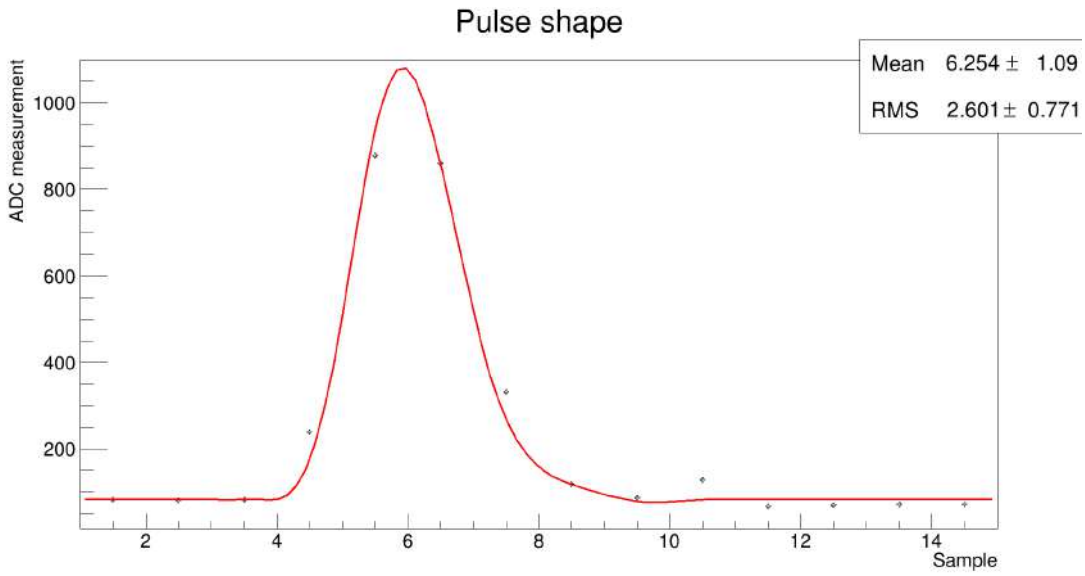


(b) Good adder signal

Figure A.2: More results on the test performed.



(a) Bad pulse shape



(b) digitizer with a low gain problem

Figure A.3: More results on the test performed.

Appendix B

More Demonstrator certification results

The integrator linearity test results for gain 4 are shown on Figure B.1 and B.2. On these figures we see how the Demonstrator performed for this gain. For mini-drawer 1 (Figure B.1(a)) we see that all the channels for this drawer are working fine for the integrator with gain 4. This is the same for mini-drawer 2 (Figure B.1(b)) since all the channels are working properly for this gain.

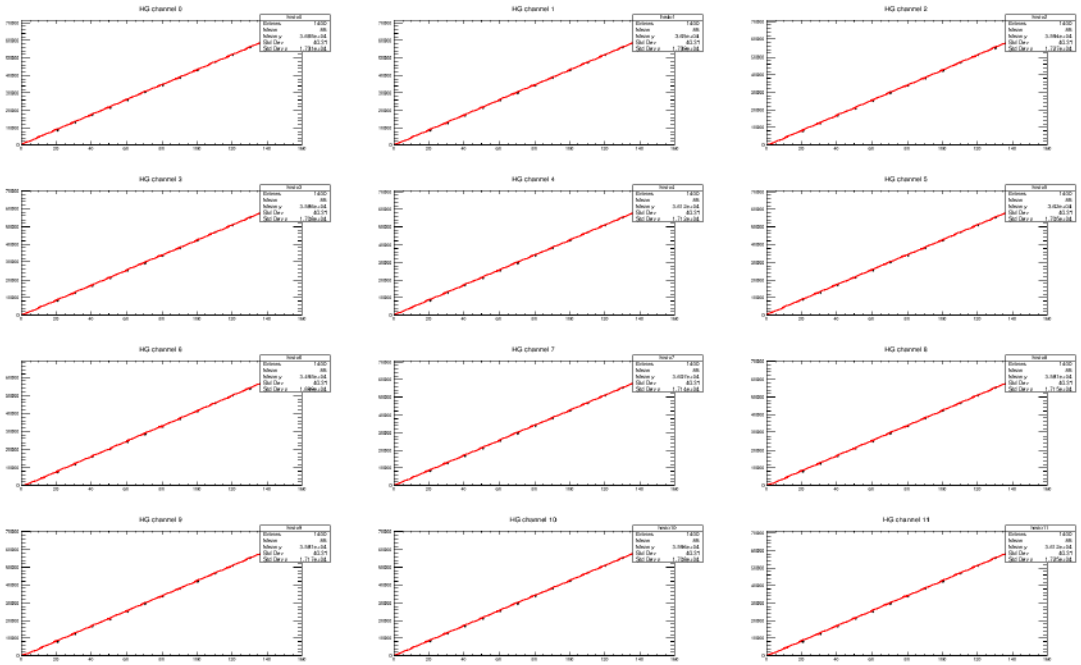
For channel 31 and 32 on mini-drawer 3 (Figure B.2(a)) there is no signal. This is because on these slots there are no PMTs hence empty channels. Channel 33 does not follow the same trend as the other channels, this is because there is something wrong with the 3-in-1 card for this channel. On mini-drawer 4 (Figure B.2(b)) channel 36 behaves like channel 33 of mini-drawer 3. This means that there is a problem with the 3-in-1 card of this channel. There is an empty slot on channel 43 of this mini-drawer as well. The rest of the channels are working properly.

The integrator linearity results of mini-drawer 1 (Figure B.3(a)) and mini-drawer 2 (Figure B.3(b)) for gain 5 are all good, meaning that everything for these mini-

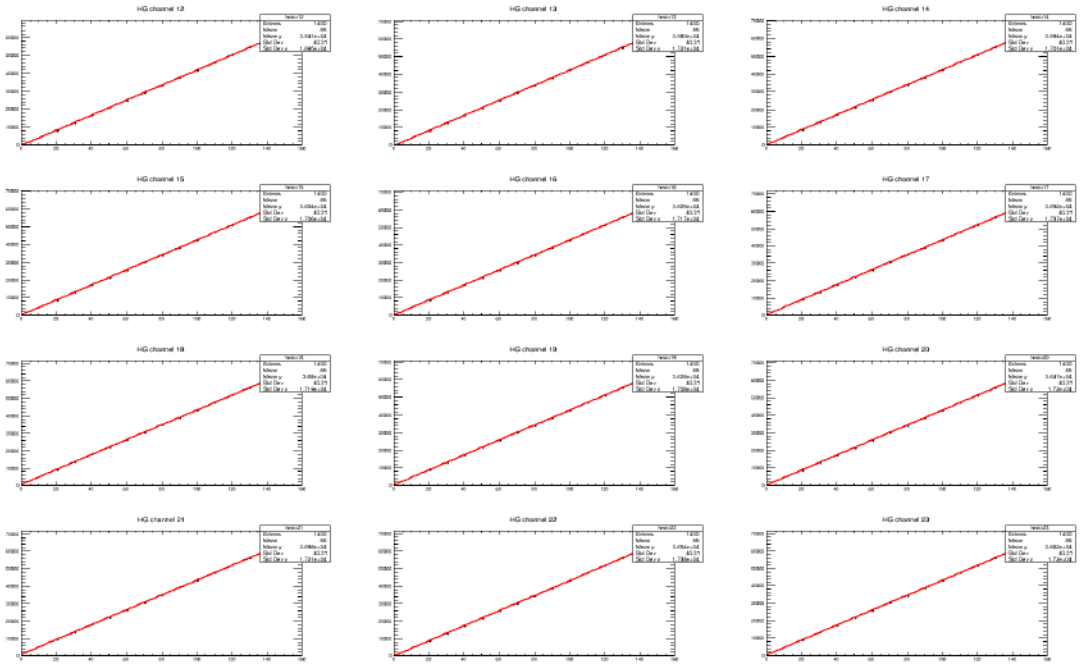
drawer is working fine. On mini-drawer 3 (Figure B.4(a)) all channels are okay except for channel 31, 32 and 33. We already know that on channel 31 and 32 we have empty slots, but on channel 33 we do have a PMT there, but it behaves like there is nothing. This can only mean that the integrator circuitry on the 3-in-1 card of this channel is sensitive to this gain. For mini-drawer 4 (Figure B.4(b)), the channels all are working properly except for channel 36, which shows to be not working proper. This is expected since it was not working properly for the previous gains.

Again, all the channels for mini-drawer 1 (Figure B.5(a)) and mini-drawer 2 (Figure B.5(b)) for gain 6 are working properly. This means that the integrator circuitry in the 3-in-1 cards of these channels are working. The same problems that we encountered with gain 5 are also encountered on gain 6.

For all the gains, mini-drawers 1 and 2 all have their channels working, but from gain 3 going up channel 33 and 36 are not working properly. As mention above, this is because of the integrator circuitry on the 3-in-1 cards of these channels. This is fixed by replacing the 3-in-1 cards of the problematic channels.

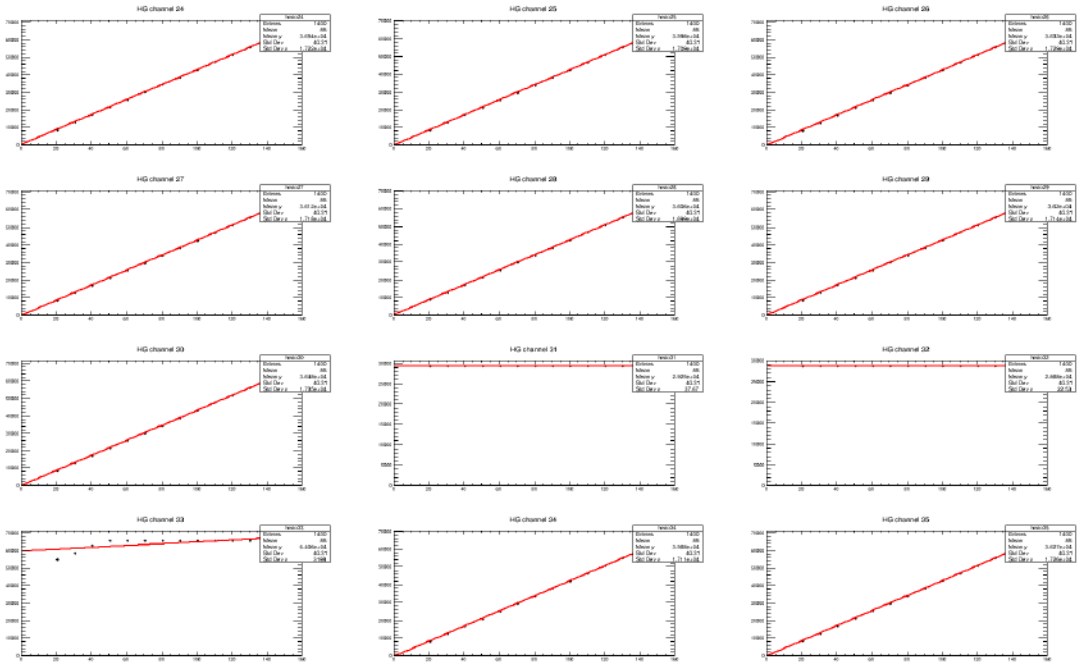


(a) mini-drawer 1

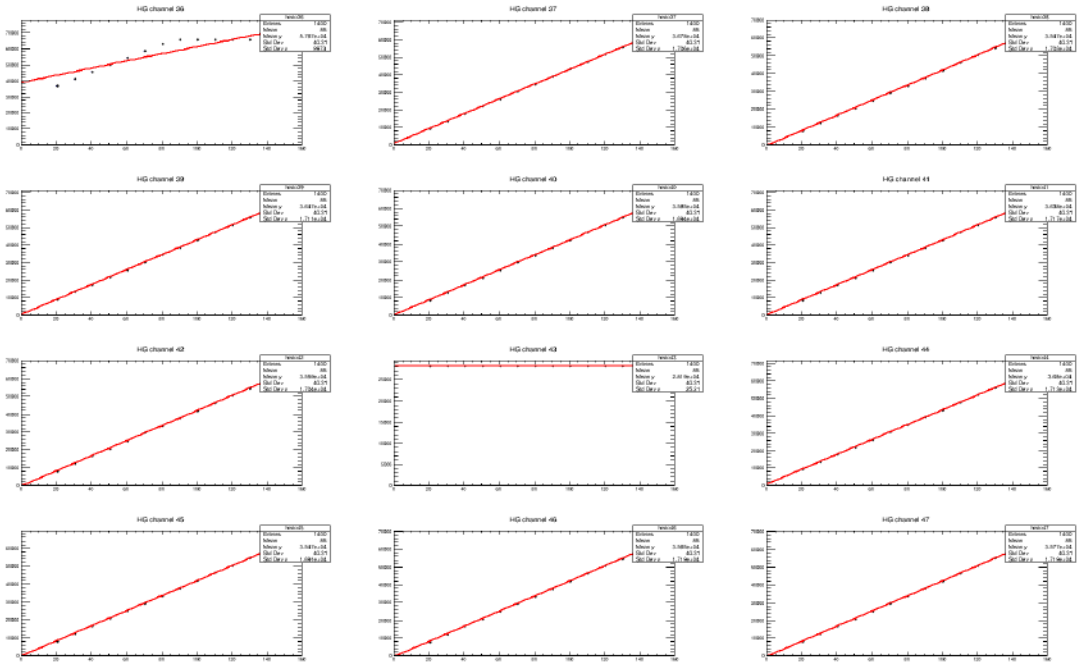


(b) mini-drawer 2

Figure B.1: Integrator Linearity test results for gain 4 (mini-drawer 1 and 2).

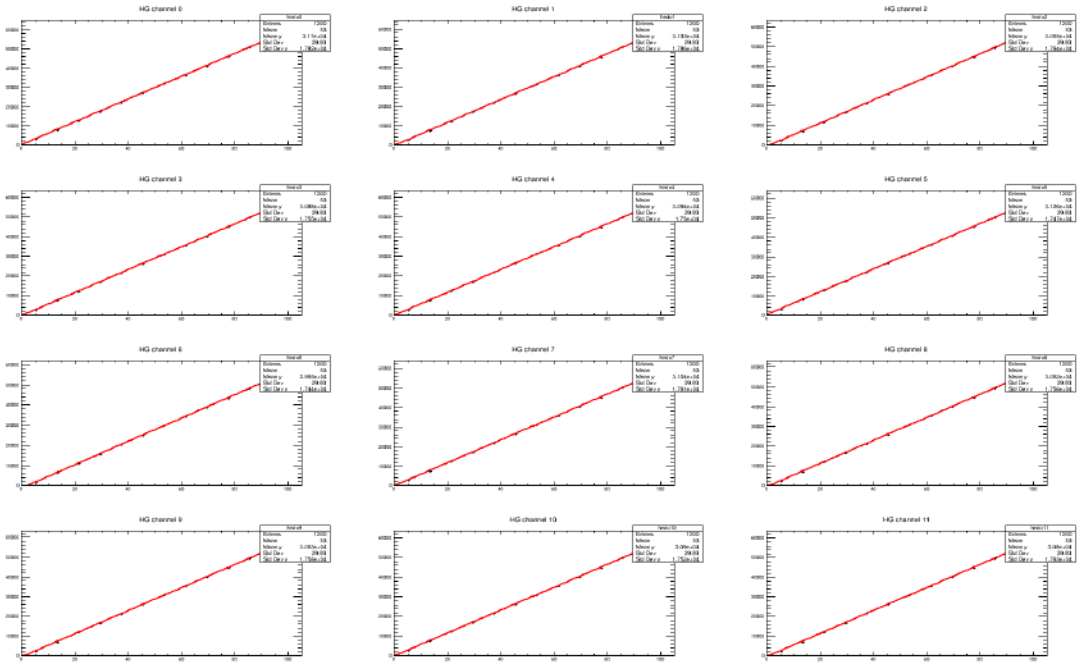


(a) mini-drawer 3

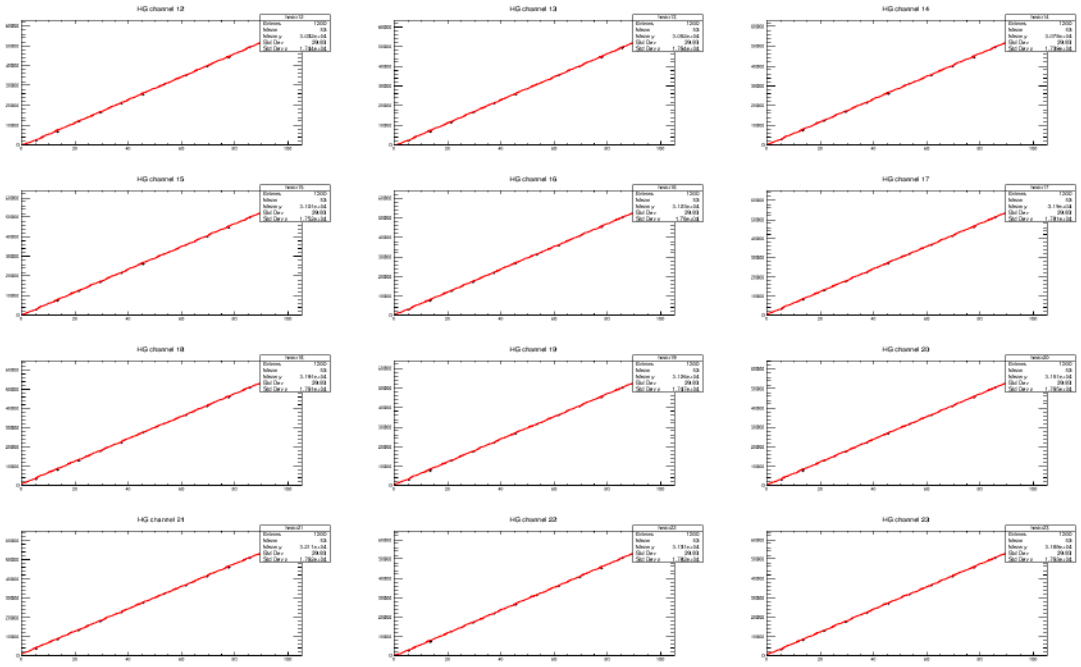


(b) mini-drawer 4

Figure B.2: Integrator Linearity test results for gain 4 (mini-drawer 3 and 4).

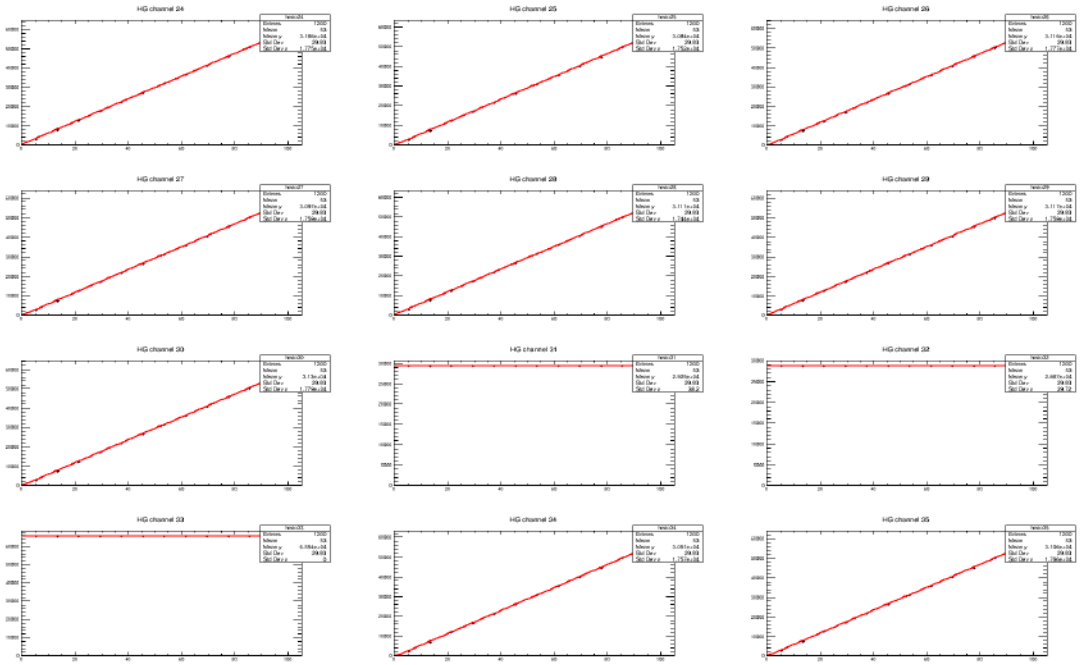


(a) mini-drawer 1

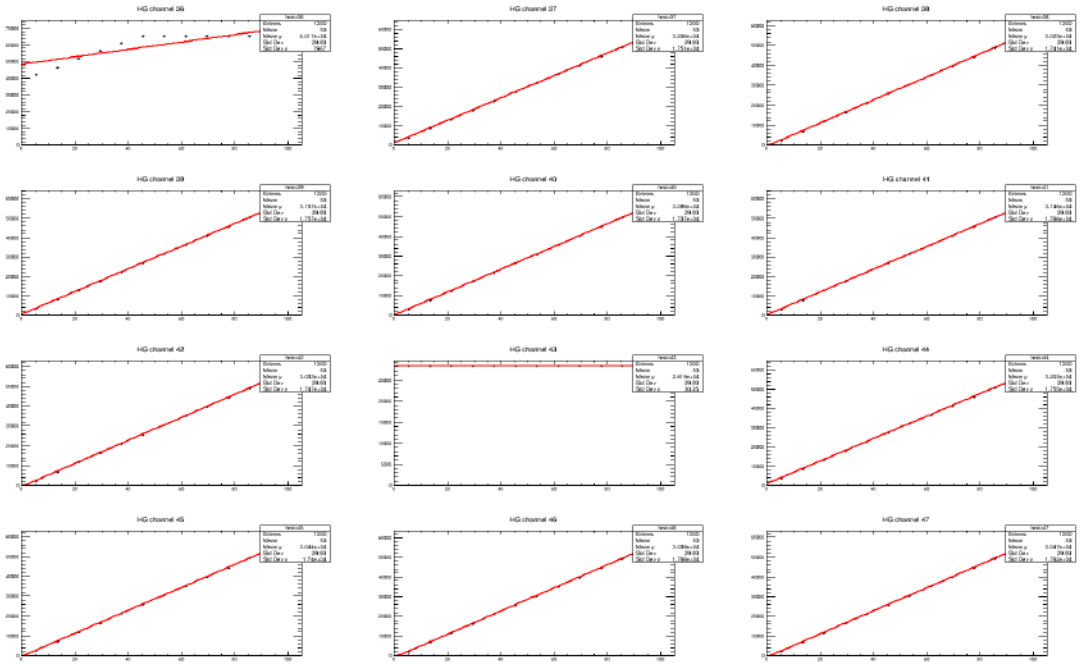


(b) mini-drawer 2

Figure B.3: Integrator Linearity test results for gain 5 (mini-drawer 1 and 2).

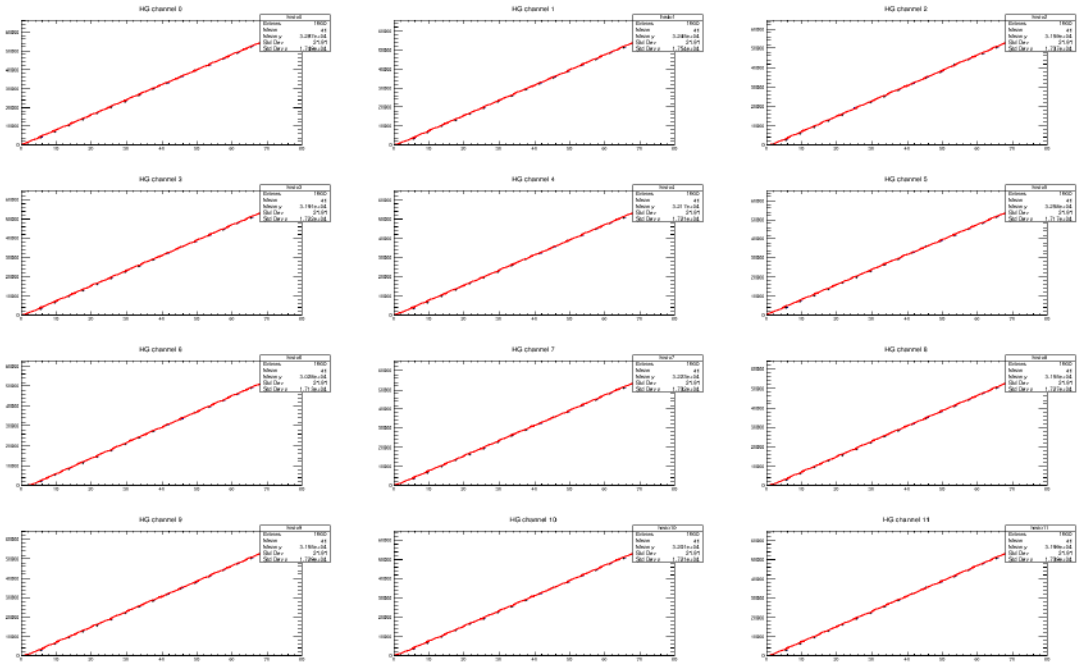


(a) mini-drawer 3

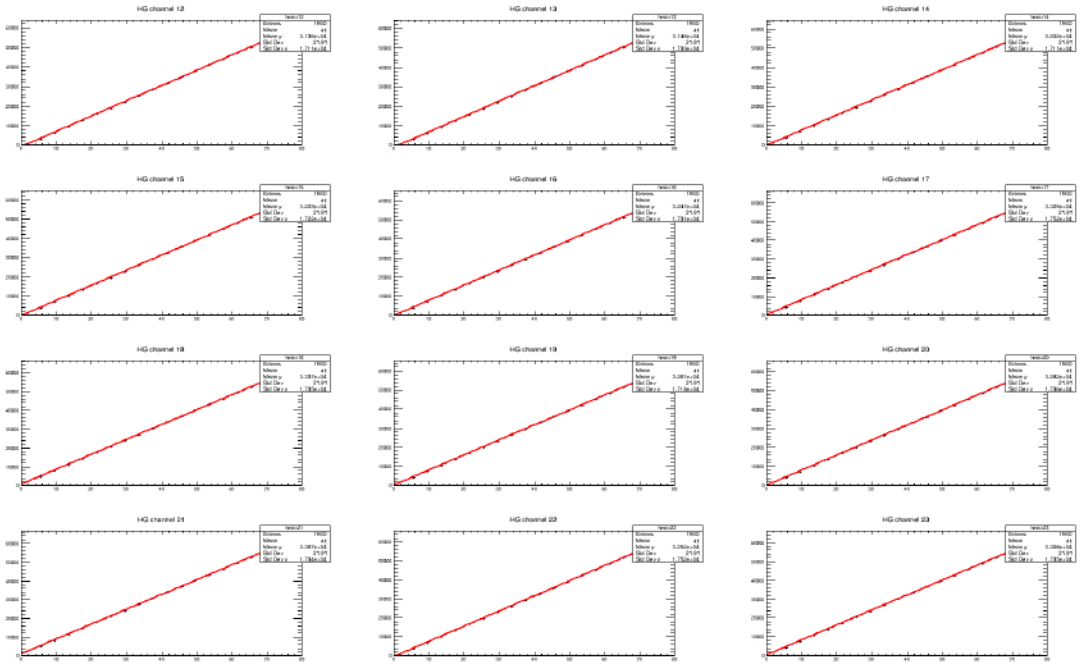


(b) mini-drawer 4

Figure B.4: Integrator Linearity test results for gain 5 (mini-drawer 3 and 4)

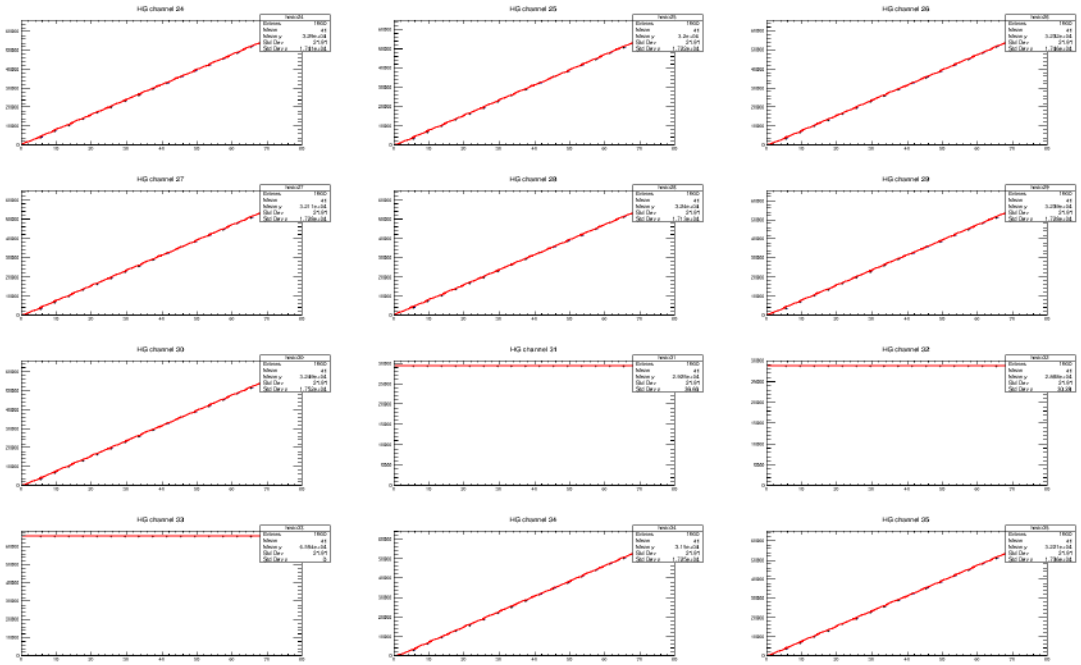


(a) mini-drawer 1

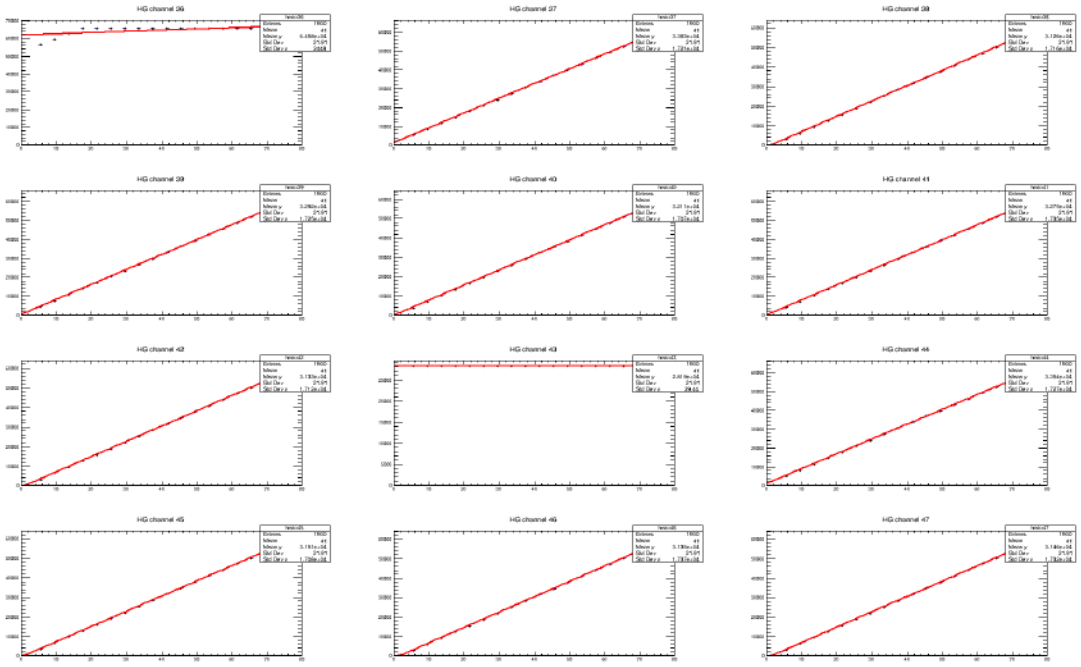


(b) mini-drawer 2

Figure B.5: Integrator Linearity test results for gain 6 (mini-drawer 1 and 2)



(a) mini-drawer 3



(b) mini-drawer 4

Figure B.6: Integrator Linearity test results for gain 6 (mini-drawer 3 and 4).

Nomenclature

ADC Analogue to Digital Converter

ALICE A Large Ion Collider Experiment

AMC Advanced Mezzanine Card

ASIC Application Specific Integrated Circuit

ATCA Advanced Telecommunications Computing Architecture

ATLAS A Toroidal LHC Apparatus

BCID Bunch Crossing Identifier

BE Back-End

CERN Centre European pour la Recherche Nucleaire

CIS Charge Injection System

CMS Compact Muon Solenoid

CPU Central Processing Unit

CRC Cyclic Redundancy Check

CTP Central Trigger Processor

DAC Digital to Analog Converter

DAQ Data Acquisition

DCS Detector Control System

DMU Data Management Unit

DQ Data Quality

DSP Digital Signal Processor

DVS Diagnostic and Verification System

EB Event Builder

EBA Extended Barrel A side

EBC Extended Barrel C side

EF Event Filter

EM Electromagnetic

ERS Error Reporting System

FATALIC Front-End ATLAS Tile Circuit

FE Front-End

FEB Front End Board

FELIX Front-End Link eXchange

FPGA Field Programmable Gate Array

FSM Finite State Machine

HG High Gain

HL-LHC High-Luminosity LHC

HLT High Level Trigger

HOLA High-Speed Optical Link

HV High Voltage

HVPS High Voltage Power Supply

IGUI Integrated Graphical User Interface

L1A Level 1 trigger Accept

L1Calo Level 1 Calorimeter

L1Topo Level 1 Topological Trigger

LBA Long Barrel A side

LBC Long Barrel C side

LG Low Gain

LHC Large Hadron Collider

LS Long Shutdown

LTP Local Trigger Processor

LTPi Local Trigger Processor Interface

LVL1 Level 1 trigger

LVL2 Level 2 trigger

LVPS Low Voltage Power Supply

OF Optimal Filtering

OKS Object Kernel System

PCI Peripheral Component Interconnect

PCIe PCI express

PMT Photo Multiplier Tube

PPr PreProcessor

PU Processing Unit

QIE Charge Integrator and Encoder

ROB Read-Out Buffer

RoI Region of Interest

ROS Readout System

SM Standard Model

TDAQ Trigger and Data Acquisition

TM Transition Module

TTC Timing, Trigger and Control

TTCex Timing, Trigger and Control Encoder Transmitter

TTCoc TTC Optical Coupler

TTCpr TTC receiver and PMC Form Factor

TTCvi Timing, Trigger and Control VME Interface

VME Virtual Machine Environment

WLS Wavelength Shifting