VOLTAGE DIP COMPATIBILITY TESTING FOR VARIABLE SPEED DRIVES

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A dissertation submitted to the Faculty of Engineering, University of the Witwatersrand, in fulfilment of the requirements for the degree of Master of Science in Engineering.

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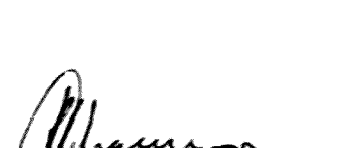
DECLARATION

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination in any other University.



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ABSTRACT

Voltage dip sensitivity of variable speed drives (VSDs) plays a major role in dip compatibility design. Collaboration between WITS, Eskom and EPRI resulted in the development of a dip testing facility at WITS. This report presents a test procedure for dip testing of VSDs at WITS. To accurately test for, and compare equipment sensitivity, there has to be a consistent process – develop criteria, observe protocol and develop methodology. The objectives, test criteria, test specifications, and reporting formats all contribute to consistent testing and relevant result comparisons. It is concluded that testing requires proper characterisation of voltage dips and knowledge of their effect on equipment to design a test procedure. Another conclusion is that to optimise the testing process, one has to consider the variety of impacts of dips on different equipment. It is recommended that the test process be further optimised and applications be sought for the test program.

In memory of my dear friend Darryl Cloete, a brilliant engineering student, who dreamt of us all achieving great things, but whose life came to a tragic end, before completing his undergraduate degree.

ACKNOWLEDGEMENTS

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NOMENCLATURE

AC	Alternating Current
A/D	Analogue To Digital
ASD	Adjustable Speed Drive
CBEMA	Computer Business Manufacturer Association
CSI	Current Source Inverter
D/A	Digital To Analogue
DC	Direct Current
DMA	Direct Memory Access
LV	Low Voltage
EHV	Extra High Voltage
EPRI	Electric Power Research Institute
EMC	Electromagnetic Compatibility
ESKOM	Electricity Supply Commission
GTO	Gate Turn Off Thyristor
HV	High Voltage
IEEE	Institute Of Electrical And Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
LV	Low Voltage
MV	Medium Voltage
PC	Personal Computer
PCC	Point Of Common Coupling
PEAC	Power Electronic Application Center
PLC	Programmable Logic Controller
PQ	Power Quality
PWM	Pulse Width Modulation
SLG	Single-Line-To-Ground fault
UNIPEDE	International Union Of Producers And Distributors Of Electrical Energy
VSD	Variable Speed Drive
VSI	Voltage Source Inverter

1 INTRODUCTION

1.1 Problem Statement

The cost to industry of voltage dips, due to loss of production, is estimated at R1.2 billion [1]. This loss of production can be attributed to the tripping of equipment due to the voltage dips. Solutions can only be devised if the behaviour of equipment during voltage dips is known. Therefore, it is essential to have data available on equipment sensitivity to dips. The testing of equipment to accumulate data cannot be done on an ad hoc basis. To accurate test and compare equipment sensitivity, there has to be a consistent process – develop criteria, observe protocol and develop methodology.

Hypothesis:
To optimise the dip testing process, one has to consider the variety of impacts of dips on different equipment.

1.2 Background

Voltage dips are a common cause of plant disruption and are the result of a fault at one point on the electricity supply network causing the voltage at another point to reduce. The type of voltage dip depends on the type of fault (e.g. single line to ground fault, three phase fault, etc). During the voltage dip, a change in magnitude and phase of the voltage waveform of one or more input supply lines can occur. These voltage dips can interfere with the operation of equipment connected to the mains supply.

To investigate the effect of voltage dips on industrial equipment a voltage dip test facility was set up at the University of the Witwatersrand in conjunction with Eskom, the South African national supply utility. The voltage dip test facility (and onwards called the PQ test lab) was developed to be completely flexible so that voltage dips with adjustable dip magnitude and phase shift during the dip can be generated independently for each of the supply phases. Together with the other voltage dip parameters that can be specified, this flexibility allows virtually any complex voltage dip to be generated.

The initial goal of the PQ test lab was to test for the susceptibility of variable speed drives (VSDs) to voltage dips. Future design of the PQ test lab will facilitate the testing of other equipment and for other power quality disturbances, as these will also have an impact on industry processes.

VSDs are used in many industrial applications but, being electronically based, can be susceptible to power disturbances. Voltage dip testing was performed on commercial VSDs to determine the response of the drives during voltage dip conditions. Results from these tests can be used by the utility (Eskom), and by customers to determine the effect of voltage dips on plant, and by drive manufacturers to improve the voltage dip performance of their product. More importantly, the required dip performance of drives can be included in the specification of new plant and in the retrofitting of existing equipment.

The testing of variable speed drives has been undertaken by EPRi-PEAC and Clemson University in the US before the testing program at the University of the Witwatersrand started. There, testing had been more broadly covered in a test protocol SC-610 [6]. This forms part of the system compatibility research conducted at PEAC. Not only does this testing program extend beyond voltage dips in immunity testing, but other aspects of the variable speed drive performance are also addressed.

In South Africa, it has been decided that a focus on voltage dip immunity testing is a first priority in developing a broader test program for VSDs. This should be seen in the light of voltage dips being the most pressing power quality problem in South Africa and the sponsorship by the Power Quality Research Portfolio (of the test facility). The objectives of this report are to describe the development of dip testing requirements, protocol and methodology in South Africa.

1.3 Report Structure

The report starts by establishing the need in industry to consider dip compatibility design, and consequently the need for dip testing. Chapter two discusses this in two parts. Firstly the philosophy for dip compatibility design is explored and then testing experience in the USA is discussed as an example of international initiatives.

Chapter three discusses the first of two important aspects of voltage dips – that of the electrical environment where they originate and a means to describe these phenomena in a way that is applicable to their impact on plant equipment. Chapter four continues this theme, extending it to the impact of voltage dips on equipment, especially variable speed drives.

Chapter five formalises a dip testing protocol, drawing from international experience, guidelines, standards and the activities of working groups in the USA and Europe. The objectives for testing, the criteria for establishing accurate results, the test environment, equipment specifications and reporting formats are discussed in detail.

Chapter six continues by firstly discussing the voltage dip test facility in South Africa. Thereafter, it discusses the preparations that are done before testing and the development of the underlying methodologies and step-by-step processes that are applied to conduct dip testing.

Finally, chapter seven explores the hypothesis applied to variable speed drives, i.e. that the results of the testing program have made available data that reveals the impact of a variety of dip parameters on the different variable speed drives – PWM, CSI and DC drives. This has consolidated the economic viability of the test program, requiring that not all parameters are equally important to all the drive types.

2 DIP COMPATIBILITY DESIGN – ESTABLISHING A NEED FOR VOLTAGE DIP TESTING

It is important to be able to quantify the sensitivity of plant equipment to dips in order to predict plant losses, desensitise such equipment and improve plant performance. To understand the need for testing worldwide, one needs to investigate the need for dip compatibility design and the testing facilities that support these designs.

2.1 Dip Compatibility and Industry Concerns

System compatibility in the electricity supply industry (ESI) is the study of matching electrical equipment to the electrical supply. Dip compatibility covers one area where supply disturbances called voltage dips impact on equipment performance in the electrical environment. A dip compatibility study usually aims to quantify the susceptibility of equipment to dips and to increase their immunity to these disturbances. Tackling supply disturbances directly at the utility level (supply side) is usually more expensive than identifying existing sensitive plant (behind-the-meter) and implementing remedial measures, or specifying new equipment with adequate immunity.

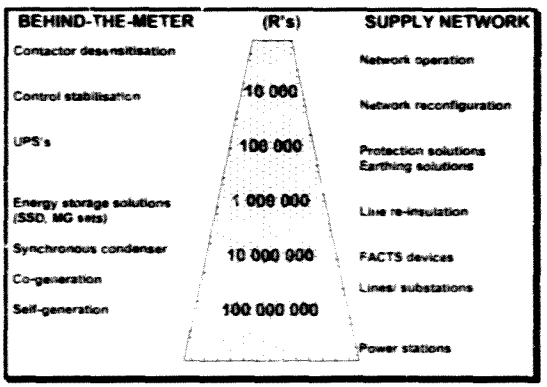


Figure 2.1 Relative costs of behind-the-meter and utility network solutions [1]

The components of the decision process are summarised in Figure 2.2 below. The fault performance of the network in the zone of sensitivity and an improvement in dip immunity levels will reduce the number of process interruptions significantly.

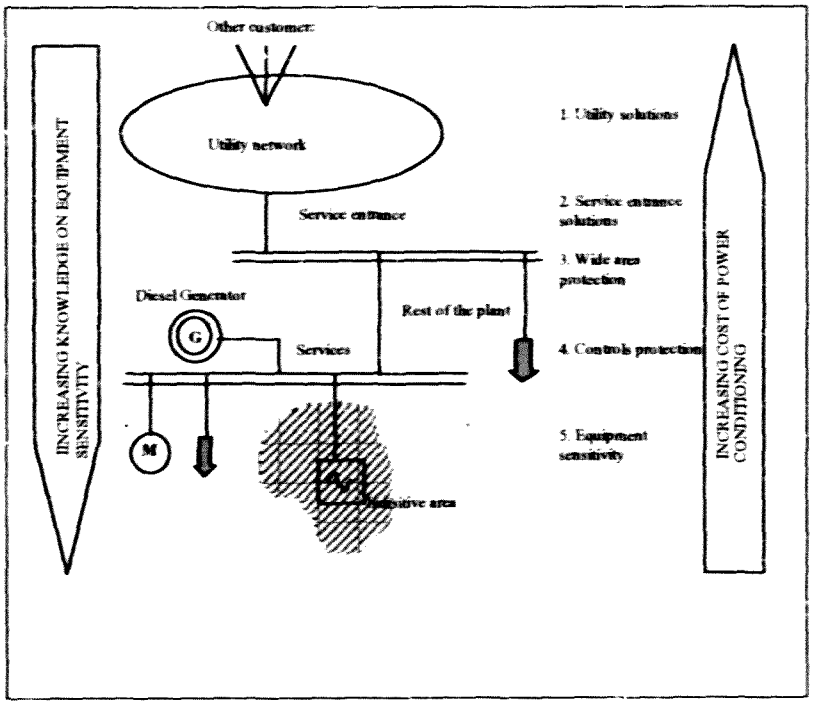


Figure 2.2 An illustration of the zone of sensitivity in which voltage dips will affect industrial processes. Different levels of decision making for increasing process immunity are shown.

The design philosophy applied to dip compatibility in a plant will depend on the frequency of events as well as on the sensitivity of the plant process to dips. A guide on design considerations and strategies can be found in [1].

These philosophies can be categorised according to the design goal as follows:

- Complete immunity (full protection) of the plant
- Compatibility design aimed at meeting pre-determined compatibility limits
- Compatibility design based on techno-economic optimisation

Different philosophies can also be applied at different sub-processes within a plant or to the plant as a whole. These philosophies can be categorised as follows:

- Critical processes (for example, from a safety point of view)
- Important processes (for example, resulting in operational damage or loss of production)
- Other processes that can be momentarily interrupted without significant impact on the plant.

2.1.1 Complete immunity

Complete immunity could be typically required by environmental, safety or security considerations. There could be a number of reasons as to why these requirements should be met that have nothing to do with the plant process or economic issues.

2.1.2 Meeting compatibility levels

Setting compatibility levels may be a result of agreements between a utility and its customers. The quantification of such levels may be different from utility to utility or may have an influence nationwide or internationally. Figure 2.3 shows compatibility concepts as specified in the NRS 048-1:1996 [19]. This is based closely on the IEC electromagnetic compatibility design philosophy for steady-state parameters such as harmonics and flicker.

Figure 2.4 shows the Computer Business Equipment Manufacturers Association (CBEMA) curve [2]. These two methods of quantifying compatibility levels are used in South Africa and the USA respectively.

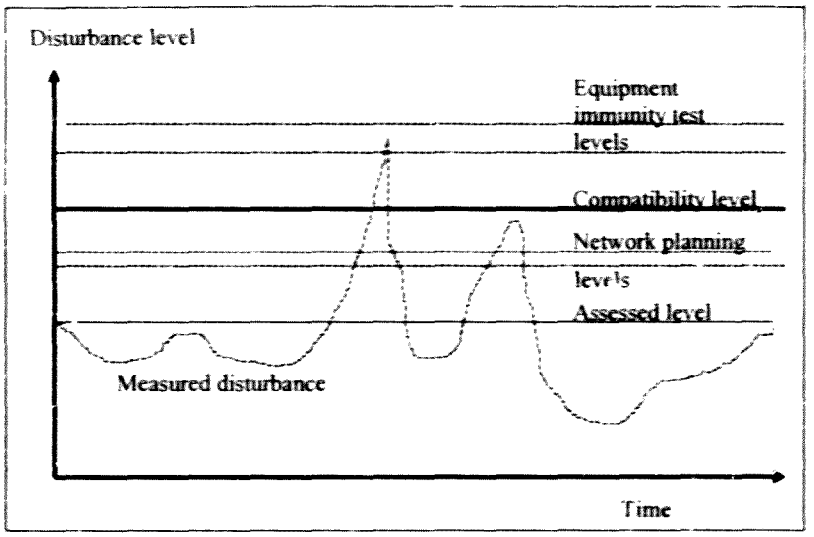


Figure 2.3 Illustration of basic compatibility concepts [19]

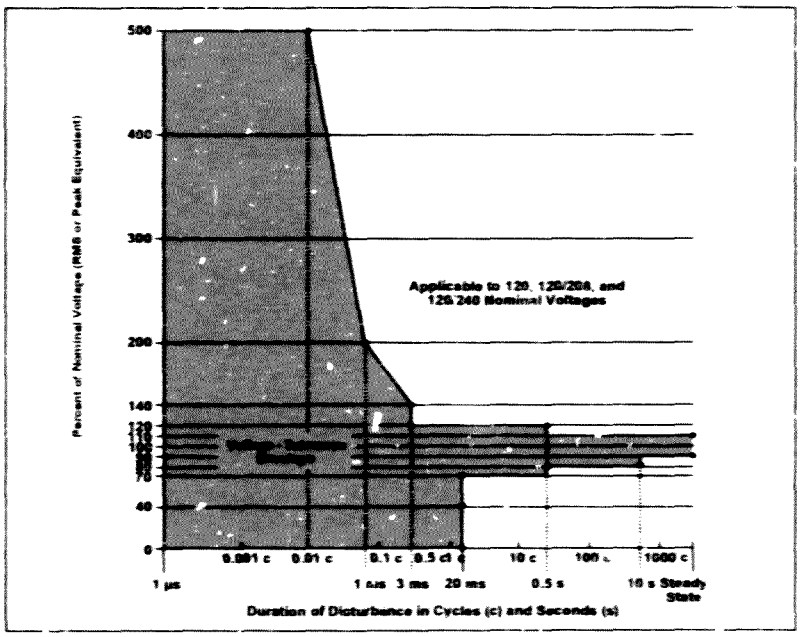


Figure 2.4 The CBEMA curve [6] was initially developed for computer equipment. It has since been developed for all categories of equipment with boundary levels as shown.

The philosophy of meeting compatibility levels is characterised by

- Agreements to meet design and performance targets set by utilities, plant operators and equipment suppliers. For example, the SEMI standards [1] were developed by utility representatives (PEAC, SRP and TU Electric), semiconductor manufacturers (AMD, IBM, Intel, Rockwell, Motorola, National, TI and SEMA TECH) and equipment suppliers (Applied materials, LAM Research, SCP Global, SVGL and FSI)
- A strong emphasis on plant and equipment design specifications and testing
- A clear definition of utility vs. industrial responsibilities in improving performance and immunity

This method avoids detailed cost assessments initially, but further optimisation may be required as experience is gained with the utility and plant compatibility.

2.1.3 Techno-economic optimisation

Techno-economic assessments require the existence of prior information (measured or predicted) of the utility performance and information on the sensitivity of the plant process to dips. The goal is to implement the most cost-effective solution (Figure 2.5).

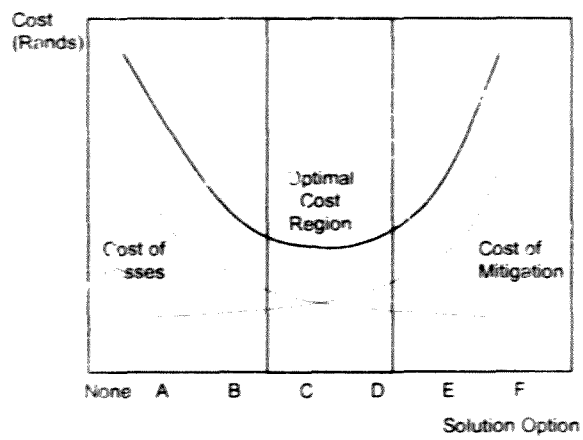


Figure 2.5 The optimisation of cost of solution for a techno-economic evaluation

There are many reference documents to describe utility performance and the voltage dip environment. Some of these will be discussed in chapter 3 and 5 respectively. The IEEE provides a dip environment chart (Figure 2.6) on typical dip environment for designers and users to design plant compatibility. The information used is based on a measurement exercise called the Distribution Power Quality (DPQ) Project conducted in the early 1990's in the USA [11].

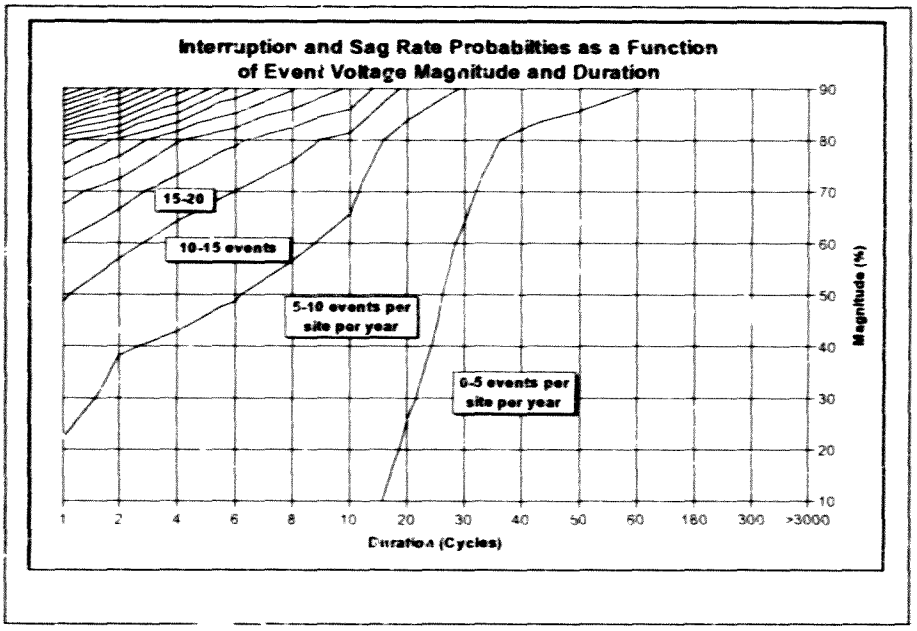


Figure 2.6 The IEEE dip environment chart [2]

Together, the IEEE dip environment chart and the CBEMA curve provide a frame of reference for techno-economic evaluations.

In summary, this philosophy is characterised by an emphasis on:

- Accurate measures of cost of losses
- Specific dip performance at the point of supply
- Determining actual plant sensitivities
- Selecting a wide range of solutions
- Investigations that compare the cost of behind-the-meter solutions with supply-side solutions

2.2 Testing Facilities in the United States

The National Motors and Drive Steering Committee (NMDSC) Meeting is held twice a year in the USA. End-user and manufacturer issues are discussed at these meetings. In the April 1999 meeting, a special presentation was made regarding the availability of testing facilities for variable speed drives in general. It was noted that there are five such laboratories in the USA [3]:

- Oregon State University (Motor and Drive Resource Facility), Corvallis, Oregon
- Advanced Energy (IEL), North Carolina
- Quebec Hydro Electric Utility (LTEE), Quebec, Canada
- Power Electronics Application Center (PEAC), EPRI/ University of Tennessee, Knoxville, Tennessee
- ORNL Electric Machinery Center, Oak Ridge, Tennessee

Of these, Oregon State University and PEAC (in collaboration with Clemson University in South Carolina), may do dip testing as well. The need for independent test facilities was discussed at length. Surprisingly, drive manufacturers have the greatest need for these facilities, as they say that their customers insist on independent testing. The potential users of these facilities were identified as:

- Government Agencies (Department of Energy)
- International Organisations (IEC)
- Agencies (UL, CSA)
- Universities (OSU)
- Motor Manufacturers (US Motors)
- Users (El DuPont)
- Original Equipment Manufacturers (Goulds Pump)
- Societies/ Institutions/ Associations (IEEE)
- Utilities (Duke Power)
- Inventors (Thomas Edison)
- Research Groups (EPRI)
- Motor Repair Shops (EASA)

The requirements for these facilities to be successful were identified as:

- Accreditation
- Accuracy
- Recognition
- Sponsors
- Funding
- University Affiliation
- Industrial Acceptance
- Program Capability Awareness
- Industry Technical Support
- Success Stories

A representative from the department of energy also had a representative at the meeting. The department provides funding for viable projects.

2.4 EPRI-PEAC Experience and Testing Programs

The "Power Electronics Application Center" (PEAC), has been instrumental in the development of dip compatibility programs as a set of tasks under the sponsorship of what is called the System Compatibility Project. PEAC has done a number of tests on variable speed drives that do not only included dip compatibility tests, but also other tests. For this a test protocol was developed, called SC610 [6], of which one section is devoted to dip immunity testing. Some of the tests performed according to SC-610, are:

- *Energy Efficiency and Performance Tests* to characterise the electrical efficiency of- the VSD itself and the overall energy performance of the VSD-motor set up.

- *Emission Tests* to characterise harmonics caused by the VSD at its supply terminals.

- *Immunity Tests* to characterise the VSDs response to power system disturbances like harmonics, dips and over-voltages.

- *SC Systems Level Tests* to investigate the system compatibility of the VSD and better understand its side effects and improve its immunity.

System compatibility criteria, their assessment and applicability had been developed in consultation with an industry advisory group. SC-610 is intended to be compatible with other industry standards, in particular the safety requirements promulgated by Underwriter Laboratories (UL), the Institute of Electrical and Electronics Engineers (IEEE), and the American National Standards Institute (ANSI).

PEAC has extensive laboratory facilities, including the dip testing facility and EMI-testing facilities amongst others. The dip testing program in South Africa is based on the program at PEAC and so the two programs are similar.

PEAC focuses on testing small (+/- 5HP) PWM drives and their test-bed has been designed to this end. A 150HP CSI drive has been tested at Clemson University. At present, a DC drive is under test. At Eskom, a 15kW PWM drive and a 120kW CSI drive have been tested as part of the local test program and the testing of a DC drive is in progress.

The dip testing facility has a different structure to that of the facility at the University of the Witwatersrand. On the load side, the PEAC test-bed is more advanced, with a programmable load fitted to the system. This facility is capable of setting adjustable inertia and torque-speed parameters. The University of the Witwatersrand test-bed has a simple resistive load bank connected to a DC generator. On the supply side, the University of the Witwatersrand test-bed is more advanced with a fully programmable amplifier supply with variable parameters (pre-dip voltage, phase shift, duration, depth, etc.). The PEAC test-bed has a simple variac-controlled utility-line supply. A diagram of the test set-up is shown in Figure 2.7.

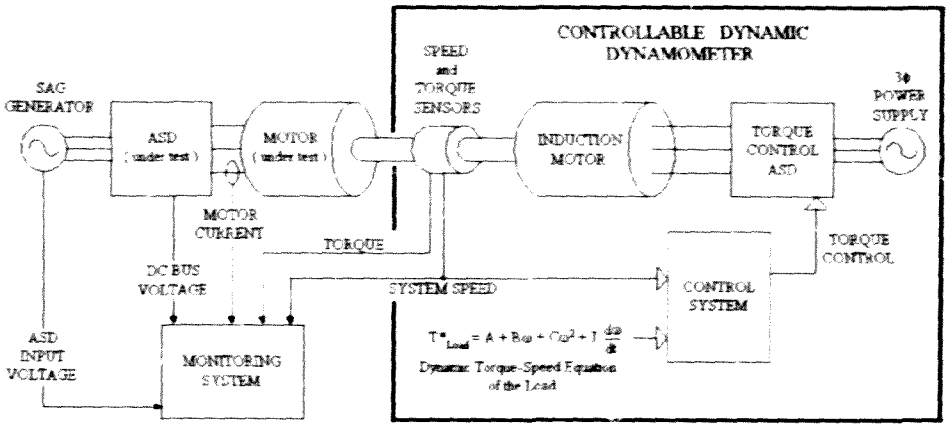


Figure 2.7 The PEAC test-bed has a highly developed programmable load, but a simple switch supply arrangement [6].

Utilities, manufacturers and customers have jointly sponsored much of the testing at PEAC. The test facility is refined to a high degree and the test units have their own special racks and housings. Testing is done more on a commercial basis than for research purposes.

The most important testing development at PEAC has been the testing of 17 5Hp PWM drives under the "Task 1" umbrella of the System Compatibility Project at the end of 1994. Traditional voltage dip testing of three-phase VSDs dictates that all three phases of a dip are dipped at once. This is a balanced dip condition and is the type of testing specified in IEC-1000-4-11 [7]. A variable dip is considered optional in the testing guidelines of this standard. However, field studies and large-scale measurement projects have shown that most dips are unbalanced one- and two-phase dips. One of the goals of the "Task 1" exercise was to reconcile these differences.

In South Africa, it has been decided that a focus on voltage dip immunity testing is a first priority in developing a broader test program for VSDs. This should be seen in the light of voltage dips being the most pressing power quality problem in South Africa and the sponsorship by the Power Quality Research Portfolio (of the test facility).

As a result of collaboration between EPRI-PEAC and Eskom, it was decided to combine efforts in this area of dip compatibility testing. In terms of the SC-610 test protocol, this includes sections in the document on dip testing of VSDs. Although some of the sections of SC-610 have been changed, these changes have never been formalised and the SC-610 document remains unchallenged for dip testing at PEAC.

The collaboration between PEAC and Eskom aims to arrive at a more internationally applicable protocol for voltage dip testing. During a recent visit to the US, some US drive manufacturers expressed an interest in dip testing for the benefit of their European customers. A standard protocol for test results worldwide would benefit comparing results from different facilities all over the world. It was proposed that PEAC and Eskom work together to establish a standard test-protocol for drive dip/sag-testing. This will help in the transfer of results between the two parties.

Three US drives were sent to South Africa via EPRI-PEAC for the purposes of duplicating under 50Hz conditions, results of testing performed previously by PEAC [27], under 60Hz conditions. The 50Hz test results from South Africa was done in a draft format based on work on the new protocol. This would make comparisons with the 60Hz test results easier. The testing in South Africa has been completed at the end of 1999, but the comparison with EPRI results is still under way.

3 DESCRIBING VOLTAGE DIPS IN THE ELECTRICAL ENVIRONMENT

3.1 Characterisation of Voltage Dips

To describe voltage dips, the definition of a voltage dip should provide a convenient starting point.

3.1.1 Voltage dip definitions

The voltage dips of Europe and South Africa are also known as voltage sags, notably in the USA. Although the two names refer to the same event, the definitions are different. This is best illustrated by dip magnitude and sag magnitude as shown in Figure 3.1. From a South African perspective, voltage dip and voltage dip magnitude will be used in this document, unless otherwise stated.

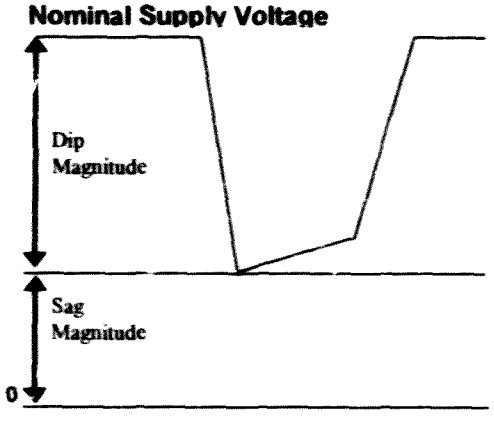


Figure 3.1 The difference between sag magnitude and dip magnitude

The definitions below are not formal definitions, but extracts from standards.

According to IEEE 1159.2-1996 draft, the definition of a voltage sag is:
" A decrease from 0.1 to 0.9 pu in rms voltage at the power frequency for 0.5 cycles to 1 minute (3600 cycles).

IEC1000-4-11-1994 says that a voltage dip is:

"A sudden reduction of the voltage at a point in the electrical system, followed by voltage recovery after a short period of time, from half a cycle to a few seconds." (Modified from IEV 161-08-10)

An adaptation from NRS-048 part I-1996, which is a South African regulatory standard, states:

"A sudden reduction in the r.m.s. voltage, for a period between 20ms and 3 s, of any or all of the phase voltages of a single-phase or a polyphase supply. The duration of a voltage dip is the time measured from the moment the r.m.s. voltage drops below 0.9 per unit of declared voltage to when the voltage rises above 0.9 per unit of declared voltage." Here the declared voltage is defined as "The voltage declared by the utility as the voltage at the point of supply." This is illustrated in Figure 3.2, taken from the NRS-048 part II-1996.

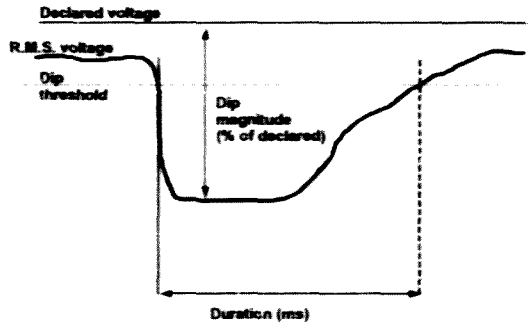


Figure 3.2 Measured voltage dip parameters [20]

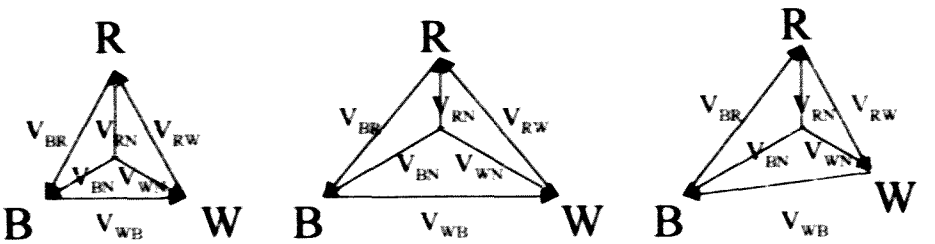
Another definition from the British Standard BS EN 50160-1995, says:

"A sudden reduction of the supply voltage to a value between 90% and 1% of the declared voltage U_C, followed by a voltage recovery after a short period of time. Conventionally the duration of a voltage dip is between 10ms and 1 minute. The depth of a voltage dip is defined as the difference between the minimum rms voltage during the dip and the declared voltage. Voltage changes that do not reduce the supply voltage to less than 90% of the declared voltage U_C are not considered to be voltage dips".

In this British standard, the declared supply voltage U_C is normally the nominal voltage U_N of the system. If by agreement between the supplier and the customer a voltage different from the nominal voltage is applied to the terminal, then this voltage is the declared supply voltage U_C. The nominal voltage is the voltage by which a system is designated or identified and to which certain operating characteristics are referred. Supply voltage is the rms value of the voltage at a given time at the supply-terminals, measured over a given interval.

Most of the definitions take on a similar focus as those shown above. These traditional views of voltage dips take only the magnitude of an rms voltage in a given time window into account. This type of description is not adequate to explain all of its effects on equipment.

Characterisation in terms of magnitude and duration provides basic information for the quantification of voltage dips. Using this understanding, we could express voltage dips in terms of rms values as in Figure 3.1 and 3.2. However, we could also express voltage dips in of phasor diagrams. Traditionally, using phasor diagrams, we could state that there are three basic voltage dip types: three-phase dips, single-phase dips and phase-to-phase voltage dips as shown in Figure 3.3. These representations would correspond to three-phase faults, single-line-ground faults and phase-to-phase faults. However, phasor representation also lends itself to using other descriptors for voltage dips, e.g. phase angle. This representation also makes the visualisation in terms of star and delta voltages possible. It makes sense to first evaluate these possibilities.



(a) Three-phase dip **(b) Single-phase dip** **(c)Phase-to-phase dip**

Figure 3.3 The three basic voltage dip types

3.1.2 Phase and line voltage magnitude changes

As can be seen in Figure 3.3, when the phase voltage waveforms change during a voltage dip, the line voltage waveforms can be affected differently. If the equipment is delta-connected (such as the three-phase power supplies and AC motor drive) and the line voltage waveforms are used as a reference, the dips can be differently categorised. References [2,3] describe the types of voltage dips experienced by star and delta connected loads depending on the fault categorisation. This leads to the dif types illustrated in Figure 3.4. A delta connected AC drive will experience only A,C and D type dips.

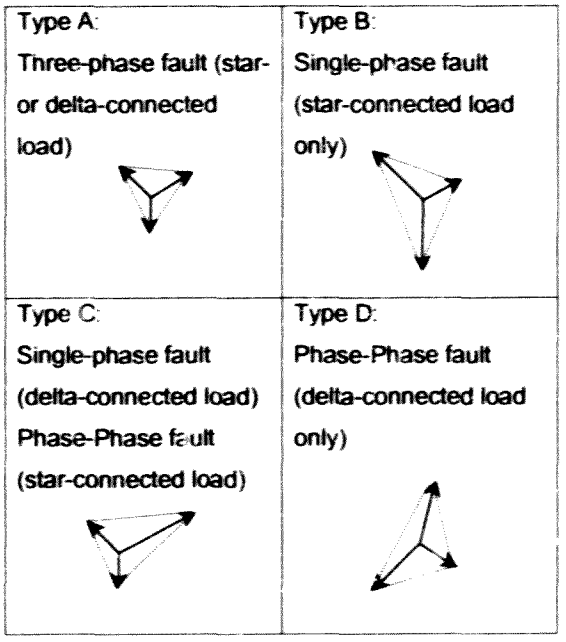


Figure 3.4 Vector diagrams illustrating four types of voltage dips in terms of line and phase voltages

Another consideration for equipment is that voltage dips may have their origin elsewhere in a power network, and experience transformations before present at equipment. These will be discussed in chapter 3.3.

3.2 Descriptors of Voltage Disturbances

Having said that magnitude and duration are not adequate to describe voltage dips, the IEEE 1159.2 task force drafting the new IEEE 1159.2 standard [8] has set out to list a set of descriptors to more accurately describe voltage dips. The goal is to be able to extract information from a waveform and use this information to accurately reconstruct this waveform. This can be done for any periodic waveform using Fourier analysis. It is difficult to develop a single transform to describe a voltage dip, which is not periodic in nature. Other approaches, including examining influences of such disturbances on equipment, are being considered.

Voltage disturbances are deviations from the nominal balanced ac sinusoid. The nominal power system voltage is composed of three phases, each of which has essentially the same amplitude, the same frequency, and a 120 degree phase displacement. Ideally, the voltage is a sinusoid with no distortion, i.e. there are no harmonics present. The three voltages can normally be expressed as line-to-neutral values as follows:

$$v_{an}(t) = V_m \sin(\omega t)\ \text{V}$$
$$v_{bn}(t) = V_m \sin(\omega t - 120°)\ \text{V}$$
$$v_{cn}(t) = V_m \sin(\omega t + 120°)\ \text{V}$$

where V_m is the peak amplitude of the voltage waveform in volts and ω is the radian frequency in rad/s. The relationship between the rms value and the peak amplitude is $\sqrt{2}$: $V_m = \sqrt{2}\, V_{rms}$ and the relationship between the radian frequency in rad/s and the frequency in cycles/s (Hz) is: $\omega = 2\pi f$ where f is the frequency in Hz.

Variations from the voltage waveform can be categorised by the deviation from the ideal. Therefore, the descriptors will focus on the amplitude, waveshape, phase angle, and frequency, as well as how much the waveform deviates from the ideal waveform. Each disturbance has a starting and an ending point. Usually these are quite distinct and will be called the initiation and recovery

points. Since the sinusoids are periodic, we can describe the initiation and recovery points in terms of where they fall (in angle) on the waveform.
The descriptors used to identify specific characteristics of each voltage waveform during a disturbance are the following:

- RMS magnitude
  Duration
- Point-in-wave of initiation
- Point-in-wave of recovery
- Phase shift
- Rate of change of phase shift
- Harmonic rms distortion (defined in section 3.2.4)
- Missing voltage

The relationship among the three phases is vitally important to many types of industrial equipment. Many devices operate on the difference between two of the phase voltages, therefore phase shift among the phases may be of significance. The descriptors for the three phase situation will be analysed by the following:

- RMS Magnitude Unbalance ratio
- Difference Voltage
- Phase Angle Relationship

With this information, insight into specific voltage disturbance waveforms can be gained. By compiling this information from many waveforms into a common data set, statistical information about the voltage waveforms can be generated. Furthermore, engineers will be able to determine why equipment at a specific location is mal-operating and how equipment can be better designed, installed, and tuned to deal with the normal power system disturbances. The new parameters will help engineers more fully understand the nature of the voltage disturbance. Ideally, a set of characteristics would enable one to recreate the continuous-time voltage waveform in much the same way that a Fourier analysis can be used.

3.2.1 RMS voltage magnitude and duration

The rms voltage magnitude is fundamentally understood by all electrical engineers. This value is the effective value of the ac waveform; the rms value is the value that a dc source would have which dissipates the same electrical power as the ac waveform in a resistive load. The rms value assumes periodicity. Since the nominal ac waveform is periodic in one 360° cycle, a one-cycle based rms calculations is used.

Conventionally, the voltage dip and its duration are based upon the rms value. A voltage dip is reported as the lowest rms value attained during the event and the duration is the time interval from when it dropped below 0.9 pu and when it recovered to above 0.9 pu.

Figure 3.5 shows the plot of a "clean" sinusoidal dip from IEEE 1159.2-1996 and the accompanying rms value using a one-cycle "window." The window is the period over which the rms value is calculated, usually one cycle.

Notice that although the actual waveform dropped rather abruptly, the rms value smoothly transitions to its final depth. The rms value essentially averages the magnitude over the period (window width), and sharp transitions are averaged away. Since the duration information is taken from the rms value, up to a one-cycle error can occur in the duration due to the "averaging" effect of the window. Therefore, the interval during which the waveform's rms value is less than 90% is longer than the real duration of the dip seen by inspection. The dip is slow to begin and slow to recover due to this window.

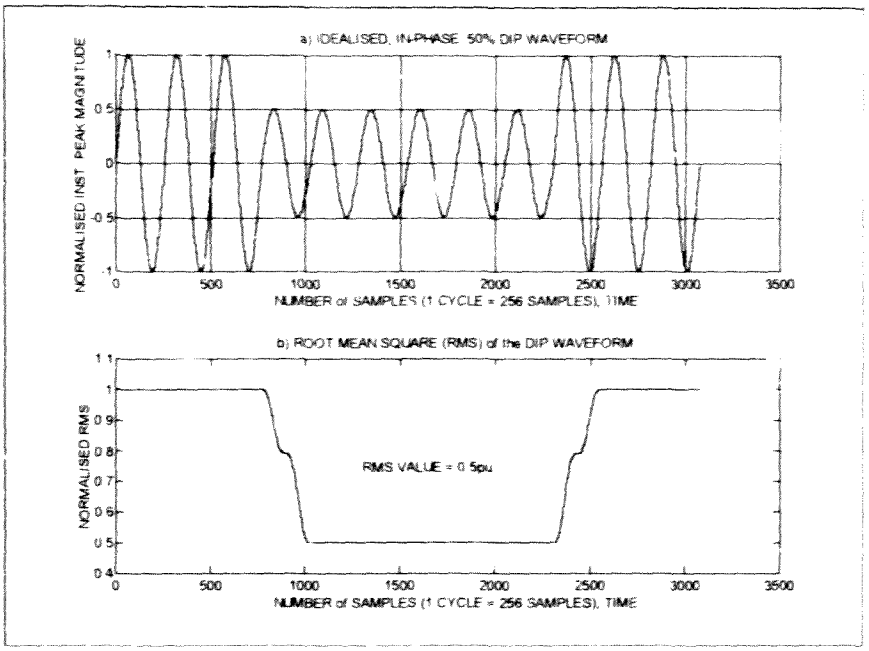


Figure 3.5 A clean sinusoidal dip and its rms value, presented using a one-cycle moving window. The depth is 0.5 pu and the duration is 5 cycles [8].

Using rms values, we can get the following information from a waveform:

- Start time: The time between the last positive-going zero crossing of the waveform before the dip start and when the rms value falls below 0.95pu.
- End time: same as above except when the voltage recovers to within 0.96pu (for a continuous 1/2 cycle). The end time is computed at the beginning of the interval in which the voltage recovers to within 0.96pu.
- RMS dip duration: The difference between the start and end times.
- Maximum rms Value: highest rms value of the waveform in a sample set.
- Minimum rms value: lowest rms value of the waveform in the sample set.
- Average rms value: average of the rms value between the dip start and end times.

3.2.2 Point-in-wave dip initiation

The point-in-wave of initiation and recovery is an instantaneous phenomenon that the rms analysis does not yield. Analysis of a many plant trips has shown that devices sometimes mal-operate on shallow dips, but not on deeper dips.

Electrical contactors are examples of devices that are extremely sensitive to point-in-wave of initiation and recovery of voltage dips. Contactors are essentially relays and are widely used in industry to control electrical devices. The force created by the simple electromagnet will vary significantly for the same level of rms voltage dip depending on the point-in-wave that the dip is initiated. In fact, dips that are caused by a slow reduction in voltage can be deeper than dips that occur at a critical phase angle on the waveform before the contactor disengages or mal-operates. The dropout point may vary from 85% to 55%, depending on how many degrees after a zero crossing, the event initiates. The boundary of operation and mal-operation (magnetic dropout/contactor chatters vs. electrical dropout/open circuit) for a typical industrial contactor is shown in Figure 3.6. The plot shows the rms voltage depth versus the point-in-wave of initiation of the voltage dip. There is a 30V difference in rms value of the dip that will make the contactor mal-operate, depending on the point-in-wave.

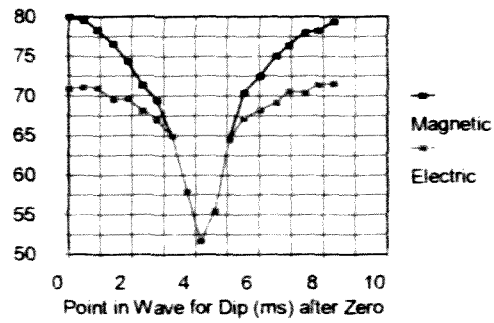


Figure 3.6 Boundary of operation for a typical industrial contactor: rms voltage magnitude of the dip versus point-in-wave of initiation of the d. Voltages during the dip below the boundary will cause the contactor to mal-operate magnetically and electrically [8].

Point-in-wave of recovery is also important. Contactors have been observed to misoperate upon recovery of the voltage. Although it is not clear why this should occur (phase shift occurring during the dip might play a role), it is clear that point-in-wave of recovery should also be a parameter to extract from the waveform. Other actively controlled devices that rely on timing information from the waveforms are also affected by the point-in-wave of initiation and recovery. These devices include dc motor drives, which employ thyristors connected to the ac line.

The difference between the point-in-wave of recovery and initiation is the actual duration of the event. If the point-in-wave of the initiation and recovery can be precisely determined, then the duration of the event can be determined precisely as well. When compared to the duration given by rms analysis, the duration is usually slightly less, but more accurate and meaningful.

A trained human observer could look at a disturbance and tell when it begins and ends. The rms moving window cannot give accurate point-in-wave of dip initiation information. There is another method, called the waveform envelope based method, which could provide a more accurate means of determining the waveform duration. The values recorded using this method are called apparent values. This technique uses two envelopes, which surround the pre-event (ideal) voltage waveform by ± 5% and ± 10%. The algorithm proceeds as follows:

- When the disturbance waveform deviates from the ideal by 10% (i.e., falls outside of the 10% envelope), the event is "detected."
- The algorithm "backs-up" to see where the waveform fell outside of the 5% envelope for the last time, and that is used as the beginning (start) of the event. This helps pick-up on the initiation of the event more accurately without reporting minor variations in voltages that were not of significance.
- When the disturbed waveform returns inside the 10% band for at least 1/2 cycle, the dip is deemed recovered.
- The initial point at which the 1/2 cycle of recovery occurs is the point of recovery. (The 10% band was chosen since most dips do not recover to within 5% in the data set intervals.)

Using the waveform envelope method, the following information can be extracted from the dip waveform:

- Apparent dip start: The point at which the voltage falls outside of the 5% envelope as described previously.
- Apparent dip end: The point at which the voltage returns to the 10% envelope as described previously.
- Point-of-initiation: The angle at which the "apparent dip start" occurs using the last positive-going zero crossing as the reference angle.
- Point-of-recovery: The angle at which the "apparent dip end" occurs using the last positive-going zero crossing as the reference angle.
- Apparent dip duration: The difference of apparent dip end and apparent dip start.
- Difference in duration: The difference in the dip duration given by the apparent method and the rms method (in seconds).

3.2.3 Phase shift and rate of change of phase shift

Normally the phase angles between the three-phase voltage waveforms are fixed. To single-phase electrical equipment, the phase angle shift (or phase "jump") of the voltage seen by this equipment is important. The jump will normally occur twice during the event: once at the initiation and once at the recovery. To three-phase equipment, the phase angle relationship among the phases themselves is at least as important as the phase angle jump. Since most three-phase equipment uses a rectifier of some sort delta-connected to the ac line, the rectifier operates based on the instantaneous line voltages.

If the phase angle of one of the phase-neutral voltages shifts relative to another phase-neutral voltage, the phase angle relationship between the line voltages will be disturbed. Thus the phase angle relationship will be affected even if the phase angle of the dipped phase does not change. If the phase angle of the dipped phase-neutral voltage does shift, the phase relationship among the line voltages will possibly be more affected.

Figure 3.7 shows the phasor diagram of a dip on the phase-neutral voltage V_{bn}. The rectifiers used in ac motor drives and other power supplies respond to the line voltages: V_{ab}, V_{bc}, and V_{ca}. They are connected phase-to-phase and do not have a neutral connection. The dip on phase B has resulted in a phase shift in the line voltages V_{ab} and V_{bc}, while V_{ca} is unaffected. The amplitudes of both V_{ab} and V_{bc} are reduced, although not as much as the amplitude of V_{bn}. A rectifier would experience increased output voltage ripple but the peak output voltage would remain the same, since the amplitude of line voltage V_{ac} is not affected by the dip on phase B.

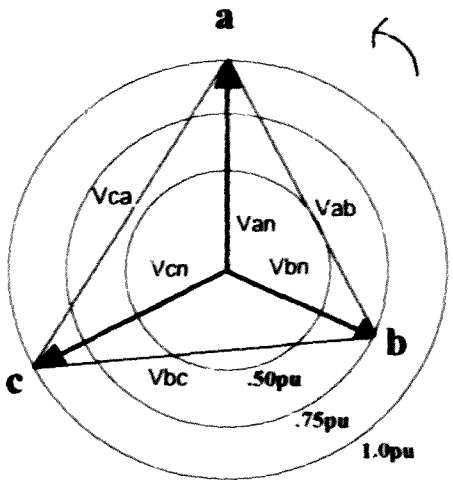


Figure 3.7 A single-phase 25% dip on phase B without phase shift resulting in a phase shift and dip for line voltages V_{ab} and V_{bc} but no change for line voltage V_{ca} [8]

If the dip on phase B also resulted in a phase shift on the phase-neutral voltage V_{bn}, then the line voltages would behave differently. For example, a phase-shifted dip on phase B is shown in Figure 3.8. Now the V_{ab} voltage experiences an increase in rms voltage, while the voltage V_{bc} experiences a dip. The V_{ca} voltage is unaffected. The voltage increase on V_{ab} will result in an overvoltage on the output of the rectifier and the ripple will increase significantly.

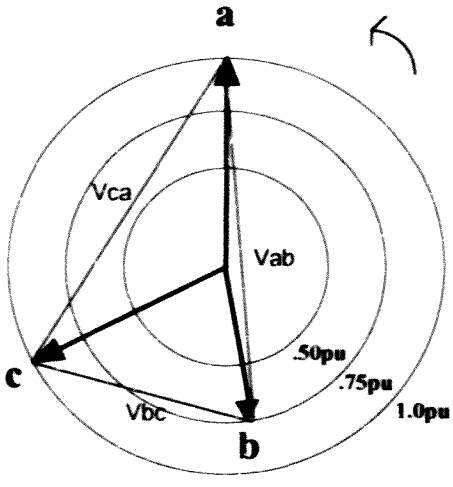


Figure 3.8 A 75%, 50° phase-shift during a voltage dip on phase B results in a voltage increase and phase shift on voltage V_{ab} and a dip and phase shift on voltage V_{bc} [8]

Due to the one-cycle window in which the rms value is calculated, the rms value of the phase-neutral voltages is not affected by the phase shift. This is obvious from the phasor diagram in Figure 3.7 since the V_{bn}'s phasor vector is the same as in Figure 3.8. The only affect the phase shift has is a small oscillation in the rms voltage during the initiation ramp down and recovery ramp up. Conventional rms analysis would not help to identify equipment mal-operation in a plant due to phase angle shifts.

It is difficult to determine how much phase angle jump can be expected. Regenerative and other active devices connected to the lines, coupling from other phases due to transformers and rotating machinery, add to this difficulty. By characterising the waveforms with phase shift information, it will be possible to obtain statistics about the amount of phase angle shift typically seen on the system, as well as to enable future studies at specific locations for determining specific needs.

Inspection of many voltage dip waveforms shows that many times the phase angles do not instantly jump from one value to another at the initiation of the dip,

nor are phase angles stationary during the events. Many types of equipment monitor one or more of the voltage waveforms for timing or protective information. Normally a phase-locked loop (PLL) or other similar device is incorporated to track the phase angle.

The PLL is sensitive to phase angle. There is a bandwidth in which it is able to track and a rate at which it can respond to a change in input. Changing phase angles can be difficult to track, even if the waveform is perfectly sinusoidal. The rate of change of phase angle, called "slew rate", is perhaps the most important parameter for determining the capability to track changes.

PLL circuits have two primary functions that compete during phase-shifted voltage disturbances. The PLL wants to remain exactly synchronised with the power system and has a high time-constant ("inertia") so that fluctuations in the system do not cause its output to respond. But since the devices it controls, such as thyristors in a dc motor drive, experience the voltage waveforms on an instantaneous basis, the PLL should move quickly to remain synchronised to the voltages during the dip. This keeps the thyristors firing properly. With too little inertia the PLL is unstable, while with too much inertia the drive will misbehave due to the inability to track accurately during a disturbance. Designers of these drives do not know what the real system behaviour during a disturbance is, so an educated guess is made when designing the circuits. The results from characterising disturbances for rate of change information will provide valuable results to improve the design of these circuits.

Using the waveform envelope method (see section 3.2.2) for phase angle information, the following information can be extracted from the dip waveform:

- Phase shift: phase angle between the ideal waveform and the disturbed waveform. This can be calculated using the zero crossing technique or the discrete Fourier Transform (DFT).
- Phase shift at dip start ($\Delta\phi$): This is computed in two different ways. One is using zero crossings and the other is using the DFT. When using zero crossings, the phase shift is computed at the first zero crossing after the "disturbed dip start." When using the DFT method, the value is computed ½ cycle after the dip start.

- Maximum phase shift: The maximum phase angle shift recorded between the "apparent dip start" and the "actual dip end" times.
- Minimum phase shift: The minimum phase angle shift recorded between the "apparent dip start" and the "actual dip end" times.
- Average phase shift: The average phase angle shift recorded between the "apparent dip start" and the "actual dip end" times.
- Maximum $\pm d\phi/dt$ (rate of change or "slew rate" of phase angle): This is the rate of change of the phase angle during the interval. The initial change at the "dip start" and the final change at recovery are not included in the calculation since sharp discontinuity, which accompanies the beginning and end of the event, will cause a very high and meaningless value.

3.2.4 Distortion of dipped waveforms

Many voltage waveforms during dips are distorted. Since rectification relies on the difference between two voltages being higher than the load voltage, the semiconductors generally conduct only near the peak voltages. This causes currents to flow only near the voltage peaks, and hence currents that are non-sinusoidal. Smoother current flow and lower output voltage ripple would occur if the input voltages were square waves.

Quantifying the distortion of a waveform is normally done using a computation of the total harmonic distortion (THD). THD is not adequate for quantifying distortion during a dip because the harmonic components are scaled using the fundamental component. During a voltage dip, the nominal voltage is dipped and the apparent distortion will be amplified by the smaller than normal fundamental component. It is more appropriate to scale the harmonic components by the nominal. If we use the per-unit system and make the nominal voltage equal to 1.0pu, then the root of the sum of all squares of the harmonic pu amplitude will be equal to the THD scaled by the nominal voltage. This value is called the "harmonic rms" value (hrms) and is used to compute the relative distortion of the voltage waveforms during a dip. The formula for hrms is given below:

$$hrms = \sqrt{V_{rms(total)}^2 - V_{dc}^2 - V_{fund}^2} \qquad \text{(Eq.1)}$$

3.2.5 Missing voltage concepts

Many power electronic-based devices are sensitive to the energy transfer during a voltage disturbance. For example, ac power supplies and motor drives that use capacitors for energy storage and voltage ripple reduction are especially sensitive. During a voltage dip, the reduction in voltage causes the capacitor to discharge and transfer its stored energy to the load, ultimately resulting in an undervoltage trip.

Devices are available to actively compensate for voltage disturbances on an instantaneous basis utilising shunt and series converter topologies. These devices inject or subtract voltage as required to compensate for the disturbance. For example, during a voltage dip, the series compensation device injects voltage in an additive fashion to the ac voltage in an attempt to produce a perfect nominal sine wave at the output of the device. The magnitude of the required injection is the instantaneous difference between the desired sine wave and the actual input wave. This difference is called the "missing voltage" [8, 24].

The missing voltage is not the difference in rms values; instead, it is the instantaneous difference. Analyses made using rms data give misleading results. An example is shown in Figure 3.9. This figure shows the ideal nominal voltage waveform, the actual dipped voltage, and the missing voltage. The missing voltage is the voltage required to boost the dipped voltage back to the ideal. Notice that this value varies with time.

The next graph in Figure 3.10 shows the same rms dip, but with a phase shift. Notice now that the missing voltage is higher since the required injection voltage is higher. Compare this to the phasor representation of phase B in Figure 3.8 to see why the required injection is higher than 50%. Although Figure 3.8 is for a 25% dip, it is clear that the phasor addition, required to compensate for the magnitude and the angle is more than 50%. Conventional rms analysis would suggest that 50% injection capability is adequate.

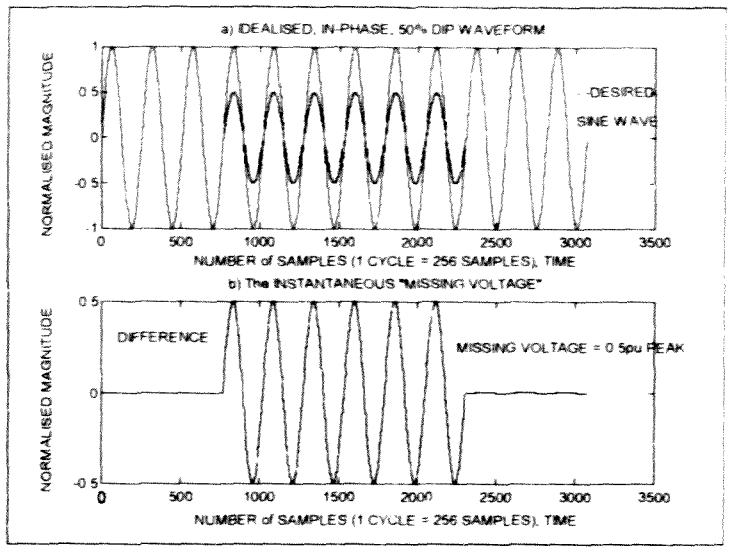


Figure 3.9 A 50% voltage dip without phase shift and the missing voltage [8]

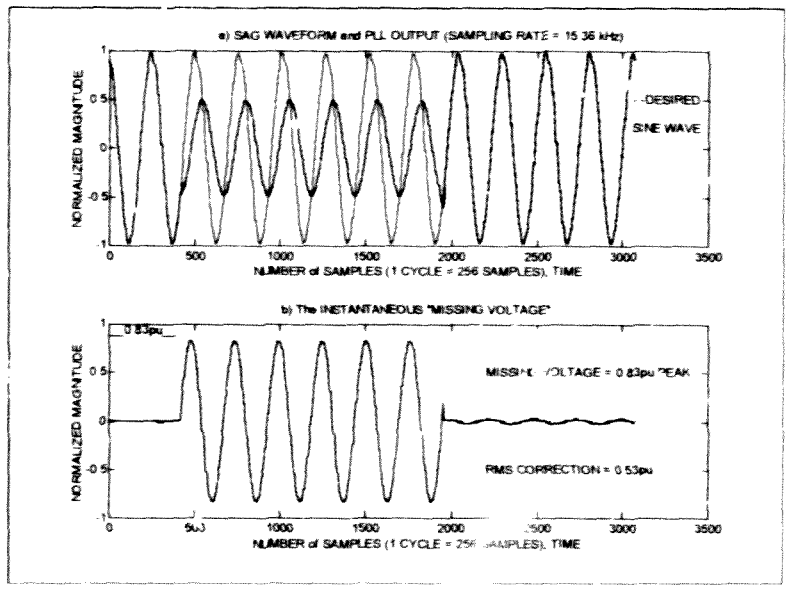


Figure 3.10 50% voltage dip with a 60° phase-shift and the missing voltage analysis showing a required peak injection voltage of 83% [8]

Energy transfer is also important. The ability of the series compensation device to correct a voltage disturbance is also related to the energy that is required during the event. The required energy is related to the power consumed by the load and the duration of the dip. Missing voltage analysis can give information required to determine the duration of the voltage injection, and hence the energy required. By properly matching the peak voltage injection amplitude, the duration of these amplitudes, and the load's energy requirements, series-injection devices can be properly sized.

The missing voltage and its analyses are determined as follows:

- The actual waveform is subtracted from the nominal waveform.
- The result is rectified to give all positive numbers.
- The voltage is subdivided into 5% bands.
- The missing voltage is the peak value that falls into one of the bands at a specific instant of time.
- The missing voltage is reported in two ways:
  - The amount of time (total number of sample points) that the missing voltage falls into a particular band (e.g., 30% to 35%) is tabulated onto a bar graph.
  - The cumulative time that the missing voltage is greater than or equal to a particular value (i.e., $\geq$ 30%) is shown on the same bar graph. This report will be particularly useful in determining how a series voltage compensation device will perform.

3.2.6 Three-phase voltage symmetry

Many industrial devices have three-phase inputs and are very sensitive to voltage balance and symmetry. A relatively small amount of voltage unbalance can result in a large current unbalance as shown in Figure 3.11 for a three-phase ac motor drive. A severe current unbalance during a voltage dip can result in semiconductor damage and fuse blowing due to overcurrents.

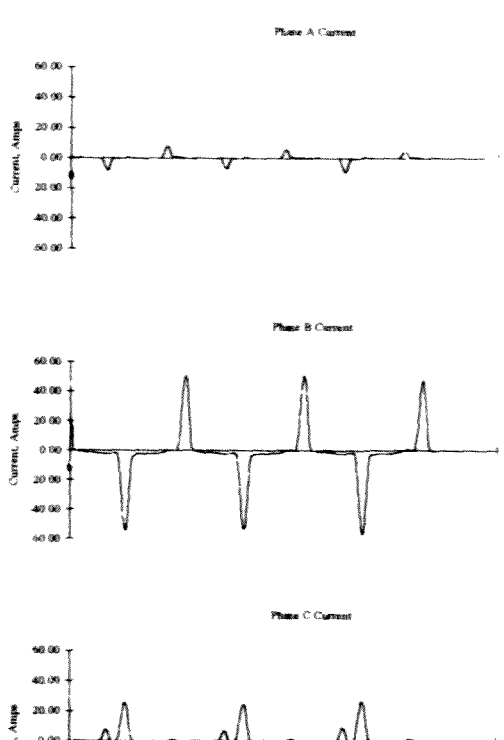


Figure 3.11 Line currents of a 5hp three-phase ac motor drive with a 3% voltage magnitude unbalance [8]

An unbalance ratio can be used to determine the relative balance of voltage magnitude among the phases. Nominally, the unbalance ratio should be zero, but any magnitude unbalance will result in a positive number. The unbalance ratio is defined as the difference in the rms values between the highest and lowest phases, divided by the average of the rms values of the three phases.

$$\text{Unbalance Ratio} = \frac{V_{high} - V_{low}}{(V_A + V_B + V_C)/3} \qquad \ldots \qquad \text{(Eq.2)}$$

This ratio is plotted on a continuous time basis using a moving window. The maximum unbalance during the interval is reported.

3.3 The Propagation of Voltage Dips through the Power Network

Voltage dips could have their origins outside of a customer's premises: on the distribution network or on the transmission network. However, the origin of the dip could also be inside the customer's premises. The purpose of this section is not to investigate the external factors that initiated a dip, but to link voltage dips directly to the faults that caused them and to evaluate their propagation through the network until they ultimately affect the equipment.

3.3.1 The propagation of voltage dips in general

Utility network faults may be of a single-phase, phase-to-phase, phase-to-phase-to-ground, or three-phase nature. The location of the fault in the network will determine the magnitude of the voltage dip seen at the customer busbar. Figure 3.12 shows common fault locations on the utility network which give rise to voltage dips. For a given fault location, factors which influence the depth of the voltage dip at the point of supply are the type of fault, the fault impedance, the effect of local generation, load dynamics, the operating state of the supply network (generation levels and network configuration) and the type of earthing employed [4].

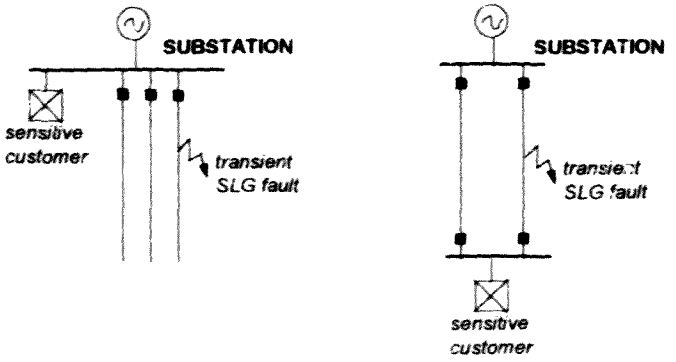


Figure 3.12 Typical fault locations, which give rise to voltage dips at the customer point of coupling [4]

The National QOS measurement campaign has now been running since 1994. Dip data was retrieved for the last 4 years. This shows single-line-to-ground (SLG) faults are most common and this corresponds to single-phase dips as shown in Figure 3.13 and in Table 3.1.

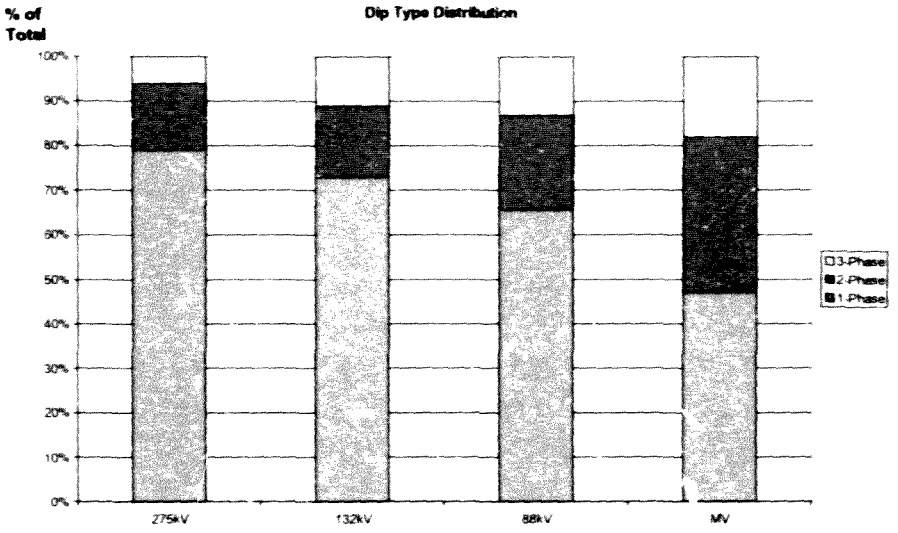


Figure 3.13 Dip types in South Africa [4]

Table 3.1 Dip characteristics in South Africa, arranged in terms of voltage level *and phase involvement* [4]

Dip Type	% of Total No of Dips	Typical Duration (ms)	Typical Depth (%)
All 275kV Dips		**50 – 100**	**15 – 40**
Three Phase	6	30 – 200 & 400	15 – 40 & 75 – 80
Phase to Phase	15	100	15 to 45
Single Phase	79	100	15 to 30
All 132kV Dips		**100**	**15 to 40**
Three Phase	11	100 to 200 & 700 & 1.5sec	15 to 50 & 100
Phase to Phase	16	100 to 150	15 to 60
Single Phase	73	100	15 to 40
All 88kV Dips		**100**	**15 to 30**
Three Phase	13	100 & 600 & 1.5sec	15 to 20 & 100
Phase to Phase	21	100	15 to 30
Single Phase	65	100	15 to 30
All MV Dips		**100 to 1.5sec**	**15 to 30 & 100**
Three Phase	18	100 to 300 & 1.5sec	15 to 20 & 100
Phase to Phase	35	100	15 to 30
Single Phase	47	100 to 1.5sec	15 to 30

The following table shows the line voltage magnitudes on the secondary side of a transformer in the case of a 70% SLG fault on the primary side (phase A) [9]. The primary network is assumed to be solidly earthed. This is usually the case when the primary winding is rated at 88kV and above.

Table 3.2 Line voltage magnitudes for a SLG fault on phase A [1,4]

Transformer connection	Line voltages on the transformer secondary		
	Vab	Vbc	Vca
Y/Y	0.58	1.0	0.58
D/D	0.58	1.0	0.58
Y/D	0.33	0.88	0.88
D/Y	0.88	0.88	0.33

From the table it is clear that for a solid SLG fault the resulting line voltage will be the smallest for Y/D or D/Y connections.

The duration of a voltage dip is determined by the speed of operation of network protection devices and the type of protection employed. Also important is whether the primary protection operates or the back-up protection. This has a significant impact on the duration of dips. Reclosing can cause multiple voltage dips with varying durations. Factors such as load dynamics and fault impedance further influence the duration of the dip e.g. re-accelerating plant actually pulling the voltage down after a dip and extending its duration. An example of equipment affecting the recovering dip is an induction motor.

Table 3.2 can also be extended to the voltage dip types shown in Figure 3.4, which include types of three-phase dips.

Table 3.3 The transformation of three-phase dips [22,23]

Transformer connection	Line voltages on the transformer secondary			
	A	B	C	D
Yn/Yn	A	B	C	D
Yy/Dd/Dz	A	D	C	D
Yd/Dy/Yz	A	C	D	C

3.3.2 Unbalances and propagation of voltage dips: phase angle jump

The occurrence of phase angle jump deserves special attention, as this will affect the performance of certain equipment types. IEC 61000-4-11 describes a testing protocol for single-phase equipment. The equipment shall be tested for one or more combinations of magnitude and duration chosen from the following list: 0, 40 and 70% magnitude; 0.5, 1, 5, 10, 25 and 50 cycle duration [32]. The standard could be applied to three-phase equipment by assuming all three-phase voltages to be equal. This is a gross oversimplification however, as three-phase faults are rare. The majority of faults in power systems are single-phase or phase-to-phase faults. Therefore the majority of voltage dips are associated with different voltages in different phases.

Next to the drop in rms voltage, the majority of voltage dips are associated with a change in the voltage phase angle. This so-called phase-angle jump manifests itself as a change in the instant of voltage zero crossing before and after the start of the dip. The origin of the phase-angle jump is understood from the voltage divider model for a voltage dip, shown in Figure 3.14.

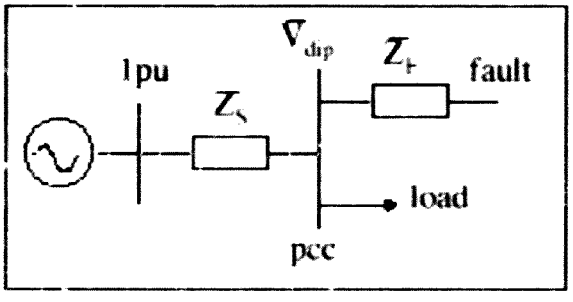


Figure 3.14 Voltage divider model for dip magnitude and phase-angle jump [22,23]

When the X/R ratios of the source and the feeder impedances are different, the voltage at the PCC not only drops in magnitude but also experiences a phase-angle jump. The maximum phase-angle jump is equal to the impedance angle. The impedance angle ranges from close to zero for transmission system faults, to -60° for faults on distribution cables [22,23]. The relation between magnitude and phase-angle jump for an impedance angle of -60° is shown in Figure 3.15.

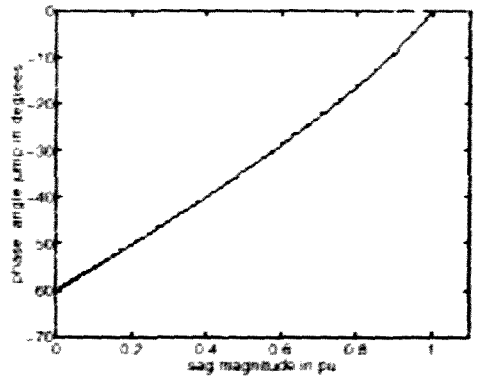


Figure 3.15 Relation between magnitude and phase-angle jump for voltage dips due to three-phase faults [22,23]

The above calculation uses a single-phase model and is thus strictly speaking only valid for three-phase faults. To obtain the range of magnitudes and phase-angle jumps at the terminals of single-phase equipment, requires a comprehensive analysis, which is described in [32]. The results of the analysis are shown in Figure 3.16, where an impedance angle of -60° has been assumed. Magnitude and phase-angle jump have been calculated for single-phase, phase-to-phase and three-phase faults. The figure should be a basis for testing single-phase power-electronics equipment.

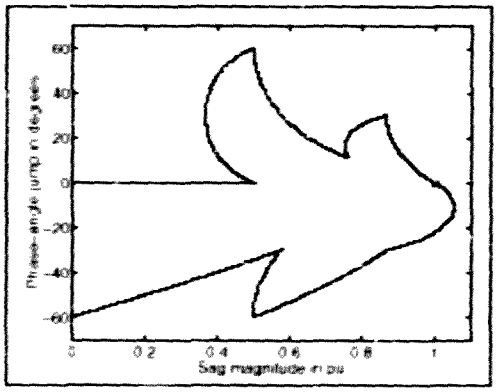


Figure 3.16 Range of magnitude and phase-angle jump for single-phase equipment [32]

The occurrence of phase angle jump significantly influences the view on voltage dip testing. It is already accepted that the first stage of voltage dip testing consists of testing against dips of different duration and magnitude. This is similar to the testing protocol described in IEC 61000-4-11. For equipment sensitive to phase-angle jumps, and for systems where large characteristic phase-angle jumps are to be expected, the effect of the characteristic phase-angle jump should be studied. It is recommended to perform tests for a number of impedance angles (see above): 0°, -30° and -60° [32].

Figure 3.17 shows the phase angle jump for a phase-phase type C voltage dip.

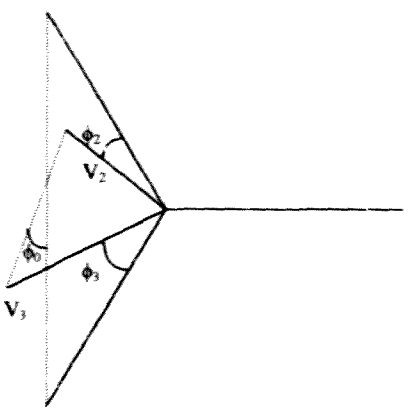


Figure 3.17 A vector diagrams illustrating a typical phase angle jump for a type C voltage dip

3.4 Voltage Dip Characterisation on the South African Network

The South African national QoS database measurement program has been running since 1994 and has collected four years of data so far. Dips have been classified in terms of a Y,X,S,T,Z dip window, shown in Figure 3.18, as used by the National Power Quality Regulatory Standard NRS-048 part II [20]. Although this type of categorisation is in terms of magnitude and duration, phase angle information is also recorded in the measurement program.

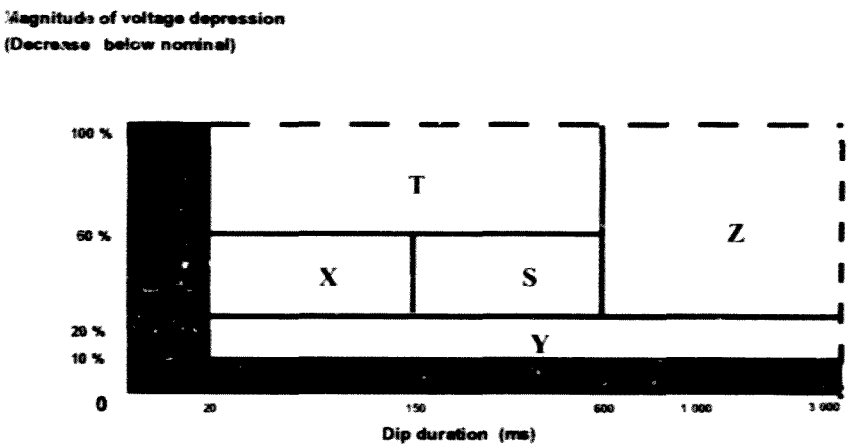


Figure 3.18 NRS-048 Dip classification window [20].

The following criteria were used in setting up the dip window:

- Dips are not classified as single phase, two phase or three phase dips. The minimum voltage magnitude of any of the three phases and longest dip duration on any of the three phases (the worst case) is used to characterise the voltage dip.
- Dip magnitudes below 0.2pu are not regulated by the National Electricity Regulator.
- The 0.6pu dip magnitude has been identified as the level above which all unprotected contactors drop out

- Dip magnitudes less than 0.1pu fall outside the definition of dips prescribed in the standard.
- Duration limits have been established at 150ms because this represents zone 1 protection and at 600ms because this represents zone 2 protection in terms of the network distance protection schemes.
- The maximum dip limit of 3 seconds is based on the operating time for auto-reclosure of the system protection.
- A duration of less than 20ms represents less than one cycle on a 50Hz system.

Faults causing dips can either be single-phase-to-ground, phase-to-phase or three-phase events. Ideally each phase should be treated separately. This however makes quick interpretation difficult. Each area on the scatter plot is indicative of the effect dips have on customer plant. The following could be indicative of the types of dip events for each area:

X Voltage dips produced by electrically remote faults which generally do not impact on customer plant operations

S Voltage dips produced by electrically remote faults with a delay in network recovery

T Voltage dips produced by electrically close faults

Z Major system disturbance with delayed network recovery

A measurement conducted at the HV level for a transmission fault will typically fall in region X on the scatter plot i.e. remote faults cleared in primary protection clearance times. For a fault closer to the point of measurement the plotted events will typically move upwards on the scatter plot and into region T. As the point of measurement moves to the LV circuits the same plotted events tend to move downwards on the scatter plot (T to X etc.) as rotating plant and star delta transformation reduce the perceived magnitude. Due to the inrush however, the dips are extended in duration and a movement of plotted LV events to region S on the window will typically be seen for HV faults. It is therefore important to

investigate both HV and LV to understand the sources and impact of dips on an installation.

The NRS-048 part 2 serves as a guideline, regulating the electricity supplier for all but Y-type dips. The limits for assessment are shown in Table 3.4, but these are continually developing in negotiations between the utility, regulator and customers and as more information becomes available from the QoS database.

Table 3.4 Limits to a number of voltage dips per year for each category of dip window [20]

1	2	3	4	5	6
Network voltage range (see Note)	Number of voltage dips per year				
	Dip window category				
	S	T	X	Y	Z
6,6 kV to ≤ 44 kV	30	30	100	150	20
6,6 kV to ≤ 44 kV Rural	69	54	215	314	49
> 44 kV to ≤ 132 kV	25	25	80	120	16
220 kV to ≤ 765 kV	11	6	45	88	5
NOTE — The network voltage is not necessarily the voltage at which the customer takes supply. It is the voltage of the network that feeds the point of common coupling.					

Recently, studies have been done to characterise the voltage dip performance of the South African network in terms of the categories set out in the NRS-048 part II, as well as in terms of geographical location [5]. An example of the results of this study are shown in Table 3.5 and illustrated in Figure 3.19.

Table 3.5 An example of dip-type distribution on the South African network [5]

Region	S	T	X	Z
Gauteng	12-16	3-6	30-40	4
Kwa-Zulu/Natal	4-16	6-13	80-85	1-5
W. Cape	0-2	1-3	17-19	1-3
E. Cape	5	8	70	2
Free State & N. Cape	5-12	6-18	30-50	2-10
Mpumalanga	10-18	6-10	40-55	5-7
N & NW	11-17	5-8	50-80	3-6

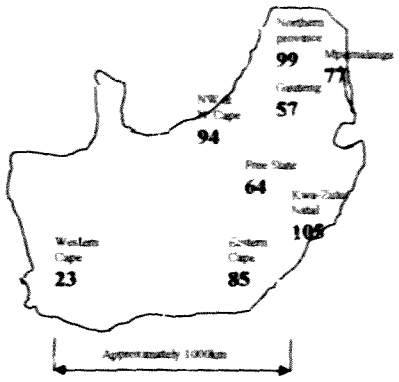


Figure 3.19 Average S,T,X & Z dips per annum in South Africa

It was established that the number of dips measured at sites within regions vary drastically, hence it is difficult to specify the number of dips expected per dip class per region. With the available data, absolute differentiation of the number of dips experienced per region is not possible. However, it is possible to compare region to region, e.g. the Western Cape has approximately half the X class dips of Gauteng [5].

3.4.1 Frequency of occurrence of dips

From a lightning exposure perspective the greater the length of overhead lines in a system the greater the exposure to dips. This means that system reinforcement which is usually beneficial from harmonic, fault level and security of supply considerations (availability) worsens the number of dips experienced. System reinforcement also increases the risk of primary equipment failure due to the increased plant item count.

3.4.2 Phase shift during dips

Line to line faults, relatively common on Eskom's 275kV networks due to the line configuration and induced flashovers, cause a significant instantaneous phase shift in the normally balanced 120° spaced voltage phasors. Phase shifts of up to 30° have been measured.

3.5 New Voltage Dip Types under Consideration

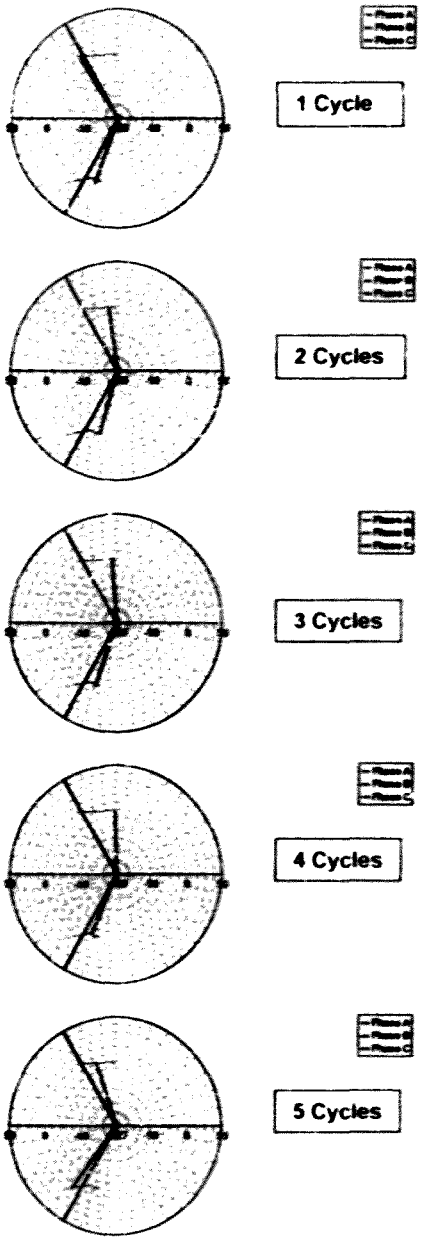


Figure 3.20 A voltage dip showing phase angle variation during the course of the dip (from the National QOS database)

An evaluation of phase angle information on the South African national QoS database reveals many of the phase angle jump phenomena described in section 3.3.2. This is illustrated by Figure 3.20, which is a phasor diagram of a voltage dip exhibiting this behaviour.

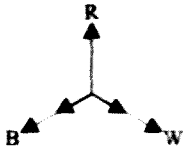
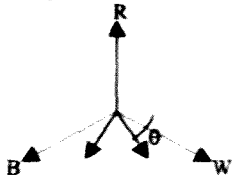
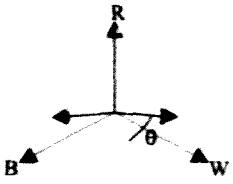
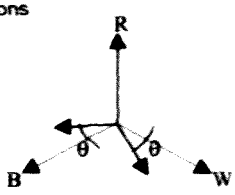
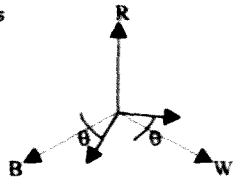
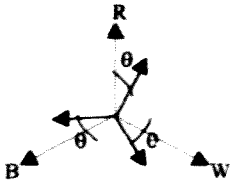
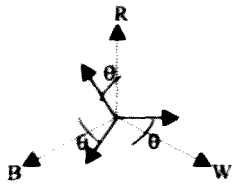
It was shown in section 3.3.1 that voltage dips are propagated from their source to other parts of a network through transformers. Most of the voltage dips recorded by the database will be single-phase dips because they are measured on the transmission network and distribution network down to 88kV. The impact of voltage dips on equipment happens at a low voltage level, typically less than 1kV. The transformation process cannot be ignored, especially with unbalanced voltage dips.

Voltage dips at a low voltage level were monitored at specific installation site in Kwazulu-Natal. These dips were evaluated in terms of their phase angle magnitude. 100 of these dips were recorded. The data for this evaluation is in Appendix B. The voltage waveform was recorded before, during and after the dip occurred. The maximum shift in phase angle on each phase was recorded. It was also noted how the dipped voltage shifted in phase from the position of the pre-dip voltage. The result of the analysis is shown in Table 3.6.

The dip type classifications were named class one to class seven. Discussions about the results of the evaluation are ongoing, but it was agreed that the phase angle variation as described by a class two dip, is common. This is supported by the discussions of phase angle jump in section 3.3.2. Phasor diagrams of a class two dip is shown together with the faults that may cause such a dip, in table 3.7

Phase-phase faults (PP) commonly have phase shifts associated with it. If the fault was bolted at the point of origin, impedance further up the network will influence the fault to an extent where the affected phases pull together and decrease in magnitude. Inductance in-line contributes to phase shift.

Table 3.6 Results of an analysis of voltage dips monitored at a selected LV site

<table>
<tr>
<td>Class1
• No phase variation
• Phase-to-phase dip
• Depth variation only
• Red, white or blue phase could be referenced
• Blue-white (BW), red-blue (RB) or red-white (RW) phases could be dipped
 
</td>
<td>Class 2
• Phase-to-phase dip
• Red, white or blue phase could be referenced
• Phase variation (θ) & depth variation on blue-white (BW), red-blue (RB), red-white (RW) phases could be dipped
• Phase shift symmetric w r t. referenced phase
 
</td>
</tr>
<tr>
<td>Class 3
• Phase-to-phase dip
• Red, white or blue phase could be referenced
• Phase variation (θ) & depth variation on blue-white (BW), red-blue (RB), red-white (RW) phases could be dipped
• Phase shift symmetric w r t. referenced phase
 
</td>
<td>Class 4
• Phase-to-phase dip
• Red, white or blue phase could be referenced
• Phase variation (θ) & depth variation on blue-white (BW), red-blue (RB), red-white (RW) phases could be dipped
• Phase shift of magnitude (θ) for both dipped phases
• Dipped phases shift clockwise from their original positions
 
</td>
</tr>
<tr>
<td>Class 5
• Phase-to-phase dip
• Red, white or blue phase could be referenced
• Phase variation (θ) & depth variation on blue-white (BW), red-blue (RB), red-white (RW) phases could be dipped
• Phase shift of magnitude (θ) for both dipped phases
• Dipped phases shift anti-clockwise from their original positions
 
</td>
<td>Class 6
• Three-phase dip
• Phase variation (θ) & depth variation
• Dipped phases displaced in magnitude and shift in angle (θ), clockwise from their original positions
 
</td>
</tr>
<tr>
<td colspan="2">Class 7
• Three-phase dip
• Phase variation (θ) & depth variation
• Dipped phases displaced in magnitud and shift in angle (θ), anti-clockwise from their original positions
 
</td>
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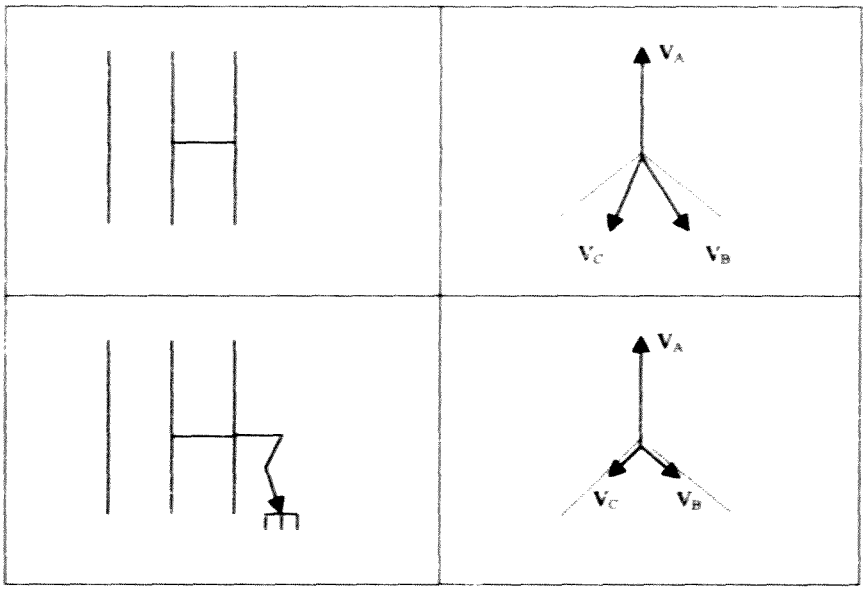
</table>

Table 3.7 Phase shift variations occurring during a phase-phase voltage dip that was caused by a phase-phase fault. A phase-phase-ground fault is shown for comparison.



In conclusion to the evaluation, it was decided that when phase angle variations were going to be tested for, this type of dip be used for angles up to 30°. Angles up to 30° on the South African network are common based on recordings taken during investigations.

Phase shift of the phase waveforms during a voltage dip is under investigation at Eskom. Voltage dip measurements from various sites in South Africa on the Eskom network are being used to compile data for evaluation of voltage dip types. The dip classes derived from the limited monitoring of LV dips will serve as a reference for the way in which these derivations can take place. Future work on the international front will be monitored.

4 THE IMPACT OF VOLTAGE DIPS ON PLANT EQUIPMENT

4.1 Equipment Sensitivity to Voltage Dips

Different types of equipment respond differently to voltage dips. Resistive loads such as incandescent lamps simply dim or brighten but continue to function. Some industrial processes can be particularly susceptible to dips because the equipment is interconnected and a trip of any component in the process can cause the whole plant to shut down. Examples of these industries include plastics, petrochemicals, textiles, paper, semiconductor, and rubber. Important loads that can be impacted include:

- Motors, heating elements, and other 3-phase loads connected directly to the LV bus.
- Variable speed drives and other power electronic devices that use 3-phase power, connected directly to the LV bus, or through an isolation transformer.
- Lighting often utilizes single-phase connections from phase-to-neutral.
- Control devices such as computers, contactors, and programmable logic controllers are often supplied through a single-phase control transformer.

The voltages experienced during a voltage dip will depend on the equipment connection. Chapter 3 showed that the individual phase voltages and phase-to-phase voltages are quite different during a SLGF condition on the transformer primary. Some single-phase loads will be unaffected and other single-phase loads may drop out, even though their sensitivities to voltage dips may be identical. Voltage unbalance is also a concern for motor heating. However, the durations of the unbalanced voltages during fault conditions are so short that motor heating is not a significant concern. Variable speed drives, however, may have controls that trip very quickly during unbalanced conditions.

Different categories of equipment and even different brands of equipment within a category (e.g. two different models of variable speed drives) have significantly different sensitivities to voltage dips [31]. This makes it difficult to develop a single standard that defines the sensitivity of industrial process equipment.

The closest document to a standard is the CBEMA curve of chapter 2 shown again in Figure 4.1, which was developed by the Computer Business Manufacturers Association [2, 31]. This applies primarily to data processing equipment. The curve shows that the load sensitivity is very dependent on the duration of the dip. Allowable dips range from 0% voltage for 1/2 cycle to 87% voltage for 30 cycles.

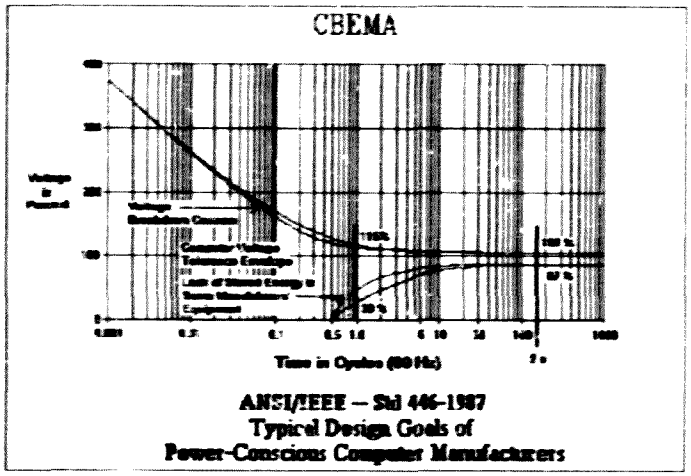


Figure 4.1 The CBEMA operating voltage envelope [31]

While the CBEMA limits suggest a "standard" sensitivity to voltage dips, actual plant equipment has a variety of operational characteristics during voltage dips.

4.1.1 Induction motors

Induction motor torque is proportional to the square of its voltage. The full load torque is usually designed to be about half of the maximum torque. This means that if the voltage drops to about 70%, the maximum torque will be equal to the full load torque. In other words, if the induction motor was driving a full load before a dip more than 70% occurs, the dip will cause it to stall, since the machine torque is now less than the load torque. During a voltage dip, the induction motor has to draw more current in order to supply the same load as before the dip. The high current will cause additional heating and may damage the motor. To prevent overheating, large motors are equipped with undervoltage and overcurrent protection. The typical setting is between 70-90% of rated voltage and for 1-3 seconds.

4.1.2 Motor contactors and electromechanical relays

Apart from motors, other electromechanical devices include relays, contactors and solenoids. Contactors tend to drop out if the voltage dips to below 50-60% for one or two cycles. One manufacturer has provided data that indicates their line of motor contactors will drop out at 50% voltage if the condition lasts for longer than one cycle. This data should be expected to vary among manufacturers, and some contactors can drop out at 70% normal voltage or higher [31]. Usually a contactor needs about 80% rated voltage to operate. A contactor may be fitted with auto-reclose feature when the voltage recovers. In the case of a large motor load equipped with automatic contactors, a new voltage dip may occur when they are started simultaneously or soon after each other. As a consequence, the motors may stall again. Therefore, delays between the starting of large motor must be introduced so that the simultaneous restart of large motor loads does not produce another significant dip.

4.1.3 High-intensity discharge (HID) lamps

Mercury lamps are extinguished at around 80% normal voltage and require time to re-strike [31]. A voltage dip that extinguishes HID lighting is often mistaken as a longer outage by plant personnel.

4.1.4 Line commutated rectifiers

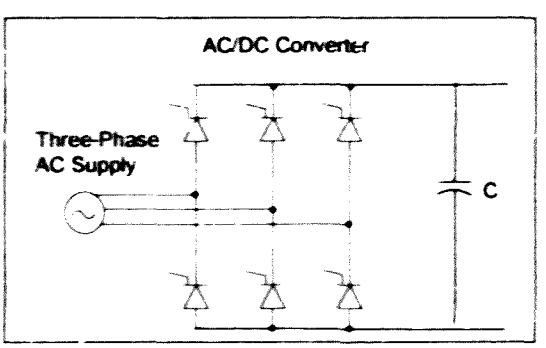


Figure 4.2 A simplified diagram of a line commutated rectifier topology

The DC voltage is controlled by varying the delay in firing angle of switching devices such as transistors (MOSFET or IGBT) or thyristors (refer to Figure 4.2). Each switch is turned on after a particular delay after it becomes forward biased as the voltage changes its phase. The common practice is to use a phase-locked loop to synchronise the firing pulses of the switching devices with the supply voltage. A voltage dip is caused by a sudden introduction of reactive impedance such as the occurrence of line faults. Therefore, voltage dips are usually accompanied by a sudden change in phase angle. The phase locked loop needs time to adjust to the sudden change of phase and misfiring results. Furthermore, voltage dips are usually caused by unbalanced faults, such as single line to earth faults, and therefore cause phase imbalance, i.e. the phase differences are no longer 120° apart. The error in firing is compounded by phase imbalance (see chapter 3). Incorrect firing of thyristors may lead to damage to the rectifier and therefore some converters are equipped with protection that trips in case the situation becomes dangerous.

4.1.5 Uncontrolled rectifier

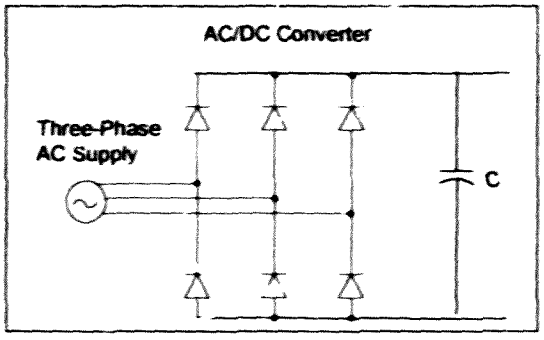


Figure 4.3 A simplified diagram of an uncontrolled rectifier topology

Uncontrolled rectifiers (refer to Figure 4.3) do not have the firing problems associated with line commutated rectifiers. In the rectifier-inverter arrangement of a variable speed drive, a DC bus capacitor is installed between them for input filtering to the inverter. If during a dip the capacitor discharges such that the DC bus voltage is significantly lowered, during voltage recovery to normal, the capacitor will charge. The charging current and the inverter load may overload

the power switching devices of the rectifier. For protection, a DC bus undervoltage relay is usually used.

4.1.6 Variable speed drives

Some drives are designed to ride through voltage dips. The ride through time can be anywhere from 0.05 sec to 0.5 sec, obviously depending on the manufacturer and model. Some models of drive manufacturer monitor the AC line and trip after a voltage dip to 90% of normal voltage is detected for 50 ms. Manufacturing industries mainly employ two types of drive – namely the induction motor drive (AC drive) and the DC drive. An AC drive employing a voltage source inverter uses an uncontrolled rectifier to produce the DC voltage, which then supplies the PWM (or stepped) inverter. As an alternative, the rectifier can be line commutated. A typical DC drive uses a phase-controlled rectifier. As can be deduced, the voltage dip tolerances of these drives are very much influenced by their rectifiers and inverters.

4.1.7 Energy storage

Rotating machines have a kinetic energy storage capability given by $I\omega^2$, where I is the moment of inertia and ω is the radial velocity. The kinetic energy stored enables the machine to remain unaffected by fast transient events. Capacitance stores energy according top the equation $\frac{1}{2}CV^2$, where C is the capacitance in Farads and V is the capacitor voltage. In a simple passive RC circuit, where the load is connected parallel to the capacitor, the voltage across the load changes according to the equation $V^{load} = V^{new} + (V^{old} - V^{new})e^{-t/RC}$.

This can be interpreted as the capacitor holding the voltage to the old value and having a hold-up period as a function of the time constant RC. Increasing C therefore increases the hold-up period.

4.1.8 Programmable logic controllers (PLC's)

This is an important category of equipment for industrial processes because the entire process is often under the control of these devices. The sensitivity to

voltage dips varies greatly but portions of an overall PLC system have been found to be very sensitive. The remote I/O units, for instance, have been found to trip for voltages as high as 90% for a few cycles [28].

As can be seen from Figure 4.4, the AC bridge of the supply is an uncontrolled rectifier. Since the load most probably may not cause an overcurrent after a dip such as in a VSD the power supply is quite robust. The voltage hold up during the dip is very much influenced by the size of the DC capacitor.

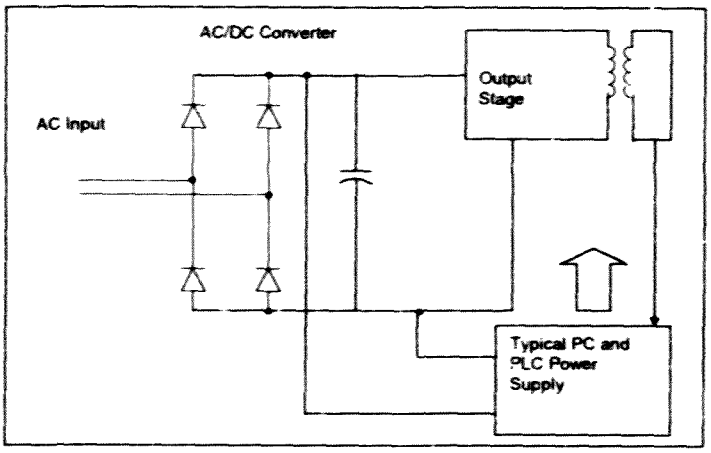


Figure 4.4 A simplified diagram of a PLC, PC and proximity switch power supply [31]

In a PLC, a line dip or interruption may cause a Normally Closed (NC) switch, which is not actuated, to change to its OFF state. An actuated normally open (NO) switch may likewise change to its OFF state during a voltage dip.

The proximity switch (figure 4.4) has a good voltage dip tolerance. The magnitude and duration of the dip affect the input state. In a proximity switch, a Normally Closed (NC) proximity switch may change to its OFF state. Conversely a normally open (NO) proximity switch may likewise, change to its OFF state. A voltage dip may also cause an error in digital logic. A proper co-ordination should be designed such that no inadvertent machine operation occurs during line disturbances.

4.1.9 Summary of equipment dip sensitivities

The dip sensitivity range for some types of equipment is shown in Figure 4.5 and presented in Table 4.1 with the durations of fault induced voltage dips also indicated. The wide range of dip sensitivities underlines the importance of working with a manufacturer to make sure the equipment can work in the environment where it will be used and to develop specifications based on realistic power system conditions [31]. It is important to recognise that the entire process in an industrial plant can depend on the sensitivity of a single piece of equipment. The overall process involves controls, drives, motor contactors, robotics, etc. that are all integral to the plant operation. This can also make it difficult to identify the sensitive piece of equipment after the entire process shuts down.

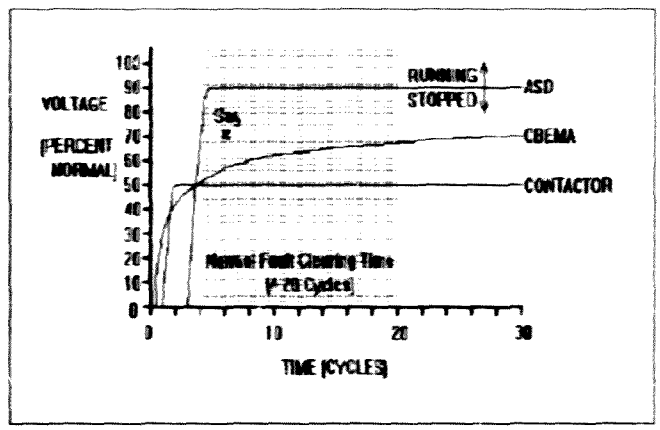


Figure 4.5 A range of equipment sensitivity to voltage dips [31]

Table 4.1 A summary of plant equipment sensitivities [31]

Equipment Type	Min. Voltage [%]	Max. Duration [ms]
Variable speed motor with electronics	85	10
Electromagnetic relays and contactors	50-60	15-40
Ferroresonant transformer fed sensitive load	50	0.5
PLC I/O device	90	20
Process controller	70	8
Off-the-shelf personal computer	50-70	60-160

4.2 The Variable Speed Drive and Its Environment

Proper evaluation of the variable speed drive includes discussing its environment in the plant. The discussion starts with voltage dip sensitivity and moves on to discussing drive types and functionality.

4.2.1 Dip sensitivity applied to variable speed drives

The equipment sensitivity presented in a CBEMA curve, uses dip depth (expressed as % of nominal voltage) versus duration (expressed in cycles or seconds). This was extended by proposals of the National Equipment Manufacturers Association (NEMA) subcommittee seven to divide drive sensitivity into regions [27] (shown in Figure 4.6).

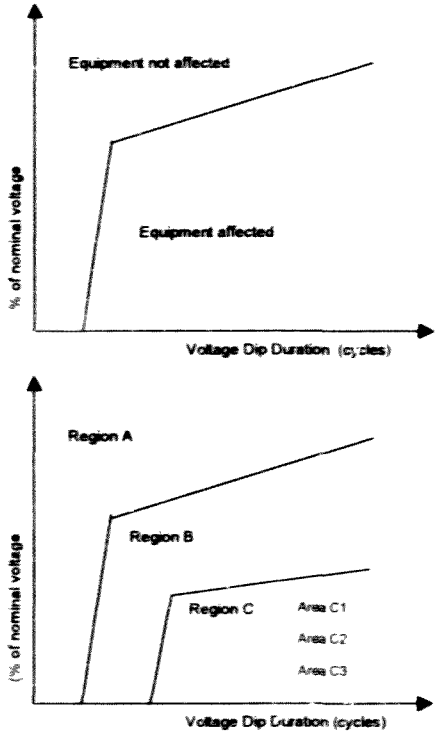


Figure 4.6 A range of equipment sensitivity to voltage dips

These regions can be described as follows:

- A: No degradation of performance
- B: degraded performance, but drive still has control of the motor current
- C: drive shutdown with possible restart, but drive has no control of the motor current

Three sub-areas are identified for region C:

- C1: synchronous restart (an inverter can start up the motor at the same speed)
- C2: Non-synchronous restart (an inverter restart may perturb the desired motor speed profile)
- C3: No restart (must be manually started)

4.2.2 Functions of variable speed drives

In a general sense, we can say that a motor drive is an apparatus that: a) transmits motion, or b) supplies the motive force to a motor in such a way as to control its speed. These controls may be as simple as a variable pulley or as complex as a microprocessor-based VSD. The most common variable speed drive methods are the following [6]:

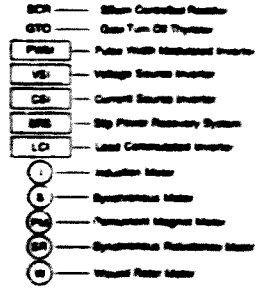
- Mechanical drives
- Hydraulic drives
- Direct current drives
- Eddy-current drives
- Multi-speed and pole-amplitude modulated motors
- Electronic variable speed drives

From these six types, the last one is becoming increasingly a preferred method thanks to the advances in semiconductor technology and is the focus of discussions.

So, in summary, it can be said that the function of a variable speed drive is to control the speed of a motor by varying the magnitude of one of its controllable variables such as voltage, current, or frequency.

4.2.3 Types of variable speed drives

The method used to vary the speed will largely depend on the type of load the drive is going to have. Since these loads have some sort of motor, either AC or DC, it is reasonable to make a drive classification based on the type of motor. Several drive classifications have been proposed in the past; some based on the type of the semiconductors (Figure 4.7); others based on the control strategy used in the drive. There are many other classifications e.g., stand-alone drives, regenerative drives, coordinated drives, and Programmable-Logic-Controller (PLC) controlled drives, etc



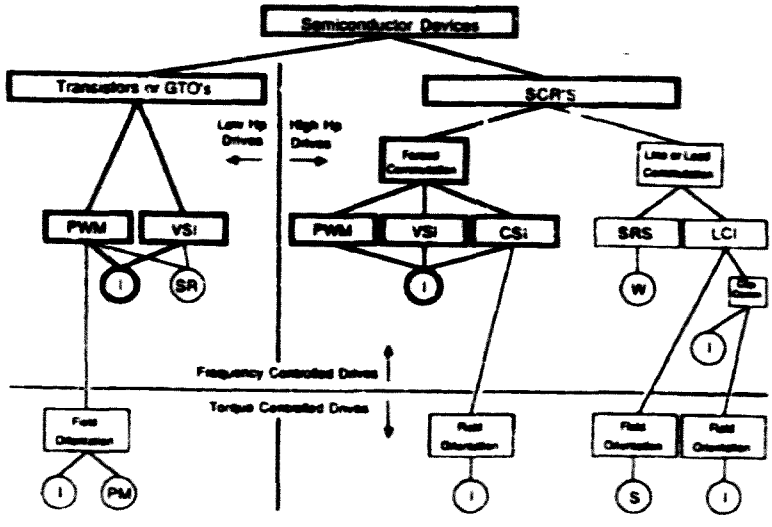


Figure 4.7 Semiconductor based drive classification [6]

Motor drives can be classified, based on the type of motors, mainly in two categories: DC Drives and AC Drives.

DC drives:

DC drives can be divided into those using phase-commutated converters and those with chopper control. The phase commutated drives are further divided into single and three-phase drives, as well as into those that provide motoring only and those that can regenerate back into the AC supply during motor braking. In this mode the motor acts as a generator (with negative induced voltage) and the converter acts as an inverter, so that mechanical energy stored in the inertia is converted to electrical energy and pumped back to the AC source.

This regenerative mode of operation becomes important when the system application requires of the drive to accelerate and decelerate frequently. Regenerative DC drives are also known as two-quadrant drives because the reversal of the motor voltage produces a reversal of the power flow. A second bridge converter can be connected in anti-parallel so that the dual converter can control the machine in all four quadrants (motoring and regenerating in both the forward and reverse directions).

Although DC motors require simple power converters and are easy to control, their construction is more complex and thus more expensive than that of a comparable induction motor due to the commutator on the rotor. The commutator also limits the motor maximum speed and restricts the environment in which DC drives can be applied.

AC drives:

AC drives, characterised by AC currents in the stator, can be divided according to motor or converter type. Motor type classification is more common and essentially consists of two groups: synchronous drives, where the rotor moves in synchronism with the stator field and induction (asynchronous) drives where there is a slip between the rotor and the stator field.

The synchronous motor group is growing, due to a continuous addition of new motors, most of which are still in the experimental stage. In addition to a division

of single-phase (of small ratings for low-power applications) and three-phase motors, the synchronous group can be further subdivided. In VSD applications, all members of the synchronous group normally need to have some means (such as rotor position feedback, for example) for synchronising the rotor with the inverter fundamental output frequency, that is, with the stator field. This is a serious application disadvantage, which explains the overwhelming industry preference for induction motors.

The other category of AC drives is the induction motor drive. Although induction motors represent today over 99% of all AC motors, which draw power from AC lines, their further division is simple – into single- and three-phase motors. Since induction motors tend to dominate the market, manufacturers have come up with a great variety of drives to satisfy the industrial as well as the residential consumers. Thus, for induction motors and synchronous drives as well, VSDs for AC motors can be further divided into the following main types.

Voltage source inverter (VSI) drives: These drives have a controlled (thyristor) rectifier which regulates the DC voltage, and a capacitor as the DC link which provides a constant DC voltage to the inverter section, hence its name, Voltage Source Inverter.

Current source inverter (CSI) drives: These VSDs also have a controlled (thyristor) rectifier and are characterised by a large inductance in the DC link, which provides a constant DC current to the inverter, hence its name Current Source Inverter.

Pulse-width-modulated (PWM) drives: Pulse width modulation is a technique that can be used to control the output voltage and/or frequency of the drive. Thus, in addition to the original control methods used in the VSI and CSI drives, both of these drives can be found with this type of speed control. Most PWM-VSI drives are found in ranges below 100kW. Furthermore, thanks to new advances in power electronics, which has allowed for the development of a great variety of VSDs, each one of them further divides into more types.

VSDs consist mainly of six parts (Figure 4.8):

- Rectifier or converter circuit,
- DC link with a filter,
- Inverter circuit,
- Control processing circuitry,
- Control signals from the operator (from two or more knobs or an alpha-numeric membrane pad), or from the plant controller (as analogue input from a potentiometer setting or as digital reference via a serial interface).
- Feedback control signals from the motor, which may come from signal transducers attached or connected to the motor.

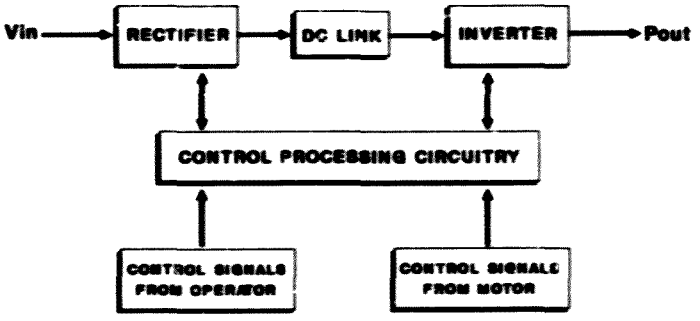


Figure 4.8 *Simplified block diagram of an AC variable speed drive* [6]

Circuit configurations: VSDs differ in the method of DC to AC power inversion and in control techniques. The main methods used to date are the following: the VSI, the CSI, and the PWM. A simplified block diagram for these three main types of VSDs is shown in Figure 4.9.

Features: The features of the main VSDs of figure 4.10 are many; however, for an example of some of them see Table 4.2, which shows a compilation of several key VSD features.

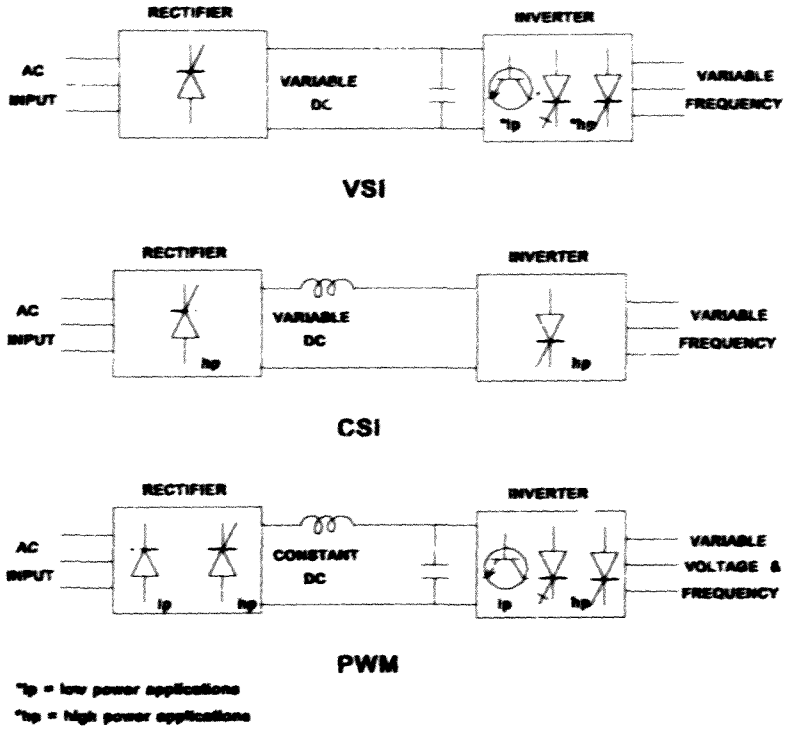


Figure 4.9 Basic circuit configurations of the main VSDs [6]

Table 4.2 Some Features of the Induction Motor VSDs (lp – low power applications; hp – high power applications) [6]

FEATURE	VSI	CSI	PWM
Rectifier device	SCRs	hp: SCRs	lp: diodes, hp: SCRs
DC link device	LC filter	L filter	LC filter
Inverter device	lp*: transistors, hp*: GTOs, SCRs	hp: SCRs	lp: transistors, hp: GTOs, SCRs
Torque control	Voltage & Frequency	Current, Voltage & Freq.	Current, Voltage, & Freq.
# of Motors	Many	Single	Many
Motor Impedance	Independent of	It is matched	Independent of
Power Factor	Low 0.90s	Low 0.90s	High 0.90s
Efficiency	Medium	Low	High
Other	Hi-output frequencies	Simple controls	High-Order Low-magnitude harmonics

Benefits: The main benefit from VSDs is their energy performance. In some cases, VSDs can reduce energy requirements by 30-50%, while minimising wear and tear. This feature alone makes them very attractive to consumers. EPRI [6] lists five other benefits:

- Improves system efficiency
- Improves equipment reliability
- Enhances product quality and reduces product waste
- Reduces the noise level
- Saves space

Applications: There are four dominant areas where VSDs are being used: pumps, compressors, fans and blowers, and air conditioning units. Furthermore, the use of drives in fans can also be divided into two primary areas: commercial and industrial. Commercially, they can be found, for example, in variable air volume systems, and air handling equipment. For industrial use, drives are used in induced draft fans, forced draft fans, boilers, exhaust hoods, process fans. For a summary of the relationship between load types and their applications, Table 4.3 illustrates several examples.

Table 4.3 Load types and applications [6]

Load Types	Applications
1. Constant T, Hp varies as the speed.	1. General machinery, hoists, conveyors, printing press, etc., represent 90% of applications.
2. Constant hp, T varies inversely as speed.	2. Metal cutting tools operating over wide speed range. Extruders, mixers, machines where operation at low speed may be continuous.
3. Hp varies as (speed)^2, T varies as speed.	3. Positive displacement pumps, some mixers, some extruders.
4. Hp varies as (speed)^3, T varies as (speed)^2.	4. All centrifugal pumps, some fans and blowers. Note: blower and fan power may vary as the 5th power of speed.
5. High-inertia loads.	5. Machinery using flywheels to supply most of operating energy, punch presses, etc.

4.3 The Impact of Voltage Dips on Variable Speed Drives

General discussions about the sensitivity of VSDs to voltage dips in previous sections are adequate as an overview, but more discussion is needed to describe drive type behaviour and the behaviour of interfacing circuits.

4.3.1 The impact of voltage dips on CSI drives

CSI drives are considered more dip sensitive than the other drive types. They are sensitive to dips of 10% (30% for more robust drives) magnitude [1].

A current source inverter is one in which the load current cannot change rapidly. This is achieved through the incorporation of a series inductor in the DC link. Varying the input AC voltage to the inductance controls the load current change.

CSI inverters are rugged and, due to sizing of the DC link inductance, can limit the short circuit currents thereby obviating the need for fuses to protect inverter components.

A simplified circuit using SCR's is shown in Figure 4.10 below.

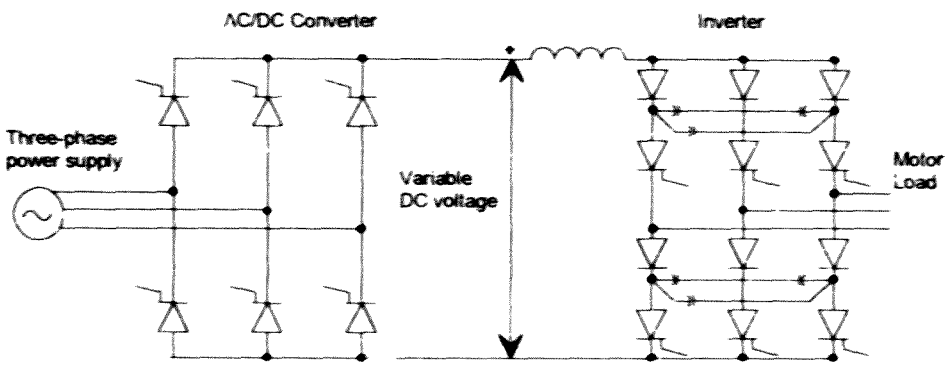


Figure 4.10 Simplified circuit diagram of a CSI variable speed drive

The output voltage waveform, generated by the back emf of the motor, contains spikes caused by SCR commutation. To change the frequency of the motor, the conduction time of each SCR is altered as shown in Figure 4.11 below.

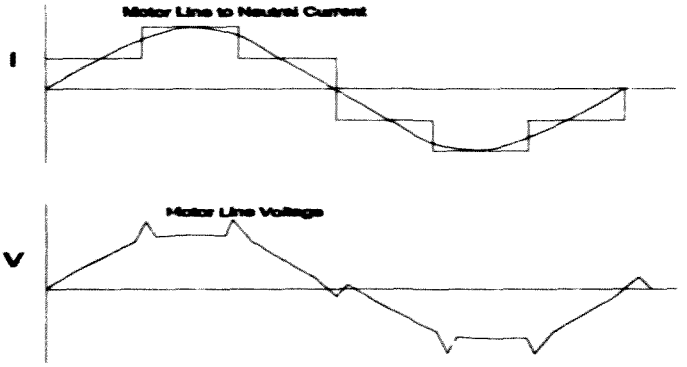


Figure 4.11 The output waveforms of a CSI variable speed drive

Balanced voltage dips are of lesser concern to CSI drives as there is no DC bus voltage to support. However, unbalanced voltage dips such as single-phase dips, phase-to- phase dips and dips with sudden phase angle changes (phase angle jump) may cause problems for the drive's line commutated front-end. Firing angle disruptions and misfires may result – so called commutation failure. This is more likely during regenerative braking.

CSI drives may suffer from commutation failure if:

- There is a sudden drop in magnitude of the input line voltage
- There is a sudden change in the phase angle of the supply voltages during a voltage dip
- The input line voltage is distorted by transformer energisation and capacitor switching

If no commutation failure occurs, CSI drives are more robust because of their DC link inductance.

4.3.2 The impact of voltage dips on DC drives

Historically DC machines have been used in VSD applications whereby the torque is controlled via the armature current and the speed via the field current. Efficiency, brush and commutator wear, have been the major reasons for movement away from them.

DC drives may trip for single-phase, phase-phase and three-phase voltage dips of greater than 10% magnitude [29]. Voltage sensing for under-voltage protection is usually on the AC supply, but may be on the DC bus as well. The sensitivity is a function of drive speed and rated load when the dip event occurs. Generally higher speed and larger load results in smaller adjustment margins for firing angle. Therefore the drive decelerates. On the other hand, lesser speed and load results in greater margins, more room for adjustment by the controller and hence a lesser effect on the speed of the drive.

Another situation may occur where the thyristor firing pulses are blocked during the dip. If the drive is not tripped or shut down, the motor speed reduces significantly. This rate of deceleration is a function of the loading and the motor inertia. When the voltage recovers and the drive re-accelerates, a large current is drawn from the supply that may cause a secondary voltage dip. This is especially true if the AC system is weak and the motor requires a high acceleration torque. The amount of current drawn by the drive will depend on the drive's control gains and algorithms used for re-acceleration. The secondary dip may cause instability of the drive and of other loads in close proximity.

As with CSI drives, unbalanced voltage dips such as single-phase dips, phase-to-phase dips and dips with sudden phase angle changes (phase angle jump) may cause problems for the drive's line commutated front-end. Firing angle disruptions and misfires may result – so called commutation failure. A large motor armature current will flow given the low AC supply impedance, resulting in a large braking torque and severe mechanical stress to the coupling.

DC drives may suffer from two types of commutation failure:

- Armature fault current flows through the thyristor front-end and the AC supply (see Figure 4.12).
- Armature fault current flows through the thyristor front-end (Figure 4.13).

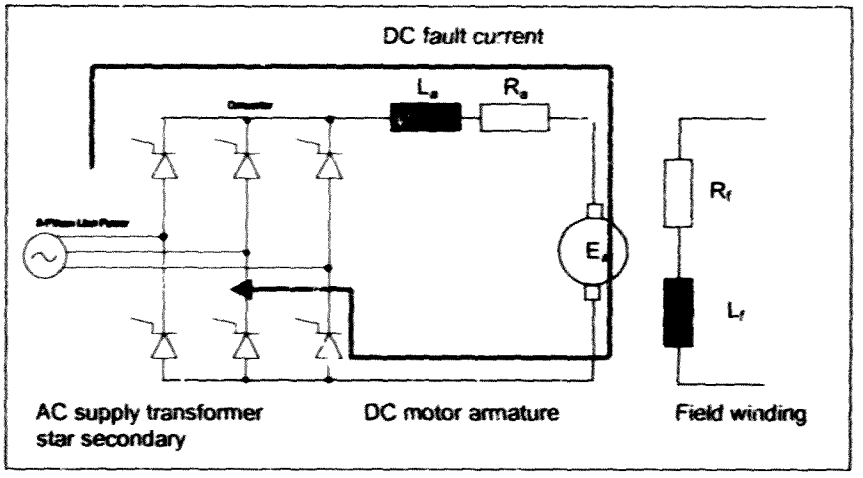


Figure 4.12 Commutation failure – DC current through AC supply transformer [1, 29]

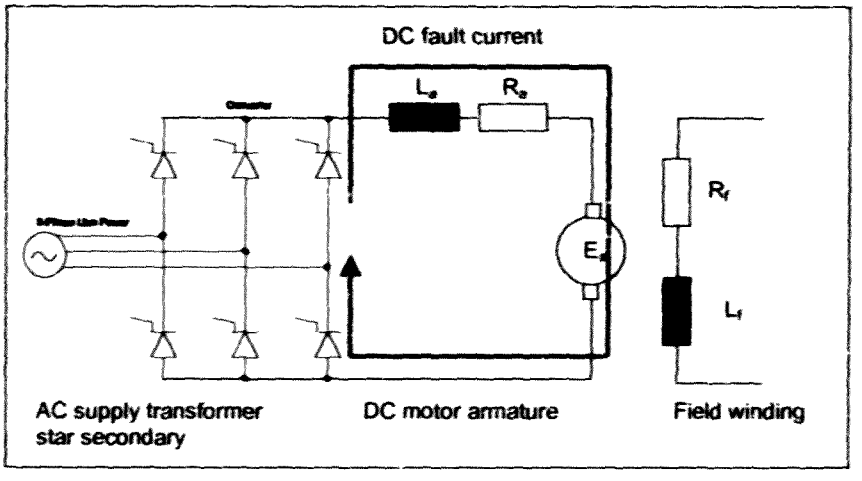


Figure 4.13 Commutation failure – DC current through thyristor stack [1, 29]

4.3.3 The impact of voltage dips on PWM drives

A voltage source inverter (VSI) is one in which the dc input voltage is essentially constant and independent of the load current drawn. They are characterised by the use of capacitors in the dc link. Voltage source inverters require built in fuse protection for the inverter to protect against internal and line faults. PWM drives are a type of VSI drive. VSI drives can also have a stepped inverter circuit (e.g. six pulse as shown in Figure 4.14). The silicon-controlled rectifiers (SCR) are switched in sequence to produce a six-step, three-phase voltage wave for the motor. By altering the conduction times of each SCR, a variable frequency output is produced in order to maintain the constant volts-per-hertz to the motor as voltage is altered. The output waveforms are shown.

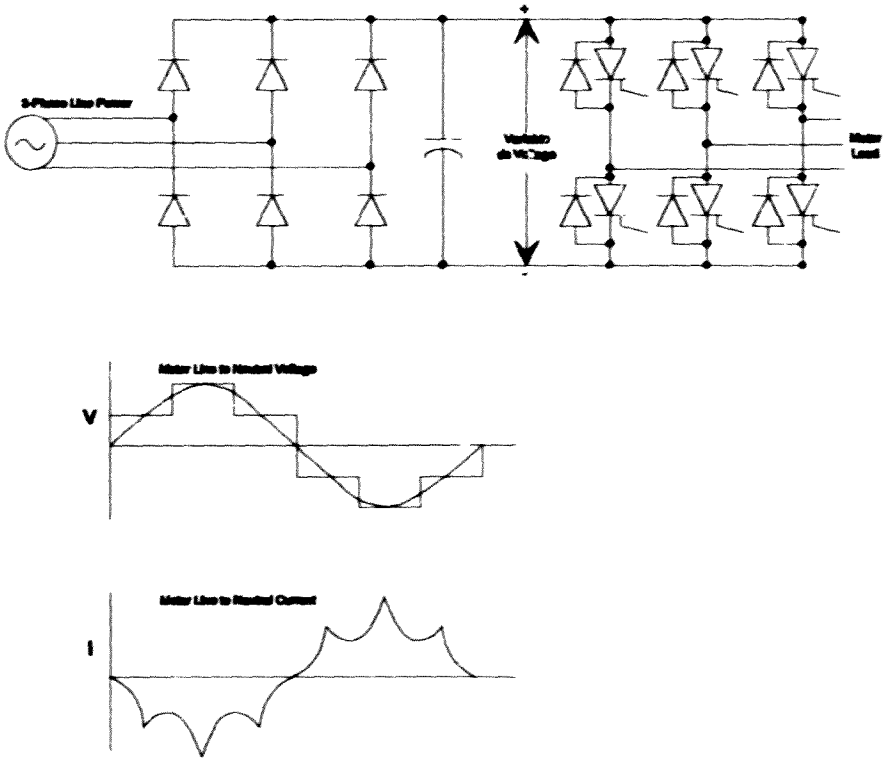


Figure 4.14 A six step VSI VSD and its output waveforms

The PWM technique can be applied to both CSI and VSI inverters. By varying both the number of pulses and their width during each half-cycle, precise motor speed control can be achieved. Figure 4.15 below shows the output waveform of a VSI drive. This type of PWM drive will be the focus of discussion.

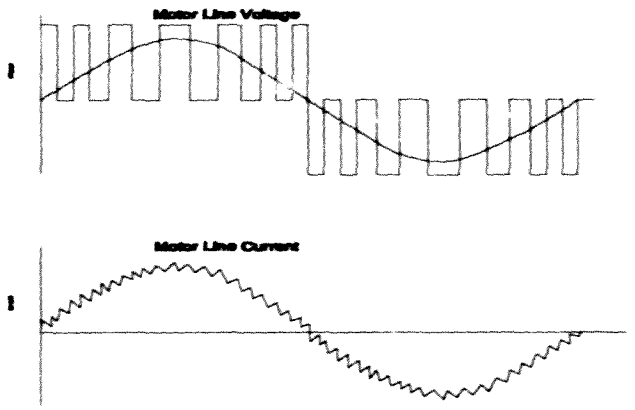


Figure 4.15 The output waveforms of a PWM VSI drive

Where high-speed responses without speed oscillations are required, vector control is used. This involves a complex machine response model and integrated control. If regeneration back onto the power system is required, for purposes of braking or energy efficiency reasons, the CSI with SCR front end is well suited. With PWM and VSI inverters, an additional front end as shown in Figure 4.16 below is needed.

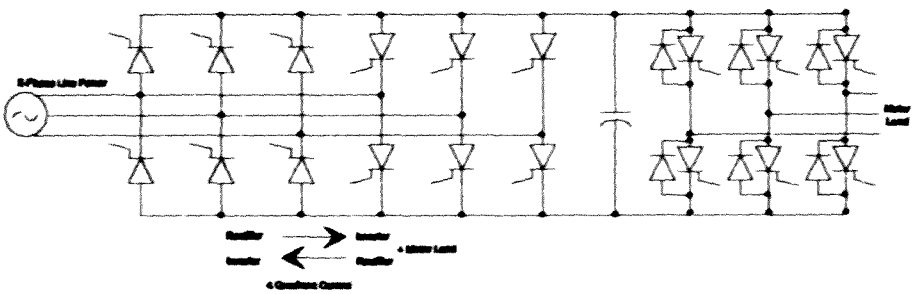


Figure 4.16 A simplified circuit diagram of a four-quadrant drive

For AC line faults or phase shifts, short circuits between phases in the converter can occur (simultaneous SCR conduction). The dc link capacitor is then shorted through the SCR's with consequent damage unless fuses are incorporated.

PWM drives are the most common type of drive topology found, especially in smaller drives, in industry. PWM drives maintain a constant DC bus voltage and has a capacitor fitted to aid this. A voltage dip does not allow the converter to maintain the constant voltage. PWM drives have undervoltage protection on the DC bus. For most drives, this trip point is set between 50% and 85% [28]. Higher load power levels will have shorter RC time constants and the DC bus will discharge more rapidly. Drive manufacturers limit the DC bus capacitance to reduce costs and packaging requirements. While under load, the DC bus voltage will track the source voltage because the DC bus capacitance is limited.

During voltage dips, the DC bus voltage will track the source voltage once the load has discharged the capacitors down to the source voltage level. The rate of discharge is therefore a function of the load power and the DC bus capacitance. The DC undervoltage trip point determines how the drive reacts to a dip. The longer the discharge on the DC bus, the longer the motor and load will continue to operate. Thus, from a manufacturers point of view, the duration of the dip is not as important as the remaining source voltage. No matter how long the dip lasts, the DC bus will continue to charge to the peak of the remaining source voltage.

A pre-charge circuit is used to charge up the filter capacitors during power up. Whatever specific technique is used, the aim is always to charge the capacitors from 0V to the full DC voltage, while limiting the current. After this process is complete, the pre-charge circuit is disabled. This implies that a voltage dip can result in a high re-charging current when the voltage is restored to normal if the pre-charge circuit remains disabled during the dip.

Three-phase dips are of most concern for PWM drives, however single-phasing causes more ripple on the DC bus, causing motor current fluctuations and instability. The line currents will also increase on the two healthy phases, resulting in possible fuse operation.

During deep voltage dips, the drive's DC bus voltage will drop significantly. When the voltage recovers abruptly, it is associated with a large inrush current. The peak of this current can be three or more time the peak full load current, but is limited by the source impedance. Small drives are very susceptible to damage due to high inrush current. The drive, drive controls and the process may survive, but the input protection fuses may blow. Sometimes only one of the three input fuses will blow. This results in a single-phasing condition, causing overcurrents to exist when the drive is significantly loaded. Two phases must carry the burden of charging the DC bus. Serious rectifier damage will occur when sustained overcurrents are drawn by the DC bus capacitor.

For most PWM drives, the DC bus undervoltage trip point would not be reached for a single-phase dip, even when the phase-neutral voltage goes down to 0V. The DC bus voltage remains above the undervoltage trip point when one phase-phase voltage remains at 100%. Most likely, if a PWM drive trips during a single-phase dip, it is because of another reason, such as the drive interface and its circuits. This is discussed in the next section.

More voltage dip sensitivity testing have been done for PWM drives than for other drive types. Results from these tests show that:

- Drive loading at the time the dip has a significant effect on the ride-through capability of the drive.
- The drives of different manufacturers have significantly different ride-through characteristics.
- Three-phase dips are significantly more severe than single-phase or phase-phase dips.

4.3.4 The impact of voltage dips on the drive interface [28]

Drive control transformer:

Early versions of AC drives derived control power directly from the AC line (Figure 4.17 . This resulted in logic circuit disruption during voltage dips. Sometimes the DC bus undervoltage sensing circuitry would be supplied in this way, which meant that a shut down command was the result of a low transformer secondary voltage and not a low DC bus voltage. A single-phase dip that would otherwise not have affected the drive could now cause an unnecessary trip. In newer drive designs, the control power is derived from the DC bus using a switch-mode power supply. The advantage is that the DC bus capacitor voltage cannot change instantaneously. The DC-to-DC converter may itself have some capacitance at its output, providing more dip ride-through support.

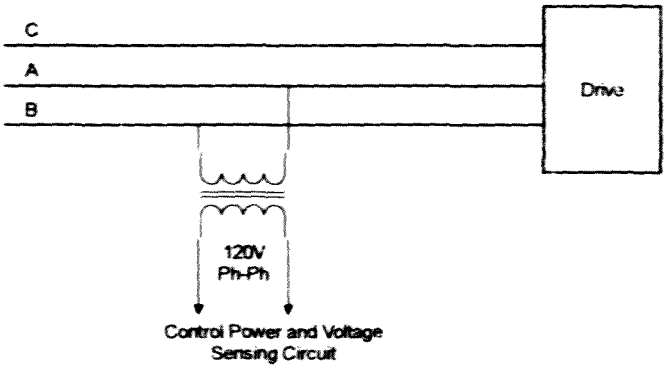


Figure 4.17 A simplified circuit diagram of a drive control transformer scheme

From the figure, the following can be said:

- A dip on phases A and B will reduce the secondary transformer voltage.
- A phase-phase dip would depend on the combination of phases. Phases A and B would be the worst case. Other combinations have a lesser effect.
- A three-phase dip would be the same as the worst case, no matter which phases it was powered from.

Dip mitigation can be done by conditioning of the input voltage, either with a constant voltage transformer or a UPS. Other issues should be considered, however, such as timing circuits and control inrush current.

Drive interface circuits:

Many drive installations require the presence of a line-side contactor. The problem with these contactors is that the contactor may be more sensitive to voltage dips than the drive itself. For example, a contactor, upstream from a VSD may drop out for a single-phase dip that a drive could have survived. This causes a three-phase interruption to the drive. If the contactor drops out at say 65% of nominal and the drive trips at 45%, the ride-through of the entire system is compromised. When troubleshooting drive trips, the fault codes should be analysed. If a DC undervoltage was the cause, the presence of a line side contactor should be investigated. Single-phase conditioning of the contactor may be the answer. However, the issue is that the contactor increases the sensitivity of the system. It would be easiest to consider not using such a control scheme.

Start/stop circuits are also additional sources of sensitivity. Modern VSDs are controlled in a variety of ways, from relays to PLCs, using different logic schemes. One should be aware of the control scheme and whether latched circuits and relays are used.

Interface circuits using PLCs:

PLCs are often used to provide the signals for drive controls. The outputs from PLCs can either be discrete (e.g. relays, triacs) or analogue (e.g. speed, torque). A few basic rules should be observed when dealing with voltage dips:

- When the PLC power supply voltage falls below a trip threshold, the PLC shuts down. The PLC outputs will be shut off or opened.
- A voltage dip may cause the PLC to sense a change in input states and mistakenly change the state of the outputs.
- If the power for analogue signals is derived from the PLC power supply, the outputs may change during a dip resulting in the incorrect feedback signals.
- Usually, the power for discrete outputs is derived from an external power supply, which may be affected by the voltage dip. This could change the apparent state of the outputs.
- The input/output (I/O) racks local to the PLC are usually powered from the PLCs power supply. Remote I/O racks are powered from their own power supply. This power supply can be a weak link and allow corruption of the PLC output signals.

4.3.5 The influence of programming features on voltage dip ride-through

Solving VSD voltage dip trip-related problems requires a system-wide approach. All aspects of drive interface susceptibility should be ruled out or proper power conditioning should be applied before focusing on the VSD dip ride-through. Assuming all necessary steps have been taken to immunise the external circuits, the drive programming features will determine the ride-through performance of drive applications. Some of the main programming features used by drive manufacturers of PWM AC drives to minimise voltage dip impact, are discussed.

Undervoltage trip point:

The manufacturer will set minimum operational requirements for the DC bus voltage before deciding on an undervoltage trip point. When the voltage reaches that point, the programming prioritises prevention of damage to the drive, motor and process. The following may be reasons for a DC bus undervoltage trip point:

- Many manufacturers use a switch-mode power supply to provide power to the logic control circuits. This voltage must be adequate for the normal control operations else the power supply must cease its operation.
- The drive must never be cut off from its control equipment. Some industrial processes must restart immediately after a dip to prevent compromising worker safety. An undervoltage trip point is set well above the minimum operating voltage of the power supply, preventing loss of control power.
- The drive must discontinue operation of the motor and load to reduce current inrush during dip recovery. A pre charge circuit may be used to limit this current. Input line reactors may also be used to limit the current.

Automatic reset and restart:

Automatic reset features allow drives to automatically reset internal fault conditions generated by software protection. Although protection features are designed to protect the drive, motor and load, they also prevent the drive from continuing operating. Some AC drives permit the user to disable specific fault conditions to prevent the drive from tripping and shutting down the process. It is advisable to contact the drive manufacturing before this is done. The drive may attempt to restart the motor when fault conditions have ended. This allows the user to set the number of times the drive attempts to restart.

Non-synchronous restart:

Processes that do not require speed and torque regulation will benefit from a non-synchronous restart. Under this condition, the drive stops operating the motor and load, which are allowed to coast. The output torque of the motor drops to zero and the speed reduces. The system decelerates as a function of the system inertia and load torque. Systems with higher inertia will take longer to spin down than systems with low inertia. Once the DC bus voltage rises above the undervoltage trip point, the drive resumes operation of the motor and load. The drive is programmed to start the motor at a pre-programmed starting frequency or at the last pre-dip frequency. The motor accelerates at a set ramp-up rate. If the drive resumes operation of the motor starting at a frequency that is significantly different to that of the motor, large torque and speed transients can be induced on the motor and load. This is more so if the system has a high inertia.

Non-synchronous time-delay restart:

Some applications require a significant speed reduction or a complete system reset before it can be restarted. This includes high inertia loads such as centrifuges where speed and torque deviations are not important. The non-synchronous time-delay restart is used to restart these applications after a pre-programmed time interval

Non-synchronous ride-through with flying restart:

Processes that can tolerate significant speed and torque deviations are suitable for this strategy. When the DC bus voltage recovers to its trip point, the drive performs a flying restart to determine the actual speed (frequency) of the motor and accelerates the system back to its original operating point. The speed change depends on the duration of the dip, the system inertia and the load torque. This approach never actively allows the system to come to a halt although this may still happen. If the system stops, the situation is the same as for a normal synchronous restart. The algorithms used by different manufacturers are different, some being more accurate than others. Therefore, process engineers should consult drive and process machine manufacturers before enabling flying restart options.

Synchronous ride-through for single drive applications:
There are distinct differences between synchronous and non-synchronous ride-through. In this strategy, the drive never loses control of the motor and load. A method called kinetic buffering is used to hold the DC bus voltage above the undervoltage trip point regardless of the dip depth. Kinetic buffering uses the system inertia to boost the voltage of the DC bus. The drive therefore uses the motor as a generator

The drive dynamically brakes the motor by adjusting its output frequency to be less than that of the motor. The difference in frequency determines the magnitude of the applied braking force. Higher braking forces result in higher DC bus voltages. Systems with high inertia will experience less speed change because they have more stored energy. Since the drive operates the motor as a generator and absorbs energy from the load, the energy drawn from the DC bus is significantly reduced. The switch-mode power supply is the largest remaining load to discharge the DC bus. Thus, the braking force required to keep the DC bus above the undervoltage trip point is small. The load consumes most of the stored mechanical energy to sustain its rotation

When the DC bus voltage recovers to the undervoltage trip point, the drive accelerates the motor and load back to their original operating point based on a pre-programmed ramp-up rate. Processes that require continuous control over motor and load or have significant inertia will benefit from this strategy. Because the DC bus voltage level is maintained at a higher level, inrush currents will be less and rectifiers and fuses less likely to be damaged. Again, not all manufacturers have the same algorithms, as with flying restart algorithms.

Synchronous ride-through for common DC bus applications:
Some industrial production lines use VSDs at several positions throughout the process. These drive are often connected to a common DC bus where a large rectifier and capacitor bank serve many drives. Processes that are extremely vulnerable to speed and torque changes between positions as found in the pulp, paper and textile industries, benefit from this strategy. Any significant speed and torque changes from one position to the next can result in breakage or stretching of the product.

Since all the drives detect the same DC bus voltage, they will respond at the same time. These drives are usually programmed to follow pre-programmed deceleration and acceleration rates when the DC bus voltage drops and recovers. Process speed and torque changes, but there will only be small differences in positions. It its less likely for the product to be damaged and the process can continue to operate without production delays.

Summary:
The acceleration rate (ramp-up), deceleration rate (ramp-down), current limit, and torque limit are all very important programming features to consider when applying ride-through features. Incorrect settings are dangerous for all equipment, product and operators involved. Most of these features revolve around the undervoltage trip setting of the DC bus voltage. Recently AC drive manufacturers provided software revisions for their products, making it possible to change this setting. Drives and processes will be able to ride-through longer and deeper voltage dips. However, the dangers associated with changing this setting as discussed in this section, should be kept in mind. There may be other drive programming features that become available from time to time. Without a full understanding of these, it is always recommended to verify them with manufacturers.

4.3.6 AC drive voltage dip ride-through alternatives

Programming features are not always sufficient in solving voltage dip trip problems for some AC drive applications. Another approach is to provide additional support to the DC bus of the drive. There are many different mitigation options for AC and DC drives, the discussion of which is beyond the scope of this report. Several publications discuss these in more detail [1,4,28,29]. However, to maintain the relevance to the subject of this report, some of these will be mentioned briefly. All of the approaches are attempts to support the DC bus voltage to prevent falling of the DC bus voltage to below the undervoltage trip point. These methods are included in the discussion because their application in the laboratory for voltage dip testing is possible and have in fact been done already [28].

Additional DC bus capacitors:

Additional capacitors on the DC bus increase the energy storage capability of the drive. The amount of stored energy is directly proportional to the total DC bus capacitance. This is true for single drive applications as well as common-bus applications. The capacitors are sized according to the necessary ride-through time and energy requirements of the load. The size of the capacitor bank is an issue for most applications. Therefore space requirements should be considered when applying this ride-through technique. It is easy to implement this ride-through option in the laboratory.

Additional DC bus capacitors should not be used for applications requiring ride-through during long duration voltage dips. They are simple to implement, but costly at the same time. Their maintenance requirements and performance during short voltage dips make them attractive for low power applications.

Boost converters:

A boost converter (Figure 4.18) is a DC-DC converter that boosts one DC voltage level to a higher output DC voltage level. A boost converter draws power off the AC supply and its output connects directly to the DC bus of the drive circuit. The components include an SCR, an inductor, a diode, filter capacitor and an IGBT.

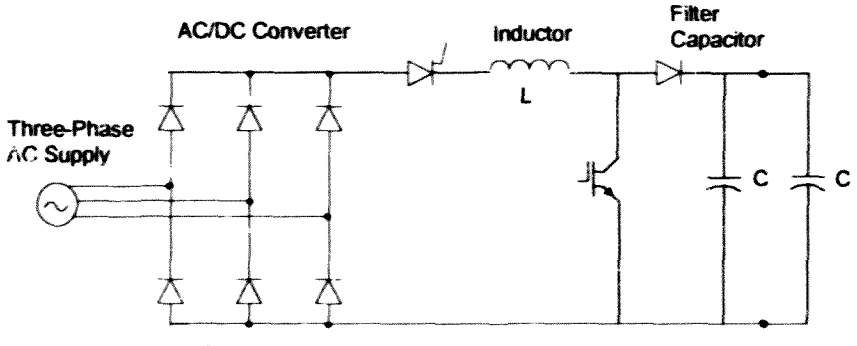


Figure 4.18 A simplified circuit diagram of a boost converter [28]

When a drive's DC bus voltage drops to a pre-selected limit, the boost converter operates, attempting to maintain a constant DC bus voltage. It does this with energy stored in its inductor. Otherwise it is idle. Two modes of operation are determined by current flow through the inductor. The converter controls establish a hysteresis band for the inductor current. In the first mode, the IGBT short-circuits the inductor across the rectifier during which the inductor charges off the rectified dip voltage. When an upper current limit is reached, a second mode begins during which the IGBT opens and the inductor discharges into the filter capacitor and the drive's DC bus. If the inductor current falls to the lower limit, the cycle repeats until the DC bus voltage recovers from the dip.

There may be a point when the remaining voltage during the dip is not enough to allow the boost converter to maintain the drive's DC bus voltage. The boost converter then discontinues its operation. This can happen during deep dips (>50%), unless the boost converter is de-rated.

Boost converter with energy storage capacitors:
Additional capacitors extend the function of a boost converter (Figure 4.19). The boost converter operates after the energy storage of the capacitors is depleted. The extended ride-through depends on the amount of capacitance and the boost converter will shut down if the remaining voltage falls below the lower limit.

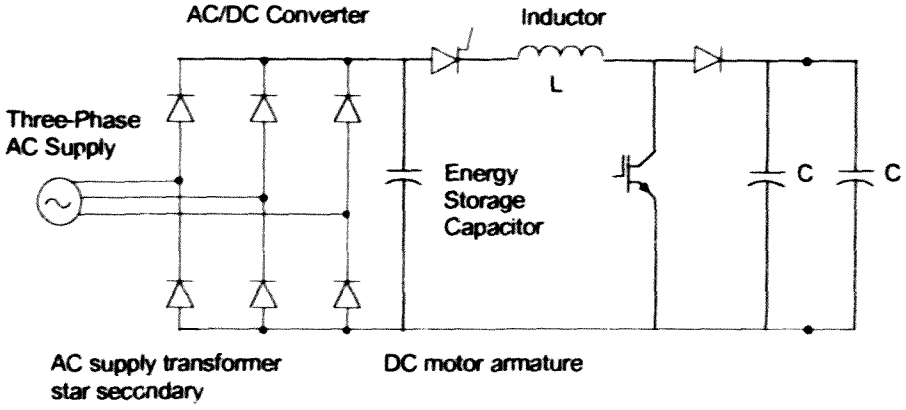


Figure 4.19 A simplified circuit diagram of a boost converter with additional capacitor storage [28]

Summary:

A comparison was done [28] to compare the three mitigation options discussed in combination with a 5hp, 460V PWM AC drive (Figure 4.20 and 4.21). The option without mitigation is also shown. Two types of drive trip conditions were set. One of these is a speed trip condition, defined as a speed change greater than 5% of nominal full load speed (in this case 1740 rpm as the test was done in the USA). The other is a torque trip condition, defined as a torque change greater than 5% of nominal full load torque (10.5 Nm). A constant-torque load type was used in both cases.

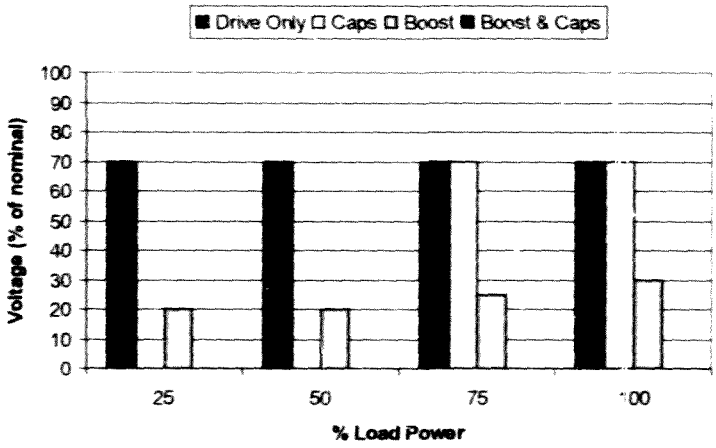


Figure 4.20 Speed trip points at various load levels for a PWM drive with and without ride-through options for 30 cycle (at 60 Hz), three-phase voltage dips [28]

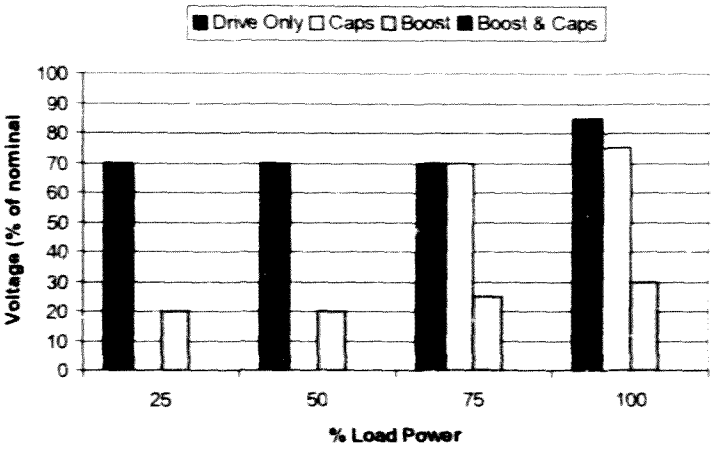


Figure 4.21 Torque trip points at various load levels for a PWM drive with and without ride-through options for 30 cycle (at 60 Hz), three-phase voltage dips [28]

As a final guideline for users of PWM AC drives, the following should be checked to improve drive ride-through during voltage dips:

1. Determine the requirements of the process application to know the amount of ride-through required.
2. Examine wiring diagrams and schematics for interface circuits that could be sensitive to voltage dips and could be improved with power conditioning.
3. Consider power conditioning from the drive's control transformer, especially if it is powered from the AC line.
4. Consult the manufacturers of the drive and process equipment to discuss the programmable restart options that may best suit the application and how to determine the best settings.
5. Investigate the possibility of adding voltage dip mitigation, e.g. DC bus supporting options for critical processes

5 A TEST PROTOCOL FOR VOLTAGE DIP TESTING

The reason for a test protocol for voltage dip testing is to establish a set of rules that are consistent for all similar tests undertaken locally (in South Africa) or internationally. By using such a protocol it will be easier to compare results from tests conducted at different test facilities. These comparisons will also have a more sound foundation. Where conditions, standards and the understanding of the processes involved are changing, these changes will be more thoroughly and efficiently implemented using a protocol.

The protocol developed here is not a final proposal and will require input from industry, manufacturers and utilities. The format of the protocol uses the IEC-61000-4-1 [7] as well as chapter 3 of the SC-610 EPRI-PEAC test protocol [6] as a basis and point of departure. Adaptations are made for the local conditions where applicable. The use of this protocol is demonstrated in part in the remainder of this report.

The central theme for the protocol is the testing process. However, the applicable standards, testing philosophy, environmental conditions and reporting formats are just as important. The following comprise the sections of the test protocol:

1. Applicable standards
2. A description of the test set-up and test environment
3. The testing philosophy
4. A description of the supply specifications
5. Loading conditions and load set-up
6. A description of the monitoring set-up
7. Drive inspection prior to testing
8. The installation and operation of drives
9. Evaluation of selected drive parameters
10. Normal operation of the drive
11. Testing methodology
12. Presentation of results

5.1 Standards Applicable to a Dip Test Protocol

The following standards contain provisions that may be applicable to voltage dip testing, as performed using the procedures outlined in the report. All standards are subject to revision and when used within the test protocol it is encouraged to investigate the possibility of applying the most recent edition of the standards listed below. These reference documents should be readily available.

1. IEC-61000-4-11: 1994 *Electromagnetic compatibility (EMC) – Part4: Testing and measuring techniques – Section 11: Voltage dips, short interruptions and voltage variations immunity tests*
2. DRAFT IEEE Standard 1159.2: (draft) *Recommended Practice for the Characterization of a Power Quality Event*
3. IEEE Standard 1250.2: 1995, *Guide for Service to Equipment Sensitive to Momentary Voltage Disturbances*
4. ANSI/IEEE Standard 995:1987-Part I, *IEEE Recommended Practice for Efficiency Determination of Alternating-Current Adjustable-Speed Drives*
5. IEEE Standard 1346: 1998, *Recommended Practice for Evaluating Electric Power System Compatibility with Electronic Process Equipment*
6. IEEE Standard 493: 1997, *Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems*
7. BS EN 50160: 1995, *Voltage characteristics of electricity supplied by public distribution systems*
8. IEC 60068-1: 1988, Environmental Testing – Part 1: General and guidance
9. ANSI/IEEE C62.41-1991, Recommended Practice for Surge Voltages in Low-Voltage AC Power Circuits
10. ANSI/IEEE C62.45-1992, *Guide on Surge Testing for Equipment Connected to Low-Voltage AC Power Circuits*
11. International Union of Producers and Distributors of Electrical Energy (UNIPEDE): 1991, No.50.02
12. UNIPEDE DISDIP, *Measuring of power failures in MV grid in Europe*
13. NRS 048-1:1996, *Electrical Supply – Quality of supply – Part 1: Overview of implementation of standards and procedures*
14. NRS 048-2:1996, *Electrical Supply – Quality of supply – Part 2: Minimum Standards*

5.2 A Description of the Test Set-Up and Test Environment

The following list of actions can be used to create a standard test environment [6].

5.2.1 Equipment used in the test

a) Select a VSD and a motor for testing
b) Record all VSD and motor specifications
c) Define the purpose, objectives and criteria of the investigation
d) Define the test set-up
e) Decide on the type of variable supply or load that will be used for the tests.
f) Define the specifications of each piece of equipment in the test set-up

A diagram should be drawn showing the relative positions of all the test equipment. Figure 5.1 and Figure 5.2 show schematics illustrating test facilities that focus on different aspects of voltage dip testing.

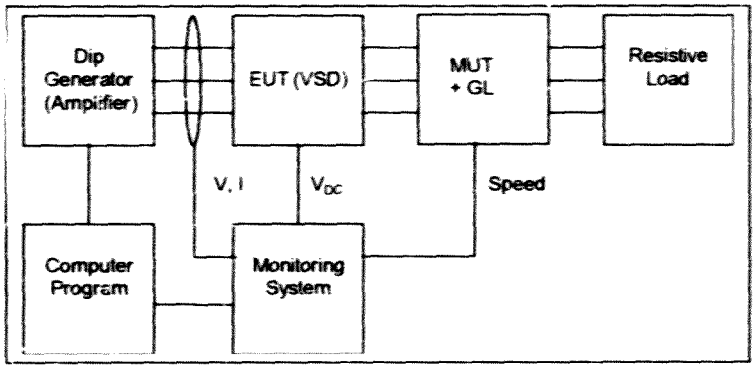


Figure 5.1 An example of a test set-up diagram with a programmable waveform generator. In the diagram, EUT = Equipment Under Test, MUT = Motor Under Test, GL = Generator Load

5.2.2 Variables to be measured

The variables to be measured should include at least:

a) VSD input voltage and current or

b) Motor input voltage and current or

c) VSD input voltage and motor current

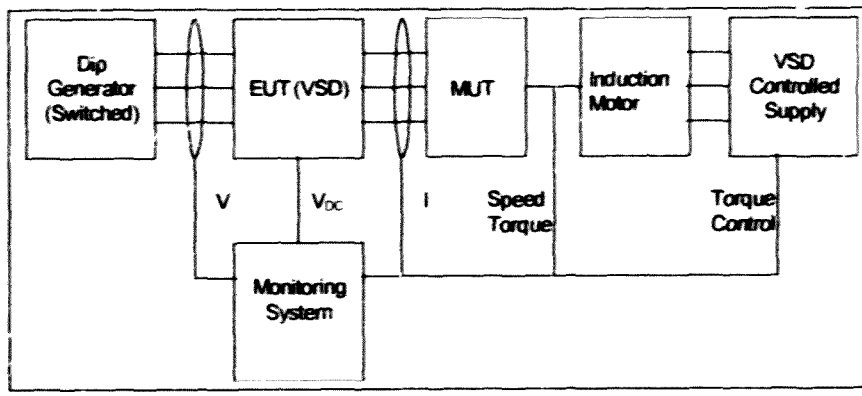


Figure 5.2 An example of a test set-up diagram with a torque-controlled dynamometer based programmable load.

Additionally, but critical for some analyses, the dc-bus voltage, motor speed and torque should be measured. These may also be critical for feedback in the supply and load control systems.

5.2.3 The test environment

The following tests conditions are based on the ANSI/IEEE standards 100-1988, 112-1984, and C62.41 and 45.

Table 5.1 Typical test conditions, as shown can be obtained from the drive service manual [14,15,16].

Item	Description	ANSI/IEEE standards 100-1988, 112-1984, and C62.41 and 45. Recommendations
1	Temperature and relative humidity	25 ± 5°C and < 85% humidity
2	Altitude	< 2000 m
3	VSD Input Voltage	sinusoidal waveform with THD < 1%
4	VSD Input Frequency	50 or 60 Hz ± 0.5%

5.3 Testing Philosophy, Purpose, Objectives and Criteria of the Test

5.3.1 The testing philosophy

Voltage dips are a common cause of equipment malfunction. This disturbance is a common direct cause of electronic system upsets. When VSDs trip, it is important to know what caused the trip. The cause for the trip could be anything from a low supply voltage to a low dc voltage. By testing for the susceptibility of such equipment to voltage dips, the answers to these types of questions can be answered. Although the methodology and presentation of results need to be done in a consistent manner, the reasons for doing the testing may vary between two testing facilities.

5.3.2 The Purpose and objectives for testing

The purpose of the testing of a VSD is usually to evaluate its voltage dip immunity. The specific purpose for such a test should always be noted. The information resulting from dip immunity testing may be confidential as specified by the sponsors of the drive testing. Records as to the identity of drives must be kept for referencing purposes.

Specific objectives of an investigation could be:

- Measure the dip behaviour by varying the dip duration from 20ms to 600ms, i.e. 1 to 30 cycles while continually increasing the magnitude of the dip.
- Evaluate the dip immunity for 25% and 75% full load conditions.
- Disable the drive ride-through aids, such as special controllers and auto-restart or flying-restart options, to identify the basic drive behaviour.

The specific objectives or instructions for a test should always be recorded with the test results.

5.3.3 Criteria that are relevant to the testing objectives

The criteria that will provide the basis for recording a trip event, could be:

- Changes in current that affect the supply
- Changes in torque that affect the process
- Changes in speed that affect the process
- Shutdown of the drive with automatic recovery
- Shutdown of the drive with manual recovery
- Complete shutdown (failure) of the drive with no recovery
- Recording the drive fault codes as a basis for establishing a trip, e.g. U/V or O/C.

There may be other conditions and these should be recorded under the trip criteria of the test. If the purpose is to characterise the susceptibility and trip levels of a VSD associated with processes with specific speed and torque deviation requirements, then define these speed and torque deviation requirements.

At this stage the format for reporting the drive trips under the relevant criteria must be established. These may take the form of, for example:

- Drive dip sensitivity plots in percentage of nominal voltage vs. duration in seconds (for the full test duration in cycles)
- Motor Speed vs. Time (with at least five cycles of pre-dip data)
- Drive Current vs. Time (at least one phase with at least five cycles of pre-dip data)
- DC Bus Voltage vs. Time (at least one phase with at least five cycles of pre-dip data)
- Drive Input Voltage vs. Time (at least one phase with at least five cycles of pre-dip data)
- All VSD parameter values entered via the programming interface must be recorded where their value could influence the trip decision.

The reasons for doing the voltage dip testing may vary depending on who initiated the testing. Information may be required for the design of a plant, the design or improvement of a VSD or as a reference of performance for plant investigations. The focus may be on individual drive dip performance or overall plant dip performance. Finally, safety issues of drive operation need to be compared with operating the drive for optimum process requirements.

The focus of testing will influence the definition of a disruptive region, the choice of parameters to enable and the choice of settings. It will also influence the choice of load and the type of dips that will be applied.

Whatever the focus of the testing, the purpose must be clearly conveyed, such as is presented below:

1. To characterise the susceptibility and trip levels of VSDs to voltage dips with and/or without VSD ride-through programming options enabled,
2. To characterise the susceptibility and trip levels of VSDs to voltage dips with and/or without VSD ride-through alternative devices, or
3. To characterise the susceptibility and trip levels of VSDs to voltage dips during process loading conditions for VSD-driven processes with specific speed and torque deviations requirements.

5.4 A Description of the Supply Specifications

The dip generator used for testing must be specified in detail. Whether this component is a complex waveform synthesiser or a series injection transformer feeding off a utility line, this should be defined and the waveform generation capability described as in the following example [6].

5.4.1 Specifications of the device(s) used to generate voltage dips

The following issues need to be addressed:

a) What type of dip generator will be used (power amplifier with arbitrary waveform generator, IBGT-switched autotransformers, synchronous generator with series injection transformer, etc.)? Provide a simplified diagram. If a waveform generator with power amplifier is used, characterise it by providing specifications such as sampling rates, software details, etc.

b) What is the switching time between nominal to dip voltage and dip voltage to nominal voltage? Is there any "dead time" during the switching?

c) Does the user have control over point of initiation and point of recovery of the dip? Does the dip generator allow control over initial phase-shift of the dip?

d) What are the characteristics of the voltage dip waveform? If the waveform is similar to the one in Figure 5.3, then define T1, T2, and T3. The duration of the dip shall be defined as $(T_1 + T_2 + T_3)$. If the waveform is similar to the one in Figure 5.4, then the dip will only be defined by the depth and duration. If single-phase, two-phase and/or three-phase dip tests will be performed, show a typical 5 cycle voltage dip waveform for each case, unless the investigation focuses only on field-recorded dip events reproduced with power amplifiers. In this case, show a typical field-recorded event used during the investigation.

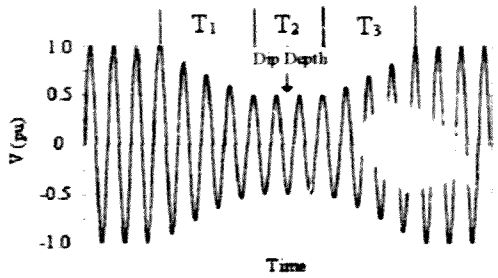


Figure 5.3 A voltage dip waveform, specifying rise and fall times [6]

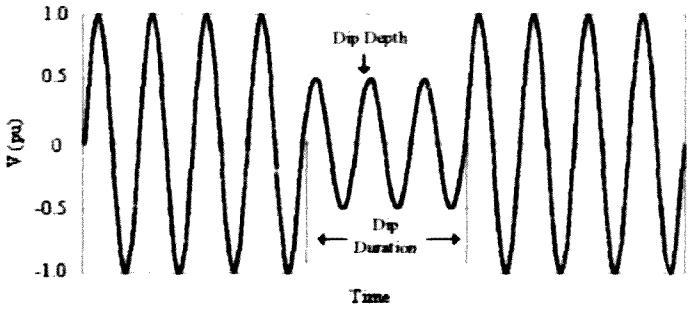


Figure 5.4 A voltage dip waveform, specifying only dip duration [6]

5.4.2 Specification of the voltage dips to be investigated

The IEC 61000-4-11 recommended voltage dip test levels and durations are listed in Table 5.2 (partially excerpted from Table 1 of IEC 61000-4-11). Other questions that can be answered are:

a) What type(s) of dip(s) (single-phase, two-phase, and/or three-phase dips)?
b) What magnitude(s) (in % of nominal) and duration(s) (in cycles) of dips?
c) How are the magnitudes of the voltage dips referenced (in % of line-to-neutral voltage or in % of line-to-line voltage)?
d) For drives with external control power transformers, will the control power be subjected to voltage dips? If not, how will the control power be supplied to the drive?

Data extracted from a UNIPEDE study [17] is shown in Table 5.3. This table is a guideline in IEC 61000-4-11, providing customers and manufacturers in Europe with adequate information related to voltage dips and short interruptions.
With reference to the European results, a well-accepted European UNIPEDE DISDIP method of reporting dips (Bin Analysis for Magnitude-Duration reporting) is documented in [18]. Utility companies provide statistics about power failures in the medium voltage (MV) area in terms of the depth and the duration of dips [17].

Table 5.2 Recommended VSD voltage dip test levels and durations [7]

Voltage Dips and Momentary Interruptions (in % of nominal)	**Duration (in cycles)**
0	½ 1
40	5 10
70	25 60 x
Notes: 1. One or more of the above test levels and durations may be chosen. 2. "x" is an open duration. This duration can be given in the product specification. 3. Any duration may apply to any test level.	

Partially excerpted from IEC 61000-4-11

Table 5.3 Average public utility disturbances per year in Europe [17]

DEPTH	**DURATION**			
(Voltage drop in % of nominal Ut)	10 to < 100 ms	100 to < 500 ms	500 ms to 1 sec	1 sec to < 3 sec
10% < 30%	61	66	12	6
30% < 60%	8	36	4	1
60% < 100%	2	17	3	2
100%	0	12	24	5
-	Number of disturbances per year			

According to these statistics, 97 percent of all power outages last not longer than 3 seconds (Figure 5.5). The reason for these outages are mainly atmospheric related short circuits in the respective or adjacent network, which are interrupted by switchgear. Reclosing follows after 0.3 to 3 s. Power failures with a longer

period of time happen due to a cable circuit, breaker or transformer fault and appear less frequently.

Table 3.4 together with Figure 3.18 in this document, as found in NRS 048-2:1996, will be relevant for South African conditions.

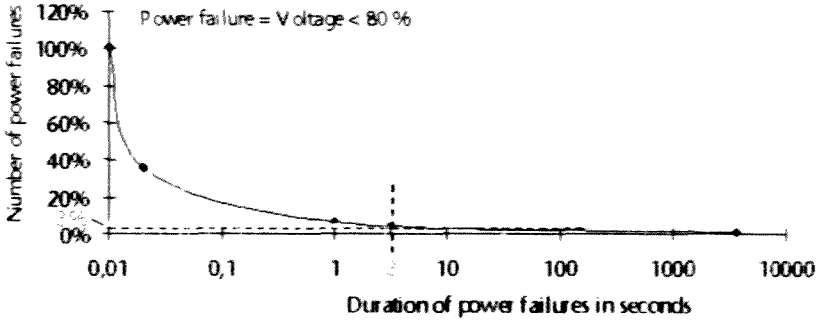


Figure 5.5 The duration of Power Failures in Europe [18]

5.4.3 Characterisation of the VSD source voltage

Measurements should be made to determine the nominal electrical conditions at the point where the VSDs will be connected to the power supply. The following measurements and calculations should be recorded.

a) Nominal Line-to-Line Voltage (V_{AB}, V_{BC}, & V_{CA})
b) Nominal Line-to-Neutral Voltage (V_{AN}, V_{BN}, & V_{CN}) (if applicable)
c) Percent Voltage Unbalance
d) Percent Over/Undervoltage
e) Percent Voltage THD
f) Short Circuit Capacity

5.5 Loading Conditions and Load Set-Up

Initial load-points need to be determined. The load attached to the motor also needs to be described. This load may be a simple dc-generator connected to a resistor bank under constant field or a complex programmable dynamometer.

5.5.1 Definition of all the load points used to load the VSD and motor during the investigation

This should include the following:

a) The steady-state speed (or VSD output frequency).
b) The steady-state torque (N-m or in-lb).
c) The steady-state power (hp or kW)
d) The load type (constant torque, constant horsepower, or variable torque).
e) The load inertia (kg-m^2).

5.5.2 Specifications of a dynamometer

If there is a dynamometer, its characteristics must be defined with calibration curves. Torque vs. Speed and Speed vs. Time calibration curves must be recorded for all load points tested to define the load type and load inertia of the dynamometer. The calibration curves must be defined over the speed range defined by the test objectives. An example is shown below that defines the Torque vs. Speed (Figure 5.6) and Speed vs. Time (Figure 5.7) characteristics for a dynamometer applying a quadratic variable torque load type.

a) Steady-state speed = 1750 rpm
b) Steady-state load torque = 20.5 N-m
c) Load type = Variable (Quadratic)
d) Load Inertia = 0.0496 kg-m^2

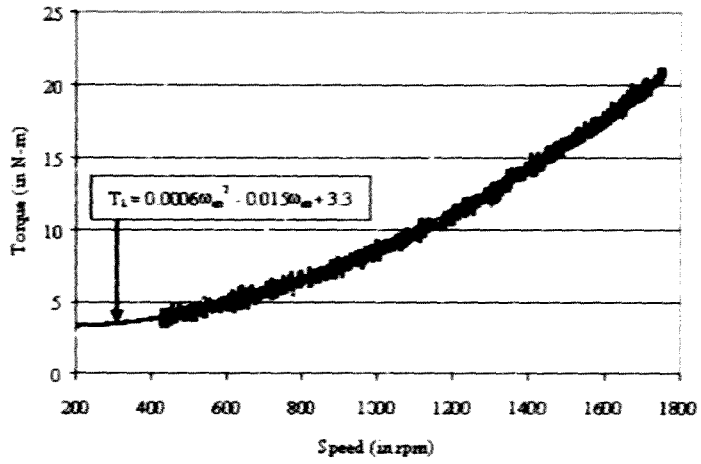


Figure 5.6 The Torque vs. Speed characteristic for a quadratic load type [6]

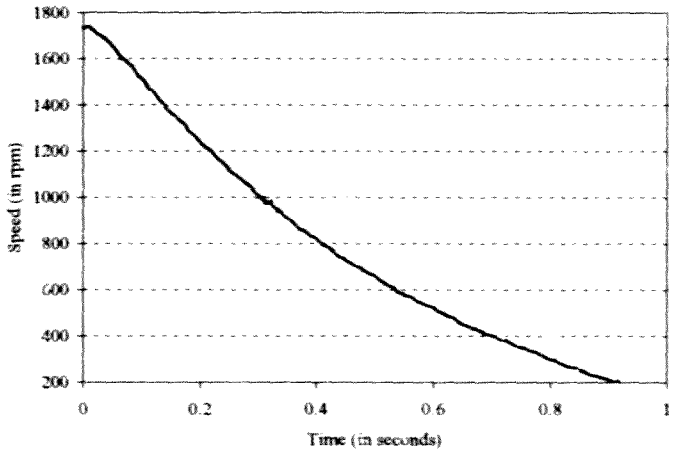


Figure 5.7 The Speed vs. Time characteristic for a quadratic load type [6]

5.6 A Description of the Monitoring System

The equipment used for the logging of waveform data needs to be specified under a description of the test set-up. Measurement equipment that forms part of the supply or load equipment should be specified under the sections describing the supply and load equipment.

The example shown below defines the specifications for the monitoring system, the speed sensor, and the torque sensor for the components listed in Figure 5.2. The example contains the recommended specifications for each component.

5.6.1 Torque sensor specifications

The torque sensor should meet the following specifications:

a) Maximum capacity of one and half times full-load torque (of the MUT)
b) Overload capacity of at least five times full-load torque (of the MUT),
c) Maximum operating speed of at least two times base speed (of the MUT),
d) Accuracy of at least ± 0.1% of full-scale,
e) Calibration Accuracy of at least ± 0.02% of full-scale,
f) Dual bi-directional outputs for clockwise and counter-clockwise torque, and
g) Output bandwidths of DC to 1 Hz and DC to 300 Hz.

5.6.2 Speed sensor specifications

A rotary encoder, tachometer or a frequency-to-voltage converter should be used to measure system speed. The devices should meet the following specifications:

Rotary encoder:

a) Resolution of at least 1024 PPR,

b) Frequency response of at least 120 kHz,

c) Rise and fall times less than 500 ns @ 10,000 pf, and

d) Maximum operational speed of at least two times base speed (of the MUT).

Frequency-to-voltage converter:

a) Frequency range of at least 0 Hz to one and half times required by the test*,

b) Accuracy of at least ± 0.05% of full-scale,

c) Step response no greater than 25 ms, and

d) Output ripple no greater than ± 0.2% at 20% of base speed (of the MUT).

* The frequency range is determined by the maximum speed required during evaluation. Thus, the upper limit for the frequency range is defined as the numbered pulses generated by the encoder per second at maximum application speed.

5.6.3 Voltage isolation probe specifications

Voltage isolation probes, used for measuring the VSD input voltages, VSD output voltages, or DC bus voltage, should meet the following specifications:

a) Voltage ratings that exceed the maximum input voltages of the test application,

b) Bandwidth of at least 100 kHz,

c) Accuracy of at least ± 1% of full-scale,

d) Common mode rejection of at least 70 dB for DC to 10 kHz, and

e) DC drift of less than 20 mV/°C.

Note: If the test requires measurements of the inverter output voltage, the voltage isolation probe specifications must meet or exceed the requirements of the measured signal.

5.6.4 Current transformer (CT) specifications

CTs used for measuring VSD output (motor) and/or input currents should meet the following specifications:

a) Current ratings that exceed the maximum currents of the test application. Special attention must be given to the post-inrush current of a drive. IEC 1000-4-11 provides a guideline to determine this limit. A recommendation is that the CT must be able to handle this current unless it is more than 500A.
b) Bandwidth of at least 100kHz,
c) Accuracy of at least ± 1% of full-scale.

5.5.5 The data acquisition system

The data acquisition system, used to capture data from the torque and speed sensors and the voltage and current isolation probes, should meet the following specifications:

a) Sufficient number of channels for capturing all required data,
b) Resolution of at least 12 bits,
c) Through-put of at least 300 kS/s per channel,
d) Simultaneous Sample and Hold (SSH) or burst mode sampling of channels, and
e) Accuracy of ± 1 LSB.

Note: If the test requires measurements of the inverter output voltage, the data acquisition system specifications must meet or exceed the requirements of the measured signal.

5.7 Drive Inspection Prior to Testing

All motor and drive specifications are recorded using the parameter checklist shown. Some of the data can be obtained by examining the exterior of the drive case or by consulting the drive's manual. Prior to conducting any test, the manufacturer should be asked to provide information relevant to testing success and analysis. Obtaining the drive operation and/or service manual should provide most of the required information. Table 5.4, 5.5 and 5.6 outline the parameters. Comments are given as to the usefulness of these parameters for the test output.

The information marked critical outlines the minimum requirements for testing and reporting of results. For example, the input voltage and current envelopes specified for a drive is critical to ensure safe operation. On the other hand, knowing the software version is useful for reporting, as long as the software parameters are specified in the operating manual of the drive. Another example is when matching a motor to the drive. Knowing the motor specifications for the drive is critical for safe operation, whereas knowing the operating temperature is useful for reporting, but not critical unless there is a departure from the standard test environment.

Table 5.4 Drive ratings

No.	Item	Critical	Useful
a	Manufacturer/Vendor, model number, and serial number	✓	
b	Firmware/Controller software edition		✓
c	Input voltage (1ϕ or 3ϕ, Volts, tolerance)	✓	
d	Input frequency (Hz)	✓	
e	Input current (A)	✓	
f	Input power (kVA and kW or hp)	✓	
g	Output voltage range (1ϕ or 3ϕ, Volts)	✓	
h	Output frequency range (Hz)	✓	
I	Output current (A)	✓	
j	Max and min motor size (hp and/or kW)	✓	
k	Enclosure (NEMA 1, NEMA 12, etc.)		✓
l	Operating temperature (°C)		✓

m	Operating altitude (m)		✓
n	Operating relative humidity (%)		✓
o	Cooling method/requirements		✓

Table 5.5 Motor Ratings

No.	Item	Critical	Useful
a	Manufacturer/Vendor, model number, and serial number		✓
b	Voltage (1ϕ or 3ϕ, Volts)	✓	
c	Frequency (Hz)	✓	
d	Current (A)	✓	
e	Power (kVA and kW or hp)	✓	
f	Service factor		✓
g	Nominal efficiency		✓
h	NEMA design		✓
I	Insulation class		✓
j	Frame		✓
k	Enclosure (TEFC, ODP, etc.)		✓
l	Operating temperature (°C)		✓
m	Operating altitude (m)		✓
n	Operating relative humidity (%)		✓
o	Cooling method/requirements		✓

Table 5.6 Information that may be relevant for the test

No.	Item	Critical	Useful
a	Drive wiring diagrams and grounding requirements		✓
b	General circuit diagram of the drive		✓
c	Drive control power (external transformer, internal transformer, internal switch-mode power supply)	✓	
d	Drive principle of operation	✓	

Other application information deemed pertinent by the drive manufacturer or the sponsor, can also be included (e.g. communication details, source of logic power, input line reactors, dc link reactor, active rectifier). An example of a drive circuit diagram is shown in Figure 5.8.

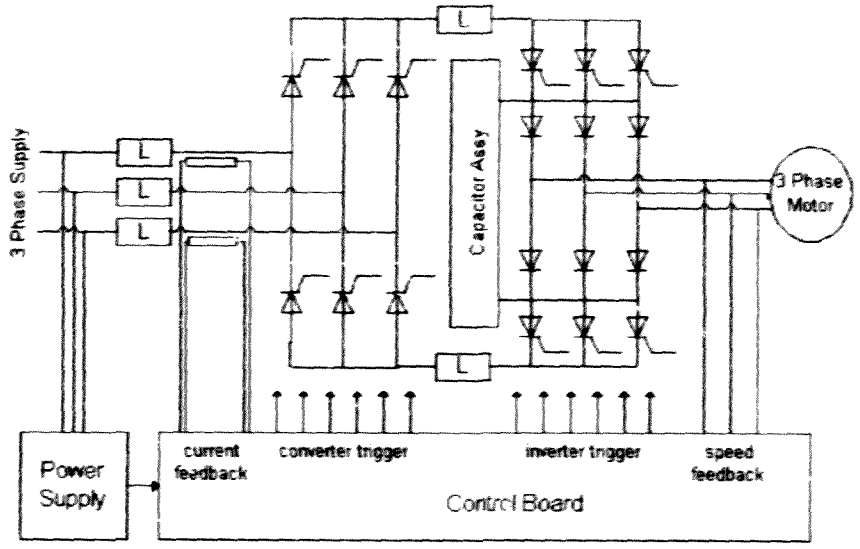


Figure 5.8 An example of a general circuit diagram of a CSI VSD [26]

5.8 The Installation and Operation of the Drives

The drive should be installed according to the instructions of its service manual. Usually the terminals of the drive are clearly marked. The parameter options for the user interface should be available in the operating manual.

5.9 The Evaluation of Selected Drive Parameters

Parameters deemed to be important to the outcome of the test should be noted as per section 5.3 and adjusted accordingly. For example, auto-restart options should be set to off unless there is a specific requirement to record the drive performance with restart enabled. Where these are enabled, proper discussions should follow in relation to criteria specified as per section 5.3.

5.10 Normal Operation of the Drive

The drive should be allowed to reach steady-state operating conditions before any dips are applied. This should be done initially for roughly 10 minutes to allow drive components to reach normal thermal operating conditions. If less time was allowed, this should be mentioned. When the drive has reached normal operation, 10 seconds running time may be allowed before executing the test dip.

5.11 The Testing Methodology

The following tasks need to be performed during testing.

Record the following information:

a) Voltage dip magnitude (% of nominal)
b) Voltage dip duration (in cycles or ms)
c) VSD fault codes.
d) VSD failures (fuses, diode bridge, SCRs etc.).

Use the monitoring system to record:

a) System speed vs. Time (with at least five cycles of pre-dip data and three seconds of post-dip data).*
b) Torque deviation vs. Time (with at least five cycles of pre-dip data and three seconds of post-dip data).*
c) Motor Current vs. Time (at least one phase with at least five cycles of pre-dip data and three seconds of post-dip data).*
d) DC Bus Voltage vs. Time (with at least five cycles of pre-dip data and three seconds of post-dip data).*
e) VSD Input Voltage vs. Time (with at least five cycles of pre-dip data and three seconds of post-dip data).*

* **Note**: Actual monitoring points will be defined by the purpose and objectives of the investigation. Choosing the items to record will also be determined by the drive under test. For example, recording the dc bus voltage is more relevant to a PWM drive than a CSI drive.

Each time before voltage dips are applied, the drive should be allowed to operate normally, as described in 5.10. If the voltage dips are applied within a short time of each other, it is not necessary to allow normal operation for as long as 10 minutes. In this case 10 seconds should do as mentioned. If at any time, there is a long period between tests, any of the other tasks, such as recording the load and supply parameters and running the drive under normal operating conditions must be repeated.

5.12 Presentation of the Results

Where the output product is a dip-compatibility report, the requirements for establishing inspection and test status must be included in the report. The test results must at least be represented as sensitivity plots that take cognisance of either

a) one of the magnitudes of the supply voltage during the dip, or
b) the duration of the event from the time that the event can be considered to be a dip to the time that the drive supply had recovered, or
c) both variables in a and b.

The magnitude of the supply voltage must take either the form of per unit voltage of the nominal supply or percentage voltage of the nominal supply. Duration shall take the form of number of cycles. This is preferred to milliseconds because 50 or 60 Hz conditions may apply.

Other desired variables and relationships shall be represented with the above variables noted in any dip sensitivity plot. The form that such sensitivity plots take, can vary and may be specified as CBEMA curves or NEMA curves, or to highlight specific relationships such as phase vs. duration plots.

Two suggested formats [6] are presented below:

a) CBEMA format – This format may be particularly useful for presenting results for investigations that attempt to characterise the susceptibility and trip levels during process loading conditions for VSD-driven processes with specific speed and torque deviations requirements. Figure 5.9 shows an example of a CBEMA plot that defines the acceptable speed deviations for voltage dips applied to a VSD. Information pertinent to the testing such as parameter options and supply and load information should be included with the plot. When using cycles for the x-axis, the fundamental frequency must be specified on the plot.

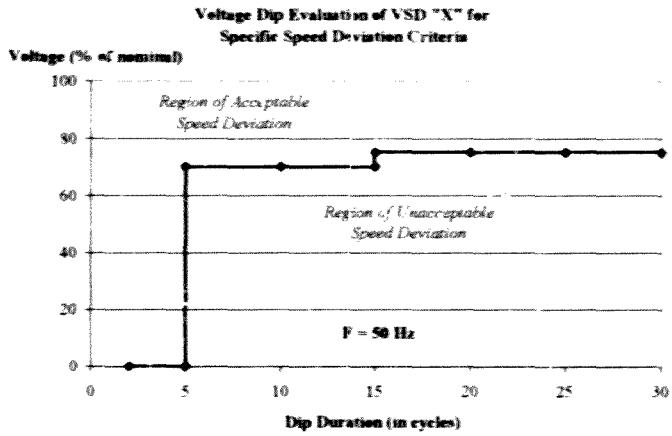


Figure 5.9 Voltage Dip Test Results: Example of the CBEMA format [6]

b) Monitored Data vs. Time plots – This format is a graphical representation of the measured data during the test (speed, torque, motor current, VSD input voltage, etc.). Figure 5.10 is an example of this format.

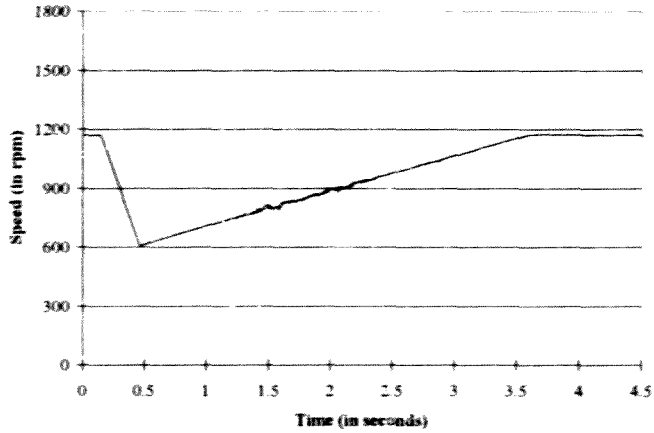


Figure 5.10 Voltage Dip Test Results: Example of the Monitored Data vs. Time format [6]

6 USING THE POWER QUALITY TEST FACILITY FOR DIP IMMUNITY TESTING

The Power Quality Test Facility (PQ Test Lab) at the University of the Witwatersrand has been designed with dip immunity testing in mind. The discussions in this chapter will discuss testing at this facility, starting with a description of the facility, test preparations and then describing the development of a test procedure.

6.1 A Description of the Voltage Dip Test-bed

The voltage dip test bed was developed around the requirements of variable speed drives. A more detailed description of the test-bed can be found in [21,24]. The voltage dip test-bed consists of:

- A controlling PC
- Input (A/D) and output (D/A) PC interface cards
- A programmable supply incorporating an IGBT output inverter stage, supplied via a three-phase rectifier.
- An output transformer
- The drive to be tested connected to a 3- phase squirrel-cage induction motor
- An induction motor mechanically coupled to a DC generator
- A variac/ rectifier to adjust the generator field
- A resistor bank to serve as the generator load

6.1.1 An overview of the facility

A PC is used to synthesise a voltage dip by specifying voltage dip parameters such as the voltage prior to the voltage dip, the voltage during the voltage dip, the phase angle and the voltage recovery profile. Parameters can be adjusted independently for each of the phases such that single-phase, line-line and three-phase voltage dips can be tested.

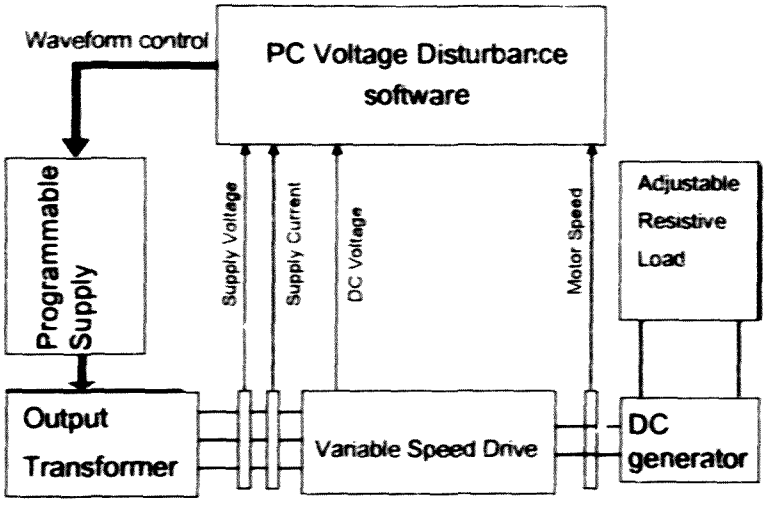


Figure 6.1 Block diagram of the voltage dip test-bed [24]

The test facility, shown in figure 6.1, consists of the following elements:

- The PC, running the dip testing software, is used to control the testing. The voltage dip software controls the pre-dip waveform generation and voltage dip generation by the programmable supply. During and immediately after an applied voltage dip, VSD measurements are recorded for analysis after the test.
- The programmable supply replaces the mains supply to the equipment. The programmable supply is IGBT based and, with the controller that was developed, is capable of generating any complex voltage dip waveform.
- The VSI or CSI inverter is connected to a standard induction motor, which in turn is coupled to a DC generator load.
- The DC generator, which is coupled to the induction motor, is connected to a resistive load bank. By adjusting the generator field current the load presented by the DC generator is varied. With constant field and resistive load the DC generator load presents a linear torque versus speed characteristic.

Future modifications to the dip-testing facility include:

- A programmable load that can simulate different load types.
- Fully automated dip testing.
- Miscellaneous improvements to the programmable supply.

6.1.2 An overview of the monitoring system

The three-phase disturbance waveform is generated via a digital to analogue converter (DAC) on a digital to analogue interface card. The measurements from the drive are done with isolation probes, current transformers and a tachometer for voltages, currents and the speed respectively. The measurements are logged via an analogue to digital converter (ADC) on an analogue to digital acquisition card.

Measurement requirements for variable speed drives:

The following parameters were identified as being important to monitor in order to comprehensively describe the dip immunity performance of a drive:

- Drive DC bus voltage
- Drive input currents
- Drive input voltages
- Drive output currents
- Drive output voltages
- Motor speed

Minimum analogue interface cards specification:

The specifications for the cards were drawn up according to the following:

a) Resolution

   It was required that all the converters are minimum 12-bit converters.

b) Number of interface channels required

   A minimum of three analogue outputs was required in order to generate a three-phase disturbance waveform. A minimum of five analogue inputs log DC voltage, motor speed and one set of three phase measurements.

c) Sampling rate

   For the output card, a minimum sampling rate of 4 KHz was chosen corresponding to the switching speed of the programmable supply. The sampling rate of the input cards is much higher (5 kHz) than that necessary for a normal 50 Hz waveform. This is because transient behaviour is analysed during and immediately after the voltage disturbance.

d) Timing

In order to generate accurate high-speed output waveforms, it is important to have timing functions available. It is possible to use the PC to generate timing for slow waveform generation, but for high- speed waveforms a dedicated timing system is preferable, ensuring that samples are output at exactly the right time. When logging input waveforms, a timing system becomes even more critical, particularly with high-speed acquisition (>50 KHz) when sampling multiple input channels. If direct memory access (DMA) is used to transfer converted data from the card directly into memory, the card operates independently of the processor and is thus not timed by the processor.

e) Software drivers available

To use the A/D and D/A cards effectively without understanding the low-level design of the card, software drivers are required. The drivers are accessed from the program and perform card configuration, analogue input and output, timing and utilise complicated card features such as DMA, required for high throughput sampling rates. All code to write to registers on the card, verify settings etc. is encapsulated within the driver such that only high-level knowledge of the card is required to use it. For instance, when using DMA, the software driver sets up the DMA channel and transfers samples directly to memory. All the user of the driver does is to call the high level DMA function.

Output card (D/A) specifications:

The output card has 8 12-bit output channels. A very high sampling rate (>100 KHz) depends on the speed of the computer in which the card is installed. The card has a dedicated timing system, based on a 2 MHz reference crystal and a counter. Data transfer to the board is 16 bit to speed up data throughput.

Output waveform generation can be done using polled I/O, in which the processor continuously monitors the card and sends new data values to the card when the DACs are updated, or interrupts, in which the card signals the processor when the DACs are updated. Only polled I/O is directly supported so that if interrupt driven waveform generation is required (for background waveform generation) code to perform this must be written. This necessitates a deeper level of understanding of the card.

Input card (A/D) specifications:

The input card has 16 single ended/ 8 differential input channels. The card is used in differential mode so 8 input channels are available. Maximum board throughput is 100 KHz, which the number of channels used multiplied by the per-channel sampling rate cannot exceed.

Acquisition can be done using polled I/O, interrupts and DMA. DMA support for data acquisition enables sampled data of unlimited length to be written directly to memory with minimal CPU intervention. The number of samples stored is limited only by the available memory

6.1.3 An overview of the voltage disturbance software

The software performs two functions: *synthesis* and *generation*.

Dip synthesis software:

The parameters categorising the disturbance waveform are drawn up in the synthesis software. From these parameters an actual waveform can be generated. It is possible to save these parameters to a file so that they can be used at a later stage to generate the output waveform. This task is not real-time, so it is possible to develop disturbance waveform parameters at a remote PC without affecting the testing. Note that because the disturbance waveform is categorised as a set of parameters, these parameters are saved to file creating much smaller files than if an actual disturbance waveform values were generated and saved to file. A screenshot from the synthesis module is shown in Figure 6.2.

Dip generation software:

This software generates the output voltage disturbance waveform while simultaneously logging test measurements. The voltage disturbance waveform to be generated is calculated by using the parameters from the synthesis module to generate the actual output waveform samples. During waveform generation, these values are output via the digital to analogue card. Testing system measurements are input via an A/D card and the sampled values are stored in memory. A screenshot from the generation module is shown in Figure 6.3.

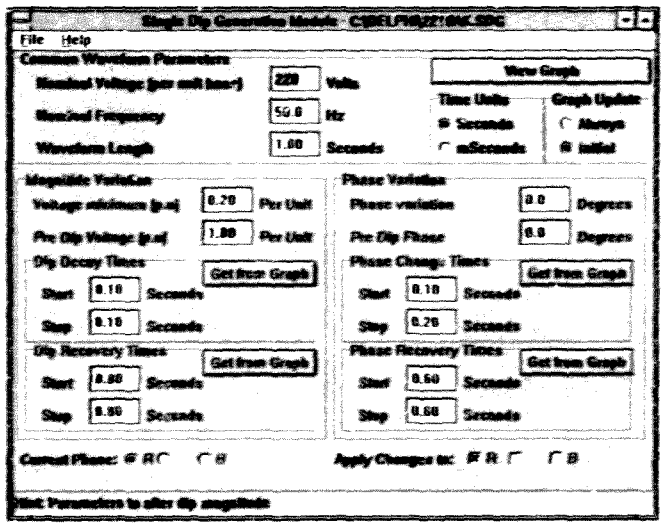


Figure 6.2 A screen shot of the main synthesis module form

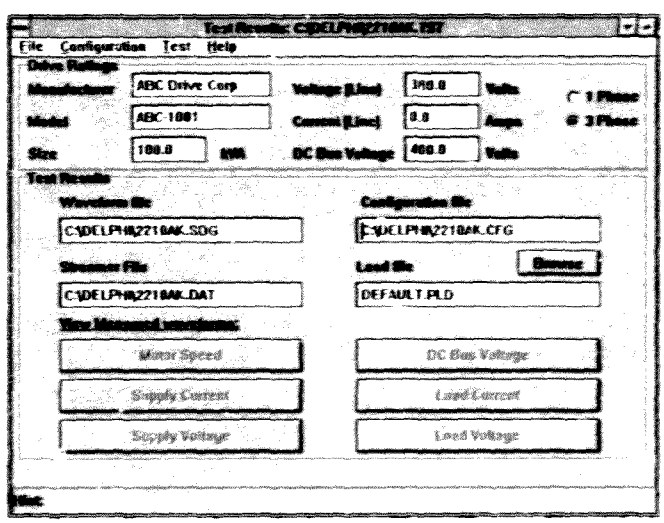


Figure 6.3 Screen shot of the generation module form

6.1.4 The voltage synthesis parameters

To synthesise the voltage dip, both magnitude and phase parameters must be adjustable for each phase. The parameters are as follows:

Magnitude parameters:

- Pre dip voltage: The magnitude of the voltage waveform before the dip occurs. This is specified in per unit taking the nominal voltage as the base voltage.
- Dip voltage: The magnitude of the voltage waveform during the dip. This is specified in per unit taking the nominal voltage as the base voltage.
- Dip decay time: The time taken for the voltage at a particular point to decay to the dip voltage. The time taken for this decay is usually very short, but can be increased by motors connected to the supply acting as generators, supporting the network voltage. For each phase this is specified by a start and end time, and the voltage decays with a negative exponential envelope during this time.
- Dip recovery time: The time taken for the voltage to recover back to the pre-dip voltage. After the dip, the voltage magnitude does not recover immediately because of motors drawing large currents when the fault is cleared. For each phase this is specified by a start and end time and the voltage recovers with a first order response during this time.
- Dip duration: This is the time for which the voltage magnitude remains below 90% of the declared voltage. This parameter is not specified directly, but can be calculated from the dip decay and recovery times.

Phase variation parameters:

- Pre dip phase shift: This is the amount by which the respective phase is shifted from the nominal (120 degrees) before the dip occurs, specified in degrees.
- Dip phase shift: This is the amount by which the respective phase shifts from the nominal during a dip.
- Phase change time: This is the time taken for the phase shift to vary from the pre dip phase shift to the dip phase shift. This is specified by a start and stop time for each phase during which the phase varies linearly.
- Phase recovery time: This is the time taken to recover from the dip phase shift to the pre dip phase shift. This is specified by a start and stop time for each phase and variation is linear.

The use of a pre dip magnitude and phase shift for each phase allows the system to generate more general dip waveforms. Because parameters can be adjusted individually for each phase, voltage unbalance, overvoltages and undervoltages can be generated thereby increasing the testing ability of the system. The pre dip parameters are important because the operating conditions that are present before the dip occurs can compound the effect of the voltage dip on the drive.

Screenshots of waveform previews in the synthesis module are shown in Figure 6.4. Screenshots of measured waveforms are shown in Figure 6.5.

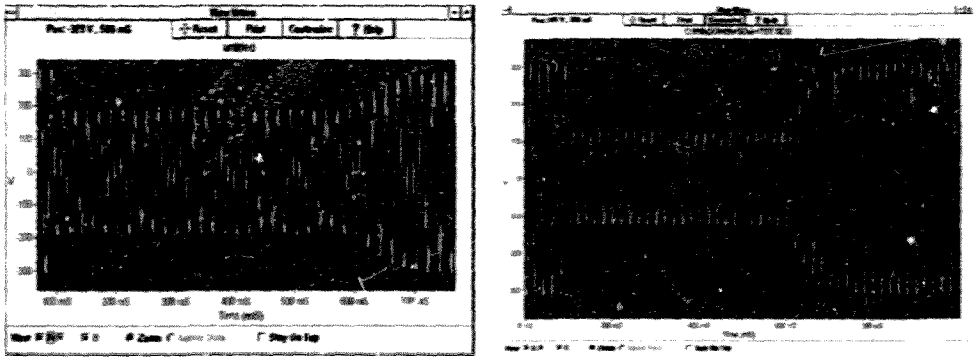


Figure 6.4 (a) and (b) Screen shot of preview waveforms in the synthesis module. A three-phase dip and a phase-phase dip are represented.

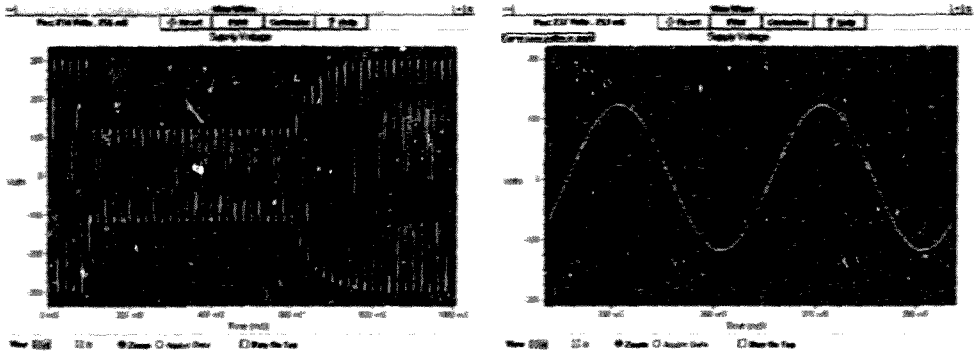


Figure 6.5 (a) and (b) Screen shot of measured waveforms in the generation module. The zooming capability is illustrated in (b).

6.2 Preparations Before Testing

Before testing can start, essential information needs to be recorded, the VSD needs to be installed and the motor matched to the VSD. Furthermore coding has to be established to conceal the identity of the drive manufacturers.

6.2.1 Recording the product specifications

Prior to conducting any test, the manufacturer should be asked to provide the following information. The information per example in Table 6.1, 6.2 and 6.3 is for three PWM drives from US manufacturers

VSD ratings:

Table 6.1 The information contained in this table can be obtained from the drive instruction manual and the exterior of the drive enclosure. Note that the drive names and models have been concealed and coded.

Item	Description	Drive PWM-1A005	Drive PWM-1B005	Drive PWM-1C005
a.	Manufacturer/Vendor	CONCEALED	CONCEALED	CONCEALED
	Model number/ Type	CONCEALED	CONCEALED	CONCEALED
	Serial number/ File No.	8X2736R0006	NSP0761-001-44/ E153436	8471483
b.	Firmware/Controller software edition	N/A	N/A	N/A
c.	Input voltage (1ϕ or 3ϕ, Volts, tolerance)	380-480V	380-480V	440-500V
d.	Input frequency (Hz)	50/60Hz	50/60Hz	50/60Hz
e.	Input current (A)	14.9A	10.2A	8.0/11.0A
f.	Input power (kVA)	N/A	5HP	5.0HP Constant Torque 7.5HP Variable Torque
g.	Output voltage range (1ϕ or 3ϕ, Volts)	380-460V	0-460V	0-Vin
h.	Output frequency range (Hz)	2-400Hz	0-400Hz	0-500Hz
i.	Output current (A)	9A (150%/1min)	8.5A	8.0/11.0A

j.	Output power (kVA)	6.8kVA	5HP	-
k.	Max and min motor size (hp and/or kW)	-	-	-
l.	Enclosure (NEMA 1, NEMA 12, etc.)	-	-	COMPACT NEMA1 (1P20)
m.	Operating temperature (°C)	-	-	50C Ambient
n.	Operating altitude (m)	-	-	-
o.	Operating relative humidity (%)	-	-	-
p.	Cooling method/requirements	-	-	Airflow 42 CFM
q.	Weight (kg)	-	4.5kg	15.4lbs

VSD circuit diagram:

Circuit diagrams can be obtained from the instruction manual of the drive or directly from the manufacturer. The principal method of operation of the drive needs to be included with this information. A typical circuit diagram is given in Figure 6.6.

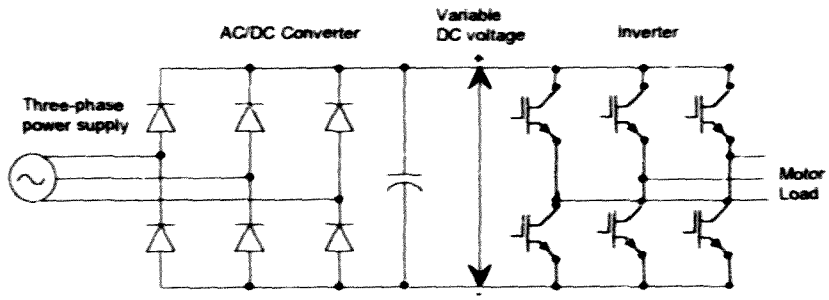


Figure 6.6 A typical PWM variable speed drive circuit diagram

Motor ratings:

Table 6.2 The information contained in this table can be obtained from the motor instruction manual and the motor nameplate.

Item	Description	Motor 1T005
a.	Manufacturer/Vendor	ALSTOM Electrical Machines South Africa
	Model No./Type	CS4130-44B1AAAA
	Serial No.	0446850/06/VI
b.	Voltage (1ϕ or 3ϕ, Volts)	3ϕ 525V
	Connection (delta/ wye)	Delta
c.	Frequency (Hz)	50Hz
d.	Current (A)	N/A
e.	Power (hp/kW)	5.5kW
	Speed (rpm)	1445rpm
f.	Service factor	N/A
g.	Nominal efficiency	N/A
	Power factor	0.91
	Duty Cycle	S1
h	NEMA/SABS/?? Design	SABS 948
i.	Insulation class	F
	Protection	IP55
j.	Frame/ Mount	132S/ IM:B3
k.	Enclosure (TEFC, ODP, etc.)	N/A
l.	Operating temperature (°C)	N/A
m.	Operating altitude (m)	N/A
n.	Operating relative humidity (%)	N/A
o.	Cooling method/requirements	1C-411
p.	Lubricant/ Grease	SHELL ALVANIA G3
q.	Bearings	DE/NDE 6208-Z-C3
r.	Mass (kg)	65

Software parameters:

A scan was done of the software parameters in the manuals of each drive. The relevant parameters are shown in Table 6.3.

Table 6.3 The information contained in this table can be obtained from the drive instruction manual. Ticks indicate the existence of an item.

Item	Description	Drive PWM-1A005	Drive PWM-1B005	Drive PWM-1C005
	Manufacturer/Vendor	CONCEALED	CONCEALED	CONCEALED
a.	Overcurrent general/ at speed	✓ errorcode OC3 (level not stated)	✓ errorcode OC (125% of rated current)	✓ errorcode O/C (4xnominal current)
	Overcurrent on acceleration	✓ errorcode OC1	-	-
	Overcurrent on deceleration	✓ errorcode OC2	-	-
b.	Overvoltage general/ at speed	✓ errorcode OU3 (+/-800Vdc)	✓ errorcode OV (+/-800Vdc)	✓ errorcode O/V (Nominal + 35%)
	Overvoltage on acceleration	✓ errorcode OU1	-	-
	Overvoltage on deceleration	✓ errorcode OU2	-	-
c.	DC bus undervoltage	✓ LU (50% of nominal)	✓ errorcode UV1 (350Vdc +/-76.1% of nominal)	✓ errorcode U/V (65% of nominal)
d.	Ramp (Auto) restart	✓	✓	✓
e.	Flying (Auto) restart	✓	✓	✓
f.	Undervoltage controller	-	-	✓
g.	Overvoltage controller	-	-	✓

6.2.2 Recording the test environment

The following tests conditions are based on the ANSI/IEEE standards 100-1988, 112-1984, and C62.41 and 45.

Table 6.4 The information contained in this table can be obtained from the drive instruction manual.

Item	Description	Actual Conditions	ANSI/IEEE standards 100-1988, 112-1984, and C62.41 and 45. Recommendations
1	Temperature and relative humidity	± 26° and <85% humidity	25 ± 5°C and < 85% humidity
2	Altitude	± 1500m	< 2000 m
3	VSD Input Voltage	Sinusoidal waveform with THD <1%	sinusoidal waveform with THD < 1%
4	VSD Input Frequency	50 Hz	50 or 60 Hz ± 0.5%

6.3. Developing The Testing Procedure

The purpose, criteria, etc. are formatted as per chapter 5. Here the development of the testing procedure will be discussed. A PWM drive is used for illustration purposes. Example test instructions are:

- Vary the dip duration from 20ms to 600ms, i.e. 1 to 30 cycles while continually increasing the magnitude of the voltage dip.
- Evaluate the dip immunity under 25% and 75% full load conditions of the drive under test.
- Disable the drive dip ride-through aids, such as special controllers and auto-restart or flying-restart options.

The drive under test is not tested in the context of its role in a specific process, but with reference to a standard load type. A trip is recorded when there is a complete shutdown of the drive. However the specific reason for a trip can be due to undervoltage, Overvoltage, undercurrent or overcurrent conditions. This can be determined per drive fault code information. Although an undervoltage trip condition is preferred when compiling trip information, any other form of drive trip will be recorded and noted.

The dip types that were tested for, were:

- Phase-Phase voltage dip ride-through for up to 30 cycles
- Three-Phase voltage dip ride-through for up to 30 cycles

The following parameters are monitored to evaluate the performance of a drive.

- Motor Speed vs. Time (with at least five cycles of pre-dip data)
- Drive Current vs. Time (at least one phase; at least five cycles pre-dip data)
- DC Bus Voltage vs. Time (with at least five cycles of pre-dip data)
- Drive Input Voltage vs. Time (with at least five cycles of pre-dip data)

Measured parameters vs. time plots contain massive amounts of data and are stored for later retrieval. Finally residual voltage vs. dip duration plots (dip immunity plots) can be presented for all test variations and for all comparisons. The results of testing done as part of the test program are shown in APPENDIX C.

6.3.1 An overview of the testing procedure

Once the voltage dip waveform has been synthesised, actual testing is commenced. To perform dip testing on VSDs, the VSD is made to run under normal operating conditions- as if it were connected to normal mains supply - by supplying the pre-dip dip waveform. When the VSD is running normally, the synthesised voltage dip is applied to the equipment. During the test the PC records various equipment parameters. These parameters are then analysed to determine the VSD performance during a voltage dip.

The testing requires that:

- The motor/drive is brought up to speed with the simulated load type
- The input parameters are defined for a range of tests, for example:
  -Increasing 3-phase voltage dip depth
  -Increasing 3-phase voltage dip duration
- The dip generator is armed with these parameters and triggered
- The response waveforms are digitised and stored for later analysis.
- The motor load type is changed on-line and measurements repeated
- The drive is stopped (if it has not tripped) and the measurements analysed

A test sample of eight scenarios is shown (Table 6.5) for the drive.

Table 6.5 Testing schedule for dip immunity testing

Case No.	Dip type	Load Size	Pre-dip voltage
Case 1 and 5	Three-phase dip	75% and 25% load	1.0, p.u.
Case 2 and 6	Red-white dip	75% and 25% load	1.0, p.u.
Case 3 and 7	White-blue dip	75% and 25% load	1.0, p.u.
Case 4 and 8	Red-blue dip	75% and 25% load	1.0, p.u.

The drive was adjusted to supply a 50Hz output frequency so that the induction motor ran at its rated speed. 75% and 25% load was achieved by varying the generator field. Supply voltage, supply current, DC bus voltage and motor speed were measured. LEM current probes were used for the current measurements and LEM voltage isolation probes for the voltage measurements.

6.3.2 Step-by-step methodology

The dip synthesis module of the software was used to set up synthesis files for each case required, e.g. case 1: three phase, 1.0 pre-dip voltage, which was then loaded into the dip generator module. First the pre-dip waveform was generated and the drive allowed to attain normal operating conditions (10 minutes initially and 10 seconds between each subsequent test). The DC generator load was adjusted to 75% or 25% of rated load, respectively. When the drive had achieved normal running conditions, the test was initiated. Two seconds of measurements were recorded for each voltage dip applied to the drive.

For each of the above cases described above the dip duration was varied from 20 milliseconds (1 cycle) to 600 milliseconds (30 cycles). This was as set out in the test instructions. After a dip duration was decided on, the dip voltage was varied until the dip voltage at which the drive just rides through was established. Voltage depth was changed in steps of 0.05 p.u. The drive was always initially tested with a 20millisecond dip and then steadily increased from 40 milliseconds up to 600milliseconds. A flow diagram of the test procedure is shown in Figure 6.6.

Most important, during testing, is to determine the drive behaviour during a dip-event. It also has to be recorded why the drive tripped, e.g. on overcurrent or undervoltage, etc.

The following is observed for the example drive:

ED indicators:
<V (undervoltage), >I (overcurrent)

Speed indicators:

S1 - Hardly audible; no change in the speed plot
S2 - Slow down and smooth recovery (no restart)
S3 - Audible oscillation
S4 - Slow down with sharp recovery (restart)
S5 - Slow down to zero speed (full trip)

Current indicators.

C1 - No visible change in current waveform

C2 - Visible overcurrent after dip (no trip)

C3 - Visible oscillation on current waveform

C4 - Low current after dip until restart

C5 - Continued zero current (full trip)

The indicators are general, applicable to most test situations. A selection should be made for a specific test. For example, for these tests, all restart functions have been disabled, so restart indicators do not apply. An example of a test sheet is shown in APPENDIX B.

Each test point is prepared as a parameter file in the dip synthesis module and tested individually. The curve for each different case can take as little as 15 minutes to complete if all the correct points were initially found, or longer than an hour if the testing does not produce consistent results. The dip settings for each point ridden through, is recorded to form a curve.

A more complete schedule is considered for future tests. This schedule can be found in APPENDIX A. An extract from the test schedule is shown in Table 6.6. The dip type indicated in the table is as per table 3.6 in section 3.5.

Table 6.6 An extract from a drive test schedule showing Type 1 dips, 1.0 p.u. pre-dip voltage, 100% resistive loading.

No.	*Directory*	*Phases involved*	*Pre-dip (pu)*	*Load (%)*	*Load Type*	*Dip type*	*Phase angle*	*Done (tick)*
1		three phase	1.00	100%	Resistive	Type 1	0	
2		Red phase	1.00	100%	Resistive	Type 1	0	
3		white phase	1.00	100%	Resistive	Type 1	0	
4		blue phase	1.00	100%	Resistive	Type 1	0	
5		Red-white	1.00	100%	Resistive	Type 1	0	
6		white-blue	1.00	100%	Resistive	Type 1	0	
7		Red-blue	1.00	100%	Resistive	Type 1	0	

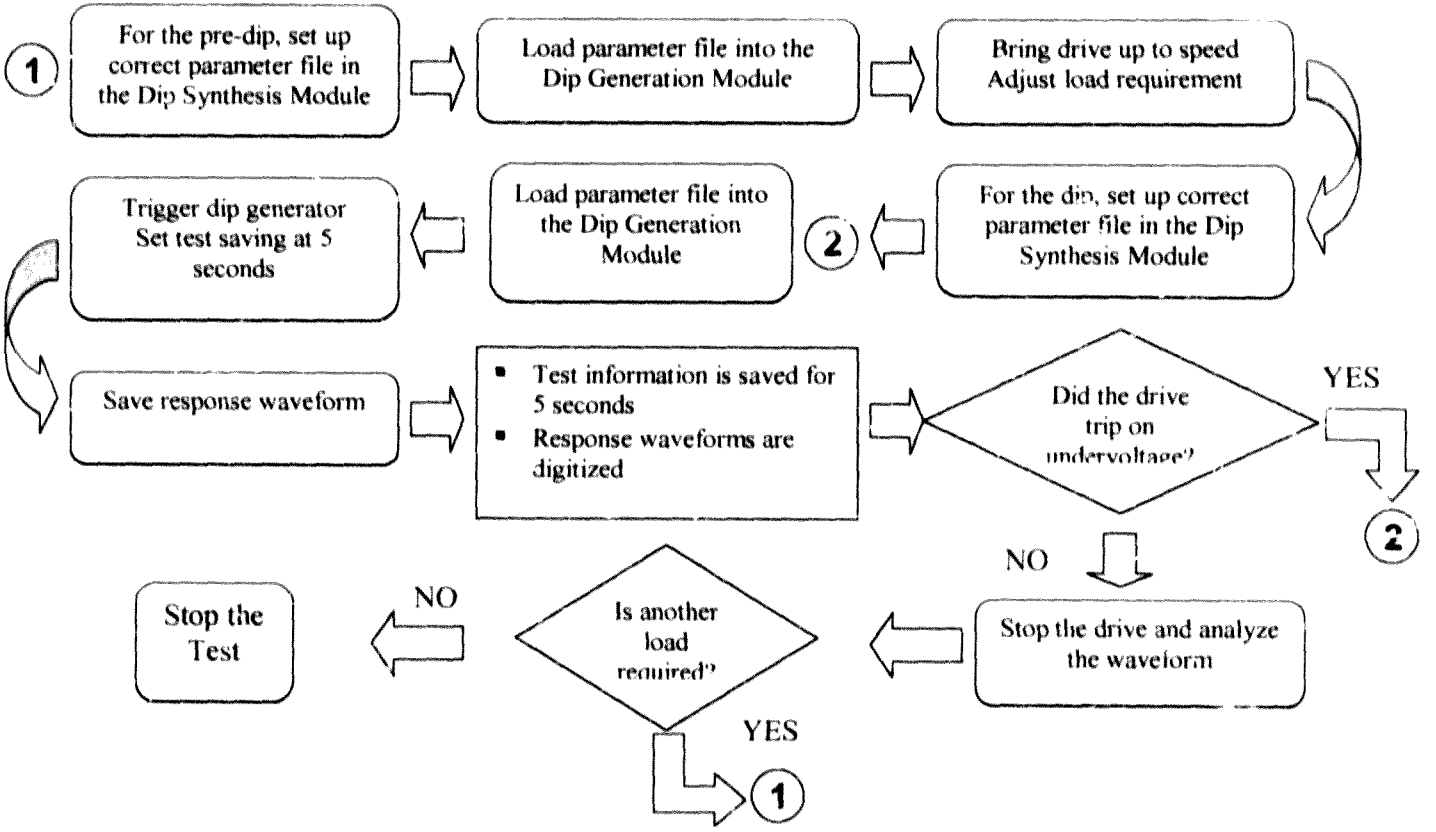


Figure 6.7 Block diagram of the voltage dip testing procedure

The test procedure can be summarised (with reference to Figure 6.7) as:

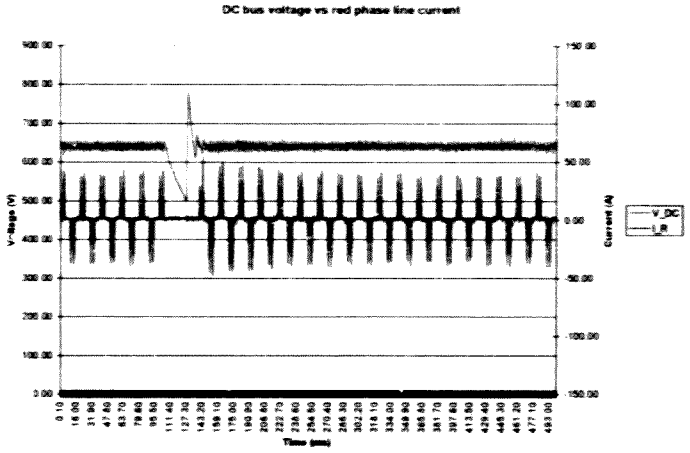
- The correct parameter file is set up in the dip synthesis module and loaded into the dip generation module.
- The drive is brought up to speed and the load adjusted to meet a 25% or 75% load requirement (for example).
- The dip generator is then triggered, saving the test information for the duration of the test and immediately following the test.
- The response waveforms are digitised and stored for later analysis.
- The process is repeated for each dip tested.
- If a different load is required, this is changed on-line and measurements repeated.
- The drive is stopped (if it had not tripped per the trip criteria) and the measurements analysed

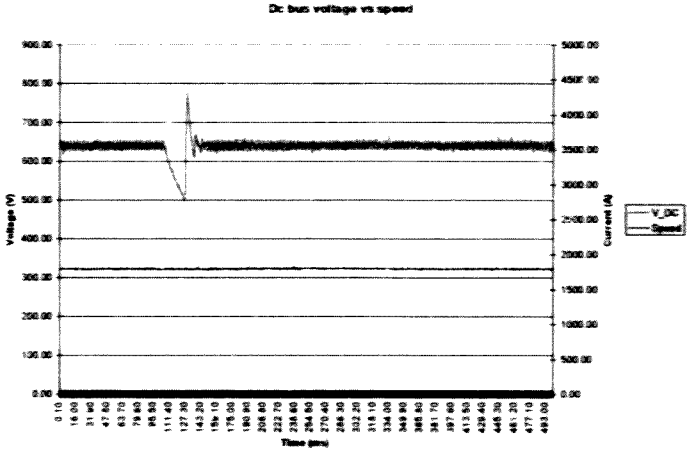
6.3.3 Evaluating performance from parameter plots

The performance of the drives can be evaluated by looking at the measured parameters such as the motor speed or the DC bus voltage plotted against time. To evaluate drive performance using these plots, there must be a clear differentiation between ride-though and trips. Drive ride though and drive tripping for the example, is illustrated. The special behaviour when a ride-through drive software parameter was enabled is also shown. In this case, an undervoltage/ overvoltage controller function, was enabled

a) When the drive rides through

At the point where the dip occurs, the current goes down to zero, and recovers to slightly higher levels right after the dip. However, during the test it was noted that this current could overshoot the pre-dip level, to the point where an overcurrent condition occurs. The dc bus voltage recovers to the pre-dip level.





Speed curves are hardly affected during a complete ride-through. However, the speed curve provides most of the information to determine the drive's performance. The speed may go down to 75% of the rated speed for 100 or 200 ms, which may be sufficient for a specific process to continue.

The short dip recovery profiles for the voltage dips tested suggested that a high output current was drawn by the motor from the drive during recovery stage of the voltage dip. If the recovery time is increased, as is often the case in practice due to, for example, induction motors re-accelerating and increasing the recovery time, the drive would be less likely to trip on overcurrent.

If there is a current spike just after the dip, it could be the result of immediate charging of the capacitors through the rectifier when the supply voltage recovers after the voltage dip (see figure 6.8). When the dip occurs, the peak supply voltage drops lower than that of the capacitor voltage and the supply current drops to zero (rectifier diodes reverse biased), explaining the zero current zone on the curves.

During the voltage dip, the capacitor voltage falls because the inverter section still runs, discharging the DC bus capacitors by drawing current from the DC bus. When the capacitor voltage drops below the peak input voltage, current is again drawn from the supply. As the supply recovers after the voltage dip, the capacitor is then immediately charged with a large current (rectifier diodes forward biased) limited only by the supply impedance and capacitor internal resistance.

When the drive is initially switched on, a current limiting resistor is in the circuit to charge the DC bus capacitors slowly and hence no current spike occurs. A timer circuit shorts this resistor out a set time after the supply has been turned on. During a voltage dip if the inrush resistor remains short-circuited because the timer circuit is not reset, a current spike will occur when the voltage recovers after the dip.

In practice, a longer recovery time after a voltage dip implies the capacitors would charge over a longer time period with less of a current spike (charge transferred over a longer time period).

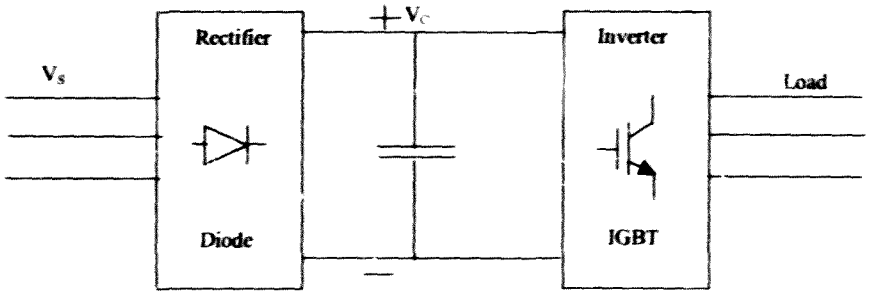
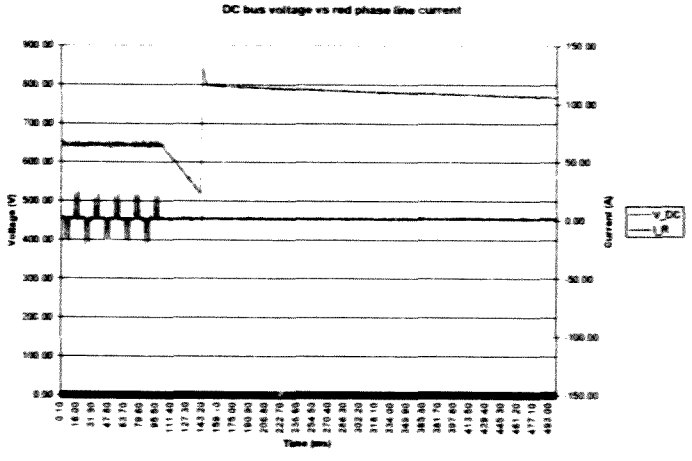
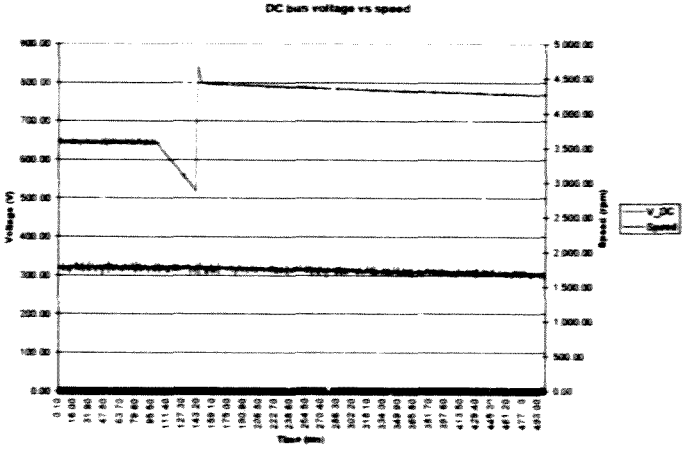


Figure 6.8 A simple schematic of the DC-bus of a voltage-source inverter drive

b) When the drive trips



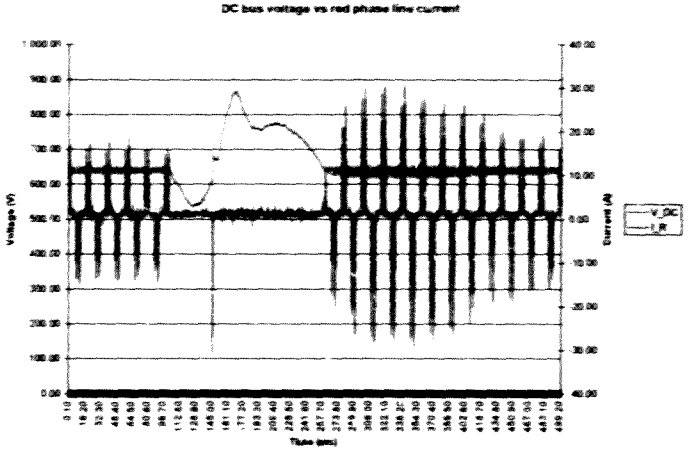
At the point where the dip occurs, the AC input current goes down to zero, and stays zero. The DC bus voltage rises to levels above the pre-dip level to reflect that it has shed the motor load of the motor. During the test it was noted that this post-dip level of DC bus voltage could reach the point where an overvoltage trip can occur.



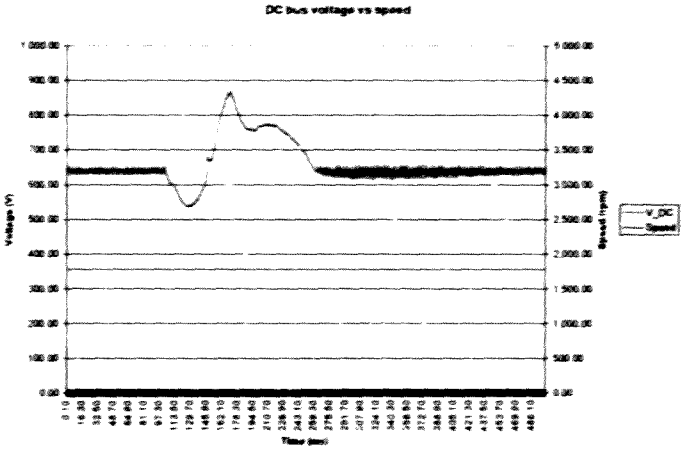
The speed drops down to zero during and after the dip. If the speed recovers it may mean that the drive still has control of the motor, or it may indicate a type of auto-restart.

c) Special behaviour with an under/overvoltage controller

An optional undervoltage and overvoltage controller ride-through function was enabled to determine its effect on the drive behaviour. It was later disabled because it altered the dip immunity region of the drive, often tripping on overvoltage as opposed to undervoltage conditions.



The DC bus voltage and current waveforms are greatly altered to keep the speed absolutely unchanged. This particular example is for a 40 ms duration dip. During the test, longer dips resulted in oscillations of the DC bus voltage.



The speed of the drive remained unchanged, while the other parameters (in this case the DC bus voltage) are adjusted continually.

7 THE IMPACT OF TEST RESULTS ON THE TEST PROCEDURE

The Voltage Dip Testing Program has been producing test results since 1998. The drives tested so far include:

- A 15kW PWM from a local manufacturer in 1998
- A 120kW CSI drive from a local manufacturer, which was sponsored by a local mine in 1999
- A 15kW Digital DC drive from a British manufacturer in 2000

During this time the testing methodology has been refined to optimise the number of tests and a test schedule similar to the one in chapter 6 is currently used. The latest test schedule can be found in APPENDIX A. The latest test sheet, in which the test data is recorded, can be found in APPENDIX B. Test results from the testing program is given in APPENDIX C. The optimisation of the number of tests is important to improve the economic viability of the test laboratory. The impact of the results is different for PWM, CSI and DC drives.

In 1999, three US-manufactured drives were sent to South Africa by EPRI-PEAC for testing under 50Hz conditions. The idea was to compare these results with those of the PEAC 60Hz testing program. The tests were completed and the comparison is under way.

The results of testing from 1998 to 2000 are presented in APPENDIX C for PWM drives, the CSI drive and the DC drive as dip sensitivity plots as described in chapter 5. Measured waveforms for some individual test-runs can be found in APPENDIX D.

7.1 AC Bus Sensing Vs. DC Bus Sensing

When testing drives, a first goal is to establish whether the sensing for DC bus undervoltage is done on the AC input side or on the DC bus itself. This can be determined from whether a drive provides balanced results for dips on each of its input phases. This is called a "Balance Routine". This is applicable to PWM and DC drives only. For example, if a PWM drive is found to have undervoltage detection on the DC bus itself, its behaviour could be the same for single-phase dips on any one of its three input phases. It would therefore be more efficient to test with say, only a dip in the red phase.

Usually, if the drive's control circuitry derives its power from the incoming AC line, it uses two of the input phases, e.g. blue and white phases on the AC side through a transformer. Such a drive would survive a single-phase dip down to 0% of nominal voltage on the red phase. In this case, the red phase will be called a "dead" phase. Continued testing on the red phase will therefore be unnecessary. An example of this behaviour is shown in Figure 7.1. While this drive runs unaffected by the absence of the red phase, the input current for the white and blue phases increases.

Many older drives still derive control power from the AC line. This often results in the drive being more sensitive than drives that derive control power directly from the DC bus. Figure 7.2 compares the results of the testing of four drives. DV4 is an older drive that derives its control power from the AC line. It is more sensitive to voltage dips than the other drives. This information impacts on the procedure because the tester can start testing for smaller dip depths for these older drives.

Establishing the source of drive control power can cut the number of tests by as much as three times.

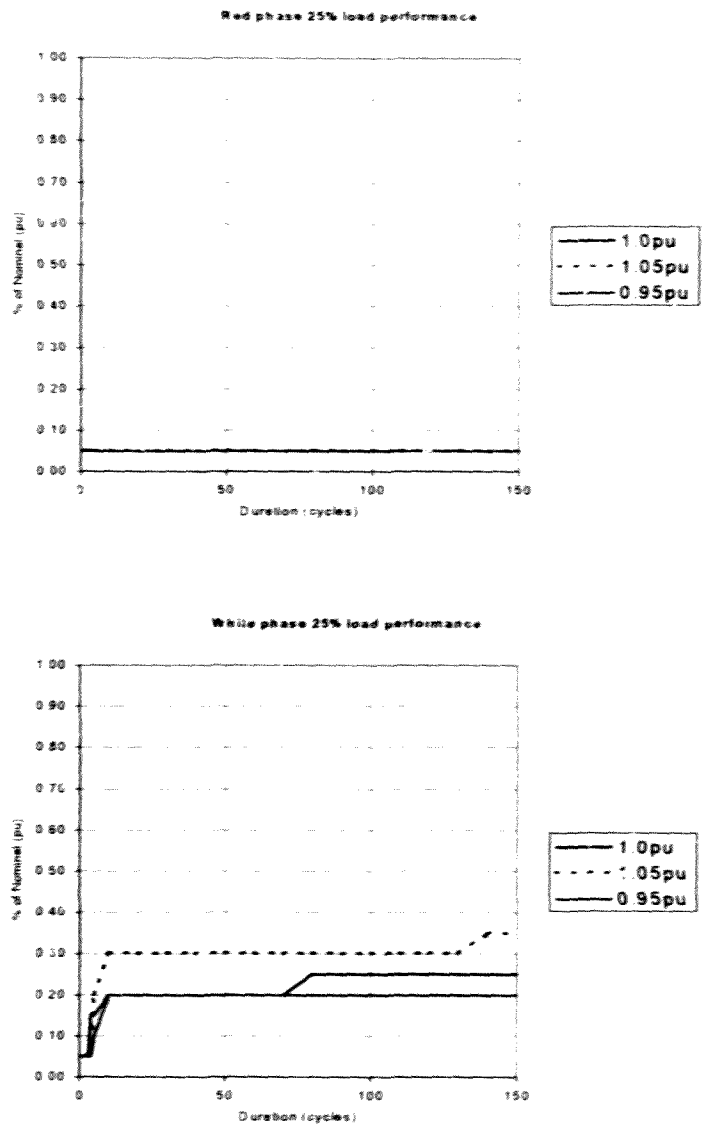


Figure 7.1 An example of a "dead" phase ride through from the results of a DC drive test. The red phase rides through down to a 5% p.u. remaining voltage, while the white phase exhibits some sensitivity to dips applied to it.

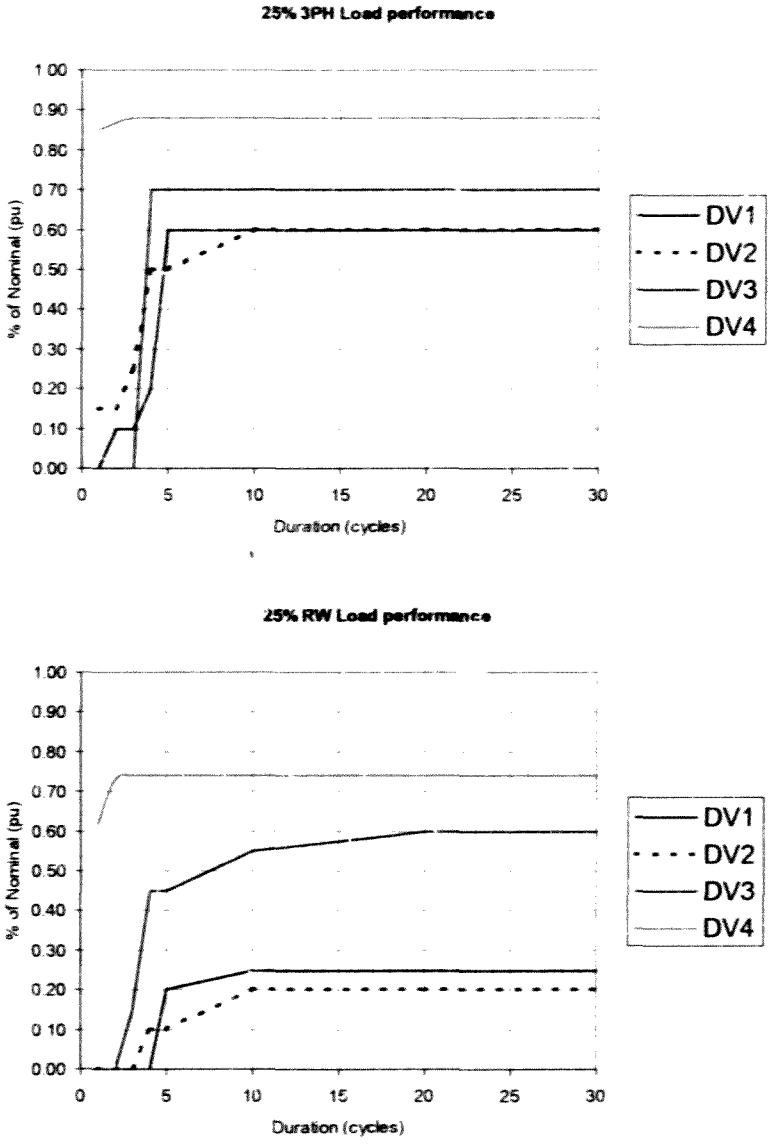


Figure 7.2 An example of an older PWM drive (DV4) exhibiting much more sensitivity than newer drives due to it deriving control power from its AC supply line. Dips with a relatively small magnitude of around 20% or less have an impact on this drive.

7.2 The Influence of Dip-Type on the Test Procedure

All of the drives tested were more sensitive to three-phase dips than phase-phase dips and especially single-phase dips. This was true for PWM, CSI and DC drives. However, PWM drives and DC drives exhibited this behaviour more clearly. This is to be expected because of the importance of the DC bus to these drives.

When PWM drives derive their control power off the DC bus, they can be expected to ride though extreme single-phase dips. Most of the PWM drives tested could ride through single-phase dips down to 0% of the remaining voltage. A DC drive is used in Figure 7.3 to illustrate better ride-through with single-phase dips than with three-phase dips.

The type of dips tested impacts on the testing procedure in that single-phase dips can be ignored for PWM drives if it can be established that they derive their control power from the DC bus. If the number of tests is severely limited by financial constraints, single-phase dip tests can be limited for DC drives and PWM drives in general.

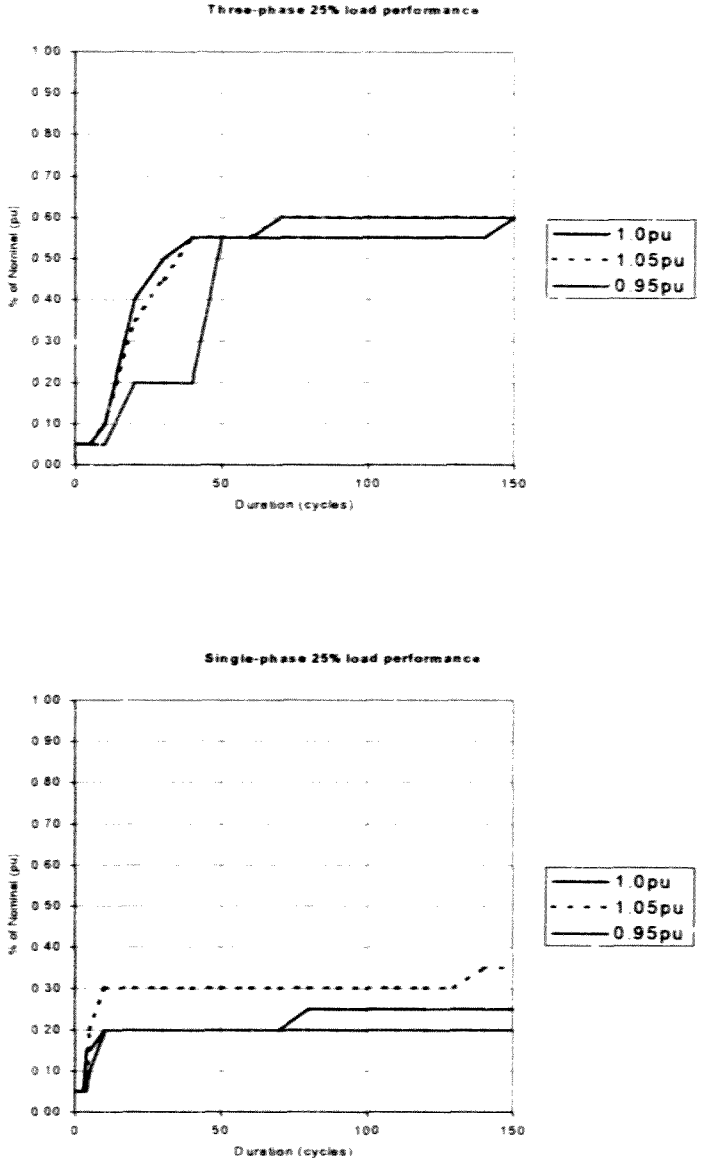


Figure 7.3 An example of a DC drive being more sensitive to three-phase dips than single-phase dips.

7.3 The Influence of Pre-Dip Voltage on the Test Procedure

Pre-dip voltage appears to have a significant influence on drive sensitivity. Testing has shown that these influences are different for PWM, CSI and DC drives. The CSI drive showed no difference in performance when different pre-dip voltages were applied during testing. The PWM drive favoured higher pre-dip voltages for improved dip performance.

The DC drive that was tested varied in performance, but it could not be deduced that it favoured higher or lower pre-dip voltages (see Figure 7.4). It sometimes performed better with a higher pre-dip voltage and sometimes the contrary was true. The reasons for this are more complex. It is thought that because different pre-dip voltages are initiated at different instances on the pre-dip voltage waveform, the drive must in fact be sensitive to the point-in-wave initiation of the dip as opposed to only the pre-dip voltage.

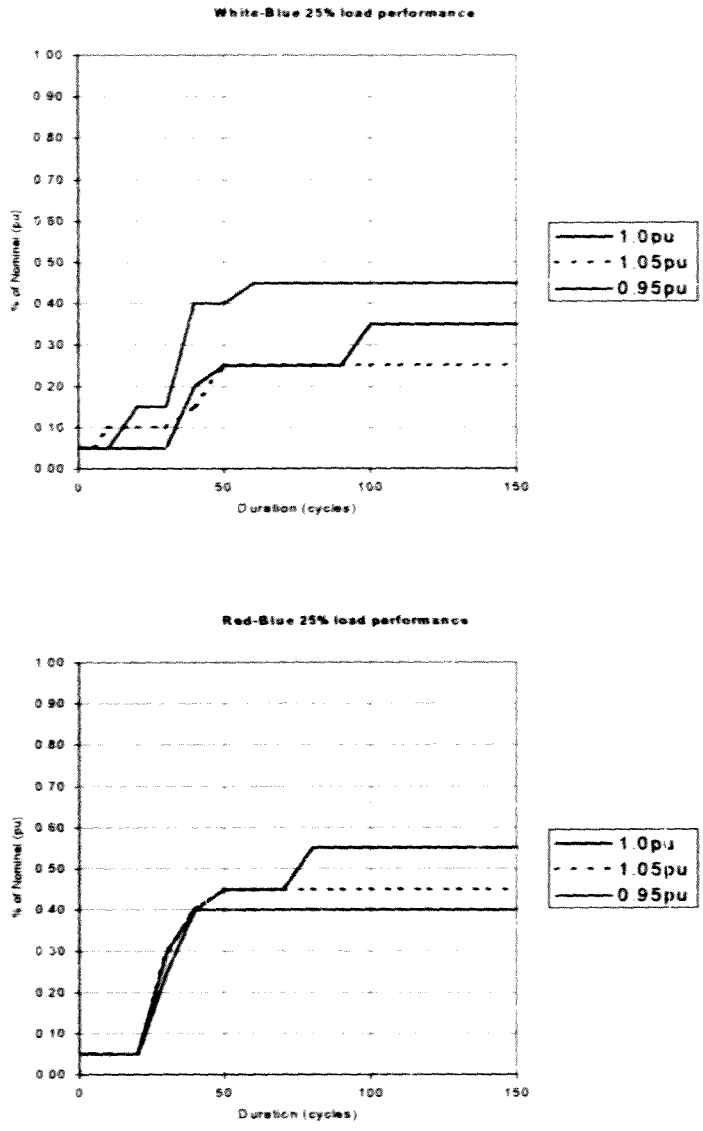


Figure 7.4 DC drive behaviour showed dissimilar results for differences in pre-dip voltage, which is though to be attributed to point-in-wave dip initiation instead.

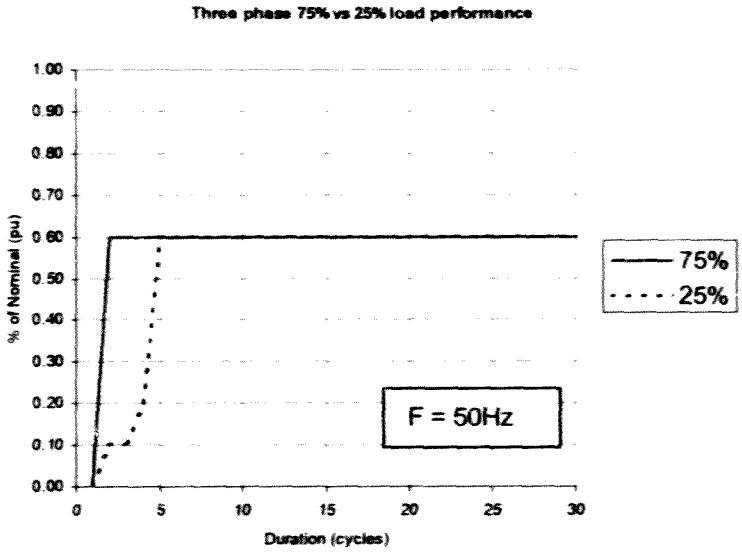
7.4 The Influence of Drive Loading on the Test Procedure

The impact of drive loading is very significant on drive dip sensitivity and the dip testing process. Although the impact in terms of the drive load size has been tested for, the type of load has an even more significant impact [28]. The loading variety at the testing facility is at this stage limited to a DC generator connected to a resistive load. This results in linear speed/torque characteristics.

The drive load size appeared to have different effects on PWM, CSI and DC drives. PWM drives perform better with a lesser load (in this case 25%) than with a larger load of 75% (see Figure 7.5). This was true for all the PWM drives tested. These drives tripped several times on overcurrent for the 75% load, but this was almost never the case with a 25% load.

The CSI drive was very temperamental to load size. It had to be de-rated to match the load in the laboratory. After it was matched to its load, the performance was better when this load was adjusted to 100% of its rating than when it was at 50% of its rating (see Figure 7.6).

The influence of drive loading was also large with the DC drive. Although the results are not available for inclusion into this report, initial test-runs have shown a more stable performance with a 75% load than with a 25% load. Severe overcurrent trips were experienced with a 25% load, whereas no overcurrent trip has been experienced during preliminary testing of the DC drive with a higher load.



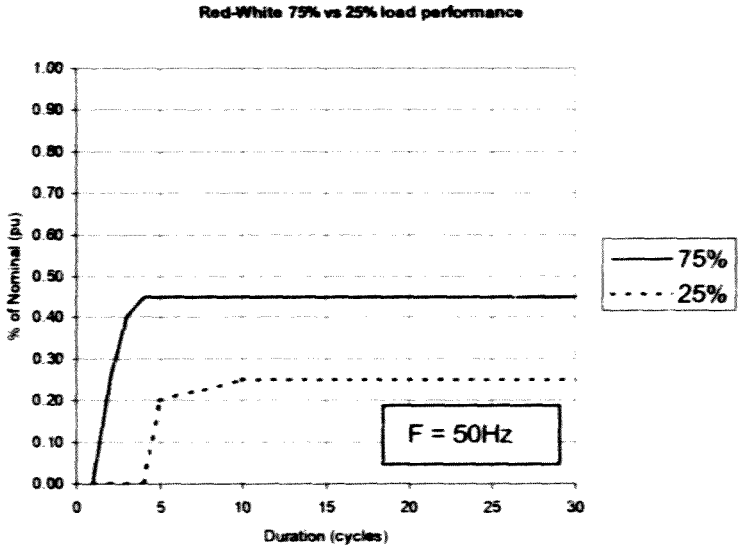


Figure 7.5 Most of the PWM drives tested, showed better performance with a smaller load than with a larger load.

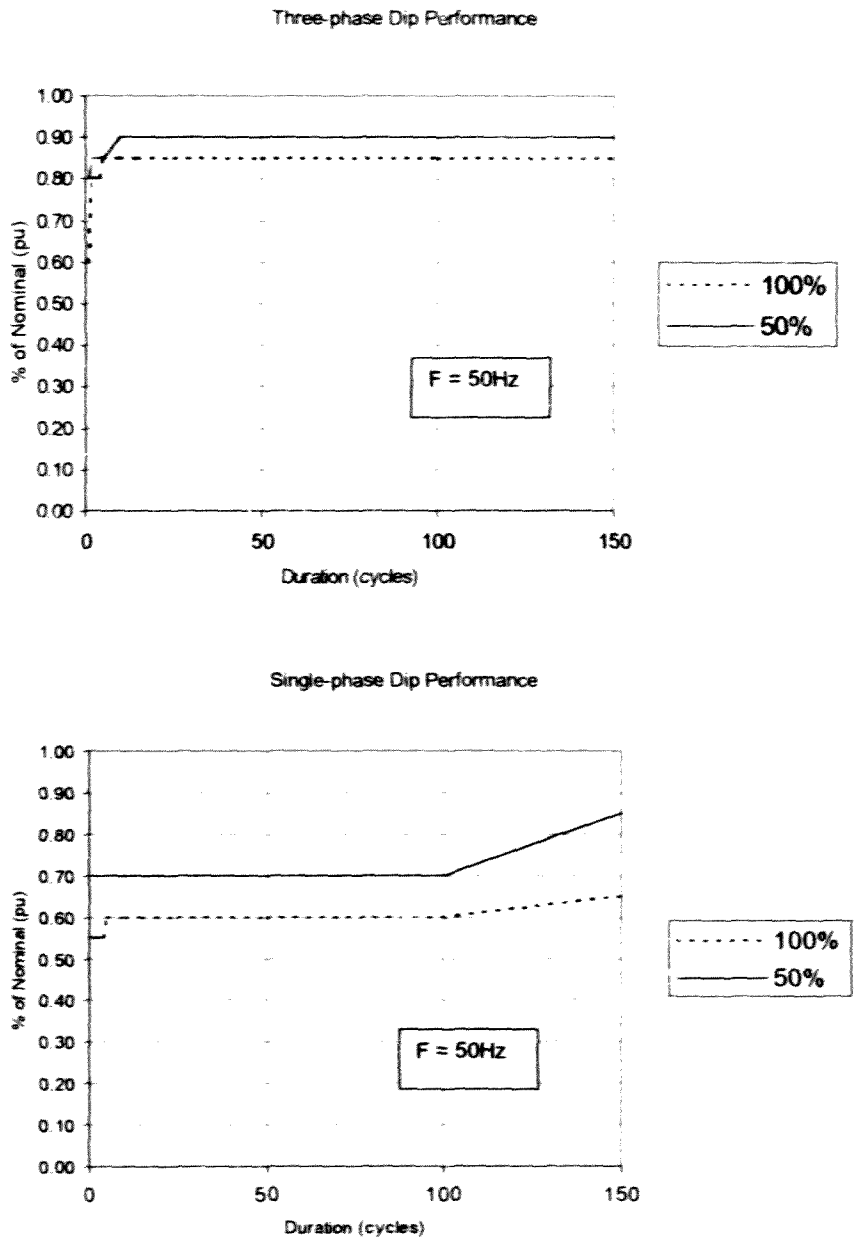


Figure 7.6 The CSI drive tested showed better performance with a larger load (exactly matched) than a with a smaller load.

7.5 Influences of Other Dip Waveform Parameters on the Test Procedure

There are other dip parameters/descriptors (see chapter 3) that can influence the drive dip performance and therefore the dip procedure as well. As already mentioned, point-in-wave dip initiation is thought to be a reason for differences in DC drive performance. This alone suggests that point-in-wave testing should be included.

Phase shift will have an effect on the dip performance of CSI and DC drives. Although sensitivity plots have not been available for inclusion in this report, preliminary test runs have shown this to be so. CSI and DC drives are sensitive to changes in the phase angle because they utilise a phase locked loop (PLL) to synchronise the thyristor firing sequences.

Software parameters will have an extremely important effect on drive performance as discussed in chapter 4. This has been illustrated in chapter 6 as well. However, standard test comparisons of results with other test facilities favour using default factory settings and disabling ride-through options. When testing drives to determine their impact on industrial plant behaviour, other objectives and criteria must be set for testing.

8 CONCLUSIONS AND RECOMMENDATIONS

8.1 Summary and Conclusions

Based on the findings of this report, the following conclusions are made.

8.1.1 General

General conclusions are:

a) Dip compatibility design remains a cost-effective approach to addressing customer plant disruptions due to voltage dips. Establishing the sensitivity of plant equipment such as variable speed drives contributes valuable data to this method of plant problem solving.

b) A number of descriptors exist that describe voltage dips in ways that are more relevant to their impact on equipment and therefore plant systems. Dip depth and duration descriptors are inadequate parameters for testing.

c) Voltage dip testing should be extended beyond testing for balanced dips. Three-phase balanced dips are rare disturbances. Dips are more likely to be unbalanced in magnitude and phase, i.e. single-phase and phase-phase dips.

d) A test protocol is essential where test results from a variety of testing institutions will be compared. The objectives, test criteria, correct documentation, equipment specifications, test specifications and reporting formats all contribute to creating an environment where testing is done in a consistent manner and result comparisons are valid.

e) The voltage dip testing facility, although flexible in the variety of dips that can be applied for testing, has shortcomings that hinder its application in industry. These include a programmable load and test automation that considers optimisation of the test procedure as suggested.

f) A variety of indicators can be used to verify whether a dip event caused a trip to a variable speed drive. These include reading the trip indicators of the equipment, studying the recorded waveforms for visual indicators and listening for audible indicators.

8.1.2 Conclusions based on the hypothesis

It has been established that the results from the testing program can be used to optimise the testing process. This is a requirement if the testing program is to become economically viable.

Specific parameters that influence an optimal test process, as established by the testing program, are:

- AC bus voltage sensing vs. DC bus voltage sensing
- The type of voltage dip applied
- Pre-dip voltage
- Point-in-wave dip initiation
- Size of drive loading

8.2 Recommendations for Future Work

Since 1998, a lot of resources and research effort has gone into the development of the voltage dip test facility (now called the PQ Test Lab) and its testing programs. The voltage dip testing project of Eskom in collaboration with the University of the Witwatersrand has reached the point where commercialisation has become an issue. Like the program's counterparts in the USA, e.g. PEAC, the test program must enter a phase of commercialisation. One could learn from the PEAC experience and its successes.

At a series of working group and steering committee meetings, it was decided that the commercialisation phase should be initiated, but at the same time the research efforts into the development of the program and its application should continue as well.

On the issue of commercialisation, the following was decided:

- A business case and market evaluation should be developed for the PQ Test Lab.
- The services of the PQ Test Lab should be made available to consultants in the field of power quality investigation.
- The services of the PQ Test Lab should be combined with current efforts in Eskom to locate VSDs in the field. The reasons for these VSDs may be for demand-side management or process-control.
- Sponsorship should be found for testing programs, especially from drive manufacturers. A joint venture between the custodians of the PQ Test Lab and a manufacturer (local or international) would initiate this type of sponsorship. Two such manufacturers have been identified.
- Case studies where VSDs have been placed in industry and the services of the PQ Test Lab have been used or illustrated should be marketed in popular media such as drive and process-related magazines.
- Articles on the activities of the PQ Test Lab should be published as briefs or in magazines as above.
- The testing efforts of the PQ Test Lab should be combined with testing initiatives elsewhere in the country such as at the University of Cape Town.

- The testing efforts of the PQ Test Lab should be combined with the testing programs of PEAC.

On the issue of future research, the following was decided:

- More drives from the US should be tested to consolidate 50Hz dip testing of 5HP PWM drives in South Africa.
- Results and methodologies should continue to be compared with EPRI programs for similarities and consistency.
- The development of testing methodologies and test protocol's for voltage dips and other power quality disturbances should be ongoing.
- The results of activities at the PQ Test Lab should be published and presented at both local and international conferences.
- Future projects and work on the PQ Test Lab should include the completion of a programmable load module as well as automated testing.
- There is a need for a portable voltage dip generator for use in field investigations.
- The database of results of testing drives at 50Hz in South Africa is still small and more testing should to be done to develop a larger database of results.
- Parts of the NRS-048 that are still under development may need test results to facilitate the classification of plant equipment into sensitivity zones.

The following are shortcomings of the test program that could not be addressed within this project and should be included in future work.

Specific parameters that could influence the test process should be included in testing, i.e.:

- Phase shift at dip initiation
- Software-enabled ride-through parameters
- Load/Process types
- Mitigation devices

REFERENCES

1. Koch RG, *"Dip Design Considerations: Plant Dip Mitigation Design Guideline"*, Eskom Research Report, RES/RR/99/00042, December 1999.

2. Ammenheuser J, *"Step: Semiconductor Manufacturing Equipment Voltage Sag Immunity"*, Presentation at SEMICON West 1999, 12 July 1999.

3. Abrahams RW, *"EPRI Staff Development: Dip Testing and Power Quality Technology Scanning"*, Eskom Research Report, RES/FR/99/00034, December 1999.

4. Smit I, *"Probabilistic Dip Assessment: South African Dip Chracteristics"*, Eskom Research Report, TRR/QS/98/712, December 1998.

5. McCurrach R, *"Geographic Analysis of Dips in South Africa"*, Eskom Research Report, TRR/QS/98/602, October 1998.

6. Domijan A Jr., Embriz-Santander E, *"System Compatibility SC-610: Adjustable Speed Drives Used In Low-Voltage AC Power Systems"*, Test Protocol, EPRI-PQTN, January 1994.

7. IEC-1000-4-11, *"Electromagnetic compatibility (EMC) – Part4: Testing and measuring techniques – Section 11: Voltage dips, short interruptions and voltage variations immunity tests"*, 1994

8 DRAFT IEEE Standard 1159.2: (draft) *"Recommended Practice for the Characterization of a Power Quality Event"*, 1996.

9. IEEE Standard 1250.2, *"Guide for Service to Equipment Sensitive to Momentary Voltage Disturbances"*, 1995.

10. ANSI/IEEE Standard 995-Part I, *"IEEE Recommended Practice for Efficiency Determination of Alternating-Current Adjustable-Speed Drives"*, 1987.

11. IEEE Standard 1346, *"Recommended Practice for Evaluating Electric Power System Compatibility with Electronic Process Equipment"*, 1998.

12. IEEE Standard 493, *"Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems"*, 1997.

13. BS EN 50160, *"Voltage · ·cteristics of electricity supplied by public distribution systems"*, 1995.

14. IEC 68-1, *"Environmental Testing – Part 1: General and guidance"*,1988.

15. ANSI/IEEE C62.41, "Recommended Practice for Surge Voltages in Low-Voltage AC Power Circuits", 1991.

16. ANSI/IEEE C62.45, *"Guide on Surge Testing for Equipment Connected to Low-Voltage AC Power Circuits"*, 1992.

17. International Union of Producers and Distributors of Electrical Energy (UNIPEDE): 1991, No.50.02

18. UNIPEDE DISDIP, *"Measuring of power failures in MV grid in Europe"*.

19. NRS048-1: 1996, *"Electricity Supply – Quality of Supply Part 1: Overview of implementation of standards and procedures – for application in the Electricity Supply Industry"* First Edition, 1996. Amendment 1, 1998.

20. NRS048-2: 1996, *"Electricity Supply – Quality of Supply Part 2: Minimum Standards – for application by the National Electricity Regulator"*, First Edition, 1996. Amendment 1, 1998.

21. Keus AK, Van Coller JM, Koch RG, *"Development of a test facility to generate complex voltage dips"*, Conference paper, FSAPQC, Durban 1997.

22. Bollen MHJ, "Characterisation of voltage sags experienced by three-phase adjustable speed drives," IEEE Transactions on Power Delivery, in print.

23. Bollen MHJ, Mansoor ., Collins ER, *"Characteristics of Voltage Sags Experienced by Single-phase and Three-phase equipment"*, International

Conference on Power Quality: End-Use Applications and Perspectives (PQA-97), Sweden, June 16-19, EPRI/ELFORSK.

24. Keus AK, Abrahams RW, Van Coller JM, Koch RG, *"The impact of the concept of "Missing Voltage" on the NRS048"*, SAUPEC2000, Durban South Africa, January 2000.

25. Keus AK, Abrahams RW, Van Coller JM, Koch RG, *"Results of Comprehensive Testing of a 15 kW PWM Variable Speed Drive"*, Conference paper, PQA'98 South Africa, Cape Town 1998.

26. Abrahams R, Keus AK, Koch RG, Van Coller JM, *"Comprehensive testing of a current source inverter drive"*, SAUPEC2000, Durban South Africa, January 2000.

27. Mansoor A, Phipps K, Ferraro R, *"System Compatibility Research: Five Horsepower PWM Adjustable-Speed Drives"*, PEAC.0393.R, Power Electronics Applications Center, July 1996.

28. Langley R, Mansoor A, Fortenbery B, Cooke T, *"Evaluation of Ride-Through Systems for Adjustable-Speed Drives"*, TR-111952, EPRI, Palo Alto, CA, November 1998.

29. Enjeti P, *"DC Drive Ride-Through Technology Alternatives and Development"*, TR-111759, EPRI, Palo Alto, CA, December 1998.

30. M.H.J. Bollen, *"The influence of motor reacceleration on voltage sags"*, IEEE Transactions on Industry Applications Vol.31, pp.667-674, 1995.

31. McGranaghan MF., Meuler DR, Samotyj MJ, "Voltage Sags in Industrial Systems, IEEE Transactions on Industrial Applications", Vol. 29., no. 2., March/April 1993.

32. Mansoor A, Collins ER, Bollen MHJ, Lahaie S, *"Behaviour of adjustable-speed drives during phase-angle jumps and unbalanced sags"*, PQA'97, Europe, Stockholm, Sweden, 10-12 June 1997.

APPENDIX A - THE VOLTAGE DIP TESTING PROGRAM TEST OPTIMISATION SCHEDULE

Due to the potentially large number of tests, exhaustive testing may not be financially viable. There could be more than a hundred tests if all the testing parameters applicable to a drive, are included in the test-run. The relevant tests therefore need to be selected according to the type of drive and the test criteria. However, the reduced number of tests can still be too large for the test-run to be financially viable. The end result is that a customer may not be willing to pay for such a service.

It was shown in chapter seven that past testing experience can be used to reduce the number of tests required for a test-run. The more testing knowledge becomes available, the more optimisation of the test procedure can be done. This, together with test-automation, makes for a product that is commercially viable. Test optimisation revolves around understanding the drive that is being tested and reducing the number of tests according to base-tests, i.e. tests that have criteria that must be met. These criteria may be any of the following.

1. Is the drive a PWM, CSI or DC drive?
2. Does the drive have an uncontrolled or line commutated front-end?
3. Is the DC bus of importance to the drive?
4. Does the drive derive its control power from the AC supply via a transformer?
5. Does the drive derive its control power directly from the DC bus?
6. Is the drive affected by pre-dip voltage?
7. Is the drive affected by point-in-wave dip initiation?
8. Does each of the phases react similarly to a load change?
9. Is the drive expected to ride through single-phase dips?
10. Is the drive affected by phase-shifts during the dip or when the dip starts?

These are just some of the questions that may be asked. The questions on the list will also depend on the capabilities of the test facility. Figure A1 shows the questions that are relevant to the PQ Test Lab in a flowchart.

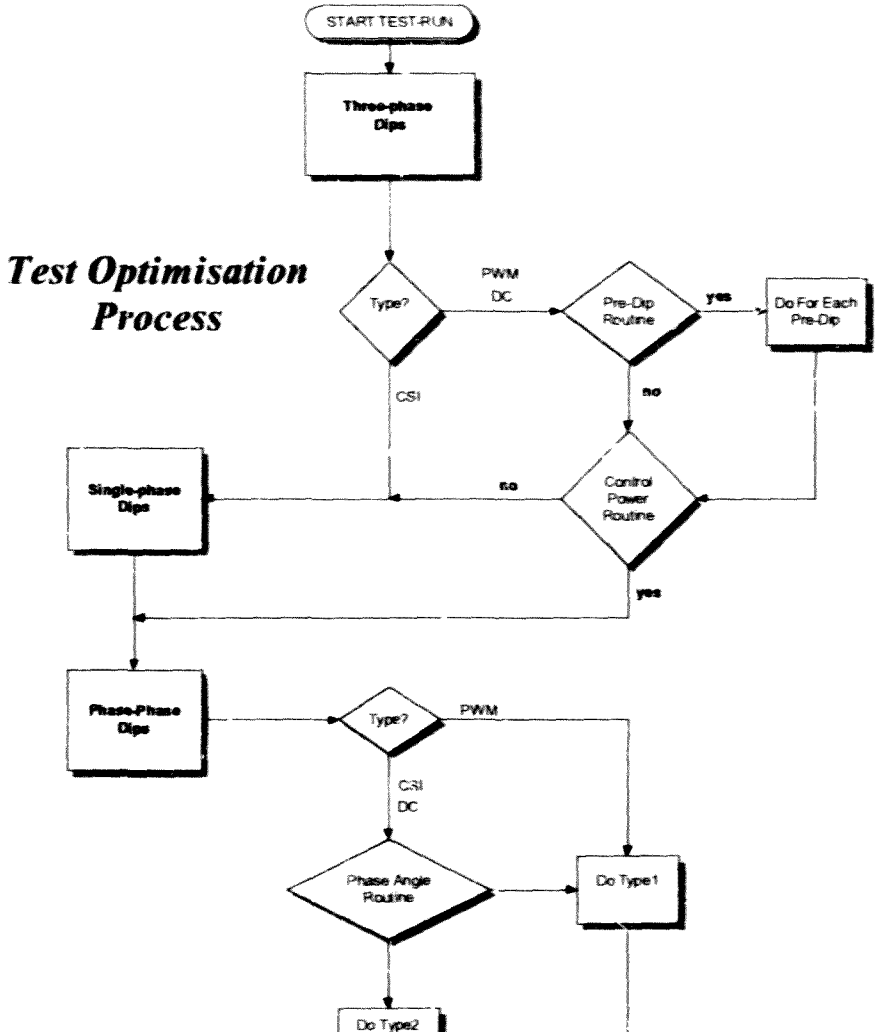


Figure A1 Questions to ask for test-optimisation. Type 1 and Type 2 Dips are detailed in chapter 4.

The following schedule forms are part of the implementation of a test-optimisation process.

A1 Cover Page

PQ Test Lab Test Schedule		
Equipment type	DC variable speed drive	**PQ TEST LAB**
Test Code	D001	**TEST NO. 1003A**
Manufacturer	Concealed	***DC DRIVE TEST***
Sponsor(s)	Part of research	
Tester(s)	Robin Abrahams Adnan Kaus John Van Coller	
Supervisor	John Van Coller	
Period (days)	*From (date)*	*To (date)*
Comments	Two quadrant operation	
Testing for	Depth and duration only	
Test code description	*Testing of a digital direct current drive*	

Test Schedule	**Number of tests**	**Done (tick)**
Test Run A		
Base tests	5	
Schedule 1a	36	
Phase tests	3	
Total	**45**	
Schedule 2a	15	
Grandtotal	**60**	
Test Run B		
Base tests	5	
Schedule 1b	10	
Phase tests	3	
Total	**19**	
Schedule 2a	15	
Grandtotal	**34**	
Test Run C		
Base tests	6	
Schedule 1a	14	
Phase tests	3	
Total	**23**	
Schedule 2a	15	
Grandtotal	**38**	
Test Run D		
Base tests	6	
Schedule 1a	4	
Phase tests	3	
Total	**13**	
Schedule 2b	15	
Grandtotal	**28**	

A2 Base Routines

	PQ Test Lab Test Schedule						
	Equipment type	DC variable speed drive					
	Test Code	D001					
	Manufacturer	Concealed					
	Sponsor(s)	Part of research					
	Tester(s)	Robin Abrahams Adrian Keus John Van Collier					
	Supervisor	John Van Collier					
	Period (days)		*From (date)*		*To (date)*		
	Comments	Two quadrant operation					
	Testing for	Depth and duration only					
	Base Tests						
No.	*Directory*	*Phases involved*	*Pre-dip (pu)*	*Load (%)*	*Dip type*	*Phase angle*	*Done (tick)*
	Pre-Dip Routine		Success (tick)		Fail (tick)		
1		three phase	1.00	25%	Type 1	N/A	
2		three phase	1.05	25%	Type 1	N/A	
3		three phase	0.95	25%	Type 1	N/A	
	Balance Routine		Success (tick)		Fail (tick)		
4		red phase	1.00	25%	Type 1	N/A	
5		white phase	1.00	25%	Type 1	N/A	
6		blue phase	1.00	25%	Type 1	N/A	
	Follow Schedule 1a						
	Follow Schedule 1b						
	Follow Schedule 1c						
	Follow Schedule 1d						

A3 Option A

PQ Test Lab Test Schedule

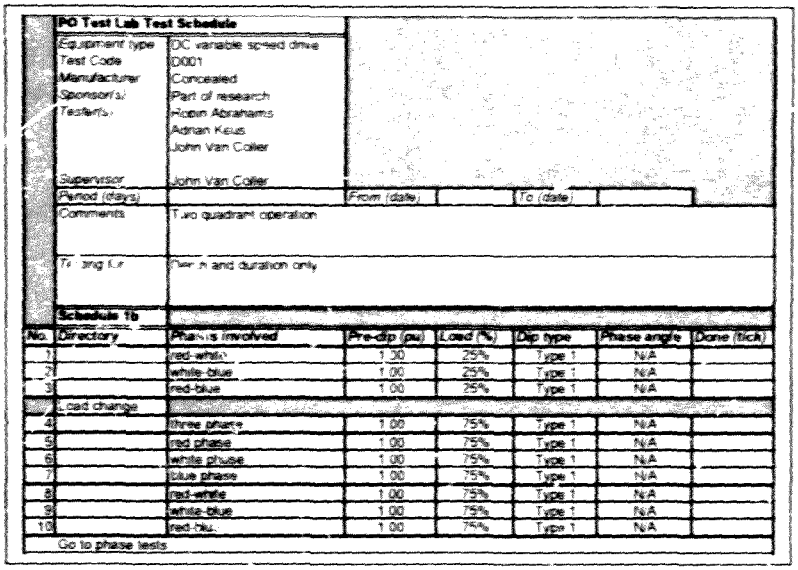
Equipment type	DC variable speed drive
Test Code	D001
Manufacturer	Concealed
Sponsor(s)	Part of research
Tester(s)	Robin Abrahams Adrian Keus John Van Collier
Supervisor	John Van Collier
Period (days)	From (date) To (date)
Comments	Two quadrant operation
Testing for	Depth and duration only

Schedule 1a

No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
1		red phase	1.05	25%	Type 1	N/A	
2		red phase	0.95	25%	Type 1	N/A	
3		white phase	1.05	25%	Type 1	N/A	
4		white phase	0.95	25%	Type 1	N/A	
5		blue phase	1.05	25%	Type 1	N/A	
6		blue phase	0.95	25%	Type 1	N/A	
7		red-white	1.00	25%	Type 1	N/A	
8		red-white	1.05	25%	Type 1	N/A	
9		red-white	0.95	25%	Type 1	N/A	
10		white-blue	1.00	25%	Type 1	N/A	
11		white-blue	1.05	25%	Type 1	N/A	
12		white-blue	0.95	25%	Type 1	N/A	
13		red-blue	1.00	25%	Type 1	N/A	
14		red-blue	1.05	25%	Type 1	N/A	
15		red-blue	0.95	25%	Type 1	N/A	
	Load change						
16		three phase	1.00	75%	Type 1	N/A	
17		three phase	1.05	75%	Type 1	N/A	
18		three phase	0.95	75%	Type 1	N/A	
19		red phase	1.00	75%	Type 1	N/A	
20		red phase	1.05	75%	Type 1	N/A	
21		red phase	0.95	75%	Type 1	N/A	
22		white phase	1.00	75%	Type 1	N/A	
23		white phase	1.05	75%	Type 1	N/A	
24		white phase	0.95	75%	Type 1	N/A	
25		blue phase	1.00	75%	Type 1	N/A	
26		blue phase	1.05	75%	Type 1	N/A	
27		blue phase	0.95	75%	Type 1	N/A	
28		red-white	1.00	75%	Type 1	N/A	
29		red-white	1.05	75%	Type 1	N/A	
30		red-white	0.95	75%	Type 1	N/A	
31		white-blue	1.00	75%	Type 1	N/A	
32		white-blue	1.05	75%	Type 1	N/A	
33		white-blue	0.95	75%	Type 1	N/A	
34		red-blue	1.00	75%	Type 1	N/A	
35		red-blue	1.05	75%	Type 1	N/A	
36		red-blue	0.95	75%	Type 1	N/A	

Go to phase tests

A4 Option B



PO Test Lab Test Schedule

Equipment type	DC variable speed drive
Test Code	0001
Manufacturer	Concealed
Sponsor(s)	Part of research
Tester(s)	Robin Abrahams Adrian Kelus John Van Collier
Supervisor	John Van Collier
Period (days)	From (date) To (date)
Comments	Two quadrant operation
Testing [illegible]	Depth and duration only

Schedule To

No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
1		red-white	1.00	25%	Type 1	N/A	
2		white-blue	1.00	25%	Type 1	N/A	
3		red-blue	1.00	25%	Type 1	N/A	
	Load change						
4		three phase	1.00	75%	Type 1	N/A	
5		red phase	1.00	75%	Type 1	N/A	
6		white phase	1.00	75%	Type 1	N/A	
7		blue phase	1.00	75%	Type 1	N/A	
8		red-white	1.00	75%	Type 1	N/A	
9		white-blue	1.00	75%	Type 1	N/A	
10		red-blue	1.00	75%	Type 1	N/A	

Go to phase tests

A5 Option C

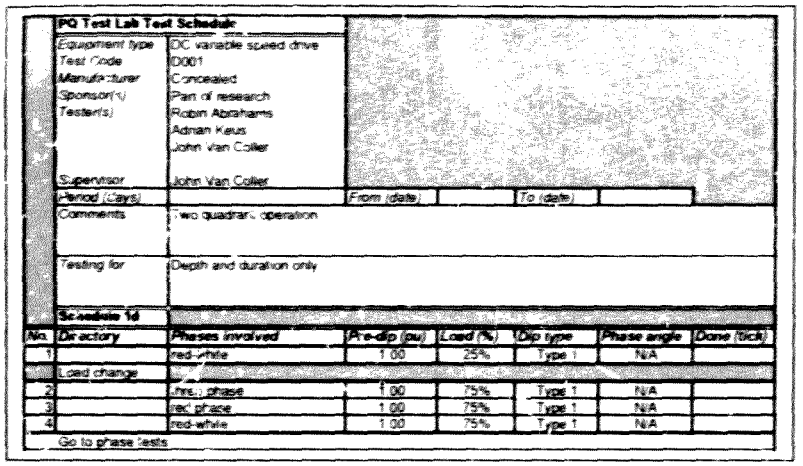
PQ Test Lab Test Schedule	
Equipment type	DC variable speed drive
Test Code	D001
Manufacturer	Concealed
Sponsor's	Part of research
Tester(s)	Robin Abrahams Adrian Keus John Van Collier
Supervisor	John Van Collier
Period (days)	From (date) — To (date)
Comments	Two quadrant operation
Testing for	Depth and duration only

Schedule 1c

No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
1		red phase	1.05	25%	Type 1	N/A	
2		red phase	0.95	25%	Type 1	N/A	
3		red-white	1.00	25%	Type 1	N/A	
4		red-white	1.05	25%	Type 1	N/A	
5		red-white	0.95	25%	Type 1	N/A	
	Load change						
6		three phase	1.00	75%	Type 1	N/A	
7		three phase	1.05	75%	Type 1	N/A	
8		three phase	0.95	75%	Type 1	N/A	
9		red phase	1.00	75%	Type 1	N/A	
10		red phase	1.05	75%	Type 1	N/A	
11		red phase	0.95	75%	Type 1	N/A	
12		red-white	1.00	75%	Type 1	N/A	
13		red-white	1.05	75%	Type 1	N/A	
14		red-white	0.95	75%	Type 1	N/A	

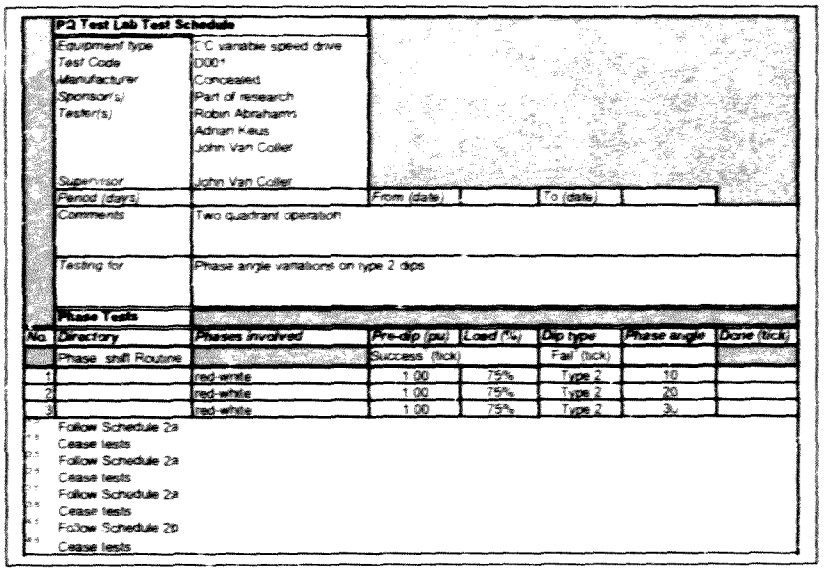
Go to phase tests

A6 Option D



PQ Test Lab Test Schedule:							
Equipment type	DC variable speed drive						
Test Code	D001						
Manufacturer	Concealed						
Sponsor(s)	Part of research						
Tester(s)	Robin Abrahams Adnan Keus John Van Coller						
Supervisor	John Van Coller						
Period (Days)		From (date)		To (date)			
Comments	Two quadrant operation						
Testing for	Depth and duration only						
Scenario 1d							
No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
1		red-white	1.00	25%	Type 1	N/A	
	Load change						
2		red, phase	1.00	75%	Type 1	N/A	
3		red phase	1.00	75%	Type 1	N/A	
4		red-white	1.00	75%	Type 1	N/A	
	Go to phase tests						

A7 Phase-Shift Routine



PQ Test Lab Test Schedule	
Equipment type	C C variable speed drive
Test Code	0001
Manufacturer	Concealed
Sponsor(s)	Part of research
Tester(s)	Robin Abraham Adrian Kwus John Van Coller
Supervisor	John Van Coller
Period (days)	*From (date)* *To (date)*
Comments	Two quadrant operation
Testing for	Phase angle variations on type 2 dips

Phase Tests

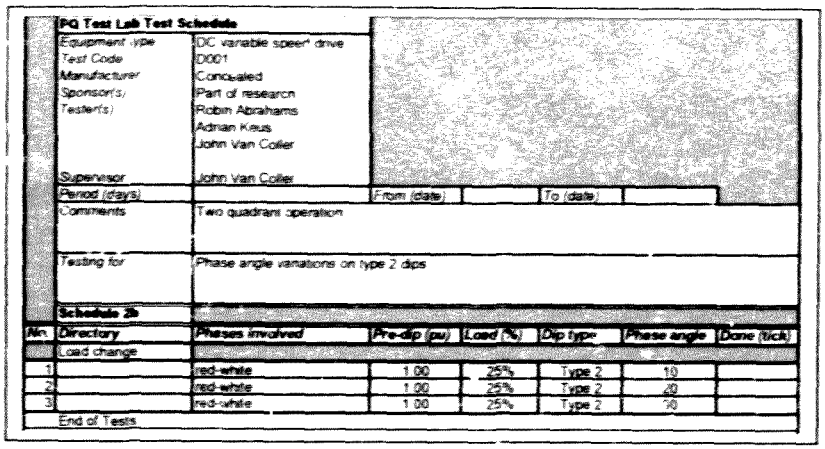
No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
	Phase_shift Routine		Success (tick)		Fail (tick)		
1		red-white	1.00	75%	Type 2	10	
2		red-white	1.00	75%	Type 2	20	
3		red-white	1.00	75%	Type 2	30	

Follow Schedule 2a
Cease tests
Follow Schedule 2a
Cease tests
Follow Schedule 2a
Cease tests
Follow Schedule 2b
Cease tests

A8 Phase-Shift Option

PQ Test Lab Test Schedule						
Equipment type	DC variable speed drive					
Test Code	D001					
Manufacturer	Concealed					
Sponsor(s)	Part of research					
Tester(s)	Robin Abrahams Adrian Kerus John Van Coller					
Supervisor	John Van Coller					
Period (days)		From (date)		To (date)		
Comments	Two quadrant operation					
Testing for	Phase angle variations on type 2 dips					
Schedule 2a						
No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
1		white-blue	1.00	75%	Type 2	10	
2		white-blue	1.00	75%	Type 2	20	
3		white-blue	1.00	75%	Type 2	30	
4		red-blue	1.00	75%	Type 2	10	
5		red-blue	1.00	75%	Type 2	20	
6		red-blue	1.00	75%	Type 2	30	
Load change							
7		red-white	1.00	25%	Type 2	10	
8		red-white	1.00	25%	Type 2	20	
9		red-white	1.00	25%	Type 2	30	
10		white-blue	1.00	25%	Type 2	10	
11		white-blue	1.00	25%	Type 2	20	
12		white-blue	1.00	25%	Type 2	30	
13		red-blue	1.00	25%	Type 2	10	
14		red-blue	1.00	25%	Type 2	20	
15		red-blue	1.00	25%	Type 2	30	
End of Tests							

A9 No Phase-Shift Option



PQ Test Lab Test Schedule						
Equipment type	DC variable speed drive					
Test Code	D001					
Manufacturer	Concealed					
Sponsor(s)	Part of research					
Tester(s)	Robin Abrahams Adrian Kreus John Van Coller					
Supervisor	John Van Coller					
Period (days)		From (date)		To (date)		
Comments	Two quadrant operation					
Testing for	Phase angle variations on type 2 dips					

Schedule 2b							
No.	Directory	Phases involved	Pre-dip (pu)	Load (%)	Dip type	Phase angle	Done (tick)
	Load change						
1		red-white	1.00	25%	Type 2	10	
2		red-white	1.00	25%	Type 2	40	
3		red-white	1.00	25%	Type 2	90	
	End of Tests						

APPENDIX B - DATASHEETS

This Appendix contains the Data Sheets to record the measurements obtained during the actual testing of the adjustable-speed drives. These forms provide the technician and/or engineer with a means to ensure that the proper data are recorded in an organised and clear fashion. Forms have also been provided to record drive, motor and environmental information. Copies of the Data Sheets for each one of the tests specified by the sponsor should be made for each VSD undergoing testing and be included in the testing report for that particular VSD.

B1 Test Log Sheet

VOLTAGE DIP TESTING LOG SHEET

Name of Tester

Schedule No		Test No (on test schedule)	
Date			(DD-MM-YY)
Time Started	H		(24hr format)
Time Ended	H		(24 hr format)

Dip class (please tick **X**)

class1	class2	class5
	class3	class6
	class4	class7

Angle Size (degrees)

Phases dipped (please tick **X**)

three-phase	red-phase	red-white-phase
	white-phase	white-blue phase
	blue-phase	red-blue phase

Pre-dip (p.u. nominal) | Load-size (%)

Please write where appropriate. Use the legend at the bottom of the table. If not applicable, write N/A

Duration (ms)	Duration (cycles)	Ride Through (p.u. nominal)	Trip (p.u. nominal)	Cause of Trip (Display indication)	Speed Indication (as per code)	Current Indication (as per code)
20	1					
40	2					
60	3					
80	4					
100	5					
200	10					
400	20					
600	30					
800	40					
1000	50					
1200	60					
1400	70					
1600	80					
1800	90					
2000	100					
2200	110					
2400	120					
2600	130					
2800	140					
3000	150					

Speed indicators

S1 : Hardly audible, no change in speed waveform
S2 Slow down and smooth recovery (No restart)
S3 Audible oscillation
S4 Slow down with sharp recovery (Restart)
S5 Slow down completely

Current indicators

C1 No visible change in current waveform
C2 Visible overcurrent after dip
C3 Visible oscillation on current waveform
C4 Low current after dip until restart

B2 Drive information

Item	Description	
a.	Manufacturer/Vendor	
	Model number/ Type	
	Serial number/ File No	
b.	Firmware/Controller software edition	
c.	Input voltage (1ϕ or 3ϕ, Volts, tolerance)	
d.	Input frequency (Hz)	
e.	Input current (A)	
f.	Input power (kVA)	
g.	Output voltage range (1ϕ or 3ϕ, Volts)	
h.	Output frequency range (Hz)	
i.	Output current (A)	
j.	Output power (kVA)	
k.	Max and min motor size (hp and/or kW)	
l.	Enclosure (NEMA 1, NEMA 12, etc.)	
m.	Operating temperature (°C)	
n.	Operating altitude (m)	
o.	Operating relative humidity (%)	
p.	Cooling method/requirements	
q.	Weight (kg)	

B3 Motor Ratings

Item	Description	
a.	Manufacturer/Vendor	
	Model No./Type	
	Serial No.	
b.	Voltage (1ϕ or 3ϕ, Volts)	
	Connection (delta/ wye)	
c.	Frequency (Hz)	
d.	Current (A)	
e.	Power (hp/kW)	
	Speed (rpm)	
f.	Service factor	
g.	Nominal efficiency	
	Power factor	
	Duty Cycle	
h.	NEMA/SABS/?? Design	
i.	Insulation class	
	Protection	
j.	Frame/ Mount	
k.	Enclosure (TEFC, ODP, etc.)	
l.	Operating temperature (°C)	
m.	Operating altitude (m)	
n.	Operating relative humidity (%)	
o.	Cooling method/requirements	
p.	Lubricant/ Grease	
q.	Bearings	

B4 Software Parameters

Item	Description	Please Tick ✓	Code (if Applicable)
	Manufacturer/Vendor		
a.	Overcurrent general/ at speed		
	Overcurrent on acceleration		
	Overcurrent on deceleration		
b.	Overvoltage general/ at speed		
	Overvoltage on acceleration		
	Overvoltage on deceleration		
c.	DC bus undervoltage		
d.	Ramp (Auto) restart		
e.	Flying (Auto) restart		
f.	Undervoltage controller		
g.	Overvoltage controller		

B5 Test Environment

Item	Description	Actual Conditions	ANSI/IEEE standards 100-1988, 112-1984, and C62.41 and 45. Recommendations
1	Temperature and relative humidity		25 ± 5°C and < 85% humidity
2	Altitude		< 2000 m
3	VSD Input Voltage		sinusoidal waveform with THD < 1%
4	VSD Input Frequency		50 or 60 Hz ± 0.5%

APPENDIX C - RESULTS OF THE TESTING PROGRAM AT THE PQ TEST LABORATORY

C1 The Test Results For PWM Drives

This section presents results from tests on PWM drives. These drives include three drives of US-origin and one drive from a local manufacturer. It should be noted, in reference to chapter 5, that US requirements for testing are different in that dips for up to 30 cycles in duration are tested for. The South African requirement is to extend the duration to 150 cycles. The drives have been coded as follows to conceal their identity:

- DV1, DV2, DV3 – US-manufactured drives
- DV 4 – A locally manufactured drive

Comparisons are made for each drive individually in terms of dip-type and loading. For ease of evaluation, only the US drive test results were used for this comparison. Thereafter, comparisons are made between all the drives simultaneously in terms of dip-type and loading (including the locally manufactured drive). Loading has been set at 75% and 25% respectively. The pre-dip voltage is 1.0 for all the cases. General comments are given in each case. All plots can be seen in reference to chapter 4 and 5. Similar criteria have been set as in chapter 6.

C1.1 Dip-Type Comparisons

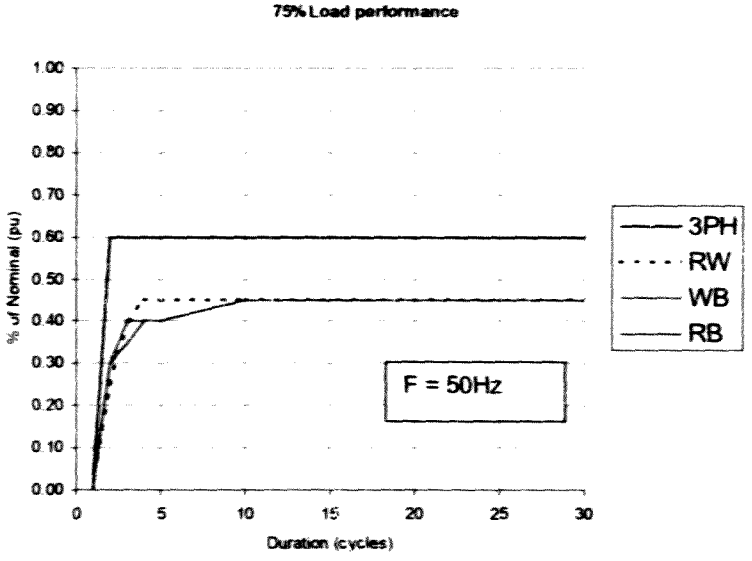
The dip types that were tested are compared in each load category for each drive and are as follows:

- Three-phase
- Red-White phase-phase
- White-Blue phase-phase
- Red-Blue phase-phase

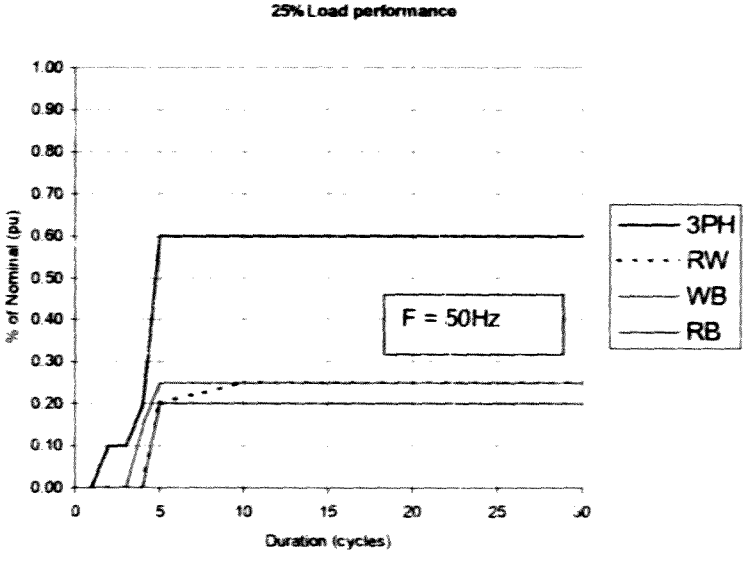
These drives could sustain single-phase dips down to 0% of nominal voltage level, so that these results were deemed useless for comparison.

DRIVE1 (DV1)

a) 75% load dip ride-through performance

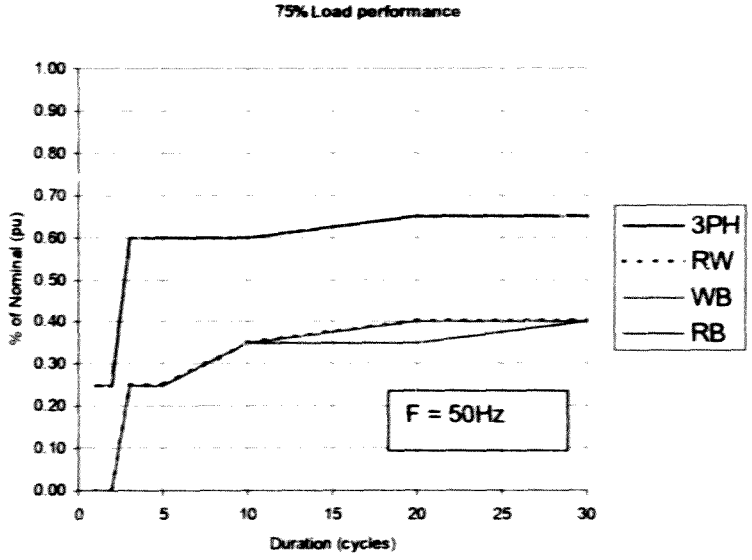


b) 25% load dip ride-through performance

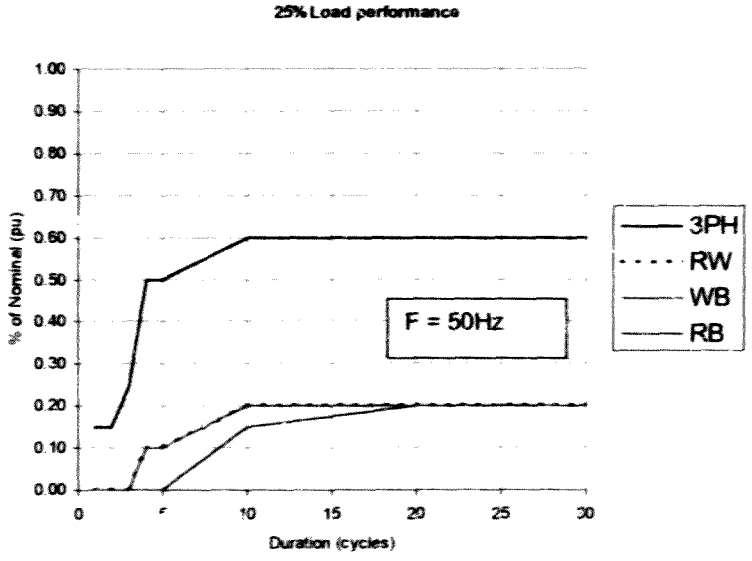


DRIVE 2 (DV2)

a) 75% load dip ride-through performance

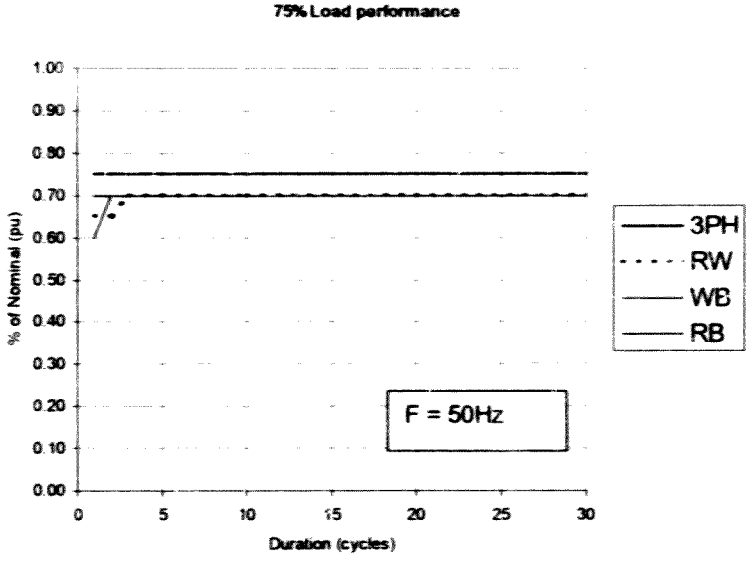


b) 25% load dip ride-through performance

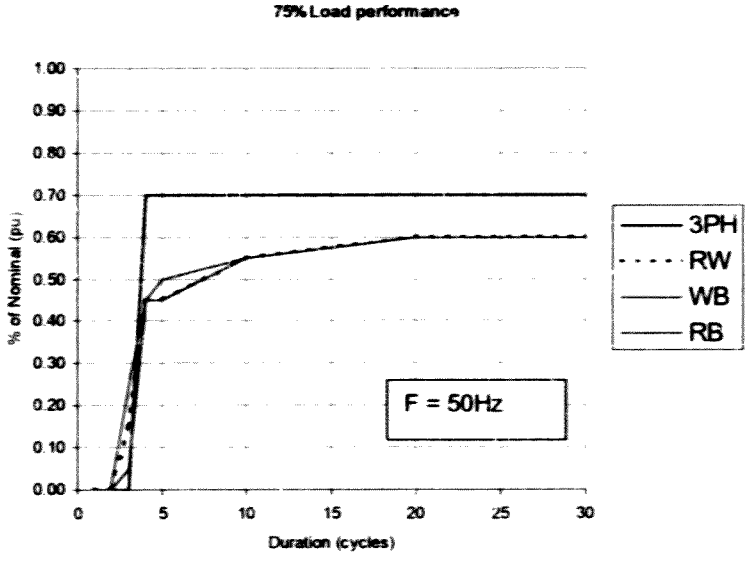


DRIVE 3 (DV3)

a) 75% load dip ride-through performance



b) 25% load dip ride-through performance



General Comments:

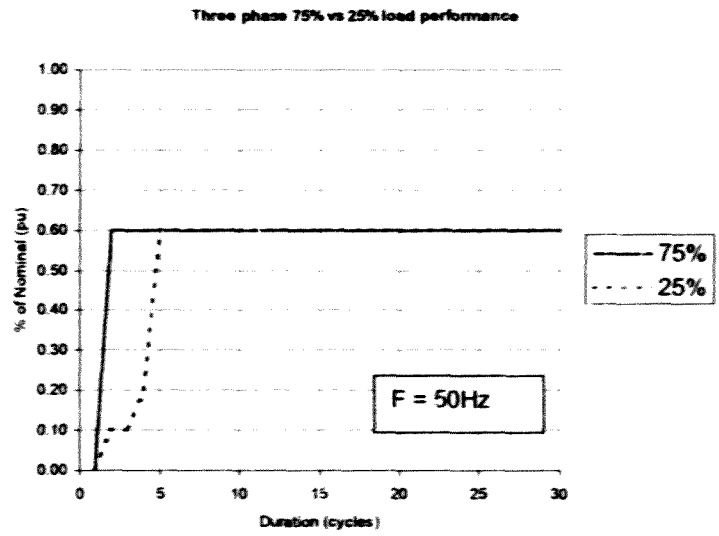
- The phase-phase dips result in better drive immunity than in the case of three-phase dips.
- Red-white, white-blue, red-white performances are approximately the same, indicating sensing of the dc-bus voltage to initiate an undervoltage trip.

C1.2 Load Comparison

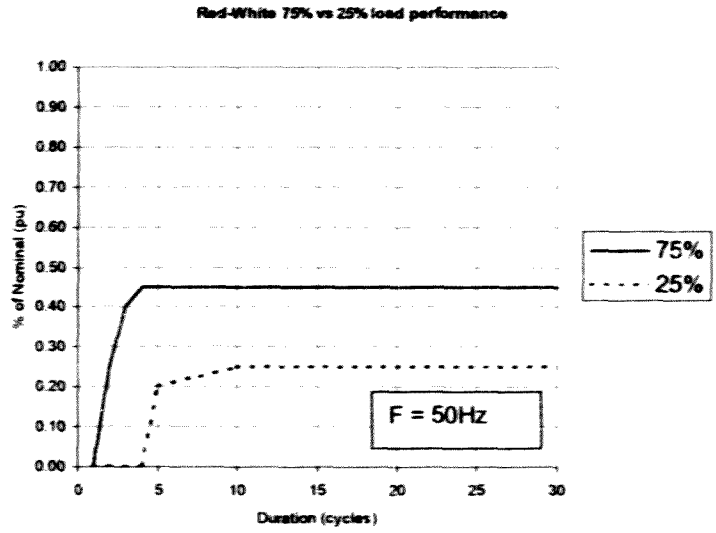
75% and 25% load conditions are compared for each dip-type category.

DRIVE 1 (DV1)

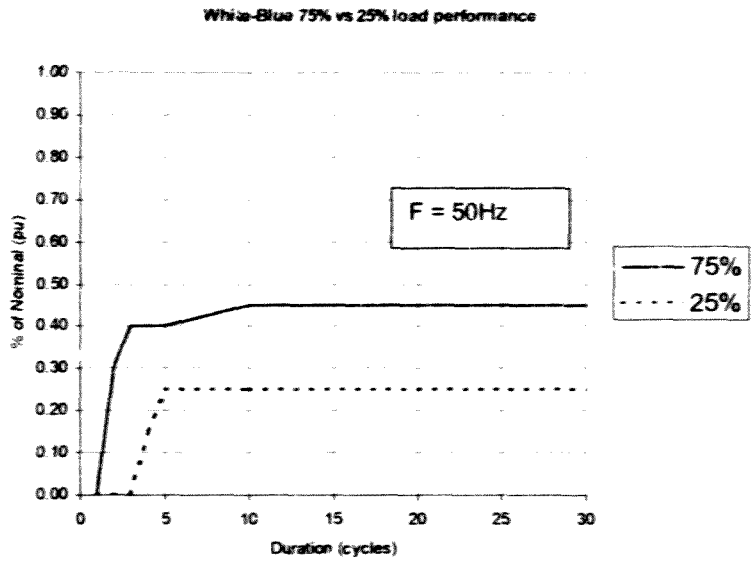
a) Three-phase dip ride-through performance



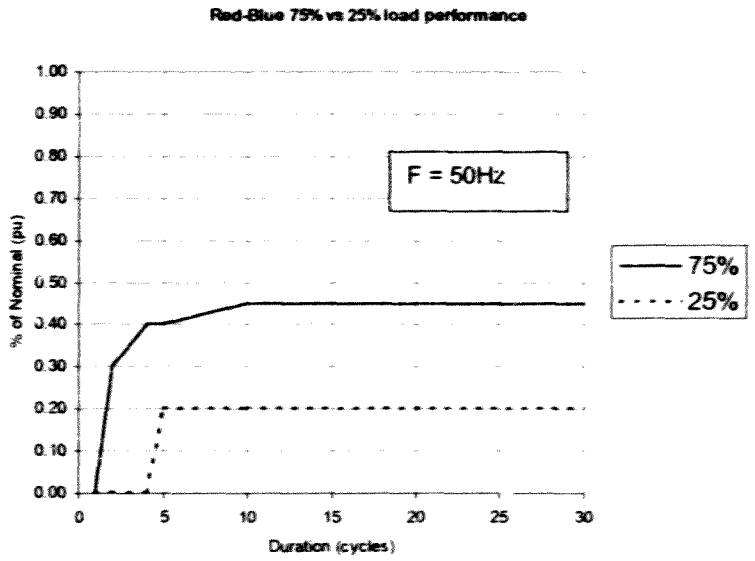
b) Red-white-phase dip ride-through performance



c) White-blue-phase dip ride-through performance

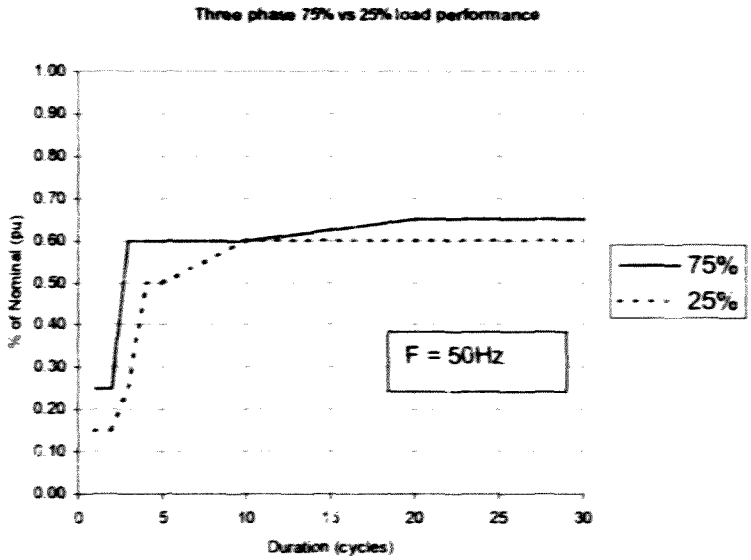


d) Red-blue-phase dip ride-through performance

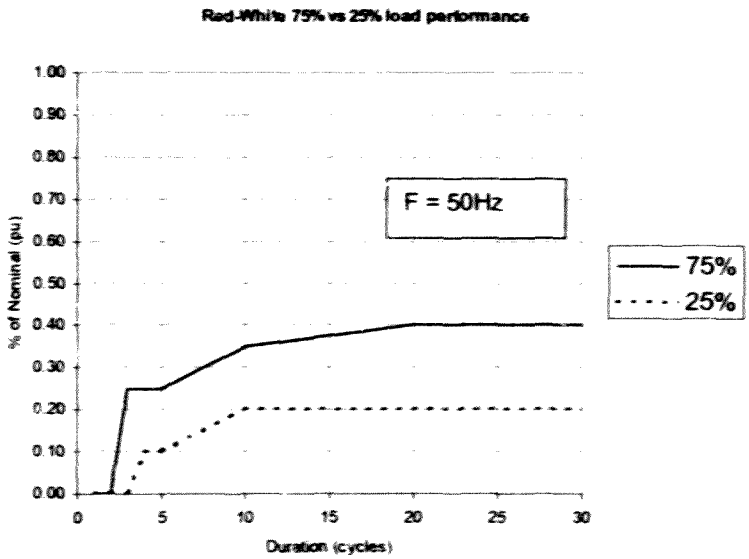


DRIVE 2 (JV2)

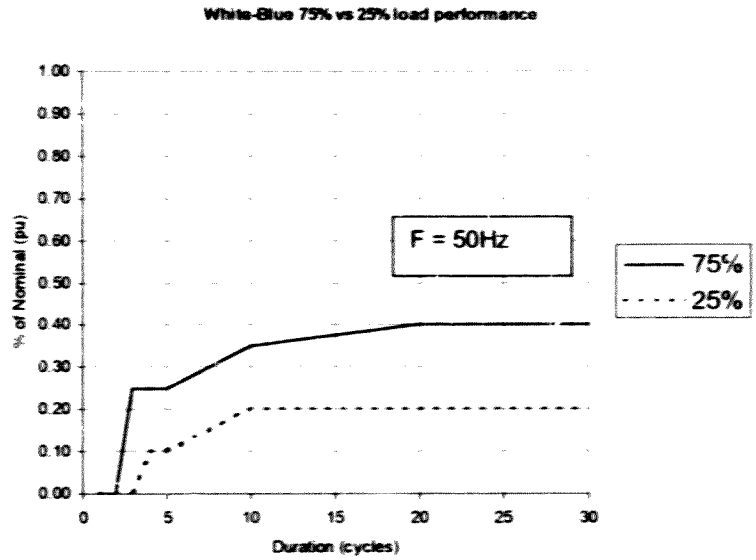
a) Three-phase dip ride-through performance



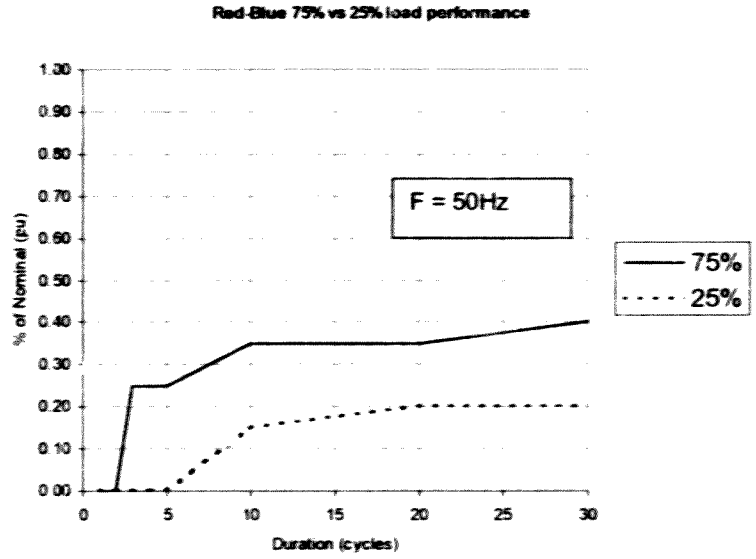
b) Red-white-phase dip ride-through performance



c) White-blue-phase dip ride-through performance

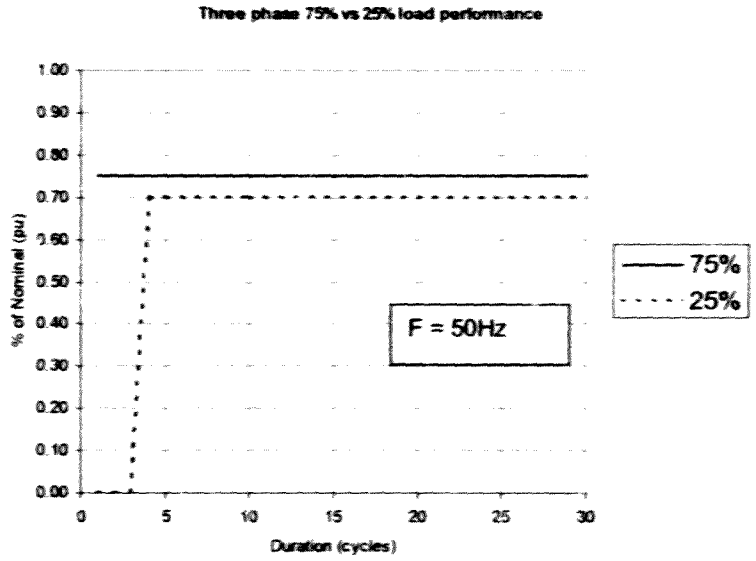


d) Red-blue-phase dip ride-through performance

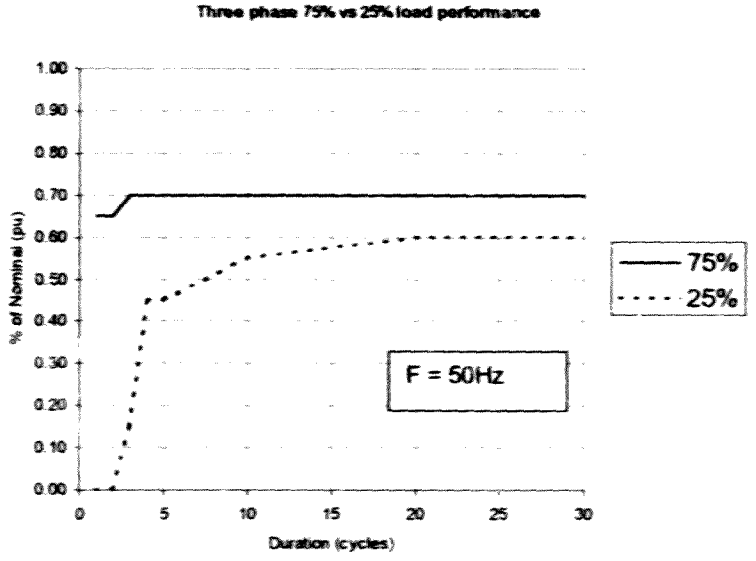


DRIVE 3 (DV3)

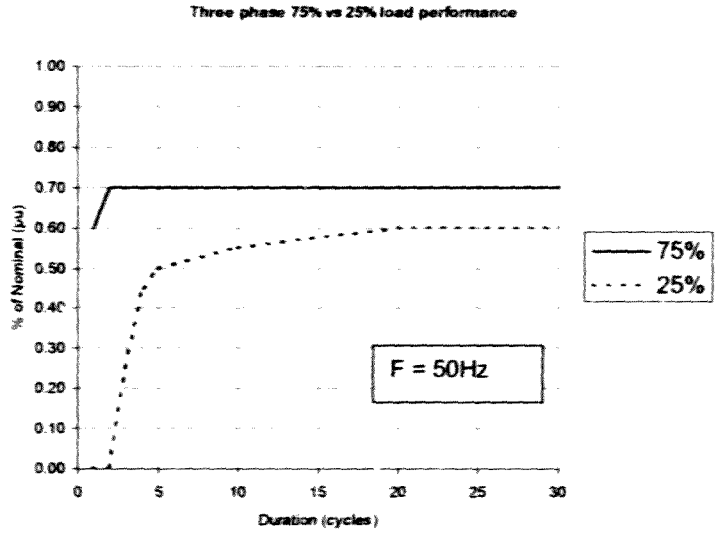
a) Three-phase dip ride-through performance



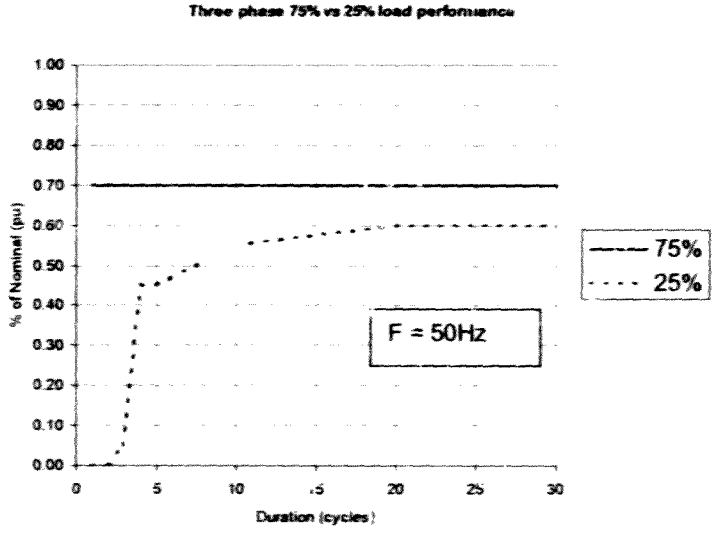
b) Red-white-phase dip ride-through performance



c) White-blue-phase dip ride-through performance



d) Red-blue-phase dip ride-through performance



General Comments:

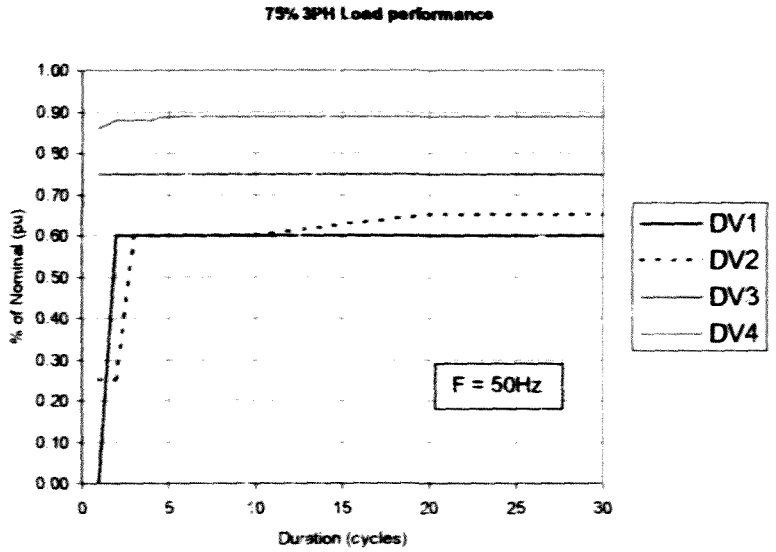
- The variable speed drives perform better when 25% loaded than when 75% loaded.

C1.3 Drive Comparison

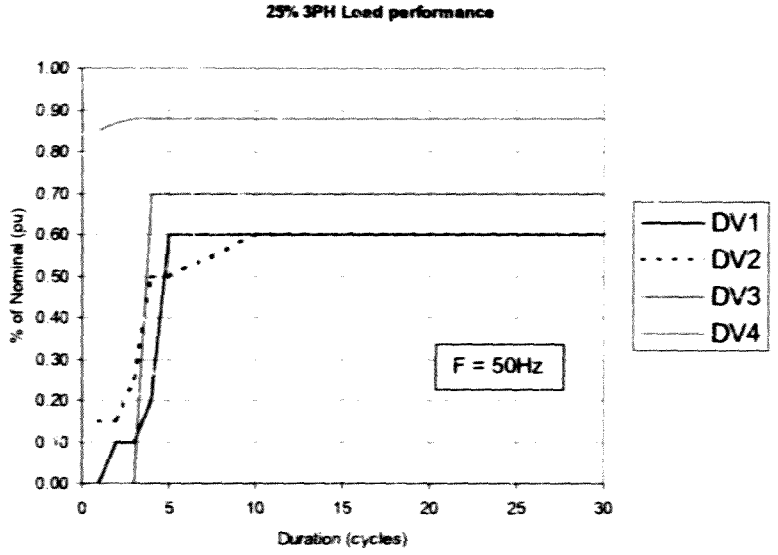
Drives are compared with each other according to the load conditions and dip-types that the drives were subjected to DV4, the locally manufactured drive, was included for comparisons. To make the comparison more relevant, the following steps were taken:

- Auto-restart options were disabled.
- Loading used exactly the same load references for 75% and 25% load respectively.
- Environmental conditions were similar to that specified in chapter 6.
- All options related to ride-through were where possible, disabled.
- Settings such as undervoltage trip voltage were not altered, so that results can be seen in the context of default factory settings.

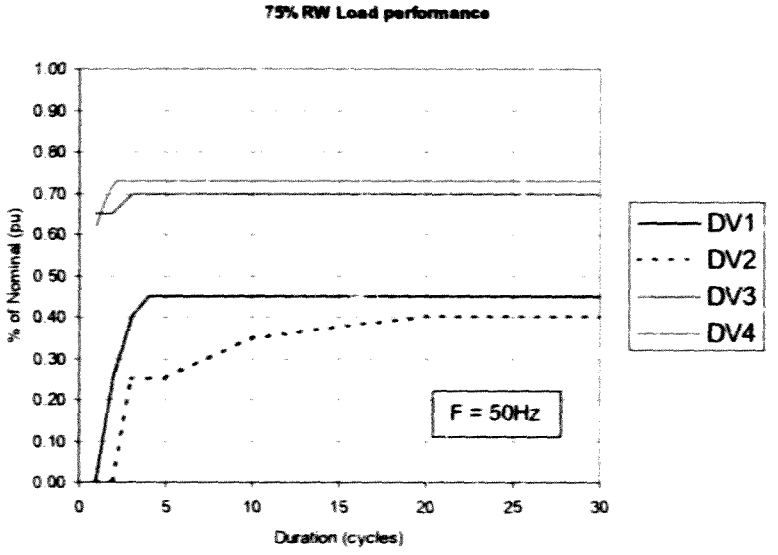
a) Three-phase 75% dip ride-through performance



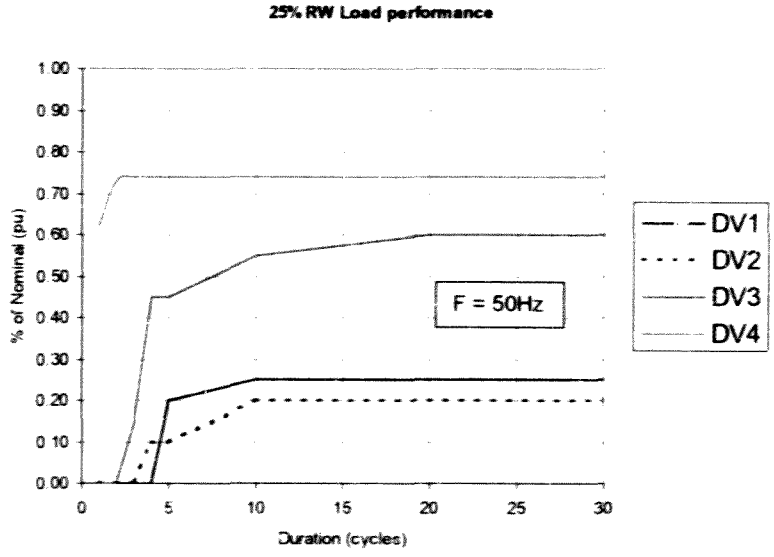
b) Three-phase 25% dip ride-through performance



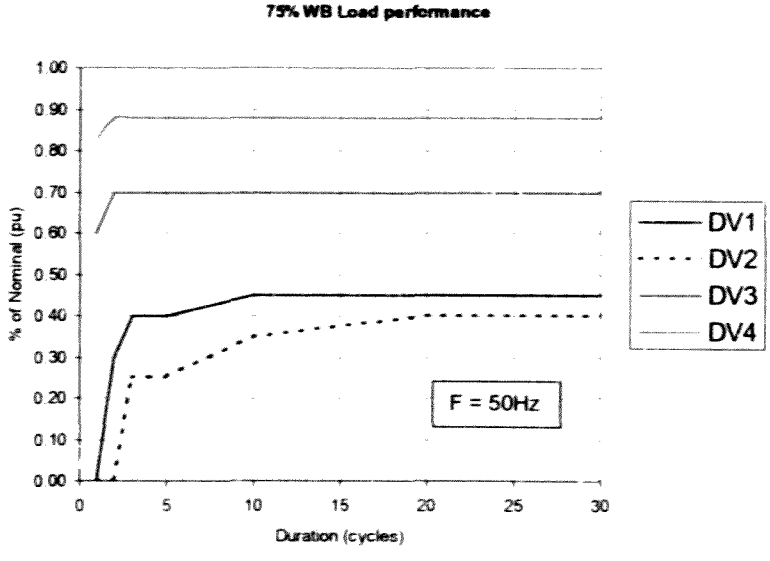
c) Red-white 75% dip ride-through performance



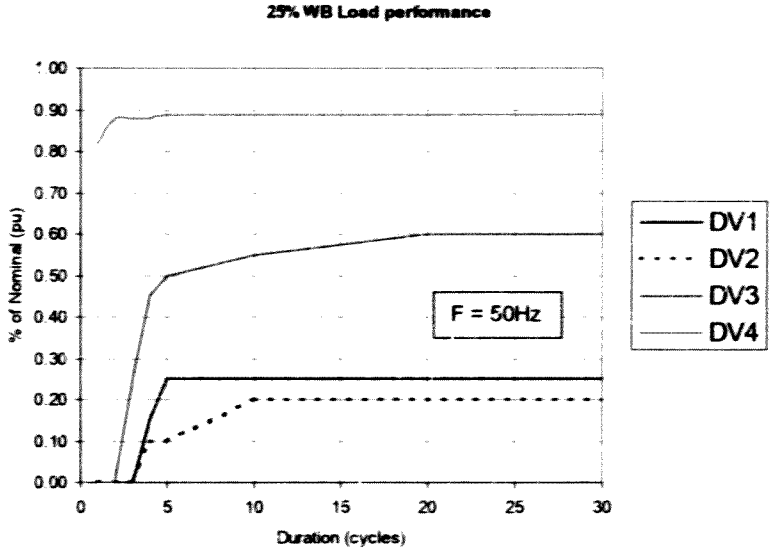
d) Red-white 25% dip ride-through performance



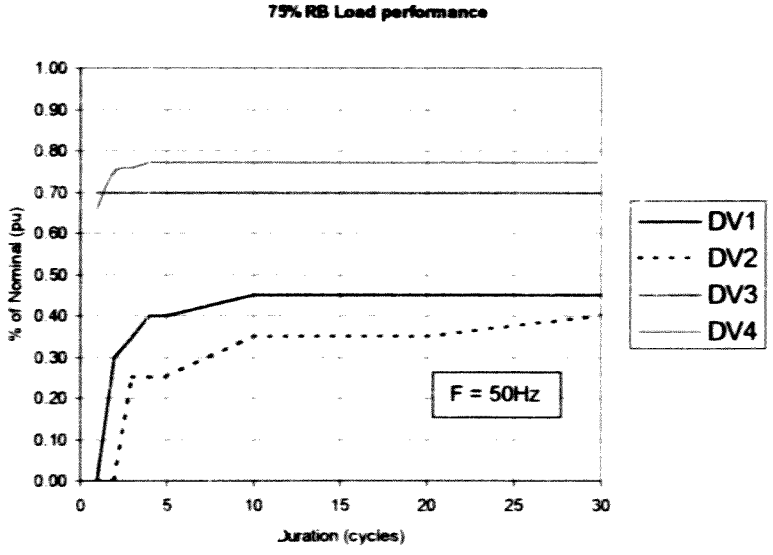
e) White-blue 75% dip ride-through performance



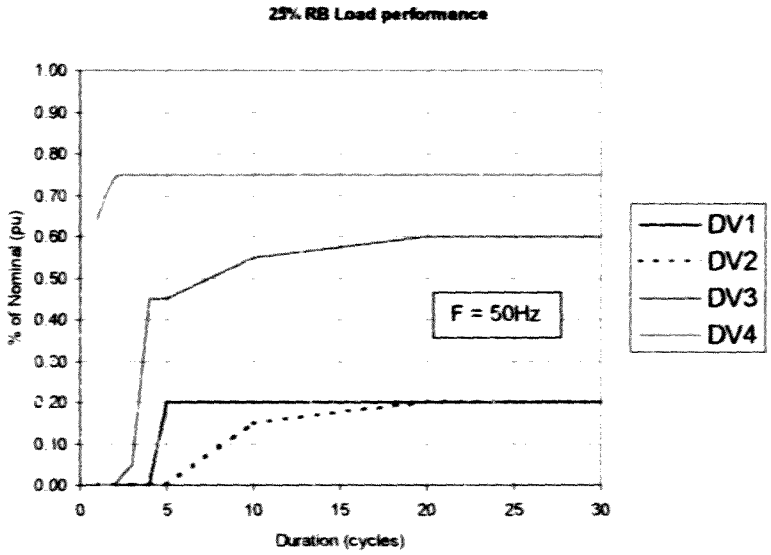
f) White-blue 25% dip ride-through performance



g) Red-blue 75% dip ride-through performance



h) Red-blue 25% dip ride-through performance



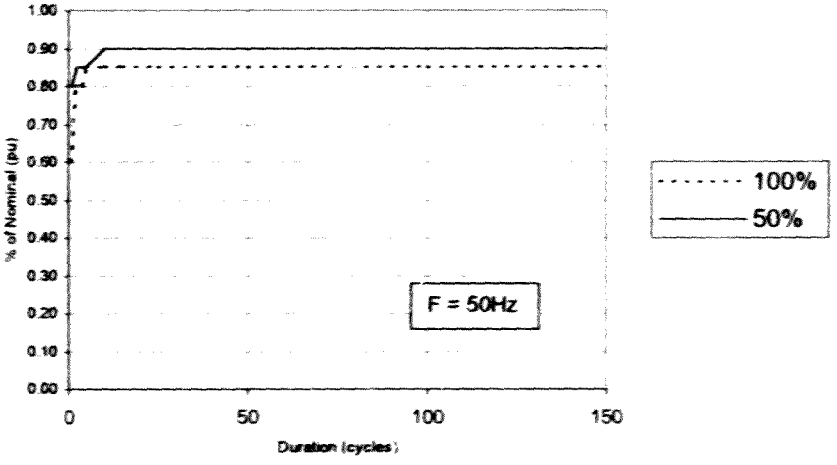
General comments:

- The overall sensitivity of drive 3 and 4 was substantially higher than that of drive 1 and drive 2. This is true for all three-phase and phase-phase dips.
- Drive 2 has a marginally higher sensitivity to three-phase dips than drive1.
- Drive 1 has a slightly higher sensitivity to phase-phase dips than drive 2.
- It was noted that drive 4 had its sensing done on the AC input side. Its ride-through performance was worse than that of the other drives. It was also sensitive to single-phase dips on its white and blue phases.

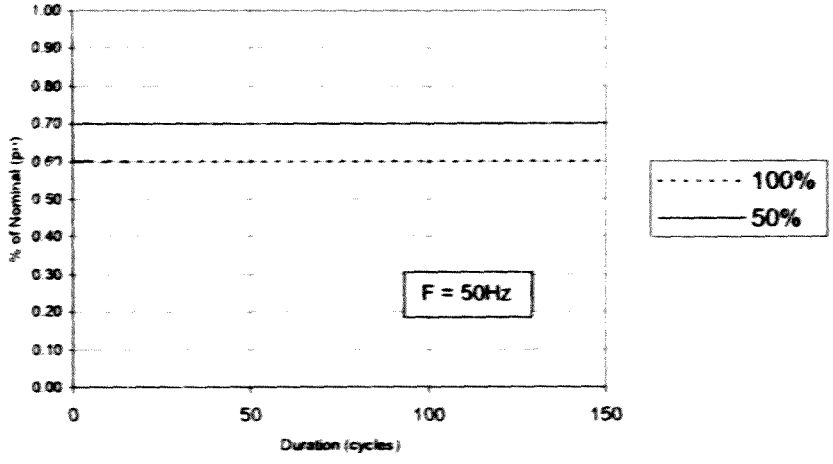
C2 The Test Results For A CSI Drive

This section presents results from tests done on a CSI variable speed drive. Loading has been set to 100% and 50% respectively. The 100% and 50% load values are plotted on the same graph for the different voltage dips tested. The pre-dip voltage is 1.0 for all cases. It was found during testing that a change in pre-dip voltage does not affect performance at all.

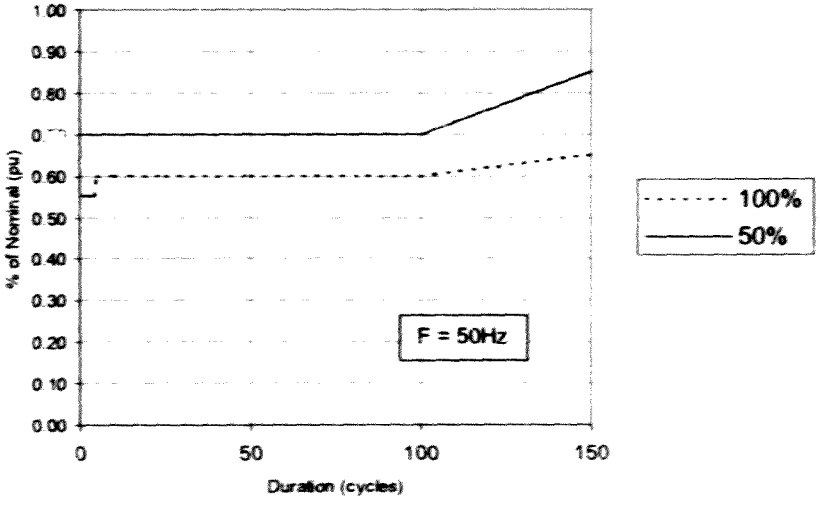
a) Three-phase dip ride-through performance



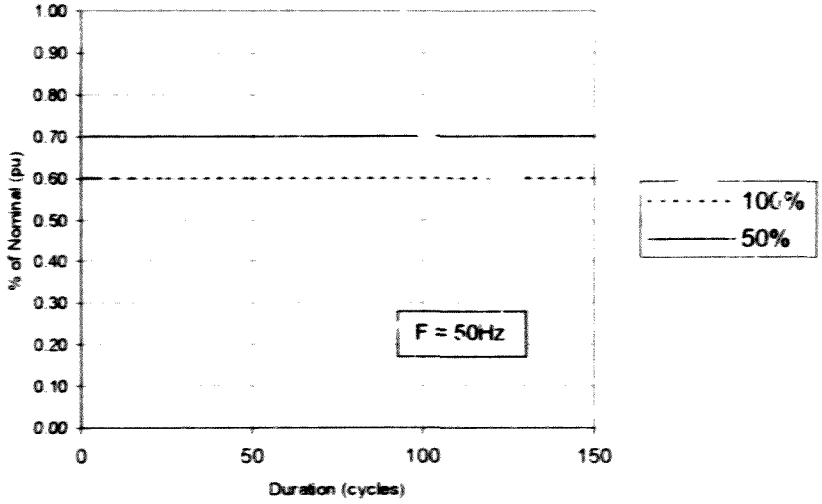
b) Red-phase dip ride-through performance



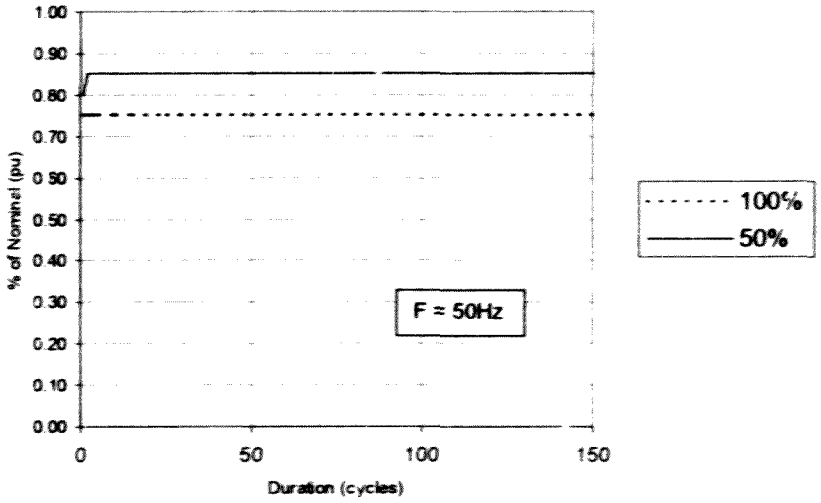
c) White-phase dip ride-through performance



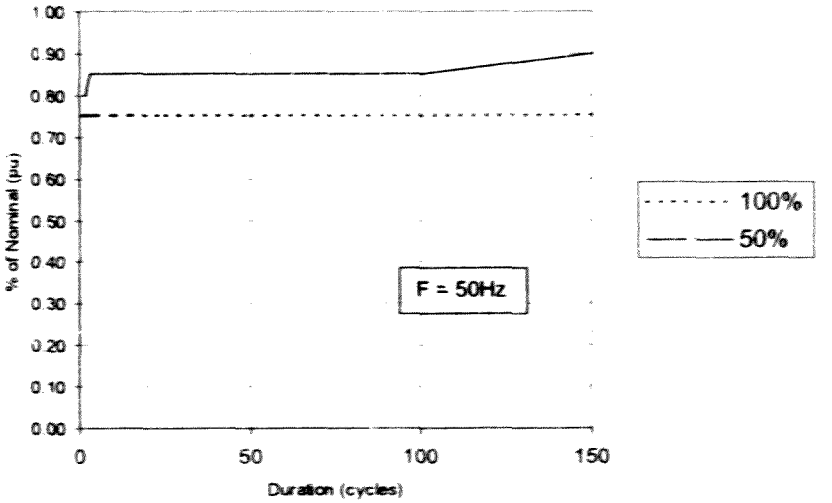
d) Blue-phase dip ride-through performance



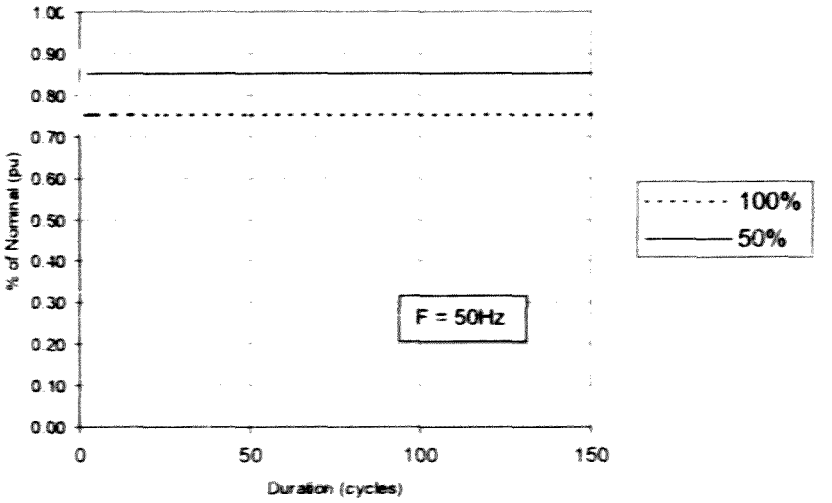
e) Red-white-phase dip ride-through performance



f) White-blue-phase dip ride-through performance



g) Red-blue-phase dip ride-through performance



The tests on this CSI drive showed some complex sensitivity results, which are a function of dip type and the phases that are affected. In comparison with the PWM drive, this drive is less sensitive to voltage magnitude variations and pre-dip voltage. This result was expected based on the principle of operation of CSI drives. It is also expected that phase angle variations will affect this drive more than PWM drives.

Going work will focus on attempting to quantify these interactions more accurately by additional testing and simulation.

C3 The Test Results For A DC Drive

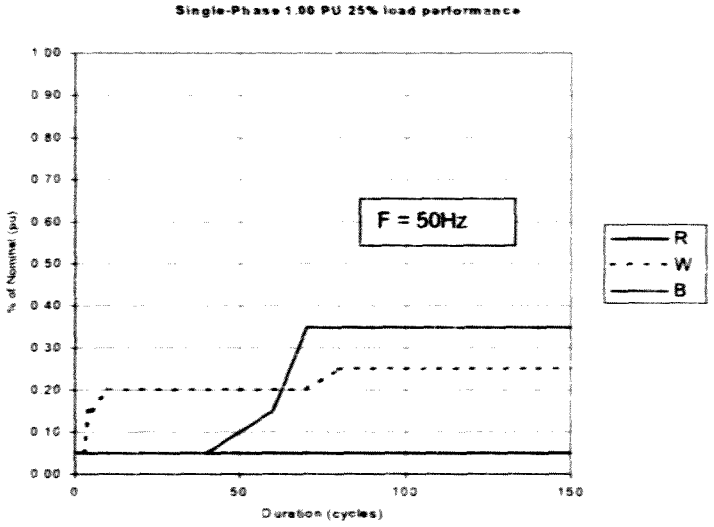
This section presents results from tests done on a digital DC variable speed drive. Loading has been set to 75% and 25% respectively. The DC drive test program is still ongoing. Results based on 25% loading are available and are presented here. Testing so far indicates that the drive gets its control information sensing off the AC input line using two of the phases. This is indicated by the complete immunity when one of the phases is dipped. When the other two are dipped, the drive would sometimes behave erratically as evidenced by current oscillations that result in overcurrent trips. The first tests done at 75% loading do not show this behaviour. This may indicate that the drive loading is a sensitive parameter and the drive should be properly matched to its load. The drive was also sensitive to changes in pre-dip voltage. This is shown as well. It was decided for safety reasons that a dip with a magnitude of more than 95%, would not be applied.

C3.1 Phase Comparisons

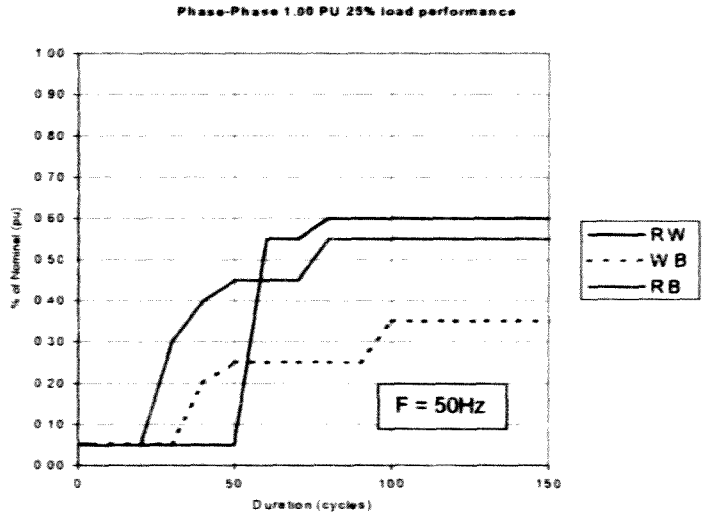
This is the comparison of the different phases when subjected to two-phase dips and single-phase dips at 1.0, 1.05 and 0.95 respectively.

Drive Performance At 1.0 P.U. Pre-dip Voltage

a) Single-phase dip ride-through performance

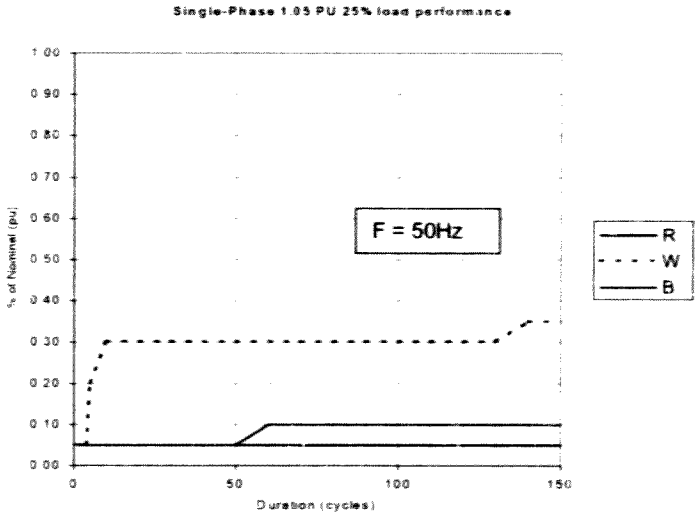


b) Phase-phase dip ride-through performance

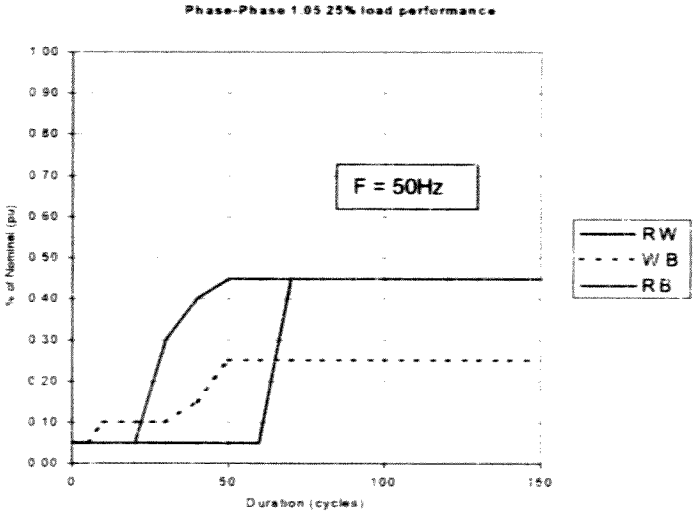


Drive Performance At 1.05 P.U. Pre-dip Voltage

a) Single-phase dip ride-through performance

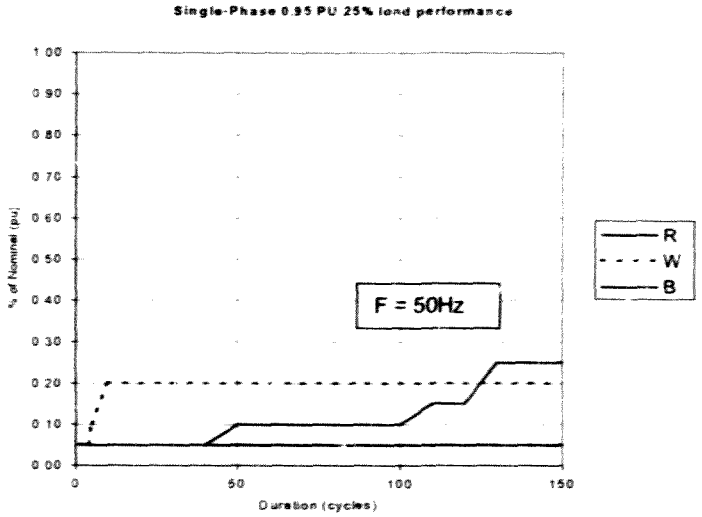


b) Phase-phase dip ride-through performance

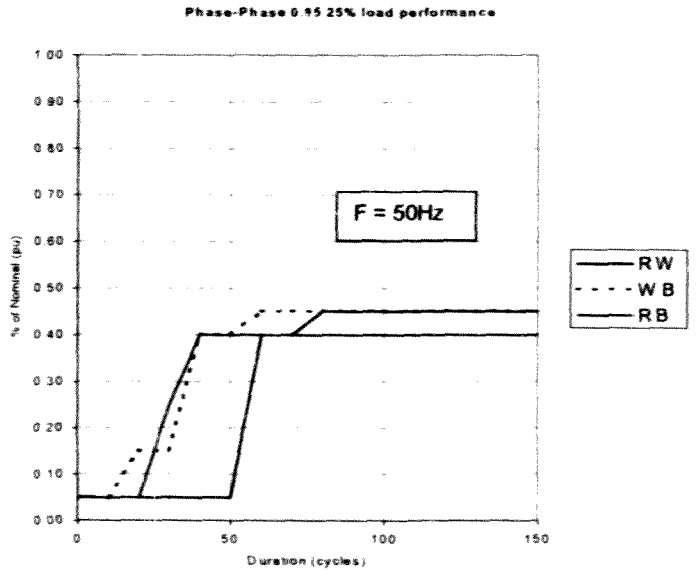


Drive Performance At 0.95 P.U. Pre-dip Voltage

a) Single-phase dip ride-through performance



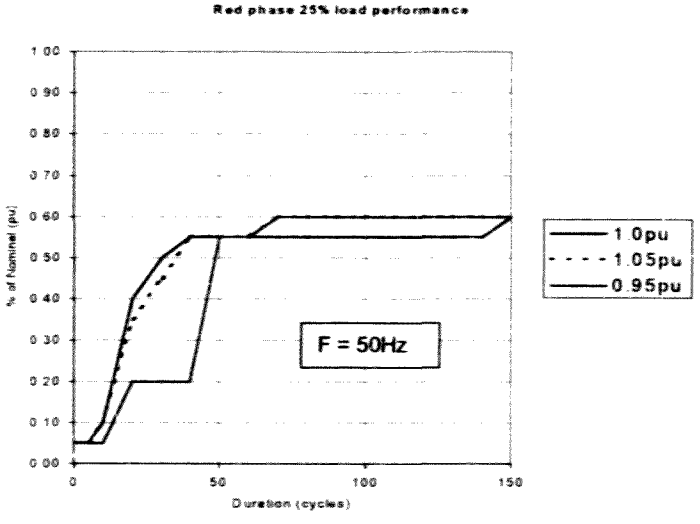
b) Phase-phase dip ride-through performance



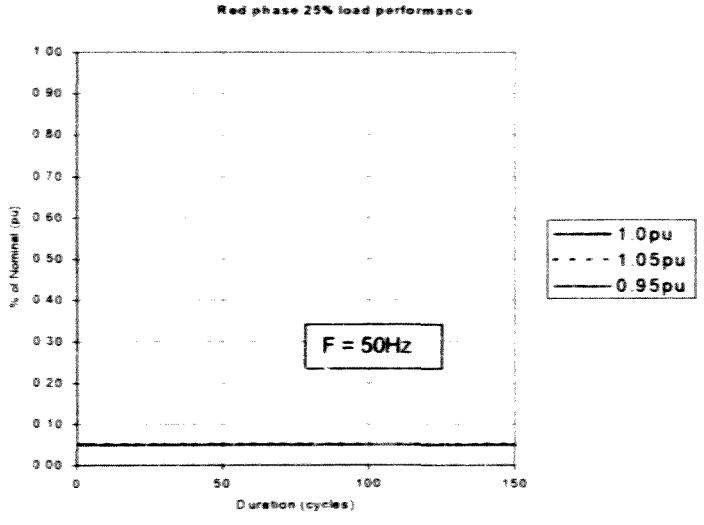
C3.2 Pre-Dip Voltage Comparisons

This is the comparison of different pre-dip voltages before applying three-phase dips, two-phase dips and single-phase dips.

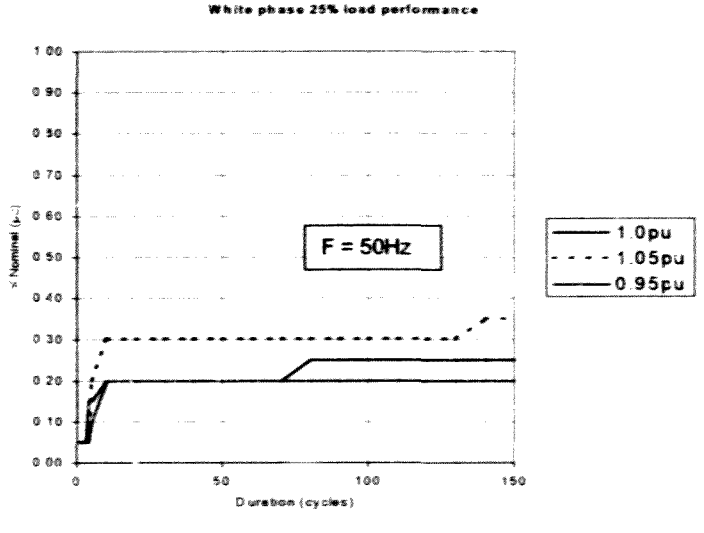
a) Three-phase dip ride-through performance



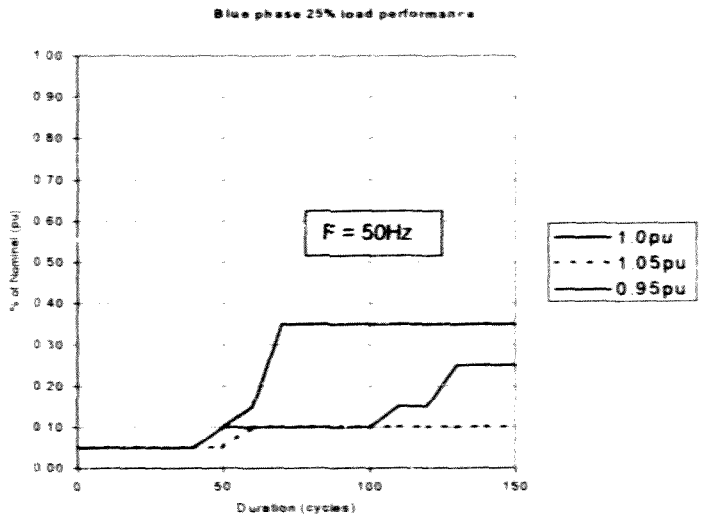
b) Red-phase dip ride-through performance



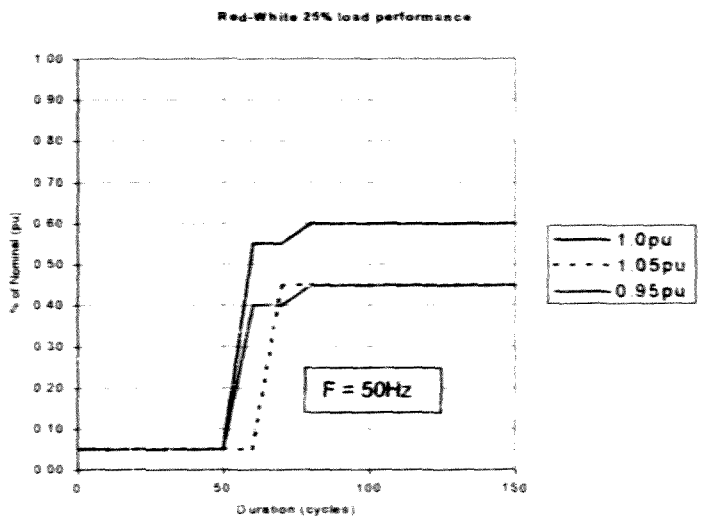
c) White-phase dip ride-through performance



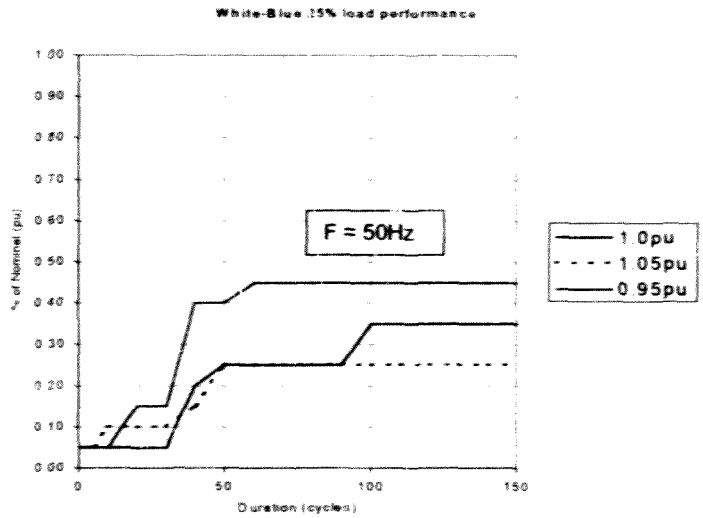
d) Blue-phase dip ride-through performance



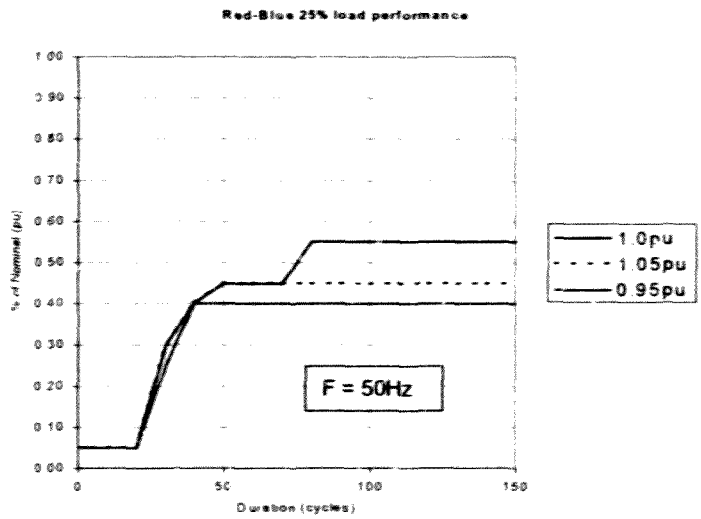
e) Red-white-phase dip ride-through performance



f) White-blue-phase dip ride-through performance



g) Red-blue-phase dip ride-through performance



APPENDIX D - SELECTED TEST WAVEFORMS

This Appendix contains selected waveforms that were captured during the testing of a PWM and CSI drive. These waveforms were captured to illustrate drive performance when there was either a trip, or drive ride-through. Complete sets of waveforms have been archived as data files as part of the testing requirements for further reference. This data includes at least every trip point that occurred during testing.

D1 Test Waveforms For A PWM Drive

Points of note during the test were:

- The supply voltage waveform was flat-topped when the drive was running (sinusoidal when the drive was off). An explanation for this is that when the drive is running, current is only drawn from the supply when the input voltage is greater than the DC bus voltage (rectifier diodes forward biased). The resulting non-linear current waveform and output transformer impedance result in a voltage drop that gives rise to the flat-topped supply waveform.
- The drive sometimes tripped on overcurrent. This was the case when it was running at 75% of rated load. It did not trip on overcurrent when running at 25% of rated load. The short dip recovery profiles for the voltage dips tested implied that a high output current was drawn by the motor from the drive during the recovery from the voltage dip. If the recovery time is increased, as is often the case in practice due to, for example, induction motors re-accelerating and increasing the recovery time, the drive would be less likely to trip on overcurrent.

Figures D1 to D7 show waveform results for a trip condition (3 phase; 0.95 pu pre-dip voltage; 40 ms dip duration; 0.86 pu dip voltage) and figures D8 to D14 for a ride-through condition (3 phase; 0.95 pu pre-dip voltage; 40 ms dip duration; 0.87 pu dip voltage).

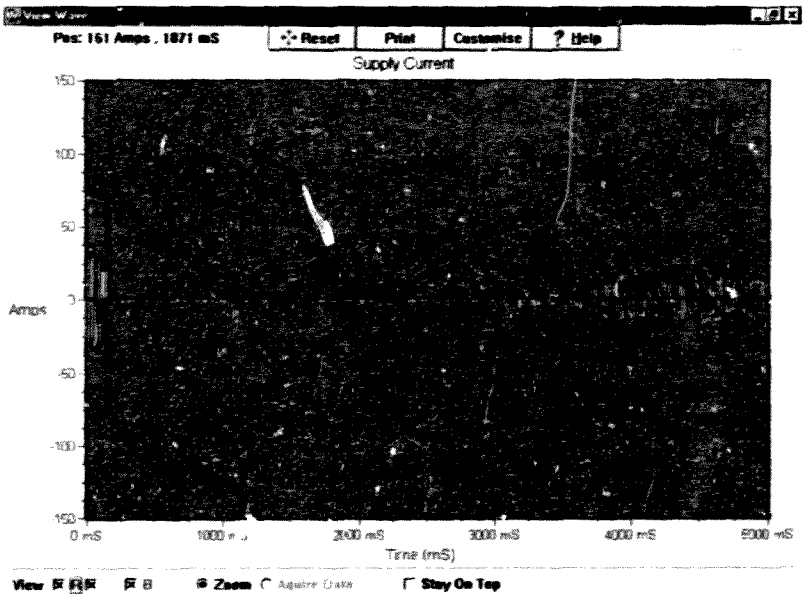


Figure D1 Supply current waveform for a trip condition and automatic restart.

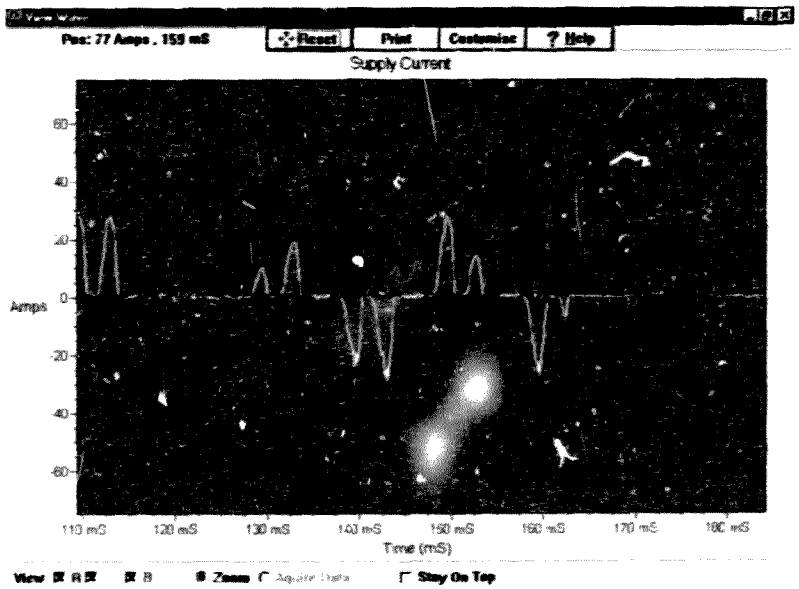


Figure D2 Supply current waveform (zoomed) for a trip condition.

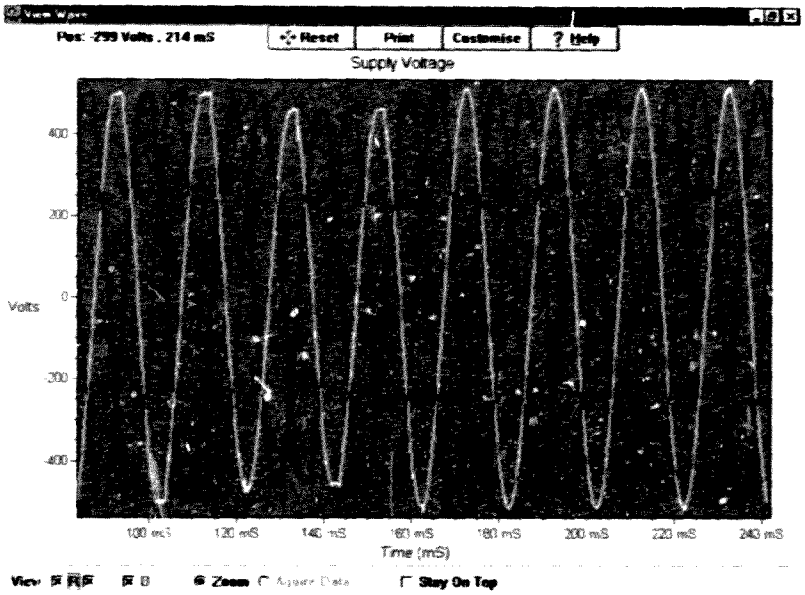


Figure D3 Supply voltage waveform for a trip condition. Note the less distorted voltage supply after the trip.

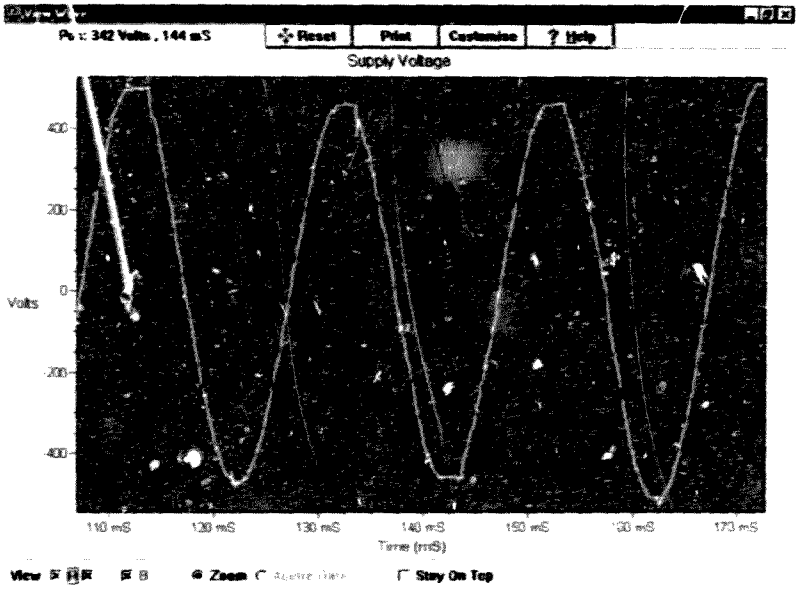


Figure D4 Supply voltage waveform (zoomed) for a trip condition.

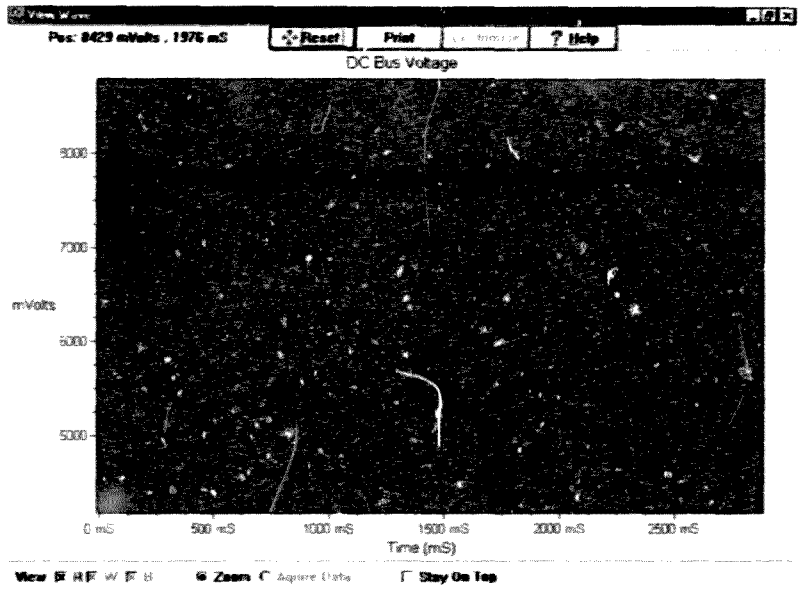


Figure D5 Supply voltage dc bus waveform for a trip condition.

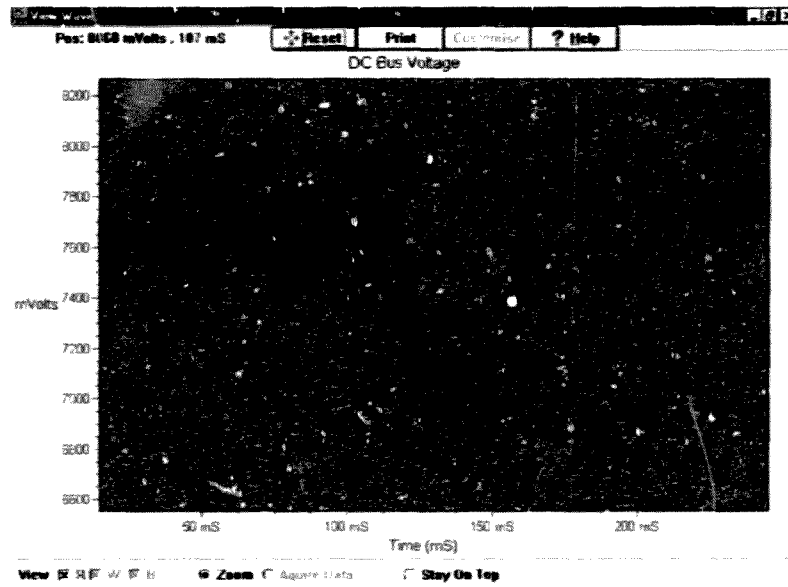


Figure D6 Supply voltage dc bus waveform (zoomed) for a trip condition. Note the 10% drop in the DC bus voltage.

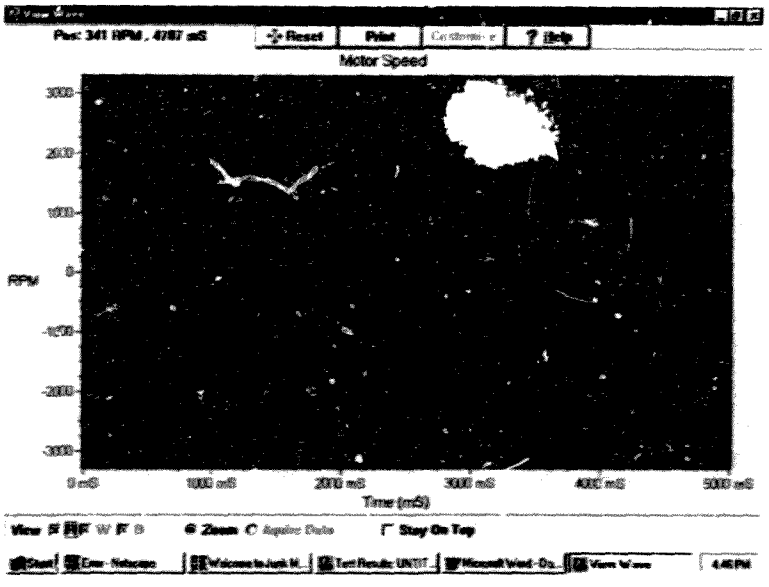


Figure D7 The speed waveform shows decreasing speed as the drive tripped after the dip.

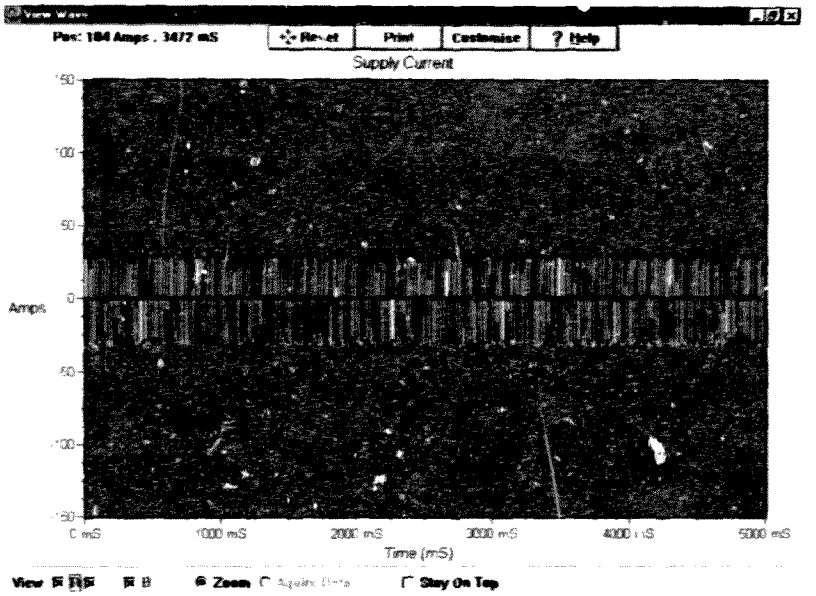


Figure D8 Supply current waveform for a ride-through condition.

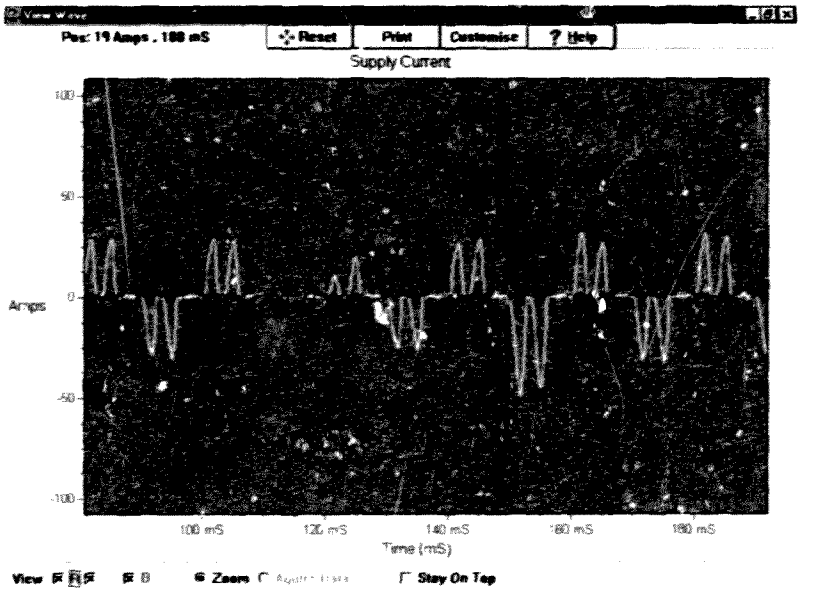


Figure D9 Supply current waveform (zoomed) for a ride-through condition

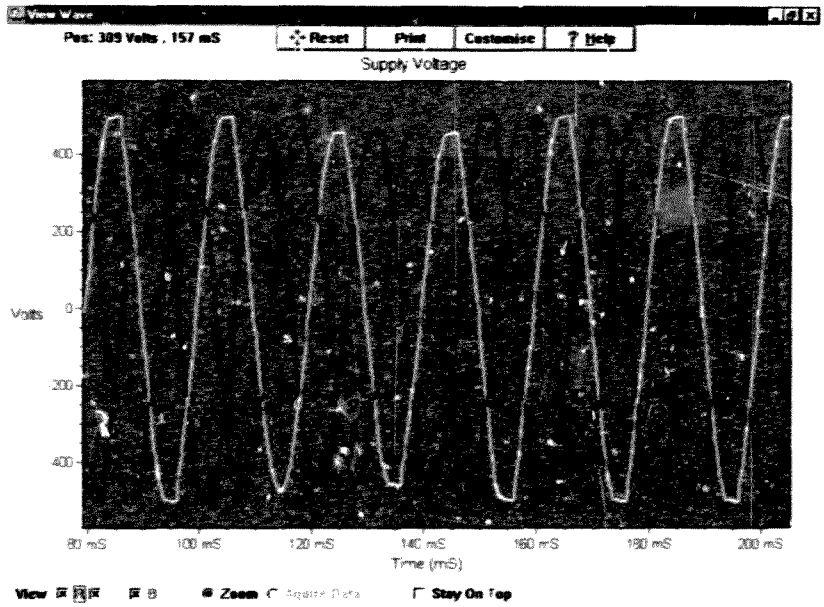


Figure D10 Supply voltage waveform for a ride-through condition. Note the distorted supply after the trip.

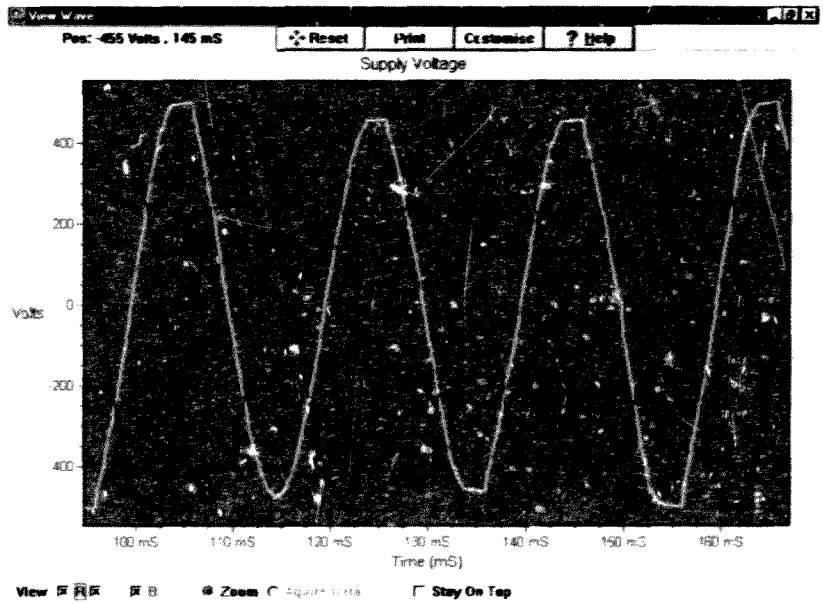


Figure D11 Supply voltage waveform (zoomed) for a ride-through condition.

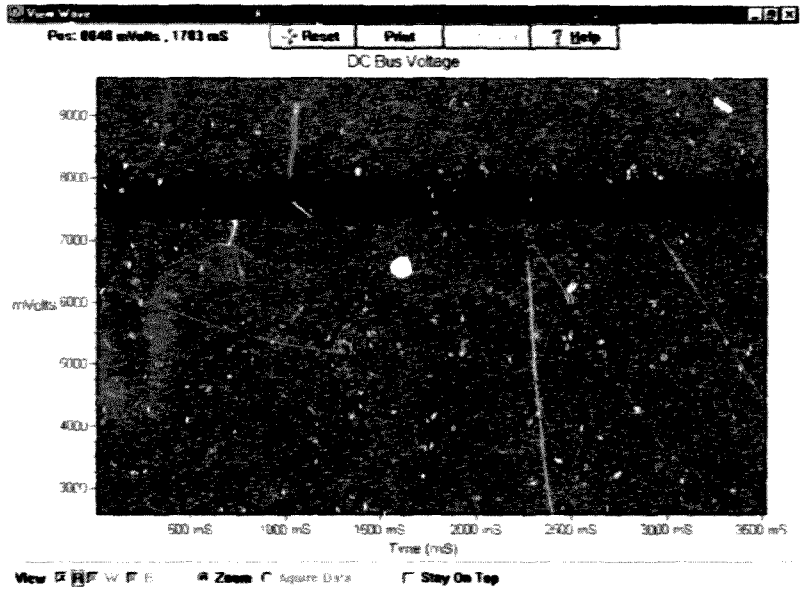


Figure I .2 Supply voltage dc bus waveform for a ride-through condition Note the distorted supply after the trip.

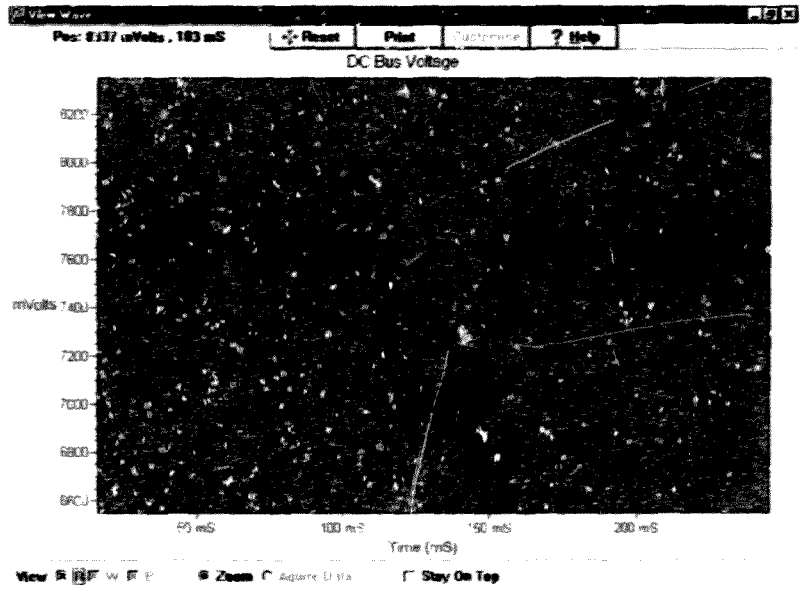


Figure D13 Supply voltage dc bus waveform (zoomed) for a ride-through condition

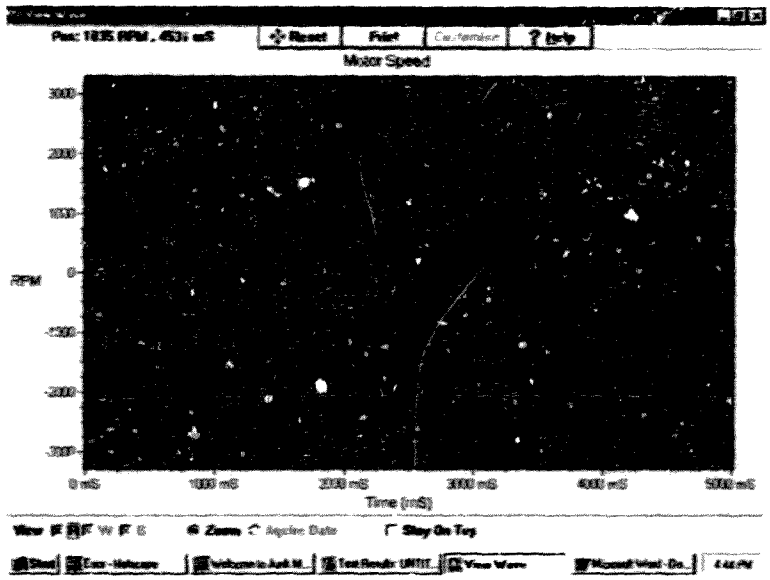


Figure D14 Speed curve for a ride-through condition.

An explanation for the current spike just after the dip is the rapid charging of the capacitors through the rectifier (see Figure D15) when the supply voltage recovers after the voltage dip. When the dip occurs, the peak supply voltage drops lower than that of the capacitor voltage and the supply current drops to zero (rectifier diodes reverse biased), explaining the zero current zone on the curves.

During the voltage dip, the capacitor voltage falls because the inverter section still runs, discharging the DC capacitors by drawing current from the DC bus. When the capacitor voltage drops below the peak input voltage, current is again drawn from the supply. As the supply recovers after the voltage dip, the capacitor is then rapidly charged with a large current (rectifier diodes forward biased) limited only by the supply impedance.

When the drive is initially switched on a current limiting resistor is in the circuit to charge the DC bus capacitors slowly and hence no current spike occurs. A timer

circuit shorts this resistor out a set time after the supply has been turned on. During a voltage dip if the inrush resistor remains short-circuited because the timer circuit is not reset, a current spike will occur when the voltage recovers with a short recovery time.

In practice a longer recovery time after a voltage dip implies the capacitors would charge over a longer time period with less of a current spike (charge transferred over a longer time period).

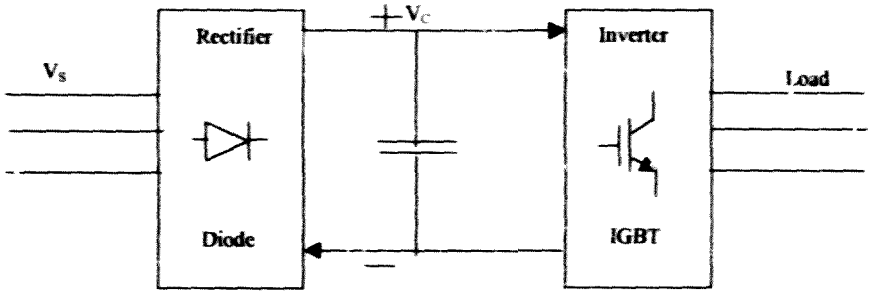


Figure D15 Block diagram of the VSD.

For the speed curves, the ride-through curve shows the speed is unaffected by the voltage dip. Notice in the trip curve that the motor slows down when the drive trips, but then slows down at a faster rate (at t=3.75s on the graph) when the drive re-starts. This is due to the drive restarting at zero frequency (non-synchronous restart).

D2 The Test Waveforms For A CSI Drive

Loading has been set to 100% and 50% respectively. The 100% and 50% load values are plotted on the same graph for the different voltage dips tested. The pre-dip voltage is 1.0pu for all cases.

The test waveform results are presented in the form of drive current and speed response waveforms.

An example of a drive trip is shown in Figure D16 for a white phase, 20 ms voltage dip. The crowbar action of the drive during this voltage dip was activated.

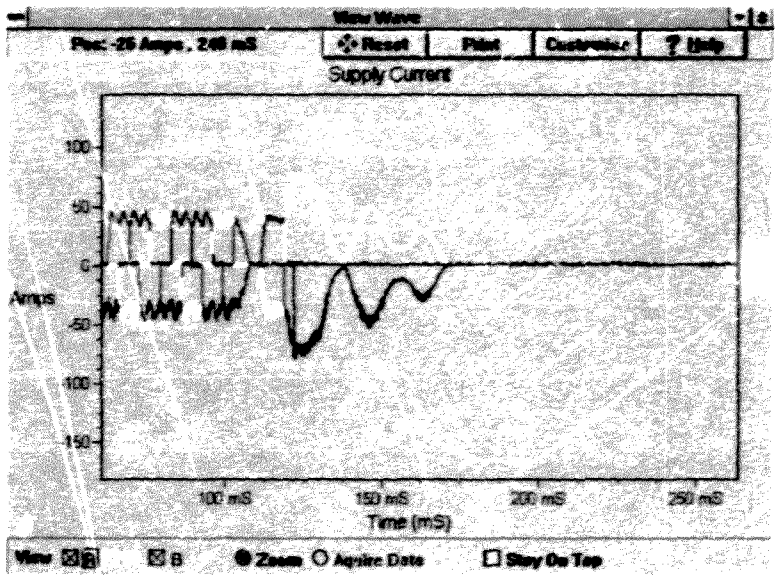


Figure D16 Drive input current waveform during a white phase, 20 ms dip (trip condition)

Figure D17 and Figure D18 show the drive input current and drive speed during a 3 phase, 20ms dip. The drive slows down to zero and then restarts after the dip.

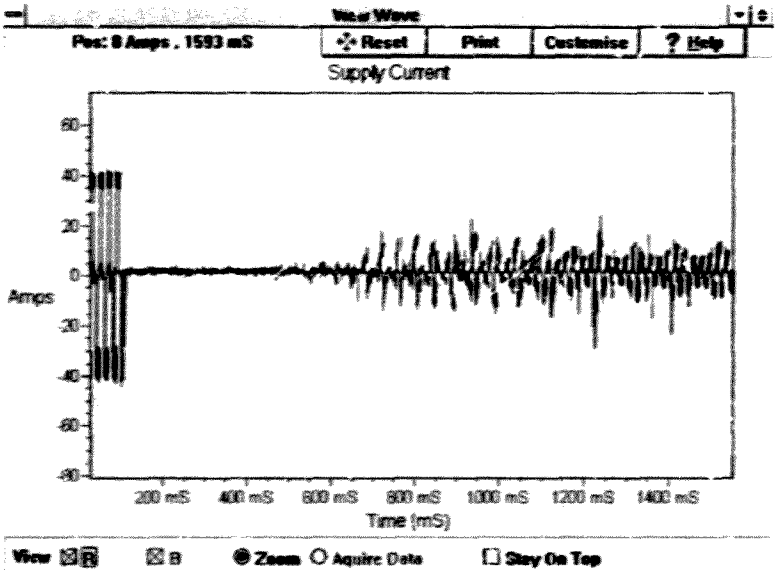


Figure D17 Drive input current waveform for a 3 phase, 20 ms dip

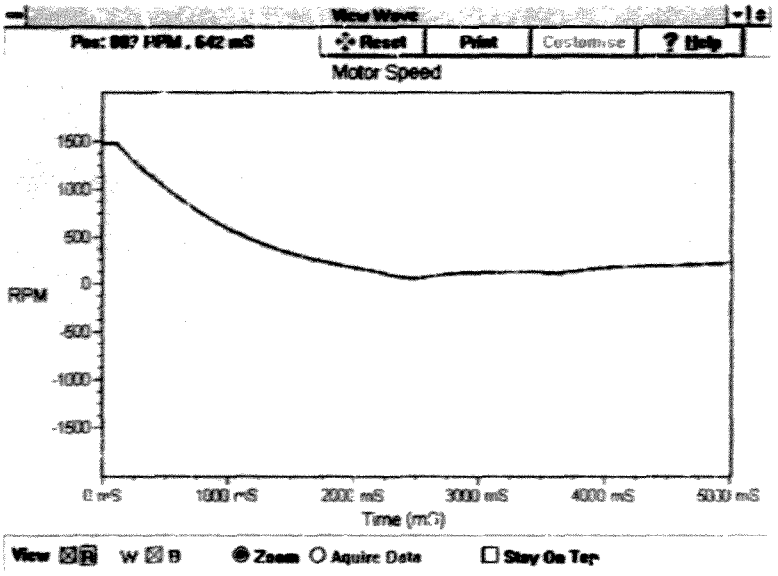


Figure D18 Drive speed waveform for a 3 phase, 20 ms dip

Figure D19 and Figure D20 show the drive input current and drive speed during a white phase, 3 second dip. During the dip, the drive goes into current limit and the motor slows down. When the supply voltage recovers after the dip, the drive trips due to a motor overvoltage.

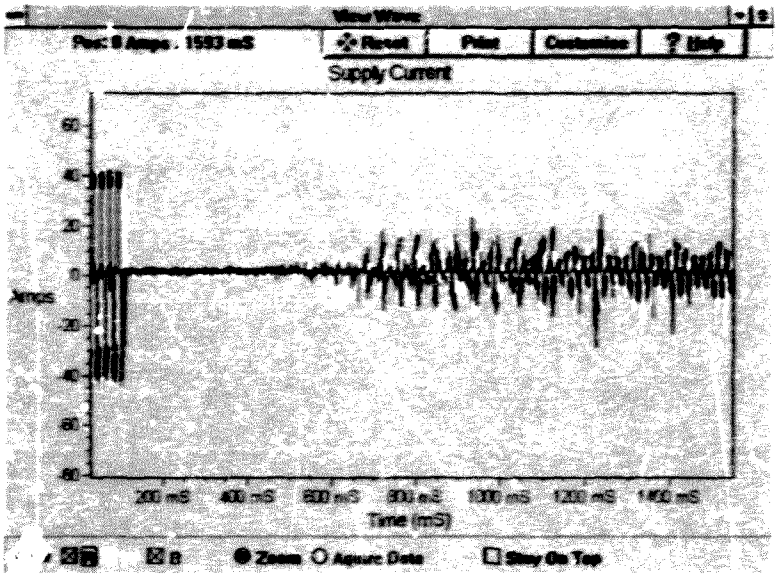


Figure D19 Drive input current for a white phase, 3 second voltage dip

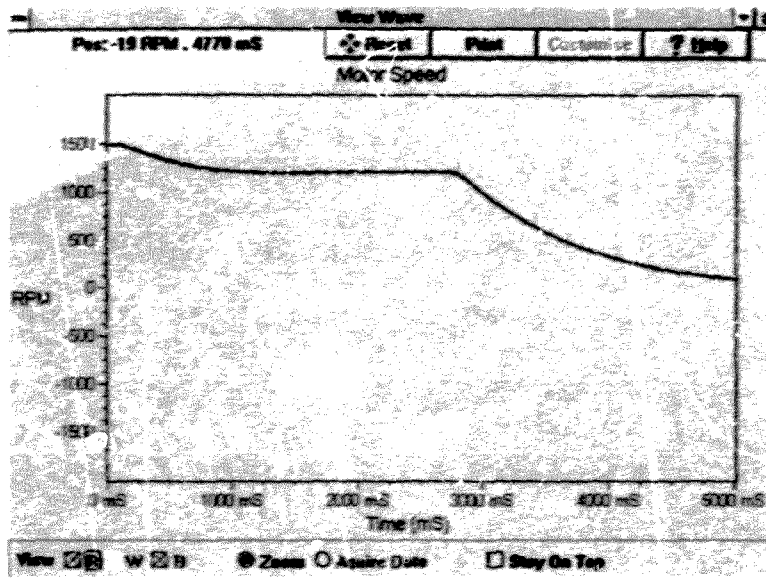


Figure D20 Motor Speed for a white phase, 3 second voltage dip