

https://dspace.org/

Reliability testing and upgrade of a low voltage power supply for the front-end electronics of the ATLAS Tile Calorimeter Phase-II Upgrade

Nkadimeng, Edward Khomotso

2022

https://hdl.handle.net/10539/37147

Downloaded from a DSpace repository. https://dspace.org/

Reliability testing and upgrade of a low voltage power supply for the front-end electronics of the ATLAS Tile Calorimeter Phase-II Upgrade



Author:
Edward Nkadimeng

Supervisor:
Prof. Bruce Mellado

A thesis submitted to the Faculty of Science, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Doctor of Philosophy

March 31, 2022

Declaration

I, Edward Nkadimeng, (Student number: 1802990) declare that this thesis titled, "Reliability testing and upgrade of a low voltage power supply for the front-end electronics of the ATLAS Tile Calorimeter Phase-II Upgrade", is submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy, represents my own work except where appropriate acknowledgement has been given. I hereby make the following declarations:

- I am aware that plagiarism (the use of someone else's work without their permission and/or without acknowledging the original source) is wrong.
- I confirm that the work submitted for assessment for the above degree is my own unaided work except where I have explicitly indicated otherwise.
- I have followed the required conventions in referencing the thoughts and ideas of others.
- I understand that the University of the Witwatersrand may take disciplinary action against me if there is a belief that this is not my own unaided work or that I have failed to acknowledge the source of the ideas or words in my writing.
- I have written about and presented many of the ideas and results in this thesis. A list of my previous works that have done so is shown on page.
- I, along with the other co-authors, have intellectual property of these works.
- I further declared that it has not been previously included in a thesis, dissertation, or report submitted to this University or to any other institution for a degree, diploma or other qualifications.

Signed: 

Date: March 31, 2022

Acknowledgements

Throughout the start of the project to submission of this dissertation, I have received a great deal of support and assistance. Prof. Bruce Mellado, my advisor, whose experience was helpful in designing the research topics and techniques, deserves my heartfelt gratitude. Your informative remarks encouraged me to improve my thoughts and raise the quality of my work. Working on this project has provided me with a tremendous amount of experience. I'd like to thank my colleagues at the University of Witwatersrand, particularly the following individuals:

- Ryan Mckenzie
- Thabo Lepota
- Nkosi Njara
- Othmane Moune
- Roger van Rensburg

as well as the ATLAS TileCal group for the wonderful collaboration, with special mention of the following people:

- Seyedali Moayedi,
- Stanislav Nemecek,
- Christophe Clement,
- Pavel Stravoitov

I want to thank you all for your patient support and all of the opportunities I was given to further my research. On a personal note, I would like to thank my parents and brother for their wise counsel and sympathetic ear. Albertina Nkadimeng, Silas Nkadimeng, and Vuyo Nkadimeng, you have always been there for me. In addition, the support of the NRF/iThemba LABS is acknowledged, for awarding me the prestigious South African Institute of Nuclear Technology scholarship.

List of Publications

JOURNALS:

[1] **Nkadimeng E**, "A monitoring and control test bench for assessing the upgraded low voltage power supplies for the ATLAS Tile Calorimeter Phase-II Upgrade front-end electronics", Journal of Instrumentation (JINST), February 2022, Submitted to Journal for review and publication.

[2] Mouane O, **Nkadimeng E**, "Heat Conduction Enhancement of a Thermal Interface Material for Heat Sink Applications Using Carbon Nanomaterials", (TNANO-00032-2022), in IEEE Transactions on Nanotechnology, January 2022, "Submitted to Journal for review and publication."

CONFERENCES:

[1] **Nkadimeng E**, Performance of the Tile Calorimeter Demonstrator system for the ATLAS Phase-II Upgrade, in the International Conference on Large Hadron Collider Physics (LHCP2021), Paris, France, June 2021.

[2] **Nkadimeng E**, Re-designing a radiation-tolerant low voltage power supply for the ATLAS Tile Calorimeter Phase-II Upgrade, South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021, Accepted for publication.

[3] **Nkadimeng E**, Quality control software development for testing the next generation of upgraded low voltage power supplies for the ATLAS Tile Calorimeter, in South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[4] Mckenzie R, **Nkadimeng E**, A Burn-in test station for the ATLAS Phase-II Tilecalorimeter low-voltage power supply transformer-coupled buck converters, in South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[5] Mckenzie R, **Nkadimeng E**, Quality assurance testing of the ATLAS Tile Calorimeter Phase-II upgrade low-voltage power supplies, in South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[6] Mouane O, **Nkadimeng E**, Heat Transfer Improvement of a Thermal Interface Material for Heat Sink Applications Using Carbon Nanomaterials, in South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[7] Lepota T, **Nkadimeng E**, The characterization and functionality of the interface boards used on the Burn-in test station for the ATLAS Tile Calorimeter Low Voltage Power Supplies phase II upgrade, in the South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[8] Njara N, **Nkadimeng E**, Programming a Load readout board for the Burn-In test bench of the ATLAS Phase-II Upgrade, in the South African Institute of Physics (SAIP 2021), North-West University, South Africa, September 2021. Accepted for publication.

[9] **Nkadimeng E**, "Reliability testing of a Low Voltage Power Supply (LVPS) and test station design for the Front-End Electronics of the ATLAS Tile Calorimeter", CERN-Fermi Lab Summer School (CERN-FERMI LAB 2021)), Europe (Virtual), August 2021, Accepted for publication.

[10] **Nkadimeng E**, "Low Voltage Power Supply (LVPS) upgrade of the Phase-II Front-end system, in the South African Institute of Physics (SAIP 2019), University of Venda, South Africa, June 2019, Accepted for publication.

Abstract

The LHC is planned to deliver five times the nominal instantaneous luminosity in the High-Luminosity LHC (HL-LHC). To address the projected greater detector occupancies and harsher radiation environment at the HL-LHC, considerable upgrades to most of the ATLAS detector sub-systems are required. The Phase-II Upgrade is planned to last approximately three years and is scheduled for 2026-2029. The ATLAS Tile Calorimeter (TileCal) will require the complete replacement of the readout electronics in order to accommodate its acquisition system to the increased radiation levels, trigger rates, and high pile-up conditions during the HL-LHC period. The Phase-II upgraded readout electronics will digitize the PMT signals from every TileCal cell for every bunch crossing and will transmit them directly to the off-detector electronics. In the counting rooms, the off-detector electronics will store the calorimeter signals in pipe-lined buffers while transmitting reconstructed trigger objects to the first level of trigger at 40 MHz. The replacement of the on-detector and off-detector read-out electronics for increased resolution, trigger performance, and radiation tolerance for the HL-LHC operation conditions is a major part of the Phase-II TileCal upgrading activities. The TileCal upgrade project has undergone an extensive research and development program as well as several test beam campaigns. Wits University's Institute for Collider Particle Physics is responsible for 50% (1024 units) of the total upgrade low voltage power supply transformer-coupled buck converter (Bricks) that delivers 10 V to the front end system. In the year 2022, a large-scale production and testing is planned for around 1024 radiation-tolerant power supplies with the same output voltage. The LVPS Brick V7.5.0 currently installed within the Tile Calorimeter will be completely replaced as part of this production. The LVPS Bricks are located within the TileCal's inner barrel and their operational reliability is off critical importance. As a result, performance screening will be implemented, which will include testing and certification of all LVPS Bricks manufactured. Radiation tests for Total Ionizing Dose (TID), Non-Ionizing Energy Losses (NIEL), and Single Event Effects (SEE) were also carried out to evaluate the radiation tolerance strategies used in the design and to qualify the LVPS Brick for the HL-LHC requirements, as per the ATLAS policy on radiation tolerant electronics.

Author's Contribution

This thesis is the result of the author's contribution as part of the University of the Witwatersrand, Institute of Collider Particle Physics towards the ATLAS Upgrade. The author was particularly involved in the Phase-II Upgrade activities of the Low Voltage Power Supply system. The author was also heavily involved in the development, testing and integration of both the Low Voltage Power Supply (LVPS) Brick and testing stations that will be used for quality assurance and validation. The author participated in several radiation campaigns, contributed to the design of the setups for the different tests, and the development of firmware and scripts used to retrieve the data. Additionally, the author contributed to processing and analyzing the data obtained from the various tests. This manuscript complements all the published work mentioned in the List of Publications, with broader descriptions of the R&D work done and results obtained. Journal Papers 1, 2 and Conference papers 1-5, 11 and 12, were written, edited and submitted by the author. While 8-11 were co-authored by the thesis author. Many tests and extensive development took place to assure that the LVPS will be compatible with the Phase-II front-end electronics. Some results of this work are described by the author briefly in paper 1-4 and more broadly in chapters 4-7. The author provided timely firmware updates for micro-controllers used for the development of a Burn-In test station, in addition to hardware installment, servicing and calibration testing. The author's work on the integration of the LVPS to the Demonstrator project resulted in the successful results from the data taken during the TestBeam campaigns in 2021. Furthermore, the author was invited to co-convene the official LVPS and LVPS DCS meetings. The author contributed to integrate and test the produced boards in test-benches that allowed the different design changes to be tested on each iteration. Additionally, the author's contribution to the radiation tests to the latest LVPS revision is described in chapter 7. This thesis presents the author's contribution to the development of the LVPS through the different revisions, the quality assurance testing and integration of the Wits LVPS Bricks to the Phase-II Upgrade and the radiation tests performed aiming to demonstrate the readiness of the LVPS Brick to withstand the radiation requirements imposed by the HL-LHC.

Contents

Declaration **i**

Acknowledgements **ii**

List of Publications **iii**

Abstract **v**

Author's Contribution **vi**

List of Figures **xi**

List of Tables **xvi**

List of Abbreviations **xvii**

List of Symbols **xx**

1 Introduction **1**

1.1 The Standard Model of particle physics 1

1.1.1 Particles in the Standard Model 1

1.1.2 Electroweak Interaction 3

1.1.3 Quantum chromodynamics 5

1.2 The Large Hadron Collider and its experiments 5

1.2.1 LHC upgrade for the high luminosity era 7

1.3 The ATLAS Experiment facing the High Luminosity LHC 9

1.3.1 ATLAS detector overview and coordinate system 9

1.3.2 Particle detection on the ATLAS detector 10

1.3.3 Muon Spectrometer 11

1.3.4 Inner Detector 12

1.3.5 The Pixel Detector 12

1.3.6 The Semiconductor Tracker 13

1.3.7 The Transition Radiation Tracker 14

1.3.8 Magnet System 14

2 The Tile Hadronic Calorimeter system **16**
2.1 Liquid Argon Calorimeter . . . 16
2.2 Hadronic Calorimeter overview . . . 17
2.2.1 Tile Calorimeter . . . 17
2.3 Current Superdrawers and front-end electronics . . . 18
2.3.1 PMT Blocks . . . 19
2.3.2 3-in-1 cards . . . 20
2.3.3 The Level-1 trigger summation boards . . . 20
2.3.4 The 3-in-1 Motherboard . . . 20
2.3.5 Digitizer Board . . . 21
2.3.6 Interface Board . . . 21
2.3.7 High Voltage Power Supply . . . 21
2.3.8 Low Voltage Power Supply . . . 21
2.3.9 Charge calibration system . . . 22
2.3.10 Laser calibration system . . . 22
2.3.11 Cesium source calibration system . . . 22
2.4 Trigger and Data Acquisition . . . 22

3 The Phase-II Upgrade programme for the HL-LHC **24**
3.1 Phase-II Upgrade overview . . . 24
3.2 TileCal Phase-II Upgrade . . . 25
3.3 Phase-II upgrade readout electronics . . . 28
3.3.1 Mechanics . . . 28
3.3.2 Photomultiplier blocks . . . 28
3.3.3 Front End board . . . 28
3.3.4 Mainboard . . . 29
3.3.5 Daughterboard . . . 29
3.3.6 High Voltage Power Supply . . . 29
3.3.7 Low Voltage Power Supply . . . 30
3.4 Back-end electronics . . . 30
3.5 Demonstator Project . . . 31
3.5.1 Demonstrator system and readout chain . . . 32

4 TileCal Low Voltage Power Supply System **34**
4.1 Low Voltage Power Supply . . . 34
4.1.1 Power Distribution system . . . 35
4.1.2 Environmental Constraints . . . 36
4.2 fLVPS components . . . 37
4.2.1 ELMB motherboards . . . 37
4.2.2 Low Voltage boxes . . . 37
4.2.3 AUX Boards . . . 38

4.2.4 Upgrade LVPS Brick description and design . . . 38
4.2.5 Improvements of latest prototype . . . 40
Real-time monitoring of LVPS Brick . . . 40
Thermal management . . . 41
Tri-State Control method testing . . . 41
Overall performance and reliability analysis . . . 42

5 Quality assurance testing of the Low Voltage Power Supply Brick 45
5.1 Pre-production and production checkout . . . 45
5.2 LVPS test bench . . . 46
5.3 Automated testing software . . . 47
5.3.1 Description and functionality of tests . . . 47
5.4 Monitoring and control results . . . 51
5.5 Summary of test bench results . . . 52

6 Software and Firmware development for a Burn-In test bench 54
6.1 Accelerated aging of the low voltage power supply . . . 54
6.2 Burn-In test bench development at WITS . . . 55
6.2.1 Burn-In test bench . . . 55
6.3 Software development for Burn-In bench Electronics . . . 56
6.3.1 Mainboard . . . 57
6.3.2 Brick Interface Board . . . 57
6.3.3 Dummy Load board . . . 58
6.3.4 Dummy Load Interface board . . . 58
6.3.5 Embedded Firmware . . . 58
6.4 Burn-In test procedure . . . 59
6.5 Preliminary Burn-In results . . . 60
6.6 Burn-In test bench Summary . . . 61

7 Radiation tests performed on the Low Voltage Power Supply Brick 62
7.1 Radiation interaction with matter . . . 62
7.1.1 Interactions of photons with matter . . . 62
7.1.2 Interactions of charged particles with matter . . . 64
7.1.3 Interactions of neutrons with matter . . . 65
7.2 Radiation effects on electronics and semiconductor devices . . . 67
7.3 TileCal Radiation requirements for HL-LHC . . . 70
7.4 Radiation Testing of the LVPS Brick prototypes . . . 70
7.4.1 Total Ionizing Dose testing . . . 71
TID Results . . . 71
7.4.2 Non-Ionizing Energy Loss testing . . . 73
7.4.3 NIEL Results . . . 73

7.4.4 SEE testing . . . 74
7.4.5 SEE Results . . . 75
7.5 Irradiation Studies Summary . . . 76

8 Conclusions **80**
8.1 LVPS project summary . . . 80
8.1.1 Brick Design and production . . . 81
8.1.2 Functional testing . . . 81
8.1.3 Burn-in testing . . . 81
8.1.4 Radiation testing . . . 82
8.2 Discussion and prospects . . . 82

A Schematics and Tri-State control simulations **83**

B Test benches set up and results **90**

C Radiation Set up and Results **101**

D Database Development **105**

Bibliography **107**

List of Figures

1.1 The fermionic particle content currently explained in the SM, with their associated masses in parentheses. All quoted masses are taken from Reference [7, 8, 9, 10]. The errors have been omitted for significantly precise measurements. 2
1.2 CERN accelerator complex with Large Hadron Collider (LHC), Super Proton Synchrotron (SPS), Proton Synchrotron (PS), Antiproton Decelerator (AD), Low Energy Ion Ring (LEIR), Linear Accelerators (LINAC), CLIC Test Facility (CTF3), CERN to Gran Sasso (CNGS), Isotopes Separation on Line (ISOLDE), and neutrons Time of Flight (n-ToF) LHC [5]. 6
1.3 The ATLAS Detector and its detector subsystems from the LS0 ATLAS layout. (1) Muon Detectors; System of magnets: (2) Toroid Magnets and (3) Solenoid Magnet; Inner Detector: (4) Transition Radiation Tracker, (5) Semi-Conductor Tracker and (6) Pixel Detector; Calorimeters: (7) Liquid Argon Calorimeter and (8) Tile Calorimeter. The inner beam line (IBL) and New-Small-Wheel (NSW) are seen on both ends of the detector [29]. . . . 9
1.4 ATLAS Detector Particle detection schematic [1]. 10
1.5 The Muon Detector [33]. 12
1.6 ATLAS Inner Detector [29]. 13
1.7 Assembly view and cross-section of an ATLAS Pixel Detector module (left) and the Schematic drawing of the ATLAS Pixel Detector (right) [34]. The IBL is not included in the image. 14

2.1 The Liquid Argon Calorimeter [36]. 17
2.2 The Hadronic Tile Calorimeter [34]. 18
2.3 TileCal wedges, optical components, drawers and on-detector electronics distribution [34]. 19
2.4 The Drawer distribution interfacing between on-detector and off-detector electronics. Digitizer blocks are used to represent 3-in-1 Motherboards and digitizer boards for ease of use [34]. 20
2.5 The ATLAS TDAQ system with three levels of event selection [31, 40]. . . 23

3.1 Phase-II Upgrade electronics diagram [30]. 25
3.2 A general segmented image of TileCal [34]. 26

3.3 TileCal read-out cell mapping for contiguous long barrel (LB) and extended barrel (EB) wedges. This cell distribution is symmetric respect to the interaction point [34]. 27
3.4 Drawer distribution of TileCal upgrade and interface between on-detector and off-detector electronics [49]. 30
3.5 Drawer distribution of the Demonstrator and interface between on-detector and off-detector electronics [49, 51]. 31
3.6 Picture of the Tile PreProcessor Demonstrator [55]. 32

4.1 TileCal power distribution block diagram. Top left includes the Minidrawer power distribution. Bottom left is the updated 3 phase power distribution scheme. Top right is the image of the LVPS Brick and bottom right is the LVPS Box or fLVPS. 35
4.2 LVPS Brick circuitry block diagram. 38
4.3 WITS LVPS Brick prototype (top side). 39
4.4 WITS LVPS Brick prototype (bottom side). 40
4.5 Two dimensional temperature maps of a +10 V Brick operating at 2.3 A with thermal coupling with Aluminum Oxide thermal coupling. These maps have been obtained with the application of a Bergquist gap-pad on the LT1681 [58] and FET drivers. Thermal reading of the previous 8.1.0 version of the power supply (left) and the Thermal reading of current 8.4.2 version of the power supply (right). 41
4.6 Simulation of 15 V start up pulse input and 15 VDC Tri-State. 43
4.7 Simulation of 15 V start up pulse input and 0 VDC Tri-State. 44

5.1 Test station block diagram. 47
5.2 Individual Brick test stand for testing and real time monitoring of LVPS Brick behaviour. 48
5.3 Test panel to perform various tests (left) and the manual control feature on a graphical user interface (right). 50
5.4 The test monitors the output voltage of the LVPS Brick. Permitted values for all the Bricks should be within the 3σ range. The test recorded for 10 minutes. 51
5.5 Temperature measurements taken for continuously for 30 minutes. B6 (left), C1 (right) thermistor measurements located on the LVPS prototype Bricks. 52

6.1 Bath-tub curve [69, 70]. 55
6.2 Burn in hardware block diagram [71]. 56
6.3 Burn-In Test bed. 57
6.4 Simplified LabVIEW control program execution diagram. 58

6.5 Burn-In procedure [71]. 60
6.6 Thermal images for the LVPS Brick (left) and Dummy Load Board (right) undergoing Burn-In testing. 61

7.1 The Auger process from two perspectives. (a) depicts the Auger de-excitation process in two steps. In the 1s level, an incident photon (or electron) creates a core hole. The transition energy is transferred to a 2p electron that is emitted when an electron from the 2s level fills in the 1s hole. As a result, there are two holes in the final atomic state, one in the 2s orbital and the other in the 2p orbital. (b) uses X-ray notation to depict the same process, K L1, L2, L3 [79]. 63
7.2 The relative contribution of various processes of photonic radiation interaction with matter [78]. 64
7.3 Fractional energy loss per radiation length in lead as a function of electron or positron energy [16]. 65
7.4 Characteristic neutron damage function for Silicon [80]. 66
7.5 Characteristic neutron damage functions for Silicon [81, 82]. 67
7.6 On the left: Total ionizing dosage in Gy/4000 fb^{-1} in the tracking and calorimeter regions of the Phase-II ATLAS detector. On the right: Displacement damage in silicon, expressed as the corresponding fluence of 1 MeV neutrons with an integrated luminosity of 4000 fb^{-1}. For both images the minimum-bias pp events are simulated with Pythia 8 at 14 TeV centre of mass energy assuming an inelastic cross section of 80 mb. The GEANT3/GCALOR code is used to model particle tracking and interactions with material using the latest geometry description of the Phase-II ATLAS detector. In azimuth, the geometry model is symmetric, with z = 0 [34]. 69
7.7 Picture of the LVPS Brick (Left) and Interface Board (Right) in the cobalt-60 test facility at CERN. 72
7.8 Output Current (A) left and output voltage (V) right of the LVPS monitored during irradiation testing at the ^{60}Co facility. 73
7.9 Output Current (A) and output voltage (V) of the LVPS monitored during irradiation testing at the Ljubljana, TRIGA reactor. 74
7.10 Output Current (A) and output voltage (V) of LVPS Brick 1 monitored during irradiation testing at the Ljubljana, TRIGA reactor. 75
7.11 Isolation amplifier Board being set-up for irradiation. 76
7.12 Instability with Isolation amplifier. 77

7.13 Irradiated Chip U1 and U2 performance. The results from Chip U1 show that in the first run, the output voltage goes to zero, which was then fixed by a power cycle to zero, which was then fixed by a power cycle. The chip survived the test after receiving 400 Gy. The results from Chip U2 show that the output voltage had some fluctuations during all the runs, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy. 78
7.14 Irradiated Chip U3 and U4 performance. The results from Chip U3 show that this chip almost behaved like the reference chip during the whole test. The chip also survived the entire dose of 400 Gy. The results from Chip U4 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the beginning of each run. The fluctuations did not stop when the beam was stopped at the end of each run (a power cycle was needed). After the last run (receiving 400 Gy), the chip stopped working properly (due to TID effects), and even the two power cycles did not fix the issue. 79
7.15 Irradiated Chip U7 and U11 performance. The tests were performed in 4 runs, and there were a power cycle between each two consecutive runs. There were also two power cycles at the end of the tests, just to see if any of the faulty chips will behave correctly after power cycle, or if any working chip will continue to work.The results from Chip U9 show that this chip almost behaved like the reference chip and did not have any large fluctuations. The chip also survived the full radiation dose of 400 Gy. The results from the reference chip (chip U11) shows that this chip behaved completely normal during the test. 79

A.1 LVPS V8.5 Schematic. 84
A.2 Schematics IR2110. 85
A.3 Schematics MOSFET. 86
A.4 Schematics SI8920. 87
A.5 Tri-State control method at 15V DC. 88
A.6 Tri-State control method at 0V DC input. 89

B.1 Test stand log results of measured HE002 Brick. 91
B.2 Test stand results of measured HE002 Brick. 92
B.3 Test stand set up of measured Brick. 93
B.4 Test stand set up of prototype Brick. 94
B.5 Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks. 95
B.6 Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks. 95

B.7 Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks. 95
B.8 MainBoard PIC16F series micro-controller code. 96
B.9 MainBoard PIC16F series micro-controller code. 97
B.10 MainBoard PIC series micro-controller code. 98
B.11 Serial PIC firmware development. 99
B.12 BLA front panel. 100

C.1 MOSFET driver 1 Board. 102
C.2 MOSFET 1 Board. 103
C.3 Irradiated Chip U5 and U6 performance. The results from Chip U5 show that the output voltage had some fluctuations during all the 3rd run, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy. The results from Chip U1 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the beginning of each run. The fluctuations did no stop when the beam was stopped at the end of each run (a power cycle was needed). Except after run 2, where the chip behaved normally after beam stopped. After the last run (receiving 400 Gy), and a power cycle, the chip started to behave properly. 103
C.4 The results from Chip U7 show that this chip almost behaved like the reference chip during the whole test, except for some time during the second run, where it showed huge fluctuations (went back to normal without a power cycle). The chip also survived the entire dose of 400 Gy. 104
C.5 The results from Chip U8 show that the output voltage had some fluctuations during all the runs, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy. The results from Chip U10 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the end of the run. The chip also survived the entire dose of 400 Gy. 104

D.1 Database development LabVIEW Block diagram. The LabVIEW Database Connectivity Toolset is an add-on package for accessing databases. The toolkit contains a set of high-level functions for performing the most common database tasks and advanced functions for customized tasks. 105
D.2 Database entry of measured Brick. 106

List of Tables

4.1 Basic design parameters for the fLVPS Brick [34]. 37

5.1 Testing station test parameter bounds. These parameters are used to restrict the response of the output to a change in measurement when evaluating the LVPS Brick under test. 49

6.1 Basic conditions for Burn-In procedure. 59

7.1 Radiation doses simulated for 4ab^{-1} of HL-LHC running [42]. 70

7.2 LVPS Radiation Type, simulated dose and target dose. The radiation is computed in terms of total ionizing dose (TID), non ionizing energy loss (NIEL) and single event effect (SEE) are shown. The three last columns show the radiation dose assumed in 2020 for the present LVPS design, the survival limit dose and the safety factor assumed for the new design. Safety factors are introduced by the ATLAS Electronics Coordination Group as specified in Table to account for error margins associated with the different types of radiation tests. Safety Factors: SF_{sim} (Safety Factor on the simulation giving the Doses or Fluences) and SF_{lot} (Safety Factor corresponding to the variation from lot to lot of components) [34]. 71

7.3 Bricks tested at ^{60}Co for gamma susceptibility. 73

7.4 Summary of components and Brick tested at different target fluences. . . . 74

List of Abbreviations

ADC	**A**nalogue to **D**igital **C**onvertor
ALICE	**A** **L**arge **I**on **C**ollider **E**xperiment
ASIC	**A**pplication **S**pecific **I**ntegrated **C**ircuit
ATCA	**A**dvanced **T**elecommunications **C**omputing **A**rchitecture
ATLAS	**A** **T**oroidal **LHC** Apparatu**S**
BCID	**Bunch** **C**ross **Id**entification
BJT	**B**ipolar **J**unction **T**ransistor
BT	**B**arrel **T**oroid
CAN	**C**ontrol **A**rea **N**etwork
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CERN	European Organization for Nuclear Research
COTS	**C**ommercial **O**f **T**he **S**helf
CMOS	**C**omplementary **M**osfet
CLK	**C**lock **S**ignal
CP	**C**harged **P**article
CS	**C**entral **S**olenoid
CMS	**C**ompact **M**uon **S**olenoid
DAC	**D**igital **A**nalog **C**onvertor
DAQ	**D**ata **A**c**Q**uisition
DB	**D**aughter **B**oard
DCS	**D**etector **C**ontrol **S**ystem
EB	**E**xtended **B**arrel
ELMB	**E**mbedded **L**ocal **M**onitoring **B**oard
ECT	**E**nd **C**ap **T**oroid
FCAL	**F**orward **C**alorimeter
FDR	**F**inal **D**esign **R**eview
FEB	**F**ront **E**nd **B**oards
FET	**F**ield **E**ffect **T**ransistor
FTDI	**F**uture **T**echnology at **D**evices **I**nternational
fLVPS	**f**inger **L**ow **V**oltage **P**ower **S**upply
FWHA	**F**ull **W**idth at **H**alf **M**aximum
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
GUI	**G**raphical **U**ser **I**nterface

HECAL	**H**adronic **E**nd Cap **C**alorimeter
HL-LHC	**H**igh **L**uminosity-**LHC**
HV	**H**igh **V**oltage
HVPS	**H**igh **V**oltage **P**ower **S**upply
HTEL	**H**igh **T**hrouput **E**lectronics **L**aboratory
IC	**I**ntergrated **C**ircuit
ID	**I**nner **D**etector
ICPP	**I**nstitute for **C**ollider **P**article **P**hysics
IDE	**I**ntergrated **D**evelopment **E**nviroment
IO	**I**nput **O**utput
LAr	**L**iquid **A**rgon
LHC	**L**arge **H**adron Collider
LHCb	**L**arge **H**adron Collider beauty
LB	**L**ong **B**arrel
LVPS	**L**ow **V**oltage **P**ower **S**upply
MCU	**M**icro **C**ontroller **U**nit
MD	**M**ini **D**rawer
MUX	**M**ulti **P**lexor
OVP	**O**ver **C**urrent **P**rotection
OTP	**O**ver **T**emperature **P**rotection
OCP	**O**ver **V**oltage **P**rotection
NIELs	**N**eutron **I**onizing **E**nergy **L**oss
PCB	**P**rinted **C**ircuit Board
PCIe	**P**eripheral **C**omponent **I**nterconnect **e**xpress
PDR	**P**reliminary **D**esign **R**eview
PIC	**P**eripheral **I**nterface **C**ontroller
PMT	**P**hoto **M**ultiplier **T**ube
POL	**P**oint **O**f **L**oad
PPr	**P**re **P**rocessor
RoD	**R**ead **O**ut **D**river
SC	**S**low **C**ontrol
SCT	**S**emi **C**onductor **T**racker
SEB	**S**ingle **E**vent **B**urnout
SEE	**S**ingle **E**vent **E**ffects
SEL	**S**ingle **E**vent **L**atchup
SET	**S**ingle **E**vent **T**ransients
SEU	**S**ingle **E**vent **U**psets
SM	**S**tandard **M**odel
SPS	**S**uper **P**roton **S**ynchrotron
TDAQ	**T**rigger **D**ata **A**c**Q**uisition

TID	**T**otal **I**onizing **D**ose
TileCal	**T**ile **C**alorimeter
TRT	**T**ransition **R**adiation **T**racker
TCP	**T**ransmission **C**ontrol **P**rotocol
TTC	**T**rigger **T**iming **C**ontrol
UV	**U**ltra **V**iolet
WLS	**W**avelength **S**hifting

List of Symbols

Global notations

η	Pseudo-rapidity	—
γ	Gamma photons	—
λ	Lambda	length (m)
ϕ	denotes the coordinates	—
δ	Delta	—
θ, ϕ	incoming direction expressed in term of spherical coordinates	rad
τ	time	s (second)
x,y	spatial coordinates	1 (uint)
p_T	Transverse momentum (Projection of the total momentum in the plane)	
E_T	Transverse Energy	

Chapter 1

Introduction

1.1 The Standard Model of particle physics

The study of particle physics is centered on understanding the properties of elementary particles and the mechanisms by which they interact. The SM of particle physics neatly contains our current knowledge of particle physics. The discovery of the Higgs boson in 2012 by the ATLAS [1] and CMS [2] collaborations, was a major breakthrough for particle physics and subsequently there are currently no particles in the SM which have not been experimentally observed.

The SM specifies the nature of every field (and every particle by extension) that has been observed in nature, according to the theoretical framework of quantum field theory (QFT). Particles are believed to be the outcome of propagating excitations in a number of fundamental fields that transcend space and time, according to quantum mechanics. Under the theoretical framework of quantum field theory (QFT), the SM describes the nature of every field (and therefore every particle by extension) which has been observed in nature. The observation of particles therefore allows us to probe the nature of the fields from which they emerge, which allows us to further understand the fundamental constituents of the universe [3, 4, 5].

1.1.1 Particles in the Standard Model

The importance of the many particles in the SM can be classified into two categories: fermions and bosons. These two definitions describe not only particle spin, but also how particles organize themselves in huge ensembles and interact with one another. This has implications for our perceptions of and interactions with the physical environment. Fermions have half-integer spin ($\frac{1}{2}$, $\frac{3}{2}$, etc.) and have quantum mechanical wavefunctions that are anti-symmetric when two of them are exchanged, implying that two fermions cannot occupy the same quantum state at the same time. The matter that we are familiar with on macroscopic scales is made up of fermionic particles, which sounds intuitive.

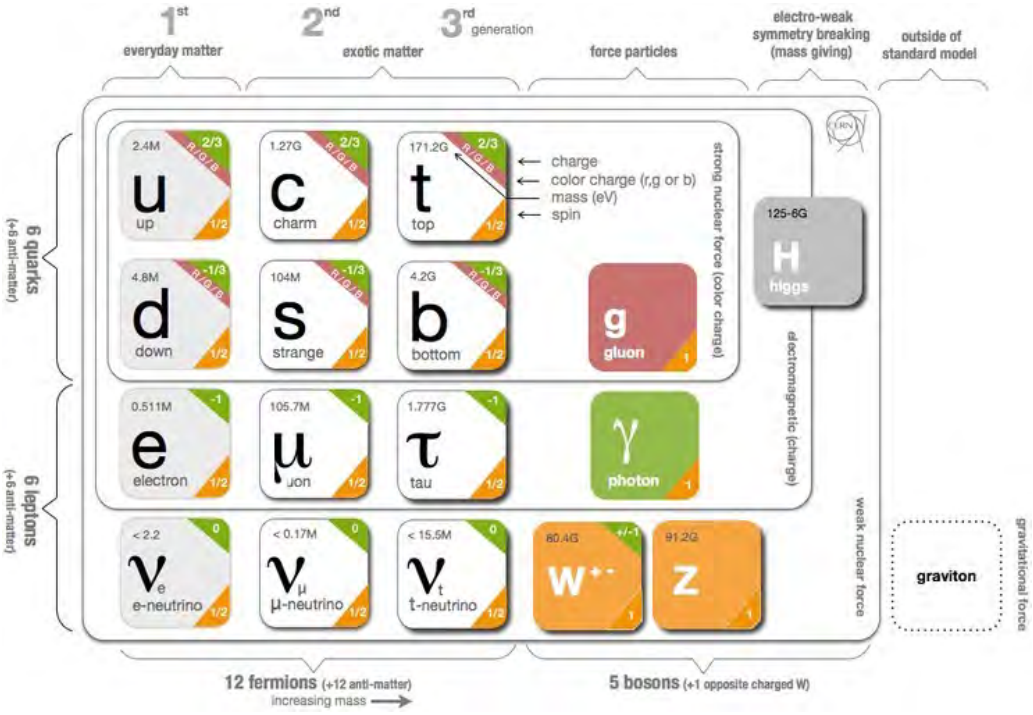

Figure 1.1: The fermionic particle content currently explained in the SM, with their associated masses in parentheses. All quoted masses are taken from Reference [7, 8, 9, 10]. The errors have been omitted for significantly precise measurements.

This is especially true in the SM, where we believe matter is virtually exclusively composed of electrons orbiting bound states of quarks (protons and neutrons). In Figure 1.1, the fermionic particles of the SM are given along with their properties. In principle, freely moving leptons can be observed in nature, but free quarks cannot. Quarks have been demonstrated to follow a concept known as "confinement", which causes them to spontaneously cluster into groups to make hadrons (such as protons, neutrons, pions, etc.). This is linked to the fact that quarks carry a color charge (different from their electric charge), which was derived from the patterns by which quarks cluster [4, 5, 6]. There is an equally massive anti-particle associated with each fermion in the SM, which has inverted internal charges. The fermions in the SM are chiral in nature and can have left-handed or right-handed projections, which is a measure of whether or not a particle's spin is aligned with its momentum [7, 8, 9, 10]. Bosons serve as interaction mediators in the Standard Model. Electromagnetism, the strong nuclear force, and the weak nuclear force are three fundamental interactions in the SM that are responsible for distinct forces that have been identified in nature. These interactions are linked to the interchange of spin 1 gauge bosons, which originate from the requirement that certain symmetries, known as gauge symmetries, be obeyed by nature. As a result, these bosons are also known as gauge bosons. The photon (γ) is linked to electromagnetism, while the gluon (g) to the strong interaction; both particles have no mass. The massive W and Z bosons, with masses of 80.385 ± 0.015 GeV and 91.1876 ± 0.0021 GeV, respectively, mediate the

weak interaction [11, 12]. The graviton, a spin 2 gauge boson, is thought to be linked to gravity. However, there is currently no experimental proof that it exists. The Higgs interaction, which is not mediated by a gauge field, is another fundamental interaction in the Standard Model. It is rather included by hand as a field that allows particles to have mass whilst maintaining the SM's required symmetries. The spin zero (scalar) Higgs boson is added to the SM as a result of this. A massive particle with a mass of 125.09 ± 0.24 GeV [12, 13]. The theoretical account of electroweak symmetry breaking clarified the origin of the Higgs boson (and the masses of all known heavy fundamental particles) [12, 13, 14, 15].

1.1.2 Electroweak Interaction

The purpose of the SM's early development was to use gauge invariance to combine multiple theories of particle interactions. Quantum Electrodynamics (QED) can be explained using a theory based on gauge invariance under a U(1) group symmetry, which gives rise to the photon and its interactions, while Quantum Chromodynamics (QCD) uses an SU(3) group symmetry to give rise to eight gluons and their interactions with quarks via colour charge. A Yang-Mills theory [13] is a theory that is built on an SU(N) group. A Yang-Mills theory can also be used to describe the weak interaction. However, there are a few caveats that make the description more complicated. This section explains these limitations and how to overcome them using the notion of electroweak symmetry breaking (EWSB). Glashow, Weinberg, and Salam (GWS) developed the Electroweak (EW) Theory to better comprehend weak interactions [6, 7]. The Yang-Mills theory combines weak and electromagnetic interactions into a single theory. According to the theory, all left-handed fermions are organized as weak iso-doublets (components that mix during transformations in an isospin space), for the neutral and charged leptons, and the up- and down-type quarks, respectively:

$$q_L = \begin{pmatrix} u \\ d \end{pmatrix}_L \; and, \begin{pmatrix} v_\ell \\ \ell^- \end{pmatrix}_L , \tag{1.1}$$

Under the EW gauge group, right-handed fermions are considered as singlets and do not transform: $U(1)_Y \; SU(2)_L \; SU(2)_L \; SU(2)_L \; SU(2)_L \; SU(2)_L \; SU(2)_L$ The $SU(2)_L$ group transformations exclusively affect left-handed fermion doublets, as shown by the subscript L. Weak hypercharge, denoted by the γ symbol, is a conserved quantity determined by the Gell-Mann Nishijima equation [16, 17]:

$$\gamma = 2(Q - I_3), \tag{1.2}$$

where I3 is the third component of a fermion's isospin, while Q is its electric charge. The U(1) group's generator is represented by the parameter γ. This fermion treatment is required, but it comes with two unavoidable drawbacks. To begin with, the need of gauge invariance necessitates the theory's bosonic mediators to be massless, just as photons and

gluons are massless. The bosonic mediators of the weak interaction (the W and Z bosons) should have a non-negligible mass, according to Fermi's prior work [18, 19]. The second issue has to do with rewriting the theory in terms of left-handed and right-handed fermion projections. Because the EW theory exclusively applies SU(2) transformations to left-handed doublets, gauge invariant mass terms for fermions that are known to be massive cannot be written down. As a result, the fermions couldn't have mass terms. Surprisingly, the insertion of the Brout-Englert Higgs (BEH) mechanism solves both difficulties [20, 21, 22]. In the 1960s, Peter Higgs, Francois Englert, and Robert Brout presented the BEH mechanism, which was the first to illustrate how a gauge field might gain mass without breaking gauge invariance. Guralnik, Hagen, and Kibble [23] followed up on this theoretical discovery with similar work. The answer lies in postulating the existence of a scalar field with a non-zero vacuum expectation value (VEV), which will be explained briefly below. Consider a complex field ϕ interacting with a U(1) gauge field A^{μ} for illustration purposes. When introducing the gauge field, gauge invariance must be preserved by embedding A^{μ} into the Lagrangian as follows:

$$\mathcal{L} = (D_{\mu}\phi)^{+}(D^{\mu}\phi) - \frac{1}{4}F_{\mu v}F^{\mu v} - \mu^{2}\phi^{*}\phi - \lambda(\phi * \phi)^{2}, \tag{1.3}$$

where $F_{\mu v}$ = ∂_{μ} A - ∂_{v} A_{μ} and D_{μ} is the covariant derivative D_{μ} = ∂_{μ} - ieA_{μ}. The kinetic terms of the scalar field and gauge field, respectively, could be denoted by the first two terms in Equation 1.5. The other two terms can be thought of as the negative of a potential V(ϕ) (i. e. such that L = T - V). Interactions between ϕ and A_{μ} arises from the covariant derivative, and gauge invariance rules out the possibility of a mass term for A_{μ}. It's worth noting that ϕ has two degrees of freedom because it is complex. The gauge boson is a massless particle with no mass. A has two degrees of freedom as well, bringing the total number of degrees of freedom in the theory to four. The particle spectrum produced by the theory can be approximated from a quantum mechanical standpoint by looking at minor variations of the Lagrangian in Equation 1.5 around a stable background.We can now analyze the particle spectrum by expanding around the new vacuum of the theory by changing the fields such that h = Re(ϕ) -v and = Im(ϕ). This will result in the following (without all of the interaction terms):

$$\mathcal{L}(h,\chi) = \frac{1}{2}(\partial_{\mu}h)(\partial^{\mu}h) - \lambda v^{2}h^{2} + \frac{1}{2}(\partial_{\mu}\chi)(\partial^{\mu}\chi) - \frac{1}{4}F_{\mu v}F^{\mu v} + \frac{1}{2}e^{2}v^{2}A\mu A^{\mu} \tag{1.4}$$

The penultimate term in Equation 1.4 is an instantaneous mass term for the gauge field, (m_{A} = $\frac{ev}{\sqrt{2}}$). There is also a large scalar boson h with mass m_{h} = $\sqrt{\lambda v}$ as well as another massless scalar. It can be proved that is not a real particle in the theory since it can be eliminated from the Lagrangian by performing a simple $U(1)$ rotation after selecting a fixed gauge and h is a Higgs boson [24, 25]. There are four degrees of freedom in the theory as expressed in Equation 1.5, and there should be four degrees of freedom after expanding around the vacuum. Equation 1.4 has one degree of freedom for the large

scalar h and three degrees of freedom for the now massive gauge field.

1.1.3 Quantum chromodynamics

Quantum Chromodynamics (QCD) is a theory based on the $SU(3)_C$ colour group [26]. The requirement of the Lagrangian's local gauge symmetry involving colored quark fields leads to massless gluon vector bosons that can interact with each other. The $SU(3)_C$ group's unique structure implies gluon-gluon interactions that lead to the theory's asymptotic freedom and confinement, ensuring the transmission of color neutral states to macroscopic distances. The QCD Lagrangian can be read as follows:

$$\mathcal{L}_{\mathcal{QCD}} = -\frac{1}{4}(F^a_{\mu v}) + \sum_{k=(flavors)}^{n_f} \Psi_k^{-j}(i\not{D}m)_{ij})\Psi^i_k + \mathcal{L}_{gauge} \tag{1.5}$$

where $(D_\mu)_{ij}$= δ_{ij} ∂_μ - igA^a_μ $\frac{\lambda_{ij}}{2}$ For each color i and flavor k, there are eight a = 1...8 spin-1 massless gluon fields A^a_μ that mediate the strong interaction and quark fields ψ^i_k. The coupling of the strong interaction g is linked to the gauge invariance of the QCD Lagrangian. The kinetic term for - $\frac{1}{4}(F^a_{\mu v})(F^{a\mu v})$ generates the gluon self- interaction. The structure coefficients f_{abc} are related to the generators of the $SU(3)_C$ color group Gell-Mann matrices λ^a_{ij} by $[\lambda^a, \lambda^b] = i\lambda^c$ defining the corresponding Lie algebra. To perform perturbative calculations, the gauge fixing term $\mathcal{L}_{gauge}$ must be added. The propagators for the gluon fields are not defined otherwise. In summary, the application of perturbative aspects of QCD framework to hadronic scattering and final state objects not only played an important role in the development of collider physics, but also contributed to the verification of the EW sector of the SM through the discovery of the W and Z bosons, as well as the bottom and top quarks.

1.2 The Large Hadron Collider and its experiments

Particle accelerators are used in particle physics experiments. Particle physics is a branch of physics that aims to discover the structure of matter at the smallest scales possible. In terms of dimensional analysis, length and energy are inversely proportional. As a result, only high energies can probe small distances. It is for this reason that particle accelerators are an important field of investigation in particle physics since colliding particles are accelerated to high energies. The Large Hadron Collider (LHC) [11] is the world's largest and most powerful particle accelerator. It is part of the accelerator complex at the European Organization for Nuclear Research (CERN) (Figure 1.1), and located in a circular tunnel between 45 m and 170 m beneath the France-Switzerland border near Geneva. The accelerator complex is made up of a series of particle accelerators, each of which boosts the energy of a particle beam before injecting it into the next one in the chain. The LHC features a 27-kilometer circumference and two parallel beam pipes that run through 1232

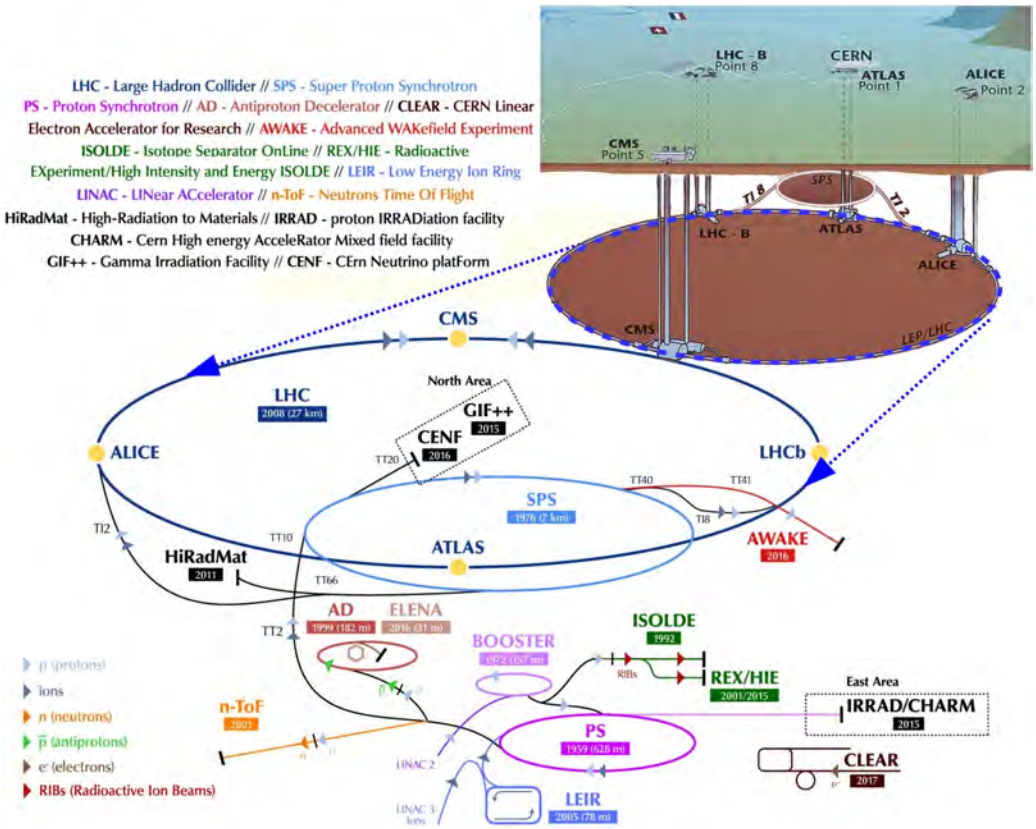

Figure 1.2: CERN accelerator complex with Large Hadron Collider (LHC), Super Proton Synchrotron (SPS), Proton Synchrotron (PS), Antiproton Decelerator (AD), Low Energy Ion Ring (LEIR), Linear Accelerators (LINAC), CLIC Test Facility (CTF3), CERN to Gran Sasso (CNGS), Isotopes Separation on Line (ISOLDE), and neutrons Time of Flight (n-ToF) LHC [5].

main dipole and 392 main quadrupole superconducting magnets, which bend and focus the two counter-rotating protons or heavy ions beams. The LHC beams cross in four experimental caverns, in which large experiments are built around the crossing point. Each experiment is outfitted with many layers of sub detectors and instrumentation in order to measure and identify the particles that emerge from the collisions energy. Two of the experiments are general-purpose detectors: A Toroidal ApparatuS (ATLAS) [1] and the Compact Muon Solenoid (CMS). These detectors are designed to investigate a variety of particle physics phenomena. A third experiment, A Large Ion Collider Experiment (ALICE) [12] is designed to measure heavy ion collisions in order to study the physics of strongly interacting particles including the quark-gluon plasma, while the Large Hadron Collider beauty (LHCb) experiment is designed for precision measurements of heavy b-quark interactions to explore questions such as CP violation and the matter-antimatter asymmetry of the universe.

1.2.1 LHC upgrade for the high luminosity era

The vast majority of collisions at LHC are low-momentum transfer minimum bias events. The LHC was designed to deliver a peak luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ in order to produce adequate rates of inelastic collisions, which produce particles with sufficiently high angles with respect to the beam axis to be measured, and which could be interesting for new physics research. The LHC has a proton bunch crossing rate of 40.08 MHz, with multiple particle collisions per bunch crossing. As a result,the LHC experiments are equipped with multi-level trigger and data gathering systems that reject uninteresting events in order to make data quantities reasonable while reducing the loss of fascinating physics. The discovery of the Higgs particle in 2012 cemented the idea of pushing the LHC to its limits by increasing the luminosity to produce a substantially larger volume of particle collisions over the accelerator's lifetime [27]. The HL-LHC program will allow for more precise measurements of SM particles and processes, as well as increased sensitivity to huge particles and unusual processes that may arise at rates lower than our current sensitivity levels. Increasing the peak LHC luminosity to 5×10^{34} cm^{-2} s^{-1} will result in an integrated luminosity of up to 250 $\text{fb}^{-}1$ each year, with a total of at least 2500 fb^{-1} during a ten-year period after the upgrade [11].

Experiments at the LHC

ATLAS, CMS, ALICE [8], and LHCb [1] are the four experiments that will be installed at the LHC [27] accelerator. ATLAS and CMS are proton-proton detectors with similar physics goals but distinct designs. The key distinction is in the magnet system, which has a significant impact on the detector geometry. Two specialized detectors, ALICE and LHCb, have also been developed. ALICE specializes in heavy ion (Pb-Pb) collisions, while LHCb focuses on B-physics and the CP-violation that goes with it. The technical design studies for ATLAS, CMS, ALICE and LHCb provide further information on the detectors.

CMS

The Compact Muon Solenoid (CMS) is a multi-purpose proton-proton collision experiment. CMS is smaller than ATLAS, with a length of 22 meters and a height of 15 meters. Despite this, its mass is over two times that of ATLAS, at 12500 t. The CMS detector will be built around a 13 m long superconducting solenoid with a bore of 5.9 m and a nominal magnetic field strength of 4 T, resulting in a compact design of the muon spectrometer.

ALICE

ALICE (A Large Ion Collider Experiment) is a heavy-ion detector that was created to study Pb-Pb collisions. The physics of strongly interacting matter and the quark-gluon-plasma will be studied with ALICE. This provides us with a better understanding of our universe as it existed just after the big bang. ALICE has a unique feature in that it will reuse components of the L3 experiment that was previously running at the Largest Electron-Positron accelerator (LEP). The ALICE detector is being developed by a team of over 1000 physicists and engineers from 105 institutes across 30 countries. It has a total volume of 161626 m^3 and a weight of around 10 000 t. ALICE is made up of a forward muon spectrometer and a middle barrel that measures hadrons, electrons, and photons. The central section covers the polar angles from 45 $^\circ$ up to 135 $^\circ$ and housed in a massive solenoid magnet that was left over from the L3 experiment at LEP. From the inside out, the barrel contains an Inner Tracking System (ITS) of six planes of high-resolution silicon pixel (SPD), Three particle identification arrays of Time-of-Flight (TOF), Ring Imaging Cherenkov (HMPID), and Transition Radiation (TR) detectors, high-resolution silicon pixel (SPD), drift (SDD), and strip (SSD) detectors, a cylindrical Time-Projection Chamber (TPC), and three particle identification arrays of Time-of-Flight (TOF), Ring Imaging Cherenkov (HMPID), and (TRD) detectors, and two electromagnetic calorimeters (PHOS and EMCal).

LHCb

The LHCb was built to investigate CP violation and other unusual events in B meson decays. These studies are important not only for elementary particle physics but also for cosmology, as they help to explain why matter dominates antimatter in our world. LHCb can work at much lower luminosity (10^{32} $cm^{-2}s^{-1}$) than the nominal luminosity of LHC. Therefore it is possible to reach its full physics potential already in the beginning of LHC operation [28]. The LHCb was built to investigate CP violation and other unusual events in B meson decays. These researches are important not only for elementary particle physics but also for cosmology, as they help to explain why matter dominates antimatter in our world. The LHCb can operate at a substantially lower luminosity (10^{32} $cm^{-2}s^{-1}$) than the LHC's nominal luminosity. As a result, it is possible to realize its full physics potential even before the LHC starts operating cite.

ATLAS

The ATLAS experiment is explained more in detail in the following sections as the ATLAS Hadronic Tile Calorimeter is subject of this thesis.

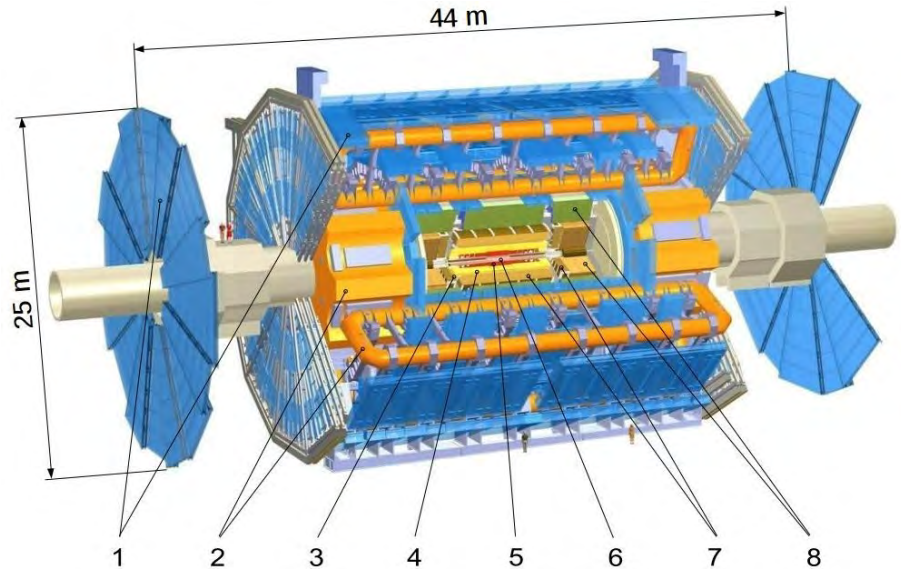

Figure 1.3: The ATLAS Detector and its detector subsystems from the LS0 ATLAS layout. (1) Muon Detectors; System of magnets: (2) Toroid Magnets and (3) Solenoid Magnet; Inner Detector: (4) Transition Radiation Tracker, (5) Semi-Conductor Tracker and (6) Pixel Detector; Calorimeters: (7) Liquid Argon Calorimeter and (8) Tile Calorimeter. The inner beam line (IBL) and New-Small-Wheel (NSW) are seen on both ends of the detector [29].

1.3 The ATLAS Experiment facing the High Luminosity LHC

Increasing the LHC luminosity [29] also poses major challenges for the detectors. The larger numbers of collisions per bunch crossing mean that interesting physics events will be overlaid by high numbers of particles from simultaneous minimum bias events, making selection of interesting events more difficult. It also means that detectors and electronics must be able to tolerate much higher quantities of radiation. These new challenges necessitate the developing of new electronic designs for the front end and off detection systems based on newer technology. This thesis highlights the author's contributions to making ATLAS capable of meeting the demanding requirements for the HL-LHC.

1.3.1 ATLAS detector overview and coordinate system

The ATLAS experiment makes use of a right-handed coordinate system with its origin located at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upwards. Cylindrical coordinates (r, ϕ) are used in the transverse plane, where ϕ is defined as the azimuthal angle around the z-axis. The pseudo-rapidity is defined in terms of the polar angle θ as $\eta = -ln\tan(\theta/2)$. is a cylindrical detector with dimensions of approximately 25 m diameter and 44 m length, weighing approximately 7000 tons. It is instrumented with multiple layers of detectors at increasing distance from the interaction point in the centre of (Figure 1.3). The four main detector subsystems are

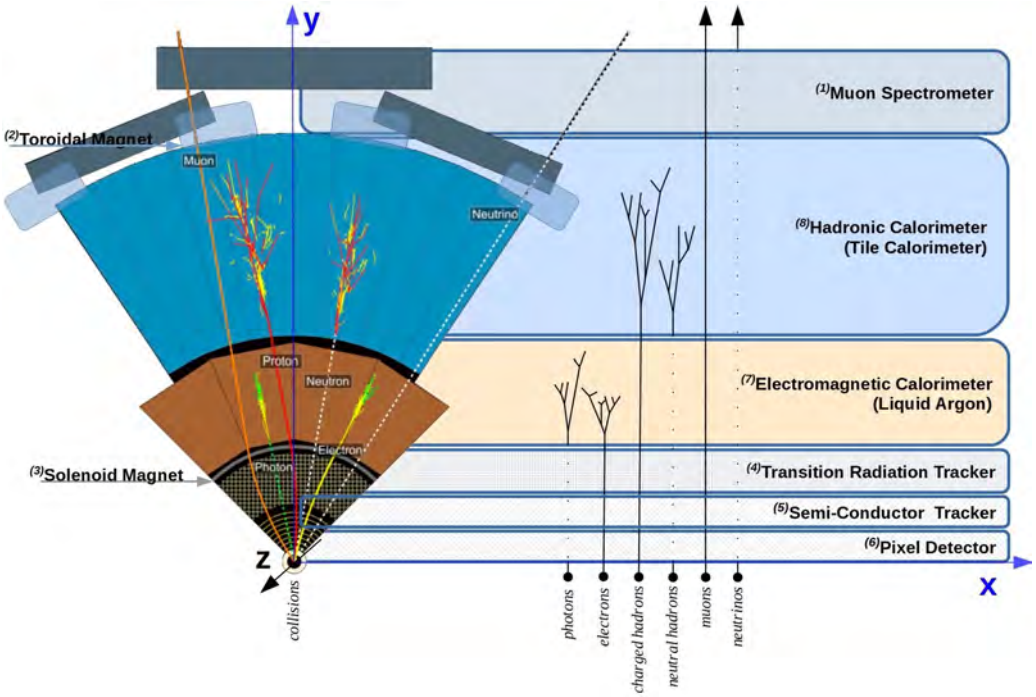

Figure 1.4: ATLAS Detector Particle detection schematic [1].

the inner tracking detector, the calorimeters, the muon spectrometer, and the superconducting magnet systems. The bunches of protons arriving each 25 ns along the z axis collide at the interaction point in the centre. A particle's momentum along the z axis is termed longitudinal momentum, while the projection of a particle's total momentum p on the xy plane is defined as the particle transverse momentum p_T. The pseudo-rapidity (η), is a convenient and commonly used way to express the polar angle θ of high energy particles [30].

1.3.2 Particle detection on the ATLAS detector

In the various sub-detectors, the Standard Model particles exhibit distinct signatures. Data from the tracking, calorimeter and muon spectrometer subsystems are combined to identify and characterize each particle produced in a collision (Figure 1.4). ATLAS uses a system of magnets to bend charged particles' paths in a known magnetic field to measure their momentum and energy. For accurate momentum and charge measurements, the central solenoid enclosing the Inner Detector generates a nominal field of 2 T. To allow accurate muon energy measurement, the muon spectrometer employs a system of superconducting toroidal magnets with a nominal field strength of 0.6 T. The Inner Detector consists of a high-granularity Pixel Detector for precise vertex reconstruction, a semiconductor strip tracking detector for high-density track measurement near the beam pipe, and a transition radiation straw-tube Tracker for large-radius tracking and particle identification. The Liquid Argon Electromagnetic Calorimeter (LAr) and the Hadronic Tile

Calorimeter (TileCal) are part of a system of calorimeters that absorb and measure the energies of both charged and neutral particles leaving the tracking volume. High-density absorber materials stop electrons, photons, and hadrons in both calorimeters, while active materials provide a signal proportionate to the energy deposited by secondary particles and particle cascades. The innermost calorimeter layer (LAr) is made up of layers of absorber material (lead) and active material (liquid argon). The electromagnetic barrel calorimeter and end-caps, which include the forward calorimeter (FCAL), electromagnetic end-caps, and hadronic end-caps, are included in LAr. For precise measurements of the energy and location of electrons and photons, LAr is highly granular, with around 200,000 channels. The outer calorimeter (TileCal) is made up of steel absorber sheets with scintillating plastic tiles sandwiched in between. TileCal has ten thousand photomultiplier channels that read out the scintillating light produced by hadrons and hadronic jets, which is less granular than LAr. The Muon Spectrometer is ATLAS's furthest detector. This sub-detector incorporates three massive superconducting air-core toroid systems with gas-filled tracking chambers to measure the bending radius of muons as they leave the detector, with a total of about 200 000 channels. The subsystem can identify muons from cosmic rays and from other muons, in addition to providing good muon momentum resolution.

1.3.3 Muon Spectrometer

The ATLAS Muon Spectrometer [13] bends the trajectories of muons in a magnetic field created by a system of large, superconducting air-core toroid magnets, and measures their tracks with four different types of tracking chambers, each with positions optimized for full spatial coverage and momentum resolution. The Muon Spectrometer uses two types of trigger detectors, as shown in Figure 1.5: Resistive Plate Chambers (RPC) for the barrel region and Thin Gap Chambers (TGC) for the end-cap region. Chambers (RPC) for the barrel region and the Thin Gap Chambers (TGC) in the end-cap region. The Monitored Drift Tube (MDT) chambers track and measure momentum for both the barrel and the end-cap, with the exception of the innermost layer of the end-cap, where Cathode Strip Chambers (CSC) are positioned [31]. The end-cap inner station (EI station) will be replaced with a NSW detector made up of eight layers of Micromegas and eight layers of small-strip TGC as part of the ongoing Phase-I upgrade. In addition, each small-sector MDT chamber in stations 7 and 8 (BIS78) for the barrel inner (BI) station will be replaced with a small-diameter MDT (sMDT) chamber and a thin-gap RPC. The following are the overall Phase-II upgrade strategies [32]: (1) increase the number of RPC and TGC trigger layers in the barrel and endcap regions, respectively; (2) combine TGC and NSW information to reduce fake trigger muons found in the endcap region; and (3) use MDT as a trigger device at the first trigger level to improve the trigger muon momentum resolution.

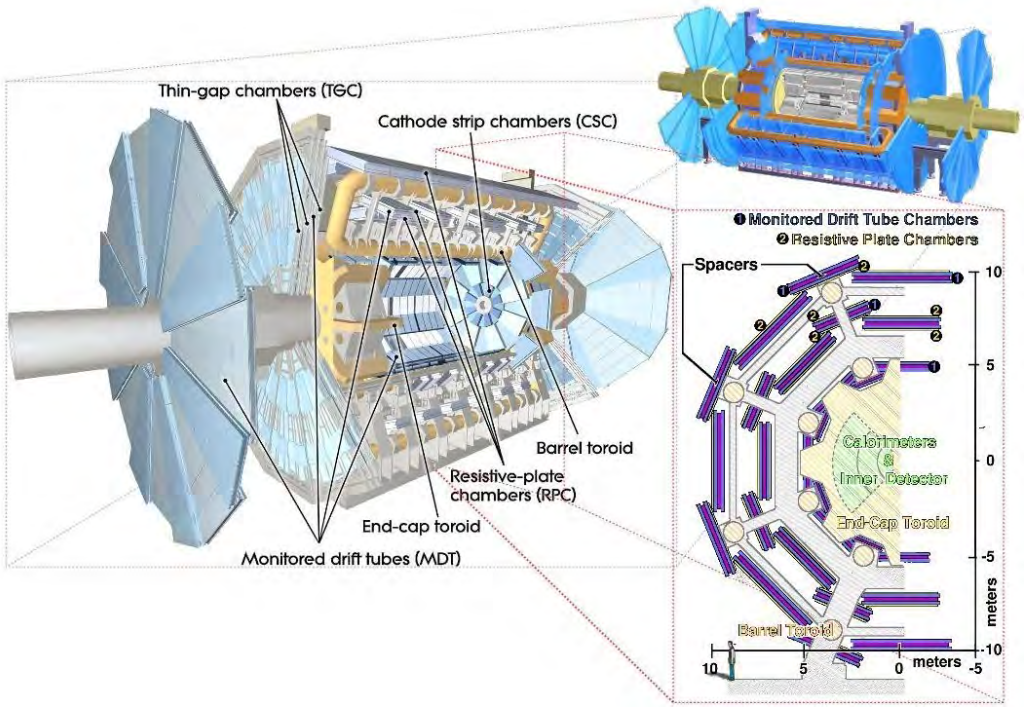

Figure 1.5: The Muon Detector [33].

1.3.4 Inner Detector

The tracks describing the trajectories of charged particles as they travel through the detector can be reconstructed. The Inner Detector's major goals are to get exact particle trajectory data and to properly estimate their initial spatial coordinates [12]. The inner detector (Figure 1.6) is made up of three different detector layers stacked in concentric cylinders around the beam axis, with a maximum length of 7 m and a radius of 115 cm. The end-cap detectors, on the other hand, are arranged in disks perpendicular to the beam axis. Over $|\eta| \leq 2.5$, the Inner Detector as a whole provides full tracking coverage.

1.3.5 The Pixel Detector

The Pixel Detector (Figure 1.7), the innermost element of the Inner Detector, was designed for very high-granularity and high-precision measurements as close to the interaction point as possible. This sub-detector takes three measurements per track over the entire acceptance and is utilized to determine secondary vertices from short-lived particles like B hadrons and τ leptons, as well as to calculate the impact parameter resolution. The Pixel detector, which has around 140 million channels, is made up of three concentric barrel layers and five disk layers on each, with the goal of achieving a high angular coverage. The pixel modules are placed on support structures in the two end-cap sections and on staves in the barrel region, as shown in (Figure 1.7 to the left).

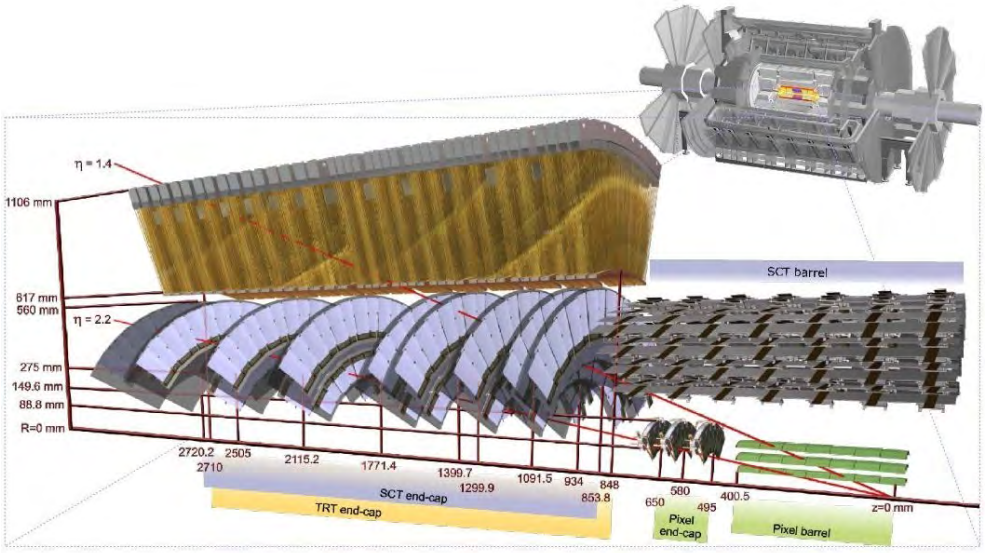

Figure 1.6: ATLAS Inner Detector [29].

To reduce energy loss from crossing particles, as well as multiple scattering and secondary interactions, light materials are used for support structures and sensors. The carbon fiber support structures incoparate cooling circuits built into them. The pieces that make up a pixel barrel module are shown in (Figure 1.7 to the right). Each module contains 61440 pixel elements read out by 16 FE chips, each of which serves a 24 × 160 pixel array. The module's interconnections are made on a flexible Kapton printed circuit board (PCB), which is wire-bonded to the electronics chips. On the sensor surface, the output signals are routed to a hybrid on top of the chips, and then to a separate clock-and-control integrated circuit. Individual circuits for each pixel element are included in the read-out chips, as well as buffers for storing data until an L1 trigger choice is made. The Pixel Detector elements were designed to withstand a total dosage of ionizing radiation of more than 300 kGy and over 10^{15} neutrons per cm^{-2} over 10 years of operations [27].

1.3.6 The Semiconductor Tracker

The Semiconductor Tracker (SCT) [12] surrounds the Pixel Detector. This subsystem contributes to momentum, impact parameter, and vertex position computations by providing eight measurements per track. The SCT's four barrel modules are mounted on carbon fiber cylinders that house the cooling system, and the end-caps are made up of nine annular disks at each end of the barrel region. This arrangement, which has over 6.2 million channels, covers the radial region from about 30 to 52 cm, with hermetic azimuthal coverage of $|\eta| \leq 2.5$. Four single-sided p-on-n silicon detectors make up each module. On each side of the module, two detectors are wire-bonded together to form strips. The electronics are set above the detectors, and two of these strips are glued together in a

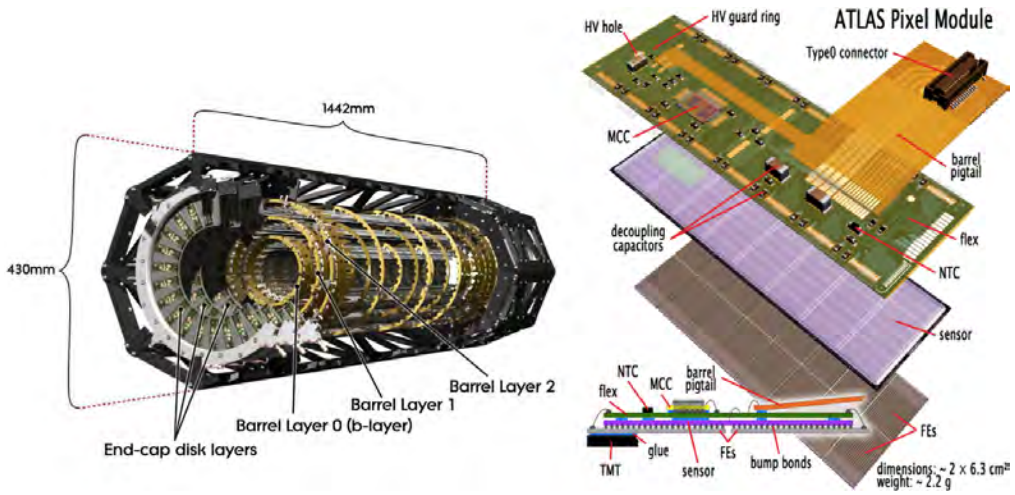

Figure 1.7: Assembly view and cross-section of an ATLAS Pixel Detector module (left) and the Schematic drawing of the ATLAS Pixel Detector (right) [34]. The IBL is not included in the image.

back-to-back configuration separated by a heat transmission plate. Both the Pixel Detector and the SCT require extremely high dimensional stability, relatively cold detector operation (–7°C), and adequate heat dissipation from both the detector leakage current and the electronics.

1.3.7 The Transition Radiation Tracker

The Transition Radiation Tracker (TRT) [12] is made up of 372000 cylindrical drift tubes or 4 mm diameter cylindrical straws. The barrel portion has about 50000 straws, each separated at z = 0 to reduce occupancy. The remaining 320000 straws are spread radially in the end-caps, with the read-out at the outer radius. Individual modules with 329 to 793 axial straws make up the barrel portion, while 18 wheels in each of the end-caps have a total of 224 layers of radially arranged straws. A thin 30μ m diameter gold-plated tungsten sensing wire sits in the center of a straw, while the 4 mm diameter conductive coated Kapton surface functions as a cathode by being held at high voltage of negative polarity. The straws are filled with a gas mixture consisting of 70% Xe for good X-ray absorption and 27% CO_2 and 3% O_2 for photon quenching and increasing the electron drift velocity. Interleaved between the straw layers are polypropylene foils or fibre radiators. Tracking is provided by the drift tubes, and additional discrimination between hadrons and electrons is provided by the visible X-ray emitted when electrons pass the interleaved radiators.

1.3.8 Magnet System

The ATLAS superconducting magnet system consists of three large air-core toroids that generate the magnetic field for the Muon Spectrometer and a central solenoid (CS) that

provides the magnetic field for the Inner Detector. The magnets are kept cool by helium at 4.5 K, which is supplied by a central refrigeration unit in the side cavern. To achieve the desired calorimeter performance, the CS is placed in front of the EM calorimeter and must be as thin as possible. As a result, the CS is built into the LAr vacuum vessel, avoiding the need for two additional vacuum walls. The central field's nominal strength is 2 T, with a peak magnetic field of 2.6 T at the superconductor. A magnet current is provided by a dedicated network of high current conductors from a Un-interrupted Power Supply (UPS). The central solenoid is powered by a 8 kA power supply, and the barrel toroid is powered by 20 kA supply. One barrel toroid (BT) and two end-cap toroids make up the eight air-core toroids (ECT). Each toroid is made up of eight double-pancake racetrack coils arranged symmetrically around the beam axis. The barrel toroid's coils are housed in independent cryostats, whereas the end-cap toroids are housed in a single huge cryostat. The superconductors in the barrel and end-cap toroids have peak magnetic fields of 3.9 and 4.1 T, respectively. A power supply powers the toroid coil system. An aluminium-stabilized NbTi superconductor is employed to achieve the requisite high magnetic fields. To provide appropriate mechanical strength, it is contained in the core of an aluminum alloy case. A sufficient and proven quench prevention system has been built to prevent the coils from overheating. The partition scheme of the barrels consists of two central long barrel segments (LBA, LBC) which are serviced from both sides aswell as the shorter extended barrel segments (EBA, EBC) at each end.

Chapter 2

The Tile Hadronic Calorimeter system

The ATLAS Tile Hadronic Calorimeter system [35, 36, 33] is designed to absorb particles coming from the collision point and measuring their energy, with the exception of the energy carried by muons, neutrinos and potentially any undiscovered weakly interacting particles. As electromagnetic particles scatter shower and lose energy more quickly than hadrons, the ATLAS calorimeters are subdivided into inner electromagnetic calorimeter and outer hadronic calorimeter layers, each optimized for the particles that they measure. Photons, positrons, and electrons in the Electromagnetic Calorimeter undergo bremsstrahlung and pair creation as they move through matter, resulting in a shower of secondary particles until there is insufficient energy to continue these processes. Particle showers are initiated in the Hadronic Calorimeter by hadrons interacting with atomic nuclei as they pass through the detector. In both scenarios, the incoming particle energies can be obtained by measuring the energy deposited by the cascades they generate. The Electromagnetic Calorimeter covers the $|\eta| \leq 3.2$ pseudo-rapidity region, a hadronic barrel calorimeter covers $|\eta| \leq 1.7$, hadronic end-cap calorimeters cover $1.5 \leq |\eta| \leq 3.2$, and forward calorimeters cover $3.1 \leq |\eta| \leq 4.9$ [35, 36, 33].

2.1 Liquid Argon Calorimeter

The ATLAS Electromagnetic Calorimeter depicted in Figure 2.1, also known as the Liquid Argon Calorimeter, is made up of two parts: a barrel that covers $|\eta| \leq 1.475$, and two end-caps that cover the region $1.375 \leq |\eta| \leq 3.2$. This subsystem's barrel region is made up of two identical half-barrels separated by a 6 mm gap at z = 0, while the end-cap region is made up of two coaxial wheels on each side. This calorimeter includes Copper-Kapton electrodes submerged in liquid Ar at –183°C with layers of lead and stainless steel absorber plates over its whole surface area [37]. The electrodes and absorber plates are placed in an accordion-shaped geometry to ensure perfect ϕ symmetry without azimuthal cracks. For better energy resolution, the lead thickness in the absorber plates was tuned as a function of η.

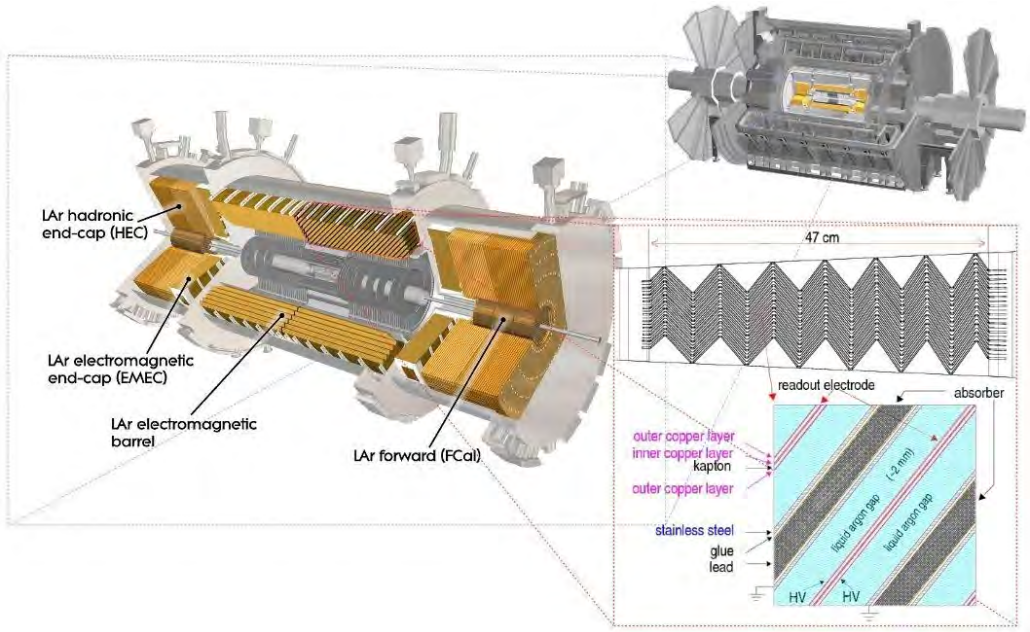

Figure 2.1: The Liquid Argon Calorimeter [36].

2.2 Hadronic Calorimeter overview

In ATLAS, the Hadronic Calorimeters are adapted to meet the various requirements and radiation exposures. The Tile Calorimeter, the LAr Hadronic End-cap Calorimeter (HEC), and the LAr Forward Calorimeter are three separate hadronic detectors (FCAL). HEC and FCAL were chosen for the larger pseudorapidities where higher radiation resistance is needed because of the intrinsically radiation-hard LAr technology. The following are the main objectives of hadronic calorimetry:

- to identify and measure the energy and direction of jets
- to measure the total missing transverse energy (E_T^{miss})
- and to improve the EM calorimeter's particle identification by measuring quantities such as leakage and isolation

The thickness of the hadronic calorimeter is a key metric in achieving these goals. Measurement and simulations showed that the total thickness of 11 interaction lengths (λ) is sufficient to reduce passage through to the muon system and provide good containment for hadronic showers.

2.2.1 Tile Calorimeter

TileCal is a sampling calorimeter [15, 34] using iron as the absorber and scintillating tiles as the active material (Figure 2.2). As the high energy hadron travels through the steel

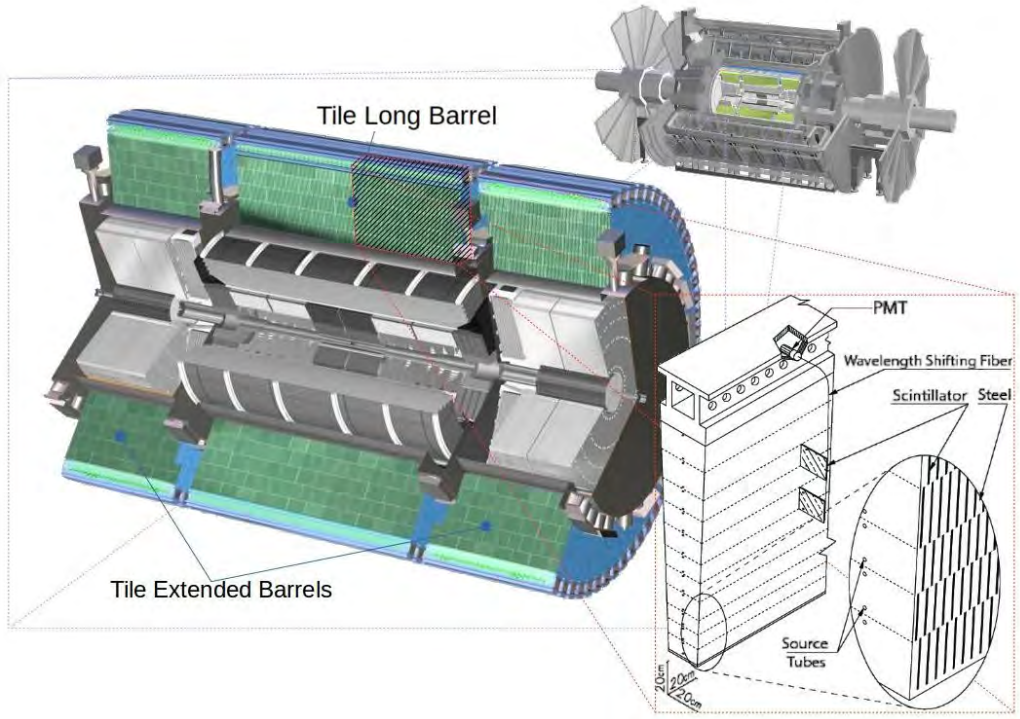

Figure 2.2: The Hadronic Tile Calorimeter [34].

tiles, they interact with the atomic nuclei. As the particle showers pass through the scintillator tiles, they excite atoms, which then emit photons as they return to their ground state. Wavelength shifting (WLS) fibres collect a portion of the emitted light from opposite sides of the scintillating tiles and provide it at a different wavelength to pairs of photo-multiplier tubes (PMTs). From the collected photons, the PMTs generate signals that are shaped into unipolar pulses of FWHM of 50 ns. The energy of the total light produced is proportional to the energy deposited by the hadron.

2.3 Current Superdrawers and front-end electronics

An EB module is read out by 32 PMTs housed in a super-drawer along with the associated electronics. The calorimeter Super-Drawers (SD) are positioned at the calorimeter's outer radius. There are 2 SD, each housing 45 PMTs and related electronics, which are all read out by an LB module. The total number of PMTs is 9852, with two PMTs reading nearly all calorimeter cells for redundancy. In the current system, the super-drawers are two 1.5 m long drawers with a common power and read out. The Front-End-Board (FEB), Digitiser Board, Interface Board, and Trigger Summing Board are the four boards that make up the present on-detector electronics. The FEB amplifies (Bi-gain x1, x64) and shapes PMT signals as well as preforms calibration functions. The first-level calorimeter trigger (L1Calo) uses analog signals that correspond to the pseudo-projective towers of 0.1 x 0.1 in $\Delta\eta$ x $\Delta\phi$ [34, 38]. TileCal generates the towers signals by summing the

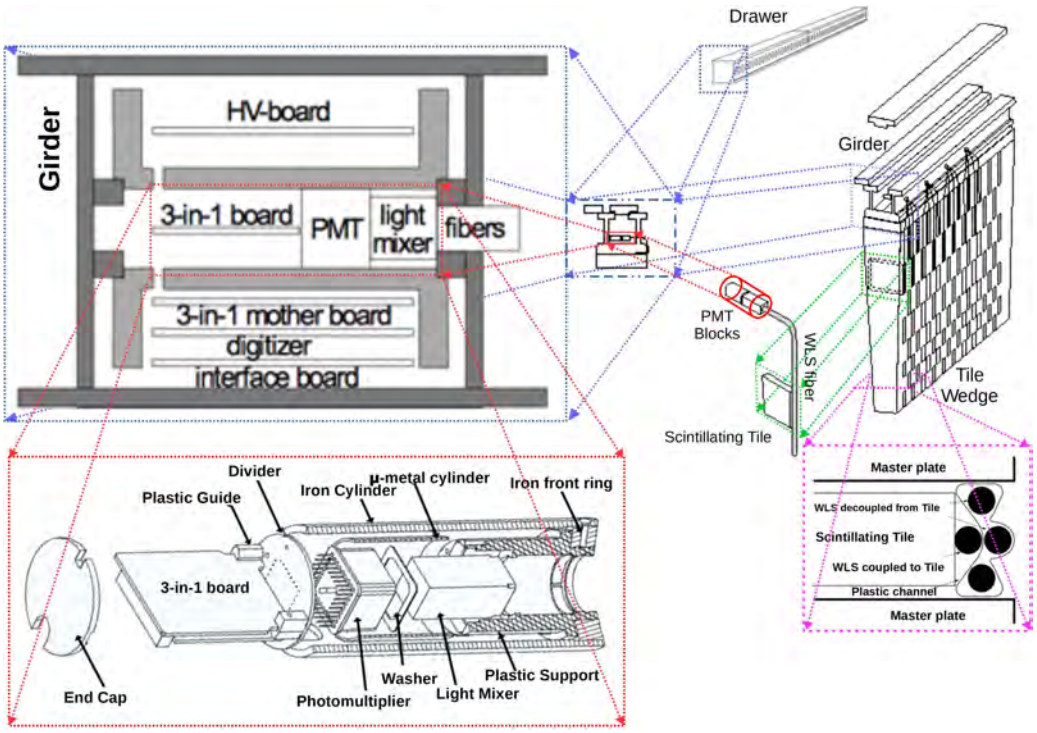

Figure 2.3: TileCal wedges, optical components, drawers and on-detector electronics distribution [34].

analog signals from each FEB using the Trigger Sum Board. The sum outputs are sent off-detector to the trigger pre-processor system through 90 m cables. The signals from the FEBs are digitised at bunch crossing frequency by the Digitiser board and stored on local pipeline memories until an L1Calo accept Trigger is received.Whenever the data is selected by the L1Calo, it will be routed to the Interface board,where it will be serialized and sent off-detector to the Read-Out Driver (ROD). The ROD further formats the data before sending it to the Data Acquisition System (DAQ). The Level 1 trigger selection process reduces the data rate from 40 MHz at the PMT output to a more manageable 100 kHz after the interface board [34].

2.3.1 PMT Blocks

The PMT blocks can be precisely positioned in front of their WLS fiber bundles (See Figure 2.3). Each incorporates a light mixer, a photomultiplier, a high voltage divider, and a 3-in-1 card inside its cylindrically formed structure. The PMTs and electronics are shielded from residual magnetic fields from the ATLAS toroids by a mechanical structure constructed of steel, iron, and -metal. The Hamamatsu R5900 is the PMT of choice, with a tiny size of 28 x 28 x 28 mm^3 and an 8-amplification-stage dynode. A light mixer is positioned between each fibre bundle and the associated PMT photo-cathode to improve light detection uniformity.

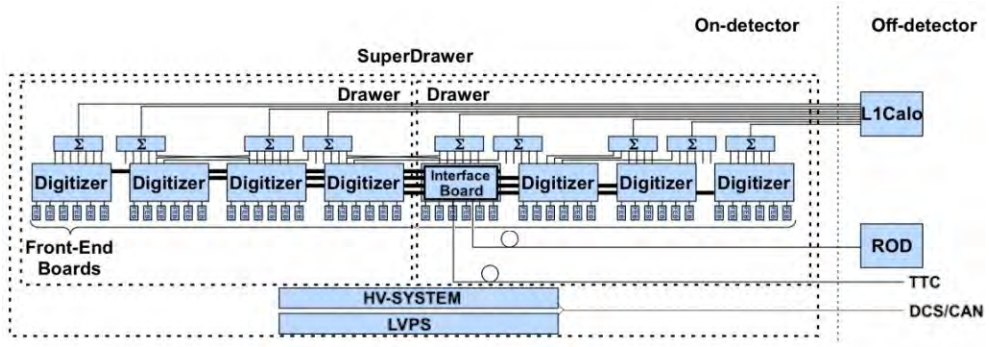

Figure 2.4: The Drawer distribution interfacing between on-detector and off-detector electronics. Digitizer blocks are used to represent 3-in-1 Motherboards and digitizer boards for ease of use [34].

2.3.2 3-in-1 cards

The current front-end electronics of TileCal's electronics, read-out the chain of the 3-in-1 cards. The name comes from the three primary roles they provide: large dynamic range pulse shaping, charge injection calibration, and slow integration of PMT currents for monitoring and calibration. The 3-in-1 cards were designed to have very low noise by reducing active components and taking advantage of the fact that non-active components like capacitors and inductors do not emit the extra noise that many active components do. This device takes fast current pulses with an FWHM of around 15 ns from the PMT and converts them to a unipolar pulse with an FWHM of about 50 ns.

2.3.3 The Level-1 trigger summation boards

The L1 trigger summation boards are located in the drawer's electronics' uppermost layer. Trigger tower signals from the calorimeter systems are required by the off-detector L1 trigger system. The barrel section requirement in TileCal is met by adding five shaped pulses from each of the three cell sampling layers: two from the first layer, two from the second layer, and one from the third layer. Given the overlapping zones for some towers between the barrel and extended barrel, less signals may need to be summed in some circumstances. The off-detector L1 trigger electronics receive the analogue sums produced by the summation boards.

2.3.4 The 3-in-1 Motherboard

The 3-in-1 Motherboards, which are in charge of transferring low voltage power and digital control signals to the PMT blocks, cover the drawer's electronics innermost layer. The Motherboard supplies +5 V, –5 V, and 9 V power, as well as a precise 4.096 V reference voltage with a very low temperature coefficient (0.5 ppm per °C) for each of the 3-in-1 cards charge injection calibration mechanism. The slow integrator and charge injection calibration systems are also controlled by differential digital and analogue buses that

run the length of the Motherboard. The 3-in-1 cards are all identical, but they must be operated and configured differently depending on where they are in the detector.

2.3.5 Digitizer Board

The digitizer board, which is located on the drawer's second layer, receives analogue shaped pulses from the 3-in-1 cards 2.4. The TileDMU and the TTCrx [39] are two specialized ASICs used on this board. The incoming pulse samples are digitized and temporarily stored in pipelines within the TileDMU. The TTCrx uses the TTC system to receive and distribute synchronized commands and LHC-synchronous clocks from the off-detector electronics. The TileDMU transfers the corresponding data samples for the triggered event to the interface board when the TTCrx receives an L1A signal.

2.3.6 Interface Board

The interface board acts as a link between the drawers and the off-detect electronics. Every super-drawer has a single interface board that sends the digitized data from the digitizer boards to the TileCal ROD. The transmission wires between the interface board and the several digitizer boards attached to it were set up in a star arrangement.

2.3.7 High Voltage Power Supply

A High Voltage Power Supply (HVPS) board system supplies the PMTs, which is separated into 256 independent and electronically equivalent sub-modules. Each sub-module is connected to an HVPS board in a super-drawer, allowing it to supply High Voltage to up to 48 PMTs. Each sub-module delivers common voltage via the off-detector HV source, which can be -700 V, -900 V, or -1100 V with a current of 20 mA. Each PMT channel can be adjusted by up to 350 V from the common voltage in the super-drawer.

2.3.8 Low Voltage Power Supply

The Low Voltage Power Supply (LVPS) system's on-detector part is known as a LVPS Box or fLVPS. It consists of a box that is plugged into each module finger [34]. The LVPS Box regulates the power for a single super-drawer from a central location. The LVPS Box distributes 300 W to the super-drawer on average via eight separate output voltages, powering the HVPS board (–15 V, 15 V, and 5 V), the 3-in-1 Motherboards (15 V, –5 V, and 5 V), and the digitizer boards (5 V and 3.3 V). The CAN Open protocol is used to connect the 256 LVPS Boxes for control and online monitoring.

2.3.9 Charge calibration system

Electronic pulses of different amplitudes can be injected into the system to test the behavior of each channel's digitization and read-out chain over its whole dynamic range. By injecting a known charge into the input of the 3-in-1's shaper-amplifier stage and monitoring the response ($\frac{pC}{ADCcounts}$) of the digitized read-out, these imitate PMT pulses. A pair of capacitors on the 3-in-1 cards are charged to a known voltage by a 10-bit Digital to Analogue Converter (DAC), with a precision reference voltage given from the Motherboard, in the Charge Injection Scan (CIS) system. The commands are interpreted by the TTCrx on the interface board and distributed to the 3-in-1 through the motherboard. An analogue switch discharges the capacitors into the analogue chain when a discharge signal is received via the TTC.

2.3.10 Laser calibration system

The high-power LASER system sends short, regulated light pulses to the light mixers in the PMT blocks through optical fibres. In the absence of collisions, this allows measurements of individual PMT gains. The light signals received by each PMT are converted into shaped analogue pulses in the 3-in-1 cards, which are then read by the digitizer. The CIS and LASER systems may test and calibrate the PMTs and down-stream electronics individually by giving calibration pulses before and after the PMT. The LASER calibration system is utilized for quick TileCal monitoring, time calibration, and channel-by-channel gain correction calculations.

2.3.11 Cesium source calibration system

Radioactive ^{137}Cs γ sources are transferred hydraulically through water-filled tubes that pass through each scintillating tile in the calorimeter in the Caesium system. The WLS fibres collect scintillation light and transport it to the PMTs. Because the Cs source generates powerful, slow signals that would saturate the 3-in-1 shaper, a separate read-out channel with a slow integrator circuit and ADC, as well as CANbus read-out, has been constructed [34].

2.4 Trigger and Data Acquisition

The luminosity (L) of an accelerator is defined as the proportionality factor between the number of events per second $\partial N/\partial t$ and the cross section σ. The LHC could achieve around 20 collisions per crossing with nominal beam currents. Particularly for p-p collisions, the luminosity is reduced to the proportionality constant between the number of inelastic particle collisions in a certain time and the inelastic cross section. The original design luminosity of the LHC is 10^{34} cm^{-2}s^{-1} [40], which was chosen chosen for research of physics processes with very small cross sections. For reading out all detector channels

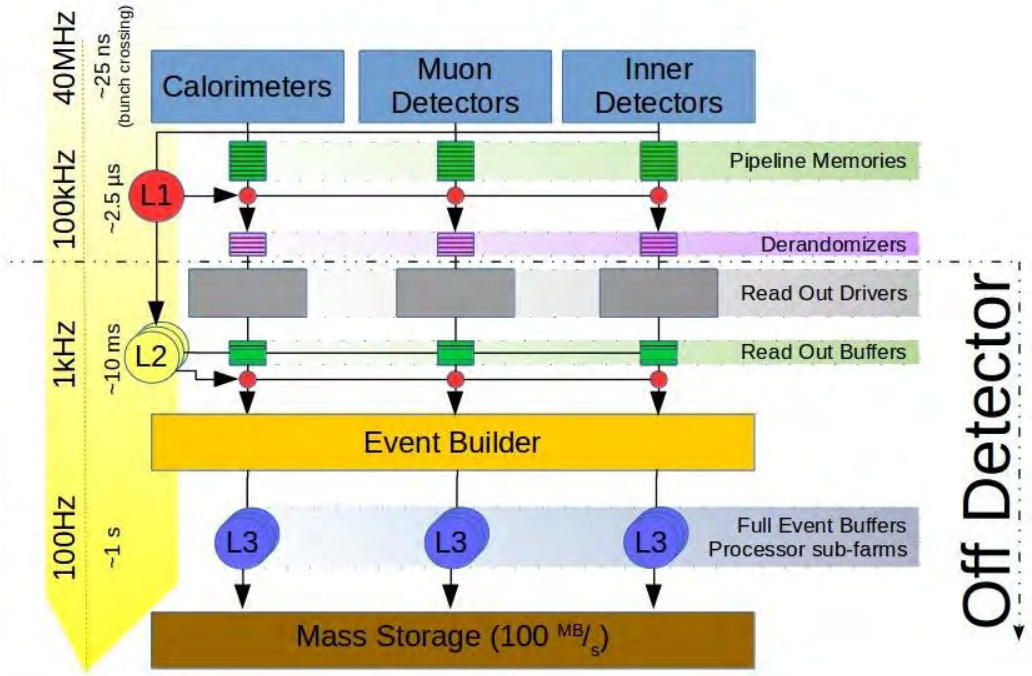

Figure 2.5: The ATLAS TDAQ system with three levels of event selection [31, 40].

at the same bunch crossing, the typical data size is around 1 MB. Given the 40 MHz bunch crossing rate, the massive volumes of data generated are impractical to store or analyse. Since a major fraction of the events will not contain interesting physics, processing and storing all of the data generated is neither practicable nor valuable.

The ATLAS trigger system was designed to be able to distinguish between interesting events and store as much of them as possible. The trigger system, as illustrated in Figure 2.5, consists of three levels of event selection, each of them refining the decisions made in the previous level, and consequently reducing the event rate by orders of magnitude by applying additional selection criteria. The Level-1 trigger (L1) is a hardware-based trigger that operates at a 100 kHz output rate. The L1 decision is based on a coincidence or veto criterion for different object combinations, which is obtained from reduced granularity data from a subset of detectors. The Level-2 trigger (L2) is software-based and reduces the rate to 1 kHz by processing energy sums, position and p_T of candidate objects. Despite the fact that L2 has complete access to all event data with full precision and granularity, it usually only needs the data in the region-of-interest defined by the L1 trigger. The level-3 trigger (L3) is also software-based and it operates by filtering events by confirming the results of L2 decisions and then using L2 data to seed its own analysis. The final rate at L3 is 100 Hz, which translates to around 100 MB/s, with an event size of about 1 MB. In order to be able to handle these high rates, parallel processing is employed in all trigger levels [31, 40].

Chapter 3

The Phase-II Upgrade programme for the HL-LHC

3.1 Phase-II Upgrade overview

The High-Luminosity era for the LHC is motivated by the potential to extend and improve contributions to the LHC physics program, as well as to help bring the scientific community closer to answering fundamental questions of particle physics. Measurements of rare Higgs decays and Higgs self-couplings, as well as extending the reach of searches for new phenomena like as supersymmetry, quark and lepton substructure, and new gauge bosons, are among the HL-LHC targets [40]. Taking data at the High-Luminosity LHC requires significant upgrades to most of the ATLAS subsystems to handle the expected higher detector occupancies and the harsher radiation environment. For geometrical considerations, HL-LHC will have the greatest influence on subsystems with low radii and large pseudorapidity. Given the considerable impact of high particle fluxes and radiation damage on each of them, replacements or significant modifications in the Inner Detector, foward calorimeter, and forward muon wheels are expected. Subsystems like barrel calorimeters and muon chambers, on the other hand, are projected to be capable of handling the new high luminosity environment, thus they won't be changed. Upgrades to ATLAS will include modern technology like radiation hard tracking detectors with better granularity and bandwidth, as well as radiation-hard FE electronics.All of these upgrades will result in higher event rates and larger event volumes, necessitating a major expansion of the trigger and (DAQ) systems [31].

ATLAS upgrade plans are divided into three main phases, corresponding to three long technical shut-down periods of the LHC [11, 12, 13]. The Phase-II is anticipated for 2027-2031 and will span around three years. Installation of new inner triplet magnets and eight crab cavities near ATLAS as part of the LHC upgrade will maximize the overlap of the proton beams at the collision location by compensating the crossing angle. Luminosity leveling will also be enabled, allowing the instantaneous luminosity to be maintained at

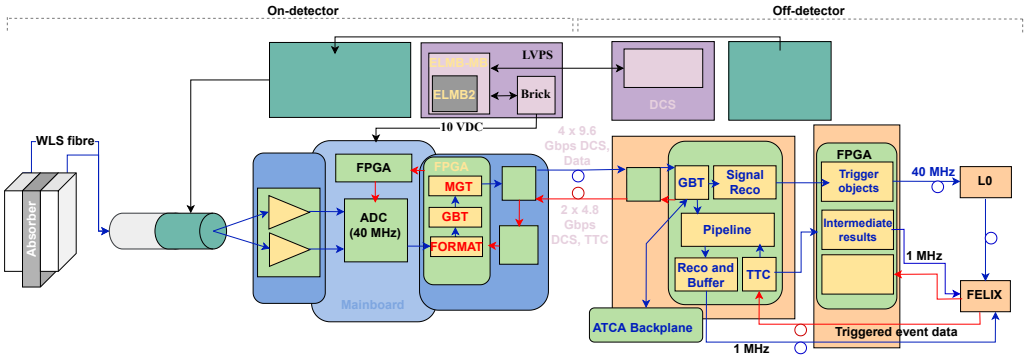

Figure 3.1: Phase-II Upgrade electronics diagram [30].

a constant value for extended running durations and limiting peak pile-up in the experimental detectors. The improved LHC is expected to have an instantaneous luminosity of around 5×10^{34} cm^{-2}s^{-1}. Phase-II upgrade plans for ATLAS include a redesigned Inner Detector without TRT, as well as additional trigger and calorimeter upgrades. The Wits University, ICPP has been involved with ATLAS TileCal and are responsible for producing and testing the upgraded LVPS system. A major part of the Phase-2 TileCal upgrade activities is a replacement of the on-detector and off-detector read-out electronics for improved resolution, better trigger performance, and radiation tolerance for the HL-LHC running conditions [11, 12, 13, 14, 15].

3.2 TileCal Phase-II Upgrade

The concern with gradually increasing the luminosity is that it will push the original ATLAS trigger and data gathering system beyond its limits. This raises the question of how to adapt ATLAS to these new conditions. The current trigger implementation will not be able to cope well with these luminosity values [12, 13, 15, 37, 38]. Since it was considered difficult to increase the input rates to the second level trigger, the first level trigger would have to be made more selective. For each bunch crossing, roughly 20-40 proton-proton collisions will occur under normal conditions, although this number might increase to 400 after Phase-II. More effort will be required to investigate these collisions. A simple way to reduce trigger rates is simply to increase the thresholds, but this would have a significant impact on physical performance. Implementing new, more advanced algorithms is a better option, but this necessitates giving the trigger with more and better data. The triggers, particularly the first-level trigger, will be significantly modified during the upgrades. Real-time topological algorithms will create more selective trigger judgments immediately after Phase 0 to increase physics performance without increasing rates. After Phase 1, the isolated-lepton, jet, and energy-summation triggers will be replaced by new feature extraction processors. For improved isolated lepton identification, they will

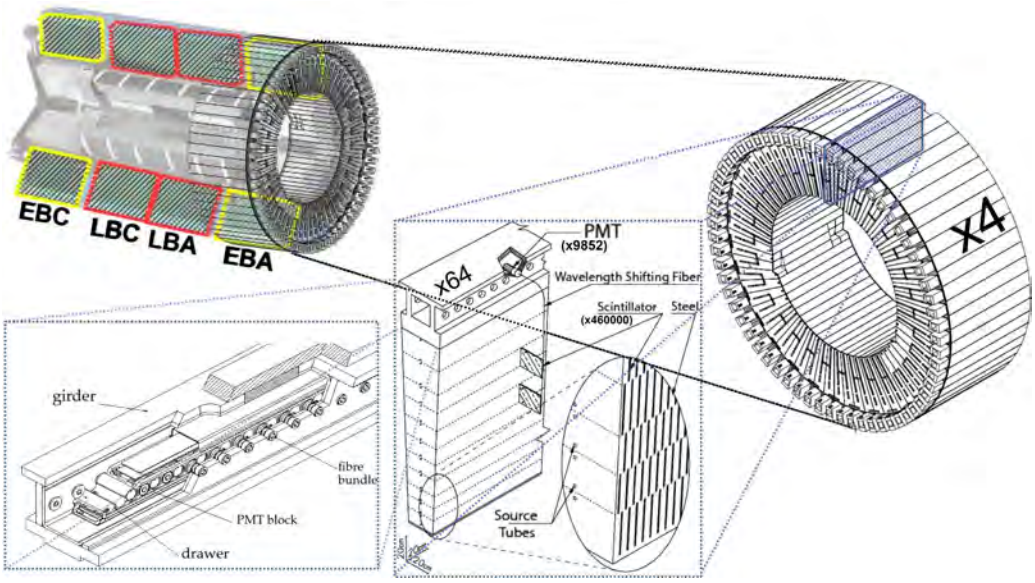

Figure 3.2: A general segmented image of TileCal [34].

leverage finer-granularity trigger data from the modified LAr calorimeter front end electronics, which will help reduce the impacts of pileup on jet and sum-ET triggers. The current analog trigger inputs for the first level trigger will be decommissioned during Phase-II , and the first level trigger will be separated into a level 0 and level 1 trigger with greater input rates and longer latencies to allow for additional processing. The muon detector will also be upgraded to improve the efficiency of its trigger, reducing the problem of fake muons by ensuring that reconstructed tracks come from the interaction region. In Phase 1, one element of the muon detector system, the so-called little wheels, will also be replaced. The TileCal, is a sampling calorimeter built with layers of steel absorber material alternating with scintillating plastic tiles as active material. High energy particles interacting with the steel plates produce showers of secondary particles. These are then sent through the plastic scintillator tiles, which, when stimulated, emit ultraviolet (UV) light. Organic compounds added to the plastic convert the UV radiation into visible blue light [35, 36, 33]. The scintillating light propagates through the plastic tile to the wedge's edges on both sides, where wavelength shifting (WLS) fibres absorb it and re-emit it at a longer wavelength (green). the majority of the green light is trapped within the WLS fibres by total internal reflection, and propagated to PMTs at the rear girder of the module. The PMTs convert the light to electrical signals which the on-detector electronics process and read out. The steel plates and 460000 scintillating tiles are radially oriented with regard to the xy plane. The optical read-out of Tilecal is radially segmented into three layers, with the steel and scintillator staggered in between layers [35, 36, 33]. Although the scintillating tiles are all 3 mm thick, their radial and azimuthal lengths vary in eleven various sizes, ranging from 97 mm < r < 187 mm to 97 mm < l azimuth < 187 mm.

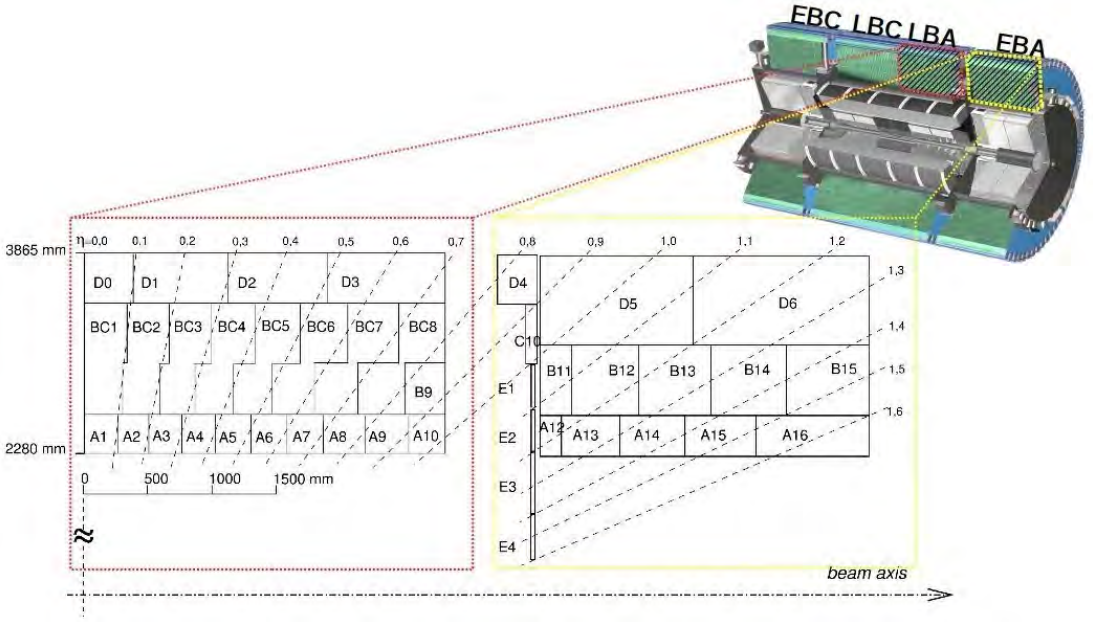

Figure 3.3: TileCal read-out cell mapping for contiguous long barrel (LB) and extended barrel (EB) wedges. This cell distribution is symmetric respect to the interaction point [34].

TileCal's steel-to-scintillator ratio is 4.7, allowing hadrons to travel an effective nuclear interaction length of λ = 20.7 cm before encountering an inelastic nuclear interaction. The TileCal is split longitudinally into four cylindrical barrel sections, each of which is made from 64 wedge shaped segments with a ϕ granularity of approximately $\Delta\phi$ = 0.1 radians, as shown in Figure 3.1. The two central barrel segments cover the pseudo-rapidity range –1.0 η < 1.0 and together they make up what is known as the long barrel (LB). The two remaining barrels segments are called the extended barrels (EB) and are located on each ends of the Long Barrel covering the region between 0.8 < | η | < 1.7. The ATLAS detector is divided longitudinally into sides A and C around z = 0, resulting in the names EBA, LBA, LBC and EBC for the 4 barrel sections. The barrels are radially segmented into 1.5, 4.1 and 1.8 λ in the case of the LB, while the EB is radially segmented into 1.5, 2.6 and 3.3 λ, giving a total calorimeter depth of 7.4 λ at η = 0. For each module the η segmentation is $\Delta\eta$ = 0.1 for layers A and BC, and $\Delta\eta$ = 0.2 for layer D. As a result, each cell has a transversal segmentation of $\Delta\eta \times \delta\phi$ = 0.1 × 0.1, or 0.2 × 0.1 for layer D. The TileCal modules are segmented into read-out cells with three dimensional coordinates r, ϕ and η by bringing bundles of WLS fibres from the scintillating tiles in each cell to separate PMTs. The TileCal detector's 5182 read-out cells is read-out by a pair of PMTs, one for each side of the wedge-shaped module. The TileCal segmentation is also designed to organize the cells into so-called "trigger towers" pointing back towards the nominal contact point and with η range in steps of around 0.1 radians to supply valuable hadronic data to the L1 trigger as seen in Figure 3.3. There is also a gap region between the LB and the EB which is equipped with unique cells. The longitudinal and radial segmentation of the

cells in each module is designed to build approximately 2000 projective trigger towers in η. Each trigger tower's cells are added together and fed into the ATLAS L1 calorimeter trigger. The girders at the back of each wedge house two extractable aluminum drawers, each of which can hold and serve up to 24 PMTs. The two drawers in each module are connected together mechanically and electrically to form a so-called super-drawer.The super-drawers hold all of the on-detector electronics in addition to the PMTs.The analogue shaping and amplification of PMT pulses, signal digitization, pipelined read-out of sampled data, and systems for calibration and high-voltage distribution are all handled by these electronics.

3.3 Phase-II upgrade readout electronics

3.3.1 Mechanics

In Phase-II, TileCal will replace the current drawer structures with structures half the length of the current drawers to improve accessibility, robustness, and lower the magnitude of a possible single point of failure. The new 70 cm-long mechanical structures are called mini-drawers (MD). For the upgraded detector, A superdrawer for the upgraded detector will be made up of four independent mini-drawers for LB, each with its own power and signal pathways to the back-end electronics. Each MD will host 12 PMTs, 12 Front-End-Cards (FENICs), 1 Main Board, 1 Daughter Board and 1 HV passive distribution board. The EB will have 3 mini-drawers and 2 micro-drawers, which are additional drawers that hold the PMTs in place but do not contain digital circuitry [38, 41].

3.3.2 Photomultiplier blocks

Due to ageing, approximately 10% of the PMTs located inside the PMT blocks will be replaced. The PMT blocks can be accurately positioned in front of their respective WLS fibre bundles. Each PMT block incorporates a light mixer, a photomultiplier, a high voltage divider, and a FENICS card inside its cylindrically formed structure. The mechanical structure is made of steel, iron and μ-metal to shield the PMTs and electronics from up to 500 Gauss from residual magnetic fields from the ATLAS toroids. A light mixer is positioned between each fibre bundle and the associated PMT photo-cathode to improve light detection uniformity. The HV divider, in addition to distributing different high voltages between the dynodes of the PMT, also provides interconnects between the PMTs and the FENICS cards via the sockets in the PMT base [41, 42, 43].

3.3.3 Front End board

The electronics at the front of the read-out chain are called Front End boards (FENICs). TileCal developed a Front End board for the new infrastructure with Signal Shaping and Calibration, which shapes and amplifies PMT analogue signals. FENICS provides two

types of read out: The "fast readout" for physics operates in two distinct gains to cover a dynamic range of 200 fC energy of a minimum-ionizing-particle (MIPS) to 1000 pC, while the "slow integrator readout" integrates the PMT current for calibration of the calorimeter with a 137^{Cs} γ source and luminosity measurements. The FENICS will provide improved precision and better noise performance. The prototypes have been properly validated for the radiation levels envisaged at the HL-LHC and are currently in the pre-production phase [44, 45, 46].

3.3.4 Mainboard

The Mainboard (MB), which is in charge of transferring low voltage power and digital control signals to the PMT blocks, is the innermost layer of the drawer's electronics. Each MD has a Mainboard (MB) that takes data from the FENICS, PMTs, digitizes it, and sends it to the DaughterBoard (DB). The fast read out uses 24 12-bit ADCs at 40Msps, while the integrator readout uses 12 16-bit SAR ADCs. The FENICS cards are all the same, but they must be controlled and set differently depending on their location in the detector. For that purpose, the Motherboard handles address decoding and selection according to each of the FENICS card locations. The Motherboard is responsible for address decoding and selection for each of the FENICS card locations. The Mainboard has been completely qualified for the radiation environment that may be encountered [44, 45, 46].

3.3.5 Daughterboard

The on- and off-detector systems are linked by a Daughterboard (DB) installed on the MB. It receives and propagates LHC synchronized timing, configuration, and control commands to the front-end electronics, as well as reading, formatting, and transferring data from MB channels to off-detector systems. Each DB is equipped with two Kintex Ultrascale FPGAs [38, 46, 47]. Both the MB and the DB have been developed with two electrically independent sides for added robustness. The digitizer board sits on the second layer of the drawer and receives the analogue shaped pulses from the FENICS cards. This board takes advantage of two custom ASICs: the TileDMU and the TTCrx. The incoming pulse samples are digitized and temporarily stored in pipelines within the TileDMU. The TTCrx uses the TTC system to receive and distribute synchronized commands and LHC-synchronous clocks from the off-detector electronics. The TileDMU then transfers the necessary data samples for the triggering event to the interface board when the TTCrx receives an L1A signal [46, 47].

3.3.6 High Voltage Power Supply

The PMTs are powered by a High Voltage Power Supply (HVPS) board system, which is divided into 256 independent and electronically equivalent sub-modules and supplies a common voltage via an off-detector HV source that can be –700 V, –900 V, or –1100 V with

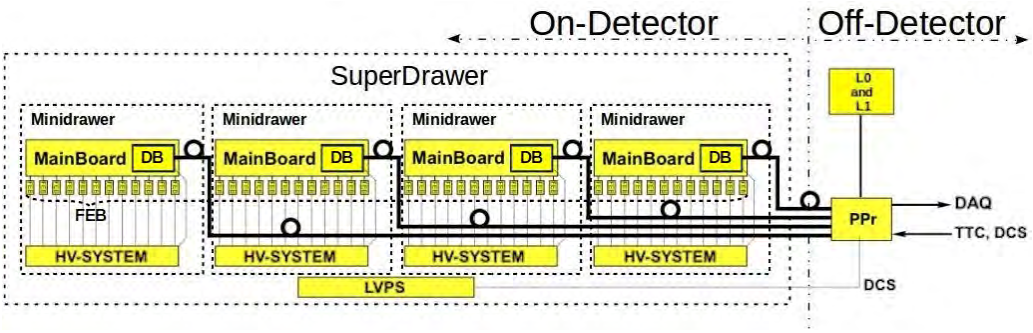

Figure 3.4: Drawer distribution of TileCal upgrade and interface between on-detector and off-detector electronics [49].

a current of 20 mA. To maintain linearity even at high luminosity, high PMT current require active dividers, hence current passive dividers will be replaced with active dividers. Unlike the current system, the HV distribution system will be controlled remotely at the HV regulation board, now known as the HV remote board, which is located outside of the detector's radiation environment in the USA15 cavern. Regulation board prototypes have been evaluated and shown to meet the HV stability requirements [38, 48].

3.3.7 Low Voltage Power Supply

The TileCal Low Voltage Power Supply (LVPS) provides power to all of the TileCal's front-end electronics of the TileCal. The current LVPS system has a two-stage LV distribution system, whereas the improved LVPS distribution system has three stages. The LVPS are the TileCal component that is most exposed to radiation due to their position in the detector located adjacent to the finger. Multiple radiation test campaigns have been conducted in order to select the best components. All LVPS Bricks convert the 200 V input from the bulk supply in the USA15 cavern to 10 V for the front-end electronics, which is then transformed to various voltages by Point-of-Load regulators. The LVPS Bricks are designed with better reliability, lower noise and improved radiation tolerance. The monitoring of the Bricks is being done by an ELMB (Embedded Local Monitoring Board) chip, hosted by an ELMB motherboard (ELMB-MB) inside the LVPS Box. The ELMB motherboard has been re-designed to be compatible with the new Tri-State control method of the LVPS Bricks. The LVPS system was fully prototyped and tested in vertical slice test with both on and off-detector elements [38, 41, 42]. This will be discussed in greater detail in chapter 4 as it falls within the scope of the thesis.

3.4 Back-end electronics

The upgraded back-end electronics system will be housed in the USA15 racks (same as the current set-up), 70 meters away from the detector. The Phase-II Tile PreProcessor modules and the Trigger and DAQ interface (TDAQi) boards are two separate systems

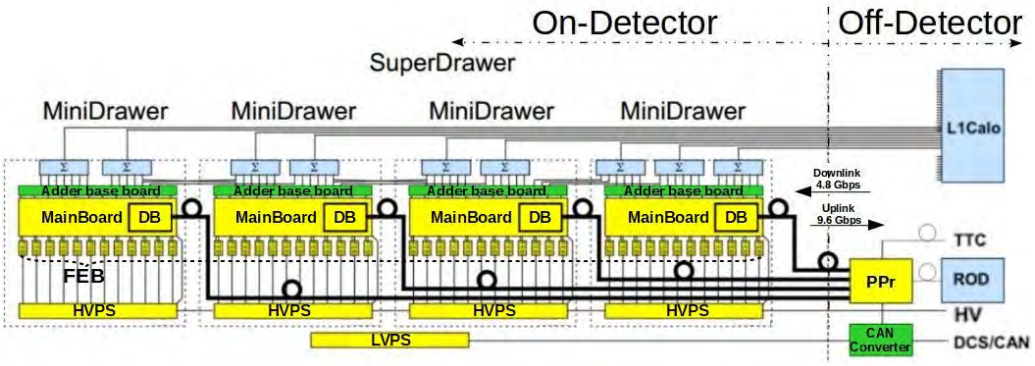

Figure 3.5: Drawer distribution of the Demonstrator and interface between on-detector and off-detector electronics [49, 51].

that make up the Phase II Tile back-end electronics. The Advanced Telecommunications Computing Architecture (ATCA) requirements are used in the Tile back-end electronics system [45, 46, 47]. The ATCA framework provides a commercially and standardized platform for high-speed serial interconnects on the back plane supporting different I/O interfaces.

The PreProcessor (PPr), which is housed in the counting rooms, collects data from the detector and uses digital filters to compute energy and time for each PMT channel. The pipeline buffers are transferred to the PPr, as opposed to the current system, which includes on-detector data pipelines. PPr is made up of CPMs (Compact Processing Modules) [50, 51], housed by an ATCA (Advanced Telecommunications Computing Architecture) carrier board, which process data from two TileCal modules. An ATCA carrier is utilized to provide a connection between the CPMs and Trigger and Data AcQuisition interface board (TDAQi) [50, 52, 53, 54].

3.5 Demonstator Project

The different components of the upgraded TileCal electronics have been developed in parallel by an international collaboration of ATLAS institutes and universities. A TileCal Demonstrator project was initiated with the purpose of inserting and testing the new hardware in the ATLAS detector for functionality, performance, and integration tests in order to ensure that the new system can be effectively integrated and operated in the HL-LHC environment. In order to operate within ATLAS, the Demonstrator is also required to maintain compatibility with the legacy TileCal hardware, so that it can operate in parallel with the legacy ATLAS systems without compromising data taking [48, 55, 50].



Figure 3.6: Picture of the Tile PreProcessor Demonstrator [55].

3.5.1 Demonstrator system and readout chain

As shown in Figure 3.5, the demonstrator is a fully functional Phase-II read-out prototype compatible with the current system (i.e. the legacy-to-be system after the Phase-II upgrade). The Demonstrator module provides energy measurements for every calorimeter cell, as well as the analog trigger sums that are sent to the current Level-1 trigger. The Demonstrator consists of four MD's, each of which can service up to 12 PMT channels, and a Superdrawer (SD) that divides a legacy TileCal drawer into four. The SD will digitize two gains of up to 48 TileCal PMTs in real time and transfer the digitized sampled data to the off-detector systems at a rate of 40 MHz. Calorimeter samples corresponding to each cell are transferred at 40 MHz to the off detector electronics through optical links, using the novel read-out architecture [56, 57].

The Off-detector electronics will be used to reset data in the pipeline buffers that are awaiting for a trigger decision and in parallel, provide the rebuilt data to the trigger system. The reconstructed information includes calibrated energy per cell or group of cells. After the trigger decision, The selected data will be sent to the central ATLAS data gathering system. The PreProcessor is the core element of the back-end system, providing communication with the front-end to transmit commands and to receive the digitized PMT data [51, 49]. Following the received trigger signal, the data are transferred off-detector to be stored in pipelines, then reconstructed and triggered-out by the TileCal PPr, which accepts legacy Timing Trigger and Control commands and triggers, as well as Detector Control Systems commands, and provides the triggered data.

The Demonstrator maintains compatibility with the current TDAQ system by providing legacy analogue trigger outputs to L1Calo, receiving ATLAS triggers and slow control (SC) commands and timing via the TTC system, and interfaces with existing detector control and operation monitoring systems. A block schematic of the Demonstrator is shown in Figure 3.6. To maintain compatibility with the legacy systems, the Mainboard and front-end boards are capable of providing analogue sums to the legacy L1Calo via the legacy summation boards. The Daughterboard [50] provides timing and propagates the configuration commands sent by the TilePPr [55], which in turn receives ADC data and conditions data from the Daughterboards, receives and decodes TTC commands and triggers from the legacy TDAQ, and reads out triggered data to the legacy ROD [15]. Data taking and results showing the response of the various particles with different beam energies and incident angles were done in 2018 and 2021 [51, 49, 56].

Chapter 4

TileCal Low Voltage Power Supply System

4.1 Low Voltage Power Supply

As explained in Chapter 2, the LVPS for the Phase-II upgrade of the TileCal LVPS (Low Voltage Power Supply) [52, 53, 54] system provides the front end electronics with 10V DC. In the finger adjacent to the superdrawer, a LVPS Box also known as a fLVPS is prepared, which gives feedback and control via a monitoring system. Each LVPS Box has eight DC/DC converters, also known as Bricks, that convert 200V DC input to 10V DC output. This results in a total of 256 LVPS Boxes in the Tile Calorimeter. The LVPS Box is water-cooled, the Bricks are affixed on both sides of the cooling plate which sink the heat inside the LVPS box. The LVPS Box contains an ELMB-MB with an ELMB chip, a Fuse Board distributing 200 V DC coming from ATLAS technical cavern USA15 to the Bricks and an internal cable set connecting elements inside the LVPS Box with outside elements via a 72 pin Harting connector.

The ELMB incorporates a CAN bus protocol for communication that allows for the monitoring of behavioural parameters of DC/DC converters such as Input Current (I_{in}), Output Current (I_{out}), Input Voltage (V_{in}), Output Voltage (V_{out}), and two onboard temperatures (TMEAS2) and (TMEAS3). The Auxiliary boards (AUX-Boards) are located at USA15 and provide control of the Bricks inside the LVPS Box, including the ability to turn each Brick on and off individually. The main difference between the LVPS Phase-II upgrade and the previous versions of Bricks is that all produced Bricks inside the LVPS Box will provide the same output voltage. There are eight types of Bricks in an LVPS box modified for the particular sub-circuit that it is powering in the current system installed in the TileCal. As a result, the output voltage and current of each of the eight Bricks are different. The upgraded Brick design is similar to the existing design [53], with the same box, water-cooled cold plate, and basic footprint as the existing system. The new design, on the other hand, will be unique. Rather than having eight separate Brick types

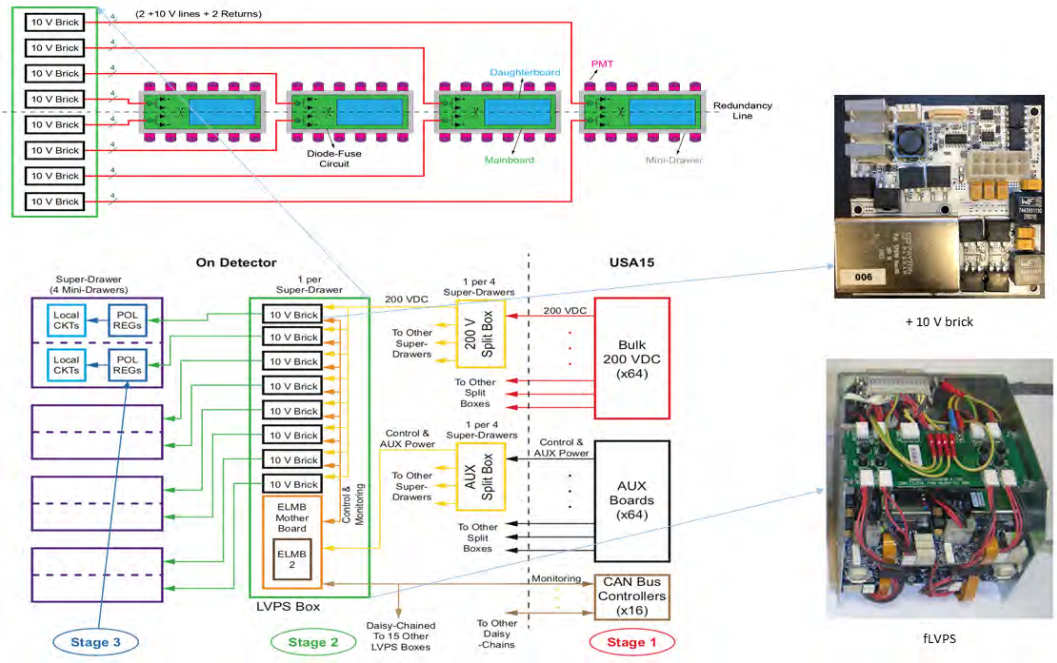

Figure 4.1: TileCal power distribution block diagram. Top left includes the Minidrawer power distribution. Bottom left is the updated 3 phase power distribution scheme. Top right is the image of the LVPS Brick and bottom right is the LVPS Box or fLVPS.

in a box with different voltages and currents, the new design will utilize only one type of Brick, converting the 200V input voltage to a 10V output voltage. The voltages for the individual loads will be created from the output voltage of the Bricks using point-of-load regulators located at the loads [52, 53, 54].

4.1.1 Power Distribution system

A 3 stage power system is used to distribute power from the Low Voltage Power Supplies [34, 56]. A picture of a LVPS box is shown in Figure 4.1. The LVPS Box uses switching "Buck Converter" technology to convert the high voltage, low current power provided from the bulk source, into the low voltages needed by the various sub circuits in the front-end electronics. In comparison to the usage of linear supply, switching technology improves the efficiency of power conversion. In the present system, eight different voltages are generated on Bricks that reside in the fLVPS. The power is distributed to the front-end circuits over cables that run inside the drawer. The TileCal electronics use Point-of-Load (POL) regulators selected for low noise and radiation tolerance [54, 56, 57]. Each Brick supplies voltage to one side of a Minidrawer, and each Mainboard and Daughterboard are operationally divided into independent sides with distinct power sources. The current monitoring and control system utilizes the ELMB (Embedded Local Monitoring Board), attached on top of a custom mother board which provides 32 analogue inputs, 8 analogue outputs and 8 digital outputs.

The control system for the LVPS has two parts. The first is a CANbus interface, which may be used to fine-tune the output voltage, monitor input and output currents and voltages, and monitor temperatures inside the LVPS. The interface in the LVPS uses the ELMB, which is a standard for slow controls in ATLAS. The second part of the control system is based on the sub-system of small power supplies, named AUXBoard which are installed in USA15 as with the bulk 200V DC power supplies. There is one AUXBoard required for 4 startup and shutdown systems (one system per LVPS Box). The second part is a startup and shutdown control system, which provides a "start-up" pulse to the LVPS to get it started, and a current loop to enable and disable the outputs of the fLVPS. The current LVPS Bricks have a well-developed, custom design that has gone through multiple versions. The requirements on the LVPS Bricks [34] are substantially more demanding than can be accommodated by commercial off-the-shelf (COTS) power supplies. These requirements include: good radiation tolerance; compact packaging to fit into the footprint available for the fLVPS; operation in a magnetic field, and low-noise are among these requirements. A summary of the basic performance requirements is shown in Table 4.1. The drawer electronics and the fLVPS are water-cooled to remove the heat from the detector and keep the electronics operating properly. Although the present system is not redundant against individual Brick failures, the design of the current Bricks emphasizes reliability. The estimated mean time to failure (MTTF) of 1.56 Bricks for the LVPS system, which corresponds to approximately 2 failures per year. A recent reliability study was performed on the selected components of the LVPS Brick.

4.1.2 Environmental Constraints

The LVPS boxes are located in the "finger" of the drawer and have a particular metallic shielding, to lower the amount of radiation received and to minimize the influence of the magnetic field, however the shielding does not provide total protection. The residual magnetic field is 0.02 T, enough to have an impact on components such as the power transformers and ferrite chokes. The LVPS boxes are also subjected to the radiation from the calorimeter, in order to better define the radiation constraint for the new design, the computation of the amount of radiation received per 10 years LHC runs at full luminosity was reconsidered by the Radiation Task Force. To cope with these radiation levels over long periods, radiation-resistant components were chosen; large scale tests were effectuated to identify the better ones [34]. While the metallic shielding protects the Bricks, it also encloses them, making it difficult to dissipate heat. In addition to the small dimensions of the Bricks suggests that the heat generators are very dense; in such conditions a robust cooling system is required. A water-cooled plate runs down the center of the LVPS box, with ceramic posts strategically positioned across the bottom side of each Brick providing coupling with the plate. From these conditions linear power supplies would not

Parameter	Value
Threshold for stable load	< 2 A
Over Voltage Protection	11.5 - 12.5 V
Over Current Protection	8 - 10.75 A
Efficiency	> 80%
Nominal Output Power	< 125 W
Duty cycle	30-40%
Frequency	280 - 320 Hz
Input Power	0.24 A
Over Temperature Protection	72° C

Table 4.1: Basic design parameters for the fLVPS Brick [34].

work correctly in the magnetic field and would have a larger size that would not fit in the restricted space of the drawer. In addition switching supplies are more efficient and, as a consequence, have a smaller heat dissipation. The LVPS's maintenance is difficult due to the strict space constraints and limited access to the detector, thus reliability and stability of operations are a critical requirement.

4.2 fLVPS components

4.2.1 ELMB motherboards

The physical mounting point for the ELMB is provided by the ELMB motherboard. The ELMB, wiring from the AUX boards in USA15, the DCS (Detector Control System) CAN-BUS network, and eight LVPS Bricks are all connected to the motherboard. The ELMB can monitor seven parameter for each Brick (voltage input and output, current input and output, two temperatures, and voltage on each Tri-State control line). The Tri-State control lines provide remote enable/on/off control of each of the 8 Bricks independently from each other. Additionally the ELMB2 monitors two temperature sensors at the inlet and outlet of the LVPS liquid cooling plate. The ELMB motherboard also provides capacitive filtering and transient voltage protection of the LVPS Tri-State control lines. One ELMB motherboard is located inside each of the 256 Low Voltage Power Supply (LVPS) boxes that are mounted inside the Tile Calorimeter.

4.2.2 Low Voltage boxes

The LVPS Box powers the front-end electronics for the TileCal. Its location in the overall TileCal low voltage distribution architecture is shown in Figure 4.1 Each box powers one "superdrawer" that is linked to a TileCal module. For the whole TileCal, 256 boxes are required. In the Long barrel (LB) part, a superdrawer has four mini-drawers, whereas the extended barrel (EB) section has three. LVPS Bricks are assigned to supply power to each mini-drawer. Therefore, an LVPS Box requires 8 Bricks for the LB modules, and 6 Bricks

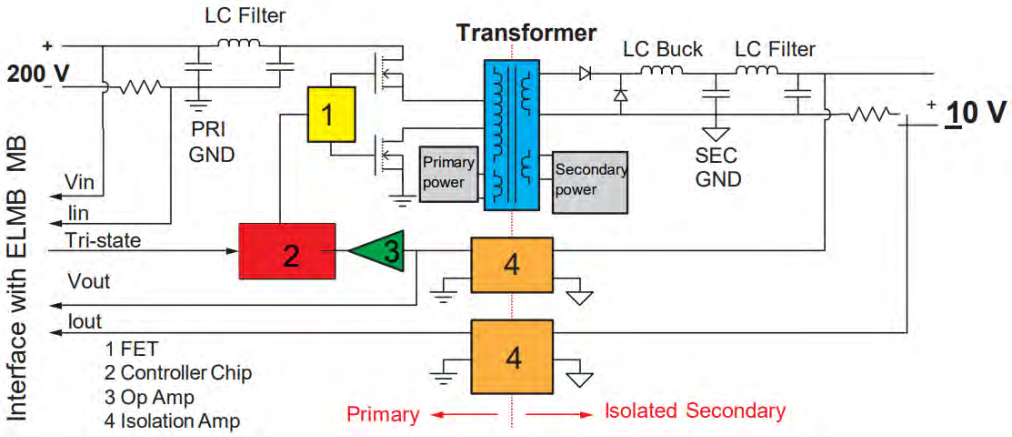

Figure 4.2: LVPS Brick circuitry block diagram.

for the EB modules. For the sake of interchangeability should the need arise, it is prudent to put 8 Bricks in all boxes. In addition to 8 Bricks, each box also houses a ELMB2 a fuse board, cabling connections between the components and I/O, and a water-cooled heat sink, in a steel enclosure that acts as a shield not only against mechanical forces, but also against the ambient magnetic field. The LVPS Box overall physical dimensions are set at 175 mm x 170 mm x 156 mm by the size of the available volume inside the "fingers".

4.2.3 AUX Boards

The AUXBoard is part of the control chain that allows the on-detector low voltage distribution to be controlled remotely. It delivers Tri-State signals for regulating the DC/DC 200/10V Bricks as well as power for the on-detector ELMB. They also have an interlock safety mechanism that shuts down the 200 V input to the Bricks if particular connections or connectors are disconnected. The AUXBoards are VME-based 6U PCBs that are located in USA15. There are 64 AUXBoards, and each one must control four LVPS Boxes remotely.

4.2.4 Upgrade LVPS Brick description and design

The LVPS Brick block diagram of the circuit shown in Figure 4.2. The heart of the design is the LT1681 controller chip [58], it is a dual transistor synchronous forward controller able to produce the drive pulse at the frequency of 300 kHz with an output duty factor that can vary from a few percent up to a maximum of 45%. The pulse width is controlled by a feedback circuit based on the values of the output voltage of the Brick. This input permits us to ensure continuous mode operation at the nominal voltages and currents. The signal from the LT1681 is sent to the FET Drivers. These are transistor drivers that have sufficient current and voltage drive to drive the high-side. Switching power supplies are objects able to produce a DC signals with reduced voltages with respect to the

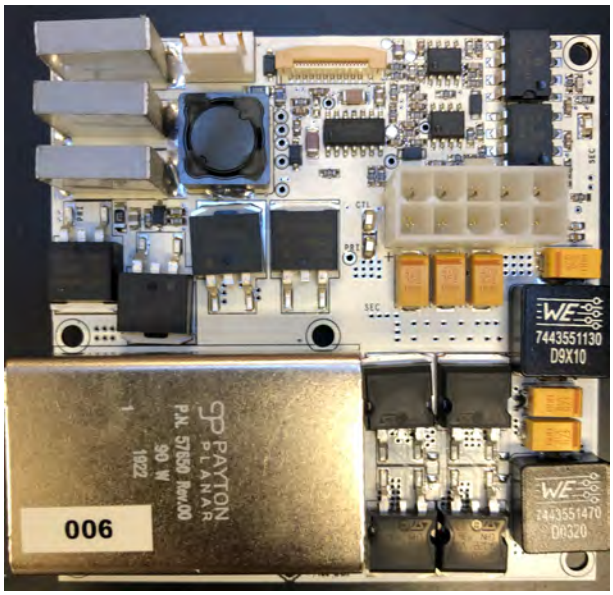

Figure 4.3: WITS LVPS Brick prototype (top side).

input signal while maintaining the power dissipation very low. Both the high-side and low-side transistors voltages turn on and conduct for the duration that the output clock is in the high state, and both are in the off state when the clock is low. When the MOSFETs conduct, current flows through the primary windings of the transformer, which transfers energy to the secondary windings. A buck converter that steps down the 200V DC to low voltages is implemented on the secondary side of the transformer and converts the signal to a constant voltage for the output. The output side also contains an additional LC stage for noise filtering. Voltage feedback, for controlling the output voltage, is provided by the optoisolators. This component processes the electrical signal converting it into digital signal, at the input stage, and transmitting it through pulsed light signal to the output where it is converted back to an electrical analog signal. The signal is transmitted maintaining the input and output electrically insulated from each other. The design also incorporates two shunt resistors for measuring the output current, the voltage for which is also fed back using an optoisolator. The value of the output voltage is controlled by a reference voltage that comes from the central controller in the LVPS box, and the ELMB. The Brick has three types of protection circuits built-in as part of the design, over voltage protection (OVP) and over current protection (OCP) are on the primary side and are configured specifically for each particular type of Brick. The third one is over temperature protection, which monitors the temperatures of the low-side transistor on the primary side. This circuit is integrated in the LT1681 design. When one protection circuit is triggered an off signal is sent to the LT1681 which stops the Brick immediately. Several monitor circuits are implemented on the Brick, these circuits send the information to the ELMB that in case of need can command a shutdown. In particular the ELMB monitors

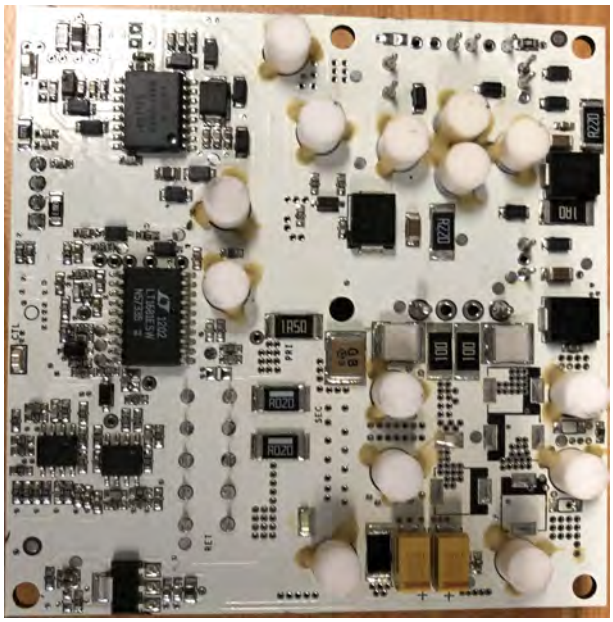

Figure 4.4: WITS LVPS Brick prototype (bottom side).

two temperatures on the primary side of the Brick both close to the input of over temperature protection of the LT1681 and the output values. The upgrade Brick will have a single Brick on/off control through a Tri-State line using the LVPS Brick. The Tri-State control lines are driven by the power supplies where the start for the Brick ranging at 15 $\pm$2 V DC and the high impedance signal enables the LM9074M regulator on the LVPS Brick(Figure 4.3). The disable state signal disables the LM9074M regulator on the LVPS Brick and thus switches off the Brick when switched to ground.

4.2.5 Improvements of latest prototype

Real-time monitoring of LVPS Brick

The Brick senses six analog signals and sends them to the ELMB motherboard, which includes input voltage and current, output voltage and current, and the temperature readings from two points on the Brick (primary and secondary side switches), measured using thermistors. Custom computer software was compiled to perform and monitor the LVPS Brick and the tests are graphically displayed and recorded onto log files [57, 59, 60]. Testing ensures that LVPS Bricks meet the criteria listed in 4.1. The feasibility of the design regarding the electrical parameters of specification was verified using a test-station [60, 61] that was assembled at the University of the Witwatersrand. Various tests determine whether the protection circuitry of the LVPS is functioning correctly. Built-in protection circuitry are assessed for over current protection (at 10.5 A) and over temperature protection (at 72 °C), in addition to the over voltage protection (at 12 V).

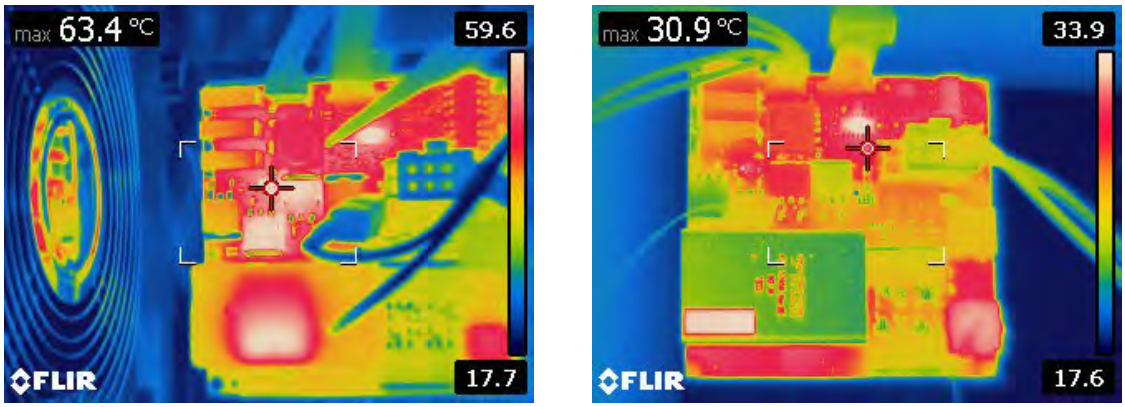

Figure 4.5: Two dimensional temperature maps of a +10 V Brick operating at 2.3 A with thermal coupling with Aluminum Oxide thermal coupling. These maps have been obtained with the application of a Bergquist gap-pad on the LT1681 [58] and FET drivers. Thermal reading of the previous 8.1.0 version of the power supply (left) and the Thermal reading of current 8.4.2 version of the power supply (right).

Thermal management

In the upgraded design the ceramic posts utilize the same Aluminumn Oxide (Al_2O_3) material (Figure 4.4) to provide thermal coupling. The ceramic posts provide sufficient heat dissipation and can be seen from the two dimensional temperature maps of a +10 V Brick operating at 2.3A which are shown in Figure 3, the old version of the power supply which had significantly lower efficiency MOSFETs (left) and new upgraded version with high efficiency MOSFETs (right). Even if the obtained improvement are clear, there are two zones, where the location of the converter LT1681 and the location of the FET driver, that still show a very high temperature during operation. For this reason, these chips at the bottom side are coupled to the plate with the application of the Bergquist gap-pad for further reduction of the temperature to the two critical components responsible for heat generation of the power supply.

Tri-State Control method testing

The legacy Bricks need separate two signals to run whereas the upgrade Bricks will utilized an individual Brick on and off control through a Tri-State control method where each Brick can be controlled, started and disabled by a Tri-State control line. The start up voltage ranges from 15 V $\pm$ 2 V DC. This signal initially powers the primary side of a Brick. The high impedance or (keep alive signal) is maintained by the Brick as it enables the LM9074M regulator. This is a logic signal. This signal ranges from 4 V - 7 V DC. The disable signal ranges from 2 V DC to 0 V DC. This signal disables the LM9074M regulator on the LVPS Brick, which will turn the Brick off. Once the Brick is turned off, the start-up pulse is required to turn the Brick back on. The line is pulled low at the Brick, so a floating condition at the Aux Board or an open circuit will disable the Brick. The Tri-State method

was simulated using virtual components on Proteus software [62] to mimic the start up circuitry of the Brick and using the voltage divider rule with the bias (Tri-State) voltage as can be seen on equation 4.1 and an example calculation on equation 4.2 as follows:

$$V_{On/Off} = (V_{supply} - V_{Tri-State}) * [R54/(R54 + R62)] + V_{Tri-State}, \tag{4.1}$$

for example if we have a $V_{Tri-State}$ = 1 V, V_{SUPPLY} = 15 V; R54 = 680 ohms; R62 = 4.3k ohms

$$V_{On/Off} = 15\ V - 1\ V)[680\ ohms/(680\ ohms + 4.3k\ ohms)] + 1\ V = 2.9116\ V \tag{4.2}$$

which would switch the Brick ON as the linear voltage regulator chip is power by 5 V and run enable is 2 V. Several simulations can be seen on Figure 4.6 and Figure 4.7 and in the Appendix. The start up voltage ranges from 15V $\pm$ 2 V DC. This signal initially powers the primary side of a Brick. The high impedance or (keep alive signal) is maintained by the Brick as it enables the LM9074M regulator. This is a logic signal. This signal ranges from 4 V - 7 V DC.The disable signal ranges from 2 V DC to 0 V DC. This signal disables the LM9074M regulator on the LVPS Brick, which will turn the Brick off. Once the Brick is turned off, the start-up pulse is required to turn the Brick back on. The line is pulled low at the Brick, so a floating condition at the Aux-Board or an open circuit will disable the Brick.

Overall performance and reliability analysis

The overall performance of the tested low voltage power supplies must meet the stringent specifications of the ATLAS Phase-II LVPS project. Testing is based on two testing stations, both followed by debug and repair sessions. The sessions address protection and monitor circuits and are separated by the Burn-In which aims at having the Bricks working under stress conditions. At the end of the checkout procedure all the Bricks must match the design parameters within the allowed ranges before checkout. Quality control testing at the University of the Witwatersrand is ongoing and test benches are operable. The LVPS prototype guarantees over 80.5% efficiency at 2.3 A nominal load, +10 V input and able to withstand harsh environments from the overall design [60].

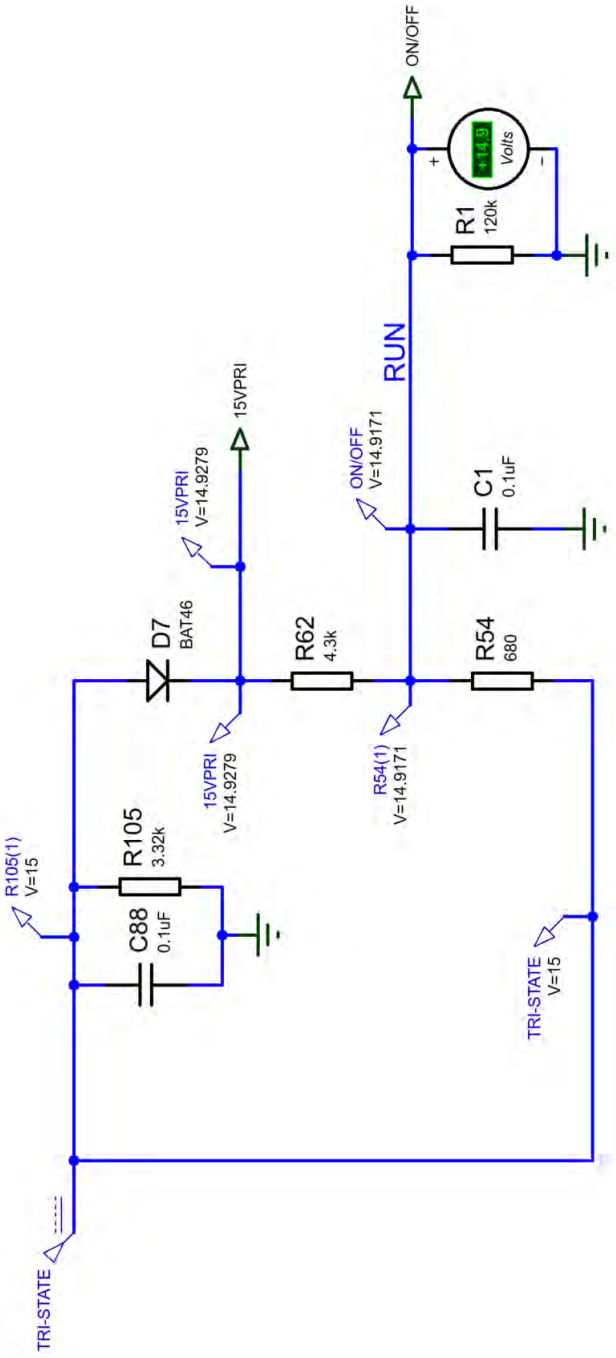

Figure 4.6: Simulation of 15 V start up pulse input and 15 VDC Tri-State.

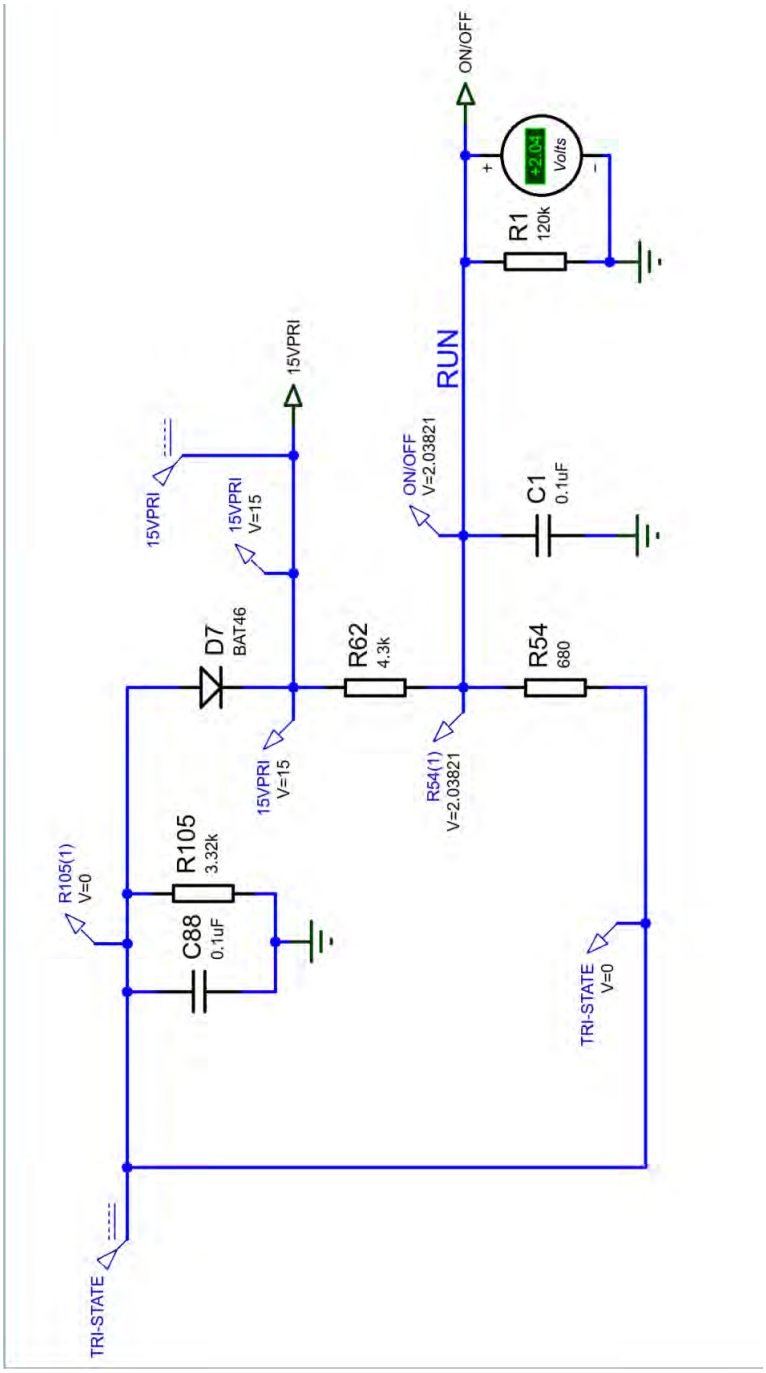

Figure 4.7: Simulation of 15 V start up pulse input and 0 VDC Tri-State.

Chapter 5

Quality assurance testing of the Low Voltage Power Supply Brick

5.1 Pre-production and production checkout

The components for the LVPS Bricks are obtained in part from the industry and the University of the Witwatersrand, where the upgrade Bricks have been re-designed and are being tested. A technical document was written to explain the techniques and requirements for the production of Bricks to the local industry. When the Bricks arrive at WITS, they come with all of the necessary components as well as a label indicating the Brick ID. To ensure the high quality of the final product transported to CERN, each Brick must be tested. The following steps make up the test procedure:

- Visual inspection;
- Initial tests (debugging, repair, repetition of initial test if required;
- Burn-in testing;
- Final test (debugging and repair , repetition of final test if necessary);
- Shipping to CERN

The initial step is visual inspection, which includes inspecting each part's soldering and the cleanliness of the Brick, as well as validating the correct installation of individual components.

During the visual inspection, a serial number and a barcode are assigned to the Brick, which will be used to identify it. The Brick has logged into the database at this stage. The initial test, which consists of a set of highly automated tests, is the next phase. The test determines the general state of the Brick (output voltages and currents, clock efficiency, Brick start-up and shutdown) as well as the proper operation of the protection and monitoring circuits. The next section contains more information about this test bench used for certification. If the Brick fails one or more tests, a technician and/or engineer will investigate the cause and correct the problem before retesting the Brick. The database is then

updated with the initial test results, repairs, and the final passing date. The Brick is now ready for Burn-In, a 6-hour test that stresses components and solder joints on the verge of failure by running at the upper limit current. Temperatures, input and output voltages, and currents are monitored and measured on each Brick during the test to ensure that it is working properly. Thermal grease is put under the posts to aid the coupling of the Bricks with a water-cooled plate during the Burn-In process, as it is done in regular working conditions. Temperatures from the Burn-In are stored in a database along with the date. The Brick is put through its last test after the Burn-In. This session is followed by debugging and repairs if necessary; nonetheless, just 3.7% of the Bricks are expected to fail the final test. After repairing only the final test is repeated. The final part of the procedure is the application of the Bergquist gap-pad [63] and the packaging for shipping. During the performance, Bricks are accompanied by a personal datasheet that contains all the information on the tests and on the details of the failures and repairs. Whenever Bricks are not under test, they are placed in electrostatic resistant bags and stored according to Brick and test phase they are undergoing [34, 59, 60].

5.2 LVPS test bench

The test bench was developed for the purpose of evaluating the functionality of the LVPS Bricks following their production [59, 60]. The test bench provides a set of independent parametric and functional tests (input current, LT1681 DC/DC converter chip functionality, and feedback loop parameters) tests to be performed by personnel and would generate reports that can be stored in a database for future analysis. The test bench consists of a test fixture providing support for both the LVPS Brick and interface card that facilitates the monitoring and control of the power supplies. The test bench is fully automated by means of a LabVIEW control program [64]. The test of one LVPS Brick requires only 4 minutes to go through the sequence of automated tests and guarantees full functional testing. The control software is read out and controlled by different commercial instruments. The central element of the system is a data acquisition (DAQ) [65] module from National Instruments which serves as the primary method for acquiring data from the Brick under test. The DAQ module communicates with the computer via a PCI-express card [66], which acts as a gateway for the PC to the Data Acquisition module. In addition to the Data Acquisition module, the test stand has several other instruments, including an electronic load meter which provides a programmable load for testing the performance of the upgraded Bricks. A programmable power supply is used for providing +5V for peripheral circuitry of the interface card, including the bias voltage for the temperature sensors as well as Tri-State voltages to start. A programmable high voltage power supply is used to provide the 200V needed to power the Brick under test. Lastly, a digital oscilloscope is used for reading out waveforms, clock and the dynamics of the output voltage. These instruments are controlled and read out using either a USB/RS232 or GPIB bus.

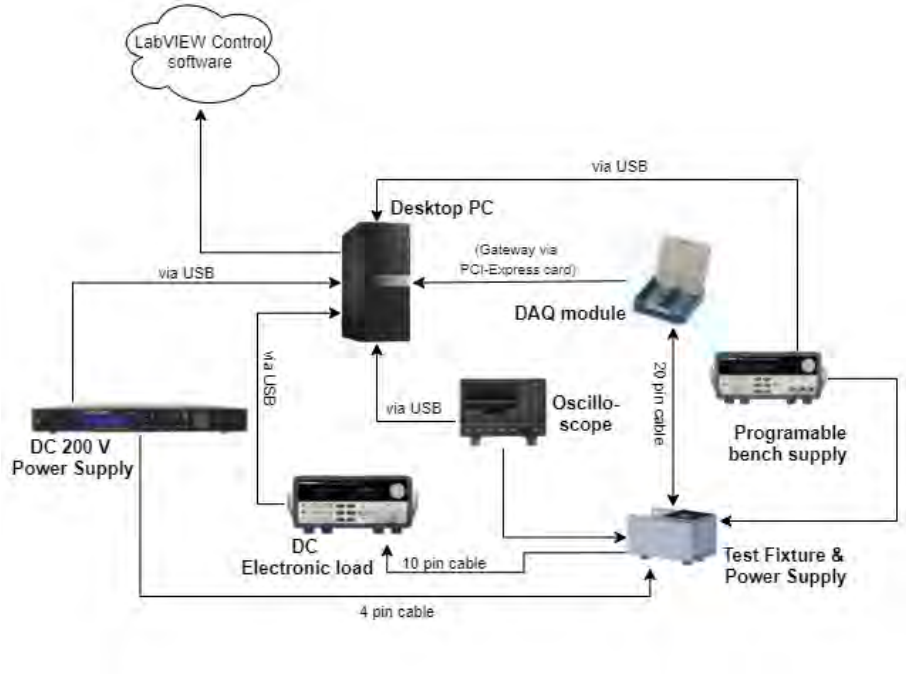

Figure 5.1: Test station block diagram.

The basic system topology is shown in Figure 5.1.

5.3 Automated testing software

A real-time program was modified to read the status and the internal test results of all the individual Bricks under test. The test program can also evaluate the data read for each test, and applies cuts to determine if the measurements meet the acceptance criteria. The program is written graphically in a National Instruments LabVIEW framework, together with drivers provided by the commercial instruments and the routines for communication with the DAQ module. The program also checks the functioning of the LVPS Bricks (current, voltages and temperature). The program evaluates the Brick's operation and checks the data collected by commercial equipment, which are used to perform the procedure. It also saves the data for each Brick test. The test bench is based on a computer controlling and reading out several commercial equipment which performs the tests. Eleven separate tests in total complete the procedure, each communicating with several instrumentation devices. The full composition of the test stand can be seen in Figure 5.2.

5.3.1 Description and functionality of tests

In the initial and final tests we check that the main functions and parameters (shown in Table 5.1) of the Bricks are correct. The required parameter range corresponds to 3σ

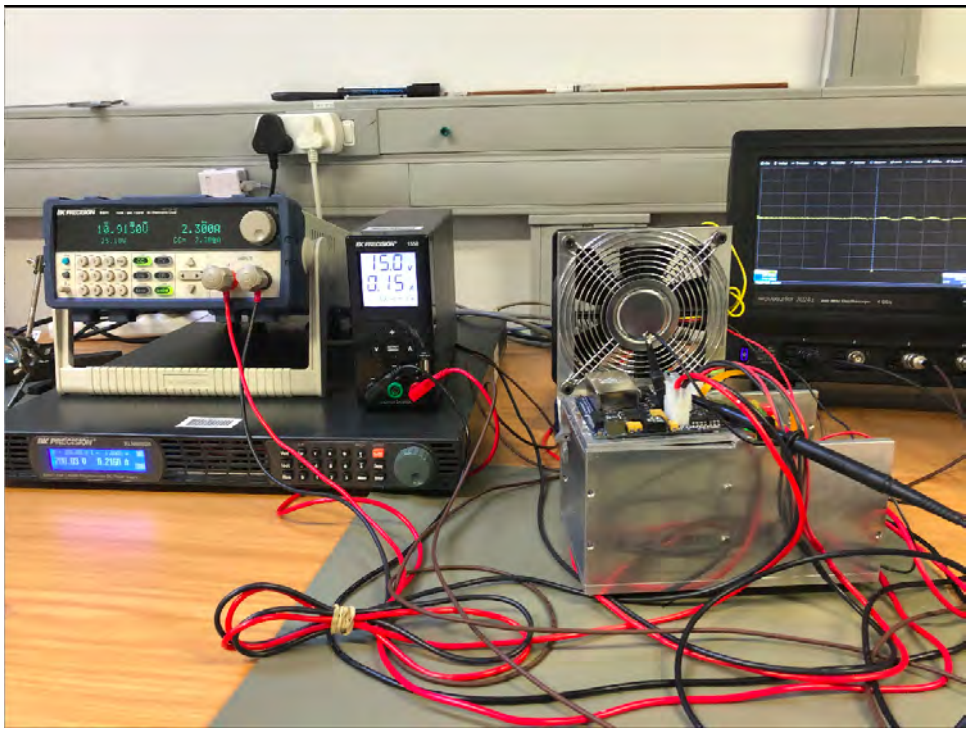

Figure 5.2: Individual Brick test stand for testing and real time monitoring of LVPS Brick behaviour.

around the nominal value for all tests except the over voltage and over current protections. For these tests the requirement is set by quality assurance procedures. In the following a brief functionality of each test is given however the goals of these tests can be summarized as follows: Ensure that the Brick responds correctly to regular start-up and shut down procedure commands and that it respects the load parameter (tests 1, 6); checks the voltages and the currents at the input and output stages, verifies the functioning of the relative monitor and ensures that the Brick responds correctly to the external reference changes (tests 2, 7, 8, 9, 10); check the output and the feedback sent to the LT1681, to ensure the stability of the output (test 5); ensure the correct behavior of the over voltage and over current protection circuits by forcing the Brick in the condition to trigger the circuits (tests 3, 4) verifying the functioning of the temperature monitors (test 11). The following are the test purposes:

1. The minimum stable load test is designed to determine the minimum load that the power supply can behaving correctly. In this condition, the output from LT1681 is read with the oscilloscope. The load is then decreased until missing clock cycles are registered, the load value is recorded. Permitted values for the test can be seen from the minimum and lower bounds listed in Table 5.1.

2. Minimum Output Voltage test measures the minimum output voltage. The lower

Parameter	Minimum	Maximum
Frequency Standard Deviation (Hz)	0	1000
Frequency Max (Hz)	290000	350000
Frequency Min (Hz)	250000	310000
Minimum Stable Load (A)	0	2.3
Minimum Output Voltage (V)	9.8	10.9
Over Voltage Protection Trip Point (V)	11.5	12
Over Current Protection Trip Point (A)	10.25	10.75
Duty Cycle Standard Deviation (%)	0	0.1
Clock Duty Cycle Average (%)	0	45
Clock Duty Cycle Standard Deviation (%)	0	0.15
Maximum Start-up Delay (s)	0.2	0.08

Table 5.1: Testing station test parameter bounds. These parameters are used to restrict the response of the output to a change in measurement when evaluating the LVPS Brick under test.

limit for each Brick is shown in Table 5.1. These values are within a few percent of the nominal output values.

3. The voltage trip point test checks the over voltage protection circuitry of the Brick. The test simulates an over voltage (for the output voltage) triggering the protection circuit that trips the Brick. The condition of over voltage is reached decreasing the external reference value. The test records the voltage when the Brick trips. The protection circuit is set to shutdown the Brick at 10-20% over the nominal operating voltage.

4. The current trip point test simulates an over current event which would cause the protection circuit to trip the Brick. The test simulates an over current event (for the output current) triggering the protection circuit that trips the Brick. The condition of over current is reached decreasing the load value. The test records the current when the Brick trips. The protection circuit is set to shutdown the Brick at 25-50% over nominal operating current.

5. The output stability test is used to check the stability of the output and the signal from the Brick. The test also measures the frequency and duty cycle of the driving pulse. The output voltage, the frequency and the duty cycle of the driving pulse are measured over several iterations. The maximum output voltage RMS is then required to be within the values listed in table 5.1 The driving pulse frequency must be within 10kHz range of the nominal frequency of 300kHz. The duty cycle for the 10V Brick generally accepted RMS value is 0.1% for all Bricks. In Table 5.1 the desired duty cycle factors for each Brick are shown.

6. The startup verification test measures the delay that the Brick takes to start-up. It

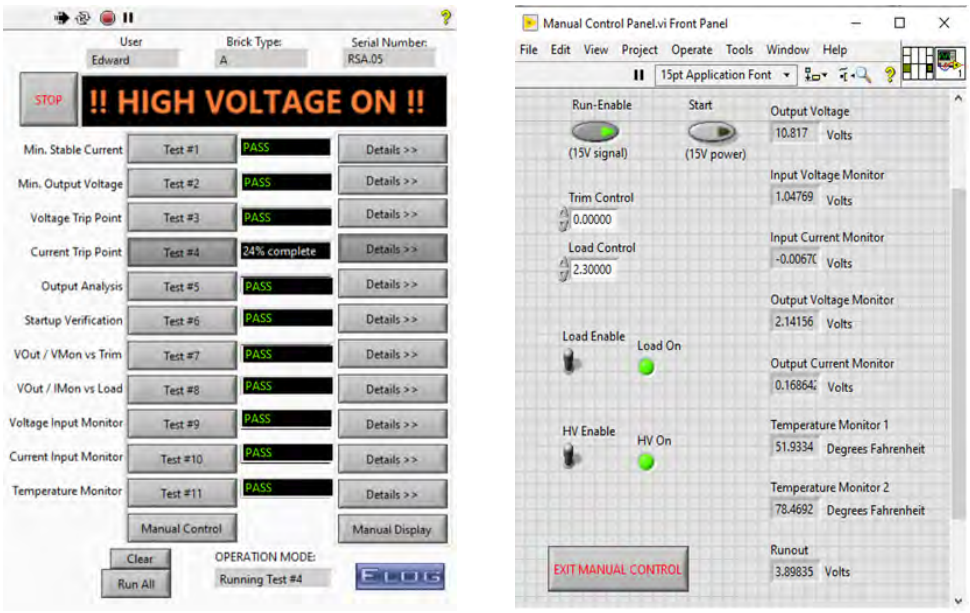

Figure 5.3: Test panel to perform various tests (left) and the manual control feature on a graphical user interface (right).

is typically measured when the voltage reaches 90%. For this measurement the oscilloscope probes are connected to the output and to the input of the Brick to register the pulse, the delay is measured when the voltage amplitude reaches 90%. Start-up delay acceptable values are shown in Table 5.1.

7. The reference voltage is also measured at regular intervals to determine the response of the output of the external reference and checks the correct functioning of the output voltage monitor. In the test, we measure the slope and offset of the output voltage (V_{out}) versus the reference, then we take the same measurements for V_{out} monitor versus offset. The output has a well defined slope in the process which allows us to check that the output monitor sees the changing in the output and to define the proportional coefficient between the monitor and V_{out}.

8. The output current versus load test checks the correct working of the monitor's circuit. The Brick is started at the minimum output voltage and the load is increased to 80% of the trip point. Output of I_{out} monitor is taken at regular intervals of the load. The test measures the slope and offset of the plot.

9. The calibration test is performed to make sure that the voltage input monitor is set to the correct value. The output voltage is set to the nominal value and the test measures the value of the input voltage monitor. The correct value is 1 V for all Bricks with a tolerance of ± 0.05 V.

10. Current Input Monitor This test checks the correct calibration of the current input monitor. V_{out} is set to the nominal value and the test measures the value of the

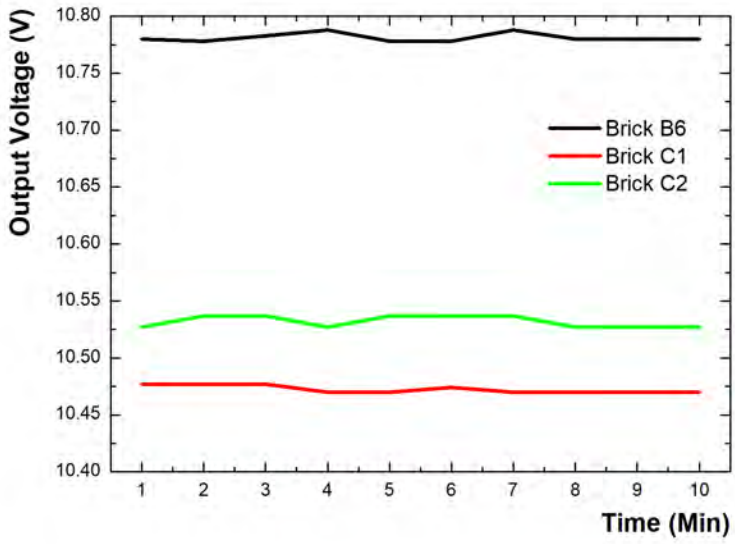

Figure 5.4: The test monitors the output voltage of the LVPS Brick. Permitted values for all the Bricks should be within the 3σ range. The test recorded for 10 minutes.

input current (I_{in}) monitor.

11. The temperature monitor test is used to check the temperature of the monitor located near the input of LT1681 temperature protection. The Brick is cooled using a fan during the test therefore the measured values do not correspond to the operation values.

The manual control feature has been included in the test bench along with an Electronic LOG book feature which is a widely used service on many CERN experiments. A LabVIEW-based program has been implemented into the test bench to automate new ELOG [67] entries containing test parameters immediately after a LVPS Brick test is completed. The Test bench logs 50 parameters of each Brick in a single ELOG entry. The ELOG client is run locally on the test bench, and pipes parameters to the ELOG daemon on the local PC. Further the copy of the results is stored in a TileCal database for future reference. The development of the database can be seen on Appendix D.

5.4 Monitoring and control results

Some notable metrics that are also measured are the clock and its jitter which are monitored to see how they affect the system's stability and to make sure that the LVPS Brick protection circuitry is operating properly. This test bench also verifies the protection circuitry of LVPS Brick, which protects it from over temperature, current and voltage. If the output voltage, current or the temperature of the Brick exceeds the allowed range it can

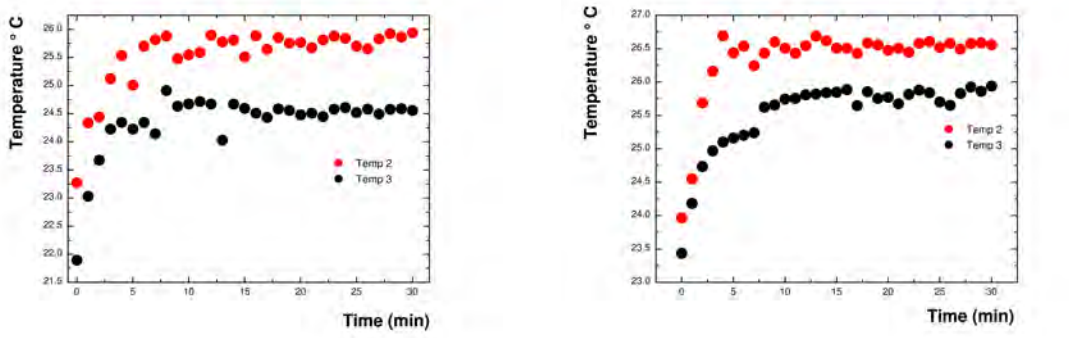

Figure 5.5: Temperature measurements taken for continuously for 30 minutes. B6 (left), C1 (right) thermistor measurements located on the LVPS prototype Bricks.

damage the Brick itself, as well as to the components it is powering. If the temperature or the output voltage of the Brick exceeds the tolerance limit it can damage the components of the system and reduce the life expectancy of the Brick. The test process is initiated by the user with the required test. After the test is completed, the program then automatically configures all the necessary parameters and displays a binary pass or fail alongside the respective test as shown in Figure 5.3. The program can also export the results as a text file or if required in a form of a graphical representation. For the completion of a test sequence, all tests need to be successfully completed without any error messages being displayed. The pass status all of its respective tests must have yielded results within the allowed parameter distribution, that is, all eleven tests within the sequence must have received a pass.

Another significant metric we are measuring is the signal feedback where the test checks the correct functioning of the monitor circuit of output voltage (see results in Figure 5.4) to be distributed at the front end electronics of the TileCal. The Brick is started at a nominal load of 2.3 A. The manual control feature is a new addition, which allows the Brick to be monitored at any period interval. Permitted values for all the Bricks should be within the 3σ range. For values outside the specified values, these are considered as a failure of a Brick. The expected voltage of the power supply should not exceed 12.5 V, which can be observed from Figure 5.4 where both the upper and lower bounds of the tested Brick are with the required specifications. The two single-ended temperature measurements (TMEAS2 and TMEAS3) for the prototype Bricks under test can be observed in Figure 5.5.

5.5 Summary of test bench results

The results of the different tests for all produced LVPS Bricks were tested in the period 2019-2021. Most common failures were on tests number 3, 5, while tests number 3 represents a special case where some constants will be verified. The Over voltage protection

tuning (test 3) involves an operational amplifier which has been updated and specification of value bounds is a subject of discussion in internal meetings. Almost all the 10 V Bricks will be tested and their respective output files (see Appendix C) will be uploaded on the CERN document repository as machine readable files, and to the ATLAS TileCal Phase-II upgrade.

Chapter 6

Software and Firmware development for a Burn-In test bench

6.1 Accelerated aging of the low voltage power supply

Burn-In testing, often known as accelerated aging, is a method of detecting premature component failure. The LVPS Brick and components will be stressed in an environment with an increased temperature during the Burn-In process [68]. This environment stresses the electronics under test, causing components that would otherwise fail prematurely to fail during the test period, before the newly manufactured electronics are deployed on the detector, where access can be limited. "Infant mortality failure" refers to a form of failure that occurs early in the life of new electronics. The failure rate distribution in Figure 6.1 depicts this period of early failure. The bathtub curve described in Figure6.1 [69] describes the expected failure rate as a function of time of any component taking into account infant mortality, constant random failures, and wear out failures. The three stages of failure that define the full life span of a population of electronics are described by the following:

- Infant Mortality: This is the period where early failures reveal themselves. This is possibly due to a lack of control in manufacturing processes. Components fail at a high rate, but this rate decreases with time.
- Stage 2, Normal Useful Life: This is the period where rate of failure is nearly constant, and due to randomly occurring faults.
- Stage 3, End of Life: Period marked by increase in failure rate due to aging of components; this period marks the end of the useful life span of a device.

The failure rate of any of these stages can be quantified in terms of the hazard function h(t) which is the number of unit failures per unit of time.

$$h(t) = \frac{f(t)}{R(t)} \tag{6.1}$$

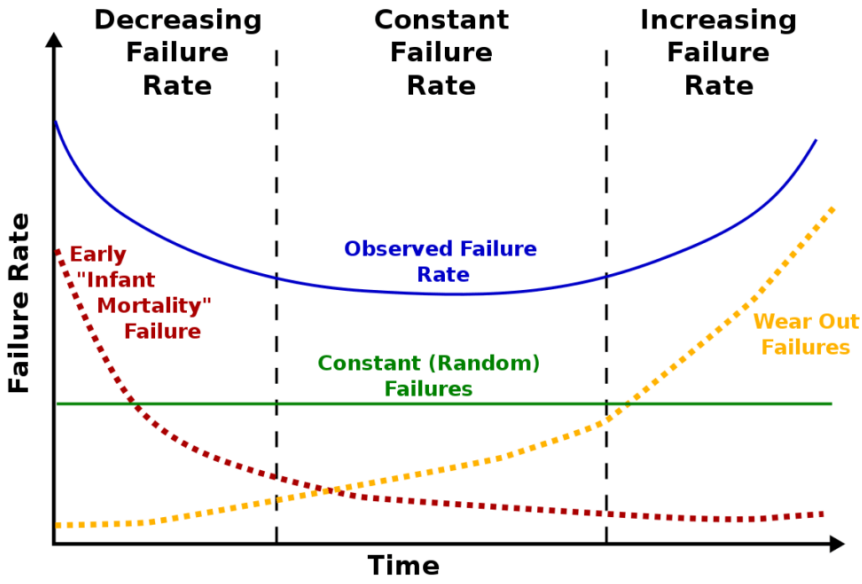

Figure 6.1: Bath-tub curve [69, 70].

$f(t)$ is the time to (first) failure distribution (failure density function) and $R(t)$ is the probability of no failure before time t. $R(t)$ can be related to the failure distribution F(t) as

$$R(t) = 1F(t) \tag{6.2}$$

The Hazard function f(t) depends on the existence of the a failure distribution F(t) describing the probability of failure where T is time at which failure occurs.

6.2 Burn-In test bench development at WITS

6.2.1 Burn-In test bench

The Burn-In station's electronics is comprised of a desktop PC with software that operates eleven compartmentalized micro-processors within the Burn-In station. The Burn-In station is controlled from a central PC, and data is saved locally. The LabVIEW environment was used to construct the main program that runs on the PC. The LabVIEW program had previously existed, but it had to be modified and updated to work with the new Burn-In station. Although portions of old code were used for inspiration, the software used in the microprocessors local to the Burn-In was specifically designed. An external coolant refrigeration unit was employed in this design, and the entire equipment and electronics required to operate the Burn-In station is a PC, and a high voltage power source located outside of the Burn-In station. This hardware interconnection is depicted in Figure 6.2. The high voltage power supply (PVS60085MR) normally supplies 1 kW of power at 200 V while the Burn-In station is operating with 8 Bricks. The programmable

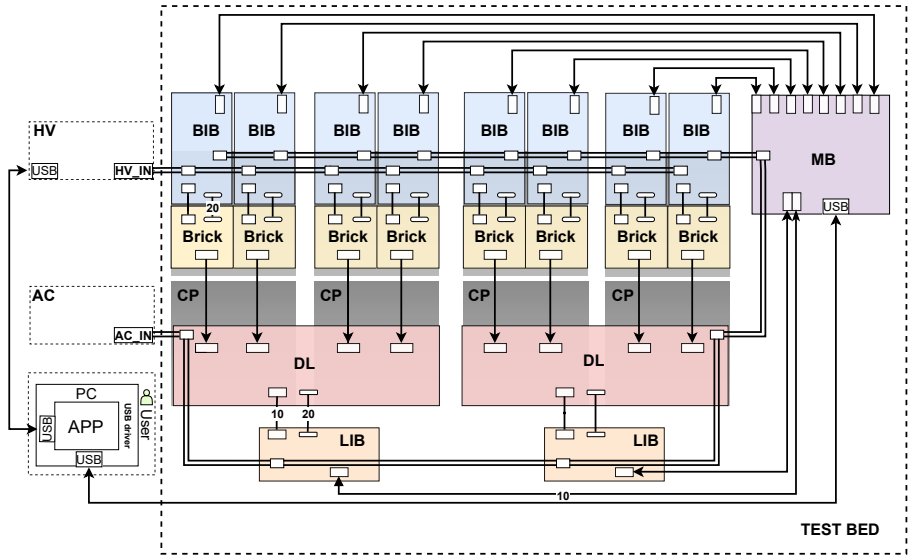

Figure 6.2: Burn in hardware block diagram [71].

power supply is controlled by the PC LabVIEW software via a VISA [68] communication link over Ethernet.

6.3 Software development for Burn-In bench Electronics

A single serial communication via UART [70] over USB link is sent to the LabVIEW software to all eleven micro-processors on each Brick interface card in the Burn-In station. UART communication is suited for communications between embedded systems and PC-based microprocessors [70]. To enable UART over USB, an FTDI IC [72] is used. The eleven microprocessors internal to the Burn-In station perform specific function tasks. Within the Burn-In station, there are 8 "Brick Interface" PCBs (one for each Brick), two "Load Interface" PCBs, and one "Supervisor or MainBoard" PCB. Only the Main Board physically communicates with the PC, and communicates with the other interface boards. Its main job is to multiplex data between the PC and the other 10 interface boards.

This way, the LabVIEW software on the PC communicates with only one micro-processor at a time. The full set up of the test bed can be seen in Figure 6.3 where the black-colored paths are UART buses. Note that these buses do not represent traditional UART over a RS232 bus (+/-15 V), but over a USB bus from the PC to the Main Board, and then from the main board to the various interface boards over TTL logic. Each interface board for the Brick and load contains a 16 bit PIC16F883 micro-controller. All the other colored paths carry power. The HV path carries 200 V to each Brick, a path carries 12 V to power each interface PCB, and the 12V output from each individual Brick to the electronic load.

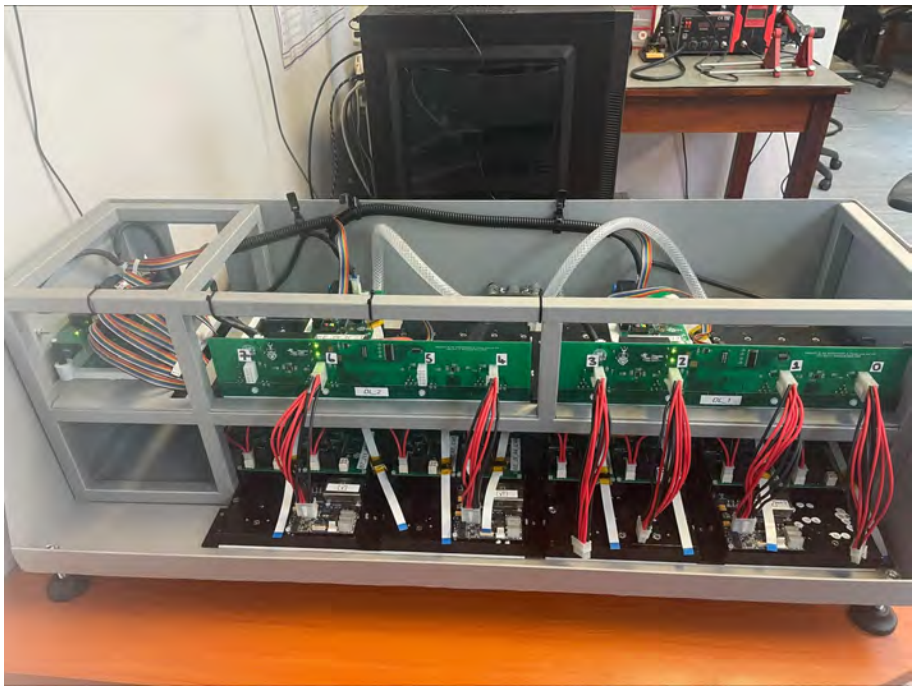

Figure 6.3: Burn-In Test bed.

6.3.1 Mainboard

This PCB board contains a PIC16F883 [73] micro-controller that allows for direct communication between each micro-proccesor and the PC through UART. It acts as a serial data multiplexor between the PC and the Brick Interface and Load Interface boards that are selected (MUX 1 of 11, addresses 0 - 10). The communication is established utilizing an FTDI IC and a serial link (RS232) over a USB virtual COM port. Multiplexing is accomplished in LabVIEW on the PC by asserting the RTS (Request to Send) flag on the UART level and transmitting the desired address. Following this address initialization, all bytes transmitted from the PC are delivered directly to the corresponding read out board, with no work or interference from the main board.

6.3.2 Brick Interface Board

The Brick Interface board's primary role is to digitize and transmit data to the PC via a 20-pin ribbon cable's through the various analog inputs. A Linear Technology (LTC2449) 16-channel ADC digitizes all analog input signals from a Brick. All of the Brick behavioral characteristics are measured, including V_{in}, I_{in}, V_{out}, I_{out}, and two Brick temperatures. To control and monitor each Brick, each has its own identical and equivalent interface board. The interface board additionally provides a Voltage startup of +15 V and +5 V for powering the Brick's thermistors.

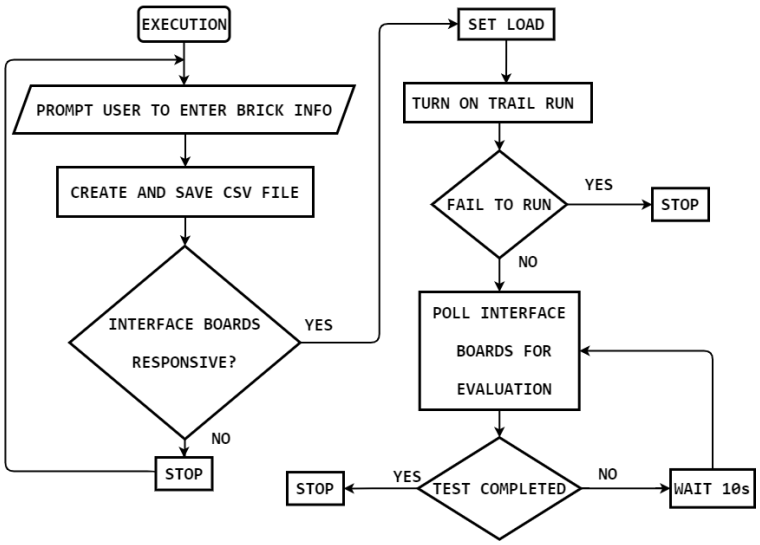

Figure 6.4: Simplified LabVIEW control program execution diagram.

6.3.3 Dummy Load board

Two Dummy Load boards are included in a Burn-In test-bed. Each PCB has four programmable current loads for Bricks (currents ranging from 0.5 to 20 A. The Load Readout Board controls each Dummy Load. Each Dummy Load is controlled by Load readout board. A Voltage on the load (V_{load}) and the sink programmed current (I_{load}) are measured.

6.3.4 Dummy Load Interface board

This PCB board is almost identical to the Brick Interface board. The program and commands for the Peripheral Interface Controller (PIC) are also the same. The purpose of the Load Interface Board is to read, control, and alter the parameters of a four-channel electronic Dummy Load board, as well as to read V_{load}, I_{load} measurements. The load interface board contains the same LTC2449 ADC which samples the voltage and current of the Brick's output measured at the electronic load. The second task of the load interface is to shift bits into the DAC registers contained on the electronic load to command the load current.

6.3.5 Embedded Firmware

The firmware of all the interface boards was written in embedded-C [74]. Both the Brick interface board and the load interface board used a state machine. Representative diagrams for each the boards are displayed in Figure 6.4. The PIC16F883 micro-controller unit (MCU) is critical because it receives signals from the board-mounted Analog Digital Converter (ADC) chip and delivers them to the main board. Digital communication for the Main boards and, by extension, the LabVIEW control software was also provided by

Parameter	Burn-In	Nominal range	Trip Point
Operating Temperature	60°C	35°C	70°C
Applied Load	5 A	2.3 A	6.5 A
Run-time	6 hours	-	-

Table 6.1: Basic conditions for Burn-In procedure.

the MCU. This communication allows the Brick interface boards' aforementioned functionality to be controlled. It achieves it by employing its ADC chip to understand data from its input/output (I/O) peripherals. The LabVIEW control program uses the Brick interface boards to control and collect data from a Brick during its automated procedure. The micro-controller stores the temporary data it receives in its data memory, which the processor accesses it using instructions from its program memory to understand and apply the incoming data. It then communicates with its I/O peripherals and takes the appropriate action. Multiple software programs, notably MPLAB X [73] and Custom Computer Services (CCS) software compiler [75] are required to program an MCU. A commercial compiler was chosen as the legacy code was compiled in CCS. An Integrated Development Environment (IDE) is used for writing and configuring the code. It works in conjunction with the CCS software compiler, which builds and compiles the code into a Hexadecimal (HEX) source file. The HEX file contains settings, configuration information and register data. The MCU only recognizes the hex file as machine code, which it uses to send and receive commands. The MPLAB X Integrated Programming Environment and PICKIT 4, allows for debugging and programming of the Microchip PIC [73]. The Proteus framework [62], is used for design, simulation and debugging of a firmware circuit. We used this framework to convert a schematic of the BI board to functional diagram whereby a simulation was carried out to debug the circuits connections. This procedure is critical since it aids in the resolution of difficulties that may develop on the Printed Circuit Board (PCB) prior to its populating. Because the PIC is the major component on the PCB, the simulation is also utilized to check signal flow and operation.

6.4 Burn-In test procedure

During the Burn-In procedure, the Bricks are exposed to higher operating conditions, which stimulate failure mechanisms within the Bricks. These requirements must be met within the constraints imposed by the Brick's design and operation. There are two reasons for this. The first is concerned with effective Burn-In, and the second with the procedure's implementation. The failure modes that are simulated must be failure modes that can occur during TileCal operation, such as an increase in operating temperature. If the OCP or OTP trip parameters are met during Burn-In, a Brick will initiate a trip. Phase-II Brick Burn-In procedure thermal profile is illustrated in Figure 6.5. The temperature value originates from a thermistor located in between the primary side MOSFETs. This

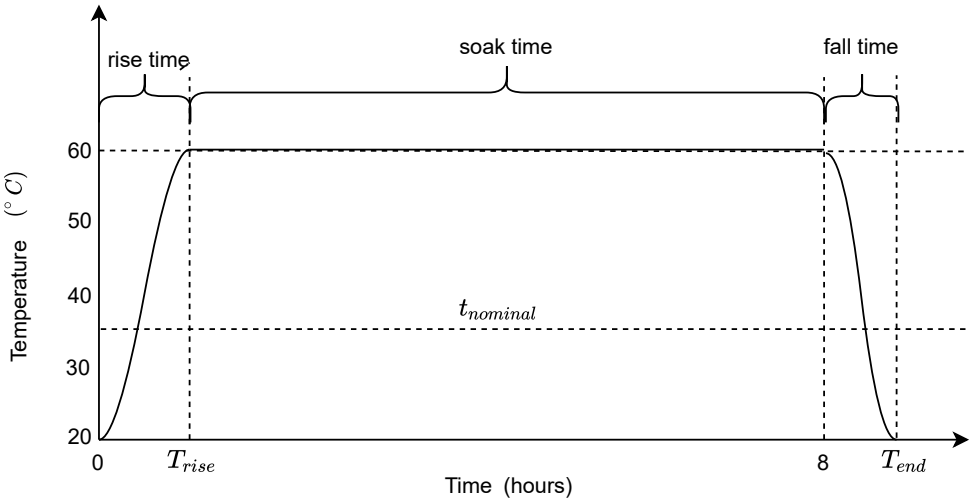

Figure 6.5: Burn-In procedure [71].

thermistor, which records one of two on Brick temperatures, was selected as it is utilized in the Brick OTP circuitry in which it measures the highest on-Brick temperatures originating from the MOSFET switching losses. The thermal profile can be sub-divided into three distinct regions. These are known as the rise, soak and fall regions. At the onset of the Burn-In procedure the Bricks are switched on and put under a 5 A load. The Bricks and the cooling system are thermal equilibrium at 20 °C at this point. This lower bound was selected due to it being the average on-detector temperature of the Bricks when they are are off. The temperature steadily climbs via the action of the cooling system increasing the temperature of the heat-sinks. This process is assisted by the Bricks self-heating due to inherent power conversion inefficiency. The characteristic curve is a result of the heat capacity of the system, conductive as well as radiative losses. The soak region begins after time T_{rise} and continues for a total time period known as the soak time at the Burn-In temperature of 60 °C. The Burn-In procedure run-time is taken as the sum of the rise and soak time. This as the Brick must remain under load during the entirety of Burn-In. At the eight hour mark the Burn-In procedure is terminated with the Bricks being switched off and brought down to their starting temperature. The time that it takes for the Bricks to be brought down to their starting temperature is known as the fall time.

6.5 Preliminary Burn-In results

During the production testing cycle of LVPS, each Brick will be checked into a Burn-In station which performs the accelerated aging. Here, a LVPS Brick is subjected to a stressed environment where the load and temperature are both elevated. In this environment the expected operational life of the Brick is slightly reduced, in order to get the run duration through the infant mortality state in a more timely manner. It is ideal to operate the test

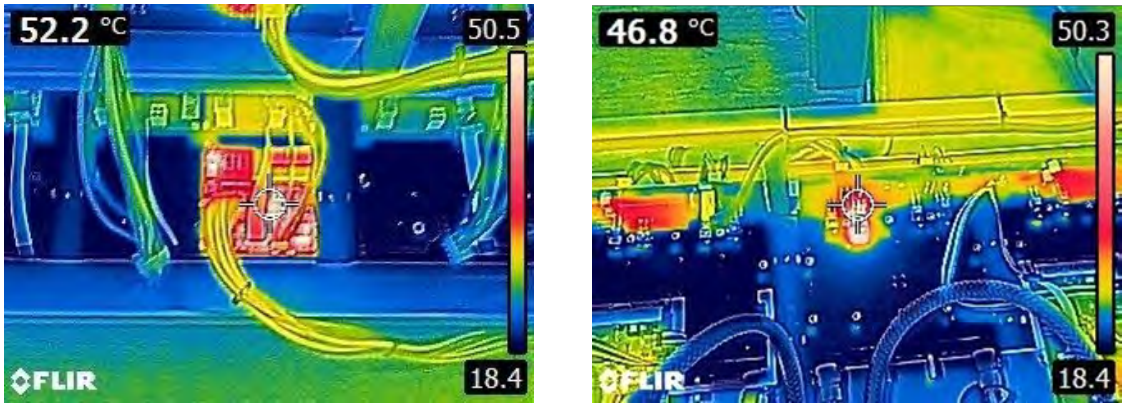

Figure 6.6: Thermal images for the LVPS Brick (left) and Dummy Load Board (right) undergoing Burn-In testing.

at 60 °C, and slightly below the lowest maximum temperature of any device on the Brick, which is 72 °C. The following parameters have been selected for the burn in procedure. A preliminary Burn-In was done on an individual Brick as part of the development of the test station at Wits University.

6.6 Burn-In test bench Summary

As of the time of writing the thesis, the large scale manufacturing of over 1000 LVPS Bricks for the ATLAS Tile Calorimeter will occur in third quarter of 2022. Testing mechanisms are in place necessary for quality assurance testing to ensure that the design, construction, and production techniques of the Bricks are reliable before they are inserted into ATLAS. The Burn-In is currently being finalized with some calibration of , with the integration of the LabVIEW control software and hardware. An extensive study will be conducted once more Bricks are available.

Chapter 7

Radiation tests performed on the Low Voltage Power Supply Brick

7.1 Radiation interaction with matter

Ionizing radiation can have an impact on semiconductor devices. The characteristics of the interaction between a semiconductor and high-energy radiation are determined by a variety of properties of both the incident radiation and the semiconductor material. Ionization effects from incoming radiation interacting with shell electrons, displacement of atoms in the target material from their initial lattice position, and nuclear reactions from incident hadrons interacting with the target nucleus are the three main categories of radiation effects on semiconductor devices. These three phenomena can happen at the same time and are sometimes triggered by a single impact particle. Ionization is very common, resulting in free electrons that can generate electron-hole pairs if they have enough energy. The energy required to form an electron-hole pair and the ionization capability of unit volume for the particular material or generation rate determine the production of electron-hole pairs [76].

7.1.1 Interactions of photons with matter

Photons are electrically neutral particles with zero rest mass [77, 78, 79]. Depending on the energy of the photon and the Z of the target atom, one of three possible routes dominates the interaction of a photon with an atom (Figure 7.1). The total cross-section of an interaction of a photon with an atom is equal to the sum of all three partial cross-sections of the following processes:

1. The photoelectric effect occurs when a photon is absorbed by one of the atomic electrons, resulting in the ionization of the target atom when the excited electron is released. The difference between the energy of the incident photon and the binding energy of the electron is the energy of the released electron or photo-electron. The atom nucleus absorbs the majority of the recoil momentum during the operation. If the incident photon's kinetic energy is high enough to extract a K-shell electron,

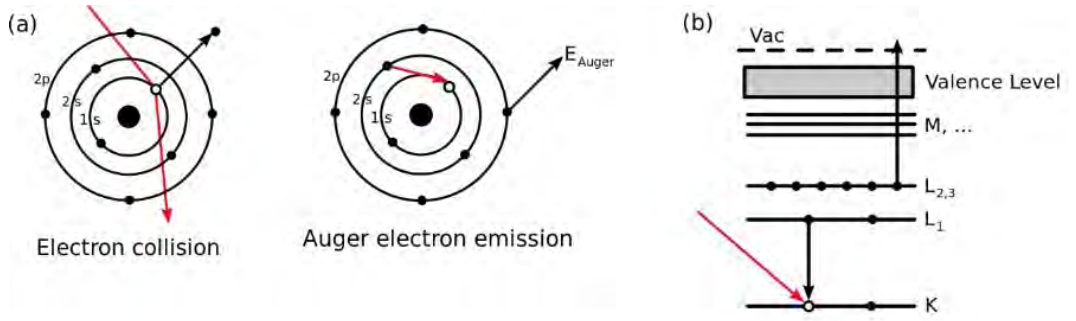

Figure 7.1: The Auger process from two perspectives. (a) depicts the Auger de-excitation process in two steps. In the 1s level, an incident photon (or electron) creates a core hole. The transition energy is transferred to a 2p electron that is emitted when an electron from the 2s level fills in the 1s hole. As a result, there are two holes in the final atomic state, one in the 2s orbital and the other in the 2p orbital. (b) uses X-ray notation to depict the same process, K L1, L2, L3 [79].

an electron from the L-shell will inhabit the newly accessible lower energy state, a process that ends with the L-shell emitting either a low-energy Auger electron or a characteristic X-ray. An incident electron can also occur in the Auger electron emission process, as shown in Figure 7.1, can also occur by means of an incident electron. A secondary ionization can occur along the path of a photo-electron, resulting in the formation of more e-h pairs in a semiconductor material.

2. The incident photon's energy is substantially higher than the binding energy of the K-shell atomic electrons during Compton scattering. An atomic electron is released as an energetic Compton electron when it receives a fraction of the energy of the incident photon. The energy transferred to the rebound electron can be a significant fraction of the initial energy of the photon. The incident photon loses energy as a result of the inelastic collision, resulting in a wavelength shift known as the Compton shift. Compton scattering takes precedence over the photoelectric process as the energy of the input photon is emitted. The charged particle interaction phenomenon will be aided by the Compton electrons created.

3. Pair production is a natural phenomena that occurs when energy is converted to matter. A photon striking a high Z nucleus can be entirely absorbed and its energy turned into a positron-electron pair by the pair production process, which has a minimum energy threshold of 1.02 MeV (2 x 0.511 MeV). The photoelectric effect prevails for Silicon (Z=14) up to energies of around 50 KeV, while pair formation dominates from energies of around 20 MeV, as seen in Figure 7.2. The vast intermediate energy range between 50 keV and 20 MeV is dominated by Compton scattering.

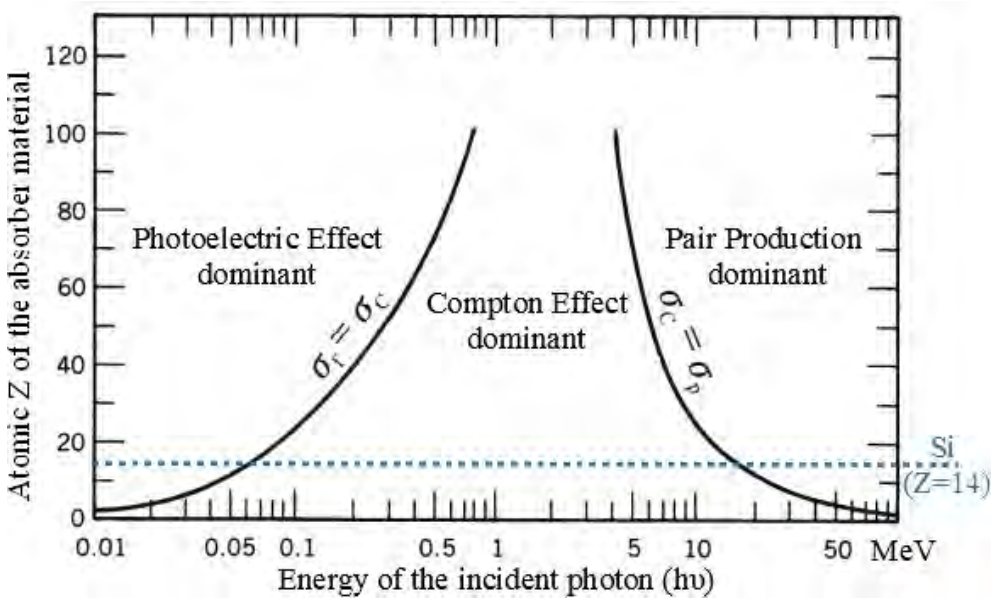

Figure 7.2: The relative contribution of various processes of photonic radiation interaction with matter [78].

7.1.2 Interactions of charged particles with matter

The penetrating particles lose energy in all interactions between charged particles and matter. The main interaction mechanism is based on the Coulomb interaction, which can result in either elastic Rutherford scattering of the charged particle with the target atom's nucleus or inelastic scattering of the charged particle with the atom's orbital electrons, causing both excitation of atomic electrons and atomic ionization. In addition, the following less common processes can occur: Cherenkov radiation, which occurs when a particle moves faster than light non the same medium, and transition radiation, which occurs when the medium is in-homogeneous [78]. The mass difference between heavy and light charged particles, the interaction mechanisms change. The relative contribution of these processes to total energy loss is determined by the incoming particle's kinetic energy and the target material's characteristics. The energy of incident particles delivered to the material is expressed by the Linear Energy Transfer (LET), which is defined as the differential energy loss divided by the differential route length. The dominant process in the interaction of matter with light charged particles for lower energies is ionization. However, other channels of interaction can also take place. These include Moeller interaction in the presence of elastic scattering of an electron from another electron, and Bhabha scattering when a scattering of an electron from a positron occurs and electron-positron annihilation results in two photons. The emission of Bremsstrahlung radiation is the primary interaction mechanism at higher energy. One or more Rutherford scatterings can occur, resulting in large variations in the particle's path. For a wide energy range of incoming electrons or positrons traveling through lead [78], Figure 7.3 displays the contributions of several processes to the fractional energy loss per radiation length.

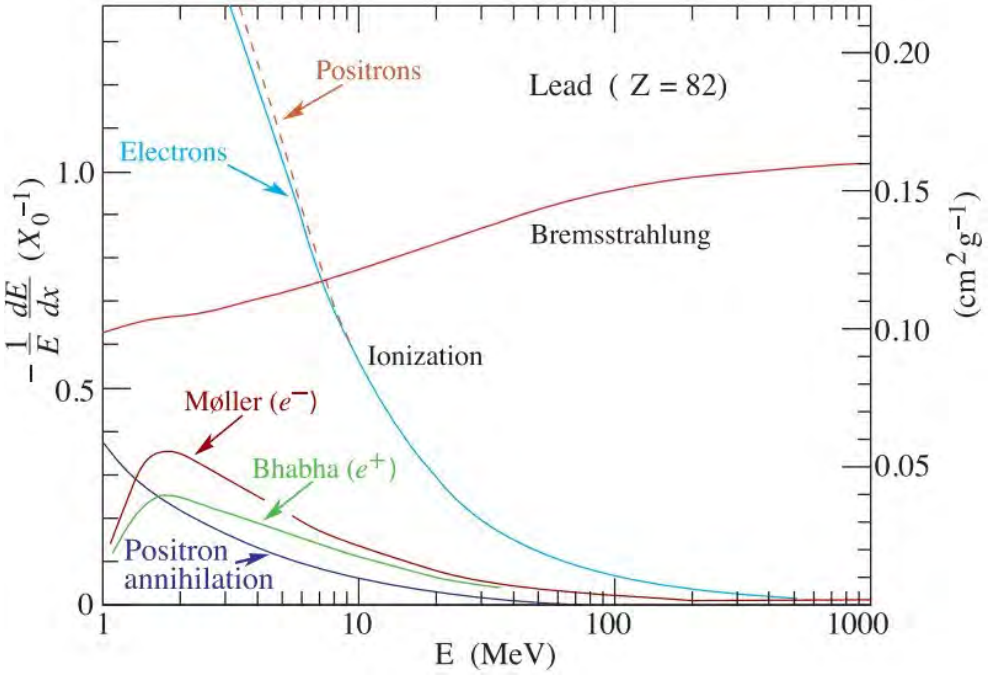

Figure 7.3: Fractional energy loss per radiation length in lead as a function of electron or positron energy [16].

7.1.3 Interactions of neutrons with matter

Neutrons have zero charge and interact with matter through nuclear processes such as elastic scattering, inelastic scattering, spallation, fission, radiative capture, and transmutation. The neutron transmits some of its energy to the nucleus of an atom of the target material through elastic collisions. After catching a portion of the energy from the incident neutron, the nucleus of the target atom is left energized in the process of inelastic scattering. When the excited state of the nucleus transitions to a stable state by producing a gamma particle as a result of the nucleus de-excitation [80], inelastic scattering can lead to radiative capture. Both elastic and inelastic neutron scattering processes can shift the target atom from its lattice position if the transmitted energy is substantial. A high-energy neutron can trigger a spallation reaction, in which the nucleus is split into many fragments. Fission occurs when a heavy nucleus captures a sluggish neutron, becomes excited, and splits into fragments as a result. And the transmutation process entails a nuclear reaction in which the incident neutron is captured by the target nucleus and another particle, such as a proton or an alpha particle, is emitted as a result. The material atom transmutes, or changes atomic number, as a result of this nuclear reaction. TIonization causes the recoiling atom from any nuclear event to lose energy and may displace other lattice atoms in the process. Scattering processes and nuclear reactions favor generation of displaced atoms and ionization for silicon atoms interacting with fast neutrons (EN > 1 MeV), causing changes in the electronic behavior of silicon based semiconductor devices. The capture effect dominates the interaction with slow neutrons. The two most popular

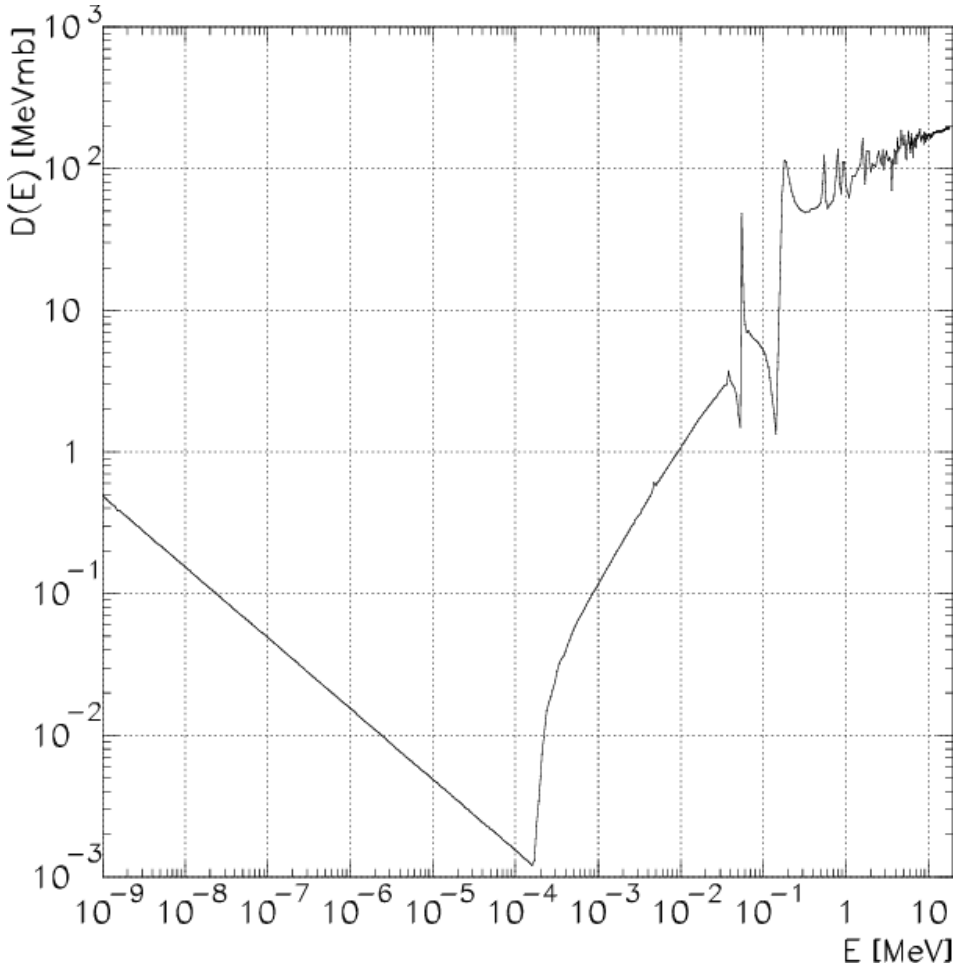

Figure 7.4: Characteristic neutron damage function for Silicon [80].

techniques of defining the neutron damage function are shown in equations 7.1 and 7.2.

$$DN = \sigma(EN) \cdot v(EN) \tag{7.1}$$

$$DN = EN \cdot \sigma(EN) \tag{7.2}$$

where: EN is the Energy of the incident neutron, σ(EN) is the interaction cross section of a neutron of energy EN with a lattice atom, and v (EN) is the average number of displaced atoms after the primary knock-out interaction with a neutron of energy EN. The neutron damage functions are characteristic of the properties of both the lattice and its atoms. Both neutron damage functions for Silicon are shown in Figure 7.4.

When neutral hadrons interact with matter, displacement processes generally take precedence over ionization processes. In contrast, ionization processes dominate interactions with charged hadrons like protons, with only a small fraction generating displacement damage.

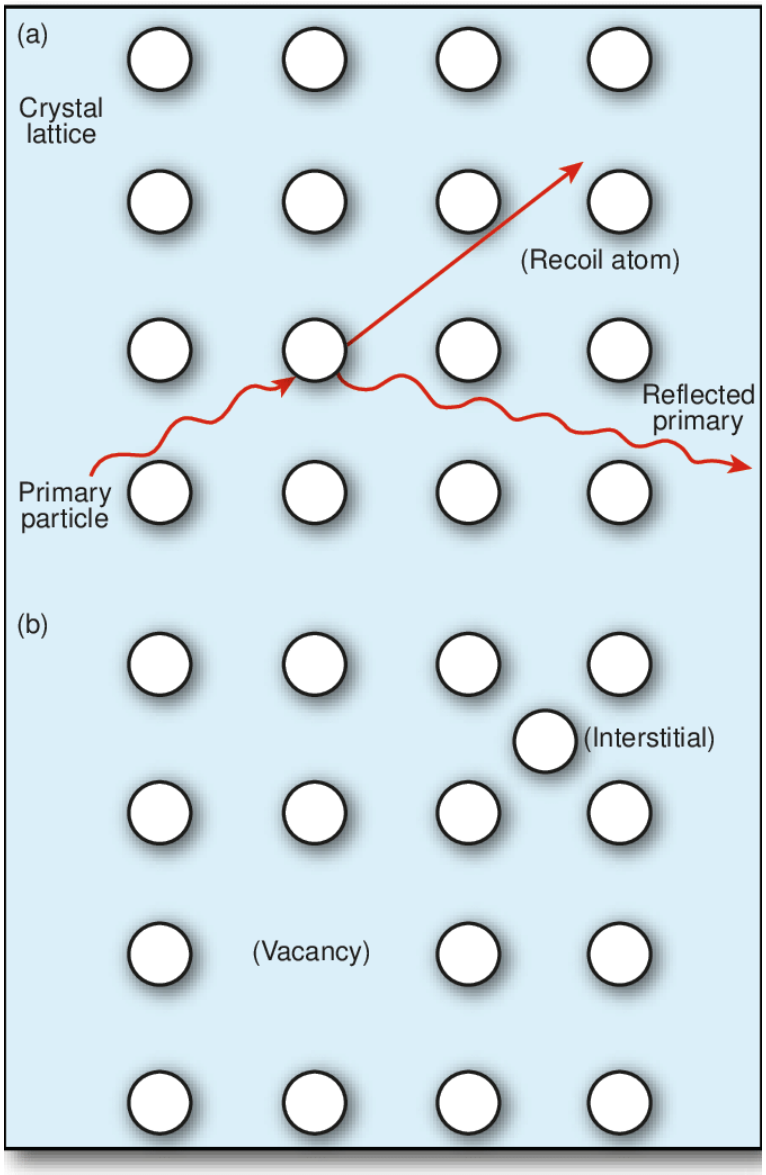

Figure 7.5: Characteristic neutron damage functions for Silicon [81, 82].

7.2 Radiation effects on electronics and semiconductor devices

Semiconductor devices can be impacted in a variety of ways, depending on the type of radiation. The different effects for understanding how radiation causes changes in the electronic behavior of semiconductor devices can be divided into three categories:

1. Total Ionizing Dose (TID) effects: When a device is exposed to a low ionizing radiation dose over a lengthy period of time and creates trapped charges and interface states are created in the gate oxides and isolation oxides. The trapped charges accumulate over time, causing quasi-permanent device changes that eventually lead to functional failures. Various effects can be found in various types of electronic components, including: Threshold voltages in Field Effect Transistors are shifted due to

holes trapped in the gate oxide layer. Gain is reduced in operational amplifiers, but bias currents, offset voltages, and currents increase.

2. Single Event Effects: When ionization occurs above a certain LET (also known as the LET threshold) in sensitive parts of an exposed electronic device, the deposited charge might disrupt the device's operation or produce transient current pathways. The critical charge required to form a SEE is highly dependent on the size of the device feature (See Figure 7.5). There are two types of SEEs: non-destructive and destructive: Non-destructive, or soft, SEEs can be recovered by a system reset, reprogramming/re-configuring the device or reprocessing of affected data. Non destructive SEEs include the following types: Single Event Upsets (SEU) occur when the logic state of an electronic element changes because of charge accumulation during the ionization processes. When the logic state of an electronic element changes due to charge accumulation during the ionization processes, Single Event Upsets (SEU) occur. Flipped bits or logic state changes are most common in digital devices including memory, CPUs, and FPGAs. Devices using MOS or bipolar technology are both susceptible to SEUs. When the collected charge is spread throughout different circuit elements, multiple bit upsets can occur, resulting in logic state changes in many cells of the circuit. When an ionizing particle causes voltage pulses that propagate through the circuit, Single Event Transients (SET) occur. A SET can create analogue output signal distortion that does not always result in a flipped bit unless it is passed through a digital circuit, resulting in an incorrect bit value being latched in a sequential logic unit. SETs are more difficult to record and correct than SEUs due to their spontaneous nature. The manufacturing method, current pulse amplitude, and operation frequency all affect a device's sensitivity to SETs. Because of their smaller feature sizes and wider frequency ranges, current devices are more susceptible to SET.

   When a device fails, destructive or hard SEEs occur, resulting in lasting device or system damage. The following are the several types of hard SEEs: When ionized particles produce transient currents at the interface between two complementary MOS transistors in CMOS and BiCMOS devices, Single Event Latch Up (SEL) occurs. The transistor pair can be thought of as a P-N-P arrangement that works similarly to a Silicon Controller Rectifier (SCR) or a thyristor. Single Event Burnout (SEB) is a problem that mostly affects high-power MOS transistors like DMOS and VDMOS. In the presence of a high drain source voltage, an ionizing particle travelling through a volume of parasitic bipolar transistor can generate an overly large localized current. When voltage is provided to the base-emitter junction, avalanche multiplication of the current in the BJT (Bipolar Junction Transistor) collector allows the transistor to be switched on. The BJT may overheat, causing the device to burn out, if the localized power density is high enough. SEBs are always harmful,

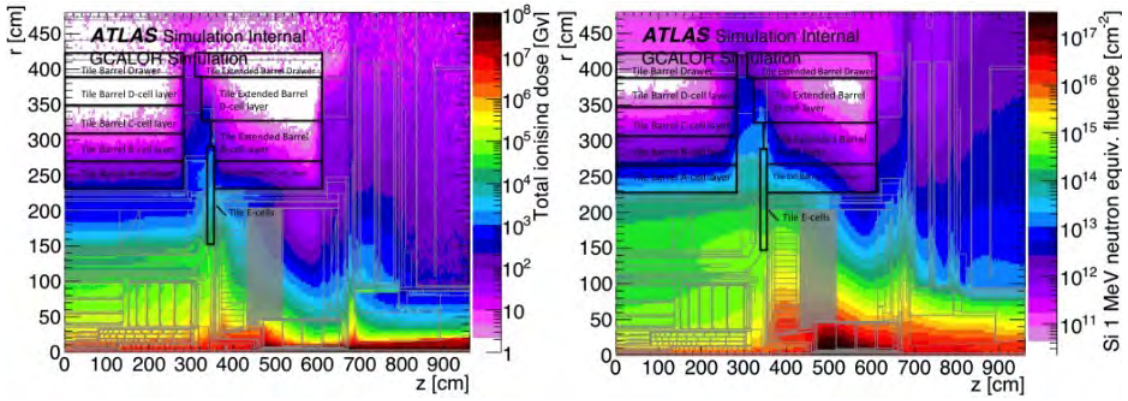

Figure 7.6: On the left: Total ionizing dosage in Gy/4000 fb^{-1} in the tracking and calorimeter regions of the Phase-II ATLAS detector. On the right: Displacement damage in silicon, expressed as the corresponding fluence of 1 MeV neutrons with an integrated luminosity of 4000 fb^{-1}. For both images the minimum-bias pp events are simulated with Pythia 8 at 14 TeV centre of mass energy assuming an inelastic cross section of 80 mb. The GEANT3/GCALOR code is used to model particle tracking and interactions with material using the latest geometry description of the Phase-II ATLAS detector. In azimuth, the geometry model is symmetric, with z = 0 [34].

leading the gadget to fail permanently.

3. Non-Ionizing Energy Loss (NIEL) effects lose the majority of the kinetic energy of an incident proton; however, a minor part of the energy known as Non-Ionizing Energy Loss (NIEL) can contribute to lattice displacement effects. Incident protons and neutrons, as well as electrons with energies exceeding 150 keV, can produce displacement damage, as can gammas indirectly through photo-nuclear interactions with protons and neutrons [81, 82]. The minimal energy necessary to permanently displace an atom from its lattice location to a defect position is called the displacement energy (E_d) On average, E_d = 25 eV for many materials [83, 84].

   If the recoil atoms' acquired kinetic energy is greater than twice the displacement energy of other atoms (Trecoil–atom > 2 x E_d), they can cause displacement [81, 82, 83]. As shown in Figure 7.5 a classic collision between two spherical balls can be used to visualize displacement events. Different types of simple displacement flaws are presented in the following:

   - (a) Vacancy: the lattice position left unoccupied by a displaced atom.
   - (b) Divacancy: two adjacent vacancies.
   - (c) Interstitial: a displaced atom occupies a non-lattice position.
   - (d) Di-interstitial: two adjacent interstitials.

Electronics	Z-High	R-High	R-Low	TID	NIEL	SEE
	cm	cm	cm	Rad	n/cm^2	p/cm^2
High-Voltage	275	400	400	1000	$1.32x10^{12}$	$2.31x10^{11}$
Mainboard	275	410	410	1000	$1.03x10^{12}$	$2.46x10^{11}$
FENICS	280	400	410	1000	$1.03x10^{12}$	$2.46x10^{11}$
Daughter Board	240	400	400	200	$2.44x10^{11}$	$1.50x10^{10}$
LVPS-Barrel	300	390	400	2000	$1.77x10^{12}$	$4.20x10^{11}$
LVPS-Endcap	635	390	400	400	$2.44x10^{11}$	$5.64x10^{10}$

Table 7.1: Radiation doses simulated for $4ab^{-1}$ of HL-LHC running [42].

7.3 TileCal Radiation requirements for HL-LHC

TileCal's read-out electronics are shielded by the calorimeter body, therefore radiation exposure limits are less stringent than those of other ATLAS sub-detectors (see Figure 7.6). The expected increase in particle fluxes for the HL-LHC, however, requires more radiation tolerance in the on-detector components [85]. For the LVPS Brick, an integrated total ionising dose (TID) of up to 200 Rad and displacement damage (NIEL) corresponding to 2.44×10^{11} 1 MeV n/cm^2 is expected over the 10 years of HL-LHC operations. SEE rate estimations are based on a fluence of up to 1.5×10^{12} protons cm^{-2}. The current on-detector read-out electronics save digitized data from every bunch crossing that passes through digital pipelines, making the data subject to corruption due to higher SEE rates. The improved TileCal circuits address this issue by transferring data off-detector, away from the pipeline memory, which are exposed to radiation. Table 7.1 lists quantitatively the locations of the on-detector electronics boards and the simulated doses for the most exposed electronics during the whole HL-LHC period. Safety factors are introduced by the ATLAS Electronics Coordination Group as specified in Table 7.1 to account for error margins associated with the different types of radiation tests.

7.4 Radiation Testing of the LVPS Brick prototypes

To qualify the LVPS Brick for use at the HL-LHC, the power supply must be tested for Total Ionizing Dose (TID), Non-Ionizing Energy Loss (NIEL), and single-event effects (SEE), using radiation doses that correspond to the expected exposure over the course of 10 years of HL-LHC operation, with safety factors. Following the ATLAS Radiation Policy and the ATLAS policy on radiation tolerance electronics [85]. For our radiation tests, since the specifications differed depending on the type of radiation, we chose three sites with relatively pure particle sources for our radiation experiments. This seemed prudent in order to clearly understand the sources of radiation damage, since the mechanisms are different for each type of radiation. We performed six sets of radiation susceptibility measurements total to test (see Table 7.2) the various prototype LVPS Brick. The following is a summary of these studies.

Radiation Type	Location	Simulated Dose/ Fluence	SF_{sim}	SF_{lot}	Target Dose
TID [Gy]	Barrel	53.56	1.5	4	1607
	End-caps	34.3	1.5	4	1029
NIEL [n/cm^2]	Barrel	3.49 x 10^{12}	2	4	2.79 x 10^{13}
	End-caps	9.59 x 10^{11}	2	4	7.67 x 10^{12}
SEE [p/cm^2]	Barrel	5.3 x 10^{11}	2	4	4.24 x 10^{12}
	End-caps	9.8 x 10^{10}	2	4	7.84 x 10^{11}

Table 7.2: LVPS Radiation Type, simulated dose and target dose. The radiation is computed in terms of total ionizing dose (TID), non ionizing energy loss (NIEL) and single event effect (SEE) are shown. The three last columns show the radiation dose assumed in 2020 for the present LVPS design, the survival limit dose and the safety factor assumed for the new design. Safety factors are introduced by the ATLAS Electronics Coordination Group as specified in Table to account for error margins associated with the different types of radiation tests. Safety Factors: SF_{sim} (Safety Factor on the simulation giving the Doses or Fluences) and SF_{lot} (Safety Factor corresponding to the variation from lot to lot of components) [34].

7.4.1 Total Ionizing Dose testing

We performed one test on the Bricks for Total Ionizing Dose susceptibility using gamma irradiation from the cobalt-60 (^{60}Co) CERN facility. The test was performed on 28 April - 01 May 2019. The gammas were produced from a ^{60}Co source, with energy equivalent of 1 MeV. The dose rate of the source was measured by an ionization chamber at the start of the runs. The test apparatus was configured as shown in Figure 7.7 The port containing the ^{60}Co source is on the left side of the picture. The Bricks were situated 76 centimeters from the source. At this location, the dose rate was estimated to be 2.2 krad/hr. In each run, we went up to 500 Gy of TID at the center of the setup to make sure we get 480 Gy at the farthest point of setup from the source. The 4 Bricks were assembled on a panel with cooling fans and 5 Ohm resistive loads. The Bricks were operating at 2 A (similar to condition of powering half of a mini drawer). The flux from the source was parallel to the plane of the printed circuit boards. There were also buffer boards that were utilized below the line of sight of the port, and were protected with lead Bricks. The apparatus was cooled using a 40 cm fan that blew ambient air onto the Bricks. The readout computer was located outside of the room, connected to the buffer boards through 16 meters of cable. The Bricks were being controlled and monitored from the control room using a data acquisition module from National Instruments. Each Brick was connected to DAQ module through a buffer board. Monitored parameters from each Brick were the output voltage and current, and temperatures on two points on the Bricks.

TID Results

There were no hard failures of Bricks during the TID irradiation study. No transient event phenomena occurred during gamma irradiation, in the power supplies. All the Bricks

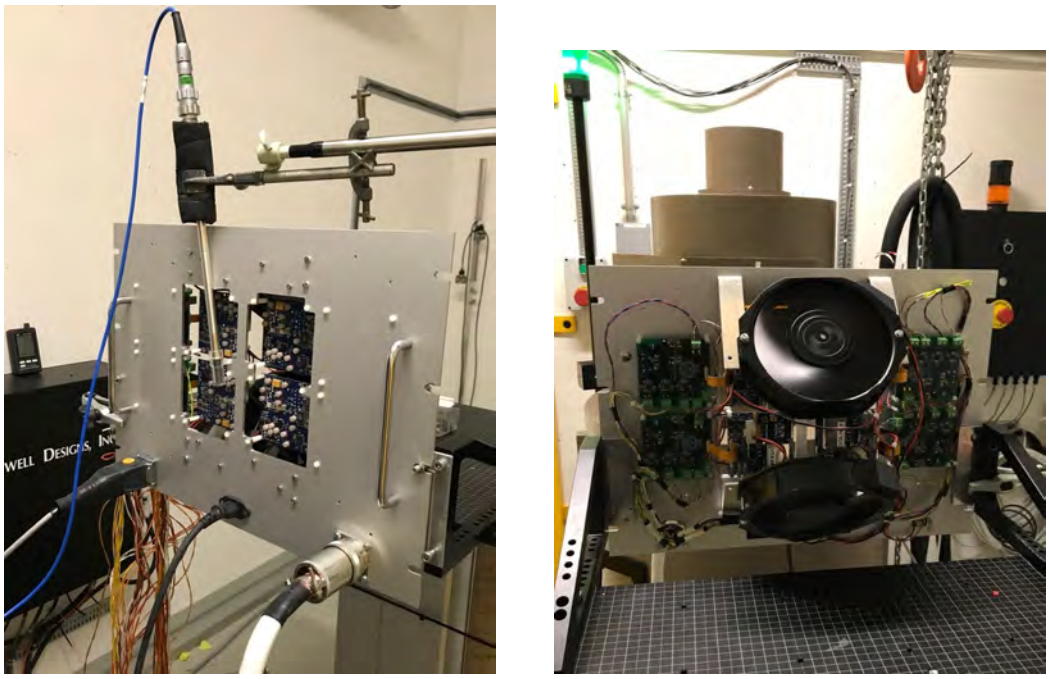

Figure 7.7: Picture of the LVPS Brick (Left) and Interface Board (Right) in the cobalt-60 test facility at CERN.

were running and monitored during up to end of the tests with only an output voltage drop of 1 mV/Gy. Since the accepted range of output voltage is 8 to 12 V from the point of load regulators, this drop is completely acceptable due to wide range of input voltage for our front end electronics. Parameters showed expected behaviour as a function of time for output voltage as shown in (Figure 7.10) and the output current in (Figure 7.10) both over a 12 hour duration. There was a general degradation of performance observed as the total dose increases. Most notable are:

- An increase in clock jitter
- An increase in the clock frequency
- Slow deviations of the monitored voltages
- A tendency of the opto-isolator to eventually fail at very high dose rates. The nature of the failure was such that the Brick failed to restart after being turned off in a normal way.
- A tendency of the FET driver to eventually fail at very high dose rates

We noted that these effects for the most part showed up at very high dose rates. We conclude that the design is sufficient for the next decade of running, given the high safety factor imposed on the TID specification.

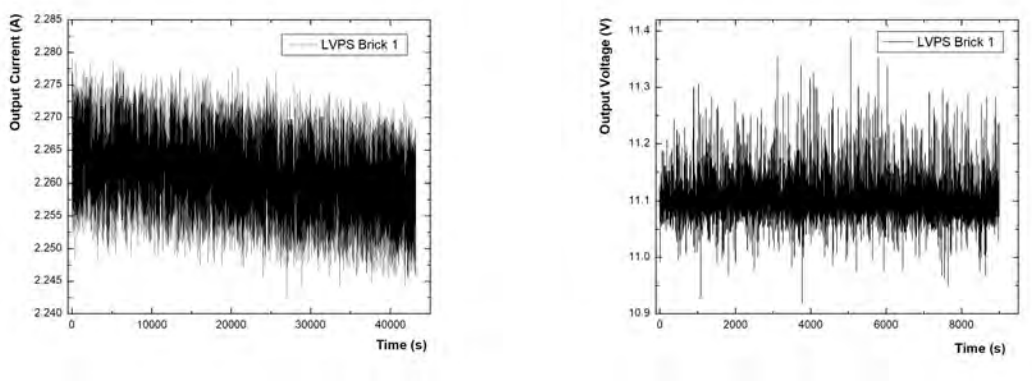

Figure 7.8: Output Current (A) left and output voltage (V) right of the LVPS monitored during irradiation testing at the ^{60}Co facility.

Brick	Buffer Board	Load	Trip?
V8.3.1	0	150 ohms	No
V8.3.2	1	150 ohms	No
V8.3.1	2	150 ohms	Once
V8.3.2	3	150 ohms	Once

Table 7.3: Bricks tested at ^{60}Co for gamma susceptibility.

7.4.2 Non-Ionizing Energy Loss testing

Three runs of NIEL tests on the Bricks with neutrons were performed in the TRIGA reactor [86] in Ljubljana, Slovenia from Quarter 4 in 2019 and Quarter 3 in 2020. The Bricks were irradiated in the in the tangential Channel, a horizontal channel piercing the concrete biological shield, the reactor tank and the graphite reflector around the core is to allow irradiation of electronics of lateral dimensions of at least up to 12 cm in a relatively intense neutron flux, of the order of 10^{12} n/cm^{-2} s^{-1}. The tests were performed on individual components and on full Bricks with energy equivalent to 1 MeV equivalent neutrons. To use this facility, the Bricks and components under test were placed in a water-tight vessel, and lowered into the cooling pond of the reactor. At the bottom of the pond is the exposure area. When the reactor is powered, a door is opened, allowing the sample to receive the neutron flux from the reactor core. Because of the configuration, this reactor can support a large sample volume, with a nearly uniform flux over a 30 cm x 30 cm area. Pictures of the setup are shown in Figure 7.9.

7.4.3 NIEL Results

Table 7.4 below shows the results of the neutron tests performed at Ljubljana. Three of the components did not survive the full fluence of 2.5 x 10^{13} n/cm^2, but they survived a lower fluence of 2 x 10^{13} n/cm^2. It was discussed in several internal meetings that if the lot safety factor can be removed, the NIEL target fluence will become 7 x 10^{12} n/cm^2. We



Figure 7.9: Output Current (A) and output voltage (V) of the LVPS monitored during irradiation testing at the Ljubljana, TRIGA reactor.

Component	Test Result at 2×10^{13} n/cm^2	Test Result at 2.5×10^{13} n/cm^2
Brick	Fail (1)	Fail (4)
LT1681, LT3080	Fail (2)	Fail (4)
LM6142	Pass (6), Fail (2)	Pass (3), Fail (1)
LM9074, IR2110	Pass (2)	Pass (1)
SI8920	Pass (4)	Pass (2)

Table 7.4: Summary of components and Brick tested at different target fluences.

concluded our NIEL tests, considering that we can procure the three mentioned components from a single batch as per the radiation electronics task force (RETF) recommendations.

7.4.4 SEE testing

SEU testing was performed at the Paul Scherrer Institute (PSI), using the Proton Irradiation Facility (PIF) which is constructed for testing spacecraft components. Of particular interest in these studies was the performance of certain critical parts: the LT1681 controller chip; the IR2110 FET driver; and the SI8920-Isolation amplifiers. The functions of these parts in the circuit were described in Section 4 under the LVPS Brick Design. We performed three sessions of irradiation tests on the Bricks with protons using at PSI with 200 MeV proton beam with a flux of 3×10^8 p/cm^2/s. The beam cross section in PSI is 5 cm by 5 cm. This means we cannot test the Bricks and had to design boards for individual components to perform the tests and mimic the operation of the chips on the LVPS Brick. A single reference chip outside the beam circle was used for the tested boards. An active measurement of the response of the Bricks and component boards under irradiation was desired, thus a reasonable time period to search for any detrimental effects was chosen to be several hours. The SEE effects should be independent of rate. The general setup that we used is shown in Figure 7.11. The Boards were placed so that the front face in the

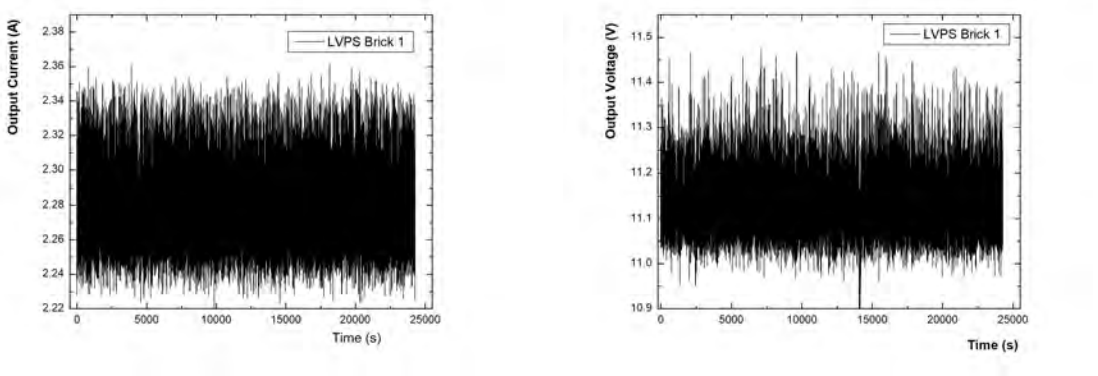

Figure 7.10: Output Current (A) and output voltage (V) of LVPS Brick 1 monitored during irradiation testing at the Ljubljana, TRIGA reactor.

fixture was at a distance of 157.5 cm from the beam with the boards situated to be perpendicular to beam. Although not shown in this photo, several equipment (Oscilloscope, Function generator, Power Supply and DAQ module and PC) were put out in the maze area. Alignment was done with a laser and mirrors and the intensity normalized. The Beam intensity was controlled by us in a remote section facility. The readout computer located 16 meters away in a room outside of the radiation area. The monitor voltages of the Boards under test were measured continuously during the runs.

7.4.5 SEE Results

Results obtained from testing the PSI facility. Due to the beam size of the facility (cross section of circle with diameter of 5 cm). We only needed to test 3 chips (1 isolation amplifiers and 1 MOSFET driver and MOSFET). Three boards were made, each having 10 pieces of one of the components placed in a circle of 5 cm diameter. Voltages and currents of the components were monitored during the tests using a DAQ module. Target fluence for each board is 5.42 x 10^{11} p/cm^2 (5.42 x 10^{12} p/cm2 will be received in total by each type of chip). Having a flux of 2 x 10^8 p/cm^2 , we need 2700 seconds for each board. From 10 irradiated chips on the board, at the end of the runs, 4 chips were damaged due to TID effects caused by the interaction of high-energy photons or charged particles (mainly protons and electrons) with the atoms of that material. The output voltage of 5 of the irradiated chips measured by DAQ was as expected (from which one was dead at the end of the tests). The output voltage of 3 of the irradiated chips measured by DAQ showed huge fluctuations. The output voltage of 2 of the irradiated chips measured by DAQ went to almost zero for some time during irradiation. Results of some of the chips are illustrated in Figures 7.13, 7.14 and 7.15. The tests were performed in 4 runs, and there were a power cycle between each two consecutive runs:

- There were also three power cycles at the end of the tests, just to see if any of the faulty chips will behave correctly after power cycle, or if any working chip will

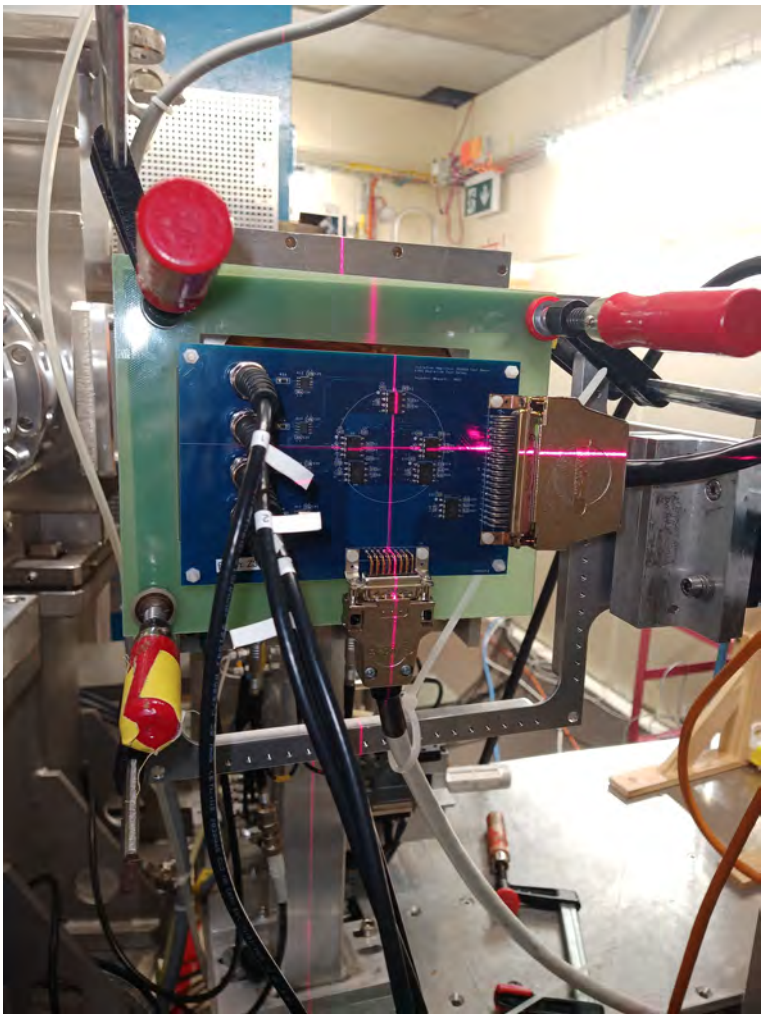

Figure 7.11: Isolation amplifier Board being set-up for irradiation.

continue to work

- The results from the reference chip (chip U11) showed that this chip behaved completely normal during the test however several isolation amplifier chips had huge fluctuations during irradiation as seen in Figure 7.12. 6 out of 10 chips from each isolation amplifier board didn't survive the full dosage.

7.5 Irradiation Studies Summary

The LVPS Brick was tested for TID, NIEL and SEE to verify the readiness of the design for the HL-LHC era. The design proved to withstand up to 20 kRad of TID, being enough to qualify it for the HL-LHC lifetime within the radiation doses simulated as reported in the ATLAS Tile Calorimeter Phase-II Upgrade Technical Design Report [44]. However, the new dose values showed in were obtained after new simulations with new geometry were done as presented in an internal meeting [44]. The new values dictate that to qualify

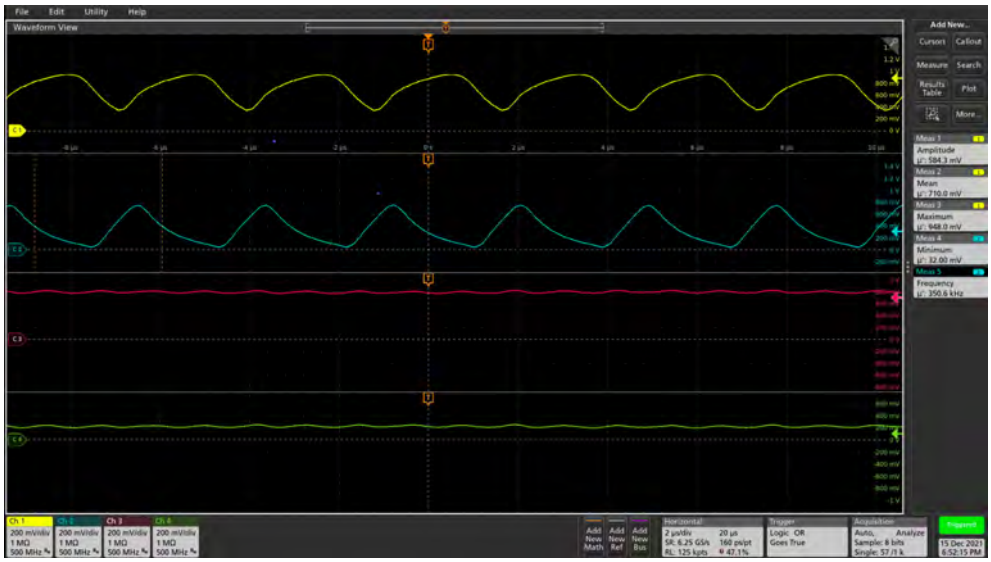

Figure 7.12: Instability with Isolation amplifier.

the board, either a TID test should be done up to either 72 kRad or to 14.4 kRad if the test includes annealing of the chips up to a day (24 hours) under bias room temperature. This neutralizes the oxide-trapped charge that was built up during the exposure to radiation. A radiation testing campaign to test the new LVPS Bricks for radiation tolerance has been completed.

1. The measurements of the Brick performance to gamma irradiation (TID) showed the following: There were no hard failures of Bricks during the irradiation study. There is a general degradation of performance observed as the total dose increases. Most notable are: an increase in clock jitter; an increase in output noise; an increase in the clock frequency; slow deviations of the monitored values; a tendency of the opto-isolator to fail, probably at very high dose rate, with the net result that the Brick fails to restart after turned off. We note that these effects for the most part showed up at very high dose rates. We conclude that the design is probably sufficient for the next decade of running, given the high safety factor imposed on the TID specification.

2. The measurements of the Brick performance to neutron irradiation (NIEL) showed the following: There were no hard failures during the irradiation studies that were attributable to radiation damage. There is a small degradation of performance observed as the total dose increases. Since the changes observed were small, we concluded that the design is sufficient for the next decade of running, given the high safety factor imposed on the NIEL specification.

3. The measurements of the Brick performance to proton irradiation (SEE) showed the following: There were hard failures for 1 of the components during the irradiation studies. However, these failures are attributed to the isolation amplifier which

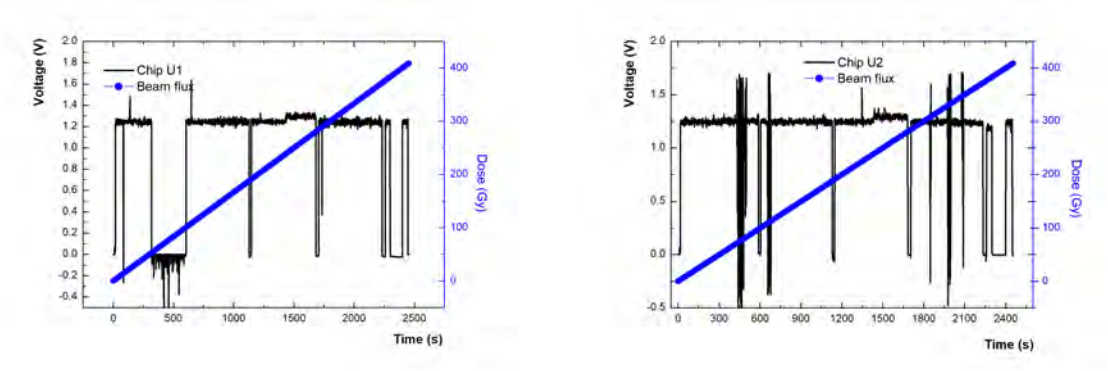

Figure 7.13: Irradiated Chip U1 and U2 performance. The results from Chip U1 show that in the first run, the output voltage goes to zero, which was then fixed by a power cycle to zero, which was then fixed by a power cycle. The chip survived the test after receiving 400 Gy. The results from Chip U2 show that the output voltage had some fluctuations during all the runs, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy.

showed huge instabilities as soon as the beam was turned on 7.12. An attempt to find a suitable candidate to test for TID, NIEL and SEE is being investigated. The conclusion is that once a suitable candidate is found on the detector is much higher than what would be predicted by SEE in the controller chip. Nonetheless, we conclude that the SEE problem with the isolation amplifier should be addressed before pre-production commences.

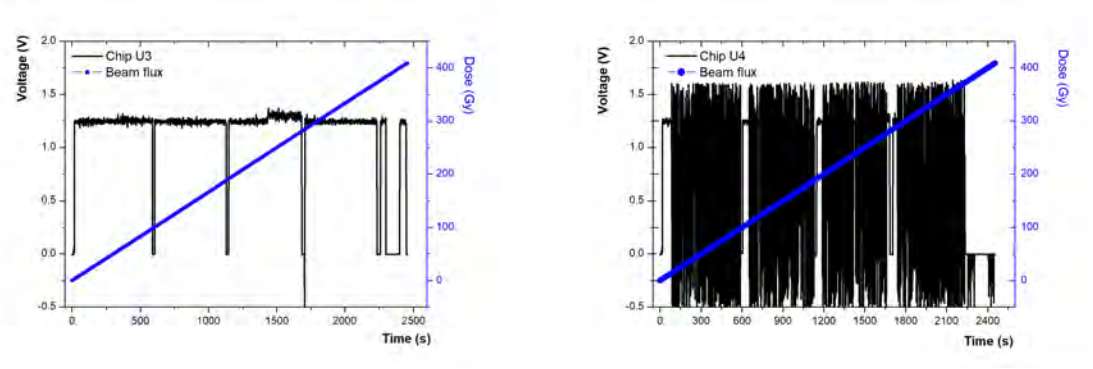

Figure 7.14: Irradiated Chip U3 and U4 performance. The results from Chip U3 show that this chip almost behaved like the reference chip during the whole test. The chip also survived the entire dose of 400 Gy. The results from Chip U4 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the beginning of each run. The fluctuations did not stop when the beam was stopped at the end of each run (a power cycle was needed). After the last run (receiving 400 Gy), the chip stopped working properly (due to TID effects), and even the two power cycles did not fix the issue.

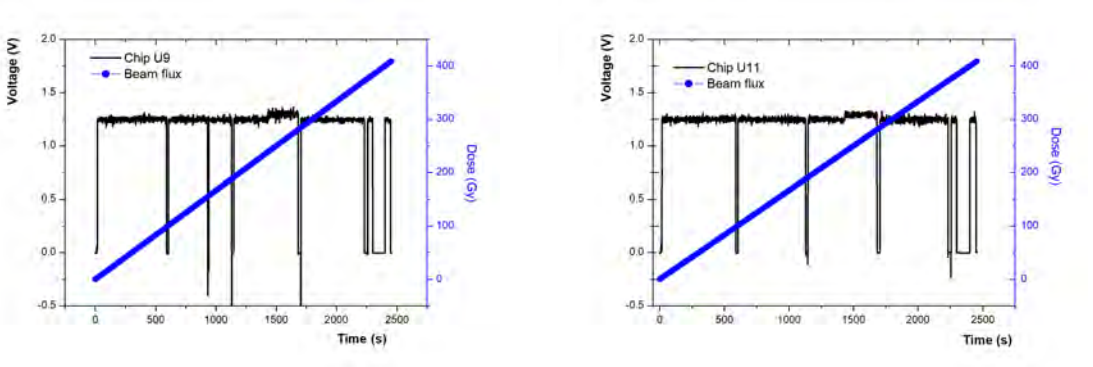

Figure 7.15: Irradiated Chip U7 and U11 performance. The tests were performed in 4 runs, and there were a power cycle between each two consecutive runs. There were also two power cycles at the end of the tests, just to see if any of the faulty chips will behave correctly after power cycle, or if any working chip will continue to work.The results from Chip U9 show that this chip almost behaved like the reference chip and did not have any large fluctuations. The chip also survived the full radiation dose of 400 Gy. The results from the reference chip (chip U11) shows that this chip behaved completely normal during the test.

Chapter 8

Conclusions

The LVPS Brick project and progress were examined in both a Preliminary Design Review (PDR) and Final Design review at CERN. Several points were raised for discussion prior to the pre-production stage. These crucial points from the FDR, as well as other difficulties identified in lab tests and radiation tests, strongly support a minor change of the LVPS Brick based on the identification of a good candidate for the isolation amplifier.

8.1 LVPS project summary

The work I have done for this thesis concerns the test and characterization of the all produced iterations of the Brick from version 8.1 to 8.4.2. The front-end electronics is powered by the low voltage power supplies, one for each module, composed by eight Bricks controlled by a local motherboard. Since the beginning of operation the low voltage power supplies have proved to be the critical point of the front end system of TileCal: A redesign project for the Bricks was taken by Wits University and University of Texas at Arlington aiming at producing 2048 Bricks for the HL-LHC. The latest design addresses several aspects of the Bricks that caused the instabilities of the initial design. A particular attention has been devoted to reduce the temperature of the Brick, update the start up circuitry to include the Tri-State functionality, to improve the protection circuits and to have a better coupling with the cooling and radiation tolerant for the High Luminosity phase.

A small number containing prototypes of the new Bricks have been installed and exposed to CERN's Super Proton Synchrotron accelerator for the 2021 test beam campaign. The module obtained excellent results. All the Bricks produced have undergone a long list of tests at Wits University to ensure the high quality and reliability needed for the detector operation. The strict checkout procedure is based on two large testing sessions, both followed by debug and repair sessions. The sessions address protection and monitor circuits and are separated by the Burn-in which aims at having the Brick working under stress conditions with the purpose of finding any component or soldering close to

the failure edge. At the end of the checkout procedure all the Bricks match the design parameters within allowed error ranges. The Bricks are entering the Final Design Closure in preparation for the pre production phase and will be installed on the detector during 2026-2028 period.

8.1.1 Brick Design and production

The LVPS Brick prototypes v8.1 and v8.2 were the first prototypes produced by Wits University together with several local industry partners. After the PDR, there were two design revisions. v8.3.1 and v8.3.2 designs that included the following 2 changes:

- Simplifying the enabling circuit and remove the bipolar transistors to improve the NIEL tolerance.
- Separating the bias voltages to different thermistors for temperature monitoring, to allow the over temperature protection in case of ELMB2 failure.

The finalization of the Tri-State method necessitated the slight tweak of the v8.3 Bricks. The latest designs v8.4.1 and v8.4.2 included 2 changes

- Updating the startup circuit to make it compatible with Tri-State control scheme.
- Adjusting the soft startup circuit to limit the input inrush current, and avoid the trip during the startup.
- The PCB will be fabricated in IPC class 2 with halogen free materials for LV Bricks pre-production as per the new CERN safety regulations.

It is expected to have a slight modification after conclusion of the radiation tests for the remaining component.

8.1.2 Functional testing

The Prototype LVPS Bricks have been tested both at the University of the Witwatersrand and in the TileCal low voltage Vertical Slice Tests (VST) at CERN. Pre-production LVPS Bricks are planned to be tested in the second VST in 2022. The LVPS Bricks initial test stand hardware has been prepared to test all new Brick that will be produced with results of previous test on the Appendices.

8.1.3 Burn-in testing

Burn-in test bench design has been finalized and in operation, using a water cooling system with temperature controlled by a chiller. Two sets of burn-in stations will be used for main production testing. The Burn-in test sequence has been defined, each LVPS Brick will be tested with a 5 A load for 6 hours with preliminary results shown in section 6.

8.1.4 Radiation testing

The campaign of irradiation tests for LVPS Bricks started 2 years ago, and has been mostly following the original ATLAS radiation policy.

- The SEE tests were only focused on the replaced components after CHARM tests. The new components (SI8920 and LT3080) were tested at PSI facility. SEU were observed for the isolated amplifier (SI8920), which a few were recovered by a power cycle.
- TID test was performed at Cobalt-60 facility at CERN with 3.75 Gy/hr up to 500 Gy, then 0.3 Gy/hr up to 305 Gy on LVPS Bricks. Similar behavior was observed in both low and high dose rate tests
- NIEL test was performed at TRIGA reactor in Ljubljana on LVBricks, 3 components (LT1681, LT3080 and LM6142) were found to survive a lower fluence of 10^{13}, 1 MeV n/cm^2.

8.2 Discussion and prospects

This work has followed the development and testing of the ATLAS TileCal LVPS Brick over three revisions. The latest revision of the LVPS Brick is version 8.4.2 which has been extensively developed, tested, and ready for installation in the TileCal upgrade Demonstrator system for testing in ATLAS running conditions. A new revision, v8.5, is currently under development and aimed at solving the remaining issues. The LVPS Brick will need to be produced and extensively tested in advance of the scheduled Production Readiness Review in 2022, after which approximately 1024 Low Voltage Power Supplies will be produced, tested and delivered to CERN as per the contribution of Witwatersrand University to the ATLAS Upgrade for the HL-LHC era.

Appendix A

Schematics and Tri-State control simulations

Appendix A is used to provide some supplementary materials. For example, schematics of the LVPS Bricks shown in Figure A.1, the custom schematic boards used for irradiation studies to test individual components shown in Figure A.2, A.3. This is provided to both the PCB manufacturer and the population house. The Tri-State control simulations were done to validate the Brick start-up circuitry using the new Tri-State control method. This allows for the Brick to be started, kept alive and switched off using a single line. The simulations can be seen on Figures A.5 and A.6.

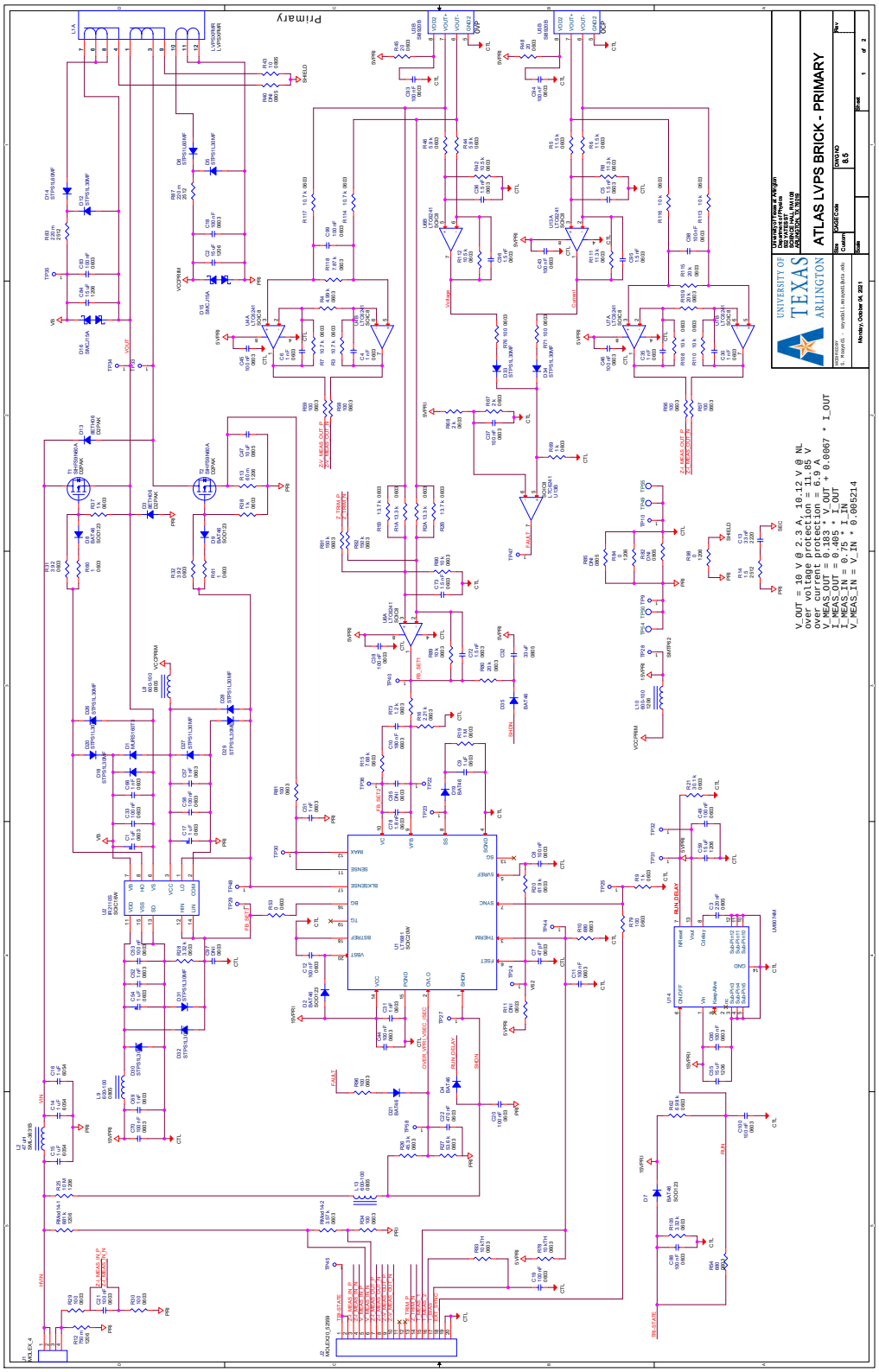

Figure A.1: LVPS V8.5 Schematic.

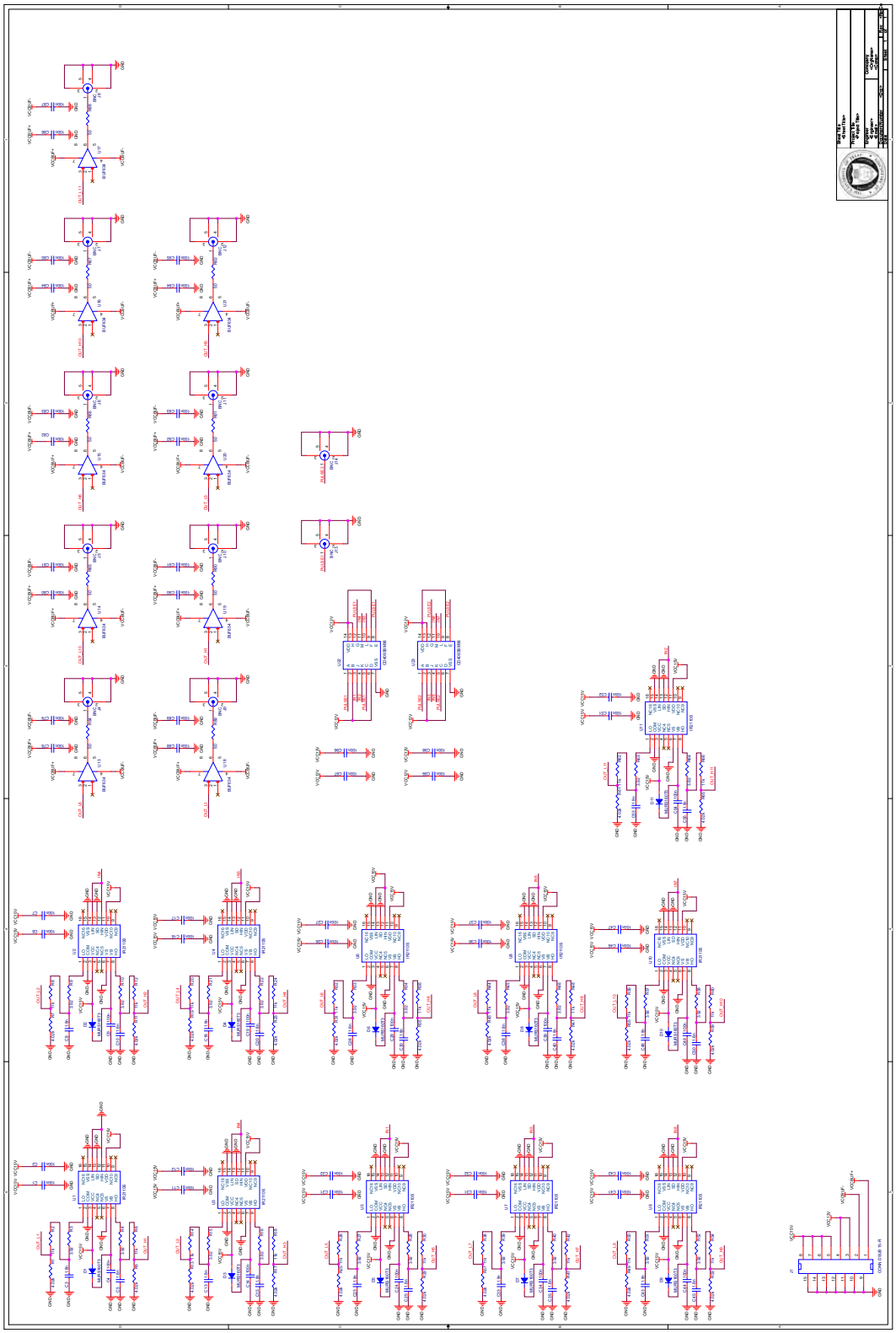

Figure A.2: Schematics IR2110.

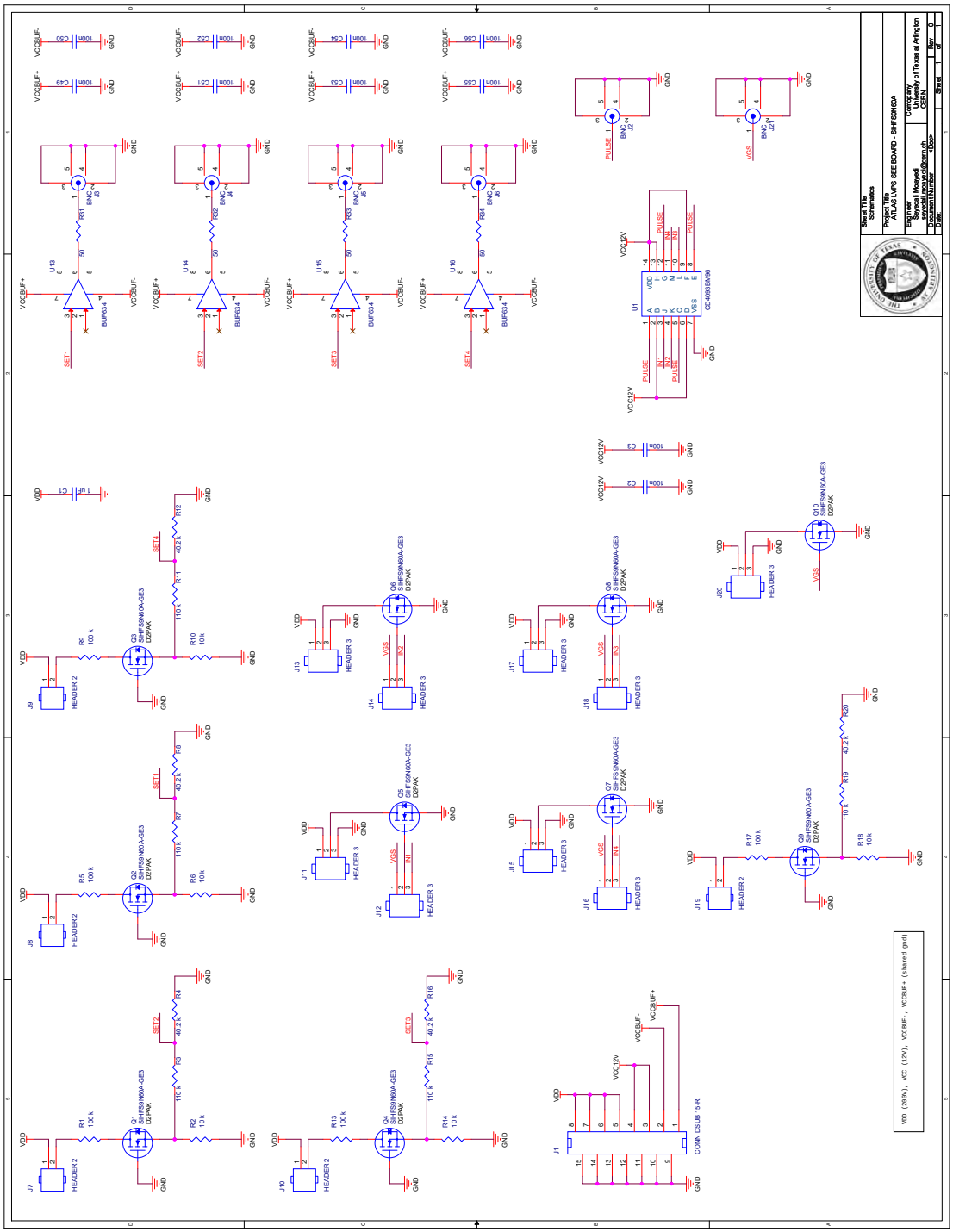

Figure A.3: Schematics MOSFET.

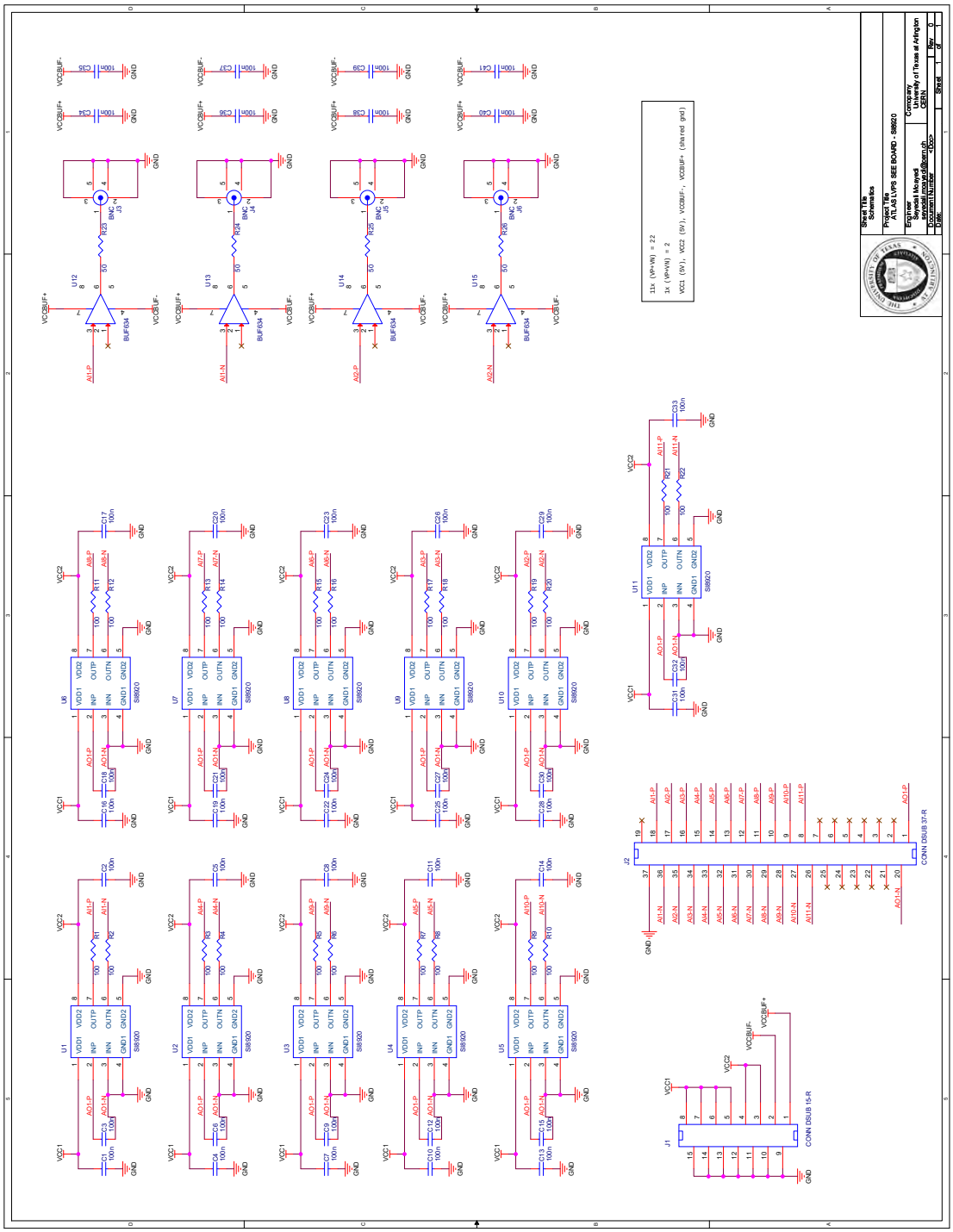

Figure A.4: Schematics SI8920.

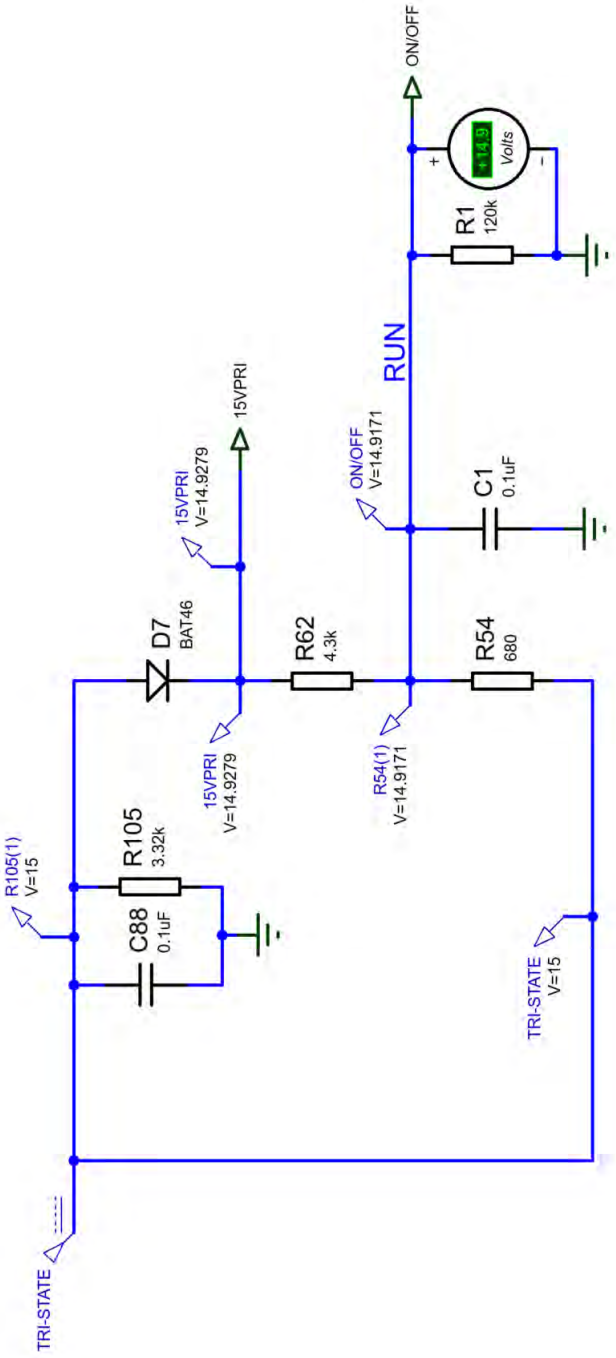

Figure A.5: Tri-State control method at 15V DC.

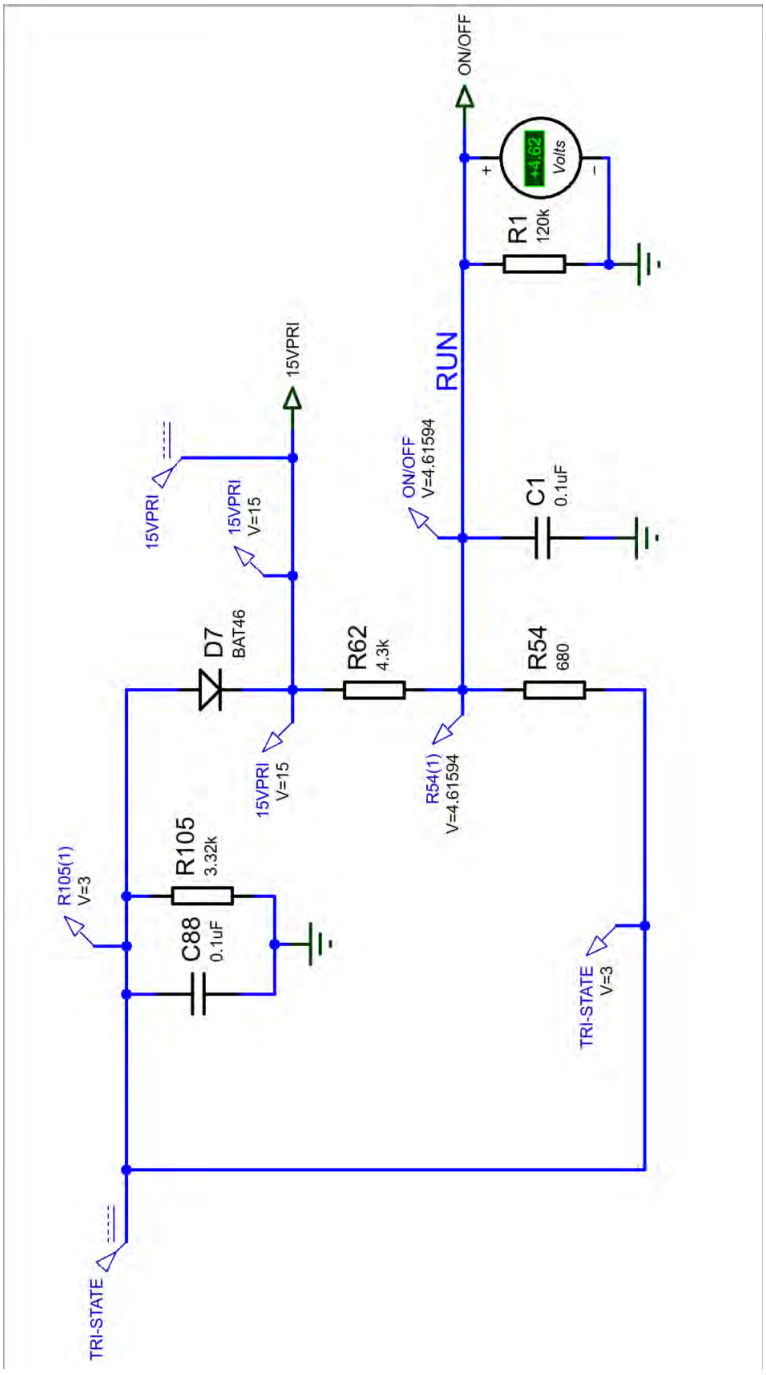

Figure A.6: Tri-State control method at 0V DC input.

Appendix B

Test benches set up and results

Appendix B includes the Test station set-up for the individual Brick and the Burn-In test Bench firmware development discussed in section 6. Experimental results, test station architecture, detailed radiation experimental settings. Figure B.1 shows the output log file during testing of the LVSP Brick. The results consists of checking the minimum stable load, voltages and temperature readings B.2. Figure B.3 depicts the set up of the Brick on a heat sink plate running on an external refrigeration unit. Figure B.4 shows the full compilation of the initial test stand and a custom temperature test stand to test individual components. Some results of the Bricks are also shown in Figures B.5, B.6 and B.7. The MainBoard PIC16F series micro controller code was written and modified for the new custom boards used for the Burn-In test station. The registers and clock frequency was also updated this can be seen on Figures B.8, B.9 and B.10. Testing of the code and ADC channels was performed using a serial monitoring program and some values from the ADC chip can be seen on Figure B.11. The new LabVIEW control panel was refactored without changing the overall functionality of the software but updated and modified for the use case of the latest version of the LVPS Bricks as seen in Figure B.12.

```
Username
Edward
1 status
PASS
1 DC sdev
0.270600
1 min freq
297162.100000
1 max freq
297430.600000
1 freq sdev
59.950000
1 min stable load
1.640000
2 status
PASS
2 Vout
9.962730
2Waveform

3 status
PASS
3 OVP
11.777100
4 status
PASS
4 OCP
10.440000
5 status
PASS
5 DC stdev
0.608000
5 DC avg
23.117100
5 Vout rms
0.013200
5 Vout feak
0.175000
5 freq
294.285500
6 status
PASS
6 Max Startup
0.000000
6 Min Startup
0.000000
6 #Startups
5.000000
7 status
PASS
7 Vout vs trim rms error
0.000927
7 Vmon vs trim slope
0.080204
7 Vmon vs trim offset
-2.305309
7 Vmon vs trim rms error
0.000977
7 Vout vs trim offset
10.929211
7 Vout vs trim slope
-0.380826
7 Monitor vs Trim
```


Figure B.1: Test stand log results of measured HE002 Brick.

```
7 Vout vs Trim

8 status
FAIL
8 Imon vs load rms error
0.172789
8 Vout vs load slope
-1.710918
8 Vout vs load offset
15.691154
8 Vout vs load rms error
2.798877
8 Imon vs load slope
-0.022267
8 Imon vs load offset
0.363318
8 Vout vs Load

8 Imon vs Load

9 status
PASS
9 Vin mon
1.031744
10 status
PASS
10 Iin mon
-0.008174
11 status
PASS
11 temp1
130.523639
11 temp2
132.756077
Brick Serial Number

Brick Type
```


Figure B.2: Test stand results of measured HE002 Brick.

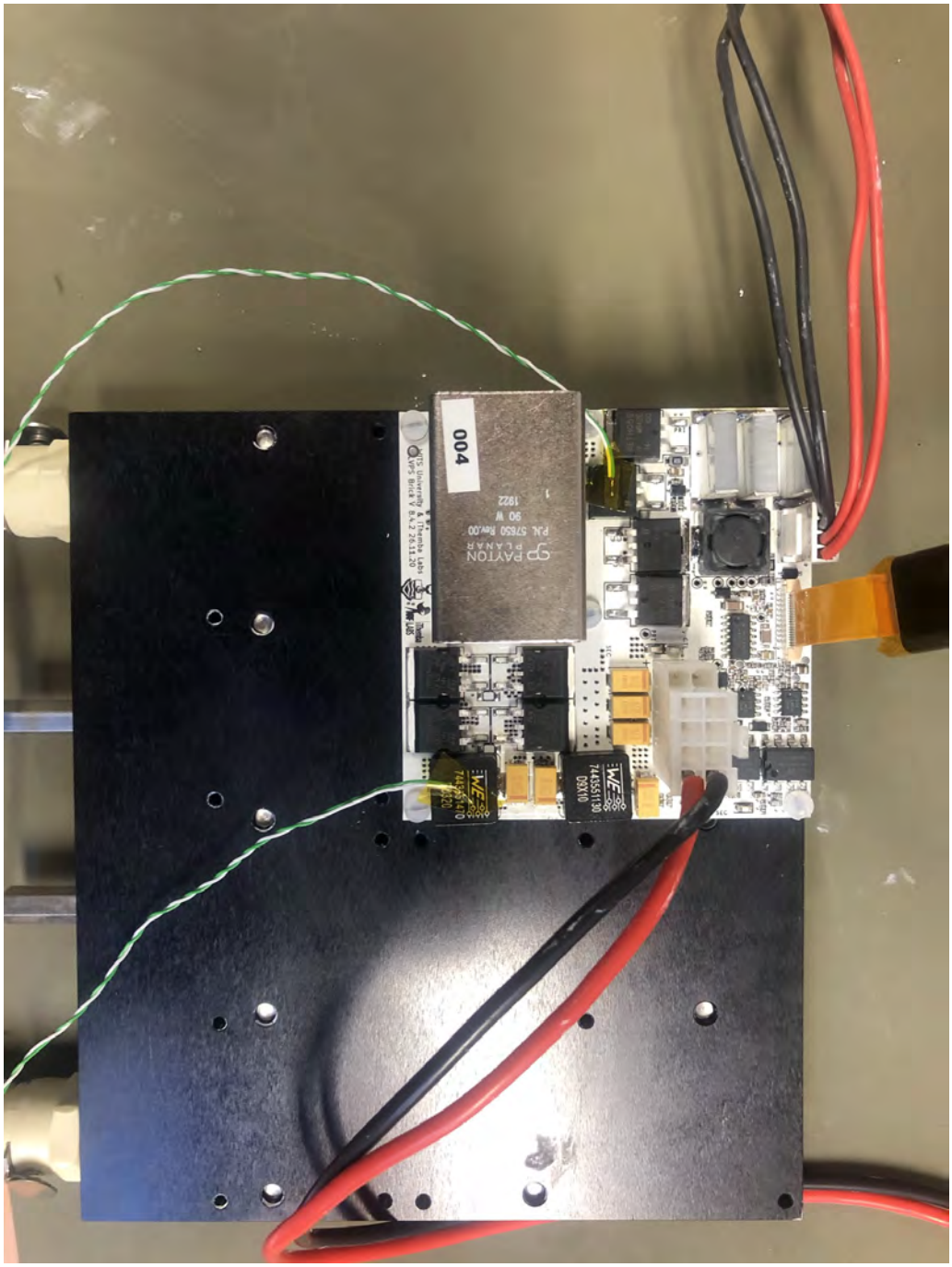

Figure B.3: Test stand set up of measured Brick.



Figure B.4: Test stand set up of prototype Brick.

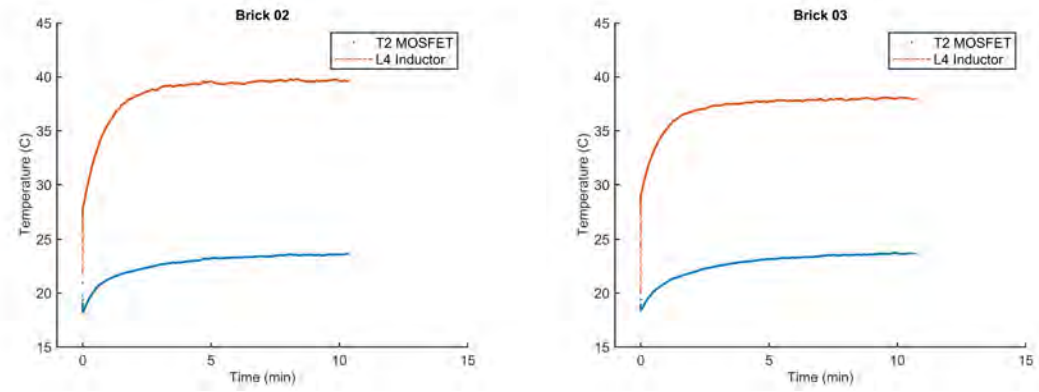

Figure B.5: Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks.

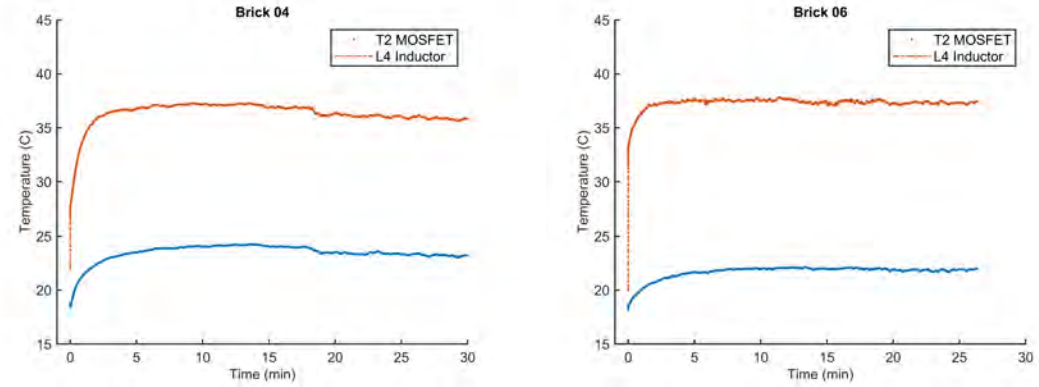

Figure B.6: Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks.

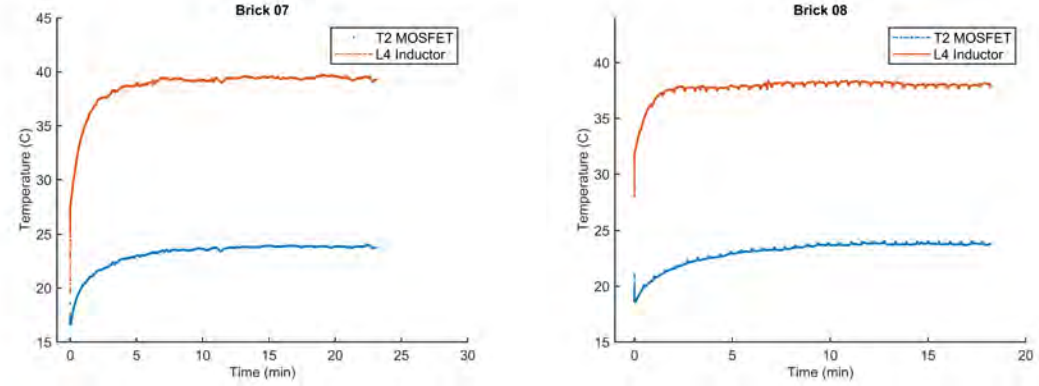

Figure B.7: Temperature distribution for the MOSFET and Inductor temperatures, measured on LVPS Protoype Bricks.

```
/*
 * File:   led.c
 * Author: Edward Nkadimeng
 *
 * Created on March 29, 2021, 1:16 PM
 */
/*
 * File:   MainBoard.c
 * Author: Edward Nkadimeng
 *
 * Created on March 29, 2021, 12:52 PM
 */


#include <16F883.h>
#include <ctype.h>
#device adc=8
#use delay(clock=16000000)
#fuses NOWDT,HS, PUT, NOPROTECT, BROWNOUT, NOLVP, NOCPD, NOWRT, NODEBUG
#use rs232(uart1, baud=9600, xmit=PIN_C6, rcv=PIN_C7)  // Jumpers: 8 to 11, 7 to 12
#use fast_io(A)
#use fast_io(B)


#define BUFFER_SIZE 32
BYTE buffer[BUFFER_SIZE];
BYTE next_in = 0;
BYTE next_out = 0;


#int_rda
void serial_isr() {
   int t;

   buffer[next_in]=getc();
   t=next_in;
   next_in=(next_in+1) % BUFFER_SIZE;
   if(next_in==next_out)
     next_in=t;           // Buffer full !!
}

#define kbhit (next_in!=next_out)

BYTE bgetc() {
   BYTE c;

   while(!kbhit) ;
   c=buffer[next_out];
   next_out=(next_out+1) % BUFFER_SIZE;
   return(c);
}

void relay(int i)
{
output_b(0);
delay_ms(100);
switch (i) {
    case 1:output_high(PIN_B0);break;
    case 2:output_high(PIN_B1);break;
    case 3:output_high(PIN_B2);break;
    case 4:output_high(PIN_B3);break;
    case 5:output_high(PIN_B4);break;
    case 6:output_low(PIN_A0);break;
    case 7:output_high(PIN_A0);break;
    default:;// output_b(0);
    }
```

Figure B.8: MainBoard PIC16F series micro-controller code.

```
}

#define MAX_CHAR 5

int MarginalityRead(void)
{
   long timeout;
   char x[MAX_CHAR];
   int hist[10];
   int i,j,index,max;

       timeout=100;
       i=0;
       for (j=0;j<MAX_CHAR;j++)
         {
          x[i]=0;
          while(!kbhit)
              {
              delay_ms(1);
              timeout--;
              if (timeout==0) goto nextchar;
              }
           /* Waiting for address */
           x[i]=getc();
           i++;
nextchar:  timeout=100;
         }
       for (j=0;j<10;j++) hist[j]=0;

       for (j=0;j<i;j++)
         {
         if (x[j]<10)
            {
            hist[x[j]]++;
            }
         }

       max=0;
       index=255;
       for (j=0;j<10;j++)
         {
         if (hist[j]>max)
            {
            max=hist[j];
            index=j;
            }
         }

       for (j=0;j<MAX_CHAR;j++) printf("%i ",x[j]);
       printf("\n\r");
       for (j=0;j<10;j++) printf("%i ",hist[j]);
       printf("\n\r");
       printf("%i\n\rXX\n\r",index);

return(index);
}

void main()
{

   char x;

   setup_adc_ports(NO_ANALOGS);
   setup_adc(ADC_OFF);
   setup_spi(FALSE);
   setup_timer_0(RTCC_INTERNAL|RTCC_DIV_1);
```

Figure B.9: MainBoard PIC16F series micro-controller code.

```
   setup_timer_1(T1_DISABLED);
   setup_timer_2(T2_DISABLED,0,1);

   enable_interrupts(global);
   enable_interrupts(int_rda);

   set_tris_a(0);
   set_tris_b(0);
   set_tris(0);
   output_b(255);


output_low(PIN_A4);
      delay_ms(1000);
      output_high(PIN_A4);
      delay_ms(1000);
      output_low(PIN_A4);
      delay_ms(1000);
      output_high(PIN_A4);
      delay_ms(1000);
      output_low(PIN_A4);
      delay_ms(1000);
      output_high(PIN_A4);
      delay_ms(1000);
      output_low(PIN_A4);
      delay_ms(1000);
      output_high(PIN_A4);
      delay_ms(1000);
      output_low(PIN_A4);
      delay_ms(1000);
      output_high(PIN_A4);
      delay_ms(1000);


//   prints("\r\nTransformer tester ready\r\n");
  output_low(PIN_B0);
   while (kbhit)
   x=getc(); // Buffer clear
   while (input(PIN_B0)==0);
   while (1)
   {


      if (input(PIN_B0)==0)
         {
         x = MarginalityRead();

         if (x!=255) output_b(x & 15);

         while (kbhit) getc(); // Buffer clear

        while (input(PIN_B0)==0);
         }
   }
}
```

Figure B.10: MainBoard PIC series micro-controller code.

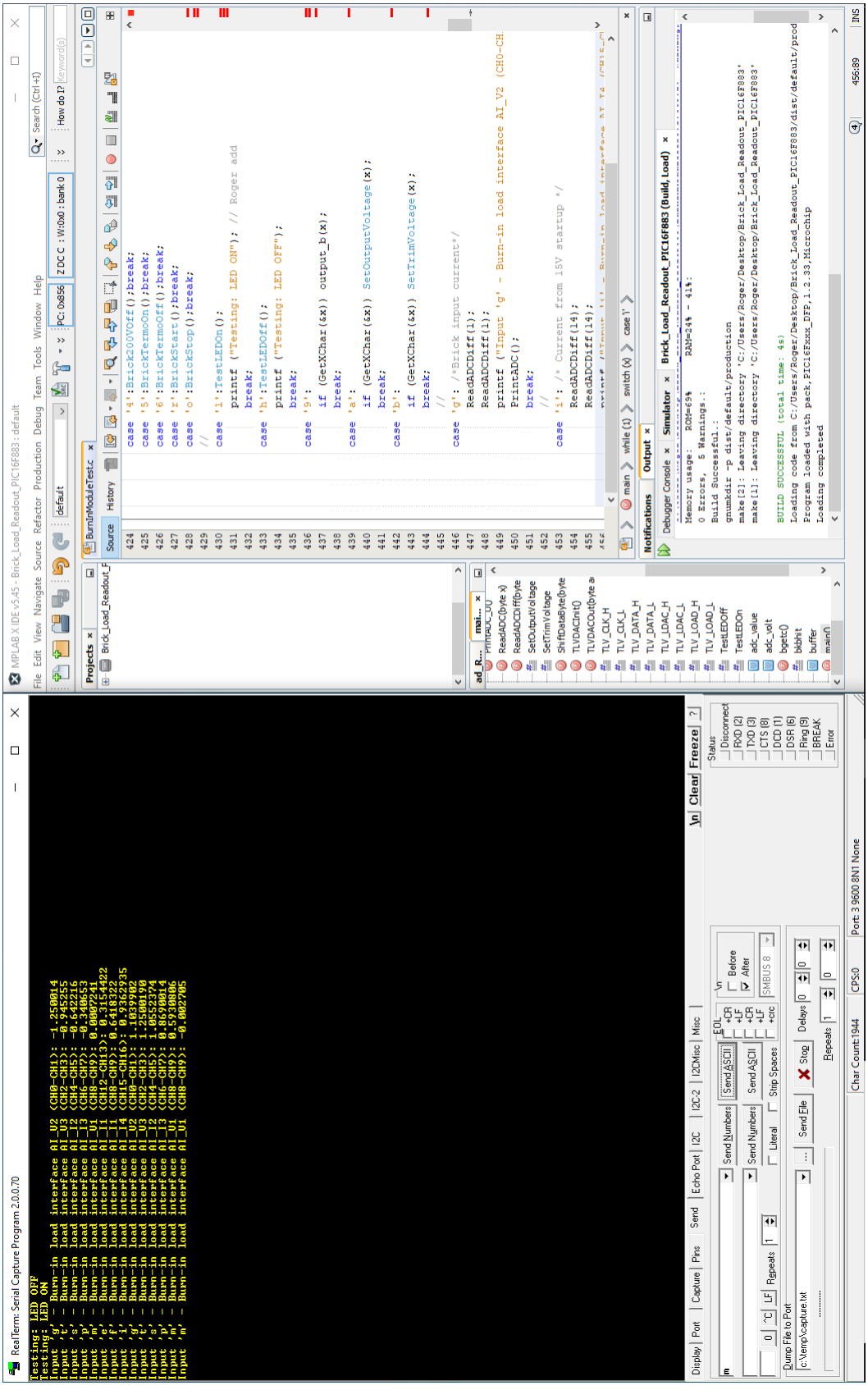

Figure B.11: Serial PIC firmware development.

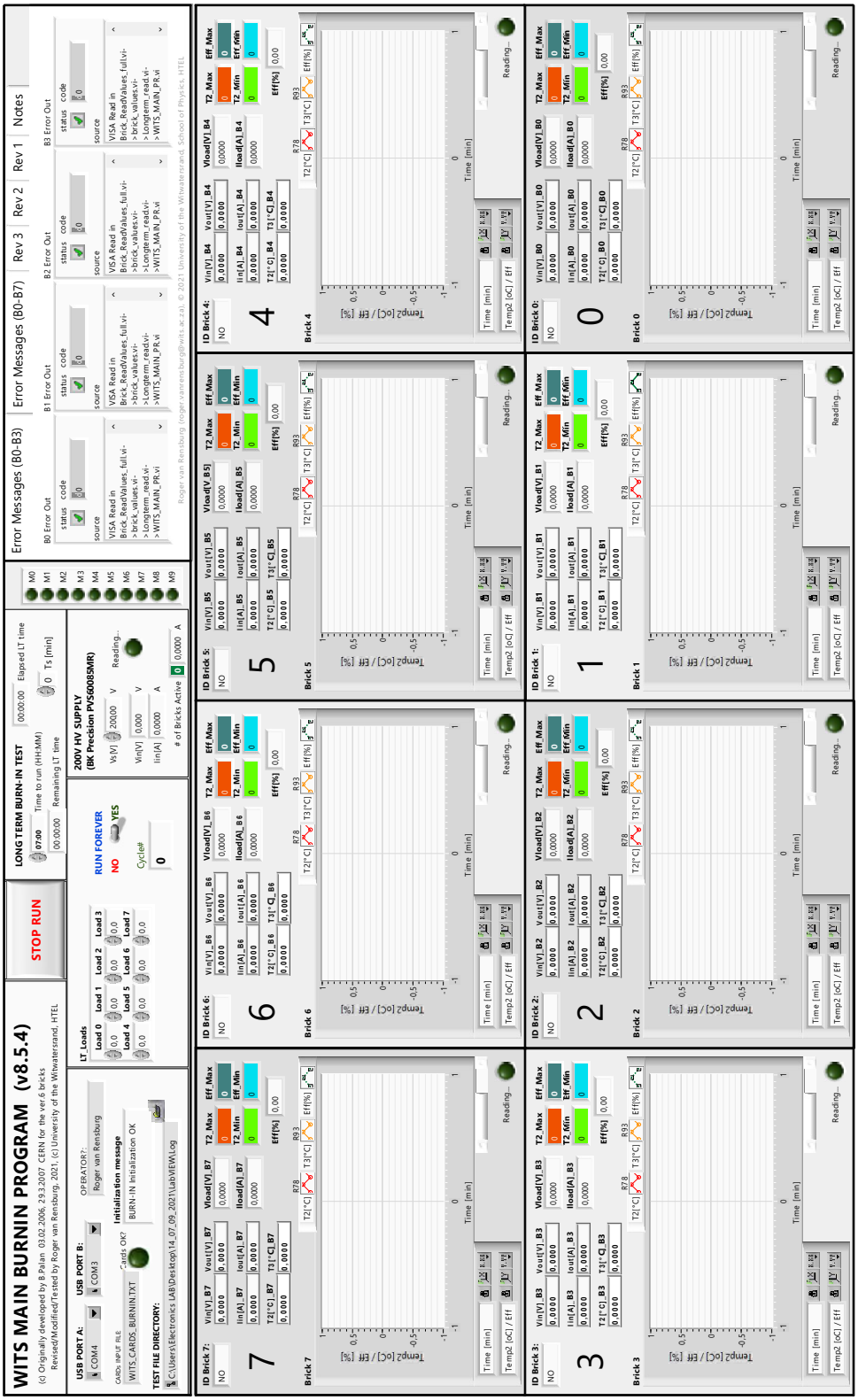

Figure B.12: BLA front panel.

Appendix C

Radiation Set up and Results

The irradiated test boards shown on Figures C.1 and C.2 were set up at the proton radiation facility. This included the Mosfet driver chips and Mosfets that were validated and can be used for the latest LVPS Brick. Additional radiation test results are shown for some of the isolation amplifier chips that had huge fluctuations during Single Event Effects testing and can be seen on Figures C.3, C.4 and C.5.

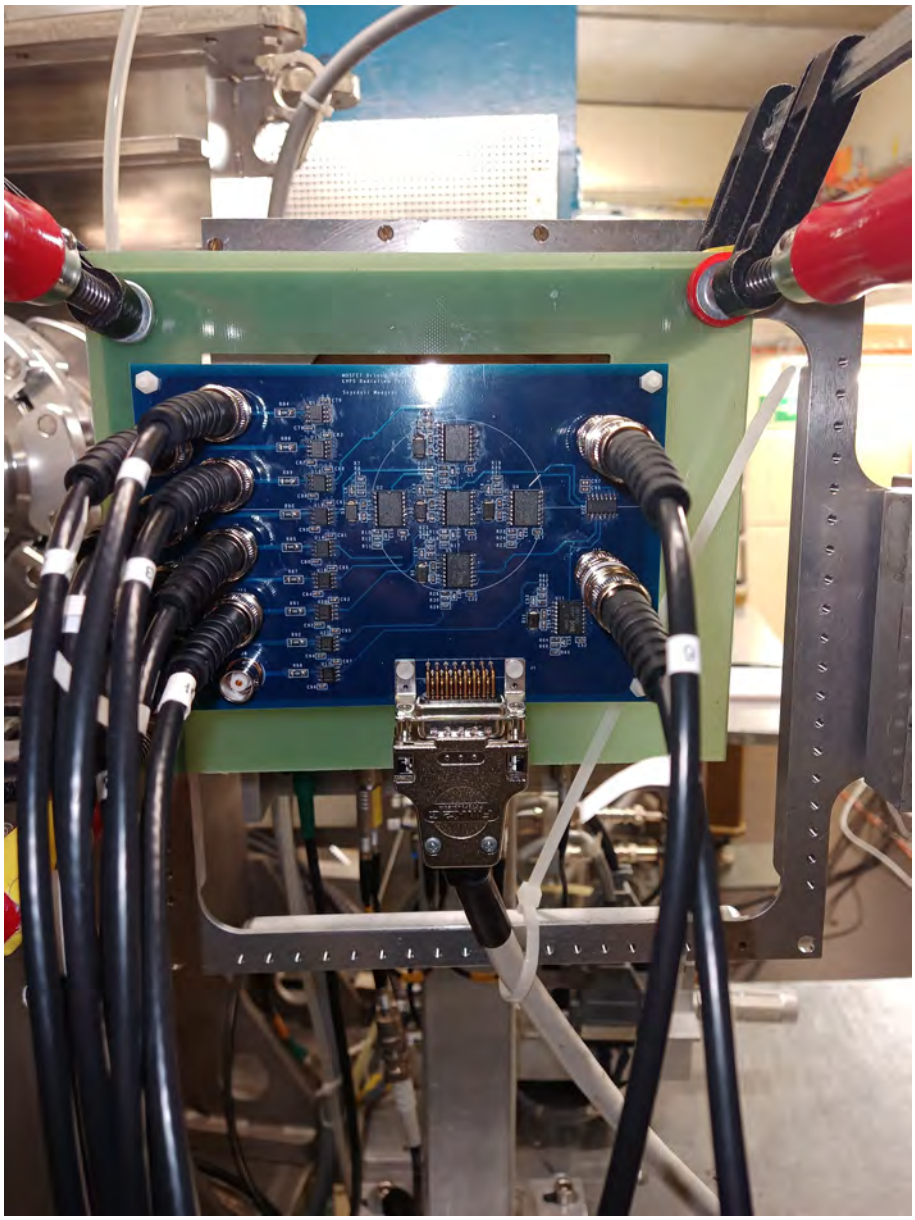

Figure C.1: MOSFET driver 1 Board.

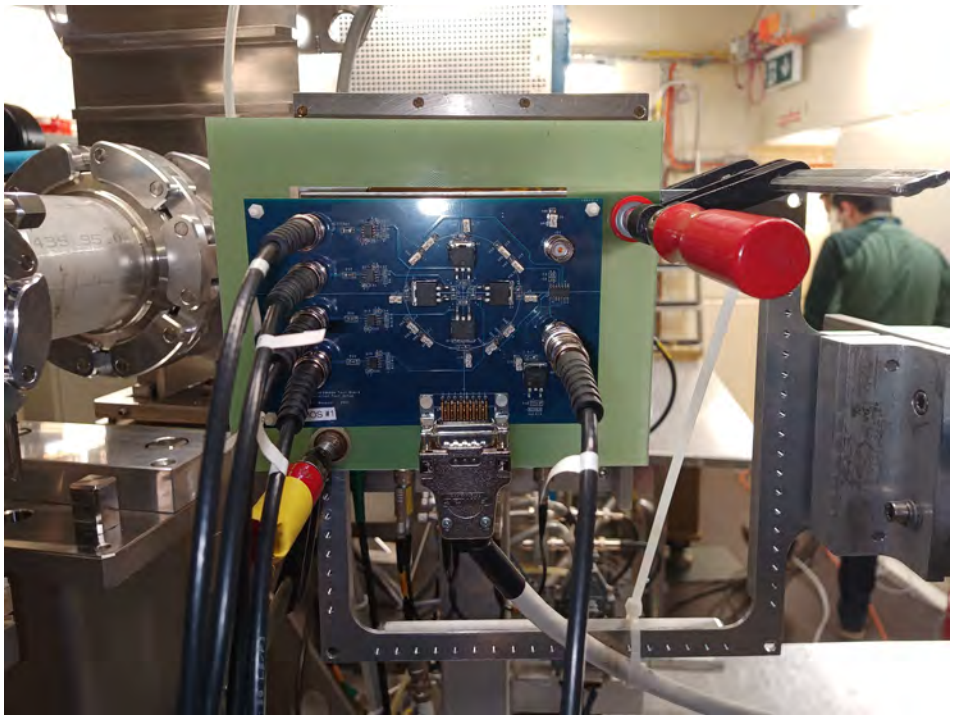

Figure C.2: MOSFET 1 Board.

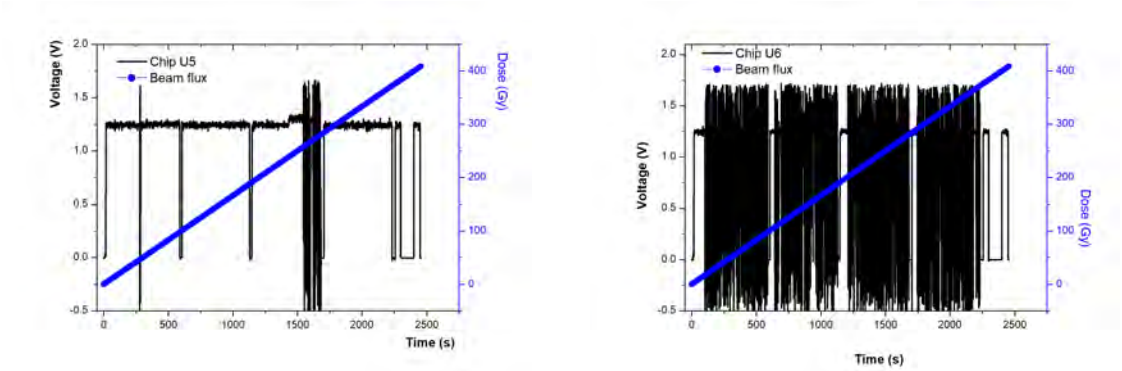

Figure C.3: Irradiated Chip U5 and U6 performance. The results from Chip U5 show that the output voltage had some fluctuations during all the 3rd run, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy. The results from Chip U1 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the beginning of each run. The fluctuations did no stop when the beam was stopped at the end of each run (a power cycle was needed). Except after run 2, where the chip behaved normally after beam stopped. After the last run (receiving 400 Gy), and a power cycle, the chip started to behave properly.

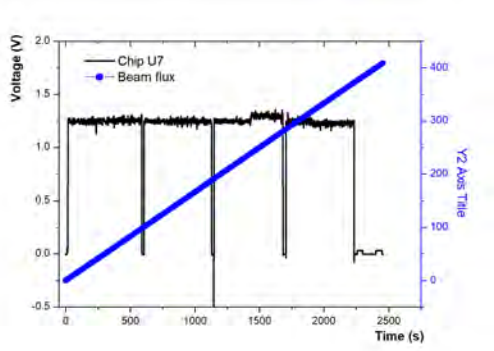

Figure C.4: The results from Chip U7 show that this chip almost behaved like the reference chip during the whole test, except for some time during the second run, where it showed huge fluctuations (went back to normal without a power cycle). The chip also survived the entire dose of 400 Gy.

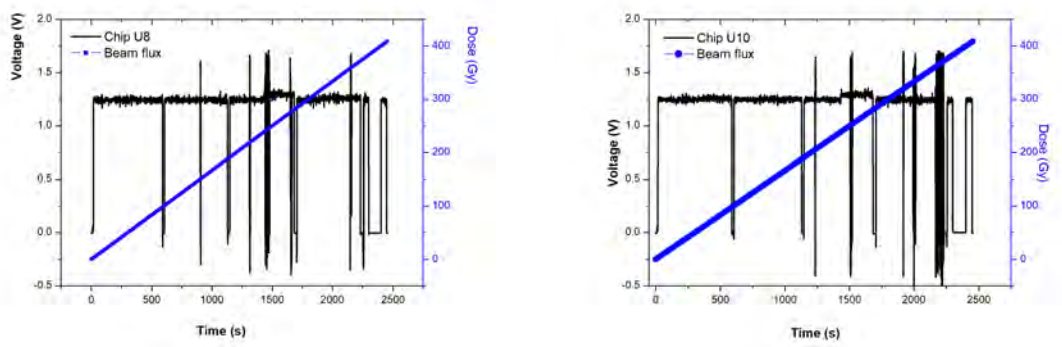

Figure C.5: The results from Chip U8 show that the output voltage had some fluctuations during all the runs, which went away without a need to power cycle. The chip also survived the test after receiving 400 Gy. The results from Chip U10 show that in all of the 4 runs, it goes to an unstable mode, where the output voltage fluctuates a lot. The fluctuations started almost at the end of the run. The chip also survived the entire dose of 400 Gy.

Appendix D

Database Development

A LabView module was provided by Prague University which helps to perform many database operations without using structured query language (SQL) programming. The idea is to create a record of the existence of a brick via LabView (see Figure D.1) or manually and then upload measurements. This will go over to the webpage link as seen on Figure D.2. The Database entries of LVPS Brick will be as follows:

1. To add new brick of 10V, Add new brick on Brick tab.
2. Enter the brick code and author of brick entry on the webpage form
3. Only basic data is required and under notes add the exact position of each brick and which LVBOX it was position in. Note the temperature, voltage output and current (RMS) metrics.
4. Compare with the UTA bricks on each of the recorded metrics.

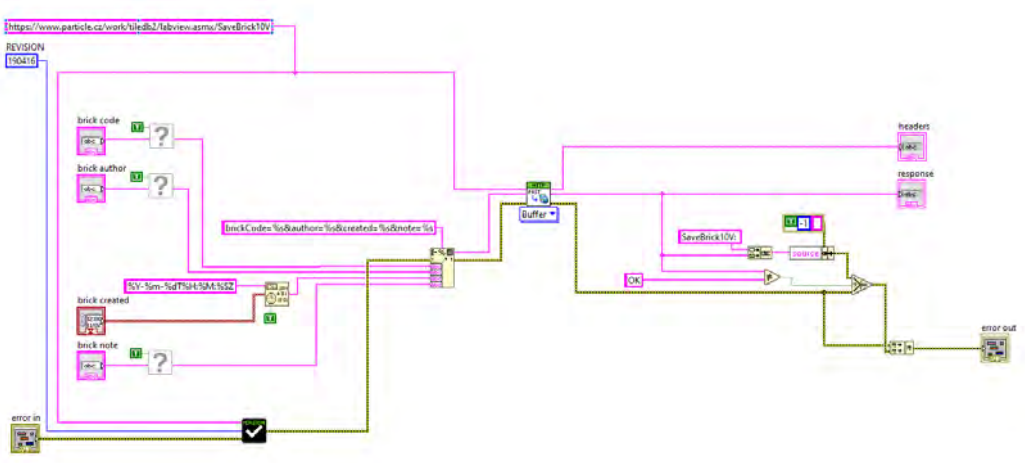

Figure D.1: Database development LabVIEW Block diagram. The LabVIEW Database Connectivity Toolset is an add-on package for accessing databases. The toolkit contains a set of high-level functions for performing the most common database tasks and advanced functions for customized tasks.

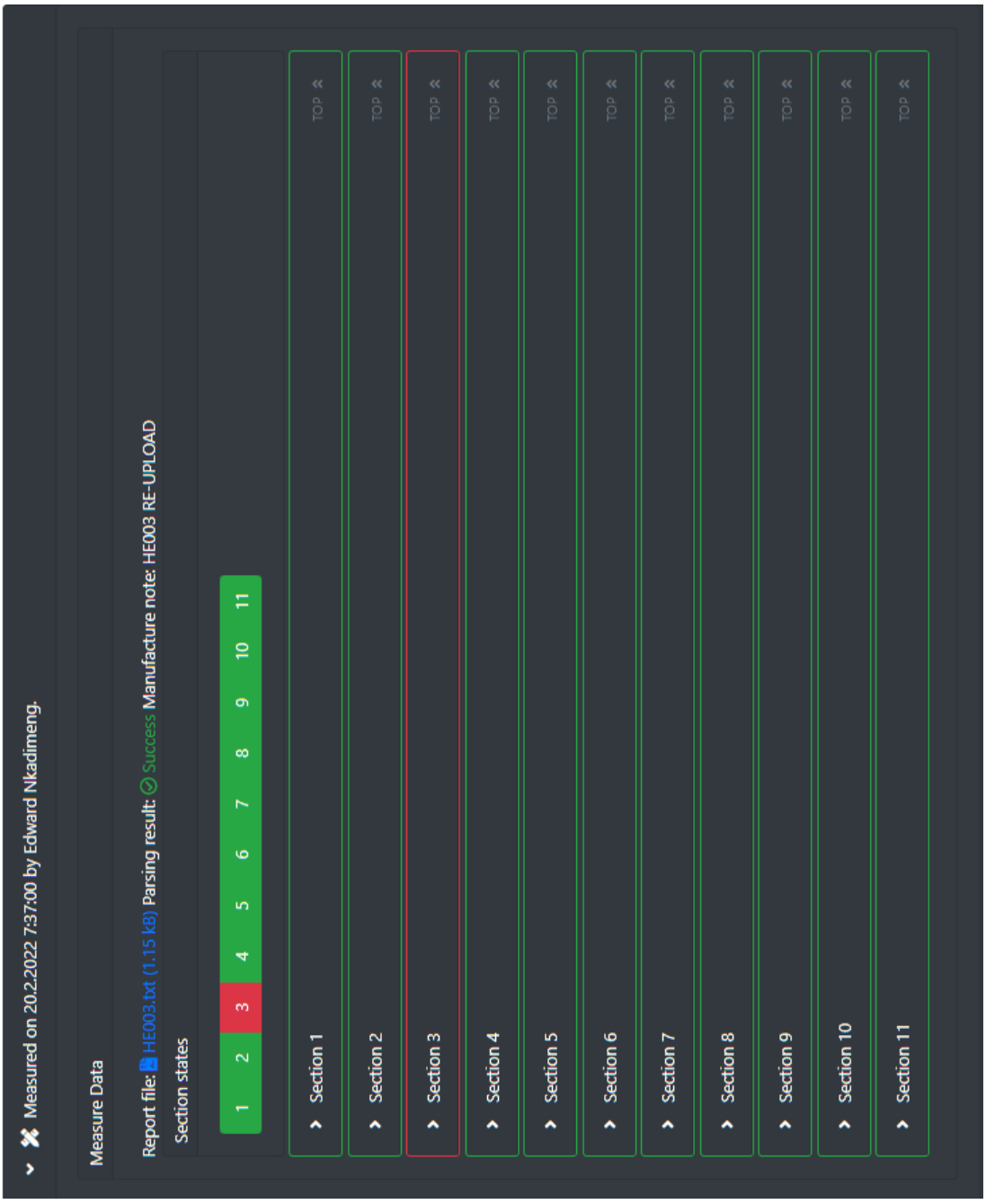

Figure D.2: Database entry of measured Brick.

Bibliography

[1] The ATLAS Collaboration. "The ATLAS Experiment at the CERN Large Hadron Collider". In: *Journal of Instrumentation* 3.08 (Aug. 2008), S08003–S08003. DOI: 10.1088/1748-0221/3/08/s08003. URL: https://doi.org/10.1088/1748-0221/3/08/s08003.

[2] S. Chatrchyan et al. "The CMS Experiment at the CERN LHC". In: *JINST* 3 (2008), S08004. DOI: 10.1088/1748-0221/3/08/S08004.

[3] E. Soldatov. *Standard Model physics at ATLAS*. Tech. rep. Geneva: CERN, Nov. 2019. DOI: 10.1051/epjconf/201922201002. URL: https://cds.cern.ch/record/2698274.

[4] M. Tanabashi and T. A. C. Hagiwara K. "Review of Particle Physics". In: *Phys. Rev. D* 98 (3 Aug. 2018), p. 030001. DOI: 10.1103/PhysRevD.98.030001. URL: https://link.aps.org/doi/10.1103/PhysRevD.98.030001.

[5] J. Thomason, R. Garoby, S. Gilardoni, L. Jenner, and J. Pasternak. "Proton driver scenarios at CERN and Rutherford Appleton Laboratory". In: *Physical Review Special Topics - Accelerators and Beams* 16 (May 2013). DOI: 10.1103/PhysRevSTAB.16.054801.

[6] S. L. Glashow. "Partial-symmetries of weak interactions". In: *Nuclear Physics* 22.4 (1961), pp. 579–588. ISSN: 0029-5582. DOI: https://doi.org/10.1016/0029-5582(61)90469-2. URL: https://www.sciencedirect.com/science/article/pii/0029558261904692.

[7] M. Tanabashi and K. Hagiwara. "Review of Particle Physics". In: *Phys. Rev. D* 98 (3 Aug. 2018), p. 030001. DOI: 10.1103/PhysRevD.98.030001. URL: https://link.aps.org/doi/10.1103/PhysRevD.98.030001.

[8] J. Thomason, R. Garoby, S. Gilardoni, L. Jenner, and J. Pasternak. "Proton driver scenarios at CERN and Rutherford Appleton Laboratory". In: *Physical Review Special Topics - Accelerators and Beams* 16 (May 2013). DOI: 10.1103/PhysRevSTAB.16.054801.

[9] G. Aad and B. Abbott. "Combined Measurement of the Higgs Boson Mass in pp Collisions at s=7 and 8 TeV with the ATLAS and CMS Experiments". In: *Physical Review Letters* 114.19 (May 2015). ISSN: 1079-7114. DOI: 10.1103/physrevlett.114.191803. URL: http://dx.doi.org/10.1103/PhysRevLett.114.191803.

[10] S. Weinberg. "A Model of Leptons". In: *Phys. Rev. Lett.* 19 (21 Nov. 1967), pp. 1264–1266. DOI: 10.1103/PhysRevLett.19.1264. URL: https://link.aps.org/doi/10.1103/PhysRevLett.19.1264.

[11] K. Aamodt, A. A. Quintana, R. Achenbach, S. Acounis, D. Adamová, C. Adler, M. Aggarwal, F. Agnese, G. A. Rinella, Z. Ahammed, et al. "The Alice Experiment at the CERN LHC". In: *Journal of Instrumentation* 3 (Aug. 2008), S08002. DOI: 10.1088/1748-0221/3/08/S08002.

[12] ATLAS Collaboration. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1–29. ISSN: 0370-2693. DOI: https://doi.org/10.1016/j.physletb.2012.08.020. URL: https://www.sciencedirect.com/science/article/pii/S037026931200857X.

[13] S. C. et al. "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 30–61. ISSN: 0370-2693. DOI: https://doi.org/10.1016/j.physletb.2012.08.021. URL: https://www.sciencedirect.com/science/article/pii/S0370269312008581.

[14] G. Apollinari, I. Béjar Alonso, O. Brüning, M. Lamont, and L. Rossi. "High-Luminosity Large Hadron Collider (HL-LHC) : Preliminary Design Report". In: (Dec. 2015). DOI: 10.5170/CERN-2015-005.

[15] A. A. Alves Jr, L. Andrade Filho, A. Barbosa, I. Bediaga, G. Cernicchiaro, G. Guerrer, H. Lima Jr, A. Machado, J. Magnin, F. Marujo, et al. "The LHCb detector at the LHC". In: *Journal of instrumentation* 3.08 (2008), S08005.

[16] M. Gell-Mann. "The interpretation of the new particles as displaced charge multiplets". In: *Il Nuovo Cimento (1955-1965)* 4.2 (1956), pp. 848–866.

[17] T. Nakano and K. Nishijima. "Charge Independence for V-particles". In: *Progress of Theoretical Physics* 10.5 (1953), pp. 581–582.

[18] E. Fermi. "Tentativo di una teoria dei raggi β". In: *Il Nuovo Cimento (1924-1942)* 11.1 (1934), pp. 1–19.

[19] E. Fermi. "Versuch einer Theorie der β-Strahlen. I". In: *Zeitschrift für Physik* 88.3 (1934), pp. 161–177.

[20] P. W. Higgs. "Broken symmetries and the masses of gauge bosons". In: *Physical Review Letters* 13.16 (1964), p. 508.

[21] P. W. Higgs. "Spontaneous symmetry breakdown without massless bosons". In: *Physical review* 145.4 (1966), p. 1156.

[22] F. Englert and R. Brout. "Broken symmetry and the mass of gauge vector mesons". In: *Physical review letters* 13.9 (1964), p. 321.

[23] G. S. Guralnik, C. R. Hagen, and T. W. Kibble. "Global conservation laws and massless particles". In: *Physical Review Letters* 13.20 (1964), p. 585.

[24] Y. Nambu. "Quasi-particles and gauge invariance in the theory of superconductivity". In: *Physical Review* 117.3 (1960), p. 648.

[25] J. Goldstone. "Field theories with «Superconductor» solutions". In: *Il Nuovo Cimento (1955-1965)* 19.1 (1961), pp. 154–164.

[26] L. Heelan. "Performance of the ATLAS forward calorimeter". In: *Journal of Physics: Conference Series*. Vol. 160. 1. IOP Publishing. 2009, p. 012058.

[27] L. E and P. B. "The LHC Machine". In: *Journal of Instrumentation* 3.08 (Aug. 2008), S08001–S08001. DOI: 10.1088/1748-0221/3/08/s08001. URL: https://doi.org/10.1088/1748-0221/3/08/s08001.

[28] ATLAS Collaboration. *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*. Tech. rep. Draft version for comments. Geneva: CERN, Dec. 2012. URL: https://cds.cern.ch/record/1502664.

[29] ATLAS Collaboration. *ATLAS detector and physics performance: Technical Design Report, 1*. Technical design report. ATLAS. Geneva: CERN, 1999. URL: https://cds.cern.ch/record/391176.

[30] R. P. Mckenzie. *Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC*. Tech. rep. Geneva: CERN, Sept. 2021. URL: http://cds.cern.ch/record/2781520.

[31] K. Anderson, J. Pilcher, H. Sanders, F. Tang, S. Berglund, C. Bohm, S.-O. Holmgren, K. Jon-And, G. Blanchot, and M. Cavalli-Sforza. "Front-end Electronics for the ATLAS Tile Calorimeter". In: Sept. 1998.

[32] T. Kawamoto, S. Vlachos, L. Pontecorvo, J. Dubbert, G. Mikenberg, P. Iengo, C. Dallapiccola, C. Amelung, L. Levinson, R. Richter, and D. Lellouch. *New Small Wheel Technical Design Report*. Tech. rep. ATLAS New Small Wheel Technical Design Report. June 2013. URL: https://cds.cern.ch/record/1552862.

[33] S. Palestini. "The muon spectrometer of the ATLAS experiment". In: *Nuclear Physics B-Proceedings Supplements* 125 (2003), pp. 337–345.

[34] K. Einsweiler and L. Pontecorvo. *Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter*. Tech. rep. Geneva: CERN, Sept. 2017. URL: https://cds.cern.ch/record/2285583.

[35] E. K. Nkadimeng. *Performance of the Tile Calorimeter Demonstrator system for the ATLAS Phase-II Upgrade*. Tech. rep. Geneva: CERN, Oct. 2021. URL: http://cds.cern.ch/record/2783051.

[36] G. Aad, B. Abbott, J. Abdallah, A. Abdelalim, A. Abdesselam, B. Abi, M. Abolins, H. Abramowicz, H. Abreu, B. Acharya, et al. "Readiness of the ATLAS liquid argon calorimeter for LHC collisions". In: *The European Physical Journal C* 70.3 (2010), pp. 723–753.

[37] V. Gonzalez, E. Sanchis, J. Soret, J. Torres, J. Castelo, V. Castillo, C. Cuenca, A. Ferrer, E. Fullana, E. Higón, et al. "Development of the optical multiplexer board prototype for data acquisition in the TileCal system". In: *IEEE Transactions on Nuclear Science* 53.4 (2006), pp. 2131–2138.

[38] A. Gomes. "The new front-end electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade". In: *Journal of Instrumentation* 11.02 (2016), p. C02015.

[39] J. Klereborn, S. Berglund, C. Bohm, K. Jon-And, M. Ramstedt, B. Selldén, J. Sjölin, A. Kerek, L.-O. Norlin, D. Novak, A. Fenyvesi, and J. (J. i. H. Molnar. "Functional irradiation tests of the Atlas TileCal Digitizer using FPGA testbenches". In: (Mar. 2022).

[40] F. Tang, K. Anderson, G. Drake, J.-F. Genat, M. Oreglia, J. Pilcher, and L. Price. "Design of the Front-End Readout Electronics for ATLAS Tile Calorimeter at the sLHC". In: *IEEE Transactions on Nuclear Science* 60 (May 2010). DOI: 10.1109/RTC.2010.5750382.

[41] F. Carrio. "Upgrade for the ATLAS tile calorimeter readout electronics at the high luminosity LHC". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 718 (2013), pp. 69–71.

[42] S. Moayedi. *Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC*. Tech. rep. Geneva: CERN, Nov. 2020. DOI: 10.22323/1.390.0860. URL: https://cds.cern.ch/record/2744389.

[43] C. Clement. "Upgrade of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC". In: *Physics of Atomic Nuclei* 84.3 (2021), pp. 368–372.

[44] E. Valdes Santurio. "Upgrade of Tile Calorimeter of the ATLAS Detector for the High Luminosity LHC." In: *Journal of Physics: Conference Series* 928 (Nov. 2017), p. 012024. DOI: 10.1088/1742-6596/928/1/012024.

[45] F. Carrió, P. Moreno, and A. Valero. "Performance of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade". In: *Journal of Instrumentation* 11 (Mar. 2016), pp. C03047–C03047. DOI: 10.1088/1748-0221/11/03/C03047.

[46] F. Vazeille. "Performance of a remote High Voltage power supply for the Phase II upgrade of the ATLAS Tile Calorimeter". In: *Journal of Instrumentation* 11 (Feb. 2016), pp. C02050–C02050. DOI: 10.1088/1748-0221/11/02/C02050.

[47] M. N. Agaras. "The ATLAS Tile Calorimeter performance and its upgrade towards the High-Luminosity LHC". In: *arXiv preprint arXiv:2105.09099* (2021).

[48] F. Tang, H. Åkerstedt, K. Anderson, C. Bohm, K. Hildebrand, S. Muschter, and M. Oreglia. "Design of Main Board for ATLAS TileCal Demonstrator". In: (May 2014). DOI: 10.13140/2.1.1475.1685.

[49] J. Abdallah. "Study of energy response and resolution of the ATLAS Tile Calorimeter to hadrons of energies from 16 to 30 GeV". In: *The European Physical Journal C* 81.6 (June 2021). ISSN: 1434-6052. DOI: 10.1140/epjc/s10052-021-09292-5. URL: http://dx.doi.org/10.1140/epjc/s10052-021-09292-5.

[50] M. G. D. Gololo, F. C. Argos, F. Martins, and B. Garcia. "Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter". In: 1690.1 (2020), p. 012054.

[51] T. Zakareishvili. *Studies of the ATLAS hadronic Calorimeter response to different particles at Test Beams*. Tech. rep. 6th Beam Telescopes and Test Beams Workshop starting date - 16.01.2018. Geneva: CERN, Jan. 2018. URL: https://cds.cern.ch/record/2299394.

[52] G. Schlager. "The Energy Response of the ATLAS Calorimeter System". Presented on 04 Dec 2006. 2006. URL: http://cds.cern.ch/record/998248.

[53] G. Aad et al. "Readiness of the ATLAS Tile Calorimeter for LHC collisions". In: *Eur. Phys. J. C* 70 (2010), pp. 1193–1236. DOI: 10.1140/epjc/s10052-010-1508-y. arXiv: 1007.5423 [physics.ins-det].

[54] G. Drake. "Design of a new switching power supply for the ATLAS TileCAL front-end electronics". In: *Journal of Instrumentation* 8.02 (Feb. 2013), pp. C02032–C02032. DOI: 10.1088/1748-0221/8/02/c02032. URL: https://doi.org/10.1088/1748-0221/8/02/c02032.

[55] M. G. D. Gololo, F. C. Argos, F. Martins, and B. Garcia. "Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter". In: 1690.1 (2020), p. 012054.

[56] I. Hruska, B. Palan, F. Calheiros, S. Némécek, Z. Kotek, J. Palacky, J. Price, M. Lokajícek, A. Tikhonov, and A. Solin. "Radiation-Tolerant Custom Made Low Voltage Power Supply System for ATLAS/TileCal Detector". In: (2007). DOI: 10.5170/CERN-2007-007.369. URL: https://cds.cern.ch/record/1091490.

[57] G. Drake, T. Cundiff, P. De Lurgio, A. Henriques, I. Minashvili, S. Nemecek, L. Price, J. Proudfoot, and R. Stanek. "An Upgraded Front-End Switching Power Supply Design for the ATLAS TileCAL Detector of the LHC". In: (2011). Ed. by D. Townsend, pp. 779–786. DOI: 10.1109/NSSMIC.2011.6154297.

[58] *LT1681, Dual Transistor Synchronous Forward Controller*. LT1681. Datasheet. Linear Technology. 2017. URL: www.analog.com/media/en/technical-documentation/data-sheets/1681f.pdf.

[59] E. K. Nkadimeng. "Reliability testing of a Low Voltage Power Supply(LVPS) and test station design for the Front-End Electronics of the ATLAS Tile Calorimeter". In: (May 2020). URL: https://cds.cern.ch/record/2719376.

[60] E. K. Nkadimeng. "A new test-bench design and performance testing of a Low Voltage Power Supply for the ATLAS Tile Calorimeter front-end electronics". In: (Oct. 2020). URL: https://cds.cern.ch/record/2741305.

[61] M. Hibbard, S. Moayedi, H. Hadavand, and A. Davoudi. "ATLAS TileCal low voltage power supply upgrade hardware and testing". In: *Nucl. Instrum. Methods Phys. Res., A* 936 (2019), 112–114. 3 p. DOI: 10.1016/j.nima.2018.10.198. URL: https://cds.cern.ch/record/2717572.

[62] E. A. Brewer, C. N. Dellarocas, A. Colbrook, and W. E. Weihl. "Proteus: A high-performance parallel-architecture simulator". In: *Acm Sigmetrics Performance Evaluation Review* 20.1 (1992), pp. 247–248.

[63] E. Beville and J. Yin. "LTM4600 DC/DC μModule® Regulator Thermal Performance". In: (2006).

[64] R. Bitter, T. Mohiuddin, and M. Nawrocki. *LabVIEW: Advanced programming techniques*. Crc Press, 2006.

[65] *SCB-68 and SCB-68A : DAQ Multifunction I/O Accessory*. SCB-68 and SCB-68A. NI SCB-68A User Manual. National Instruments. 2021. URL: https://www.ni.com/pdf/manuals/375865a.pdf.

[66] *PCI-e 6321 Data Acquisition: 16-Bit, 250 kS/s, 16 AI, 24 DIO, 2 AO*. NI 6221. User Guide. National Instruments. 2021. URL: https://www.ni.com/documentation/en/multifunction-io-device/latest/specs-pcie-6321/specs/.

[67] A. C. Radu, G. L. Miotto, and L. Magnoni. "The electronic logbook for the information storage of ATLAS experiment at LHC (ELisA)". In: *Journal of Physics: Conference Series*. Vol. 396. 1. IOP Publishing. 2012, p. 012014.

[68] M. J. Hibbard. "Accelerated Aging of a switching power supply prototype". PhD thesis. 2018.

[69] G.-A. Klutke, P. C. Kiessler, and M. A. Wortman. "A critical look at the bathtub curve". In: *IEEE Transactions on reliability* 52.1 (2003), pp. 125–129.

[70] L. Frenzel. *Handbook of serial communications interfaces: a comprehensive compendium of serial digital input/output (I/O) standards*. Newnes, 2015.

[71] R. P. Mckenzie. *The Burn-in testing of advanced custom low-voltage power supply components within ATLAS TileCAL testing facilities.* Tech. rep. ATL-COM-TILECAL-2020-047, 2020.

[72] Module Plus. "FTDI Chip". In: (2014). Datasheet. URL: https://ftdichip.com/wp-content/uploads/2020/08/DS_UM232R.pdf.

[73] M. Verle. "PIC microcontrollers-programming in C". In: *Mikro Elektronika, st edition* (1998).

[74] M. Siegesmund. *Embedded C programming: Techniques and applications of C and PIC McUs*. Newnes, 2014.

[75] M. P. Bates. *Programming 8-bit PIC microcontrollers in C: with interactive hardware simulation*. Newnes, 2008.

[76] C. Leroy and P. G. Rancoita. *Principles of radiation interaction in matter and detection*. World Scientific, 2011.

[77] E. B. Podgoršak. "Interaction of Photons with Matter". In: *Compendium to Radiation Physics for Medical Physicists*. Springer, 2014, pp. 387–514.

[78] A. Mozumder. "Interaction of fast charged particles with matter". In: *Charged particle and photon interactions with matter*. CRC Press, 2003, pp. 20–40.

[79] J. Durup and R. Platzman. "Role of the Auger effect in the displacement of atoms in solids by ionizing radiation". In: *Discussions of the Faraday Society* 31 (1961), pp. 156–166.

[80] J. Dunning, G. Pegram, G. Fink, and D. Mitchell. "Interaction of neutrons with matter". In: *Physical Review* 48.3 (1935), p. 265.

[81] Z. Dejan. "Study of radiation damage in silicon detectors for high luminosity experiments at LHC". In: (Feb. 2022).

[82] P. Sempere Roldan. "Quality control and preparation of the PWO crystals for the electromagnetic calorimeter of CMS". PhD thesis. Santiago de Compostela U., 2011.

[83] R. Maurer, M. Fraeman, M. Martin, and D. Roth. "Harsh Environments: Space Radiation Environment, Effects, and Mitigation". In: 28 (Jan. 2008).

[84] J. Stacy and W. Vestrand. "Gamma-Ray Astronomy". In: *Encyclopedia of Physical Science and Technology (Third Edition)*. Ed. by R. A. Meyers. Third Edition. New York: Academic Press, 2003, pp. 397–432. ISBN: 978-0-12-227410-7. DOI: https://doi.org/10.1016/B0-12-227410-5/00274-X. URL: https://www.sciencedirect.com/science/article/pii/B012227410500274X.

[85] P. Farthouat and H. Williams. "ATLAS policy on radiation tolerant electronics". In: (Nov. 1997).

[86] V. Radulovic, M. Stepisnik, T. Kaiba, D. Kavsek, V. Cindro, M. Mikuz, and L. Snoj. "Large Object Irradiation Facility In The Tangential Channel Of The JSI TRIGA Reactor". In: (May 2017). URL: https://cds.cern.ch/record/2284353.