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WITWATERSRAND,
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ATLAS Tile Calorimeter Online Software Reorganization and Phase-II test-beam campaigns

by

Dingane Reward Hlaluku

A thesis presented in fulfillment of the requirements for the degree of:

Master of Science in Physics

Supervised by

Prof. Bruce Mellado

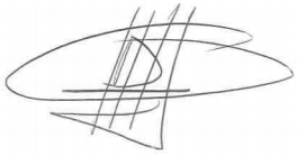
Dr. Xifeng Ruan

School of Physics

2017

Declaration

I declare that this Thesis is a result of my own work, except where explicit reference is made to the work of others. It is being submitted for the Degree of Master of Science at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any qualification or examination at any other University.



Dingane Reward Hlaluku, **6th of November 2017 in Johannesburg.**

Abstract

Tile Online software is a set of Trigger and Data Acquisition (TDAQ) required for the operation of Tile. It is built on top of ATLAS TDAQ software following ATLAS management tools and policies. The TDAQ software has been migrated from CMT to CMake, and from SVN to Git, in favor of modern software development tools and procedures. Since Tile Online software follows ATLAS TDAQ, there was a need of reorganization, simplification and clean-up of Tile Online software packages. Tile Online software packages have been migrated and reorganized to the newest ATLAS TDAQ release and the outcome is now used at Point-1 with success.

The diagnostic and verification system (DVS) is part of the ATLAS TDAQ online software packages used for configuring and executing tests for TDAQ components, and for advising recovery actions to the TDAQ operator/user. A wrapper way to start complex Tile DVS tests that required two separate programs to run on separate computers has been implemented and tests can now be run from a graphical user interface with detailed presentation of the results by non-experts.

The upgrade of the Large Hadron Collider (LHC) to the High-Luminosity LHC will provide significant opportunities to explore new physics beyond the Standard Model. This however presents significant challenges to the detector and the TDAQ systems. The Tile Calorimeter will undergo upgrades whereby the current readout electronics will be completely redesigned and replaced in phase-II to cope with the increased luminosity imposed by the HL-LHC.

Acknowledgements

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willing to help whenever I hit a brick-wall.

On a personal capacity, I would like to sincerely thank and acknowledge my family and friends for their motivations and support ever since I came to CERN in May 2016. A special dedication goes out to my grandfather who passed away while I was writing chapter 3 of this document, it was very sad that I was unable to attend his funeral. May his soul rest in peace.

No amount of words could ever be enough to express how grateful I am to Bruce Mellado for granting me this opportunity without any prejudice, for this I would like to sincerely acknowledge him. I would also like to thank Carlos Solans for teaching me how to write Object-Oriented computer programs and for his assistance with the Tile Online software every time I encountered problems that I did not even know how to begin solving.

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Nomenclature

ADC	Analogue to Digital Converter.
AFS	Andrew File System.
ALICE	A Large Ion Collider Experiment.
AM	Access Manager.
AMC	Advanced Mezzanine Card.
API	Application Programming Interface.
ASIC	Application Specific Integrated Circuit.
ATCA	AdvancedTCA or Advanced Telecommunications Computing Architecture.
ATLAS	A Toroidal LHC AparatuS.
BCID	Bunch Crossing IDentifier.
BE	Back-End
CERN	Centre Europeen pour la Recherche Nucleaire.
CIS	Charge Injection System.
CMS	Compact Muon Solenoid
CMT	Configuration Management Tool.
CPU	Central Processing Unit.
CTP	Central Trigger Processor.
COOL	LCG Conditions Database Project.
CRC	Cyclic Redundancy Check.
DAC	Digital to Analog Converter.
DAL	Data Access Library.
DAQ	Data AcQuisition.

DB	Daughter Board.
DCS	Detector Control System.
DDC	DCS DAQ Communication.
DMU	Data Management Unit.
DVS	Detector Verification System.
DSP	Digital Signal Processor.
DQ	Data Quality.
DQL	DQ Leader.
DQV	DQ Validator.
EB	Event Builder.
EBA	Extended Barrel A side.
EBC	Extended Barrel C side.
EF	Event Filter.
EM	Electromagnetic.
ERS	Error Reporting System.
ESD	Event Summary Data.
FATALIC	Front-End ATLAS Tile Circuit.
FE	Front-End.
FEB	Front End Board.
FELIX	Front-End Link eXchange.
FPGA	Field Programmable Gate Array.
FSM	Finite State Machine.
GBT	GigaBit Transceiver.
HG	High Gain.
HL-LHC	High-Luminosity LHC.
HLT	High Level Trigger.
HOLA	High-Speed Optical Link.
HV	High Voltage.
HVPS	High Voltage Power Supply.

IGUI	Integrated Graphical User Interface.
IPC	Inter-Process Communication.
IS	Information Server.
L1A	Level 1 trigger Accept.
L1Calo	Level 1 Calorimeter.
L1Topo	Level 1 Topological Trigger.
LBA	Long Barrel A side.
LBC	Long Barrel C side.
LG	Low Gain.
LHC	Large Hadron Collider.
LS	Long Shutdown.
LTP	Local Trigger Processor.
LTPi	Local Trigger Processor Interface.
LVL1	Level 1 trigger.
LVL2	Level 2 trigger.
LVPS	Low Voltage Power Supply.
MB	Mother Board.
MobiDICK	Mobile Drawer Integrity ChecKing.
OC	Output Controller.
OF	Optimal Filtering.
OFC	Optimal Filtering Constants.
OH	Online Histogramming.
OKS	Object Kernel System.
OMB	Optical Mutiplexer Board.
PCI	Peripheral Component Interconnect.
PCIe	PCI express.
PMG	Process Manager.
PMT	PhotoMulTiplier.
POL	Point Off Load.

PPr	PreProcessor.
PU	Processing Unit.
QCD	Quantum ChromoDynamics.
QED	Quantum ElectroDynamics.
QIE	Charge Integrator and Encoder
QSFP	Quad Small Form-Factor Pluggable
RCD	ROD Crate DAQ.
RITMO	ROD Information for Tile MOnitoring.
RM	Resource Manager.
ROB	Read-Out Buffer.
RoI	Region of Interest.
ROS	Readout System.
SFT	Software Development for Experiments.
SLC	Scientific Linux.
SM	Standard Model.
sROD	Super Readout Driver.
SVN	Apache Subversion.
TDAQ	Trigger and Data AcQuisition.
TM	Transition Module.
TTC	Timing, Trigger and Control.
TTCex	Timing, Trigger and Control Encoder Transmitter.
TTCoc	TTC Optical Coupler.
TTCpr	TTC receiver and PMC Form Factor.
TTCvi	Timing, Trigger and Control VME Interface.
TTYPE	Trigger type.
VME	Virtual Machine Environment.
WLS	WaveLength-Shifting (WLS).

List of Resulting Publications

- Hlaluku DR. Tests with beam setup of the TileCal phase-II upgrade electronics. Journal of Physics: Conference Series. 2017;889(1):012005. Available from: http://stacks.iop.org/1742-6596/889/i=1/a=012005.

- D. Hlaluku and B. Mellado. Trigger and data acquisition systems readout architecture of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter phase-II upgrades. Submitted to Proceedings of SAIP2017, the 62nd Annual Conference of the South African Institute of Physics, July 2017; Stellenbosch, South Africa.

- H. Tlou, H. Wilkens, B. Mellado and D. Hlaluku. Stopless removal in Muon trigger system of the Tile Calorimeter in the ATLAS detector. Submitted to Proceedings of SAIP2017, the 62nd Annual Conference of the South African Institute of Physics, July 2017; Stellenbosch, South Africa.

Chapter 1

Introduction

The Large Hadron Collider (LHC) is the world's largest proton-proton accelerator and is situated at the European Laboratory for Particle Physics (CERN). It constitutes a wide variety of various experiments to probe the fundamental structure of the universe. The ATLAS (A Toroidal LHC Apparatus) experiment is one of the LHC's two large general-purpose experiments optimized for precise Standard Model (SM) [1] measurements and new physics searches [2]. The ATLAS detector is composed of several layers of distinct sub-systems that work in synergy to detect different particles. The hadronic Tile Calorimeter (TileCal) is used to detect and measure energies and directions of hadrons and jets. TileCal is an iron-scintillator sampling detector which is read-out by 9852 photomultiplier tubes (PMT). This document is largely based on the TileCal's Trigger and Data Acquisition (TDAQ) system relative to the global ATLAS TDAQ system. The main purpose of the ATLAS TDAQ is to readout, transport and store physics data originating from collisions at the LHC. It is also however used as a data acquisition system for test setups, test beams and detector calibrations due to its modularity and reconfigurability nature. The TileCal Online software is a set of TDAQ software used for the operation of TileCal. It is built up of packages using the same software build system as that of ATLAS. The ATLAS experiment heavily relies on

multi-component infrastructure to provide software for simulation, reconstruction, trigger, analysis and data acquisition, and has for many years relied on the tailor made Configuration Management Tool (CMT) for compiling software. However, the ATLAS code base has now evolved beyond CMT capabilities and has resulted in replacing CMT with CMake, in favor of modern software development tools and procedures. The TileCal Online software adapted to build with CMake and stored in Gitlab software repository, a modern distributed version control system in contrast to Apache Subversion (SVN) since ATLAS plans to stop SVN support by the end Run 3 foreseen in 2020. The migrations of TileCal Online software packages from CMT to CMake, and from SVN to Git will be discussed together with the implementation of the TileCal stand-alone Diagnostic and Verification System (DVS) tests in this document.

The second part of the thesis discusses the TileCal Phase-II upgrades. The LHC has planned a series of upgrades envisaged to reach the High Luminosity LHC (HL-LHC) that will deliver an instantaneous luminosity about 7 times larger (7 x $10^{34}\text{cm}^{-2}\text{s}^{-1}$) than the nominal Run 2 value. TileCal plans to undergo an upgrade to cope with the HL-LHC parameters by adopting a new readout architecture. In this new architecture, the back-end (BE) and front-end (FE) electronics will be completely redesigned and replaced. The PMT signals will be fully digitized and transmitted for every bunch crossing to the BE Tile PreProcessor (PPr) located off-detector. The PPr will provide an interface path data readout, control, configuration, and monitoring of the FE electronics, and will send calibrated information to the ATLAS Level 0/1 trigger for trigger event selection. The PPr will further provide preprocessed digital data to the Level 0/1 with better spatial resolution in contrast to the current analog trigger signals. A single super-drawer module commissioned with the Phase-II upgrade electronics is to be inserted into the detector to evaluate and qualify the new trigger and readout concepts in the overall ATLAS TDAQ. This new super-drawer, so-called hybrid Demonstrator,

must provide analog trigger signals in oder to be compatible with the current detector readout system. This Demonstrator module has been inserted into a TileCal module prototype to evaluate the performance in the lab. In parallel, one more module has been instrumented with two other FE electronics options which are under evaluation. The two other FE options are the Charge Integrator and Encoder (QIE), and the FE ATLAS Tile Circuit (FATALIC) which are based on custom Application Specific Integrated Circuits (ASIC). These two modules together with three other modules composed of the current system electronics were exposed to different particles and energies in four test beam campaigns during 2015, 2016 and 2017 [3]. This thesis will describe in detail the various components of the TDAQ infrastructure (software and firmware) of the upgrade specific electronics developed explicitly for the tests with particle beams, and will also discuss some preliminary results for different types of particles as well as for calibration data.

1.1 Overview

This document is arranged according to the following schema: Chapter 2 is an introduction to the LHC at CERN, followed by detailed review of the ATLAS experiment and the hadronic Tile Calorimeter. Chapter 3 describes the implementation of the TileCal Online software and stand-alone DVS tests. Chapter 4 is devoted to the detailed description of the TileCal Phase-II upgrade electronics and the study of their performances during test beam campaigns. Chapter 5 is a summary and conclusions of the entire document.

Chapter 2

The ATLAS experiment at CERN's LHC

CERN is a particle physics research facility located at the French border, in Geneva Switzerland. This facility works in synergy as a collaborative effort by scientists and engineers from all over the world to probe the fundamental structure of the universe. It operates the LHC particle accelerator which is currently the most sophisticated and advanced in the world. The LHC is a proton-proton collider with a center of mass energy of 14 TeV and an original luminosity design of 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [4]. There are four large experiments constructed around the LHC ring. These are two general-purpose experiments viz. ATLAS [5, 6] and the Compact Muon Solenoid (CMS) [7] which are optimized to study new physics at the TeV scale. After three years of operation, these two experiments in 2012 announced the discovery of a new elementary particle with mass around 125 GeV consistent with the 50 years old prediction, the SM **Higgs Boson** [8]. The other two experiments are the LHC beauty (LHCb) which is designed to study CP violation in the bottom quark sector [9], and the other one being A Large Ion Collider Experiment (ALICE) which is designed for quark-gluon plasma through heavy-ions; lead-lead and lead-proton collisions [10]. In addition to this large experiments, there are

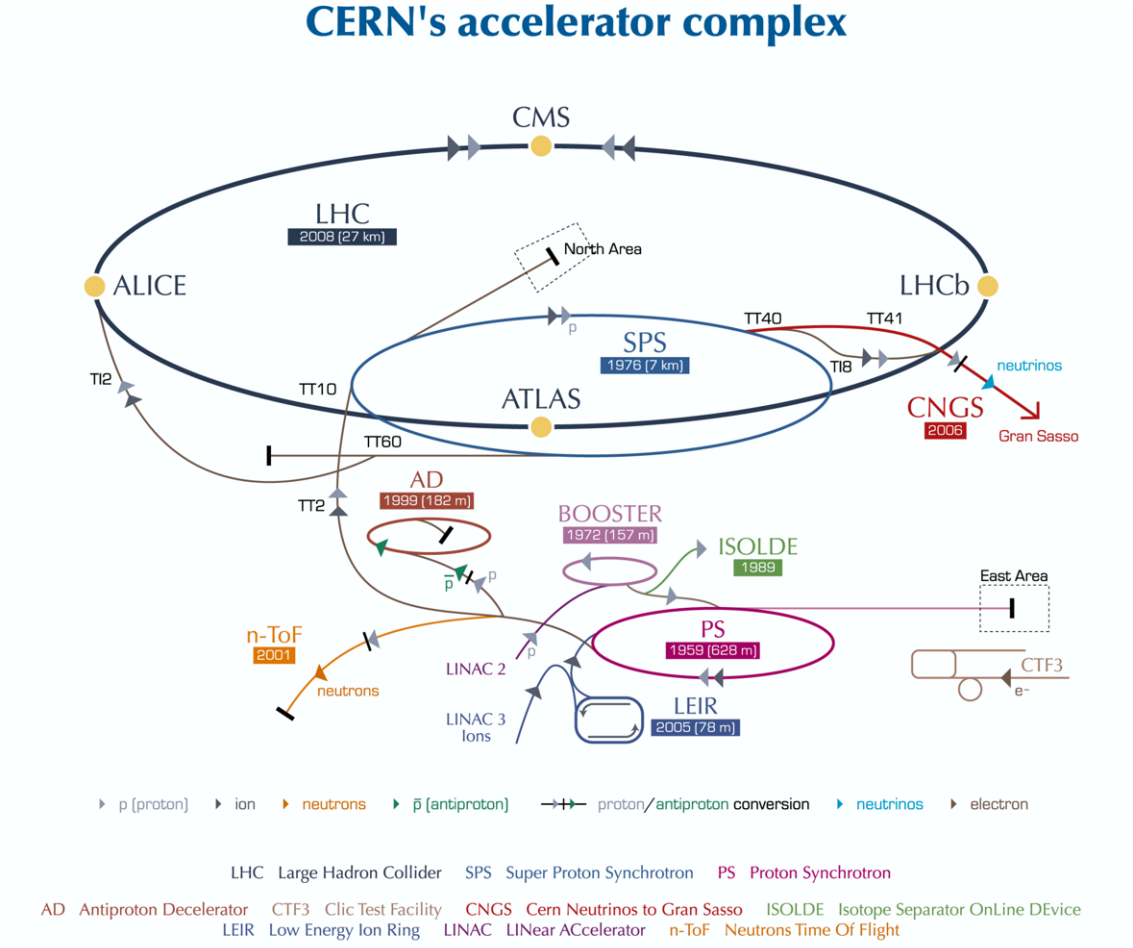


Figure 2.1: A schematic overview representation of the LHC showing the four largest experiments and all other connected experiments [12].

other experiments i.e., MoEDAL, LHCf and TOTEM which are much smaller in size (see Fig. 2.1) [11].

Inside the LHC, two high-energy particle beams travel at speeds close to that of light in opposite directions, and are made to collide at strategic locus points. New particles are created using the kinematic energy available in the collision. The number of events produced in proton-proton collisions for a given process is obtained using equation 2.1 that depends on the physics process itself and the

total integrated luminosity.

$$R = \sigma L \tag{2.1}$$

The σ represents the cross section of the process, and L is the total integrated luminosity obtained by $\int L_{inst} dt$; where L_{inst} is the instantaneous luminosity. This quantity is obtained using equation 2.2, by measuring the beam parameters during specific LHC runs called van der Meer (vdM) scans.

$$L_{inst} = \frac{1}{4\pi} \frac{N^2 f}{\sigma_x \sigma_y t} \tag{2.2}$$

N represents the number of protons per bunch, f represents the fraction of bunch positions containing protons, t is the time between bunches, and σ_x and σ_y are the transverse dimensions of the Gaussian beam profiles. All those parameters are optimized to obtain a satisfying production rate for the process of interest.

The LHC stages of operation and milestones are defined in terms of Phases, Long Shutdowns (LS) and Runs. Phase-I and Phase-II refer to the LHC machine and detector upgrades anticipated to be completed by 2021 and 2025 respectively. The terms LS1, LS2, LS3 refer to the LHC machine's long shutdown periods in 2013-14 and again anticipated for 2019, 2020 and 2024, to mid 2026, during which the detector upgrades occur. Run 1, 2 and 3 refer to ATLAS data-taking period operations before and between long shutdowns [13, 14].

In addition to proton-proton collisions, the LHC also collides heavy lead-ions. This lead ion collisions enable LHC experiments the opportunity of studying transient matter states similar to those which existed after the big bang [15]. The design instantaneous luminosity and center of mass energy for Run 2 are 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $\sqrt{s}$ = 13 TeV respectively [16]. Phase-I upgrades in 2019 will increase the luminosity to approximately 3 x 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, and finally, Phase-II

upgrades are envisaged to reach a design center of mass energy of $\sqrt{s}$ =14 TeV, and to increase the peak luminosity by up to 7 x 10^{34} $cm^{-2}s^{-1}$ in 2023 [17].

2.1 The ATLAS Experiment

The ATLAS experiment is a multi-purpose detector designed to utilize the maximum discovery prospectives of the LHC. The technique used is direct detection of mostly charged and neutral particles that result as outcomes of unstable SM particles like the Z and the $W^{\pm}$, the Higgs boson and several other particles theorized beyond the SM. This detector system is currently the most tremendous detector ever built for a particle collider with cylindrical dimensions; diameter of 25 m, 46 m wide, and weighs 7,000 tonnes [18]. This cylindrical detector covers an angle of 2.5 for the trackers and 4.9 for the calorimeters given in pseudo-rapidity (η). The η is is defined by relation 2.3, with θ being the positive angle of elevation from the axis of the beam. ϕ is the azimuthal angle covering $2/\pi$ measured from the direction pointing to the center of the LHC ring upwards.

$$\eta = -\ln(\tan(\frac{\theta}{2})) \tag{2.3}$$

The detector system is tailored as a composition of several distinct sub-detector systems at various layers (see Fig. 2.2) for different particle detection techniques. These sub-detectors are grouped into three major components that are concentrically wrapped around in layers around the collision point (see Fig. 2.3) to register the energy and trajectory of particles. The major components are the: Inner Detector, Calorimeter system and Muon spectrometer. Additionally, the detector employs a huge magnet system for bending charged particles' trajectories enabling the computation of their momenta. Integrated with the detector components are: the TDAQ system used for the selection of physics events with noteworthy attributes, and the Computing system which develops and improves

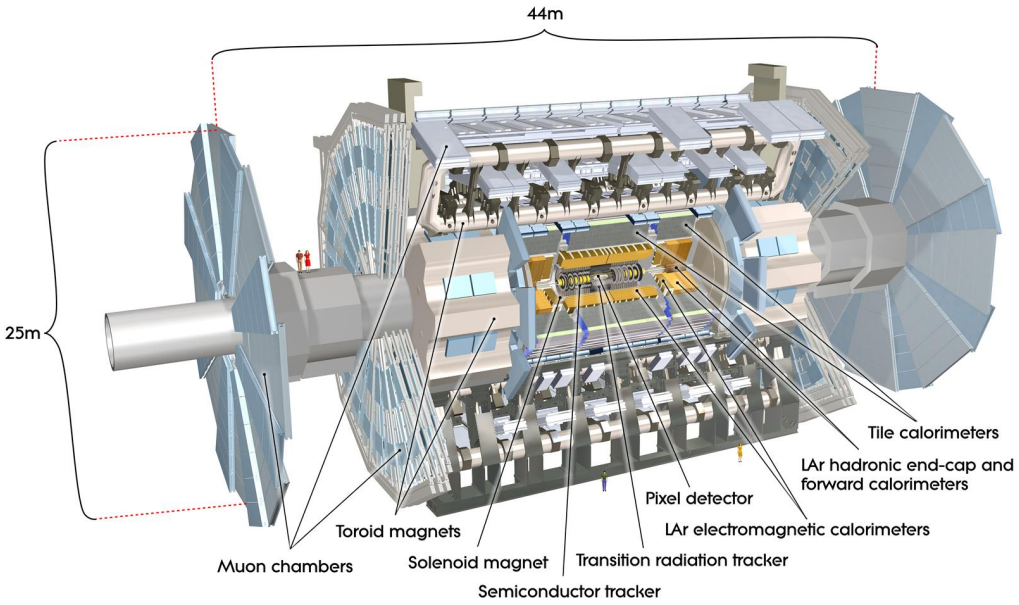


Figure 2.2: A rendering of the ATLAS experiment detector system [5].

computing software used to store, process and analyze substantial magnitudes of collision data at 130 computing centers around the world [18].

2.2 The ATLAS TDAQ Systems

The ATLAS detector has been optimized to perceive about one billion proton-proton collisions per second with a unified magnitude of data that is at least 60 million Mbps. However, only a small number of these events contain distinguishing attributes with potentials that might lead to new discoveries. A specialized multi-level computing system termed the TDAQ is employed by ATLAS to lessen the data flow to manageable levels [18]. The TDAQ system is coupled into 2 parts; the trigger (T) and the data acquisition (DAQ). This system picks events with interesting noteworthy attributes for physics analyses. The trigger system selects events at three levels of the online DAQ, viz. Level 1 (LVL1), Level 2 (LVL2) and the Event Filter (EF). Each of these levels reduce the accepted event rate. The

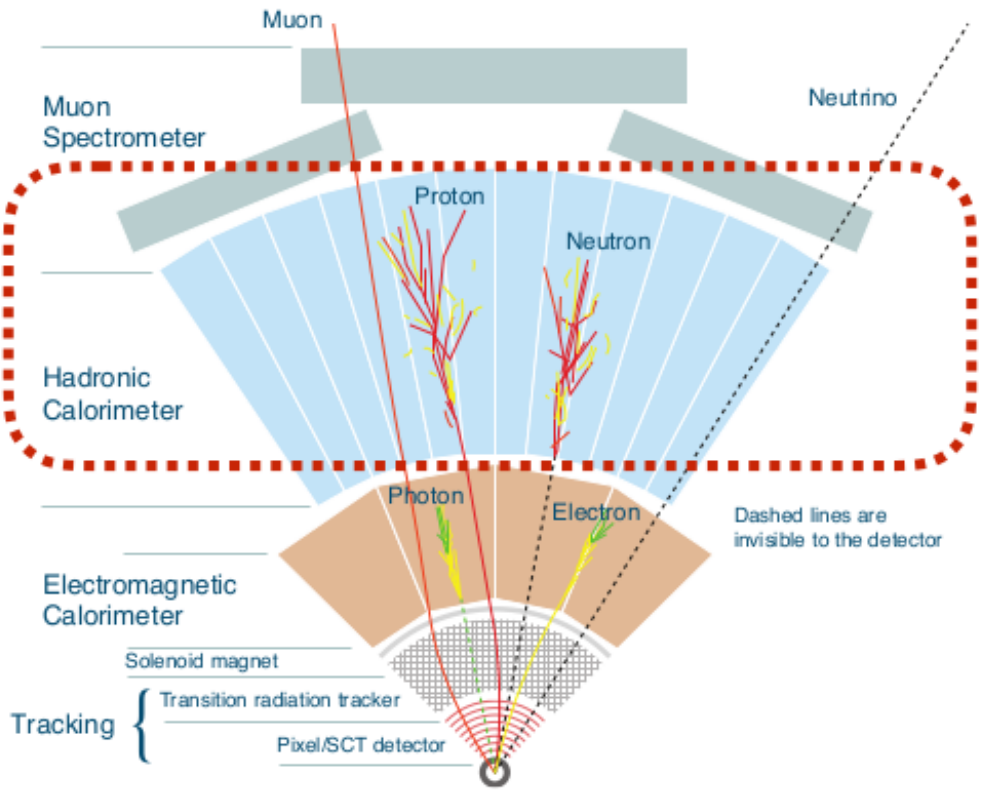


Figure 2.3: A slice representation of the ATLAS detector showing the various sub-detector layers and what particles they detect [18]

.

TDAQ system as a whole reduces the event rate from 10^9 to 10^2 Hz. The LVL1 trigger is implemented from custom-made electronics in contrast with the LVL2 and EF which are purely based on commercially off-the-shelf software and hardware. The LVL2 and the EF together form the software based High Level Trigger (HLT). A schematic representation of the TDAQ system for Run 2 is shown in Fig. 2.4. A new and improved DAQ data flow architecture has been adopted for Run 2. In this improved architecture, there is no longer a separate LVL2 and EF or a separate event building step. Everything is done on a generic HLT node. In addition to this, the DAQ also provides infrastructure for control, configuration and monitoring of the overall ATLAS data acquisition [19]. Supervision of the detector hardware components is provided by the Detector Control Systems (DCS) [20].

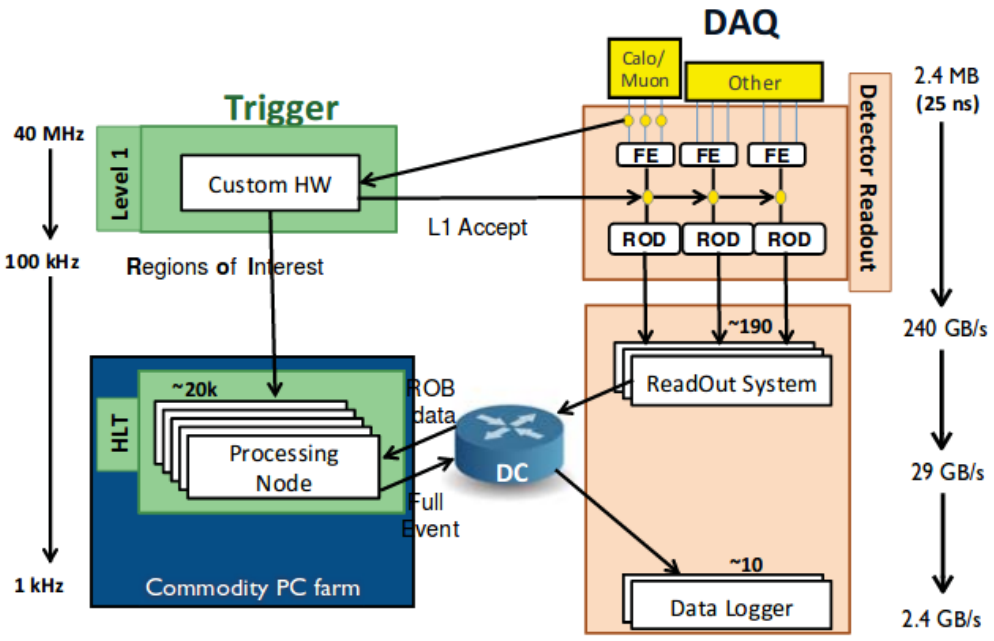


Figure 2.4: Schematic overview of the Trigger and DAQ system in Run 2 [6].

2.2.1 Level 1 Trigger

The LVL1 trigger works on a set of reconstructed quantities from the calorimeters and the muon spectrometer to define Regions-of-Interest (RoIs) as shown in Fig. 2.5. The LVL1 defines the RoIs by using reduced granularity information to search for signals from high-p_T muons, electrons/photons, jets, and τ-leptons decaying into hadrons. The calorimeter selection is based on reduced granularity and precision information from all the calorimeters gathered by the LVL1 Calorimeter (L1Calo). During Run 1, the LVL1 was only able to search for single objects (like muons and jets), or require simple unifications of such objects to be present in events. A new hardware component called the LVL1 Topological Trigger (L1Topo) has been added to the system in order to improve the functionality of the LVL1 trigger [6]. It receives information in detail about the energy and direction of the candidate objects gathered by the L1Calo and LVL1 muon triggers. This information is then further processed by specific algorithms which have been implemented in the component's FPGAs to look for signatures such as

jet like muons [21].

The Central Trigger Processor (CTP) is the core of the LVL1 trigger and implements the overall trigger selection schema for different types of objects. The trigger menu is programmable to a maximum of 256 distinguishable units with each of them classified as a unification of specific requirements on the data input. The LVL1 logical trigger decision is computed by the CTP based on information that is received from the trigger, L1Calo, L1Topo and the LVL1 muon trigger. This information is then transmitted as the LVL1 accept (L1A) signal together with the LHC timing information to all sub-detector front-end and back-end electronics by the Timing, Trigger and Control (TTC) network. The decision to keep event data is made in less than 2 μs after every event occurrence and the event is retrieved from pipelined storage buffers. The LVL1 trigger reduces the LHC 40 MHz (25 ns) bunch crossing rate to 100 kHz of L1As. The L1A trigger event is further propagated to the LVL2 with its associated geometrical RoIs for further processing [22].

2.2.2 High Level Trigger

The RoIs formed at LVL1 are received by the HLT which implements complex selection algorithms at full granularity information from the detector in either the entire event or the RoIs. The HLT lessens the event rate LVL1 output rate from 100 kHz to about 1 kHz within a 0.2 μs computational processing time on average. The LVL2 is implemented by tremendous arrays of state of the art commercially-of-the-shelf servers which analyzes in-depth the specific RoIs selected by the LVL1 for every event. The full event data is gathered into buffers in parallel. A couple of thousand events pass the LVL2 every second with their data transmitted to the EF. The trigger for the EF is implemented as a huge farm of CPUs which perform in-depth analysis of the entire full event data. On average, approximately

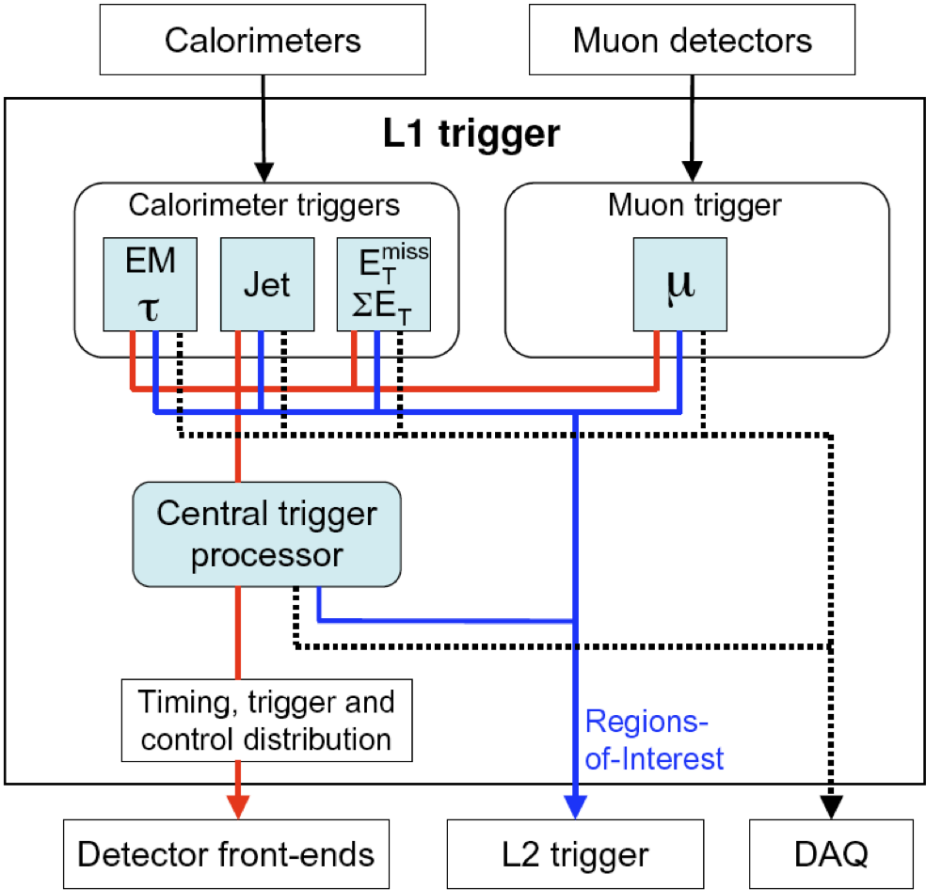


Figure 2.5: A schematic representation of the ATLAS LVL1 trigger architecture [17].

200 events every second remain after the EF processing and these are then further distributed on to CERN permanent storage system for offline data analysis.

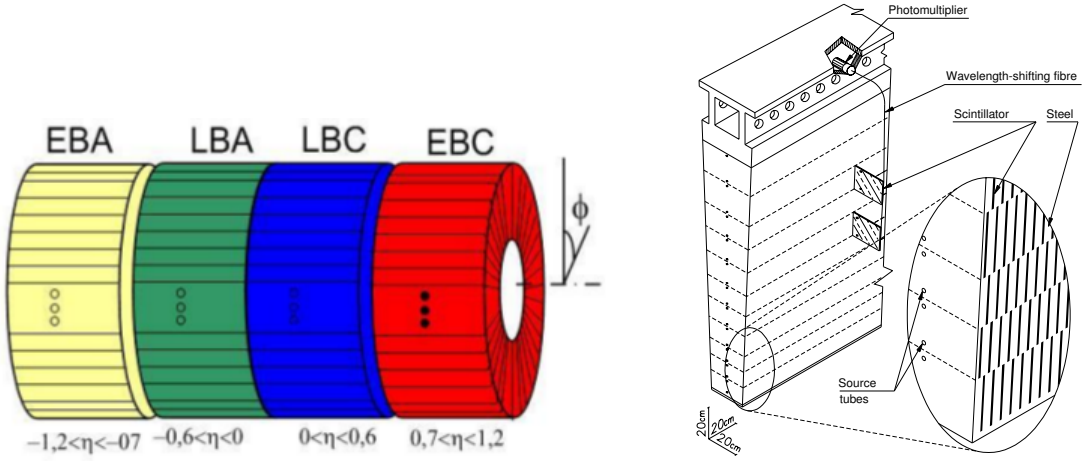
The merged HLT

During the Run 1 data-taking period, ATLAS trigger scheme was implemented such that there was separate LVL2 and EF trigger levels running on separate computing clusters/nodes. This has been modified for Run 2, the system has now been unified into one event processing farm. This allows for sharing of dynamic resources between algorithms by lessening the complexity of the HLT farm processing.

The HLT still separates the algorithms implemented by the EF and the LVL2 levels [19]. This configuration has been optimized to reduce duplication of algorithms and code which in turn results in a more versatile HLT. Almost all of the trigger reconstruction algorithms have been augmented to minimize differences between offline analysis and the HLT selections, and this has reduced inefficiencies by more than a factor of 2 for some cases like hadronic tau triggers. The HLT computational processing implemented within the RoIs have also been optimized to allow accumulation of the RoIs into one object for some triggers. The average event output rate of the HLT has been improved and upgraded to 1 kHz from 400 Hz as required by the data storage constraints [23].

2.3 The Hadronic Tile Calorimeter

TileCal is the intermediate region of the ATLAS detector's calorimeter system which covers the $|\eta| < 1.7$ region behind the electromagnetic Liquid Argon (LAr) calorimeter [24]. It is a sampling calorimeter which makes use of steel as the absorber material and plastic scintillating plates as the active medium, that are readout by wavelength shifting (WLS) fibers (see Fig. 2.6b) [25]. It is mechanically partitioned as three barrels, two extended barrels and one central barrel. And operationally, the system is split into four partitions which are labeled as LBA and LBC for the long barrel, and EBA and EBC for the extended barrel as shown in Fig. 2.6a. Each barrel is assembled out of 64 wedge-shaped modules staggered in the ϕ direction. For each module, the scintillating tiles are grouped into cells which are readout on both sides by a photomultiplier located along with the rest of the FE electronics in the so-called super-drawers axially oriented at the outermost part of the barrels. The FE electronics are powered by low-voltage power supplies (LVPS). The data from the FE electronics is transferred to the BE electronics for further processing and readout to permanent storage. The communication between the FE and BE electronics is done via redundant optical links,



(a) The TileCal detector partitions.

(b) TileCal module

Figure 2.6: The TileCal system, 4 barrels with 64 modules per barrel [6].

which are of two types: Write only which are used for the TTC, and the read only which are used for readout. Finally, TileCal is instrumented with three detector calibration systems viz. charge injection scan (CIS) system, laser system and a ^{137}Cs radioactive source. Together, these systems are used to calibrate the signals to the electromagnetic scale with a very good precision. A schematic representation of the TileCal readout electronics and detector components is shown in Fig. 2.7. This section discusses in detail the entire TileCal readout electronics which will be referenced in the phase-II upgrades sections of Chapter 4.

2.3.1 Front-End Electronics

The TileCal readout electronics are divided into the FE electronics which are those mounted on the detector, and the BE which are installed in the counting rooms of the ATLAS cavern in a low radiation environment. The FE electronics are contained in mobile drawer units located in the radius beam back region of the calorimeter. Two drawers form a super-drawer which is inside of the two sides of the Long Barrel and on one side in each of the two Extended Barrels. The main FE components are the: PMTs, mother-boards, digitizer boards and the

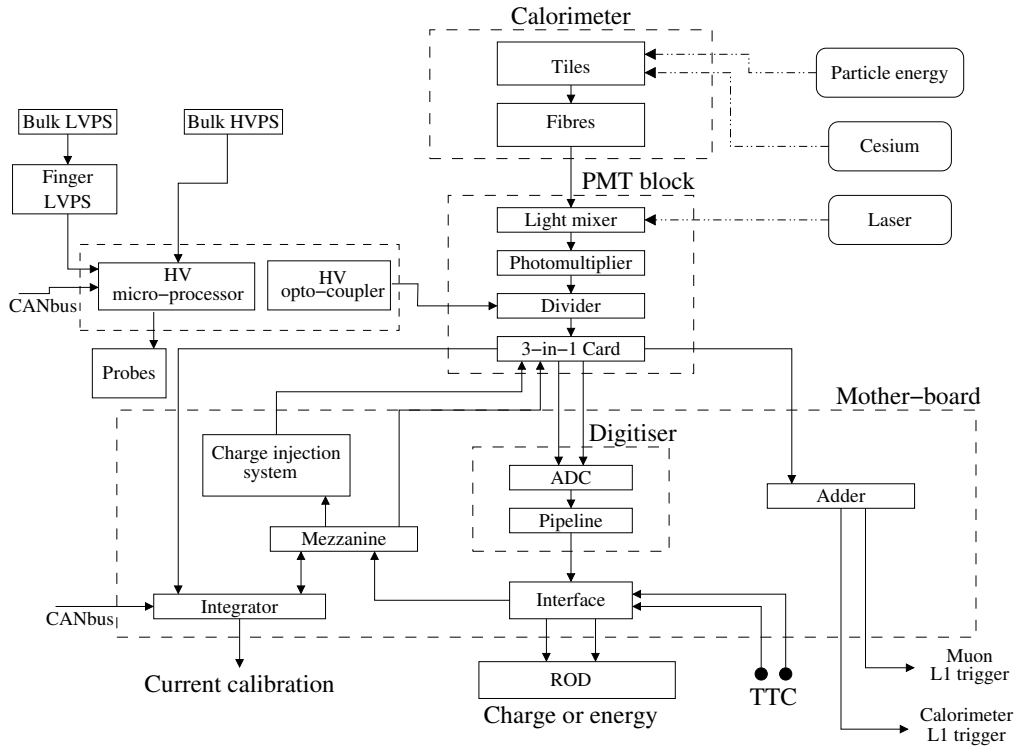


Figure 2.7: A schematic overview of the Tile Calorimeter read-out electronic components [26].

interface boards [25]. The functionally of each of these components will be briefly presented next.

Photomultiplier tube block

A particle passing through the scintillating tiles emits light that is transferred to the PMT by the WLS. The main function of the PMT block is to convert the light from the scintillating tiles into analogue signals, which are then digitized by two separate analogue-to-digital converters (ADCs) with a 1:64 gain ratio. Mechanically, it is assembled as a mu-metal shield for magnetic shielding and a steel cylinder. Its main components are: a light mixer, a PMT, a voltage divider and the 3-in-1 board, as shown in Fig. 2.8. Each drawer module of TileCal is capable of housing a maximum of 48 PMT blocks.

- **Mixer:** This device is an optical plastic insert and it's main functionality

is to mix the light from all the readout fibers ensuring consistent lighting of the photo-cathode.

- **PMT:** This device is a compact 8-dynode structure and is used to measure light from the scintillators. It is responsible for converting the light pulses from the fiber bundles into an electrical charge.

- **Divider:** PMTs require high voltage for operation. This voltage is supplied to them by external high voltage power supplies (HVPS) that deliver 800 V from the low radiation environment counting room (USA15). The divider is used to partition the high voltage between the dynodes of the PMTs. This device is a printed circuit with surface mounted components and is attached onto the 3-in-1 board.

- **3-in-1 board**: After a light pulse has been detected and amplified by the PMT, it is then transmitted through the pre-amplifier in the 3-in-1 board. The main functions of this board are to provide a high and a low gain shaped pulse for the digitizer boards, slow integrator readout signals used for monitoring and calibration, and the CIS system. This board also provides a third analog trigger signal output that is provided to the LVL1 trigger summation board.

Mother-boards

The mother-board serves as the core element that holds together all the drawer electronics as shown in Fig. 2.7 and is essentially the interface between the 3-in-1 board and the BE. It provides power and TTC commands to the 3-in-1 boards. It also hosts up to four digitizer boards and one interface board. Each super-drawer contains two mother-boards.

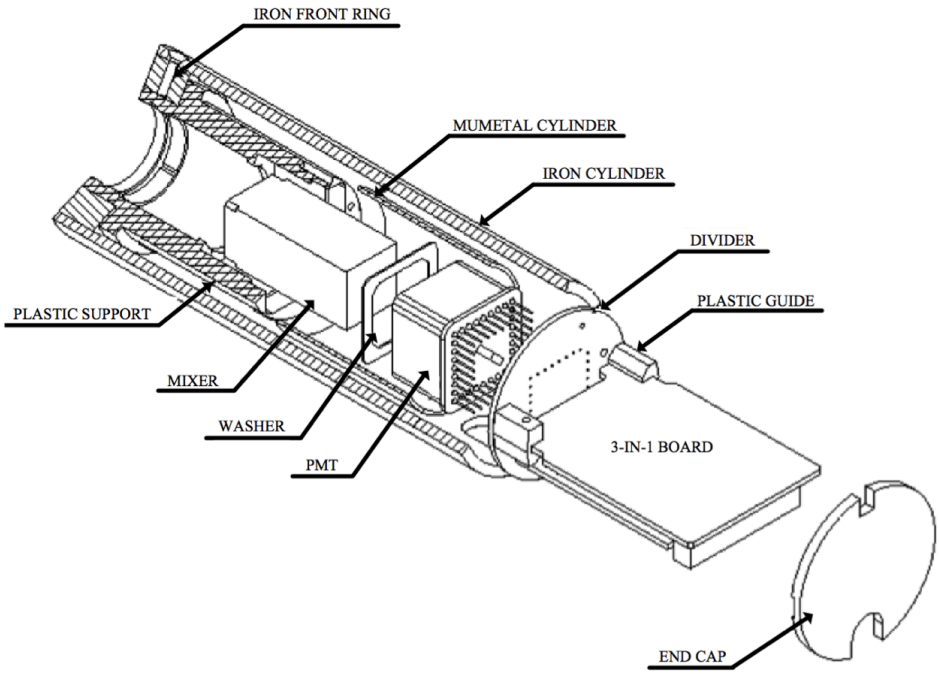


Figure 2.8: A diagram showing the structure of the PMT block [6].

Digitizer board

The digitizer board receives bi-gain (low and high) signals from the PMT 3-in-1 cards as input to its ADCs. Each PMT is readout by two separate ADCs. The digitized data from six ADCs (3 PMTs) is sent to one data management unit (DMU) ASIC chip which implements specific circuitry for the required pipeline and buffer memories, cyclic redundancy check (CRC), memory parity checking, bunch crossing identification (BCID) and gain logical selection computations. Essentially, each board is equipped with 12 ADCs for reading 6 PMTs, 2 DMU chips, and one TTC receiver (TTCrx) chip for the control and distribution of ATLAS clock [27]. There are 8 digitizer boards in each Long Barrel super-drawer that readout 45 PMT blocks, and 6 digitizer boards in each Extended Barrel super-drawer that readout 32 PMT blocks. Figure 2.9 shows a sketch representation of the TileCal digitizer system.

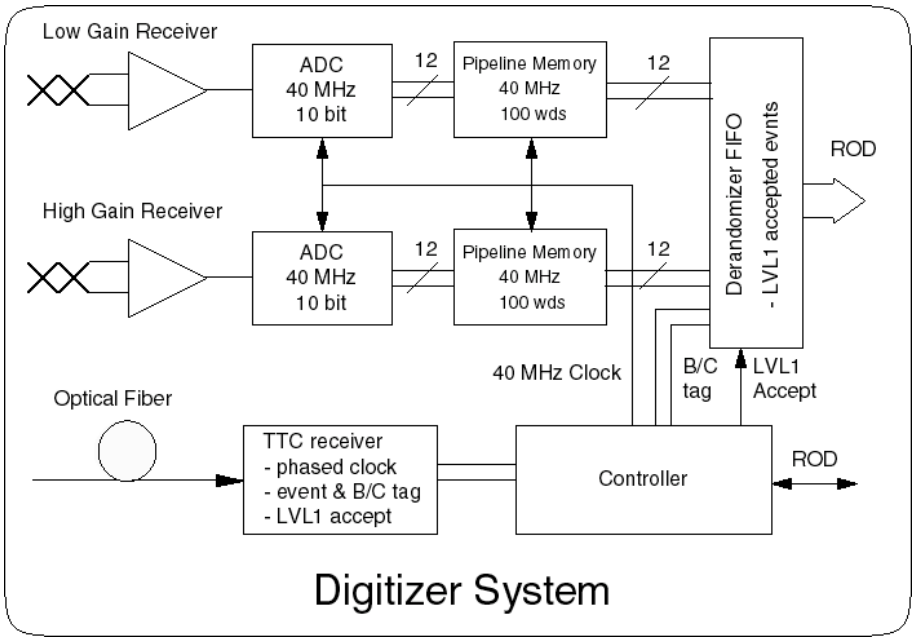


Figure 2.9: A sketch representation of the Tile Calorimeter digitizer system [27].

Interface board

The Interface board receives digitized data from the digitizer board upon the reception of a L1A signal from the LVL1. Each super-drawer is equipped with one interface board. This board essentially encodes and transmits the data through dedicated fiber-optical links to the BE electronics and receives TTC commands from it as seen again in Fig. 2.7. The entire readout section for the interface board has been replicated with two dedicated output optical fibers for redundancy and to reduce single event upset errors. The interface board also computes the CRC on the input and output data streams which are used in the BE electronics to process data not affected by single event upset errors and to perform online data quality checks [28].

Trigger summation boards

This is a special type of board that is also mounted onto the mother-board. It's primary purpose is to merge low gain signals from 3-in-1 boards up to a maximum

of six to form the analog trigger-tower sums which are required by the LVL1 trigger.

2.3.2 Back-End Electronics

As mentioned in the introduction of this section, the TileCal detector is composed of four logical partitions (see Fig. 2.6a), the BE electronics are organized into four TTC partitions as well. Each partition has 64x2 TTC links and 64x2 Readout Driver (ROD) links to write and read from the detector respectively. The TTC links are connected to TTC modules in a 6U Versa Module Eurocard (VME) crate [29] and the ROD links are connected to ROD modules in a 9U VME crate. These crates have been nicknamed the TTC and ROD crates in TileCal to specify the type of units they contain. Each of the crates is controlled by one Single Board Computer (SBC). The crates are powered and monitored by DCS as well. A simple schematic of the VME crate modules is show in Fig. 2.10. Each of the VME crate modules is briefly presented next.

Local Trigger Processor

The ATLAS Local Trigger Processor (LTP) receives timing and trigger signals from the CTP and injects them into the TTC system of the sub-detector. This module can also be used in stand-alone by using local TTC signal sources or by internal signal generation via a pattern generator.

Local Trigger Processor Interface module

The ATLAS LTP interface (LTPi) module is used to provide an interface between the CTP and LTP to allow combined operation between various sub-detectors simultaneously in contrast to the ATLAS global operation.

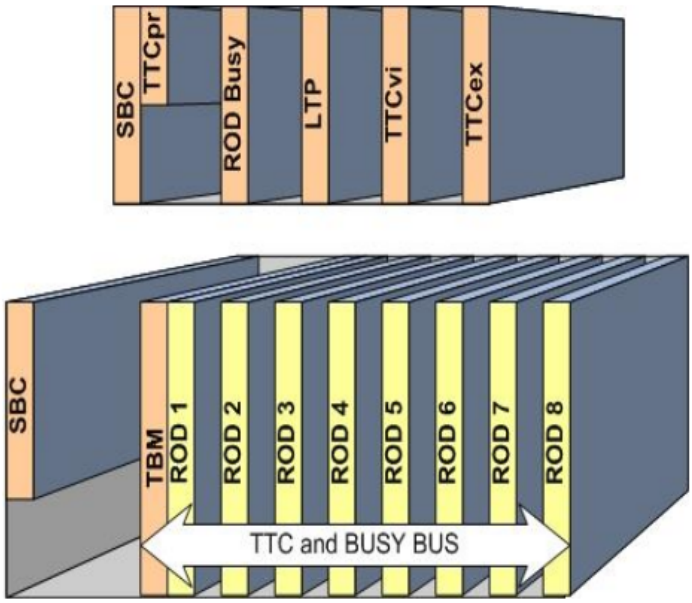


Figure 2.10: A sketch representation to show some of the TTC and ROD VME crate modules of TileCal BE electronics partitions [30].

TTC VME bus interface module

The ATLAS TTC VME bus interface (TTCvi) module is used to configure the FE electronics and interface the local TTC system to the global TTC system. It provides A and B channel signals to the TTC distributors for optical conversion, encoding, multiplexing and distribution to the TTCrx chips for the corresponding FE and BE electronics controllers. The TTC channel A is used for the distribution of the L1A signal to the TTCvi consolidates a L1A computable source selector and an internal trigger emulator used for test purposes. The TTC channel B is used for the transmission of formated and framed commands and LHC clock synchronous or asynchronous data.

TTC emitter (TTCex) module

The TTC emitter (TTCex) is a laser based module which converts TTCvi commands into optical signals that arrive to the FE and BE electronics. It provides 10 optical outputs at a level of approximately 0 dBm. The optical outputs of the

TTCex are fanned out by a 1:32 TTC optical coupler (TTCoc) to broadcast to a total of 320 destinations.

TTC receiver in PMC Form Factor module

The TTC receiver and PMC Form Factor (TTCpr) module is a TileCal specific card that is plugged into the SBC of the TTC crate. It is used to make available the TTC information in the TDAQ framework for calibration runs. It was designed to provide event ID, BCID, and trigger type for each event in the data records. It provides a busy signal which is connected to the ROD Busy module.

ROD Busy module

This ATLAS module is used to monitor the busy. It measures the busy in bunch crossing units and produces the sum of each of its 16 busy input lines which can be conveniently masked. This module generates a VME interrupt signal after a programmed time-out. In TileCal, this module intercepts the busy signal from the ROD crate Trigger and Busy Module (TBM) and the TTCpr card. The busy output is sent to the LTP busy input.

Shaft module

This is another TileCal specific module which controls the different calibration trigger requests. It is a specific VME board module that is able to share calibration requests during physics runs. Each calibration request can be enabled and its firing timed with respect to the TTC signal that clocks the turn of the LHC beam.

Laser ROD

This module is a 6U VME module that provides information from the Laser calibration system into the data-flow and furnishes TTC signals to the Laser system. It is equipped with a High-speed Optical Link (HOLA) card which provides data

fragments to a Readout Buffer (ROB) of the LBC partition ROS through a dedicated readout link (ROL).

ROD module

The ROD is the last element of the LVL1 trigger. It is located between the FE electronics and the ROS of the LVL2 trigger. The data from the FE electronics is transmitted in and out of the ROD through optical links on the board for each super-drawer. The ROD motherboard houses a maximum of 4 Processing Units (PUs) for computing the energy and time for each readout channel. The PU is a mezzanine card which is very important to the RODs. It is instrumented with two input FPGAs, two Digital Signal Processors (DSPs) and one output FPGA. The output FPGA provides interface with the rest of the ROD. The Input FPGA receives data from two FE links which are checked and formatted for DSP processing.

The ROD is coupled to a Transition Module (TM) placed behind it which receives the data fragments through the connectors of the VME crate. TileCal has been using only two PUs until mid March 2017 when the number of PUs, ROS, ROLs and HOLA cards were doubled to increase the readout bandwidth. The TM was also upgraded during the ROD upgrades and is now equipped with four HOLA cards that transmit data fragments to the ROS through the ROLs (see Fig. 2.11). The author's contributions to this ROD upgrades was to modify the TileCal Online software to accommodate the doubled number of HOLA cards, PUs, fiber connections and the ROLs. Details of the current TileCal Online software as re-arranged and compiled by the author will be presented in Chapter 3.

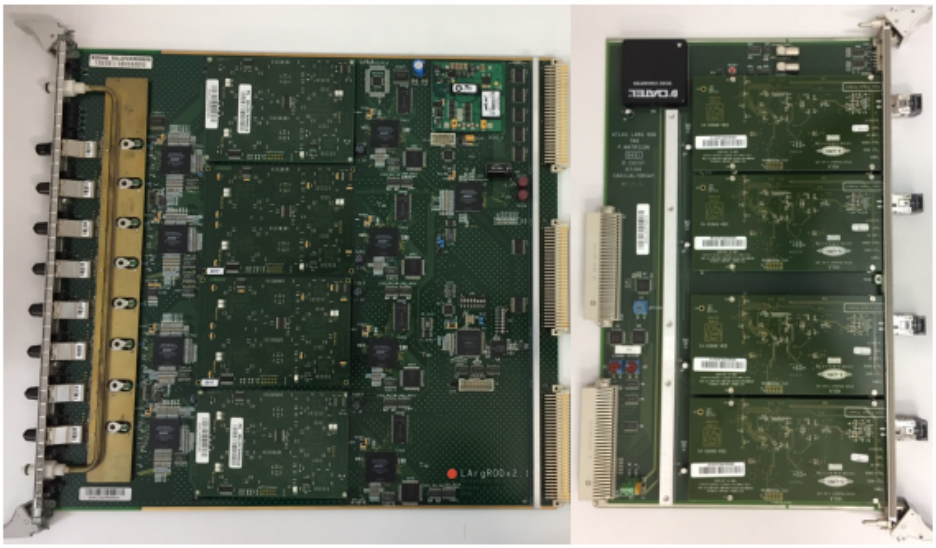


Figure 2.11: The TileCal ROD motherboard module with 4 PUs (left), and the Transition module (TM) with 4 HOLA cards (right) [19].

Trigger and Busy Module

The TBM is a 9U VME module. It receives TTC signals through optical links from the local TTC system. The signal is propagated to every ROD module through P3/J3 connectors using the CP3 backplane in the ROD crate. The TBM also gathers busy signals through the CP3 plane from the eight RODs in a VME crate and provides a busy signal to the ROD Busy module.

Detector Control System

The DCS architecture is implemented as a distributed BE system that runs on computer nodes and various FE systems. The BE software functionality is two-fold such that it requires data from the FE components and offers supervisory control functionality like data processing and analysis, storage or archiving and display. The system also provides handling of alarms, messages and commands. To provide the needed functionality, the BE system of the ATLAS DCS is organized hierarchically in three layers or levels as depicted in Fig. 2.12 [31]. The main DCS systems for TileCal monitor and control the LVPS, the High Voltage

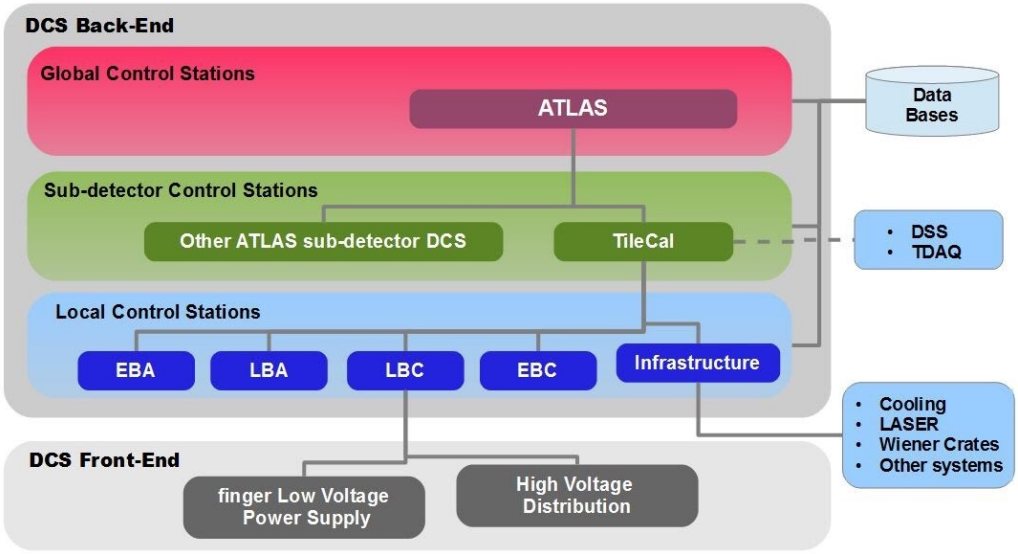


Figure 2.12: The Hierarchal organization of the TileCal DCS system for Run 2 [31].

(HV) power system (HVPS) and the cooling of the electronics. The HV system is needed for operation of the PMTs, the LV system is required for powering the entire readout electronics and for HV regulation, and the cooling system is required to keep all the electronics within the correct temperature range. There are other dedicated control systems specifically for the calibration related systems independent of the DCS, but however interface with the TileCal DCS for data and command exchange [32].

Calibration System

TileCal construction has been augmented for good energy resolution achieved by the use of highly accurate and precise system calibrations. There is three main tests and calibration systems that work together to provide accurate jet energy measurements. These systems are the previously mentioned CIS, the Laser system, and the Cesium system. Each system tests a specific element of the readout electronics chain and the combination of the three provides the overall calibration of each readout channel as shown in Fig. 2.13.

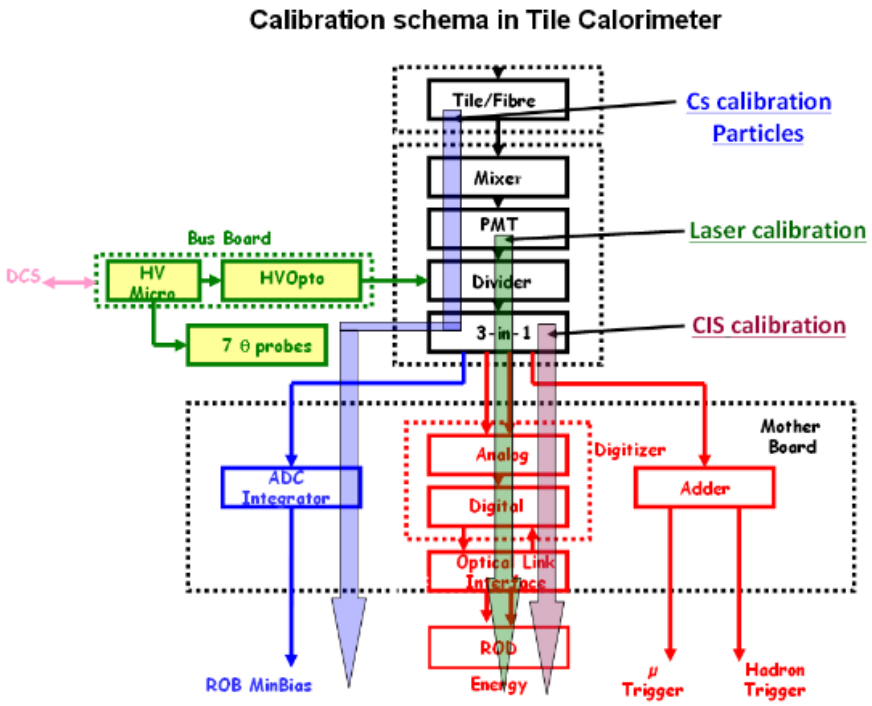


Figure 2.13: The TileCal test and calibration system.

- **CIS:** This calibration system consists of the simulation of physics signals through the injection of known charge values into the readout electronics. This is achieved by using using dedicated capacitors (5 pF and 100 pF) plus a 4096 DAC controlled by the ADC. The relation of the peak amplitude in the response of the electronics (measured in ADC counts) to the value of charge injected (in pC) gives the calibration of each ADC in units of ADC counts/pC. This enables verification and identification of errors with the readout chains and allows for calibration of single ADC outputs of every PMT for every 3-in-1.
- **Laser:** The Laser calibration involves sending laser pulses into the PMTs allowing for calibration with respect to each PMT's response. This allows for the calculation of corrections to the optical gain of the PMT and a test for the stability of each PMT over time.
- **Cesium:** The Cesium calibration consists of circulating sources of ^{137}Cs

isotope that emit 662 keV photons around the detector. These photons interact with the plastic scintillator tiles which then emit photons to the WLS. This allows for the test of stability and uniformity of the optical response of the cells. In a Cesium scan, the radioactive sources are circulated around TileCal using a hydraulic system.

Chapter 3

Tile Calorimeter Online Software

3.1 Online Software

The Online Software system is in charge of the overall experimental configuration, control, and the monitoring of TDAQ systems and management of data taking configuration. It is implemented such that it allows users to be grouped into two categories: the TDAQ operator, and the TDAQ developer. The former is a user who considers TDAQ as a black box and issues high level commands to it or uses for monitoring of the data taking process, whilst the latter is a user who deals with the system at much deeper level and customizes it to satisfy specific requirements. Basically, the Online Software is essentially the glue that holds the various sub-systems and provides not only a uniform control interface, but also the ability of easily hiding the specificities of those sub-systems so that they can be provided with control services. The Online Software does not contain any specific sub-system components because it is developed as a customizable framework with strong requirements on distribution, robustness flexibility, scalability and modularity. The TDAQ is defined from the control point of view as a collection of applications running on a set of hosts. It is modeled around a common Finite State Machine (FSM) that defines few well defined states and transitions

and hides the complexity of the individual components. The overall TDAQ status is kept in a coherent state by a Run Control (RC) service which implements a hierarchical tree with a Root Controller acting as the root. The TDAQ is best described by the configuration database service [33].

The configuration database is a service containing the TDAQ system description and detector specific information including software, hardware, partitions and run parameters. This information description is gathered in form of configuration for distinct run types (calibration, physics, debug, etc.). This service is used by sub-detector experts to develop their own configuration parts and to write the code configuring their applications using common configuration service tools. Its implementation is based on the Object Kernel System (OKS), a persistent in-memory object manager. The primary persistent storage for this OKS is XML files. There are two types of this XML files; the schema files which define classes, and the data files to store database objects.

An XML file can include other files to build a complete database from well structured files and to share them between different OKS databases. Figure 3.1 shows an overview of ATLAS' OKS configuration service architecture. The configurations database can be accessed via API provided by the config package based on two layers; the first config layer provides an abstract interface to access configuration schema description objects and to work with databases, and the second Data Access Libraries (DAL) layer uses the above abstract config to instantiate database data as appropriate objects of such classes and to map the database schema on C++, Java and Python classes [33].

The starting point that defines a TDAQ configuration is the Partition. In ATLAS a Partition is a synonym for a data taking configuration, it is essentially an object of the configuration database from which all the configuration of the

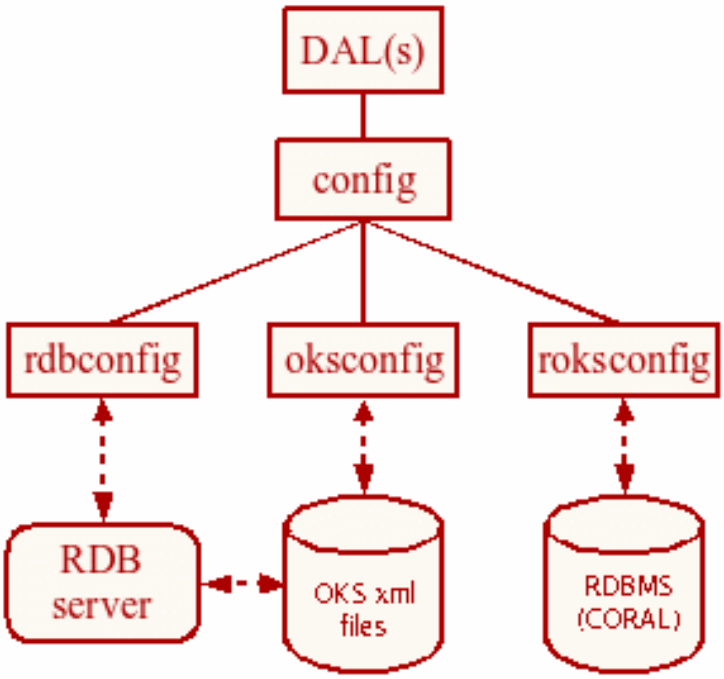


Figure 3.1: Schematic overview of the ATLAS OKS configuration database architecture [34].

hardware and software elements which are included in the readout is spanned. Multiple Partitions can run in parallel provided that they use distinct or shareable resources. A Partition contains a number of Segments: those are modular parts of the TDAQ that can be included or excluded as a whole from one or more Partitions. In ATLAS we typically have one Segment per sub-detector (see Fig. 3.2), which is further subdivided into as many Segments as there are TTC partitions (TTC partitions are hardware-wise the smallest entity that can be run, i.e. take data independently). There are four TTC partitions in TileCal (EBA, LBA, LBC and EBC) as already described in the BE electronics section of chapter 2. Starting from a Partition, we thus have a nested tree of segments. This tree matches one-to-one to the RC tree, i.e. every Segment is controlled by one controller application. Besides containing other segments, a Segment is associated to a set of hardware components and software applications. Each of the four TTC partitions is defined as a segment inside the overall TileCal segment which itself

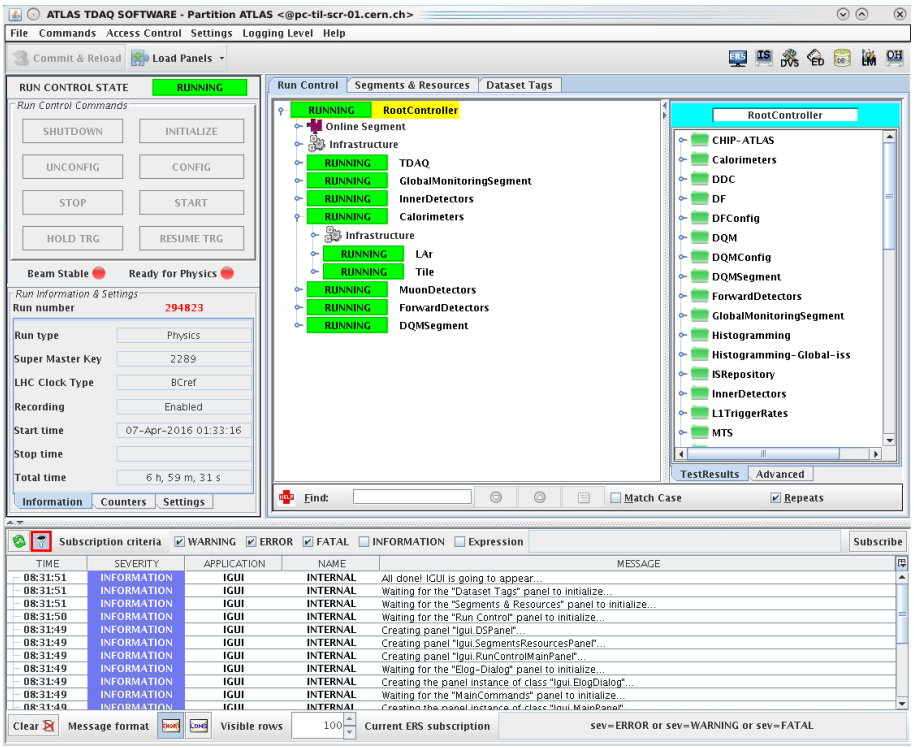


Figure 3.2: A screen shot of the GUI for ATLAS TDAQ partition in state running, TileCal is included as a segment into this partition.

is referenced as a segment in the main ATLAS partition. The author contributed in the implementation of the current production version (2017) TileCal data taking partition. The basic services needed to run a partition are listed below with brief descriptions, detailed information for each service is described in the ATLAS TDAQ monitoring working group website accessible from [35].

- **Resource Manager (RM):** It allows to lock resources for exclusive or limit shared usage as described in the configuration database [34].
- **Access Manager (AM):** This service introduces action authorization based on user access or role. Also used at system administration level and in the DCS [34].
- **Process Manager (PMG):** This is the only service in the system that starts and stops processes. It uses the AM and the RM services to evaluate

whether an operation can be executed.

- **Inter-Process Communication (IPC):** The core communication service. It relies on the underlaying TCP/IP message passing.
- **Information Service (IS):** Provides a means of sharing information between software applications in the distributed environment.
- **Online Histogramming (OH):** Provides the means for online data analysis and monitoring by implementing user defined histogram tasks to retrieve data from a number of histogram providers.
- **Error Reporting System (ERS):** This service allows experts and shift crew to track and address errors relating to the TDAQ infrastructure [36].
- **Integrated Graphical User Interface (IGUI):** The user interface with the RC (see Fig. 3.2).

3.1.1 Tile Calorimeter Online Software

The TileCal Online software is the set of TDAQ software used for the operation of TileCal which is not provided by the ATLAS TDAQ online software. It is basically an extension of the ATLAS TDAQ software which provides TileCal detector specific software for the BE electronics, infrastructure for calibration systems, monitoring (including hardware), and the diagnostic and verification systems tests (DVS). One of the core components of the TileCal Online Software elements is the BE electronics ROD Crate DAQ (RCD). It is supported by the ATLAS Data Flow policy for which the TileCal Online software provides plug ins. This keeps the programming efforts focused on specific hardware handling since the core software is centrally managed. The RCD was already implemented for Run 1 as described in the following note [37].

The RCD is an extension of the ROS software that provides a complete framework for implementing DAQ functionality between ATLAS system specific elec-

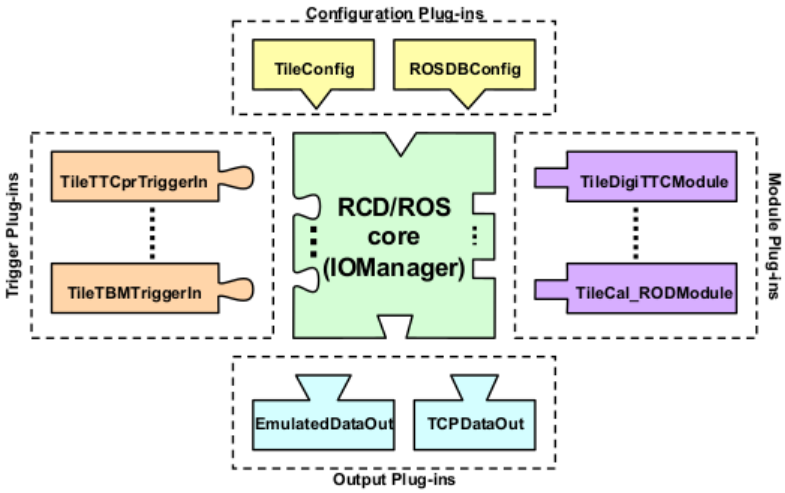


Figure 3.3: ROD Crate DAQ schematic representation [30].

tronics and the DAQ system common parts boundary. It allows the use of common services (such as data output and monitoring channels) together with dedicated libraries for control, monitoring, event building, DAQ and emulation of detector specific electronics. The application employs four specific runtime (dynamic) plug-in types to implement the different I/O protocols. The RCD is an RC application and it reacts to the FSM transition commands initiated by TDAQ user through the GUI. A schematic overview of the TileCal specific RCD application with its plug-in types is shown in Fig. 3.3. The configuration plug-in is the first one to be loaded and it informs the application about the other plug-ins. It loads the information from the configuration database and passes it to the RCD application. The Trigger plug-in implements the functionality of the trigger thread and handles trigger requests for data fragments. The Module plug-in describes a hardware or a software component that is controlled by the RCD application. And lastly, the Output plug-in which basically implements request handlers that write event fragments to output devices. Several plug-ins for distinct output devices such as Ethernet or local disk are provided by the RCD framework. Detailed descriptions of the TileCal specific plug-ins have been discussed and can be found in [26, 30].

3.1.2 Tile Calorimeter run types

There are six different run types in TileCal, five of which are calibration runs and the last being the physics run. A brief description of the run types is presented next. The detector configuration is different for physics and calibration runs. The calibration run types require the storage charge value sent to the FE electronics along with the data readout from the RODs. This requires the inclusion of additional elements in the readout which slows down the acquisition rate. Therefore, the calibration configuration is not feasible for physics runs. All run types are taken using the 7 samples window at a readout window of 25 ns $\times$ 7 = 175 ns. The runs are either bi-gain: both ADC gains are readout for each channel, or mono-gain: only one ADC gain is read-out per channel. The gain is chosen automatically by the DMU on the basis of the 2 following criteria:

- High Gain overflow: if the number of ADC counts in HG is 1023 for at least 1 of the samples, then the gain is switched to LG.
- High Gain underflow: if the number of ADC counts in HG is 0, then the gain is switched to LG.

During ATLAS operation, sub-detector DAQ experts or shifters take calibration runs that must be checked offline to validate the quality of the data prior to physics analysis. This process is somewhat automated by the TileCal standalone offline frameworks, however, shifters are needed to evaluate the results. The Data Quality Validator (DQV) and the Data Quality Leader (DQL) are the shifters responsible for performing this analysis and recording the results. The primary role of the DQV is to analyze and validate both the calibration and physics data as instructed by the DQL, and the DQL's primary role is overseeing all operational data quality activities and reporting the results to the TileCal group and the broader ATLAS community. The author has assumed both responsibilities

in 2016 and 2017. The checks are mainly for faulty hardware components to be included in the repair list (during yearly maintenance periods) or to be inserted in the channel/PMT status database (beam period).

Calibration Runs

- **Pedestal:** This is a bi-gain calibration run to monitor electronics noise without a signal. This is used to verify the noise level of the detector and the data integrity.
- **Charge Injection Scan (CIS):** This is a bi-gain calibration run that yields the ADC count/pC conversion for each channel. A DAC ramp is performed for each of the two capacitors (5 pF and 100 pF). For each DAC step the timing is varied. This run scans the entire range of the TileCal electronics to verify the correct linearity of the ADC, the control of the DAC settings and to find stuck bits and data integrity problems.
- **Mono CIS:** This is a mono-gain calibration run in which a constant charge is injected to monitor electronics stability. The purpose of this run is to verify the correct response of the ADC, find gain switching, Mother-board timing, and data integrity problems.
- **CIS ramp:** CIS is fired with a configurable pattern and data is read-out in physics mode for Optimal Filtering reconstruction validation.
- **Laser:** This is another mono-gain calibration run in which a Laser light is injected into the laser fibers to make sure there are no dead PMTs/fibers and to calculate PMT gain and timing. The purpose of this run is to verify the correct response of the PMT, find gain switching, digitizers timing, and data integrity problems.

Physics Runs

This a mono-gain run with ATLAS setup and TileCal included as a segment running in the combined partition. The L1A is provided by the CTP through the LTPi and the LTP.

3.2 Release strategy

The software used for the operation of TileCal is grouped together as packages in the TileCal Online software release. The release follows the ATLAS TDAQ software policies and release, meaning that it is updated simultaneously following ATLAS TDAQ updates and policies. It is built up of CMake packages which are stored in a Gitlab (atlas-tile-online) repository. The list of packages included in the release is referenced by a packages.txt file inside the release build area. For every new release built, the packages are checked out into an Andrew File System (AFS) account and compiled at once. All packages that are ready for a new release build are, and should always be tagged using the Git so-called annotated lightweight version tags which require a specific message. Such tags are never deleted once pushed to the Gitlab remote repository. The tags follow the guideline of 3 groups of letters and digits specifying the major, minor and patch version, e.g. v1r0p0. The latest tag for every package is used for building the release. The versioning of the TileCal Online release (tile-X.Y.Z.U) follows the TDAQ versioning (tdaq-X-Y-Z) adding additional enumeration for the number of times the release has been rebuilt due to updates. External software is used by the TileCal Online release. This includes offline TileCalibBlobObjs (used to access the information stored in COOL DB) and other specific software which resides in offline SVN/Git repository [38]. At the moment, the TileCalibBlobObjs is the only offline package used by the online software, and it is now however compiled together with the other online packages as a TDAQ package. After the compilation process, the

binaries are transferred to Point 1 and installed in the detector area. No write permissions are given to the release files once installed. In fact, a patches folder is provided for a given release with full access for developers to test their code. If a specific patch has to be applied to the release, it has to be copied from the patches to the installed directory. TDAQ software is best described by its classification viz. organization, build system and the source code management tools. A brief description of each classification will be presented next, the programming language supported by the software will also be briefly described.

3.2.1 Software Organization

The TDAQ software is organized in three projects viz. tdaq-common, dqm-common and tdaq. It provides access to a large number of external software packages such as Boost [39], GCC [40], Qt [41] just to name a few that are maintained by the SFT (SoFTware Development for Experiments) group at CERN, and this is shared with offline and other experiments like LHCb. A graphical representation of the sub-detector software project hierarchy is shown in Fig. 3.4, and Fig. 3.5 is a graph showing the list of packages in the TileCal Online software release with their dependencies.

- **tdaq-common:** This is the most basic project used by both TDAQ and offline software. Examples of the packages that it contains are the raw event format and storage, and the ERS. All other TDAQ projects are built against this project.
- **dqm-common:** This projects contains packages that are used for data quality monitoring (DQM) for both TDAQ and offline DQM. It is built against the tdaq-common project.
- **tdaq:** This is the TDAQ projects itself and contains all the rest of the packages used by sub-detectors and the HLT. This project is built against

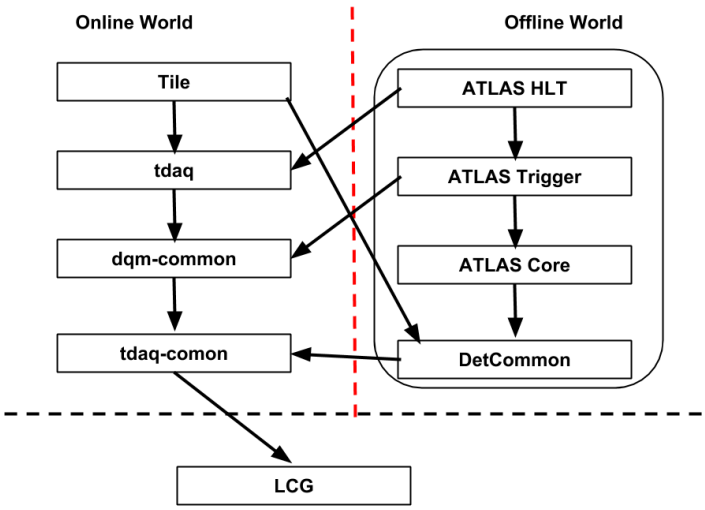


Figure 3.4: A graphical representation of the TDAQ software context organization. TileCal and other sub-detector software projects are built against the tdaq project, which is built against the dqm-common and tdaq-common projects.

both the tdaq-common and dqm-common projects. TileCal Online software is compiled against this TDAQ project.

3.3 Software Build Systems

The TDAQ software (same as offline software) has for many years relied on the CMT build system. However, the ATLAS code base has now evolved beyond CMT capabilities and this has resulted in replacing CMT with CMake in favor of modern software development tools and procedures. The TDAQ software has been migrated, and now uses the CMake tool to build, test and package software. TDAQ software is built and distributed as packages. A Package is the smallest manageable unit of a software. It is the primary development unit and can have dependencies against other packages. TDAQ provides several CMake specific commands to replace CMT. TileCal Online software has also been migrated and rebuilt with CMake following TDAQ by the author. The migration to CMake has

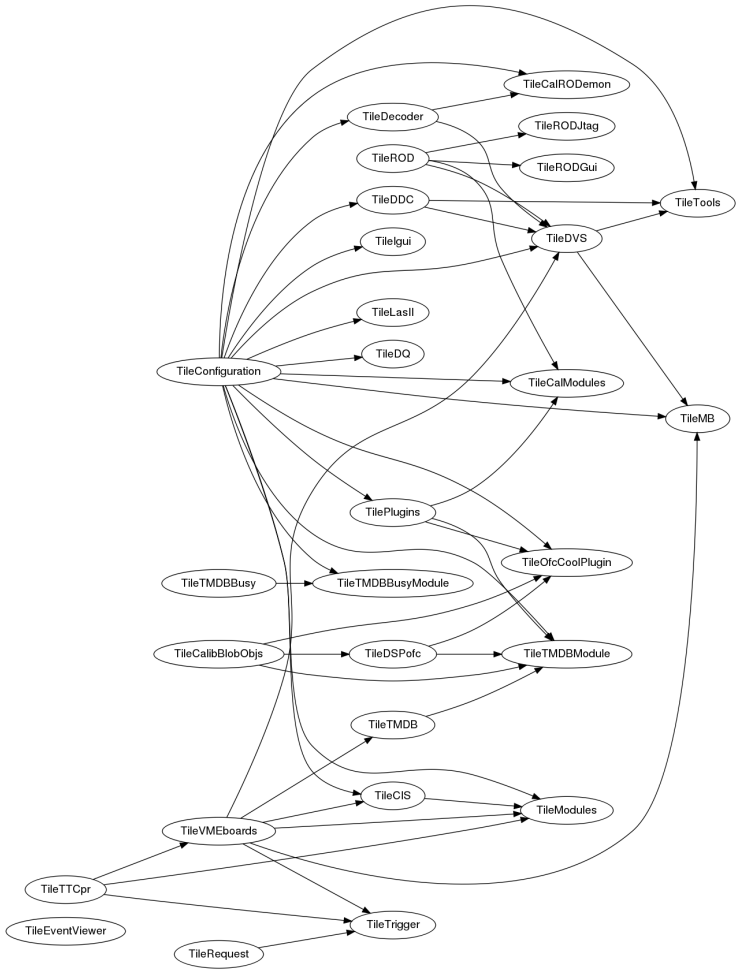


Figure 3.5: A graph showing all packages currently available in the TileCal Online software release. The total number of packages is 29 and most of them depend on the TileConfiguration package.

provided greater similarity and better integration between the offline and online worlds (see Fig. 3.4).

CMT is a configuration management environment based on some management conventions and comprises several shell-based utilities. It was developed as an open-source academic project aimed at providing support to software developments in the context of large physics experiments by LAL (Laboratoire de l'Accélérateur Linéaire - CNRS) [42]. It structures software into projects where

each project contains a number of packages. A package typically contains some well-defined functionality such as a library or an executable application. A package typically has one or a few authors that maintain it and are responsible for it. CMT works as a layer on top of the usual make program to build, clean and install e.t.c., you basically specify libraries an applications in a high-level way and it creates a Makefile for you. It supports the building of multiple configurations for different compilers and operating systems.

CMake was created by Kitware Inc. as an open-source cross-platform family of tools designed to build, test and package software. It is used to control the software compilation process using simple platform and compiler independent configuration files, and generate native makefiles and workspaces that can be used in the compiler environment of your choice [43]. CMake is in essence very similar to CMT but provides better performance, maintainability and multi-platform support. One of the reasons for the migration was the maintenance of CMT by itself, which was at an end of life stage while CMake is community developed and supported. Figure 3.6 shows a package compilation time comparison plot between CMT and CMake. The fasted a full TDAQ release can be built with CMake is about 45 minutes, whilst it takes CMT more than 1 hour to build the same release on the same set of hardware. The plot also shows that for relatively small projects, the build time differences are within a few minutes and can be neglected.

ATLAS relies on multi-component infrastructure to provide software for simulation, reconstruction, trigger and analysis. It has a huge code base which needs to be modular in a way that is not too common in industry. The amount of resources used for software building need to be lowered and the existing build systems have already been pushed to their limit. TDAQ and almost all other ATLAS releases have nightly build projects which are large and CMake does a better job because it is by design enhanced to parallelize software builds much

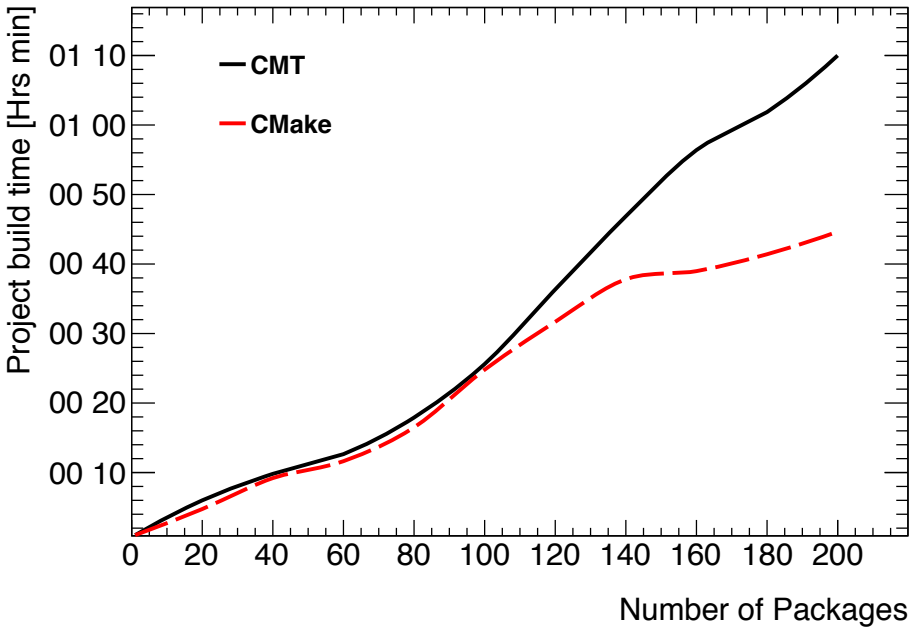


Figure 3.6: CMT vs CMake.

better. This eliminates the need for build accelerators such as Distcc (a program to distribute builds across several machines on a network) [44], and also provides much faster and simpler release deployment and installation.

3.3.1 Software Programming Languages

A chart representation of the programming languages in the TileCal Online software repository is shown in Fig. 3.7. C++ is the main programming language for TDAQ software with a share of 97%, almost all services and libraries are used from C++. Java is used for the IGUI that controls the TDAQ sessions, it accounts for only 2.3% of the Tile Online software. Also used for various web based services on the back-end side, most services (e.g. Expert system) are used from Java as well. Python is the preferred scripting language. Many services have a Python binding for ease of use and quick solution implementations. Widely used when speed is not of adamant importance. The officially supported architecture

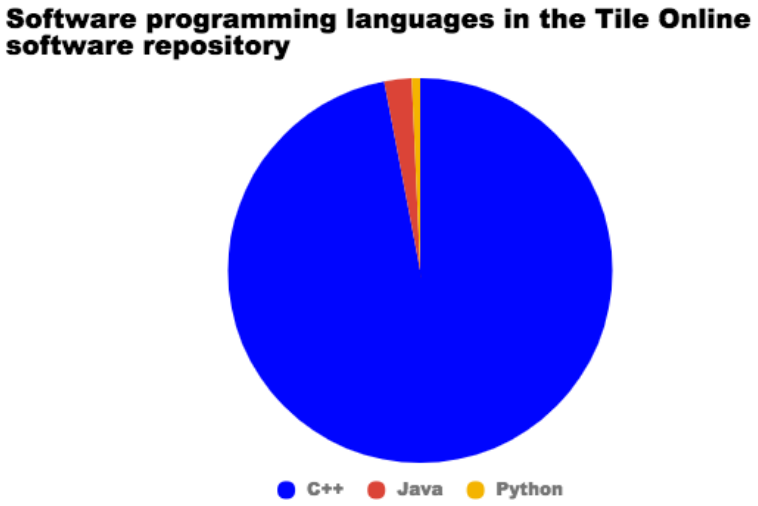


Figure 3.7: A chart representation to show the amount of applications developed using the 3 main TDAQ software programing languages (C++, Java and Python). The total number of applications (executables and libraries in the Tile Online software repositories 133 applications. There is only 1 application developed in Python (TileEventViewer) and is used for event monitoring, 2 Java applications (TileIgui and RODTestIguiPanel) both of which are IGUI panels, and the rest of them are mostly C++ real time applications (executables and libraries).

is 64 Bit, the operating system is Scientific Linux (SLC) and the compiler is GCC.

3.4 Version Control System

Software revision control is a piece of software that records different versions of code in a persistent and recoverable way. ATLAS has been using Apache Subversion [45] (often abbreviated SVN, after the command name svn) for software conversioning and revision control and this is scheduled to stop by the end of LS2 in favor of Git [46]. Git is a modern distributed version control system, it is widely adopted in open source community and allows a more decentralized approach to software version control. Git is fully supported by CERN as the recommended VCS tool for all software projects, and this has rendered migration from SVN to git almost inevitable as a non-git solution would require dedicated

ATLAS support. TDAQ software has been migrated to use Git hosted on a modern development platform called Gitlab (`https://gitlab.cern.ch`) as the central repository. Although git is a fully distributed service, the Gitlab server plays a role similar to the Subversion server: it contains the official version of the code and this is what's used to build releases etc. The TileCal Online software has also been migrated from SVN to git by the author, and is now hosted on a Gitlab server (https://gitlab.cern.ch/atlas-tile-online).

Moving an organization from SVN to git involves convincing people to unlearn a lot of SVN stuff they're comfortable with, then learn a lot of new git stuff they don't understand. It takes several months of advocacy and education to move even a small team, and productivity will probably go down before it comes back up. In order to keep productivity afloat, the author implemented Git-SVN repositories to synchronize the git repository with any modifications pushed into the SVN repositories by developers/contributors who are not yet fully comfortable with Git. The TileCal Online Gitlab repository is also setup to assume developers coming from SVN, assuming no advanced features are used at the beginning, so all development happens on the git master branch (equivalent to SVN trunk). The use of feature branches is trivial since there is only one detector and one team in charge of maintenance and operation. Unless a huge development needs to happen in parallel to data taking, the version that is always updated is the master branch. New features are added and adopted, or discarded and not committed. Every single TileCal Online package has its own git repository and the collection of all these packages is organized in a Gitlab group called atlas-tile-online.

3.5 Diagnostics and Verification System

DVS is part of the ATLAS TDAQ online software packages used for configuring and executing tests for TDAQ components, for detecting and diagnosing faults,

and for advising recovery actions to the TDAQ operator/user. DVS is a framework which allows TDAQ developers and experts to integrate tests and knowledge into it, so it can be later used by a non-experienced shift operator to verify the functionality of the TDAQ and diagnose problems. It allows to have a number of tests defined for a single TDAQ component. Tests can be started on different hosts/computers sequentially or in parallel [47]. High precision DVS tests are available for TileCal under the TileDVS package. These tests the digital and integrator readouts of the super-drawers, other set of tests are also available as tools for special purposes. The digital DVS tests are a set of checks for the digital readout of the super-drawers, a list of the available digital tests is presented next;

- **CIS (Low and High gains):** This test checks the existence of a pulse inside some bands for low and high gains.
- **Pedestal:** This test computes the low and high frequency noise for the data and compare it to the nominal values.
- **DMU Memory:** A bitwise pattern is written into the memory of the DMU. Pattern data is read-out and checked for mistakes.
- **Stress:** A 100 kHz random trigger and a full busy logic is used to veto the acquisition. Data is processed inside the DSP. The number of CRC errors found in the data is reported.
- **Digitizer addresses:** This is a list of tests used to get the correct addresses of the components on the digitizer boards.

The TileCal DVS tests use two binaries which are executed on different machines and use the information service (IS) server to synchronize and communicate. So before executing DVS, the IS server has to be firstly booted either by starting the TileCal DAQ partition, or by other expert means. The TileCal DVS tests can be run in 2 ways: from the command line or from the DVS GUI that TDAQ provides. During the maintenance period one has to quickly assess the

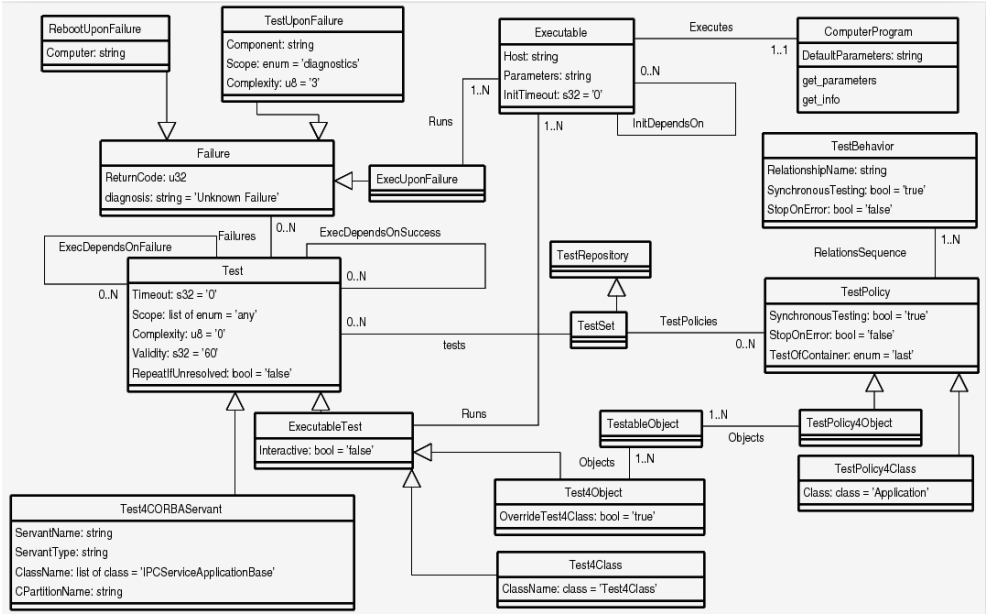


Figure 3.8: Diagram showing the different OKS classes and their dependencies for the Test Manager's DVS test configuration.

functionality of the FE electronics, first by confirming existing problems, and secondly by assessing the validity of the repairs. The command line method is rather long, tedious and mostly understood by experts. The DVS GUI method is rather preferred as it can also be used by shifters and non-experts. The author has implemented a wrapper to start the complex DVS tests from the GUI by describing all the needed hardware super-drawer objects in the configuration database.

3.5.1 DVS tests and configuration

The Testing service allows experts to introduce mechanisms that can determine the functioning of the system, diagnosing problems (via chains of tests) and fix issues (via follow-up actions). This service exists since the early days of the ATLAS TDAQ, but has recently (since tdaq-05-03-00) been expanded to allow experts to put all their knowledge into the system using the OKS database. The Test Manager (TM) is in charge of executing the tests on demand and reporting back their

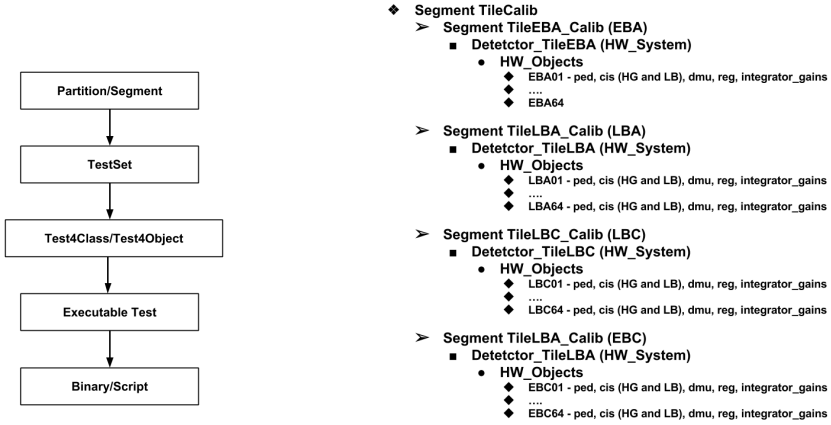


Figure 3.9: A simple diagram to show how to configure tests for the TM (left). The sketch on the right shows the tests represented as a tree hierarchy with the entire TileCalib detector segment as the root of the tree. This allows tests executed from the TileCalib object to be propagated down to all (HW_Objects) super-drawers in each detector segment (HW_System).

outcome, the TM employs an internal DVS library that is used the Run Control and the GUI.The diagram in Fig. 3.8 shows the different OKS classes and their dependencies for the TM configuration.

A component of the TDAQ can be tested in two ways; either by executing a set of binaries or scripts on it, or by invoking the ipc::servant::test method on it. The latter mechanism is only available to components that extend the ipc::servant interface, of course, i.e. applications that are published into the IPC domain server and can be contacted via their published name. A binary or script can be used as a test if it satisfies some predefined constrains like, it must support verbose mode and must use the TDAQ predefined Test-Result return codes to indicate that the test passed. The TileCal DVS tests are defined to be executed by a set of several wrapper scripts.

Tests are configured using the Test Manager which reads the OKS configuration database to select tests to be executed. Tests have to be collected in Test Repositories and linked to the Partition or one of its Segments. There are three

types of Tests that can be instantiated by the user, the Test4CORBAServant, the Test4Class and the Test4Object. The two latter ones are used to describe tests that execute one or more binaries or scripts, while the first one is used to describe tests that will use the ipc::servant::test method. The fundamental flow for test configuration is best described by Fig. 3.9, brief description for each step is also presented next.

- **Partition or Segment:** Tests have to be collected in the test repository (TestSet) and linked to the partition or one of this segment.
- **TestSet:** This contains the list of defined tests and TestPolicies. TestPolicy allows the expert to determine in which order a component shall be tested with respect to some components it relates to. For a Segment, we can define that the test for the Segment itself shall be performed before/after having tested the HW_Systems and Applications that are contained in it.
- **Test4Class/Test4Object:** The Test4Class is preferred because it allows the expert to define a single test as class that is inherited by all objects of that class.
- **Executable:** Executable object is contained within the test and is responsible of executing the script/binary. It supplies the test host and binary input arguments or test parameters. Tests can be executed synchronously or in parallel and testing may be stopped at the first failure.

Tile Calorimeter DVS Tests GUI

TileCal complex DVS tests have been implemented as Test4Class for hardware objects (e.g. each super-drawer module, EBA01 e.t.c), and defined in OKS to be loaded by the Test Manager through the GUI. The tests have been organized in trees (see Fig. 3.9) with the entire detector segment at the top and the super-drawer modules at the bottom. This way tests executed at the top of the tree are propagated down the chain, whilst maintaining modularity for instances when

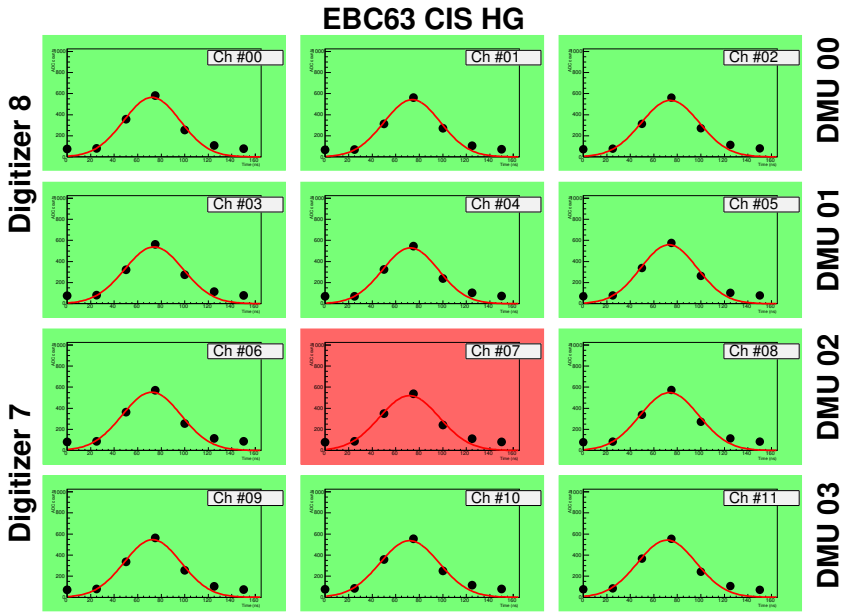


Figure 3.10: CIS HG DVS test result from IGUI. The test result shows that there is problems in the amplitude of channel 7. Log files show that the pulse amplitude, width and phase were incorrect in 100 events, and thus the channel is color coded red for bad.

tests are only required for a single super-drawer module. The tests are executed sequentially, meaning that the next test is executed after the current one has completed and has freed testing resources for use by the next object. The outcome (success or failure) of every test is communicated back to the TDAQ operator for further diagnostics. The tests also produce detailed test output log files and plots in an accessible predefined location, this log files contain in depth information on the state of the testable object. The GUI method was implemented and used during the TileCal 2017 maintenance period (early January to mid May). It was observed to provide a much quicker and easy way of running DVS tests for drawer certification after repairs.

Figure 3.10 shows a result of a high gain CIS test. A Gaussian function is fit through the samples for pulse recognition. The plots are also color coded,

green means everything is fine, and red means that something is wrong with that particular channel i.e channel 7. The log files for this test show that there was an incorrect pulse amplitude, width and phase for this channel in 100 events. Figure 3.11 shows results of a bi-gain pedestal test. The plots show that there are no noise or pedestal problems for LBA47 module. This results were consistent with those obtained from MobiDICK test-bench for this module.

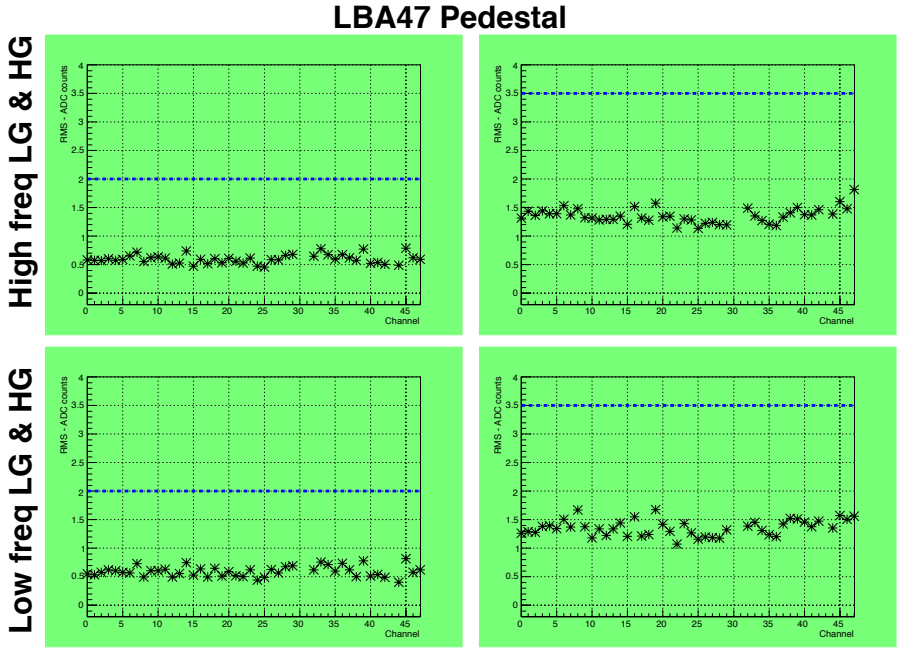


Figure 3.11: Plots showing results from DVS pedestal test for both high and low gain. Results show that noise levels are within acceptable levels for this module (LBA47).

3.6 MobiDICK test-bench

The Mobile Drawer Integrity CheckK (MobiDICK) system is a stand-alone test-bench used to verify the functionality of the Tile FE electronics [48]. it implements similar tests to DVS in an embedded system. MobiDICK is the first level test

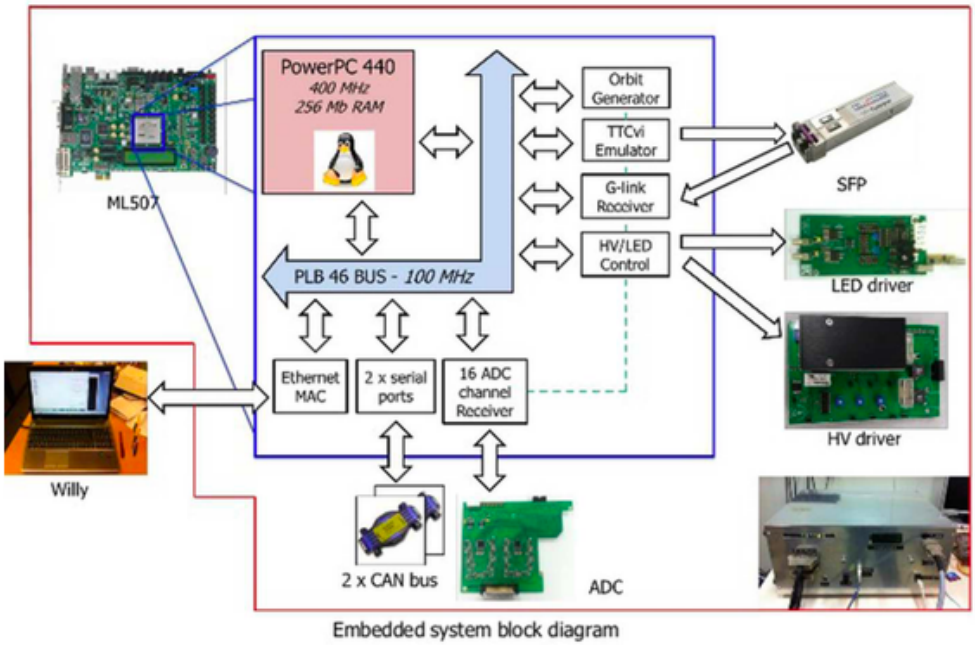


Figure 3.12: A sketch layout of the MobiDICK-4 embedded system test-bench.

after repairs, and DVS follows at the second level when module is inserted back into position and connected to the readout. Figure 3.12 shows a layout of the various components of the MobiDICK-4 test-bench currently being used at CERN. The tests performed by the MobiDICK system on the super-drawers are divided into thirteen sets (see Fig. 3.13), in the following order: CommMB, Adder, DigChk, DigShape, DigNoise, StuckBits, Integ, CommHV, DigNoiseHV, HVon, Opto, NominalHV, IntegHV, LEDon, DigShapeLED and HVoff [49]. HVon, HVoff and LEDon are not a real tests but tools to switch on/off the input HV (-830V). A brief description of each test is presented next.

- **CommMB:** This test is the most basic and is used to check the communication with the ADC-I card, the 3-in-1 cards and the motherboard TTCrx.
- **Adder:** This test checks the functionality of the analog summation cards (adders) using the 3-in-1 CIS circuit.
- **DigChk:** This test checks the integrity of the digitizers. The data integrity of a few events is checked using BCID, CRC, parity and all checks possible

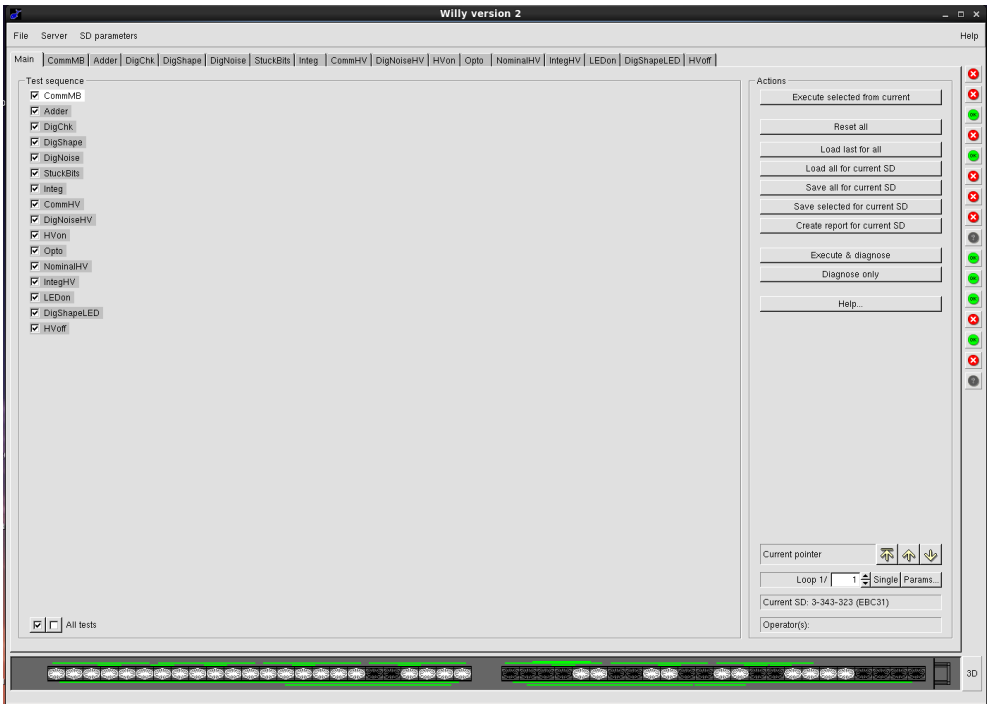


Figure 3.13: MobiDICK-4 test-bench GUI panel showing the list of all available tests.

with the header data.

- **DigShape:** This is another digitizer integrity test and the data readout, but uses the 3-in-1 CIS circuit to generate pulses which are digitized and fitted with the expected curve.
- **DigNoise:** The purpose of this test is to measure the digitizer noise and to check data integrity. A big number of events is readout at high frequency to check the data integrity (using BCID, CRC and other bits) and to measure the noise on the digitizer pedestals with HV turned off.
- **StuckBits:** The purpose of this test is to check the integrity of the data readout. The digitizers are configured to transmit different data patterns and the generated data is checked to verify stuck bits at high and low logic values.
- **Integ:** The purpose of this test is to check the linearity and noise levels of

the ADC-I, cesium system, and the charge integrator circuit of the 3-in-1 cards.

- **CommHV:** This tests the communication with the HV distribution electronics (HVmicro card, HVopto card and CANbus).
- **DigNoiseHV:** The purpose of this test is similar to the DigNoise test but with HV turned on.
- **Opto and NominalHV:** This tests check the functionality of the HV distribution electronics (HVopto, HVmicro) with HV on.
- **IntegHV:** Similar to the Integ test but with HV switched on.
- **DigShapeLED:** The purpose of this test is to check the functionality of the PMTs and the digitizers. The response of the PMTs to a pulsed LED are digitized and samples are fitted with the expected curve.

Figure 3.14 shows results obtained from the DigNoise test with MobiDICK for the LBA47 module (both high and low gains). The first 45 channels represent the LG, and the remaining 45 represent the HG signals. The results show that the digitizer pedestals and noise, and data integrity are all good. A DVS pedestal test was carried out after module was inserted back in to position and results are consistent with each other (see Fig. 3.11).

DVS tests are designed similar to MobiDICK tests, but are carried out later to assess the Tile FE electronics later on after the maintenance period. However, DVS should continue to be developed to further integrate online and offline data quality validation.

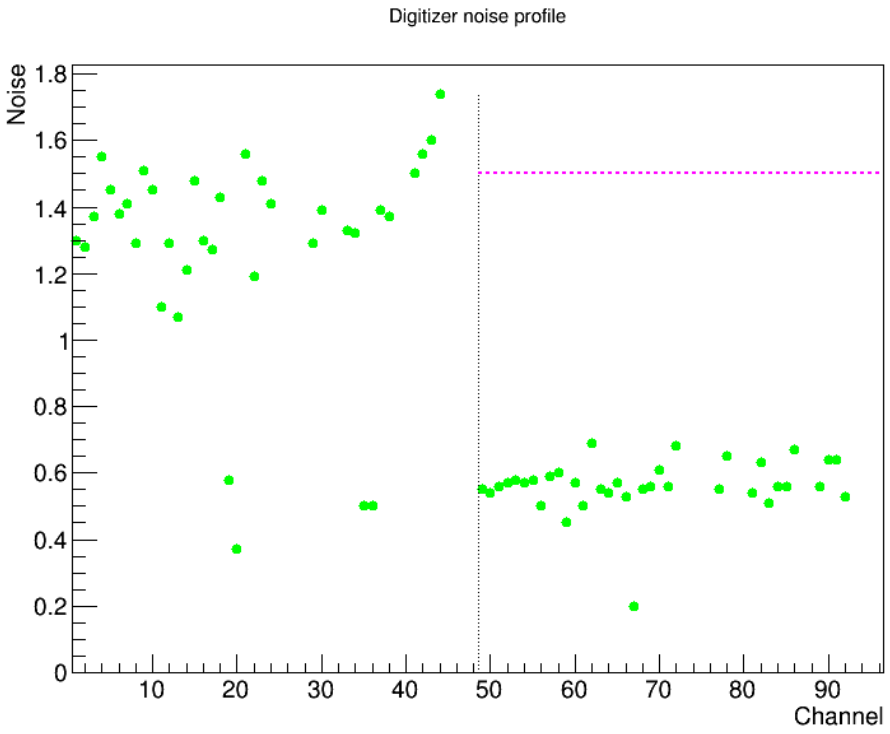


Figure 3.14: Plot showing result of readout electronics test (DigNoise) from the MobiDICK-4 test bench for LBA47 module.

Chapter 4

Tile phase-II test-beam campaigns

The HL-LHC is a proposed upgrade project called phase-II and is aimed to crank up the performance of the LHC and to increase the potential for discoveries after 2025. The objective is to increase the luminosity by a factor of 5 the current the nominal value (L = 5 x 10^{34} $cm^{-2}s^{-1}$) and to reach the design center of mass energy ($\sqrt{s}$ = 14 TeV). This will present a unique opportunity to substantially extend the mass reach in searches for many signatures of new physics, in several cases well into the multi-TeV region, and to significantly extend the study of the properties of the Higgs boson. This major increase in luminosity will result in more collisions in a given time, and thus provide a better chance to see rare processes and improve statistically marginal measurements. The large luminosity of course offers the opportunity for a wealth of physics measurements, but presents significant challenges to the detector and the TDAQ systems in the form of increased trigger rates and detector occupancy. The ATLAS TDAQ system needs to be upgraded to cope with the increased luminosity foreseen with the LHC upgrades and ATLAS detector developments. The TDAQ architectures for the ATLAS phase-II upgrade have not been fully defined yet. There are basically two

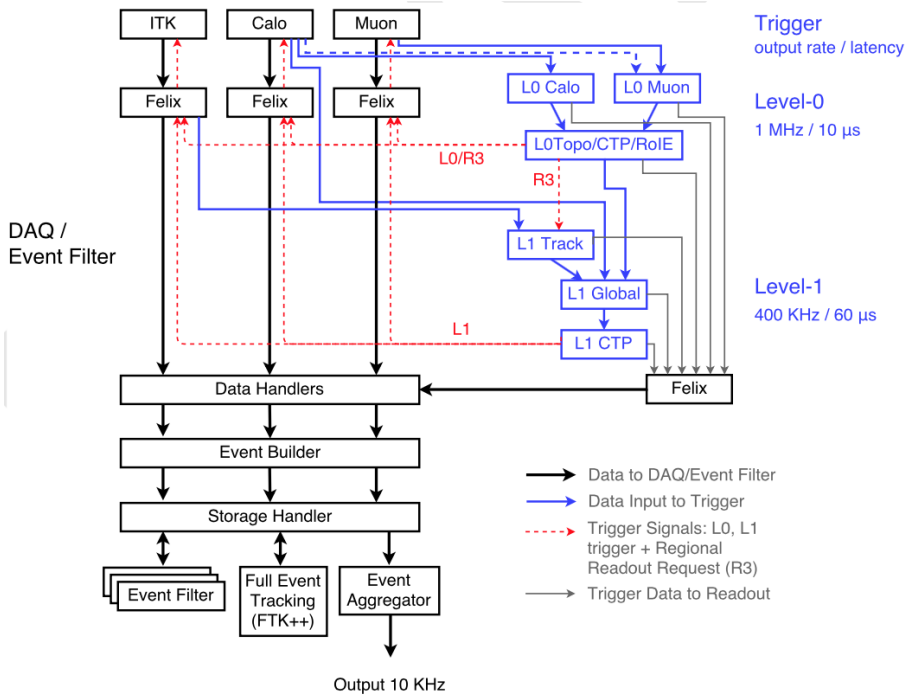


Figure 4.1: Schematic overview of the ATLAS phase-II proposed TDAQ architecture with the dual Level-0/Level-1 trigger configuration [17].

scenarios for the hardware trigger system currently under consideration, a single and a two level trigger system. Figure 4.1 represents a high level description of the ATLAS HL-LHC proposed TDAQ architecture. As already mentioned in the introduction, TileCal is planned to undergo upgrades in phase-II by completely replacing the readout electronics to cope with the HL-LHC. [50].

4.1 TileCal phase-II upgrade motivation

It is currently envisaged that the detector components (iron absorbers, scintillating tiles and optical fibers) will not be changed because they are still in good shape. An accurate study of the aging of the active detector components and the readout PMTs is being done by analyzing the evolution with time of the performance of these active elements during normal TileCal operation. Preliminary results of this study indicate that most of the PMTs could still be used in phase-

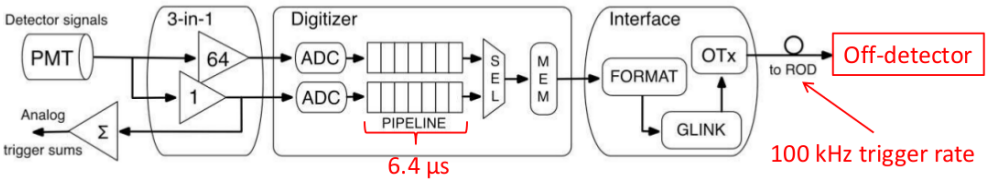


Figure 4.2: The TileCal current readout architecture [52].

II. The current readout electronics operate at a maximum rate of 100 kHz with a maximum latency of up to 3 μs and store data in 6 μs pipelines (see Fig. 4.2), it thus not compatible with the baseline trigger architecture of the HL-LHC. This mandates the replacement of the detector readout electronics to accommodate the new two-step LVL0/LVL1 architecture: the higher trigger accept rates and the extended latencies at both LVL0 and LVL1. A new TDAQ architecture is to be adopted to provide full digital calorimeter granularity at the first trigger levels. Table 4.1 shows the major differences between the present and upgrade readout systems. The upgrade BE electronics are much simpler and have no limitations like the current system. Also, redundancy and reliability are the key themes for the upgrade [17, 51].

The TileCal readout electronics are housed at large detector radius and are shielded by the calorimeter body, and this make the radiation dose requirements less critical compared to other ATLAS sub-systems. However, the large increase in the particle flux also mandates better radiation tolerant on-detector components. Total Ionizing Dose (TID) estimated for TileCal at the HL-LHC is about 24.4 krad over 10 years. The current FE components were designed to withstand a TID of 2 krad over the entire LHC lifetime. And also, most of the current components are also very old (over 10 years). Several of them have also been discontinued [17].

A new problem to face in the upgrade and operation of the ATLAS detector in the HL-LHC is the activation of the detector and accessibility. To simplify

Up Link only	Present	Upgrade
Total Available Bandwidth	200 Gbps	80 Tbps
Number of fibers	256	8192
Fiber bandwidth	800 Mbps	9,6 Gbps
Number of modules	32	32
Number of crates	4 (VME)	4 (ATCA)
Input bandwidth per board	6,4 Gbps	2,5 Tbps
Out bandwidth to DAQ per module	3,2 Gbps	40 Gbps
Out bandwidth to trigger per module	Analog front-end	˜500 Gbps

Table 4.1: The TileCal readout system in the present and phase-II upgrade architectures [51].

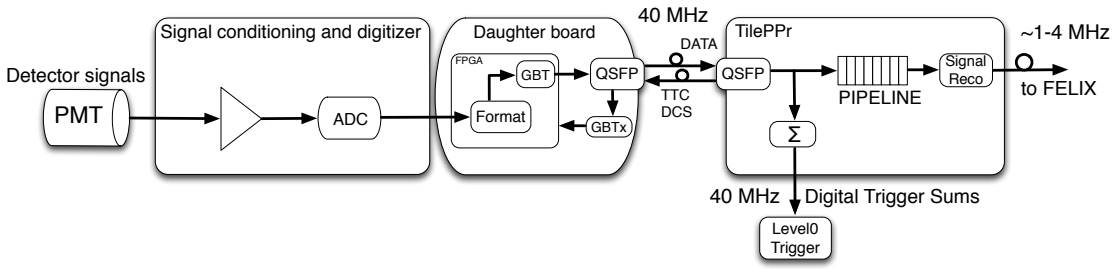


Figure 4.3: The TileCal phase-II upgrade readout architecture [53].

the manipulation, installation and maintenance, the detector FE modules have been split into 4 independent parts called mini-drawers (see Fig. 4.5). This will improve access to the electronics and will allow maintenance and operation. This will also reduce single point failures and improve reliability.

4.2 Changes and options

The proposed TileCal TDAQ architecture for phase-II is shown in Fig. 4.3. The readout is based on a continuous digitization and data transfer to the off-detector Tile PPr for very bunch crossing (40 MHz) of all readout channels. The design has fair emphasis on redundant optical transmission of the data, this means that no gain selection logic will be implemented in the FE electronics and the digitized signals of both gains will be transmitted. Pipelines and the de-randomizer

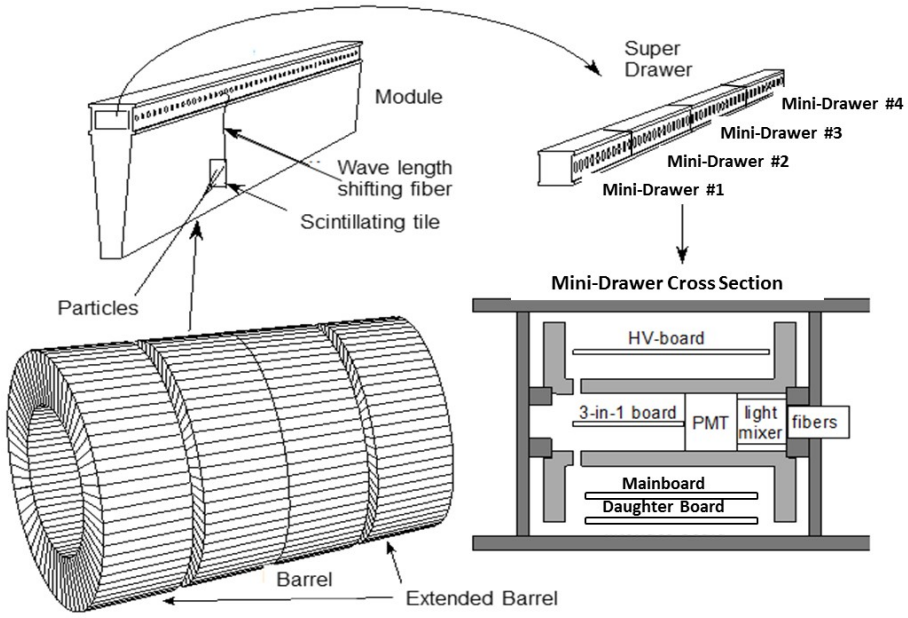


Figure 4.4: Tile Calorimeter upgrade FE drawer module configuration [17].

are implemented by the PPr units located in a very low radiation environment of USa15. The PPr will further apply energy scale calibrations as in the current RODs and prepare the LVL0/LVL1 trigger information [54].

4.2.1 Front-End Electronics

The FE readout design relies on the use of high reliability components, with a strong emphasis on radiation tolerance that satisfies the HL-LHC criteria of 10 krad over a period of 10 years. It has also been redesigned to optimize the interconnection reliability and sub-assemblies in the drawers taking into account the experience gained from the current detector. Four mini-drawers comprise a super-drawer in contrast to the current configuration of 2 drawers, and 256 super-drawers will constitute the full detector in 4 barrels of 64 wedges each (see Fig. 4.4). This particular stacking was done to improve reliability of the interconnections and to avoid single-point failures due to power distribution in particular.

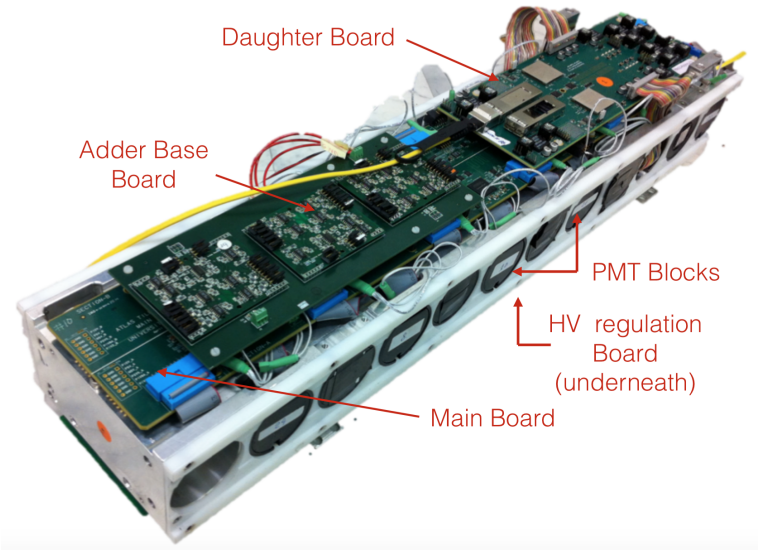
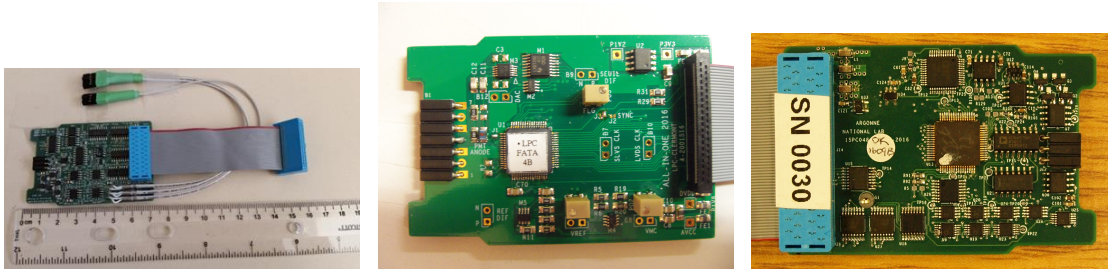


Figure 4.5: Tile Calorimeter mini-drawer and the components it comprises.

Each mini-drawer houses a total of 12 PMTs with FE amplifier cards for pulse conditioning and calibration, a main board (MB) [55] that receives PMT signals and routes them to the Daughter Board (DB) [56] which handles all communication with the BE electronics and a HV regulation board to deliver the correct HV to the PMTs. Adder boards, needed for analog trigger signals aggregation in the 3-in-1 Demonstrator, and lastly, . Figure 4.5 shows a single complete mini-drawer with the components that it comprises.

The DB is the on-detector communication interface between the TileCal FE and the counting room of USa15. The BE Tile PPr sends DCS and run control information via multiple 4.8 Gbps radiation tolerant fiber-optical links to the DBs, which in turn send readout and DCS data to the PPr via multiple 9.8 Gbps radiation tolerant fiber-optical links for redundancy [57].

As mentioned in the introduction, three options of redesigned FE cards have been proposed and studied. One of them is an optimized redesign of the of the current 3-in-1 FEB that uses state-of-the-art discrete commercially off-the-shelf



(a) 3-in-1 FEB. (b) FATALIC FEB. (c) QIE FEB.

Figure 4.6: The 3 Tile Calorimeter front-end cards under evaluation for phase-II [52].

integrated circuits. The 3-in-1 signal processing approach uses a shaper circuit to transform a PMT pulse into an easy to digitize waveform/pulse whose amplitude is proportional to the total charge of the original PMT pulse. The shaped signal is then amplified in two separate ranges and sent to 12-bit ADCs on the MB. This technology also provides a system with lower electronic noise than the present system. The new 3-in-1 system is compatible with the analog trigger and can be installed into TileCal before the HL-LHC upgrade. This option has been chosen as the main baseline option.

Another approach is the FATALIC developed by LPC in Clermont Ferrand, France, which uses shaping just like the 3-in-1 but with a different pulse. This ASIC chip is a new technology for TileCal and aims at integrating much of the 3-in-1 functionality into the FATALIC chip, this includes signal digitization. The ASIC design is based on a 130 nm CMOS process which has been already qualified in ATLAS for applications in other subsystem with much higher radiation doses [58].

The third option is the QIE ASIC developed by Argonne National Lab, USA. The QIE circuit does not shape the PMT pulse to digitize at 40 MHz. Instead, it directly integrates the PMT anode current in 25 ns intervals. This chip has been

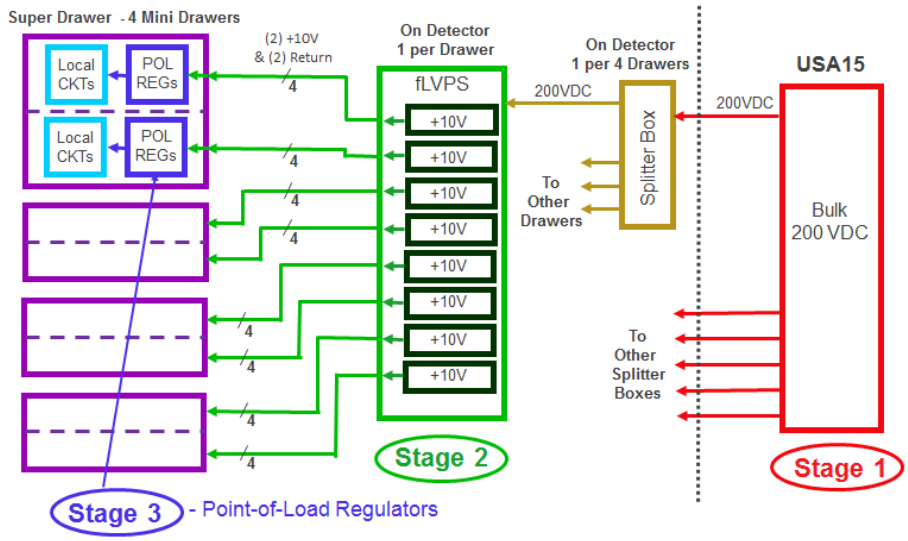


Figure 4.7: Block diagram of the 3-stage low-voltage power distribution [17].

designed to satisfy the radiation requirements tailored for TileCal. QIE offers a unique opportunity to reduce the impact of the out-of-time pileup measurements for TileCal. All the signal processing (integration and digitization) is done inside the card circuitry [59].

The voltage power distributions (LV and HV) have also been redesigned to address space constraints and concerns about efficiency and heat. To improve reliability the new LVPS will be based on a three step regulation, where the last step consists of local radiation tolerant Point Off Load (POL) regulators as shown in Fig. 4.7. And for the HVPS, 2 types of solutions have been considered, remote HV and the HV opto. The remote HV has the control and monitoring circuitry installed off-detector. This requires an individual high voltage cable from the counting room to each PMT. This architecture significantly reduces the radiation tolerance issues since the electronics are installed off-detector. And the HV Opto solution has bulk high voltage power delivered to each front-end drawer and the control and monitoring is implemented in the on-detector electronics to serve the 48 PMTs. In this case the number of long high voltage cables is reduced

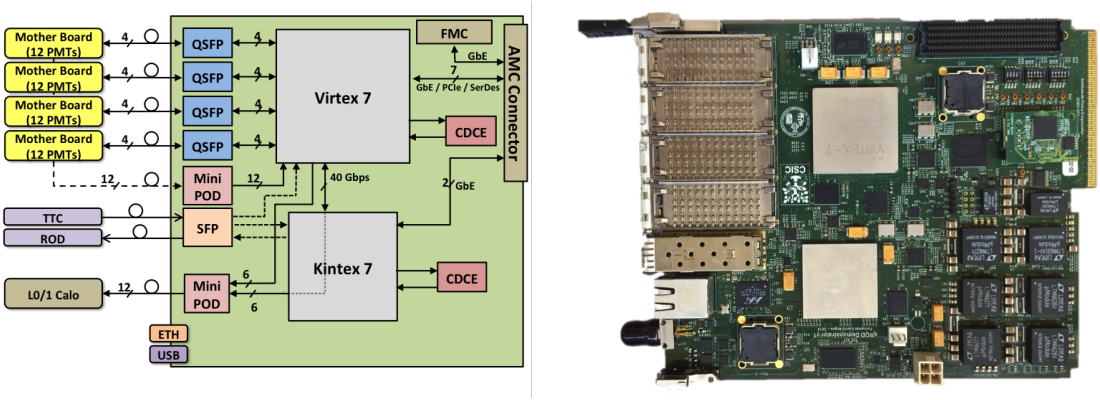


Figure 4.8: A sketch representation of the Tile PPr board (left), and the PPr AMC board (right) [60].

significantly but the radiation tolerance issues are more stringent. For yet more redundancy, it was decided to equip the mini-drawers with the two options.

4.2.2 Back-End Electronics

Figure 4.8 shows a sketch of the Tile PPr. The PPr is the core of the BE electronics system and provides benchmarks for investigating the four different parts of the upgrade system. The data is received through four optical connectors and the internal hardware transceivers located in the main FPGA. This FPGA also contains the pipeline and de-randomizer memories, the synchronization of data with TTC and the reconstruction of the events passing the LVL0/LVL1 trigger. The L1Calo preprocessor module implements the algorithms to provide digital information to the LVL0/LVL1 trigger of ATLAS. The new architecture of the read-out improves the precision and the granularity of the trigger information for the cluster and jet energy L1Calo processors. The increased granularity can be achieved in the radial direction, which would eventually allow the implementation of shower profile algorithms at LVL0/LVL1. The use of digital signals at the PPr for the LVL0/LVL1 trigger replaces the present analog LVL1 trigger preproces-

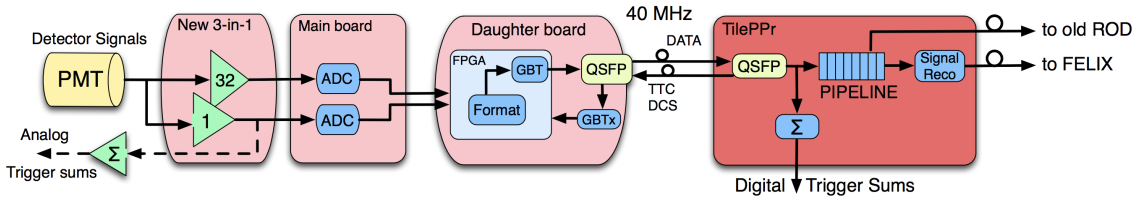


Figure 4.9: Sketch representation of the hybrid Demonstrator super-drawer.

sors. The board transmits the data accepted by the LVL0/LVL1 trigger to the ROS. In addition, the board is the BE interface with the DCS and TTC of the FE electronics [61].

4.3 Demonstrator program

The Demonstrator project aims at testing the long term performance of the upgrade system without compromising the present data taking. This is to be achieved by developing an early version of the new digital calorimeter system that is compatible with the present analog trigger, DAQ, DCS and TTC. Digital transformation will translate TTC signals into upgrade specific commands and translate upgrade outputs to a format acceptable by the present RODs. The TileCal Demonstrator is a prototype phase-II super-drawer with an additional trigger output (see Fig. 4.5). It was verified during test beams to perform according to requirements. If needed, more Demonstrator drawers could be inserted into ATLAS during one of the end of year maintenance periods. This will allow thorough testing of the major functionality of a phase-II system before full installation in phase-II [60]. Figure 4.9 shows a sketch diagram of the hybrid Demonstrator super-drawer. The data readout strategy for the demonstrator is as follows; data is readout through the PPr board which formats and transmits it to the legacy RODs for backward compatibility with current system and to the Front-End Link exchange (FELIX). More information on FELIX can be found in [62, 63].

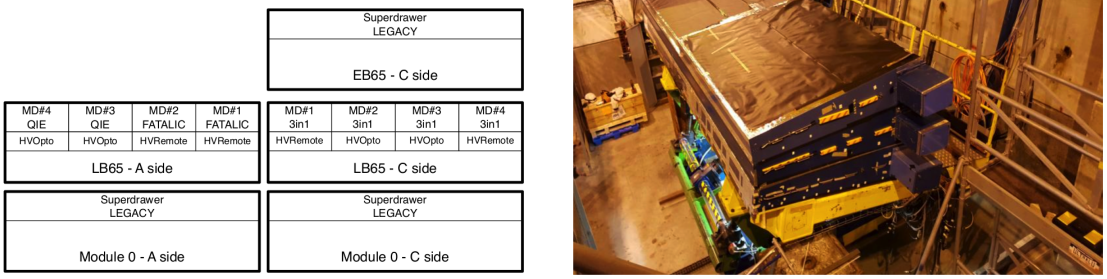


Figure 4.10: Tile Calorimeter module configuration at test beam.

4.4 Test beam campaigns

A series of test with beam setup campaigns took place between 2015 and 2017 to evaluate the phase-II upgrade electronic prototypes and to help with estimate provisions for future commissioning efforts. The primary objective is to assess the status of the Demonstrator based on the modified 3-in-1 FEB baseline option and to give some attention to QIE and the FATALIC. Several TileCal drawer modules have been equipped with upgrade specific electronics , and two other modules have been equipped with current legacy system electronics as shown in Fig. 4.10. In addition, mini-drawer prototype instrumented with the 2 HV regulation options have been produced to evaluate performance and functionality in standalone operation were integrated with the other parts of the system during this campaigns. This modules were exposed to muons, electrons and hadrons at different energies during this test beam campaigns to assess their performance. The electron beam helps with the EM scale studies, the muons are used to study the calorimeter tomography, and the hadrons for jet/E_T^{miss} performance studies. Beam instrumentation, as shown in Fig. 4.11, was installed to identify the different particles, to measure the beam position and to trigger the data acquisition synchronous to the beam. As of 2016 test beams, 3 Cherenkov counters were used to separate the protons, electrons and muons for energies below 50 GeV, and a muon hodoscope

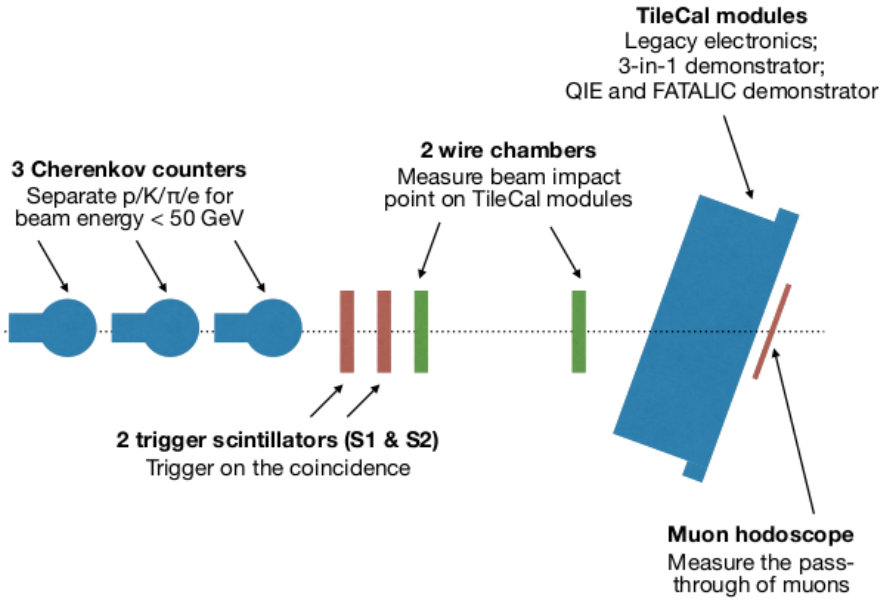


Figure 4.11: Diagram of the beam elements at the Tile Calorimeter test with beam setup.

(muon wall) located behind the modules was used to detect muons. The wire chambers are used to deduce the exact beam position in real time with respect to the modules, and the coincidences from two scintillators was used for trigger generation. The modules were mounted onto a mobile table allowing to the beam to different modules and cells at various angles.

Figure 4.12 shows the TDAQ configuration used for the tests with beam setup. The prototype PPr was used during this campaigns since it can be operated in both legacy and upgrade modes. In legacy mode, the PPr emulates the legacy FE electronics by receiving data samples at 40 MHz and stores it in pipeline memories and packs with the legacy L1A signals to be transmitted to the RODs through optical links. The ROD performs further processing and transmits to the ROS, and finally to the Event Builder which saves the data on disk. Synchronization of the Demonstrator data with the legacy system data is achieved using the clock and trigger information distributed by the legacy TTC modules. The PPr implements a trigger identification algorithm to the data packets and synchronized the

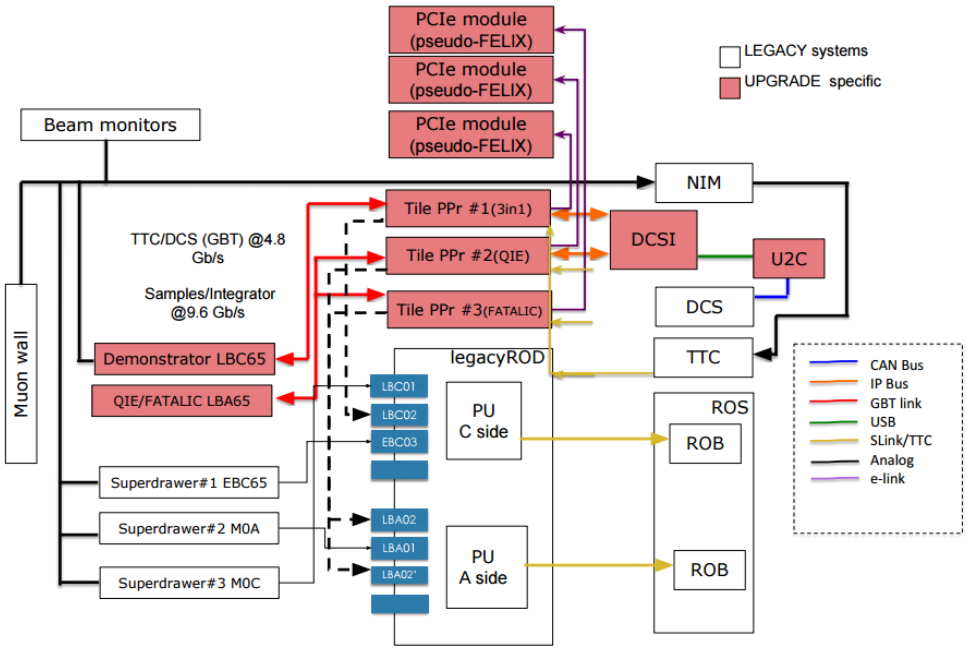


Figure 4.12: TileCal DAQ configuration at test beam.

two systems.

In upgrade mode, the PPr transfers the L1A data through dedicated high speed optical links to the FELIX system which then saves the data on local disk for offline reconstruction and analysis. There is a PPr specific package called the PPrInterface used for standalone system verification tests. The 3-in-1 Demonstrator was readout using both upgrade and legacy readouts, whilst the QIE and FATALIC are only readout using the upgrade specific FELIX readout [53].

There is new hardware components available as of the 2016 test-beams, this include the DB version 4 which uses the new GBTx (GigaBit Transceiver) chip [64] instead of the CDCE chip for clock recovery and remote FPGA programming [57, 65]. A couple of issues relating to the stability of the high-speed data links and the clock distribution circuitry have been experienced with the DB version 4. DB version 5 is under development aiming at fixing this issues and to utilize newer

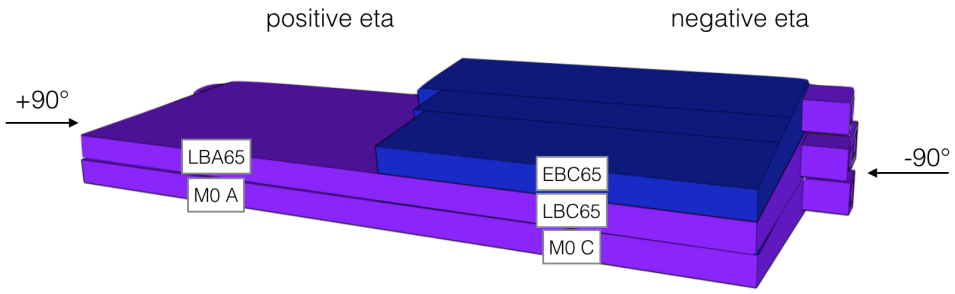


Figure 4.13: TileCal module stacking on the table with respect to beam direction.

FPGAs, this will be tested in the upcoming future test beam campaign. There is also a new MB version 2 which provides a frame and bit clock for ADC de-serialization, correct channel orientation and new 3-in-1 cards. There is a new PPr prototype with no auxiliary boards and operates at 40.08 MHz with optimized firmware versions, and the PCIe (Peripheral Component Interconnect Express) module for readout to the basic pseudo-FELIX through the PCIe-GBT link data format. And finally, there is a new mobile ^{137}Cs calibration unit to perform in-situ Cesium calibrations. The 3 FE options were all operated in parallel for the entire test-beam period. New software for the TDAQ and the DCS to improve the communication through IPBus with PPr was developed and provides; improved PPr memory stability for multiple application access, monitoring the link status and FE option configuration at the beginning of every data taking session. The DCS software has been updated to work with the IPBus OPC server [66] that provides better HV and temperature monitoring. Calibration runs (CIS, CIS mono, Ped and LED) have been successfully integrated into the TDAQ system as well [3].

4.5 Results

Figure 4.13 shows the position of the modules on the table with respect to the direction of the beam. The new 3-in-1 systems were calibrated and evaluated

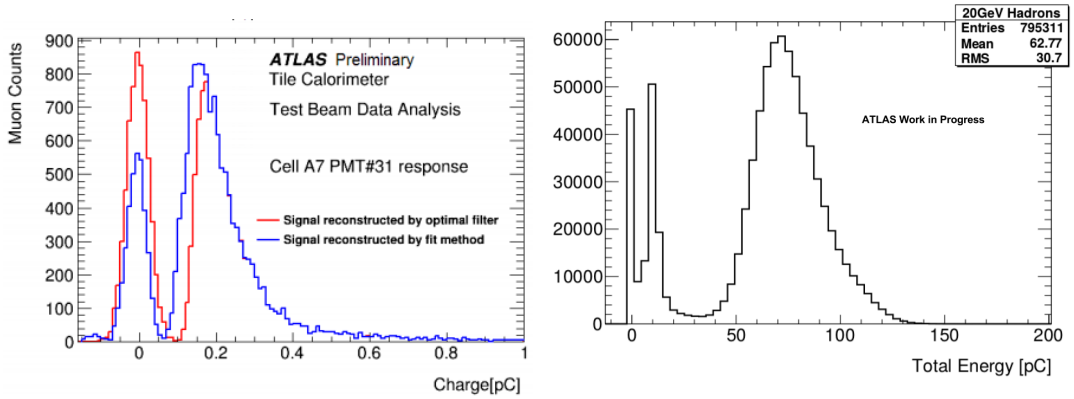


Figure 4.14: Measurements of the 3-in 1 system energy response to a 150 GeV muon beam (left), and to a 20 GeV hadron beam (right) [68]. For the muon plot, the standard optimal filter was used and was compared to another fit method, a specific ratio computation was used and the peak is observed at 0.2 as expected. For the hadron plot, the EM scale (1.05 pC/GeV) nominal gain was calibrated to a factor of 5.

with test beams electrons, muons and hadrons in 2015, 2016 and 2017. The results speak of superior system compared to the current Run-2 system. The data taken from 2016 test beam has been analyzed offline. The results allow to EM scale calibration of the new electronics. Muon signals are very useful in evaluating the electronics performance in terms of noise since their signals are very close to electronics noise values. The left hand side plot of figure 4.14 shows analysis results from the standard optimal filter method at 5 ADC counts compared with another fit method at 3.2 ADC counts for a 150 GeV muon beam hitting the 3-in-1 Demonstrator at -90 degrees, a full description of this results is available in [67]. The peak at zero represents noise events reconstructed without iterations. The standard optimal filter and fit method give similar results for good signals above the noise thresholds.

Hadron studies are used for studying the jet/E_T^{miss} performance. The plot on the right hand side of figure 4.14 shows the energy distribution for a 20 GeV hadron beam with the EM scale increased by a factor of 5. This was only done for

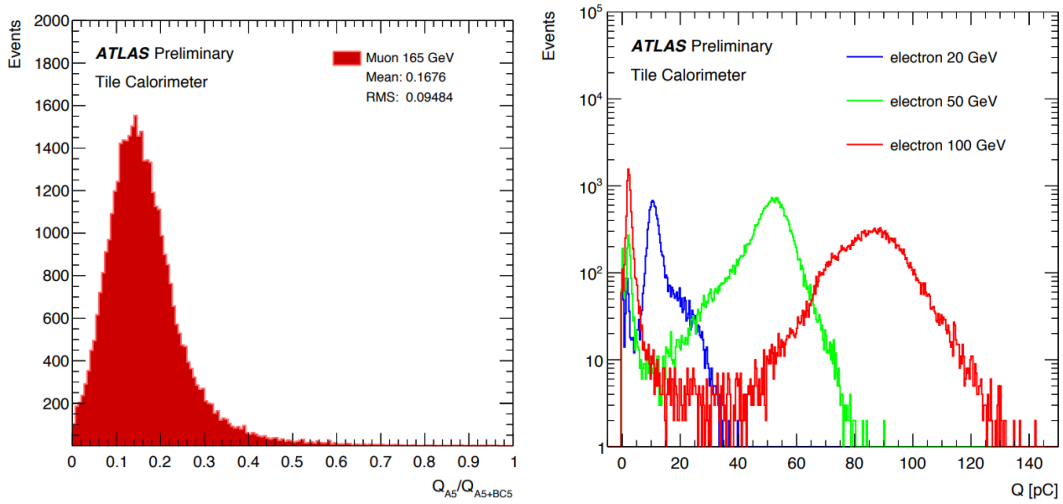


Figure 4.15: Energy response to 165 GeV muon beam (left) and to 20/50/100 GeV electron beam (right) measured by the FATALIC revision 5 chip. For the muon plot, a specific ratio computation was used and the peak is observed at 0.2 as expected [68].

the 3-in-1 option in the June 2017 test beam campaign to investigate the EM scale calibration with a high signal to background ratio. Due to the non-compensating nature of the TileCal, the response of hadrons is always lower than of particles interacting electromagnetically. This lost energy is due to the energy being used in breaking the nucleus of the material and production of secondary neutrons and neutrinos which escape the calorimeter volume.

The FATALIC system did not participate in the 2015 test beam campaign, it was only calibrated and evaluated with test beam hadrons, muons and electrons in 2016 and 2017 test beam campaigns. The results also speak of a strong and mature upgrade system. Figure 4.15 shows results observed from the 2017 June test beam campaign for the FATALIC system, on the left is an energy response plot to a 165 GeV muon beam, and on the right is an energy response to 20/50/100 GeV electron beam. The energy is calculated as the reconstructed signal in two calorimeter towers (cells A/BC[4] + A/BC[5]). The plots show the ratio of the energy in A5 compared to the sum of energy in A5 and BC5. Energy reconstruc-

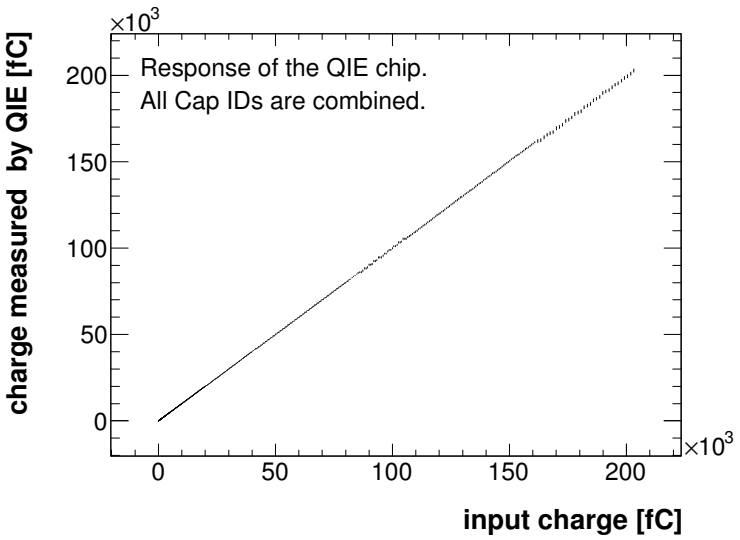


Figure 4.16: QIE system linearity scan form standard charge injection tests.

tion is done using a Flat Filtering algorithm [69]. We expect to see 20% of the energy in A5 over the total energy. The system performs well within simulated specifications. No hadron studies were done for the FATALIC system in the 2017 test beam campaign.

Figure 4.16 shows linearity scan results of the QIE system from standard charge injection tests, there is a linear correlation between the injected and measured charge. The correlation indicates that the readout was observing energetic electrons, muons and hadrons and not some random noise. The QIE system was also calibrated and evaluated with test beam hadrons, muons and electrons in 2016 and 2017. Figure 4.17 shows energy distribution plots for a 50 GeV electron beam (right) and a 200 GeV muon beam (right). The performance of the system is well within simulated specifications that show a consistent correlation between the energy measurement and the EM calibration scale of 1.05 pC/GeV.

TileCal upgrades will happen during the phase-II upgrade of ATLAS and integration efforts are progressing well with the goal of test beams to do performance

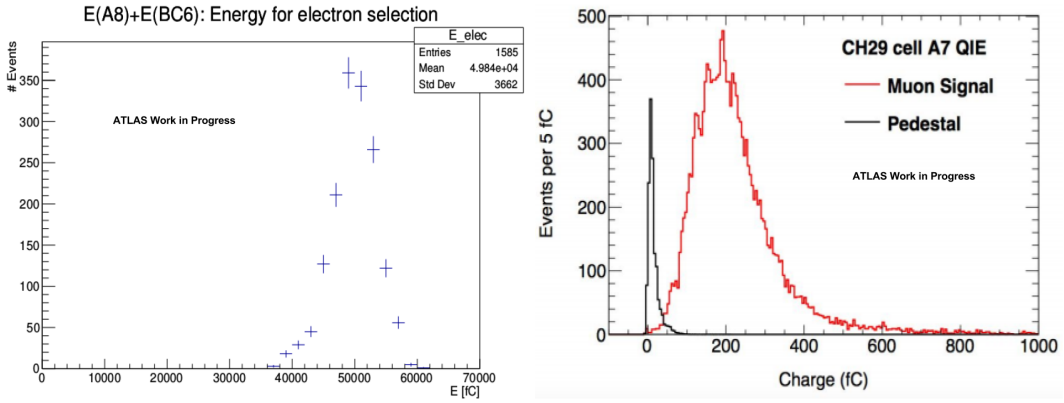


Figure 4.17: QIE system energy distribution plots for a 50 GeV electron beam (left) and a 200 GeV muon beam (right).

analysis for the 2017 FE option down-selection, and also to help with the estimations of future commissioning efforts. The reliability and stability of the system has been visibly improved with respect to the 2015 test beam. The Demonstrator analog trigger signals output has been integrated successfully into the TDAQ infrastructure for the commissioning of the hybrid Demonstrator. The FE and HV option final selection process has been defined based on extensive comparison of the performances and other criteria. The TileCal community plans to complete the R&D and make a decision by the end of summer 2017. Another test beam session has been planned for September 2017 with the primary objective of testing the maturity of the Demonstrator for insertion into ATLAS, to improve understanding of the physics performance of the current system, and to better understand the calorimeter's response to low energy hadrons and muons.

4.6 Front-End option selection criteria

The criteria for the FEB option down-selection has been set, and to name a few; the smallest charge the system must be able to resolve is 200 fC with a statistical significance of 3 sigma. The digital precision over the full dynamic range of the electronics is 100,000:1, or approximately 17 bits. Multiple ranges are acceptable,

provided that they have a minimum of 5 bits of overlap, referenced to the next smallest scale. The linearity of the system, including the electronics readout and the signal reconstruction, should be at most 1% over the full dynamic range defined as [1fC, 800 pC]. In terms of a single pulse precision, the electronics shall provide means for measuring the time of arrival of the signal from the PMT to an accuracy of at most 1 ns per channel for a channel above 10 MeV. The reference clock provided to the FE electronics shall be 40.08 MHz. The FE electronics shall produce (at least) one word of output data every 25 ns. A means for performing CIS directly into the preamplifier shall be provided. A means for a slow integrator readout shall be provided. And the foremost important, the FE electronics must be tolerant to the expected radiation levels throughout the lifetime of the HL-LHC.

Chapter 5

Conclusions

The TileCal Online software is the set of TDAQ software used for the operation of the Tile Calorimeter. It is built on top of the ATLAS TDAQ software, following its conventions, tools and policies. ATLAS relies on multiple components for building its software, the use of simple scripts or Makefiles without a proper build system would result in very unmanageably fast environments. Software packages need to be adequately built using the least amount of resources and by just providing a few lines of reasonably simple configurations. CMT was the software configuration management tool adopted for many years to handle the process of compiling and deploying ATLAS software. However, the wide adoption of nightly build projects in ATLAS has made it clear that CMT will no longer be capable of handling the ATLAS code base. ATLAS has now adopted the open source CMake tool chain that is supported that is supported by a large community for its next software build system since it is in essence like an optimized version of CMT. CMake design is enhanced to parallelize software builds much better and also provides much faster and simpler release deployment through relocatable RPMs. In parallel to CMake adoption, a new modern software revision control tool called Git was also adopted by ATLAS since SVN support is planned to be discontinued after Long Shutdown 2 in 2019. The ATLAS TDAQ projects have been migrated

from CMT to CMake and a housed in Git software repositories. TileCal Online software packages have been migrated by the author following ATLAS new code management tools. The outcomes were discussed in several meetings to the TileCal community, and this is now used as the latest production for the operation of ATLAS in a successful way.

During the maintenance of the FE electronics one has to quickly assess their state, first by confirming existing problems, and secondly by assessing the validity of the repairs. High-precision DVS tests are available for TileCal (that can be run) from the command line using two separate programs executed on separate computers. This is not efficient and is mostly understood by TileCal DAQ experts. Describing the list of tests and options in a configuration database will allow the users to run a complete suite of tests from a graphical user interface with detailed presentation of the results. A wrapper way to start this complex tests has been implemented by the author and allows simplifying the DVS configuration database for drawer objects. The high precision DVS tests used in the DQ assessment of the front-end modules after the maintenance periods, has been re-implemented in a graphical form into the DVS GUI, which is more intuitive to use by non DAQ experts. This was used during the maintenance period by experts in the ATLAS control room to quickly assess the status of repairs. The results obtained from the tests were similar to those observed from MobiDICK. Sometimes after a drawer repair, negative feedback comes one day later from the offline team about specific errors that both DVS and MobiDICK are not designed to detect. More DVS tests should be implemented to be able to improve the quality assurance procedure after the repairs. In particular, a stuck bits test should be implemented which is currently not available in DVS but it is in MobiDICK.

The High Luminosity LHC project will increase the luminosity by an order at least 5-7 times beyond the Run 2 nominal luminosity (L = 5 x 10^{34} $cm^{-2}s^{-1}$)

in order to reach the design center of mass energy ($\sqrt{s}$ = 14 TeV). The ATLAS trigger and data acquisition architecture will undergo upgrades to cope with the High Luminosity LHC. TileCal will also undergo upgrades following ATLAS developments. TileCal Demonstrator modules have been instrumented with initial phase-II upgrade electronic prototypes and assessed with beam setup at the CERN beam facilities during 2015, 2016 and 2017. Data was recorded from the 3 different front-end amplifier cards, i.e. modified 3-in-1, QIE and FATALIC. The CIS and LED system calibration tests have been successfully integrated into the TDAQ with PPr through the IPBus hub, and this is being used frequently during non-beam periods to monitor the system stability. The readout of analog trigger signals was also implemented for the 3-in-1 Demonstrator prototype and integrated into the test with beam setup partition. The online monitoring infrastructure has also been successfully into the TDAQ using the following strategy; write the data received via FELIX into a sequence of files using standard ATLAS event format, prepare the software to read and reconstruct such data, and use most part of online monitoring infrastructure already used for monitoring legacy drawers. Preliminary results speak of a strong, efficient and mature upgrade system. The operation of the Demonstrators and data analysis have been used to gain experience and identify weak points in the system. The tests with beam will continue to test the maturity of the Demonstrator for insertion into the real ATLAS detector and to improve understanding of the physics performance of the current system. This will be followed by the production and installation of the new system during the LHC Long Shutdown scheduled for 2024-2025.

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