converter. The sample and hold requires a pulse width with a minimum duration of 1 micro second, and the analogue-to-digital converter's start convert signal is the trailing edge of this convert pulse.

Depending on the size of the signal, the peak detector can produce anything between one and four peak detected pulses, each of which can be used to operate a sample-and-hold, and the analogue-to-digital converter.

To facilitate this, the peak detected signals are combined, and the leading edge used to fire a mono-stable, the output pulse of which controls the sampling of the signal, and starts the conversion. The end of convert pulse is then used to write the converter output into a buffer.

The next problem which must be touched upon is that a single peak detector is monodirectional, that is, two separate peak detectors must be used for each channel, one for the positive and another for the negative part of the signal. This means that the channels must be split and all the circuitry following the input amplifier must be duplicated to allow the processing of both positive and negative signals. The block diagram of the system as it would appear thusfar is that shown in Figure 8.4.

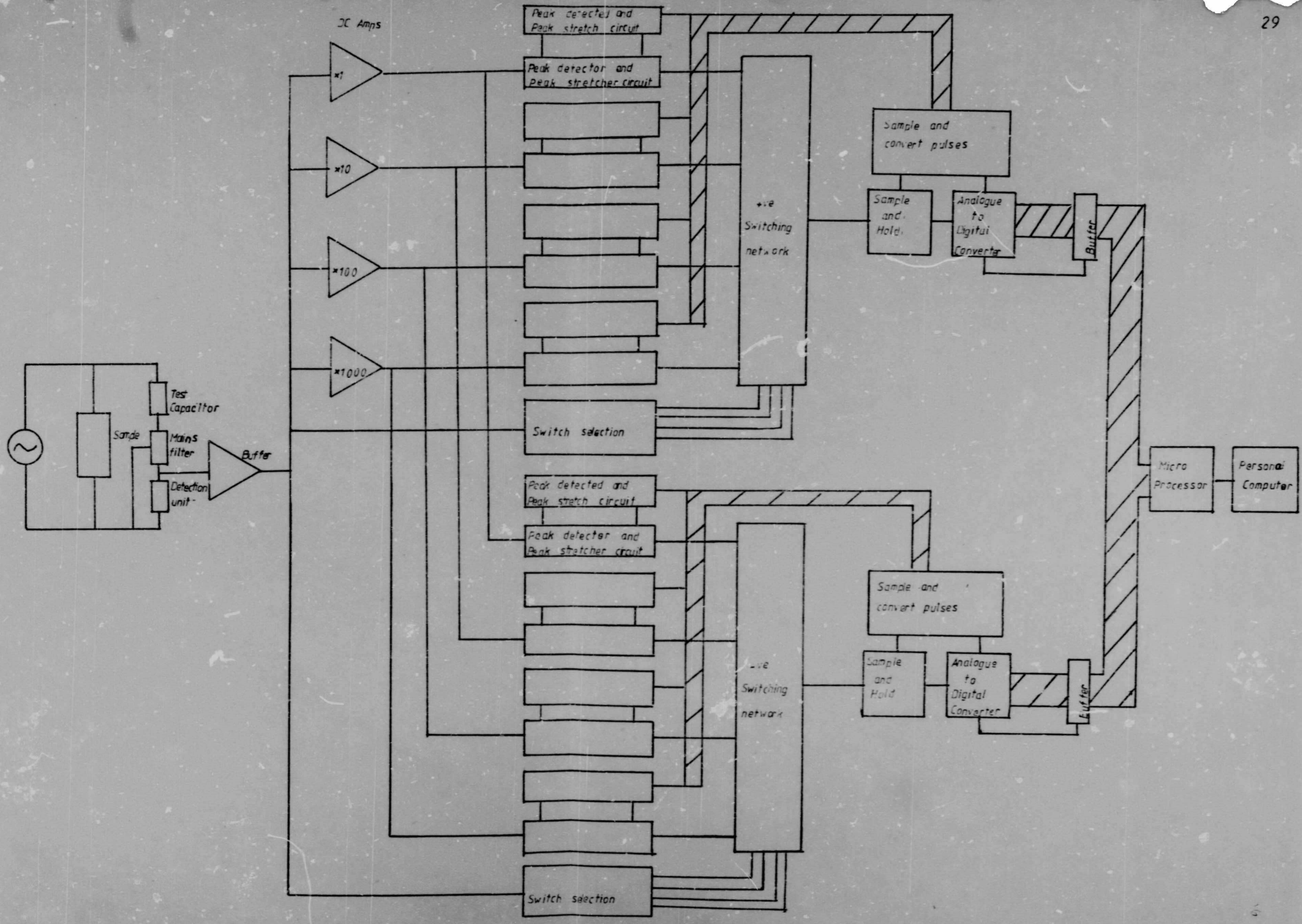

FIGURE 8.4 SYSTEM TO HANDLE BOTH POSITIVE AND NEGATIVE SIGNALS

So far the system will do the following:

a. Filter the power frequency signal, leaving only partial discharges.

b. Produce a decaying sine wave of low enough frequency to be detected by the present technology of linear electronics.

c. Detect the peak value of the signal in the range 1mV-to-10V.

d. Convert this peak value to digital form and store this value in a buffer memory.

Next the difference between the peak values have to be determined. between the peak values. The system as it stands is unable to discriminate between signals of equal magnitude within the four amplification ranges. To discriminate between these, an indication of the amplification range must be passed to the microprocessor. A four bit representation of the multiplication factor is used as follows:

1110 = Multiply by 1000
1101 = Multiply by 100
1011 = Multiply by 10
0111 = Multiply by 1

Thus the bit representation of the data which is passed to the microprocessor is as follows:

MULTIPLICATION FACTOR DATA

[ ][ ][ ][ ] [ ][ ][ ][ ][ ][ ][ ][ ]

Because of this the resolution for each range is as follows:

For the 1-to-10mV range the resolution is 80 micro Volts.

For the 10-to-100mV range the resolution is 800 micro Volts.

For the 100mV-to-1V range the resolution is 8mV.

For the 1-to-10V range the resolution is 80mV.

For each of the above cases the resolution is within one percent of full range deviation in all cases. The block diagram representing this is shown in Figure 8.5.

All that remains is to detect the time of occurrence of the discharge. In order to do this the clock information is written into memory buffers with exactly the same pulse which writes the analogue-to-digital converter and multiplication factor information.

The clock has been designed to carry out the following functions:

a. Increment the count of the number of mains cycles which have passed from the time of the start of the execution of the program.

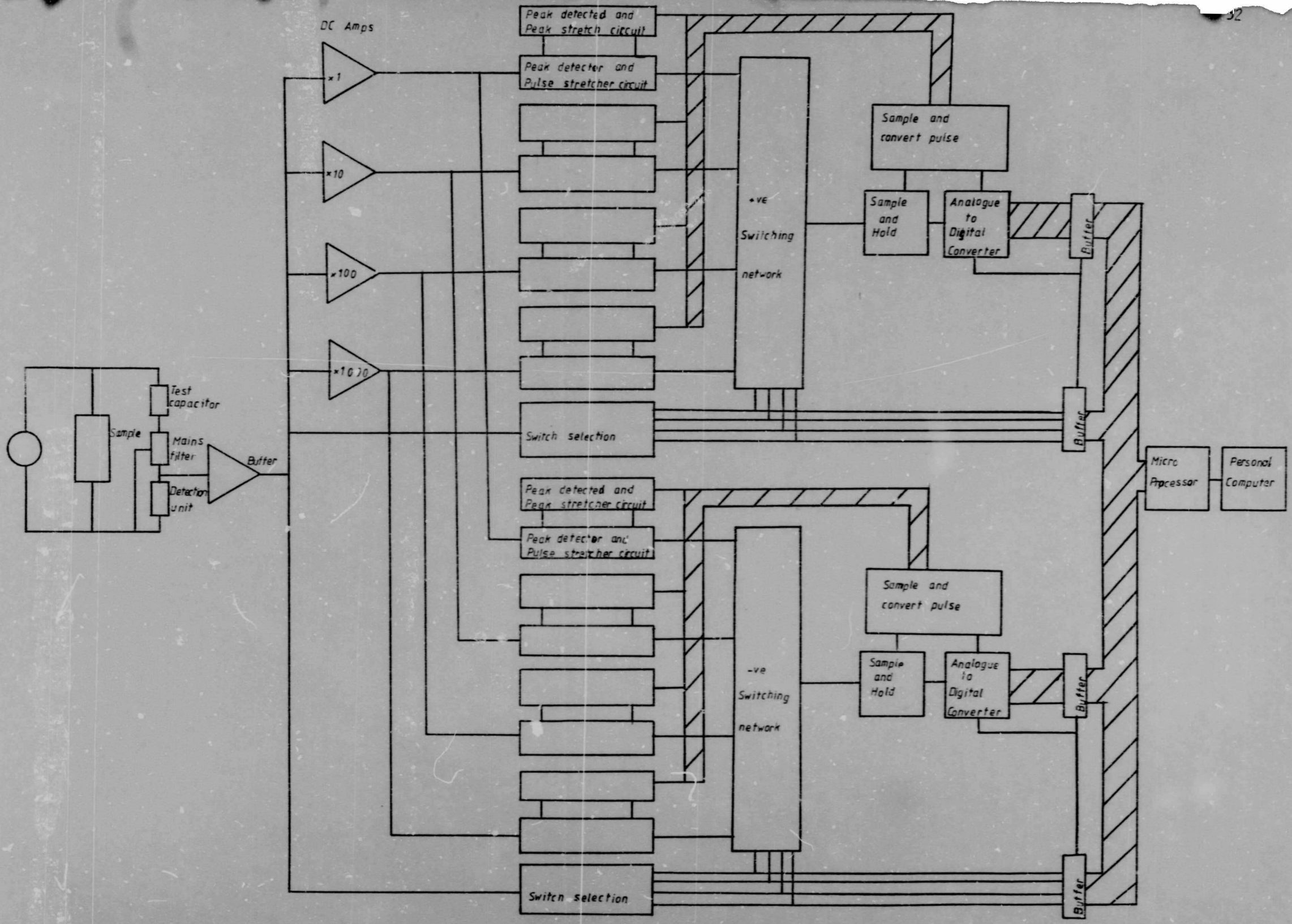

FIGURE 8.5 SYSTEM WITH MULTIPLICATION INFORMATION

b. To determine the fraction of the present mains cycle which has passed from the zero crossing on the positive slope of the mains waveform.

This is achieved by using two 16-bit counters, one with an increment pulse derived as the mains frequency passes through zero from negative to positive, while the other is given by a 40KHz oscillator.

The counter which provides the fraction of the present mains cycle is reset for each new mains cycle. In this way the occurrence of a partial discharge can be localised to 25 micro second divisions, and as this is the time it takes for the microprocessor to run the data handling program determining the time resolution of the device. The entire block diagram for the system is shown in Figure 8.6.

8.1 Resetting the peak detector

A peak detector is designed to detect peaks and hold the highest value, which means that if a peak of greater magnitude is followed by a peak of lesser magnitude, the peak of greater magnitude will only be detected. This is because the hold capacitor of the peak detector circuit remains charged for an extremely long time. To facilitate the detection of each peak the capacitor must

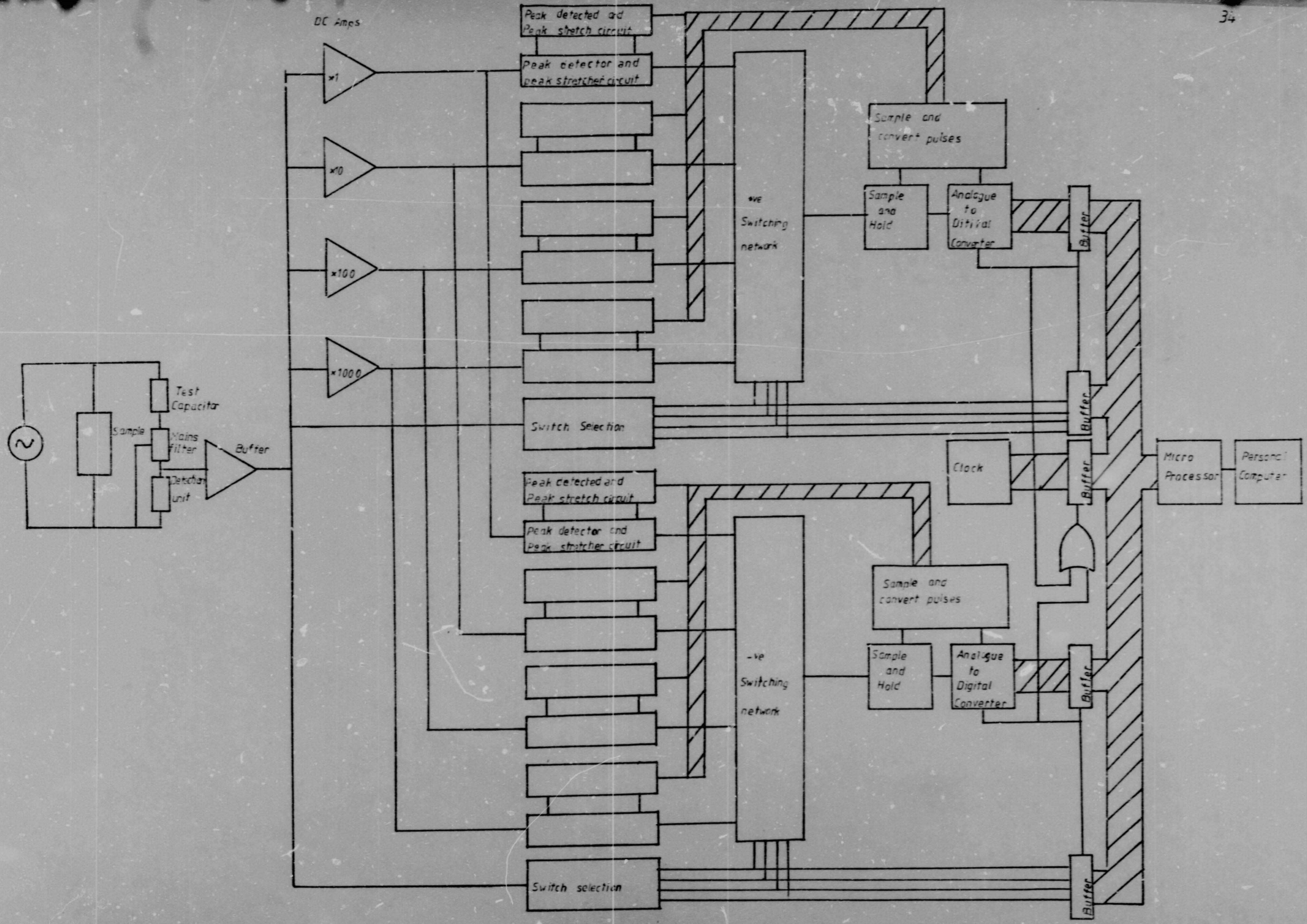

FIGURE 8.6 FULL BLOCK DIAGRAM

be discharged after each peak has been detected by the sample-and-hold. To allow the peak to be detected and sampled, the discharge-pulse occurs at least 4 micro seconds after the peak has been detected. This is shown in Figure 8.7.

8.2 Isolation of the peak from the overshoots:

As can be seen from Figure 8.7, all peaks are detected by the peak detector. The signal consists of a peak followed by two overshoots, and all of these will be written into memory, wasting memory space. Software could be written to remove the unwanted peaks from the final printout, but this is both complex and a waste of processing time. Two techniques are used to eliminate the two unwanted peaks.

Referring to Figure 7.1 it can be seen that the signal is not a simple decaying sine wave but one which has an increasing time between zero crossings. The initial peak has a decay time of approximately 2 micro seconds, the next one 15 micro seconds and the last 23 micro seconds.

To remove the first overshoot, the circuit is blanked for 20 micro seconds after the initial peak is detected. It is possible to do this because the data aquisition program takes 25 micro seconds to run, and during this

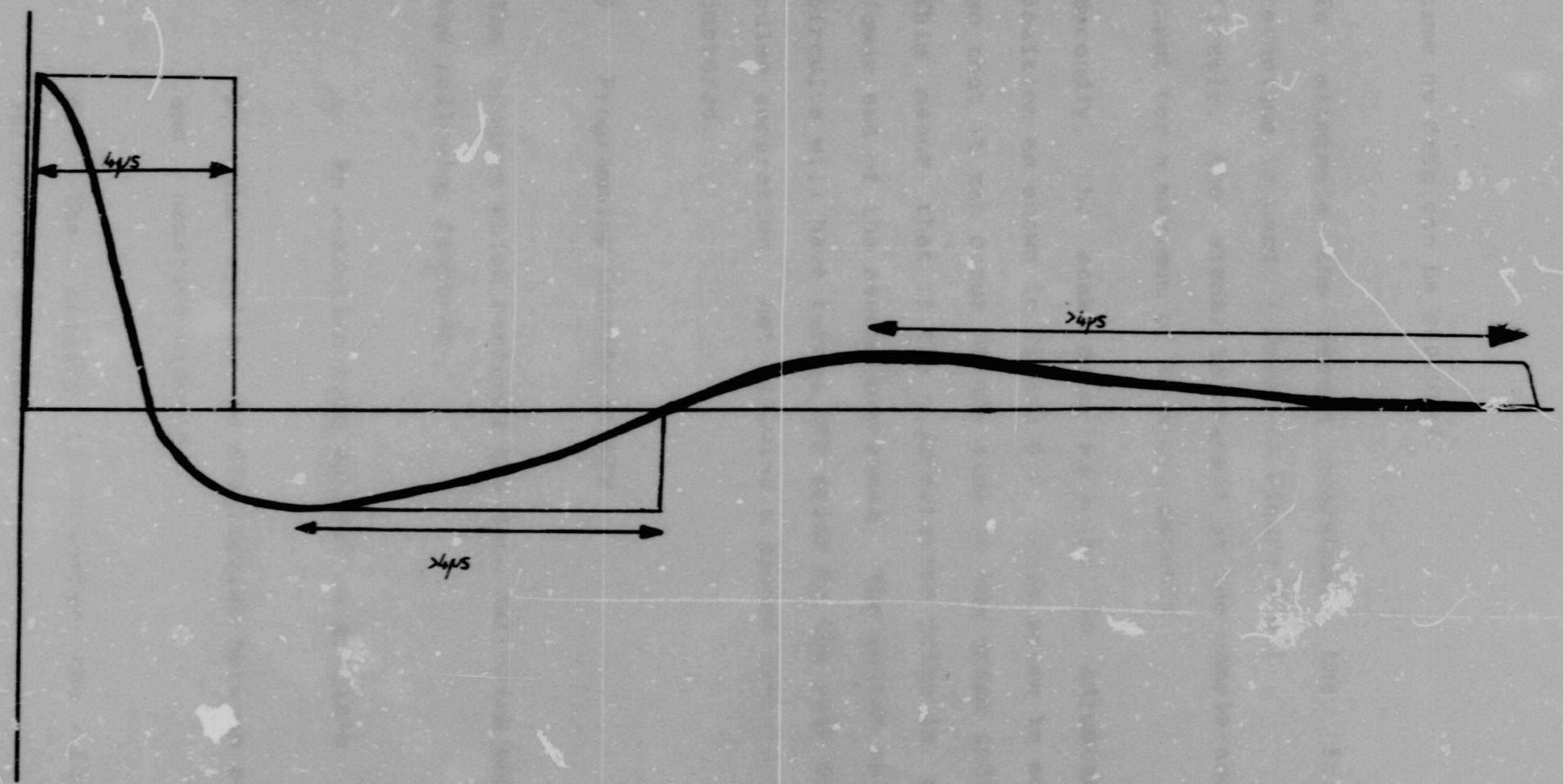

Figure 8.7 Reset times of the input signal

time no data can be captured.

To eliminate the second overshoot the following technique is used: (Refer to Figure 8.8)
Firstly, the signal is present at the sample-and-hold input for a minimum of 10 micro seconds.

Secondly, the peak detected pulse is adjustable in position as shown in Figure 8.8, this pulse is adjusted so that it can occur at any time in the areas indicated. This means that if the peak-detected pulse is at the lower end of the second overshoot, the switch selection circuits will have turned off prior to the peak detected pulse generation, not allowing a second overshoot to be captured.

9 Programming Considerations

The program which performs the data gathering must have the following features:

a. An execution time as fast as possible.

b. The ability to distinguish between positive and negative signals.

c. The ability to transfer the following information to memory:

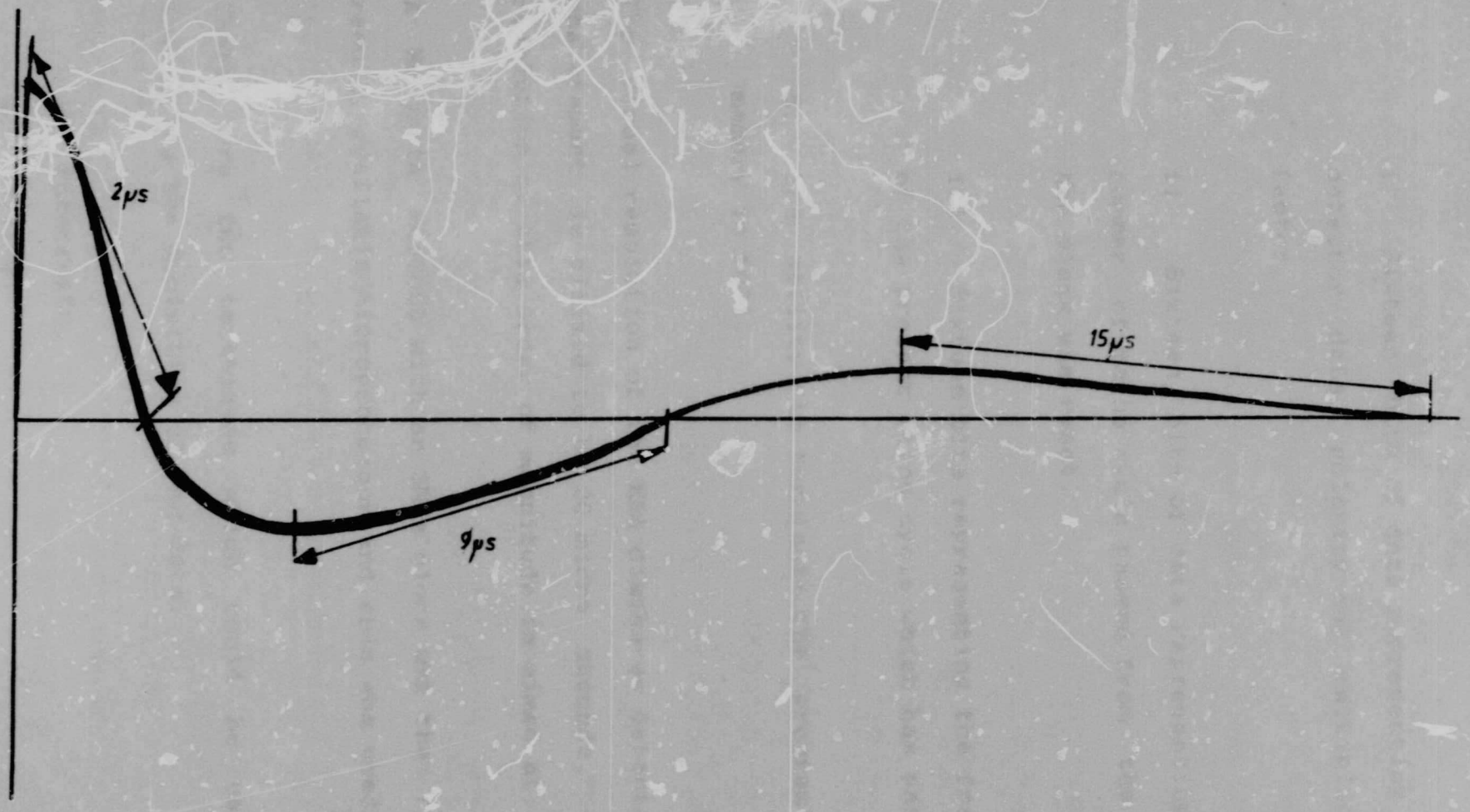

Figure 8.8 Decay times for the input signal

i. Sixteen bits of data representing peak detector data, polarity and multiplication factor.

ii. Sixteen bits of data representing the number of mains cycle passed from the time the clock was reset.

iii. Sixteen bits representing the fraction of the present mains cycle which has passed.

d. The ability to terminate the program when memory is full.

The visual resolution of the ERA discharge detector for measurement is claimed to be 20 micro seconds, and a resolution of this order of magnitude is aimed at.

A Motorola MC68000 with an 8MHz clock was the fastest readily available microprocessor and this was used.

There are two techniques which could be used for initiating the aquisition of new data:

a. Interrupts.
b. Polling.

With an interrupt routine the microprocessor's interrupt line is toggled and the processor is forced to stop whatever function it is performing at the time, and to jump to an interrupt handling routine. The use of interrupts in this application was problematic due to the fact that it takes between 20 to 30 micro seconds to service the interrupts and to execute the interrupt routine. This means that with this method it would take between 40 and 50 micro seconds to write a block of data to memory.

In polling, the microprocessor continually reads a data location and, when this alters, it jumps into the data gathering routine. The advantage of this method is that it is very fast, as the polling routine only takes a couple of micro seconds to run. There is a possible drawback to the polling approach, however, and this is that, if two consecutive discharges are of identical value, the microprocessor will not detect the second discharge as the data location will then be updated with the identical value, and thus no change can be detected!

The probability of this happening is naturally small, as tests using a test charge generator, which produced discrepancies of greater than +/- one percent from the mean, showed. If under laboratory conditions a test