Effect of Dielectric Thickness on the Bandwidth of Planar Transformers

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A dissertation submitted to the Faculty of Engineering and the Built Environment, University of the Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Master of Science in Engineering.

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Declaration of Authorship

I, Hyma Harish VALLABHAPURAPU, declare that this dissertation titled, "Effect of Dielectric Thickness on the Bandwidth of Planar Transformers" is my own, unaided work, except where otherwise acknowledged. It is being submitted for the degree of Master of Science in Engineering to the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination to any other university.

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Date:

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"You have the right to work, but never to the fruit of work. You should never engage in action for the sake of reward. Nor should you long for inaction."

– Bhagavad Gita

Abstract

This research has considered an idealistic non-interleaved planar transformer wherein only the electromagnetic parasitic capacitive and inductive elements arising out of the transformer geometry are taken into account, without considering material limitations. A suitable model for the planar transformer is used to analyse its frequency and power transfer characteristics; this model was validated by three dimensional electromagnetic simulations of various planar transformer structures in FEKO simulation software. The capacitive and inductive parasitics in this model have been found to be functions of the dielectric thickness.

The theoretical bandwidth for the planar transformer is defined in this research as a function of dielectric thickness. The effect of dielectric thickness of the transformer windings on the bandwidth of the transformer is analysed, based on the premise that the inherent parasitic capacitive and inductive elements would affect the transfer characteristics of the transformer. Upon conclusion of this analysis, it is found that the dielectric thickness of a planar transformer can be optimised such as to present an optimised bandwidth. A closed form analytic expression for the optimum dielectric thickness value is derived and presented in this research.

In a design example of a 4:1 50W transformer presented in this research, it has been shown that the bandwidth can be improved by 384%, along with a power density improvement of 45%, upon choosing of an optimum dielectric thickness of $0.156\mathrm{mm}$ to replace a standard $0.4\mathrm{mm}$ thick dielectric.

It should be noted that the results derived in this research are purely theoretical, justified by many idealisations and assumptions that are argued throughout the research. It is thus expected that practical results should at best approach the theoretical results, due to the known non-ideal nature of reality.

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List of Symbols

n	turns per-layer	
a_r	turns ratio	
N_P & N_1	Primary winding turns	
N_S & N_2	Secondary winding turns	
N_L	Number of layers in a winding	
C_1 & C_3	Primary and Secondary winding self-capacitances	F
C_k	Inter-winding coupling capacitance	F
C_{eq}	Equivalent capacitance	F
L_k	Leakage inductance	H
L_m	Magnetizing inductance	H
L_p	Per-layer inductance	H
L_t	Per-turn inductance	H
L_{eq}	Equivalent winding inductance	H
M	Mutual inductance	H
L_1 & L_2	Primary and secondary winding inductance	H
l_m	Mean magnetic flux path length	m
l_c	Length of the core	m
l_w	Width of the core's middle leg	m
l_t	Mean turn-length of a dielectric layer	m
l_s	Length of dielectric separating two adjacent conductors	m
l_{t_s}	Total length of the spiral conductors	m
b_w	Width of the core window	m

D_l	Length of the dielectric layer	m
D_w	Width of the dielectric layer	m
t	Dielectric thickness	m
t_{opt}	Optimum dielectric thickness	m
t_{max}	Maximum optimum dielectric thickness	m
f_{max}	Optimum frequency bandwidth	Hz
t'_{opt}	Optimum dielectric thickness asymptote value	m
f'_{max}	Optimum frequency bandwidth asymptote value	Hz
w	Width of conductor track	m
d	Separation distance between adjacent conductors	m
E	Electric field strength	$\mathrm{V\,m^{-1}}$
P_S	Source Power	W (VA)
P_L	Load Power	W
I_P & I_S	Primary and secondary winding currents	A
R_L	Load resistance	Ω
W_s	Total energy stored in the dielectric between two adjacent conductors	J
W_{intra}	Total energy stored in the dielectric in a spiral layer	J
$K(\,)$	is a the complete elliptic integral of the first kind.	
dn^{-1}	The inverse Jacobi dn function.	
ϵ_0	Permittivity of vacuum	$\mathrm{F\,m^{-1}}$
ϵ_r	Relative permittivity	
μ_0	Permeability of vacuum	$\mathrm{H\,m^{-1}}$
μ_r	Relative permeability	
ω	angular frequency	$\mathrm{rad\,s^{-1}}$

Dedicated to my parents...

Chapter 1

Introduction

Power processing has become the focus of development and research in recent years as robust and efficient power supplies have been known to be essential in taking advantage of renewable energy. Due to this, increasing emphasis is being placed on planar magnetics integration technology for energy processing [1,2]. The main advantage of this technology is the reduction in cost and volume of electronic circuits, as well as making the manufacturing process simpler and robust due to better repeatability.

An important and common magnetic component in many power electronics topologies is a transformer. Traditionally, these transformers are constructed by winding insulated metal wires on a ferrite core. However, the geometry of these structures lead to issues relating to repeatability [3], due to the irregular and unpredictable alignment of the wires. This in turn impacts on geometry based parasitics such as winding capacitance and leakage inductance. Planar transformers are advantageous in this regard, as parasitics can be potentially controlled fairly accurately in the design stages, thereby ensuring repeatability. In this context there is a growing preference to use planar transformers in modern power electronics.

1.1 Planar Transformers

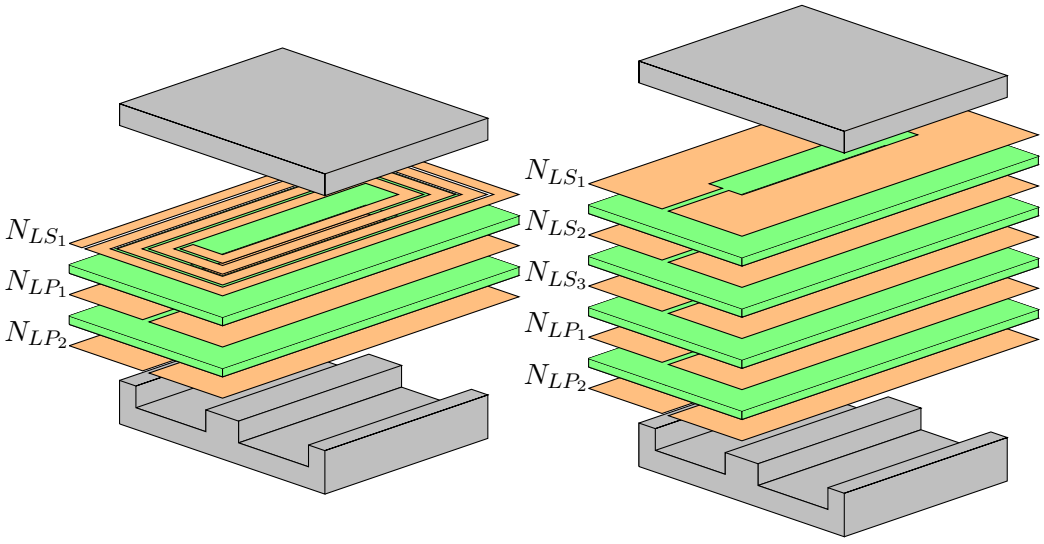
Planar transformers are a subset of planar magnetics technology. One of the first publications on this technology appeared in the year 1986 and was the work of A. Estrov [4], which was later patented in 1991 [5]. These transformers are constructed by sandwiching layers of conductors, dielectrics and magnetic materials together [6], as shown in fig. 1.1a & fig. 1.1b. A picture showing planar transformers in power electronics circuits is shown in fig. 1.2. The advantages of planar transformers become clear in this respect; the planar nature of the windings allow for more complex winding configurations and also allow for excellent repeatability in manufacturing due to well defined geometry [7]. This characteristic allows parasitics to be controlled, such that they have the least effect on the performance of the transformer. Furthermore, planar transformers exhibit good thermal characteristics and low profile [2, 8, 9].

Planar transformers often replace traditional transformers for operation frequencies higher than 100kHz [10], and for power levels in the range of several kVA [11]. Many authors [9, 12–20] cite the above mentioned characteristics as main reasons to use planar transformers in switched-mode power supplies. These benefits have allowed authors to develop planar transformers for applications in aerospace [21] and consumer electronics [18, 22, 23].

1.2 The Research Problem

The need for compact and power-dense planar transformers poses a problem, as it is not known how compact these transformers can be constructed for a given application without bandwidth deterioration.

Construction of planar transformers up to recent times have not seriously considered the combined effect of parasitic capacitance and leakage inductance in the design stages. Authors in [24] claim to be able to custom design transformer cores



(a) An exploded view of a 2:4 transformer with one multi-turn layer.

(b) An exploded view of a 2:3 transformer with single turn layers.

FIGURE 1.1: Illustrations of planar transformers. Layer-to-layer connections not shown.

in order to achieve a record power density and increase the operating frequency. In this case, the transformer has not been designed with the effects of both capacitive and inductive parasitics in mind. This is evident as stray capacitance and leakage inductance measurements have been made after the transformer was built, and no comparisons have been made with predicted values, implying that there was no effort to optimize parasitics in the design stage. Furthermore the dielectric thickness that is used in the design has been arbitrarily chosen, presumably based on what was readily available.

Authors in [8,19,25] state that the bulk of research on planar transformers place more emphasis on the modelling and optimizing of losses and leakage inductance, and that parasitic capacitance is not seriously considered. The general view is that both parasitic capacitance and leakage inductance have an impact on the 'cut-off frequency' and 'bandwidth' of the transformer respectively [7,22,24] (without describing the exact meaning of 'cut-off frequency' or 'bandwidth'). The parasitics

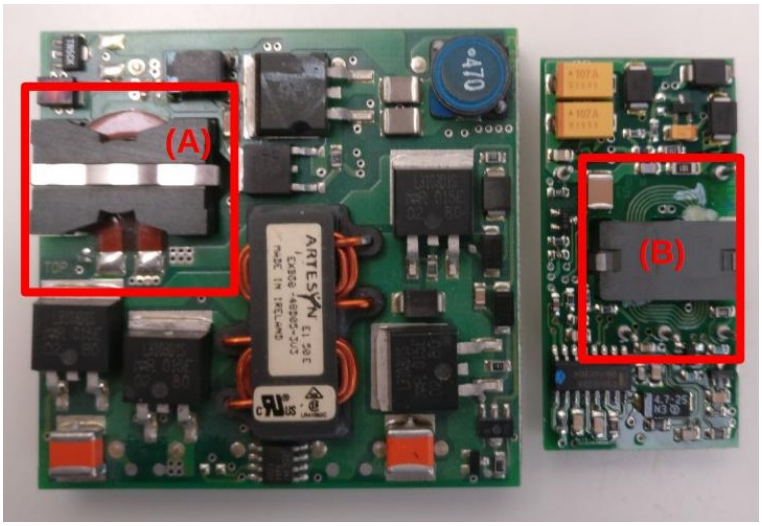


FIGURE 1.2: Picture showing (A) a planar transformer with a single turn layer and (B) a planar transformer with a multi-turn layer in red.

are also known to lead to EMI issues and distorts currents on excitation side, decreasing overall efficiency [8, 26]; discussion on EMI is out of scope of this work. Although the overall effects of the parasitics are known, there is a general lack of understanding as to how exactly they affect bandwidth.

The trade-off between leakage inductance, losses and parasitic capacitance has been investigated to some extent in [8], and in [7] the authors define a 'figure-of-trouble' LC as being the product of leakage inductance and parasitic capacitance, since both quantities are opposingly dependent on the dielectric thickness of the windings. In both papers, the trade-off has not been thoroughly investigated within the context of bandwidth and power density, thus leaving room for research in this direction.

The bandwidth is thought to be directly related to the energy flow within the parasitics, which are in turn thought to be functions of dielectric thickness. Bandwidth is conventionally defined as the 3dB cut-off point of a signal, where half the power is lost. This definition may be directly applicable to signal processing transformers, often found in broadband networks. However, such a definition is

not suitable for power processing transformers. The terms 'bandwidth' or 'cut-off' frequency of a transformer are not defined or discussed in literature, although it is commonly used [7, 22, 24]. Furthermore, there is no generalised analytical expression for the bandwidth, nor one that is based purely on electromagnetic parasitics, in literature. In order to avoid any misunderstanding and continue further with the research, there is a need for the bandwidth of a planar power transformer to be defined and expressed as a function of capacitive and inductive parasitics. Due to the exclusion of all non-ideal characteristics such as losses, it can be argued that the defined bandwidth is actually theoretical and cannot be achieved in practise.

Currently, the dielectric thickness appears to be chosen based on what is readily available, as long as it does not undergo dielectric breakdown. However, the dielectric thickness has an impact on the capacitive and inductive parasitics within the transformer, which in turn impacts on the transformer's operation bandwidth. It is therefore necessary to choose the dielectric thickness in a optimum manner with respect to bandwidth. This research is therefore meant to provide a direction in this regard by means of providing a method to choose the optimum dielectric thickness.

It is reasoned that once the optimum dielectric thickness has been found, it will lead to the optimum values of parasitic capacitance and leakage inductance. The added benefit could potentially be an increase in power-density due to the choice of optimum dielectric thickness. Since much research has been done to optimise the performance of the planar transformer by merely looking at losses and ignoring effects of parasitics, this research approaches the problem from a different direction, wherein the transformer's performance is evaluated solely based on electromagnetic interactions, and not losses due to imperfect materials.

To summarise, it is proposed that the theoretical bandwidth of planar transformers can be found by considering the intrinsic inductive and capacitive parasitics involved. From examining the effects of these parasitics on bandwidth, one can establish a method to design planar transformers of higher (or optimum) bandwidth compared to traditional transformers, by optimising the dielectric thickness, given an application's frequency and power requirements.

1.3 Research Question

"Given the inevitable presence of capacitive and inductive parasitics in planar transformers, how are they related to the dielectric thickness, and how do they influence the theoretical bandwidth of the structure?"

1.4 Research Objectives

The objectives of this research are:

- To define the theoretical bandwidth of the planar transformer as a function of capacitive and inductive parasitics.
- To evaluate the influence of leakage inductance and parasitic capacitance on the bandwidth of the planar transformer.
- To identify and evaluate the optimum thickness of the dielectric by analysing the role of dielectric thickness on the bandwidth.

1.5 Research Constraints

This research takes into account the ideal planar transformer, inclusive of inductive and capacitive parasitics. Specifically, the following constraints are considered:

- The scope is restricted to analysis of two-winding planar transformers where the primary and secondary layers are not interleaved.
- All losses are ignored. These losses include winding losses and core losses. These losses are complicated in nature and have been examined in great detail in literature [2, 8, 19, 27–33]. Inclusion of these effects would significantly complicate the analysis and scope of this research and obscure the interactions between the leakage inductance and the parasitic capacitance. In light of this, it is decided to exclude such effects from analysis in this research.
- The conductors are assumed to be significantly thinner than the dielectric layers by many orders of magnitude. This is justified as winding losses are ignored.
- The load is considered to be purely resistive. This is to ensure that the frequency response of the transformer is not band-limited by the nature of the load.
- Parasitic capacitance coupling to the environment is ignored as the determination of these capacitances is complicated due to the unpredictable nature of the environment in practice.
- Common-mode currents depend on the application and are not considered in this research. This implies that the potentials on the secondary side of the transformer are assumed to not rise to arbitrary values.
- A low-power 50W planar transformer suitable for consumer electronics is considered to demonstrate proof of concept in this research.

- Analysis will only consider a transformer operating in a conventional fashion. Thus the analysis excludes flyback coupled inductors.
- The research is not looking into the saturation curve of the core/dielectric material. The permeability and permittivity of the materials are thus assumed to be frequency independent, to simplify the analysis. This ties into the assumption that the materials are considered ideal. Material characteristics are thus not explored in this research.

1.6 Research Approach

The following approach will be used in tackling the research goal:

- An accurate model of a planar transformer is required. The leakage inductance, winding inductance and winding capacitance elements must be accurately modelled analytically. These elements must then be used in an accurate electric circuit model.
- The model of the planar transformer must be validated using an appropriate simulation tool. Such a model cannot be validated in the lab using prototypes due to various non-ideal characteristics such as non-linear losses present, as well as due to the difficulty of measuring the strengths and patterns of the electric and magnetic fields within the planar transformer structures.
- The theoretical bandwidth for the planar transformer must be defined mathematically as functions of the dielectric thickness. This is possible because the circuit elements including the parasitics are analytically defined as functions of dielectric thickness.
- The effect of the dielectric thickness on the theoretical bandwidth of the planar transformer can then be evaluated. Closed form expressions can then be derived to aid in designing of planar transformers.

1.7 Dissertation Outline

The remainder of this dissertation is outlined as follows:

- Chapter two focuses on developing an equivalent electrical circuit model, derived from analysing the electric and magnetic fields of the planar transformer structure.
- Chapter three is dedicated to analysing the effects of dielectric thickness on the bandwidth of the transformer, and thereby optimising it.
- Chapter four concludes the research and provides a summary of the research presented, along with recommendations for future work in this field.
- Appendix A presents the relevant analytical expressions needed to describe the geometrical lengths of the spirals and the dielectric. Appendix B presents derivations of analytical expressions related to power, bandwidth and optimum thickness. Appendix C presents information on the simulation models and the software packages used in the research.

Chapter 2

The Planar Transformer Model

2.1 Modelling Approach

In order to analyse the effects of the capacitive and inductive parasitics, it is important to be able to describe them using models. More importantly, analytical models of the parasitics are needed such that the results derived from the research are also analytical. Accurate analytical results are preferred as it allows for quick calculations and helps to circumvent the time-consuming and computational resource-intensive process of simulations. Furthermore, the analytical models must be relatively simplistic but adequate enough to accurately capture the behaviour of the parasitics.

The parasitics of the planar transformer appear to be distributed in nature. It is therefore possible to use a distributed model of the transformer. However, such a model would be complicated to analyse and generalise. A lumped circuit model is thus preferred as it is relatively simple to derive closed form expressions from it.

There are two levels of modelling in this chapter– the model of the electrical equivalent circuit of the planar transformer and the model of the circuit components such as the parasitic components, winding inductance and the leakage inductance; all of which are developed based on analysis of the electric and magnetic field distributions within the transformer structure. The circuit model must be able to capture the frequency response of the planar transformer accurately and

adequately, while retaining simplicity. It is essential to maintain simplicity due to the number of variables involved in determining the frequency response; it is important to be able to analyse the interplay between these variables in order to determine their effects on the transformer's bandwidth.

This research relies on theory and simulation due to the many idealistic assumptions and constraints made. The following simulation software is used to validate the theoretical analysis and derivations presented in this chapter:

- FEKO [34] & FEMM [35]: FEKO software is used to solve for electric and magnetic fields in 3D models of planar transformers. FEMM Software used to solve for electric and magnetic fields in 2D structures.
- NgSpice [36]: Software used to simulate electrical circuit models.

More information regarding the simulation tools and simulation set-up, including the use of permittivity/permeability values used in this research is given in Appendix C.

In order to restrict the complexity of the model, the constraints and assumptions in section 1.5 in chapter one are taken into account. These constraints and assumptions ensure that any results derived from the model are based only on the inductive and capacitive parasitic elements of the model. The model thus reflects the ideal nature of the transformer, with the inclusion of parasitic capacitance and leakage inductance that arise intrinsically due to the geometrical nature of the transformer.

This chapter will act as a foundation for the main results of the research found in chapter three. Various circuit models from literature will be shown and evaluated for their merit. Next, the individual capacitive and inductive parasitic models will be analysed, along with the model of the winding inductance. Finally, the circuit model will be chosen based on simplicity and its ability to capture various aspects of the frequency response, as will be shown later.

2.1.1 Existing Electrical Circuit Models

It is preferable to model the planar transformer using an electrical circuit model because the circuit can be inherently analysed analytically using mesh equations, which would eventually lead to closed form expressions for whatever that may need to be solved for.

Existing circuit models in literature commonly define the magnetizing inductance L_m, as shown in fig. 2.1 [8, 13]. This is in contrast to directly specifying the primary and secondary winding inductances as some authors prefer [37]. In the case where the winding inductances are explicitly included in the circuit model, the leakage flux can be reflected in the model in two ways:

- The magnetic coupling constant k between the two winding inductances can be directly specified, as shown in fig. 2.2a.
- The winding inductances can be ideally coupled ($k = 1$), with the leakage inductance element defined in the circuit model, as shown in fig. 2.2b. This method is valid for tight coupling and preferred as the leakage inductance can be analytically calculated based on geometry.

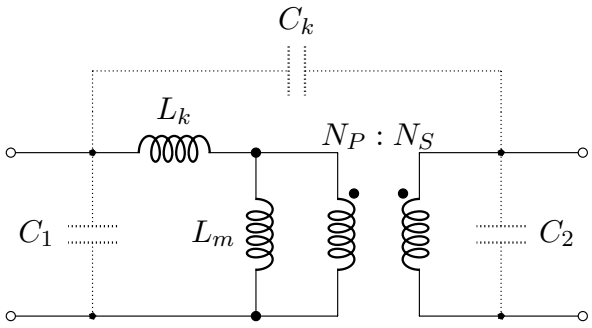
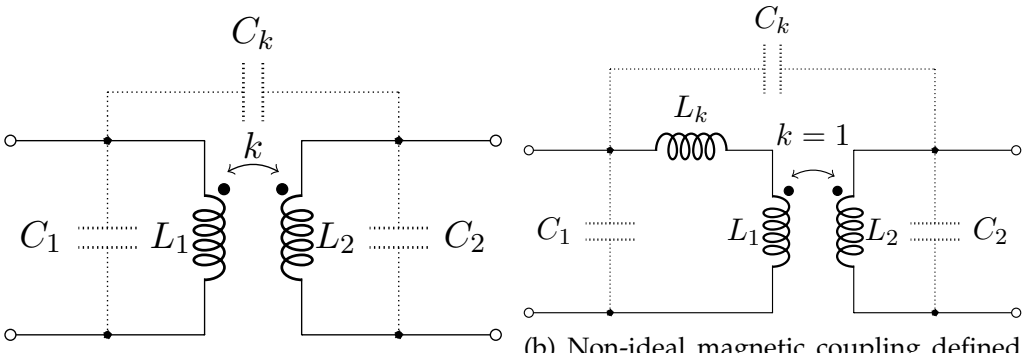


FIGURE 2.1: Transformer equivalent circuit model with magnetising inductance element L_m [8, 13].

The disadvantage of using the magnetizing inductance model is that it hides the self-resonances of individual windings with their self-capacitances, potentially



(a) Non-ideal magnetic coupling defined using the coupling coefficient k.

(b) Non-ideal magnetic coupling defined using leakage inductance and perfectly coupled windings ($k = 1$).

FIGURE 2.2: Circuit models showing the two different magnetic coupling definitions.

limiting the frequency response complexity. Furthermore, it is more intuitive to define the primary and secondary winding inductances in the circuit model as this is how they are physically constructed in a transformer. The placement of leakage inductance within the circuit model is also debatable, as some authors [11, 13, 38] place it in series with the exciting source as shown in fig. 2.3 and others [8, 39, 40] place it in position within the LC resonant tank as shown in fig. 2.1 & fig. 2.2b. It appears that both these configurations are valid; however the preferred configuration should ultimately be the one that adequately describes the frequency response of the transformer without increasing the complexity of the circuit mesh equations.

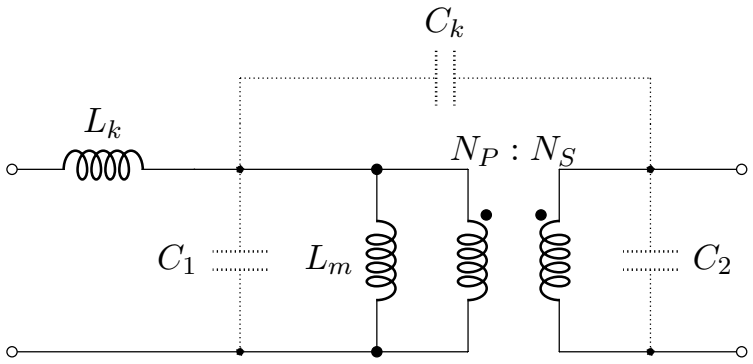


FIGURE 2.3: Circuit model with leakage inductance element L_k placed in series with the excitation [11, 13, 38].

There exists a capacitance coupling the primary winding to the secondary winding called the coupling capacitance C_k. The model also contains the self capacitances C_1 & C_2 that arise due to the sandwich nature of the conductor layers in the windings. These capacitances are discussed and modelled in section 2.2.3 and section 2.2.5. It should be also noted that some authors [8, 25] prefer to lump the coupling capacitance and the self-capacitance of the secondary winding into a single equivalent capacitance by referring them to the primary side, as shown in fig. 2.4. Although this simplifies the circuit model, it reduces the complexity of the frequency response too much; it becomes difficult to analyse the direct effect of individual capacitances on the overall frequency response.

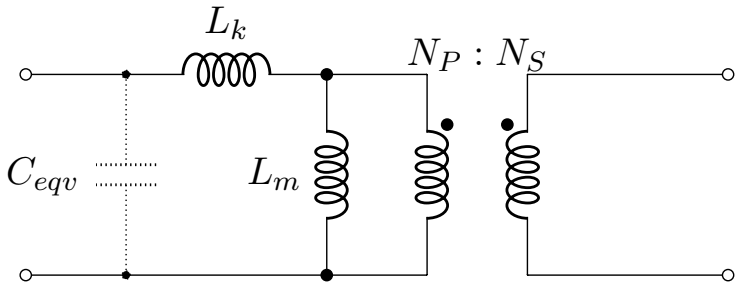


FIGURE 2.4: Circuit model with lumped equivalent capacitance C_{eqv} [8, 25].

It is preferable to use the circuit model which shows both the primary and secondary winding inductances as this is intuitive. Furthermore it is also preferable to use the model that defines magnetic coupling using the leakage inductance since it can be readily calculated. The circuit model that is to be chosen should also be based on whether the frequency response matches with the frequency response of simulated 3D FEM models in FEKO. The chosen circuit model and comparisons of the frequency responses of various models are shown later in section 2.3.

2.2 Electrical Equivalent Circuit Model

2.2.1 Winding Inductance

The winding inductance is fairly simple to calculate. All expressions are based on the geometry of the transformer core, illustrated in fig. 2.5. For simplicity, it is assumed that all layers have the same number of turns per-layer, n. The per-layer inductance L_p is given in eq. (2.1). When $n = 1$, the per-turn inductance L_t is found.

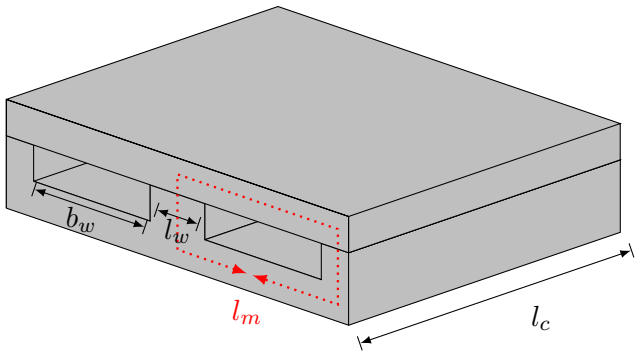


FIGURE 2.5: 3D view of the planar core.

$$L_p = \frac{\mu_0 \mu_r n^2 A_e}{l_m} \tag{2.1}$$

Where:

n is the turns per layer,

A_e is the effective area of the magnetic flux path, given as the product of the length of the core l_c and the width of the middle core leg l_w.

l_m is the mean magnetic flux path length.

The equivalent inductance L_{eq} is then simply derived from the circuit shown in fig. 2.6 and is given in eq. (2.2), for N_L number of layers. The magnetic coupling constant k is taken as unity, as the leakage flux is accounted for in section 2.2.2.

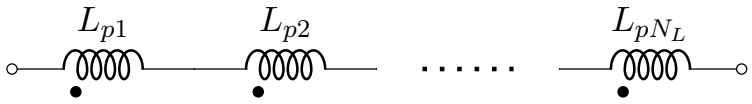


FIGURE 2.6: Circuit of coupled inductors connected in series.

$$L_{eq} = \begin{cases} \frac{\mu_0 \mu_r n^2 A_e \left(N_L + 2\binom{N_L}{2}\right)}{l_m} \text{ if } N_L > 1 \\ \frac{\mu_0 \mu_r n^2 A_e}{l_m} \text{ if } N_L = 1 \end{cases} \tag{2.2}$$

2.2.2 Leakage Inductance

The leakage inductance of the planar transformer is conventionally calculated based on the energy stored inside the dielectric volume and the conductor volume. However, it has been shown in [41] that the leakage magnetic energy within the conductors decreases with frequency due to skin effect and becomes negligible at high frequency. The leakage energy within the conductor further becomes negligible when an infinitesimally thin conductor is assumed. For simplicity sake, a frequency-independent model of leakage inductance is used in the planar transformer model. Magnetic leakage energy storage within the conductors is thus ignored.

The leakage inductance of planar transformers can be calculated based on the energy storage of the H-field in the winding volume; the energy stored in the magnetic field in a given volume V is given by eq. (2.3). As the H-field only varies in the vertical x direction as shown in fig. 2.8, the integral can be re-written as a function of vertical displacement x.

The equivalent leakage inductance L_k can be found by equating the inductor energy to the magnetic field energy as given in eq. (2.4). The total leakage inductance can be referred to the primary side by taking into account the current I_p passing through the primary winding.

$$W = \frac{1}{2}\mu_0 \mu_r \int H^2 dV = \frac{1}{2}\mu_0 \mu_r \; l_t \; b_w \int H^2(x) dx \tag{2.3}$$

Where:

l_t is the mean length of the dielectric layer, calculated from eq. (A.2) in Appendix A.

b_w is the width of the core-window or the width of a single-turn track on a dielectric layer as shown in fig. A.1, in Appendix A.

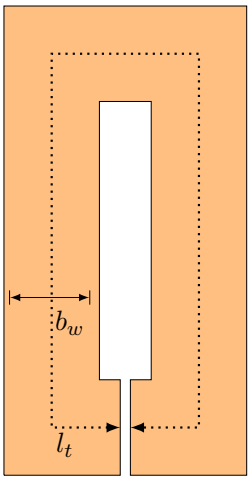


FIGURE 2.7: Illustration of a single turn winding.

$$\frac{1}{2}L_k I_p^2 = \frac{\mu_0\, l_t\, b_w}{2} \int H^2(x)dx \tag{2.4a}$$

$$L_k = \frac{\mu_0\, l_t\, b_w}{I_P^2} \int H^2(x)dx \tag{2.4b}$$

The H-field generated per layer can be given as eq. (2.5), where I can either be the primary or secondary currents I_P & I_S respectively and n is the number of turns per layer. For simplicity, the H-field function is only calculated for the non-interleaved winding configuration. The cross-section H-field pattern for a 2:4 transformer is shown in fig. 2.8 (note that thickness of the conductors has been neglected).

$$H = \frac{nI}{b_w} \tag{2.5}$$

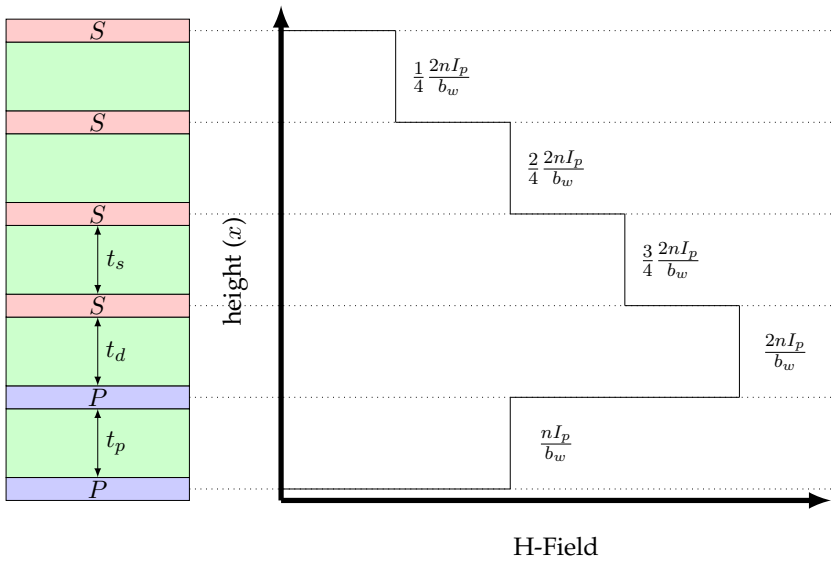


FIGURE 2.8: H-field pattern within the cross section of the core window of a 2:4 transformer.

The H-field integral in eq. (2.4) can be generalised for given dielectric thicknesses t_p, t_s & t_d and number of layers N_1 & N_2, as given in eq. (2.6a). The leakage inductance can thus be defined purely as a function of geometry, as given in eq. (2.6b).

$$\int H^2(x)\,dx = \left(\frac{nI_p}{b_w}\right)^2 \left[t_p \sum_{y=1}^{N_1-1} y^2 + t_d N_1^2 + t_s \left(\frac{N_1}{N_2}\right)^2 \left(\sum_{z=1}^{N_2-1} z^2\right)\right] \tag{2.6a}$$

$$L_k = \frac{\mu_0\, l_t\, n^2}{b_w} \left[t_p \sum_{y=1}^{N_1-1} y^2 + t_d N_1^2 + t_s \left(\frac{N_1}{N_2}\right)^2 \left(\sum_{z=1}^{N_2-1} z^2\right)\right] \tag{2.6b}$$

Where:

n is the turns per layer,

t_p, t_s are the thickness of the dielectric in the primary and secondary windings respectively.

t_d is the thickness of the dielectric separating the primary and secondary layers.

N_1 & N_2 are the number of layers in the primary and secondary windings respectively.

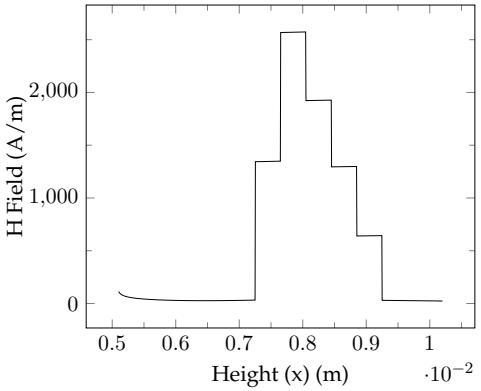
A few single-turn, multi-layer planar transformers were simulated in FEKO and the magnetic fields were analysed; they were all excited with a $1V_p$ sinusoidal signal and had their secondary sides shorted; a voltage source was chosen for exciting the structure, as it is expected that the currents within the structure will resolve themselves appropriately. The dimensions of the dielectric layers and the core used in simulations are presented in table C.1 in Appendix C; the dielectric thickness values are arbitrarily chosen. The simulated cross-section H-field patterns for a 2:4, 2:6 & 2:8 planar transformer are shown in fig. 2.9a, fig. 2.9b & fig. 2.9c respectively. The simulated H-field pattern for a 2:4 transformer with a relatively large winding separation t_d is shown in fig. 2.9d with dimensions tabulated in (d) in table 2.1, the choice being arbitrary for demonstration.

Inspection of fig. 2.9 shows that the flat peaks of the H-field patterns match the ratio pattern shown in fig. 2.8. It may be noted that the H-field patterns obtained from simulation do not show energy storage within the conductors as the conductors are specified in the simulation as being infinitesimally thin; this is to reduce the computational resources required for simulation, and such a setup also agrees with the assumption made earlier regarding the conductors being relatively much thinner than the dielectric. Comparison between calculated and simulated values for leakage inductances are given in table 2.1; the values of the simulated leakage inductances are obtained from the H-field data plotted in fig. 2.9. It can be seen from this table that the leakage inductance can be calculated reasonably accurately using the expression presented in this section. The leakage inductance model can be therefore considered valid.

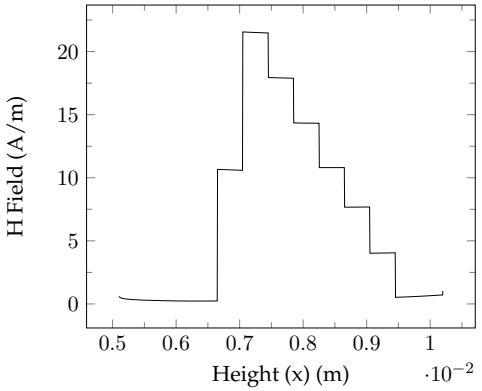
It may be noted that the current magnitude for (a) in table 2.1 appears to be an outlier. The reason for such a disparity can be attributed to a linear scaling issue, since calculations and simulations are in agreement, thereby eliminating possibility of simulation artefacts. However, further validation is necessary, but is in any case thought to not significantly impact the core outcome of this research.

Figure	Turns Ratio	t_p (mm)	t_d (mm)	t_s (mm)	I_p (A)	L_k (nH) Simulated	L_k (nH) Calculated
a	2:4	0.4	0.4	0.4	24.8	48.31	50.36
b	2:6	0.4	0.4	0.4	0.19	69.64	65.83
c	2:8	0.4	0.4	0.4	1.65	82.99	81.46
d	2:4	0.4	2.45	0.4	0.94	176.13	171.82

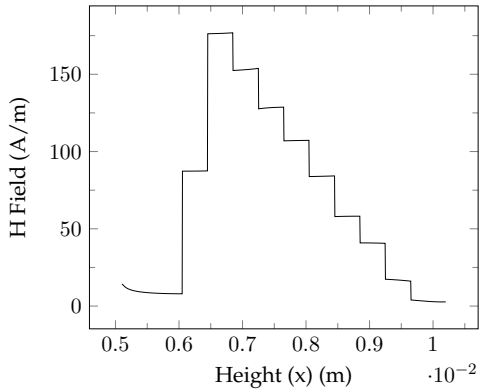
TABLE 2.1: Comparison of expected leakage inductance values and values obtained from FEKO simulation. $b_w = 18.8\text{mm}$, $l_t = 221.5\text{mm}$, $n = 1$



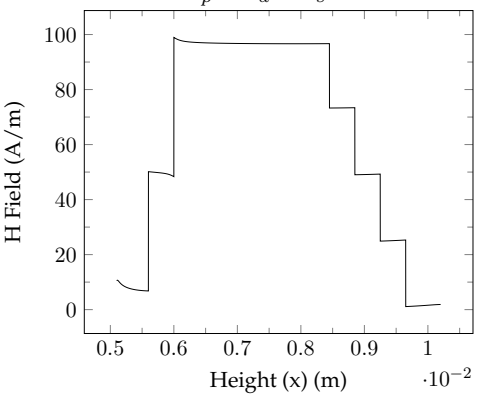
(a) H-field cross section of a 2:4 planar transformer. $t_p = t_d = t_s = 0.4\text{mm}$.



(b) H-field cross section of a 2:6 planar transformer. $t_p = t_d = t_s = 0.4\text{mm}$.



(c) H-field cross section of a 2:8 planar transformer. $t_p = t_d = t_s = 0.4\text{mm}$

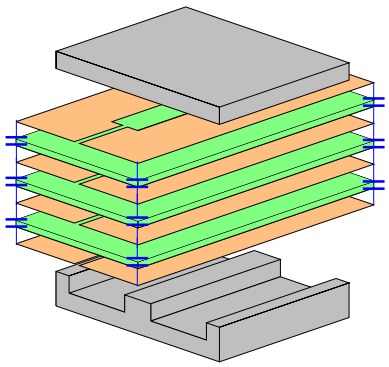


(d) H-field cross section of a 2:4 planar transformer. $t_p = t_s = 0.4\text{mm}$, t_d =2.45mm .

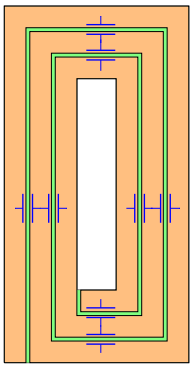
FIGURE 2.9: Cross sectional plots of H fields of the planar transformer windings simulated in FEKO. $b_w = 18.8\text{mm}$, $l_t = 221.5\text{mm}$, $n = 1$

2.2.3 Self Capacitance

The self capacitance of the windings is the sum of the inter-layer capacitance which arises due to the electric field between layers of the same winding, and the intra-layer capacitance which arises due to electric field fringing effect between conductors within the same winding layer. The inter-layer capacitance is generally thought to be larger than the intra-layer capacitance due to the larger effective surface area of the winding conductors.



(a) An exploded view of a 4-layer winding showing parallel conductors and the associated modelled inter-layer capacitances in blue.



(b) A top-down view of a 3-turn spiral showing adjacent conductors separated by dielectric and their associated modelled intra-layer capacitances in blue.

FIGURE 2.10: Illustrations of inter-layer and intra-layer capacitances.

Inter-layer Capacitance

The inter-layer capacitance can be calculated purely as a function of geometry by taking into account the voltage distribution within a winding. When the winding is excited, a voltage is dropped across the entire length of the winding. Due to the presence of the core, most of the inductance is distributed only in segments of the winding within the core. This results in a higher voltage gradient within the region of the core. However, due to the fact that the voltage has to drop equally over each of the winding layers (given that the layers have the same number of

turns), it can be assumed that the voltage gradient is linear as the electric field magnitude is the same in either case. This is thus equivalent to the case where there is no core present; the capacitance is a physical quantity and is expected to be the same, irrespective of the presence of the core. This results in a uniform electric field between all layers in the same winding. A simplified circuit model illustrating the equal voltage drops over each layer is shown in fig. 2.11.

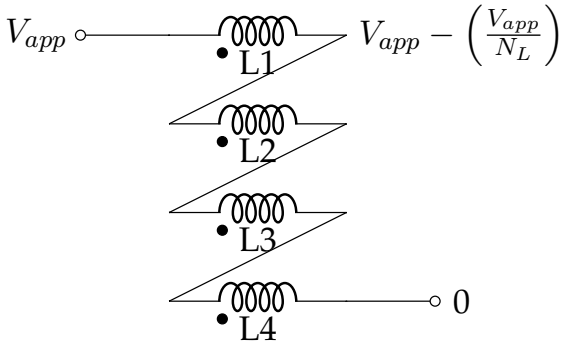


FIGURE 2.11: Circuit model showing the voltage drops over each layer in a 4-layer winding.

Simulation of a 4-layer winding shown in fig. 2.12 results in a voltage distribution shown in fig. 2.13. These results support the previous discussion.

The electric field strength E found in the winding is given in eq. (2.7a), where V_{diff} is the voltage difference across the dielectric of thickness t. For a winding with N_L number of layers of equal turns, V_{diff} is given in eq. (2.7b), where V_{app} is the voltage applied to the terminals of the winding.

$$E = \frac{V_{diff}}{t} \tag{2.7a}$$

$$V_{diff} = \frac{V_{app}}{N_L} \tag{2.7b}$$

The equivalent capacitance of the winding can be found by equating the energy stored in the electric field within the winding to the energy stored in an equivalent capacitance. The electrical field integral on the right-hand side of eq. (2.8a) can be

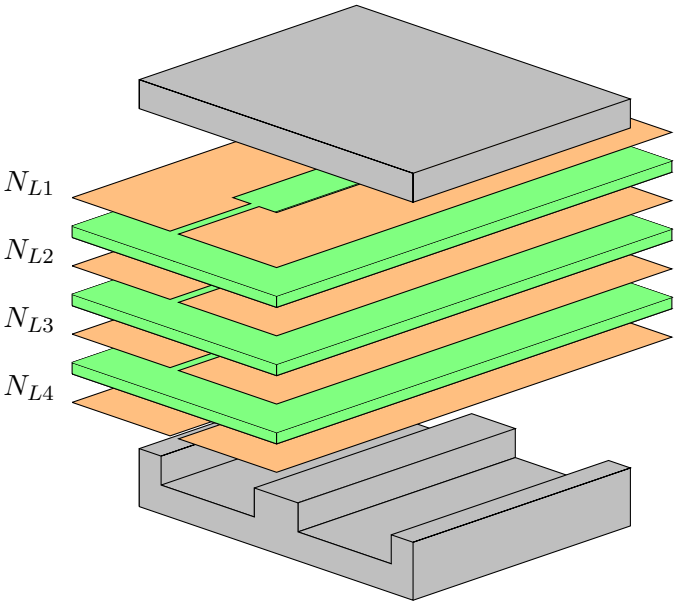


FIGURE 2.12: 4-layer winding with one turn per layer.

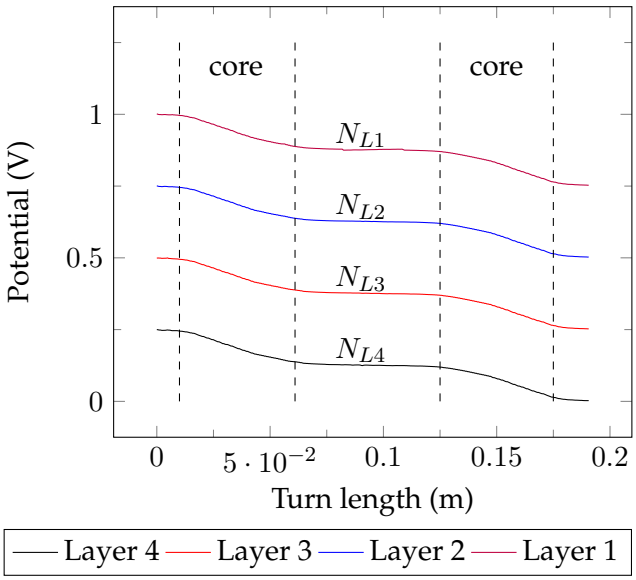


FIGURE 2.13: Voltage distribution along the length of four winding layers.

re-written as given in eq. (2.8b). The equation given in eq. (2.8a) can be re-arranged to give the expression for the equivalent capacitance as given in eq. (2.8c).

Structures with various number of layers have been simulated in FEKO with dimensions of the core and dielectric layers presented in Appendix C; the capacitance

was calculated by extracting the magnitudes of electric fields present within the structure and compared with the analytical calculations presented in this section. It can be seen from table 2.2 that the capacitance calculated using the expression presented in this section is in good agreement with the FEKO simulation results.

$$\frac{1}{2}C_{eq}V_{app}^2 = \frac{1}{2}\epsilon_0\epsilon_r \int E^2 dV \tag{2.8a}$$

$$\int E^2 dV = t\, l_t w \sum_{x=1}^{N_L-1} E_x^2 = t\, l_t w (N_L - 1)\left(\frac{V_{app}}{t\, N_L}\right)^2 \tag{2.8b}$$

$$C_{inter} = \epsilon_0\epsilon_r \frac{l_t w}{t}\left(\frac{N_L - 1}{N_L^2}\right) \tag{2.8c}$$

Where:

V_{app} is the potential difference applied to the terminals of the winding in Volts,

C_{inter} is the equivalent inter-winding capacitance,

V is the volume enclosing the electric field.

N_L is the number of layers present within a winding.

t is the thickness of the dielectric material.

w is the width of the conductor.

l_t is the length of the conductor on a single-turn layer. It is equal to l_{t_s} given in Appendix A, when there is more than one turn in a layer.

It is found from eq. (2.8c) that the inter-layer capacitance is merely a function of overlapping surface area and number of layers. It may be noted that for the case where there is more than one turn per layer ($n > 1$), the surface area for the capacitance changes. This change in surface area can be taken into account by substituting l_t for l_{t_s} (given in Appendix A), which is the total length of the spiral track. Furthermore w will be equal to the width of the conductors of the spiral tracks.

Layers	ϵ_r	FEKO (pF)	Calculated (pF)
2	5	113.20	115.30
4	5	87.67	86.45
6	100	1296	1280
8	100	1017	1008

TABLE 2.2: Comparison of simulated and calculated inter-layer capacitance values. $t = 0.4\text{mm}$, $w = 18.8\text{mm}$, $l_t = 221.5\text{mm}$. Permittivity values arbitrarily chosen for demonstration.

Intra-layer Capacitance

The intra-layer capacitance arises due to the fringing effects of the electric flux when two conductors are placed adjacent to each other on a dielectric medium. Authors in [42] have derived this capacitance expression for a dual-side layer using the Schwarz-Christoffel conformal mapping technique. However a slightly modified expression is required for a single-side layer; this is derived by changing the limits of integration. Series of conformal transformations are needed in order to reach a canonical equivalent capacitance structure.

Firstly, the capacitance per-unit-length value is found for two adjacent conductors on a dielectric illustrated in fig. 2.14; the thickness of the conductors is irrelevant as the capacitance is purely based on the edge effect. Furthermore, it is assumed that there is negligible electrical flux leakage outside of the dielectric material. The flux intensity pattern along with the equipotential lines of the electric field can be seen in fig. 2.15. The variable z represents the coordinates of the vertices of the conductors on the dielectric in the complex z-plane. The first transformation from the z-plane to the ω-plane (not to be mistaken with the frequency plane) is defined by eq. (2.9) [42]. The complex coordinates z_a and z_b are defined in eq. (2.10) & eq. (2.10b) respectively; the mapped coordinates in the ω-plane are given in eq. (2.11a) & eq. (2.11b).

$$\omega = \frac{\pi}{2t} tanh\left(\frac{\pi z}{2t}\right) \tag{2.9}$$

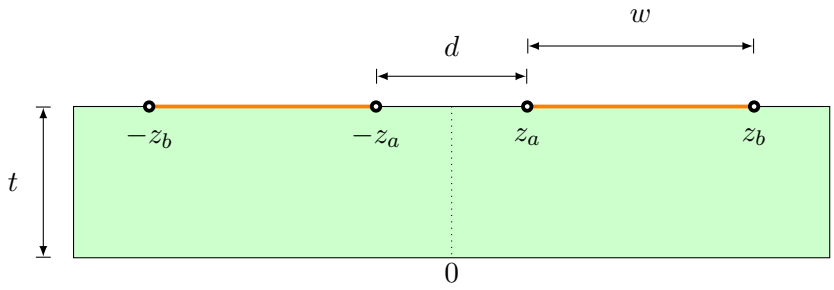


FIGURE 2.14: Cross sectional view of two co-planar conductor strips on a dielectric medium, with coordinates mapped in the complex z-plane.

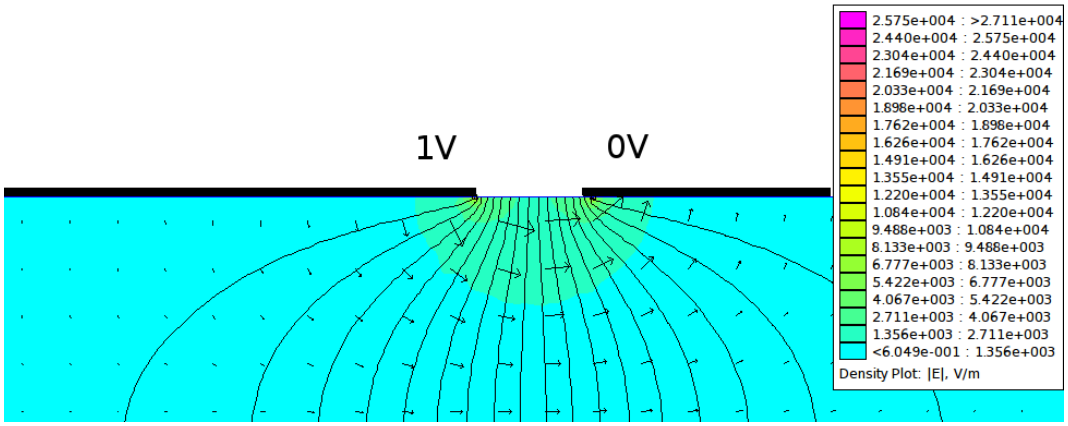


FIGURE 2.15: Simulated electric field intensity pattern of two co-planar conductor strips on a dielectric medium, same plane as fig. 2.14. Simulated using FEMM. The dielectric thickness is 1mm and the separation distance of the conductors d is 0.5mm The relative permittivity is 5.

$$z_a = \frac{d}{2} + it \tag{2.10a}$$

$$z_b = (\frac{d}{2} + w) + it \tag{2.10b}$$

$$\omega_a = \frac{\pi}{2t} tanh\left(\frac{\pi\left(\frac{d}{2} + it\right)}{2t}\right) = \frac{\pi}{2t} coth\left(\frac{\pi d}{4t}\right) \tag{2.11a}$$

$$\omega_b = \frac{\pi}{2t} tanh\left[\frac{\pi\left(\frac{d}{2} + w + it\right)}{2t}\right] = \frac{\pi}{2t} coth\left[\frac{\pi}{2t}\left(\frac{d}{2} + w\right)\right] \tag{2.11b}$$

Where:

t is the thickness of the dielectric.

d is the separation distance of two adjacent conductors.

w is the width of the conductors.

The transformed coordinates in the ω-plane are illustrated in fig. 2.16. The second transformation maps the coordinates in the ω-plane to coordinates in the ζ-plane. This transformation is given by eq. (2.12) [43]; the transformed coordinates ζ_a & ζ_b are given in eq. (2.13a) & eq. (2.13b) [44][42]. The equivalent capacitance is thus given in eq. (2.14); the total capacitance can thus be found by multiplying C_s with the length of the strip l_s. Strips with various dimensions have been simulated in FEMM and their respective capacitance values have been compared with calculated/expected values in table 2.3; it can be concluded that the mathematical expressions used to calculate the capacitance of such structures are accurate when compared to simulated results.

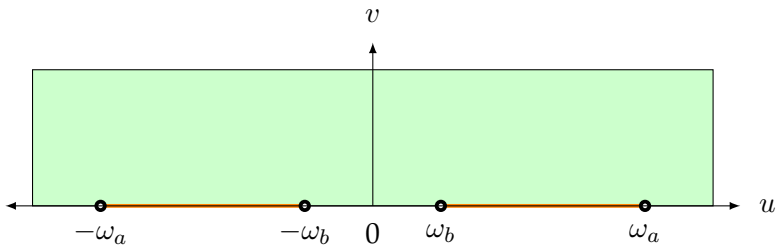


FIGURE 2.16: Transformed coordinates of conductor vertices in the ω-plane.

$$\zeta = \int_0^w \prod_{i=1}^{4} \frac{d\zeta}{\zeta - w_i} = \int_0^w \frac{d\zeta}{(\zeta^2 - w_a^2)(\zeta^2 - w_b^2)} \tag{2.12}$$

$$\zeta_a = \pm\frac{1}{\omega_a} K\left(\frac{\omega_b^2}{\omega_a^2}\right) + j\frac{1}{\omega_a} dn^{-1}\left[\frac{\omega_b}{\omega_a}, \frac{\sqrt{\omega_a^2 - \omega_b^2}}{\omega_a}\right] \tag{2.13a}$$

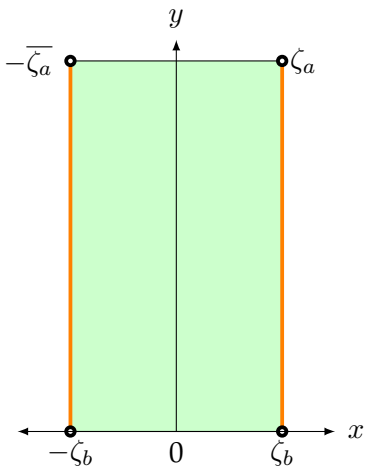


FIGURE 2.17: Final transformed coordinates in the $zeta$-plane.

$$\zeta_b = \pm\frac{1}{\omega_a} K\left(\frac{\omega_b^2}{\omega_a^2}\right) \tag{2.13b}$$

$$C_{s_x} = \epsilon_0\epsilon_r \left|\frac{Im(\zeta_a)}{2\zeta_b}\right| l_{s_x} \tag{2.14}$$

Where:

l_{s_x} is the length of the dielectric gap.

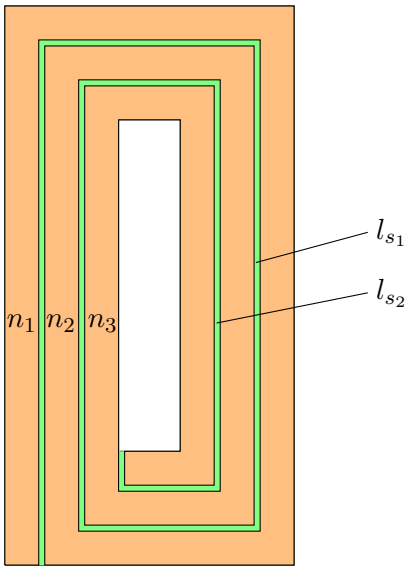
$K(\,)$ is a the complete elliptic integral of the first kind.

dn^{-1} The inverse Jacobi dn function.

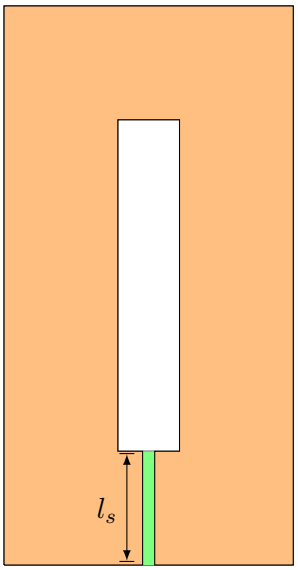
d (mm)	t (mm)	ϵ_r	w (mm)	Simulated (pF)	Calculated (pF)
0.25	0.5	5	1	33.00	32.86
0.25	1	5	1	41.11	41.68
0.5	0.25	5	2	15.49	15.26
0.5	0.25	100	2	309.84	307.19

TABLE 2.3: Comparison of simulated and calculated per-unit-length intra-layer capacitance values.

The effective intra-layer capacitance per-layer is found by considering the spiral geometry of the conductor when there is more than one turn ($n > 1$). The capacitance C_{s_x} between a pair of spiral turns is calculated by taking into account the mean length l_{s_x} of two pairs of adjacent turns. For the case when there is only one turn, eq. (2.14) is used with $l_{s_x} = w$. The values of each capacitance between pairs of spiral turns will be slightly different due to the spiral nature of the geometry. Illustrations of a three-turn and one-turn spiral are shown in fig. 2.18a & fig. 2.18b respectively.



(a) Three turn layer ($n = 3$). l_{s_1} & l_{s_2} are the lengths of the separation between each turn as indicated.



(b) Single turn layer ($n = 1$). l_s is the length of the separation as indicated.

FIGURE 2.18: Illustrations of a 3-turn and a 1-turn winding layer.

A method to calculate the total intra-layer capacitance C_s involves taking the voltage distribution along the spiral winding into account. The voltage distribution along the length of the spiral can be said to be linear. It can be argued that the electrical field between the turns is constant due to the constant gradient of voltage distribution on each turn. The capacitance is then calculated by finding the total energy stored inside the spiral geometry.

Firstly, an expression for the total length of the winding l_{t_s} is derived in eq. (A.3e) in Appendix A, which takes into account the number of turns, the width of the conductor and the dielectric spacing between each turn. The gradient of the voltage drop is then given as $-\frac{V_a}{l_{t_s}}$, where $V_a = \frac{V_{app}}{N_L}$. Knowing the voltage gradient, the expression for the voltage drop across the spiral length can be derived as eq. (2.15a). The voltage differences at the starting points of each turn can be calculated by finding the cumulative lengths l_x of each spiral turn, with $l_x(1) = 0$, and are given in eq. (2.15b). The voltage differences between consecutive adjacent pairs of turns are given as eq. (2.15c). Lastly the mean lengths of the dielectric spacing between the turns are derived in eq. (2.15d). The positions of the voltage points $V_s(k)$ are illustrated in fig. 2.19.

$$V_{spiral} = -\frac{V_a}{l_{t_s}} x + V_a \tag{2.15a}$$

$$V_s(k) = -\frac{V_a}{l_{t_s}} l_x(k) + V_a \tag{2.15b}$$

$$V_{diff}(k) = V_s(k) - V_s(k+1), \;\; \{k \leq n-1\} \tag{2.15c}$$

$$l_s(k) = 0.5(l(k) + l(k+1)), \;\; \{k \leq n-1\} \tag{2.15d}$$

The electrical field strengths between two consecutive pairs of turns are then derived in eq. (2.16a), using the equivalent transformed displacement $2\zeta_b$. The total energy can then be readily calculated using the equivalent transformed area $2\zeta_a\zeta_b$ as given in eq. (2.16b), from which the equivalent capacitance can be calculated as given in eq. (2.16c). The capacitance value C_s does not change with respect to the value of V_a indicating that it is not a function of the applied voltage, as expected.

It is preferable to use this method to calculate the capacitance of the spiral as it takes into account the nature of electrical energy distribution within the spiral.

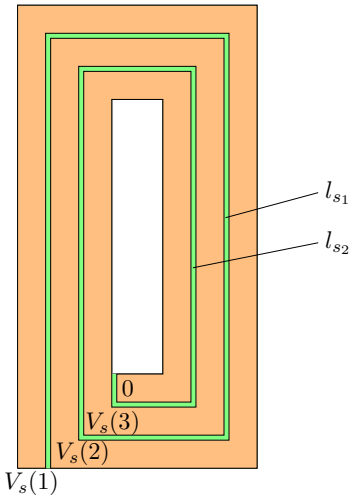


FIGURE 2.19: Three turn layer ($n = 3$). l_{s_1} & l_{s_2} are the lengths of the separation between each turn as indicated. The voltages of the starting points of each turn are indicated in the figure.

$$E_s(k) = \frac{V_{diff}(k)}{2\zeta_b}, \quad \{k \leq n-1\} \tag{2.16a}$$

$$W_s = \sum_{k=1}^{n-1} \epsilon_r \epsilon_0 \zeta_a 2\zeta_b l_s(k) E_x^2(k) \tag{2.16b}$$

$$C_s = \frac{2W_s}{V_a^2} \tag{2.16c}$$

The total intra-layer capacitance is found by method of summing the electrical energy in all layers. It may be noted that the capacitance/energy is doubled in all the layers except the two outermost layers due to the presence of dielectric material on both sides of the layers in the sandwich.

The total intra-layer energy can be described as given in eq. (2.17a). The total intra-layer capacitance is given in eq. (2.17b); it should be noted that C_{intra} is not in-fact a function of V_{app} as the variable cancels out after a full substitution.

$$W_{intra} = \begin{cases} 2W_s \,, & \text{if } N_L = 2 \\ 2W_s + 2(N_L - 2)W_s \,, & \text{if } N_L > 2 \end{cases} \tag{2.17a}$$

$$C_{intra} = \frac{2W_{intra}}{V_{app}^2} \tag{2.17b}$$

Single layer spiral windings with various turns n, conductor widths w, dielectric gap d and thickness t have been simulated in FEKO to compare simulated capacitance values to calculated values in table 2.4. It is found that the calculated values for the total intra-layer capacitance are in good agreement with the simulation results.

turns (n)	d (mm)	t (mm)	ϵ_r	w (mm)	Simulated (pF)	Calculated (pF)
1	0.5	1	1000	18.8	28.44	28.29
2	1	1	1000	8.90	301.23	268.50
3	0.25	1	1000	6.10	425.21	442.80
4	1	1	1000	3.95	201.40	208.60

TABLE 2.4: Comparison of simulated and calculated total intra-layer capacitance values for a single layer.

It is now important to see how the intra-layer capacitance compares with the inter-layer capacitance. For this, a pair of conductor strips are analysed. First, the pair of strips are placed adjacent to each other over a dielectric and their total capacitance is found. Next, the strips are placed parallel to each other, with their surfaces being perpendicular to each other. The two capacitances are then compared in table 2.5. It is found from this comparison that the intra-layer capacitance is relatively negligible, being approximately 2.7% of the inter-layer capacitance and can thus be ignored in most cases as the inter-layer capacitance and coupling capacitance would dominate in any high frequency effects. The intra-layer capacitance is therefore not taken into account for analysis presented here onwards.

Position	d (mm)	t (mm)	ϵ_r	w (mm)	length (m)	Capacitance (nF)
Adjacent	0.5	0.5	1000	10	1	4.72
Parallel	–	0.5	1000	10	1	177.08

TABLE 2.5: Comparison of inter-layer and intra-layer capacitance.

2.2.4 Validation of Self Capacitance and Winding Inductance Model

The proposed equivalent circuit model of the winding is shown in fig. 2.20. The total equivalent self-capacitance of the winding is the sum of the inter-layer capacitance and the intra-layer capacitance, as given in eq. (2.18).

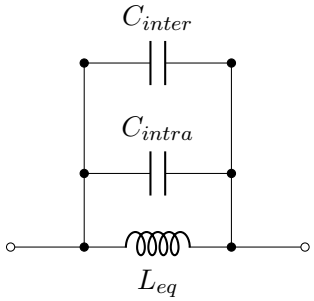


FIGURE 2.20: Equivalent circuit of a transformer winding.

$$C_{eq} = C_{intra} + C_{inter} \tag{2.18}$$

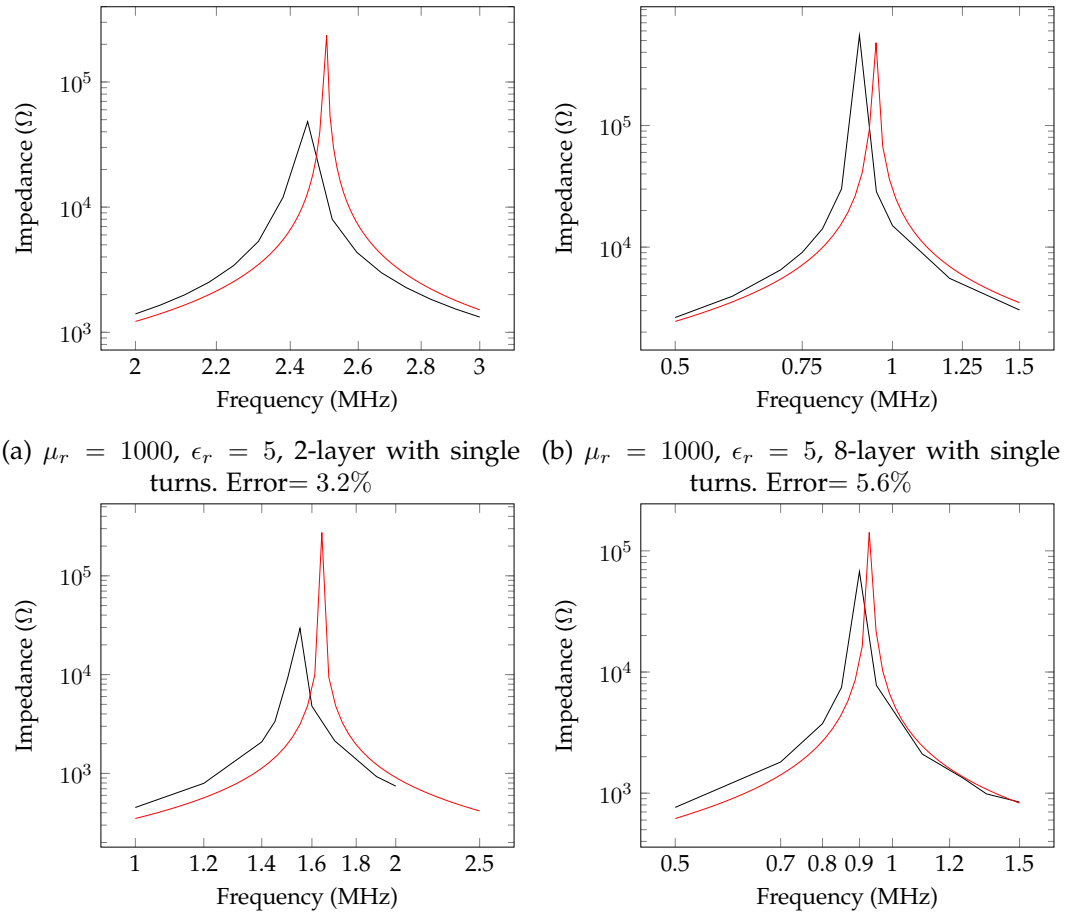
Various structures were simulated in FEKO; the details of these structures are given in fig. 2.21 and table C.1 in Appendix C. The equivalent capacitance and inductance values of these structures are given in table 2.6 using analytic expressions shown in previous sections. Using the values given in table 2.6, the equivalent resonant tank models (shown in fig. 2.20) were simulated in NgSpice.

The structures were constructed such that the intra-layer capacitance or inter-layer capacitance would resonate with the winding inductance in the presence of a core. Resonances of various winding arrangements are compared with resonances of their equivalent NgSpice circuits and plotted in fig. 2.21. The errors found are minimal, and are thought to arise from inaccuracies of geometry dimensions, insufficient meshing of FEKO models (see Appendix C for details).

Inspection of the plots in fig. 2.21 shows that the LC resonant tank model shown in fig. 2.20 is a good model for the planar winding. The errors are calculated by comparing the resonance frequencies of the FEKO model and the NgSpice model.

L-C Circuit	L (µH)	C (pF)
a	32.6	120.0
b	522.4	50.5
c	32.6	295.0
d	130.6	230.0

TABLE 2.6: Table showing values of self capacitance and inductances of equivalent circuit.



(a) $\mu_r = 1000$, $\epsilon_r = 5$, 2-layer with single turns. Error= 3.2%

(b) $\mu_r = 1000$, $\epsilon_r = 5$, 8-layer with single turns. Error= 5.6%

(c) $\mu_r = 1000$, $\epsilon_r = 1000$, 1-layer with 2-turns, $d = 0.5mm$. Error= 6.5%

(d) $\mu_r = 1000$, $\epsilon_r = 1000$, 1-layer with 4-turns, $d = 1mm$. Error= 3.41%

FIGURE 2.21: Comparison of simulated winding impedance with modelled impedance in the frequency domain of various windings. Dielectric layer and Core dimensions used in simulation presented in Appendix C.

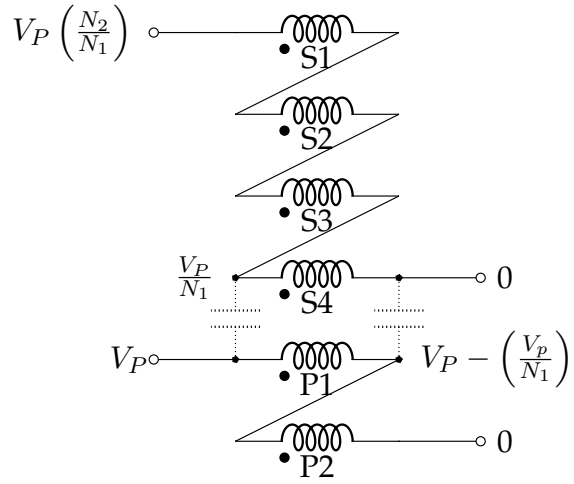


FIGURE 2.22: Circuit model showing the equivalent voltage drops over each layer of a 2:4 transformer. The energy stored in the coupling capacitance C_k is based on the electric field located between layers S4 & P1.

2.2.5 Coupling Capacitance

The coupling capacitance C_k (inter-winding capacitance) between the primary and secondary winding can be found by analysing the voltage distribution along the layers of each respective winding that lie on opposing sides of the dielectric that separates them; these would be layers S4 and P1 in fig. 2.22. The potentials along layers P1 and S4 are given as a function of turn length x in eq. (2.19) & eq. (2.19b) respectively. It is assumed that each turn length is l_t long. The voltage difference found along the length of the separating dielectric is given in eq. (2.19c); the associated electric field is given in eq. (2.20). The coupling capacitance C_k is given in eq. (2.21).

$$V_b(x) = -\frac{V_P}{N_1 l_t}x + V_P = V_P\left(1 - \frac{1}{N_1 l_t}x\right) \tag{2.19a}$$

$$V_a(x) = -V_P\frac{\frac{N_2}{N_1}}{N_2 l_t}x + V_P\frac{\frac{N_2}{N_1}}{N_2} = \frac{V_P}{N_1}(1 - \frac{x}{l_t}) \tag{2.19b}$$

$$V_d = |V_a(x) - V_b(x)| = \left| V_P \left(\frac{N_1 - 1}{N_1} \right) \right| \tag{2.19c}$$

$$E(x) = \frac{V_d}{t} \tag{2.20}$$

$$C_k = \frac{\epsilon_0 \epsilon_r \int E^2(x)\, dV}{V_d^2} = \epsilon_0 \epsilon_r \, \frac{l_t \, w}{t} \tag{2.21}$$

Where:

V_a is the potential distribution of the layer in the secondary winding at the interface of the dielectric that separates the primary and secondary windings.

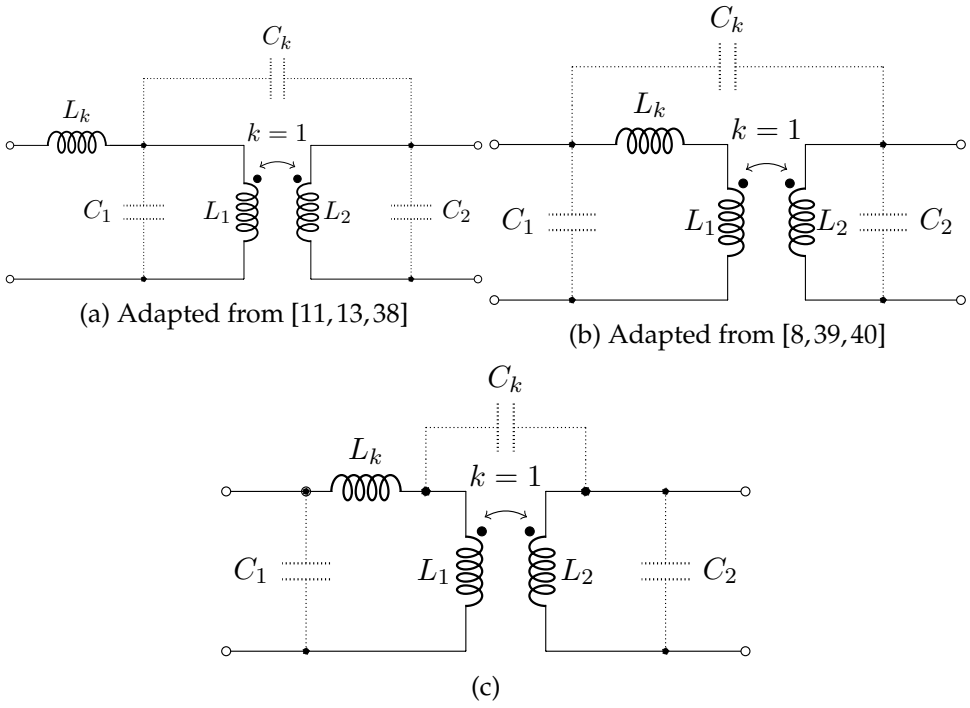
V_b is the potential distribution of the layer in the primary winding at the interface of the dielectric that separates the primary and secondary windings.

V_d is the potential difference across the dielectric that separates the primary and secondary winding.

It may be noted that although the capacitance was calculated by grounding the primary and secondary windings, the capacitance calculation should still hold true if they did not share the same ground as the voltage difference along the length of layers S4 and P1 would have cancelled out when substituted into eq. (2.21).

It is found from eq. (2.21) that the coupling capacitance is merely a parallel-plate capacitance based on the overlapping surface area of the primary and secondary windings. When the winding layers have more than one turn per layer ($n > 1$), the equation for the coupling capacitance can be adapted by changing the effective surface area of the capacitance. This is done by substituting l_t with l_{t_s}, which is the total length of the spiral. It may be noted that the expression given in eq. (2.21) only holds true when all layers in the transformer have the same number of turns.

2.3 Transformer Circuit Model Validation



(a) Adapted from [11,13,38]

(b) Adapted from [8,39,40]

(c)

FIGURE 2.23: Candidate equivalent circuit models for planar transformers.

Two candidate equivalent circuit models have been chosen from literature along with one proposed model fig. 2.23c; these models are shown in fig. 2.23 and have been modified to present direct coupling between the primary and secondary winding inductance. The proposed model is presented in this research as such a model has not been found or analysed in literature. These models were chosen because they allow the leakage inductance to be specified. However, the placement of the leakage inductance within the circuit model needs to be verified using simulation. The frequency response of the models are compared to simulation results of the FEKO models to find which model is most suitable to work with (explained later in summary, context given in section 2.1.1).

Transformer models are constructed in FEKO, and are simulated to extract the primary source and secondary load currents in the frequency domain, from which

the source and load power can be calculated. The source and load power values are then plotted as functions of frequency. The reason the load and source power are plotted is because a plot of the impedance of the transformer referred to the primary side does not reveal information about the currents and voltages present in the secondary side of the transformer. Resonance-like behaviour is expected to be seen in the power plots; these resonance-like regions indicate where the transformer's secondary side voltage no longer follows the transformer's voltage ratio. The bandwidth is thus defined as the frequency range beyond which the transformer no longer acts as a transformer, in terms of the voltage and currents no longer following the transformer ratio. The bandwidth is described more in detail in chapter three.

The circuit models were simulated using NgSpice. The ground of the secondary side was connected to the ground of the primary side so as to overcome the matrix singularity error in spice. The 3D models of the transformer were simulated in FEKO using the MoM solver based on the Surface Equivalence Principle (SEP). Ideal (lossless and frequency independent) dielectric and ferrite materials with various permittivity and permeability constants respectively were used; ϵ_{r_1} is the permittivity of the dielectric within the primary and secondary windings, whereas ϵ_{r_2} is the relative permittivity of the dielectric separating the primary and secondary windings. Here also, the ground of the primary side is connected to the ground of the secondary side in order to resolve the voltage distributions within the transformer correctly; this is shown in fig. C.1 in Appendix C.

A 2:4 turn transformer and a 4:8 turn transformer has been simulated in FEKO with the specifications provided in table 2.7; the values of the circuit elements were calculated using the analytical expressions derived in this chapter and are provided in table 2.8. The results from these simulations are in shown in fig. 2.24, fig. 2.25 and fig. 2.26. The frequency response of the candidate equivalent circuits are given

in the same plots for comparison. It may be noted that the simulations were conducted only in the frequency range where the resonance-like 'knee-points' are expected to occur, to save on simulation resources. For simplicity of FEKO model construction, windings with single turns are used in the simulation. Windings with multiple-turns per layer would only change the values of the capacitances and inductances in the circuit model as discussed in previous sections. An arbitrary 50 ohm load was used for all simulations for purpose of demonstration. The dimensions of the core and the dielectric layers used in simulations are given in Appendix C.

It is to be noted that due to the inherent distributed nature of the capacitance and inductance elements within the transformer structure, one cannot perfectly capture the exact frequency response using a lumped model. It is also important to note that the simulation results may not be completely accurate due to the lack of computational resources to allow finer meshing. As it will become clear in the following chapter, the lumped model should be able to capture the position of the 'knee-point' frequency with sufficient accuracy; this is the point where the first resonance-like behaviour is observed.

Inspection of fig. 2.24 shows that the FEKO model matches the NgSpice model (a) fairly well. However, close inspection reveals that there is a slight mismatch of the source and load power plots. Inspection of fig. 2.25 shows that circuit model (b) presents higher order effects in the source and load power plots. These features would manifest as higher order terms in circuit mesh equations, making this model undesirable for derivation of analytical expressions. Finally, inspection of fig. 2.26 shows that the source and load power plots of the NgSpice model match the power plots of the FEKO simulation model fairly well, except for fig. 2.26a. However it is thought that this minor mismatch may be caused by inadequate meshing, seeing that such a mismatch does not occur for the other three NgSpice simulations of the same model. It may be further noted that the source power plots of the circuit

Turns Ratio	t (mm)	$\epsilon_{r_1}/\epsilon_{r_2}$	μ_r	l_t (mm)	w (mm)
2:4	0.4	5/1	1000	220	18.8
2:4	0.4	500/500	500	220	18.8
4:8	0.4	5/5	1000	220	18.8
4:8	0.4	500/1	500	220	18.8

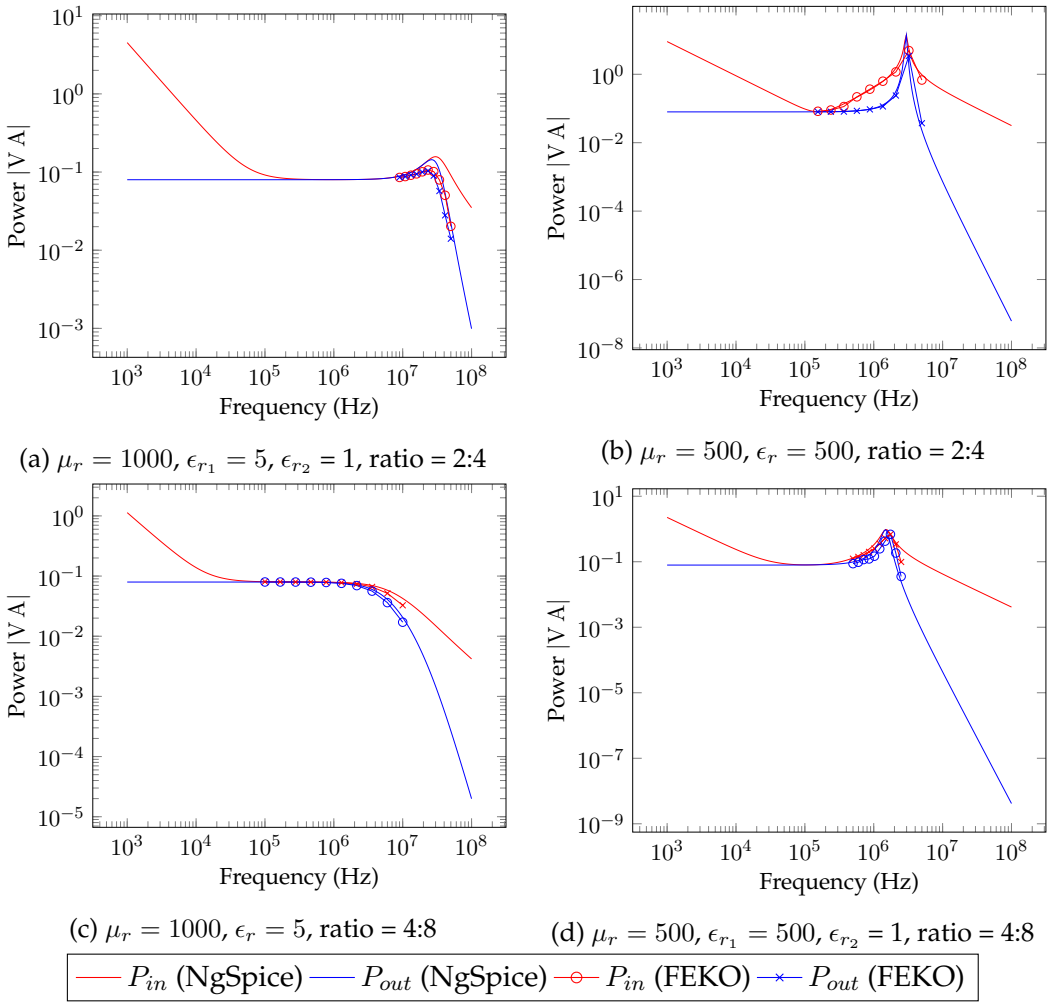
TABLE 2.7: Specifications of transformers simulated in FEKO.

Turns Ratio	$\epsilon_{r_1}/\epsilon_{r_2}$	μ_r	C_1 (pF)	C_2 (pF)	C_k (pF)	L_1 (µH)	L_2(µH)	L_k (nH)
2:4	5/1	1000	115.27	86.45	92.21	35.10	140.40	50.36
2:4	500/500	500	11.527×10^3	8.645×10^3	46.110×10^3	17.55	70.20	50.36
4:8	5/5	1000	86.45	50.43	461.10	140.40	561.63	385.12
4:8	500/1	500	8.645×10^3	5.043×10^3	92.21	70.20	280.81	385.12

TABLE 2.8: Values of elements in the circuit models of the planar transformer.

model (c) in fig. 2.26 presents higher order effects. However, these higher order features are acceptable, seeing that these features do not appear in the load power plot. This would mean that the analytical expressions derived from this circuit model would be manageable yet accurate. For details regarding the simulation meshing, refer to Appendix C.

Based on the observations made previously, the circuit model shown in fig. 2.23c appears to be the best model suitable for derivation of analytical expressions.



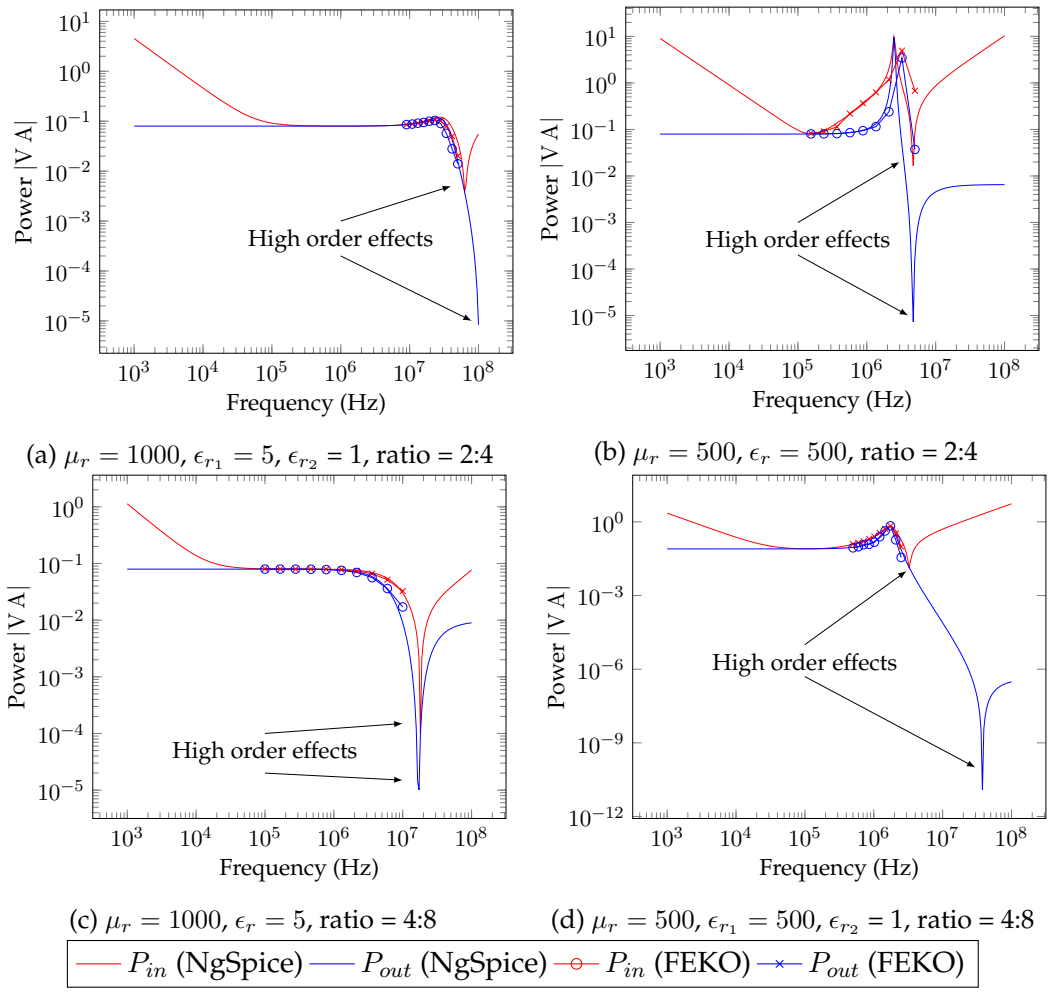
(a) $\mu_r = 1000$, $\epsilon_{r_1} = 5$, ϵ_{r_2} = 1, ratio = 2:4

(b) $\mu_r = 500$, $\epsilon_r = 500$, ratio = 2:4

(c) $\mu_r = 1000$, $\epsilon_r = 5$, ratio = 4:8

(d) $\mu_r = 500$, $\epsilon_{r_1} = 500$, ϵ_{r_2} = 1, ratio = 4:8

FIGURE 2.24: Comparison of power response in the frequency domain of model (a) against FEKO results. FEKO results are plotted with markers.



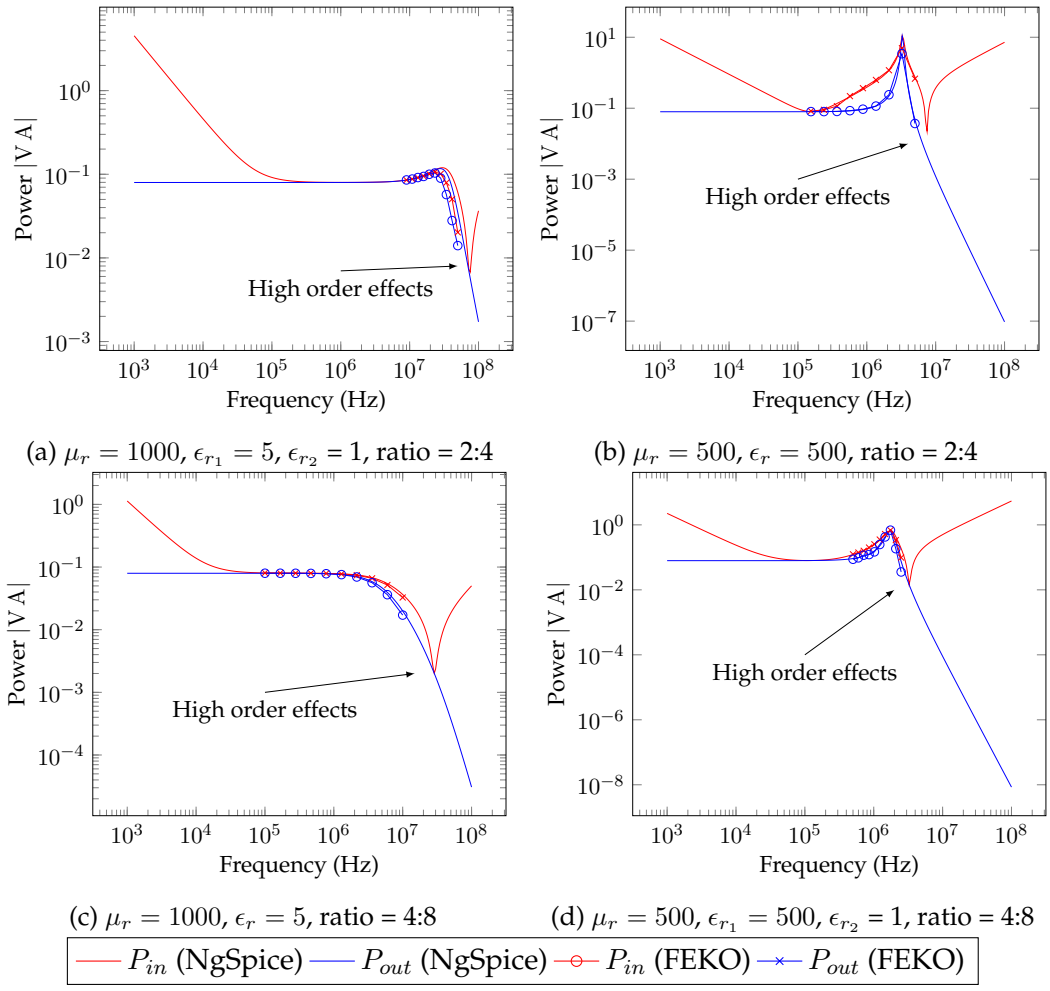
(a) $\mu_r = 1000$, $\epsilon_{r_1} = 5$, ϵ_{r_2} = 1, ratio = 2:4

(b) $\mu_r = 500$, $\epsilon_r = 500$, ratio = 2:4

(c) $\mu_r = 1000$, $\epsilon_r = 5$, ratio = 4:8

(d) $\mu_r = 500$, $\epsilon_{r_1} = 500$, ϵ_{r_2} = 1, ratio = 4:8

FIGURE 2.25: Comparison of power response in the frequency domain of model (b) against FEKO results. FEKO results are plotted with markers.



(a) $\mu_r = 1000$, $\epsilon_{r_1} = 5$, ϵ_{r_2} = 1, ratio = 2:4

(b) $\mu_r = 500$, $\epsilon_r = 500$, ratio = 2:4

(c) $\mu_r = 1000$, $\epsilon_r = 5$, ratio = 4:8

(d) $\mu_r = 500$, $\epsilon_{r_1} = 500$, ϵ_{r_2} = 1, ratio = 4:8

FIGURE 2.26: Comparison of power response in the frequency domain of model (c) against FEKO results. FEKO results are plotted with markers.

2.4 Summary

The inter-layer, intra-layer and coupling capacitance, and the leakage inductance have all been described as expressions based on the thickness of the dielectric. Based on this, it is understood that there is energy circulating within the dielectric space due to the inductive and capacitance parasitics, which leads to resonance-like behaviour that limits the transformer's bandwidth. The bandwidth in this case is defined as the frequency range beyond which the transformer output no longer follows the transformer ratio. These inductive and capacitive parasitics have been modelled using physical dimensions as parameters. The nature of the effect of the parasitics on the bandwidth is described in the following chapter.

Furthermore it has been shown that the capacitance that arises out of the spiral nature of the windings is negligible compared to the inter-layer capacitance, and can be ignored in most cases. Even though this result might seem obvious, it was necessary to prove it mathematically. It can be argued that even in the case where there is only a single layer and a single turn on the secondary side, the intra-layer capacitance will be relatively much smaller than the coupling capacitance C_k, due to the overlapping surface area between primary and secondary winding, and can thus be ignored. This is further explained in section 3.6.2 in Chapter three. However, the analytical geometrical approximation of the spiral derived in this chapter could prove useful in future studies.

Finally, a suitable equivalent electrical circuit model of a transformer has been chosen. The parameters that have been taken into account that lead to this decision are:

- The model is generally in good agreement with simulation.
- The mesh equations in the model are not expected to be relatively unwieldy, and also not lack too much in complexity, which otherwise could lead to loss of potential information about the knee-point frequency.

Chapter 3

Transformer Design for Optimized Bandwidth

It has been established in chapter two that there is energy circulation/storage in the winding volume of the transformer. This energy is circulated through the leakage inductance and parasitic capacitance, which are both functions of dielectric thickness. It is therefore meaningless to find the absolute limits for the parasitic capacitances and the leakage inductance individually, as certain values for capacitance and leakage inductance cannot co-exist given a unique set of physical dimensions. A better approach would be to find the effect of the dielectric thickness, which is common to both parasitics, and evaluate its effect on the frequency response of the transformer.

This chapter presents a method of designing transformers by taking into account the effect of parasitics on the bandwidth of the transformer. In the process, the effect of dielectric thickness on the bandwidth is analysed. Emphasis is placed on deriving analytical expressions that describe the influence of dielectric thickness on the bandwidth such that a closed form solution for the limits of the dielectric thickness can be found. All expressions derived in this chapter will thus originate from the circuit model chosen in the previous chapter (presented again in the following section).

3.1 Equivalent Circuit Mesh Equations

It was found in the previous chapter that the transformer exhibited resonant-like behaviour when the input and output power waveforms were plotted against frequency. This behaviour can be analysed by studying the voltages and currents within the transformer. In light of this, a good metric for observing resonant-like behaviour is power since information of both current and voltage are enclosed within it.

The input and output power expressions of the transformer circuit can be found by setting up mesh equations using the mesh current loops shown in fig. 3.1. The mesh equations are given in eq. (3.1). Note that the coupling capacitor C_k has been split into two halves, to maintain the symmetry of the circuit in order to complete the loop for mesh current I_3.

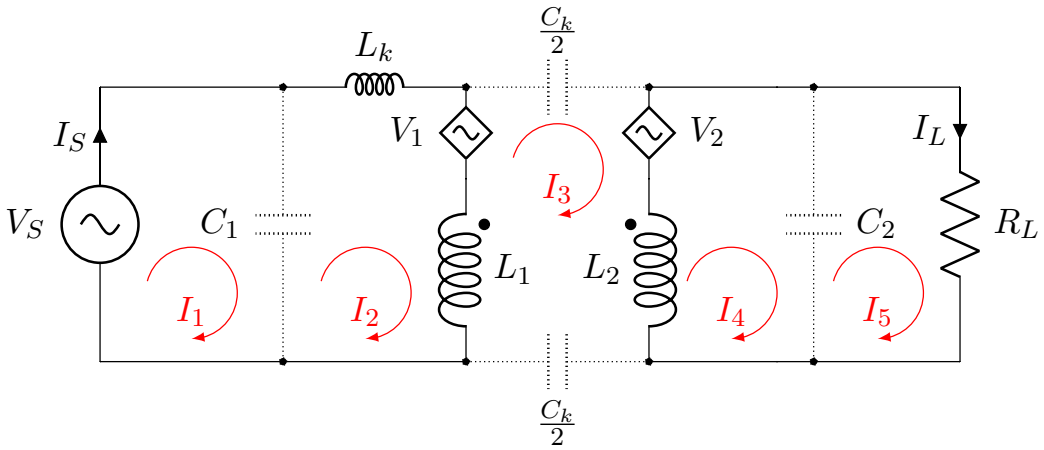


FIGURE 3.1: Transformer equivalent circuit model showing mesh current loops. C_k has been split in half based on geometry.

$$M = k\sqrt{L_1 L_2},\ k = 1 \tag{3.1a}$$

$$V_1 = j\omega M(I_3 - I_4) \tag{3.1b}$$

$$V_2 = j\omega M(I_2 - I_3) \tag{3.1c}$$

$$V_S = \frac{I_1 - I_2}{j\omega C_1} \tag{3.1d}$$

$$0 = \frac{I_2 - I_1}{j\omega C_1} + I_2 L_k + V_1 + (I_2 - I_1)L_2 \tag{3.1e}$$

$$0 = (I_3 - I_2)L_1 + (I_3 - I_4)L_2 + 2\frac{I_3}{0.5j\omega C_k} - V_1 + V_2 \tag{3.1f}$$

$$0 = (I_4 - I_3)L_2 - V_2 + \frac{(I_4 - I_5)}{j\omega C_2} \tag{3.1g}$$

$$0 = \frac{(I_5 - I_4)}{j\omega C_2} + I_5 R_L \tag{3.1h}$$

The source current I_1 and load current I_5 can be solved from these mesh equations and denoted as I_S and I_L respectively in fig. 3.1. The power expressions can then be given as eq. (3.2); the solutions of which are described in Appendix A. The impedance of the transformer as referred by the source is given in eq. (3.2c). It may be noted that the load power is given in units of VA even though it is dissipated by a purely real impedance, for sake of convention.

$$|P_L(\omega)| = |I_L^2(\omega)|R_L \qquad [\text{V A}] \tag{3.2a}$$

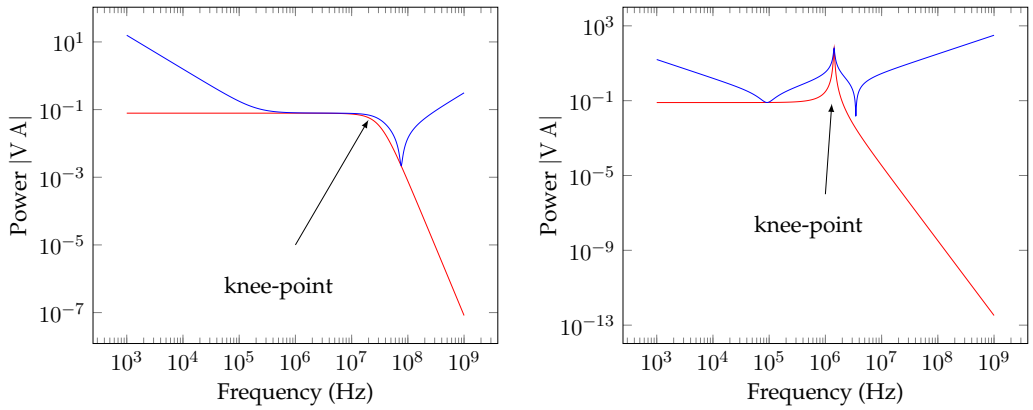
$$|P_S(\omega)| = |I_S(\omega)||V_S| \qquad [\text{V A}] \tag{3.2b}$$

$$X_T(\omega) = \frac{V_s}{|I_s(\omega)|} \tag{3.2c}$$

3.2 The Bandwidth

The source and load power waveforms P_S & P_L are plotted in fig. 3.2a & fig. 3.2b with arbitrary values of $L_k, C_1, C_k, C_2, L_1, L_2$ & R_L in order to visualise the frequency response of the transformer; the knee points of the load power are also indicated in the plots.

The bandwidth (knee-point) is defined as the frequency beyond which the load power P_L either starts resonating or 'rolling' off. This indicates the point beyond



(a) Plot showing a rounded knee-point of the load power P_L.

(b) Plot showing a sharp knee-point of the load power P_L.

FIGURE 3.2: Plots of source and load power plotting against frequency. Note that the converging P_L and P_S merely indicates unity power-factor and not unity efficiency.

which the currents and voltages of the secondary side are not following the transformer turns ratio. This is an important metric to gauge whether a transformer is operating ideally (concept of ideal transformer is derived from assumptions and constraints described in chapter one), as the turns ratio is a fundamental attribute of a transformer. The bandwidth phenomenon can be observed to occur in both FEKO simulation and NgSpice simulation (in previous chapter). Emphasis is placed on analysing the load power as the change in turns ratio is observed at the knee-point of load power plot. The source power also exhibits resonance-like behaviour at the same frequency point, however it exhibits other resonances as well, and solving for these resonances might be mathematically unwieldy.

The power waveform at the knee-point frequency shows resonance-like characteristics with the q-factor either being high or low; the location of the knee-point can be difficult to find when the q-factor is low. However, the exact frequency can be found by analysing the poles and zeros of the load power expression given in eq. (B.1b) in Appendix B. The expression given in eq. (B.1b) under the square exponent is a fourth order polynomial. It is possible to solve this polynomial for its

roots using the method of suppression, however the result is expected to be unwieldy. The exact roots can be found numerically but this defeats the objective of finding an analytical solution. An approximation for the denominator of the load power expression is thus presented in eq. (3.3). The resultant approximated load power function is plotted against the original function in fig. B.1 in Appendix B for various parameter values; inspection of these plots shows that the approximation matches the original function well. With this approximation, it is now possible to derive closed form analytical expressions from the load power expression.

$$\left|P'_{L_{denom}}(\omega)\right| = \Big| -\Big((C_k L_k(L_1 - 2M) - (4C_2 + C_k)M^2 + (4C_2 + C_k))(L_1 + L_k)\omega^2 + 4j(L_1L_2 + L_2L_k - M^2)\omega + 4R_L(L_1 + L_k)\Big)^2\Big| \tag{3.3}$$

3.3 Optimum Dielectric Thickness

To find the relationship between bandwidth and dielectric thickness, the load power function must be re-written as a function of dielectric thickness t.

Expressions for the inter-layer capacitance, coupling capacitances and leakage inductance are given in eq. (3.4a), eq. (3.4b) & eq. (3.4c) respectively as functions of thickness t with parasitic coefficients denoted with subscript 'c'. These expressions are derived based on the assumption that all layers of the primary and secondary windings are identical (equal turns, dielectric thickness and dielectric spacing between turns). A further assumption is made that every layer has a single turn for simplification (the track width w can always be later expressed as a fraction of the core window width b_w, in this case $w = b_w$). Another assumption is that the intra-layer capacitance is ignored. The reasoning for these assumptions are discussed later in section 3.6.5, to maintain focus on the derivations.

$$C_{inter} = \epsilon_0 \epsilon_r \frac{l_t b_w}{t}\left(\frac{N_L - 1}{N_L^2}\right) = \frac{1}{t}(C_{i_c}) \tag{3.4a}$$

$$C_k = \epsilon_0 \epsilon_r \frac{l_t\, b_w}{t} = \frac{1}{t}(C_{k_c}) \tag{3.4b}$$

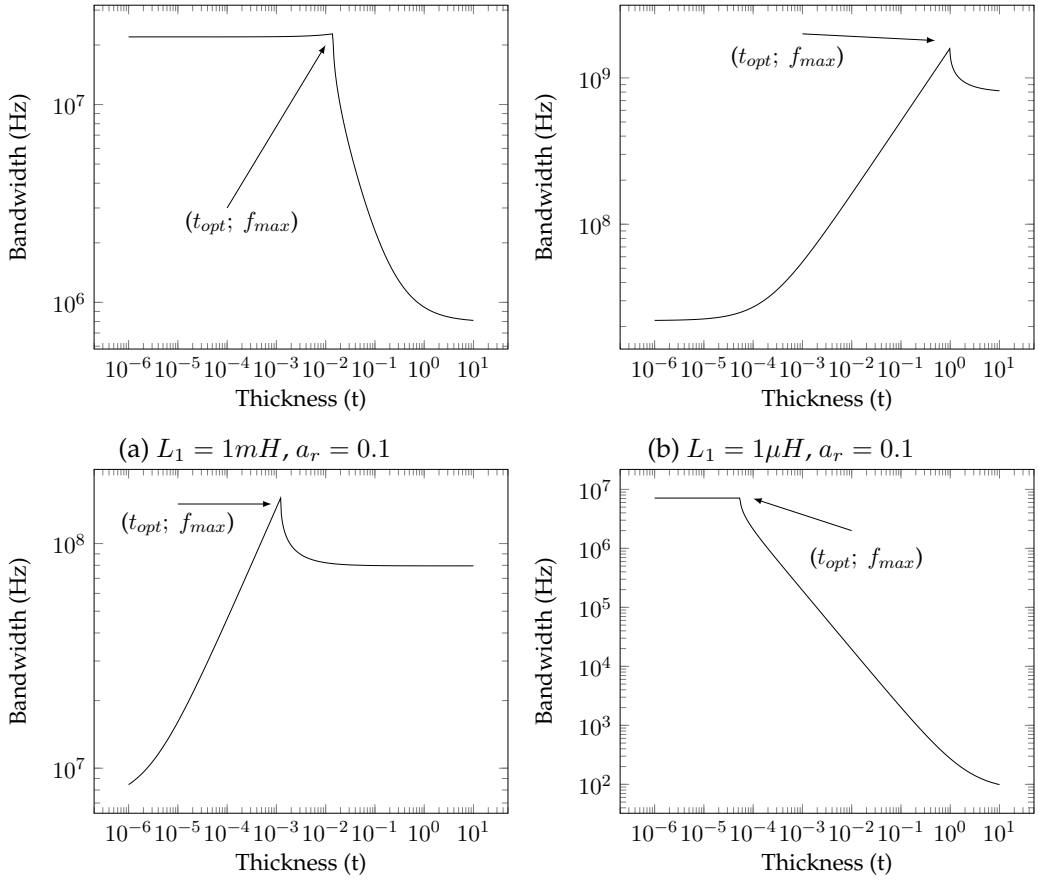
$$L_k = \frac{\mu_0\, l_t\, n^2}{b_w} \left[t \sum_{y=1}^{N_{LP}-1} y^2 + t\, N_{LP}^2 + t \left(\frac{N_{LP}}{N_{LS}} \right)^2 \left(\sum_{z=1}^{N_{LS}-1} z^2 \right) \right] = t(L_{k_c}) \tag{3.4c}$$

Inspection of these expressions show the opposing nature of the capacitive and inductive parasitics to changes in dielectric thickness t. It is therefore especially important to understand how the dielectric thickness affects the parasitics, which in turn affects the bandwidth. To analyse this, the parasitics C_1, C_2, C_k & L_k in eq. (3.3) are re-written as a function of the dielectric thickness t in eq. (3.5); the coefficients of this polynomial are defined in eq. (B.4b) in Appendix B.

$$\left| P'_{L_{denom}}(t, \omega) \right| = \left| \left(a\omega^2 + b\omega + c \right)^2 \right| \tag{3.5}$$

The exact bandwidth at which the load power starts exhibiting resonant-like behaviour can be found as the frequency roots of eq. (3.5), and are given in eq. (B.4b) as functions of t. These roots are plotted for various primary winding inductance values in fig. 3.3; here a_r represents turns ratio (not to be confused with the coefficients presented in eq. (3.6b) or Appendix B). Inspection of these plots reveals that the bandwidth is the highest at a certain value of t, as indicated on the plots; solving for this point will result in finding the optimum thickness t_{opt} and by extension the optimized bandwidth f_{max}. There are some cases such as fig. 3.3d where the bandwidth stays constant when the thickness value is less than t_{opt}; in such cases, t_{opt} actually becomes the maximum thickness value t_{max}. This will be explored in further detail later in the section.

The value of t_{opt} is found by evaluating the auxiliary function given in eq. (B.6a), which can then be simplified to eq. (B.6c); this function can be solved for t to give t_{opt}. The solution of t_{opt} & f_{max}, is given in eq. (3.6a) & eq. (3.6b) respectively; coefficients are defined in eq. (B.6b) and eq. (B.4b) respectively in Appendix B.



(a) $L_1 = 1mH$, $a_r = 0.1$

(b) $L_1 = 1\mu H$, $a_r = 0.1$

(c) $L_1 = 1nH$, $a_r = 10$

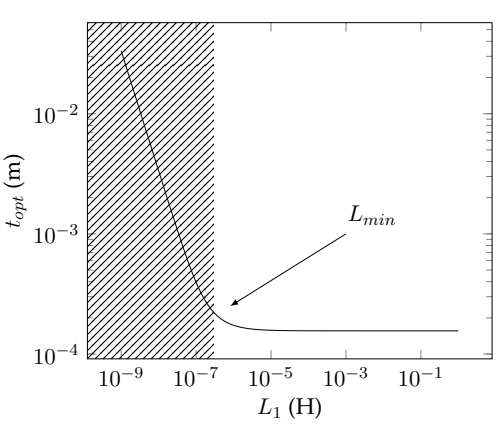
(d) $L_1 = 1mH$, $a_r = 10$

FIGURE 3.3: Plots showing effect of dielectric thickness on the bandwidth of the transformer's load power. Plots with various winding inductances are shown. The variable a_r represents the turns ratio of the transformer.

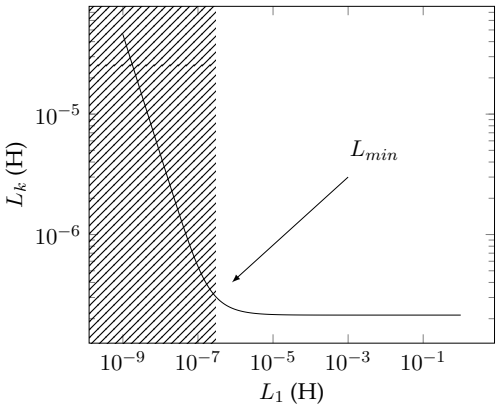
$$t_{opt} = \left| \frac{-b_x - \sqrt{b_x^2 - 4a_x c_x}}{2a_x} \right| \tag{3.6a}$$

$$f_{max} = \left| \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \right|_{t=t_{opt}} \tag{3.6b}$$

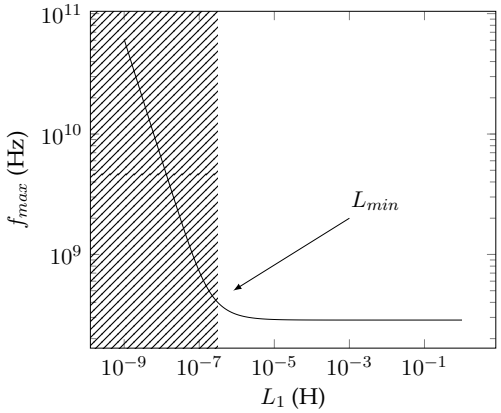
Inspection of coefficients in eq. (B.6b) shows that t_{opt} is a function of the turns ratio a, winding inductance L_1 and load R_L; typically a and R_L are given as requirements, leaving the designer to choose L_1. Plots showing the influence of winding inductance L_1 values on the optimum thickness and optimum frequency range are shown in fig. 3.4.



(a) Influence of winding inductance on t_{opt}.



(b) Influence of winding inductance on optimum Leakage inductance L_k.



(c) Influence of winding inductance on bandwidth f_{max}.

FIGURE 3.4: Plots showing the influence of winding inductance on various optimum values with arbitrary parameters. The shaded region represents values that are not feasible.

Inspection of fig. 3.4 shows that f_{max}, t_{opt} do not change much beyond the knee-points on the plots. The winding inductance value L_{knee} of knee-point can either be found as the roots of the f_{max} function or the t_{opt} function as they co-exist as

a single coordinate; the t_{opt} function is chosen for convenience. L_{knee} is found by considering the expression given in eq. (B.7a) in Appendix B; the expression can be rewritten as a function of L_1 and solved, giving eq. (3.7).

$$L_{knee} = \left| \frac{R_L \sqrt{L_{k_c}(-4C_{2_c}a_r^2 - C_{k_c}(a_r^2 - 2a_r + 1))}}{2a_r^2} \right| \tag{3.7}$$

$$t'_{opt} \leq t_{max} \leq \lim_{L_1 \to \infty} t_{opt} \leq \left| \frac{R_L \sqrt{(4C_{2_c} + C_{k_c})a_r^2 - 2C_{k_c}a_r + C_{k_c}}}{\sqrt{L_{k_c}}a_r^2} \right| \tag{3.8a}$$

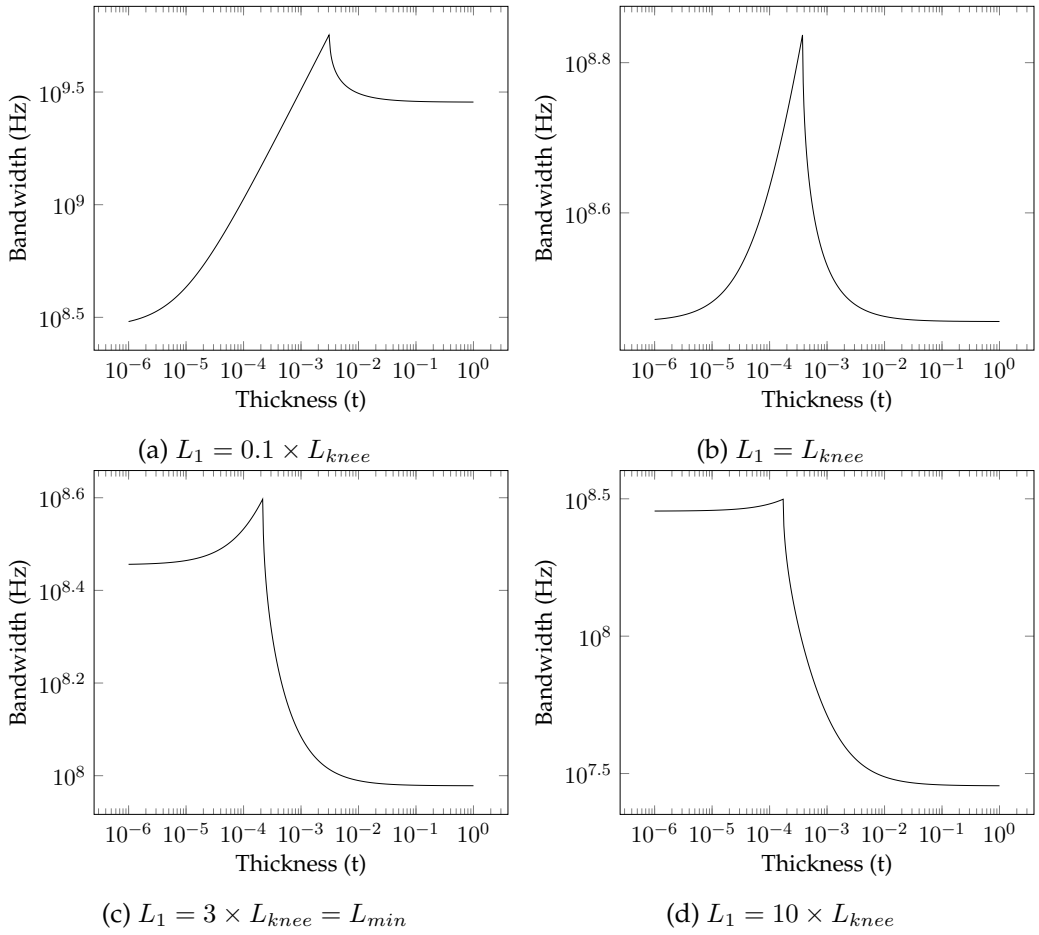
$$f'_{max} = \lim_{L_1 \to \infty} f_{max} = \left| \frac{2jL_{k_c}a_r^2 t'_{opt} + 2\sqrt{(L_{k_c}a_r^4 t'^2_{opt} + ((4C_{2_c} + C_{k_c})a_r^2 - C_{k_c}(2a_r - 1))R_L^2)L_{k_c}}}{((4C_{2_c} + C_{k_c})L_{k_c}a_r^2 - 2C_{k_c}L_{k_c}a_r + C_{k_c}L_{k_c})R_L} \right| \tag{3.8b}$$

The winding inductance L_{knee} has been established; this is the winding inductance value that results in the knee-point of the plots in fig. 3.4. It is found that the region left of the boundary drawn on the plot is not physically realisable. The reason for this is that the winding inductance values inside of the shaded boundary at ($L_1 \leq 3 \times L_{knee}$) gives rise to optimum thickness values that result in leakage inductance values that are higher than the winding inductance; although this is possible on a circuit model from which the expressions are derived, it is impossible in a real transformer. The minimum feasable primary winding inductance for a given transformer configuration is thus found as $L_{min} = 3L_{knee}$.

Furthermore it is found that both t_{opt} and f_{max} approach their respective asymptotes as the winding inductance increases past L_{knee}. These asymptote values can be found as given in eq. (3.8a) & eq. (3.8b). These asymptote values are useful as the optimum thickness and bandwidth values can be readily calculated using closed form expressions if the winding inductance is much greater than L_{knee} (at least 10 times greater). This is usually the case as inclusion of a core will drastically increase the winding inductance.

It is further found that when the winding inductance L_1 is much greater than L_{knee}, the optimum thickness effectively becomes the maximum thickness t_{max}. It is found that in these cases, choosing a thickness less than t_{opt} has a negligible impact on the bandwidth.

Plots showing influence of dielectric thickness on bandwidth for various values of winding inductance L_1 are shown in fig. 3.5; the winding inductances have been chosen in such a way that it is possible to see what happens when the winding inductance value is smaller or larger than L_{knee}. It can be seen from these plots that as the winding inductance becomes much greater than L_{knee}, the bandwidth no longer becomes a function of thickness below the threshold t_{opt} ; t_{opt} thus effectively becoming t_{max}.



(a) $L_1 = 0.1 \times L_{knee}$ (b) $L_1 = L_{knee}$

(c) $L_1 = 3 \times L_{knee} = L_{min}$ (d) $L_1 = 10 \times L_{knee}$

FIGURE 3.5: Plots showing effect of dielectric thickness on the bandwidth of the transformer for various values of L_1 (smaller and larger than L_{knee}). Arbitrary parasitic coefficients used.

3.4 Planar Transformer Design

3.4.1 Dielectric Layer & Core Design

This section uses time-domain analysis to find the minimum core area required to prevent flux saturation in the transformer core. Assuming that a square wave is applied with a frequency f of duty cycle D, the time t_{on} that the applied voltage V_p is at peak value is given as eq. (3.9); the reader may note that the transfer function of the transformer is applicable to the harmonics of this square wave. The expression for peak flux ϕ_p is given in eq. (3.10a). According to Faraday's Law, the expression for ϕ_p is also given as eq. (3.10b)(where dt is delta time). From eq. (3.10a) & eq. (3.10b), the minimum cross sectional area A_ϕ for the magnetic flux to pass through the core to avoid saturation is given as eq. (3.10c). It should be noted that D is practically always 0.5 to prevent saturation of the core, due to drifting magnetic flux.

$$t_{on} = \frac{D}{f} \tag{3.9}$$

$$|\phi_p| = B_{peak} A_\phi \tag{3.10a}$$

$$|\phi_p| = \left| \frac{\int V_p \mathrm{dt}}{-2N} \right| = \frac{V_p t_{on}}{2N} = B_{peak} A_\phi \tag{3.10b}$$

$$A_\phi \geq \frac{V_p D}{2 f N B_{peak}} \tag{3.10c}$$

The dielectric layer must then accommodate for this area by selection of either l_c or l_w (illustrated in fig. A.1 in Appendix A) such that the product is equal to A as given by eq. (3.10c); l_c or l_w must be less than $\sqrt{A_\phi}$ to maintain planar form. The width of the core window b_w can then be chosen, after which the dimensions of the dielectric layer D_l & D_w can be calculated as given in eq. (A.1a) & eq. (A.1b).

The total inductance is given as eq. (3.11a) from chapter two; l_m is given as eq. (3.11b), where t' is given in eq. (3.11c). The effective area A_ϕ of the core will then be equal to or greater than the minimum area requirement calculated from

eq. (3.10c) to prevent core saturation.

$$L_{eq} = \begin{cases} \frac{\mu_0 \mu_r n^2 A_\phi \left(N_L + 2\binom{N_L}{2}\right)}{l_m} \text{ if } N_L > 1 \\ \frac{\mu_0 \mu_r n^2 A_\phi}{l_m} \text{ if } N_L = 1 \end{cases} \tag{3.11a}$$

$$l_m = 2(t' + b_w + 2l_w) \tag{3.11b}$$

$$t' = t_{opt}(N_1 + N_2 - 1) \tag{3.11c}$$

It is understood that at this stage, the core volume has been optimised such as to present the smallest volume possible without allowing the core to saturate; the core volume is also optimised to an extent as a result of the volume optimisation of the winding structure due to the choice of optimum thickness t_{opt}.

3.4.2 Design Procedure

Since the turns ratio and load resistance are pre-defined as requirements, the goal is to choose n, N_1, & b_w such that the design process results in favourable dielectric thickness t_{opt} and optimum operating frequency range f_{max} values. However, t_{opt} does not guarantee a planar form. For this condition to be met, the requirement given in eq. (3.12) must be satisfied. This can be done by increasing the turns-per-layer n of each winding.

$$\frac{b_w}{t_{opt}(N_1 + N_2 - 1)} \geq 1 \tag{3.12}$$

The value of the minimum effective area for the core is first calculated in the design process; the dielectric geometry is then defined based on this. Next, t_{opt} is calculated after which f_{max} can be calculated. It is important to realize that as the calculated L_1 is generally going to be much greater than L_{min}, the asymptotes f'_{max} and t'_{opt} can be used instead of f_{max} and t_{opt}.

The process flow-chart shown in fig. 3.6 describes the design process of an optimized planar transformer.

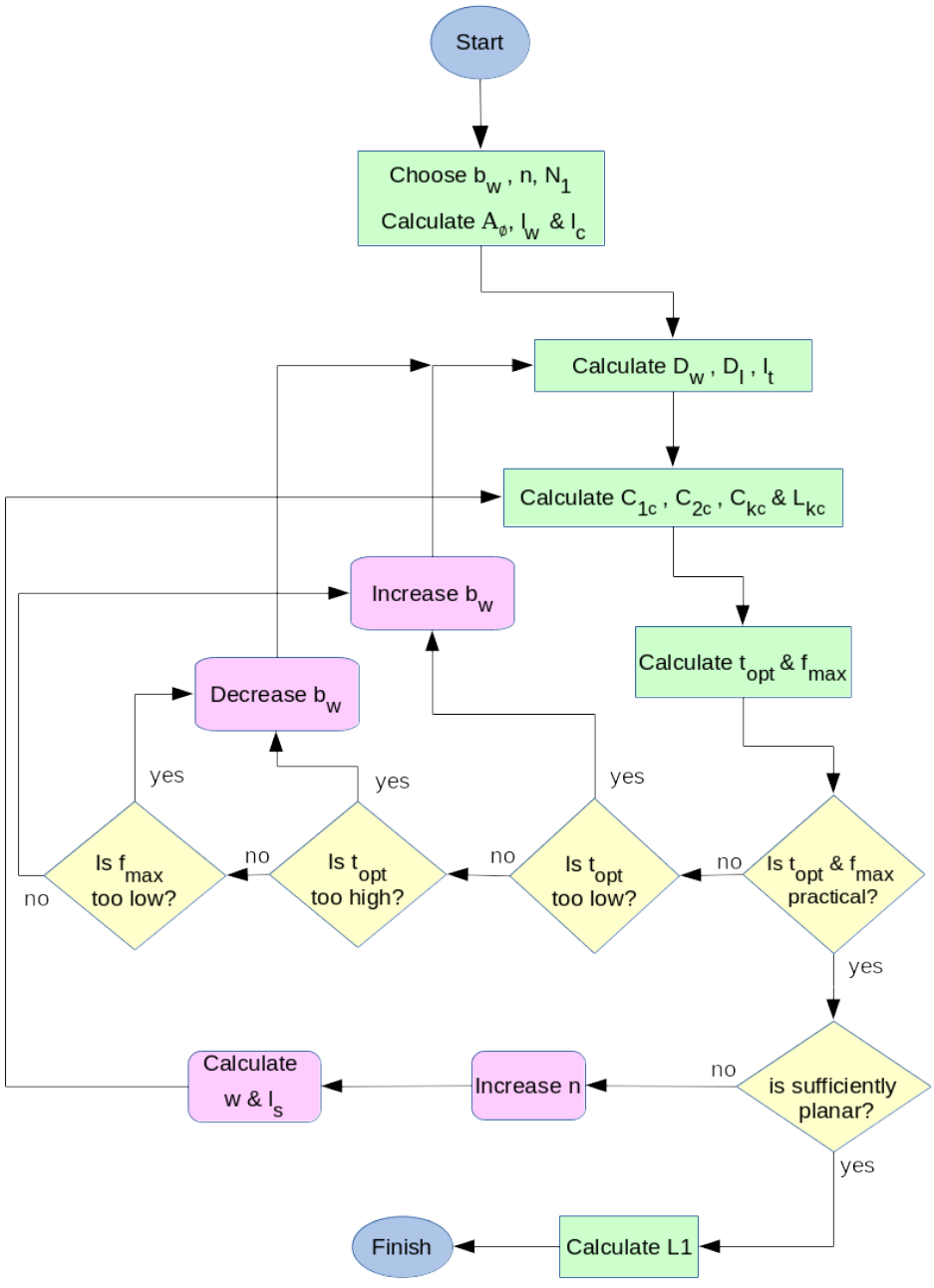


FIGURE 3.6: Design process of an planar transformer with optimized bandwidth and dielectric thickness.

3.5 Design Example

A 4:1 low power, high frequency transformer is designed as an example using the design procedure shown in this chapter. The specifications of the transformer are given in table 3.1.

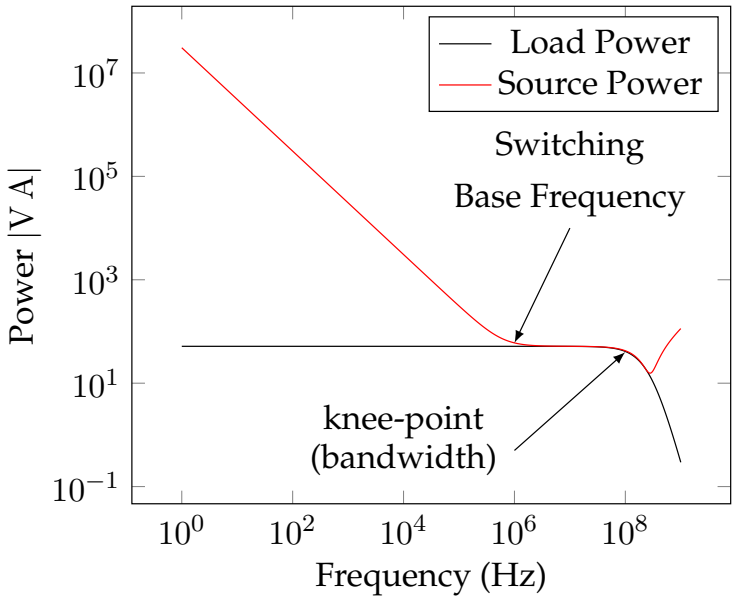
TABLE 3.1: Requirements of transformer design

Parameter	Value
Frequency	1MHz
Power	50W
Turns Ratio	4:1
V_{in}	100V
V_{out}	25V
B_{peak}	0.2T

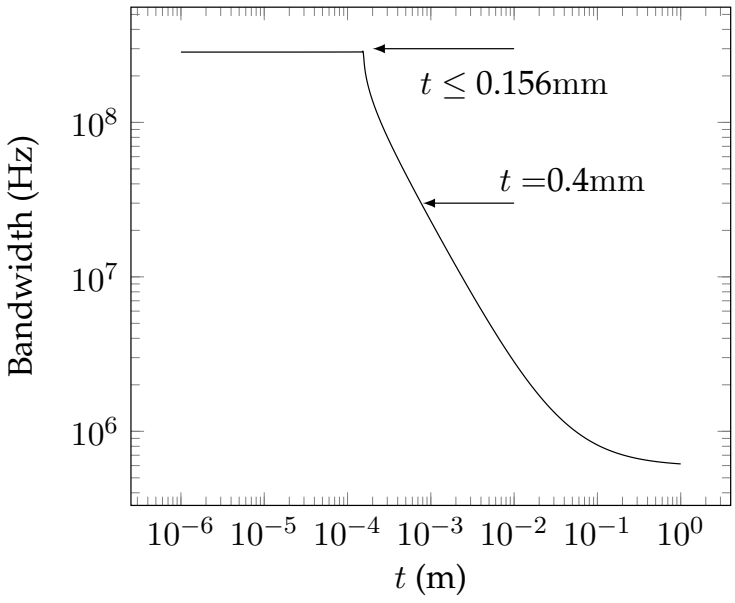
The specifications have led to the optimised transformer design with parameters specified in table 3.2 (the blanks represent values that are unchanged). The power transfer characteristics in the frequency domain for the optimised transformer are presented in fig. 3.7a. The effect of dielectric thickness on the frequency range is presented in fig. 3.7b for the designed winding inductance value.

TABLE 3.2: Transformer Design Parameters. $\mu_r = 1000$, $\epsilon_r = 5$

Parameter	Value (optimised)	Value (non-optimised)
L_{knee}	2.71µH	–
$L_{designed}(L_1)$	51.5µH	44.4µH
R_L	12Ω	–
t	0.156mm	0.4mm
$Bandwidth$	286MHz	59MHz
b_w	1mm	–
l_w	2.23mm	–
l_c	14mm	–
l_m	12.2mm	14.14mm
L_k	214nH	549nH
C_1	2pF	0.75pF
C_k	10.3pF	4pF
C_2	0	–
Power Density	177MW m^{-3}	122MW m^{-3}



(a) Plot showing the optimised power transfer characteristics of source and load power in the frequency domain. The transformer is using an optimised dielectric thickness of 0.156mm.



(b) Plot showing the influence of dielectric thickness on the frequency knee-point.

FIGURE 3.7: Plots showing characteristics of designed transformer.

3.6 Discussion

3.6.1 Discussion on Design Example

It can be seen in the design example from fig. 3.7b & table 3.2 that the bandwidth is optimised when an optimum dielectric thickness of $0.156\mathrm{mm}$ is used. A 384% improvement in bandwidth is found compared to when a standard thickness of $0.4\mathrm{mm}$ is used; a power density improvement of 45% is also found.

Inspection of the frequency characteristics of the structure shown in fig. 3.7a shows that operation of the transformer far below the frequency of 1 MHz requires a significant amount of power to deliver the same load power due to poor power-factor. The practical operational bandwidth of the transformer thus starts at 1MHz and ends at 285MHz. The lower end of the bandwidth is loosely based on the choice of switching frequency chosen in the initial design process. The improvement of bandwidth would allow for more harmonics of the switching waveform to be passed through the transformer undistorted.

The improvement in power density appears to be relatively high, given that it is 45% and that this significant improvement is arising from merely optimising the dielectric thickness. However, it is known that the dielectric thickness parameter also affects the core volume, together with the winding volume. Given that the dielectric thickness has been changed (optimised) by 61% and that the winding volume makes up about 26.41% of the total volume, in perspective the percentage change in total volume of the transformer appears to be reasonable. However, it may be noted that the power density may not always be improved, as there may be cases where the optimum dielectric thickness is larger than the original choice of dielectric thickness. The track width b_w may then be adjusted as required such that the optimum dielectric thickness is lower, as indicated on the design flow chart in fig. 3.6.

The optimised dielectric thickness presents the optimum values for the capacitive and inductive parasitics present in the transformer. Furthermore, the power density of the transformer can also be improved as a benefit of optimising the dielectric thickness. It is also found from fig. 3.7b that using a dielectric thickness less than t_{opt} will have negligible impact on the bandwidth. Therefore t_{opt} can be said to be the maximum allowable dielectric thickness t_{max}. This implies that the planar transformer's windings can be constructed as dense as possible with no effect on the bandwidth of the transformer.

A 60W planar transformer was designed in [24], with a dielectric thickness of $0.4\mathrm{mm}$. It may be noted that a direct comparison with the transformer design in [24] could not be made, as the exact details of the transformer were not readily available. Thus, an independent design was used in the design example. It has been shown in [24] that a high power density transformer can be designed with a band-limited frequency range of 10MHz. In light of the bandwidth and power density improvement shown in the design example, it is reasonable to assume that the transformer designed in [24] could take advantage of the optimisation process, given that the authors have used a dielectric thickness of $0.4\mathrm{mm}$ for their transformer with similar design specifications. However, the authors have shown that due to core losses, their planar transformer was band-limited to around 10MHz due to non-linear core losses. Due to this, choosing a higher or lower dielectric thickness would not have made significant difference to the overall bandwidth of the transformer. In any case, it is still reasonable to expect an increase in power density of the same transformer, if an optimum dielectric thickness is used, even if there is no effective improvement in practical bandwidth.

This work is thus useful for high frequency operation of transformers, where the application is sensitive to the bandwidth, and where the bandwidth of the transformer is controlled by the dielectric thickness and not limited by the core material.

3.6.2 Exclusion of Intra-layer Capacitance

It should be noted that in the design example presented in section 3.5, the total self capacitance of the secondary side is considered to be zero. Of course this is not exactly true, as there will always be a small amount of intra-layer capacitance between the terminals of the single layer winding, as shown in fig. 2.18b in section 2.2.3 of chapter two; it may be noted that the self capacitance is effectively a sum of the total intra-layer capacitance and the inter-layer capacitance as discussed in section 2.2.4 in chapter two. However, upon inspecting the bandwidth and thickness expressions shown in eq. (B.4c), eq. (3.8b) and eq. (3.8a), the terms shown in eq. (3.13) are found. From this expression, it is easy to see that the coupling capacitance C_k will always dominate, since it as an addition operation, and not a multiplication operation. This is supported by the fact that the intra-layer capacitance will always be much smaller than the inter-layer or coupling capacitance, as shown in chapter two.

$$(4C_2 + C_k) \tag{3.13}$$

3.6.3 Considerations for Spiral Winding Structures

When a spiral structure is considered, expressions for the inter-layer capacitance, coupling capacitances and leakage inductance given in eq. (3.4a), eq. (3.4b) & eq. (3.4c) respectively need to be slightly modified to accommodate for the change in geometrical structure. Please note that all references to equations, figures and tables that have a capital letter can be found in the relevant appendix.

The width of the tracks is no longer equal to the width of the core window b_w, but is given in eq. (A.3a), taking into account the number of turns n present on each winding layer. It is found to be more convenient to express the dielectric spacing distance between turns d as a fraction k_p of the track-width w. The track width w can thus be re-written as eq. (3.14). The turn length for windings in each layer is

given in eq. (A.3e); l_{t_s} is the total length of the spiral track, whereas l_t is the effective length of a single turn track as illustrated in fig. 2.7. It is important to use the l_t for leakage inductance as the magnetic flux effectively sees the spiral as a single-turn layer, with the magnetic field intensity multiplied by the square of the number of turns per layer n.

$$w = \frac{b_w}{n + k_p(n-1)} \tag{3.14}$$

With these geometrical changes taken into account, the inter-layer capacitance, coupling capacitance and leakage inductance can be expressed as eq. (3.15a), eq. (3.15b) & eq. (3.15c). The effective width and length for the leakage inductance is equal to b_w and l_t respectively.

$$C_{inter} = \epsilon_0 \epsilon_r \frac{l_{t_s} w}{t} \left(\frac{N_L - 1}{N_L^2} \right) = \frac{1}{t}(C_{i_c}) \tag{3.15a}$$

$$C_k = \epsilon_0 \epsilon_r \frac{l_{t_s} w}{t} = \frac{1}{t}(C_{k_c}) \tag{3.15b}$$

$$L_k = \frac{\mu_0 \, l_t \, n^2}{b_w} \left[t \sum_{a=1}^{N_{LP}-1} a^2 + t \, N_{LP}^2 + t \left(\frac{N_{LP}}{N_{LS}} \right)^2 \left(\sum_{b=1}^{N_{LS}-1} b^2 \right) \right] = t(L_{k_c}) \tag{3.15c}$$

The dimensions of the dielectric layer for D_w, D_l, b_w needs to be chosen (refer to fig. A.1), along with d (or k_p) as this allows for the calculation of the spiral length l_{t_s}; the length l_t also needs to be calculated for the leakage inductance and is given as eq. (A.2).

3.6.4 Bidirectional Operation

The results derived in section 3.3 holds valid for step-up and step-down operation. Bidirectional operation implies that power flows in both directions (primary->secondary & secondary->primary) of the transformer. It is true that an ideal transformer should transfer power equally in both directions. However, once the transformer is optimised for operation in one direction, optimized parameters cannot be guaranteed to hold true for operating the reverse direction, using the same design

parameters, due to changing parasitics and magnetising inductance. Thus, bidirectional operation would require the user to find optimum parameters for both ports; this would mean that bandwidths of both directions need to be found, and an optimum dielectric thickness that is common to both directions of use must be found (this usually means the lowest common optimum dielectric thickness). Of course, this is not an issue for unidirectional operation, where power only flows from the primary to secondary side.

3.6.5 Reasoning for Assumptions

Previously it was discussed in section 3.3 that the following assumptions were made in order to derive analytical expressions:

- All layers of the primary and secondary windings are identical
- Every layer of both windings have a single turn
- Intra-layer capacitance is ignored as its considered negligible.

Furthermore, the following assumptions are also made:

- The dielectric thickness of all layers are the same
- The dielectric permittivity of all layers are the same.

It may be noted that such assumptions may seem to potentially limit the scope of the work. However these assumptions are supported by practicality. The following reasons are presented:

- The dielectric thickness and permittivity of all layers is usually kept the same. This is to allow for simpler construction/manufacturing of the structures.
- All layers may have the same number of turns as this allows for generalisation of the analytical calculations for parasitic inductance and capacitance due to

well defined geometry. Including different number of turns will complicate the leakage inductance and parasitic capacitance expressions and will lead to a non-analytical model of the parasitics.

- A single turn per layer is used for demonstration of concept. The results are equally valid for multiple turns as this would merely change the effective surface area of the inter-layer capacitance and coupling capacitance. As for the leakage inductance, the leakage H-field magnitudes of each layer will be multiplied by the product of n, which is the number of turns per layer as illustrated in fig. 2.8. Such changes are accounted for and described in section 3.6.3. Furthermore, the total self-capacitance of the winding would be only slightly higher due to the presence of intra-layer capacitance.

- The intra-layer capacitance is ignored in this analysis as it has been shown in the previous chapter that its contribution is thought to be insignificant compared to the coupling capacitance C_k and the inter-layer capacitances.

Planar transformers can be designed with many different winding configurations, resulting in complex electric and magnetic field distributions, which can be difficult to analyse analytically. This is because complex winding configurations leads to complex geometry. However, it can be argued that the parasitic capacitance and leakage inductance of any winding configuration can be reduced to the form shown in section 3.3, with the proportionality to dielectric thickness maintained. The effective capacitance and leakage inductance would be scaled by a scaling factor which takes into account the complex geometry; this scaling factor is accounted for within the parasitic constant described in section 3.3. Given this, one can argue that the results presented in this chapter would be valid for any winding configuration, provided that the designer is able to analytically capture the details such as the effective areas and lengths of the relevant geometry.

3.7 Summary

This chapter has shown that the dielectric thickness has a definite impact on the bandwidth of the transformer. It has been shown that there are values of dielectric thickness t_{opt} that results in the highest possible bandwidth f_{max}. These optimum thickness values presents the optimum values of the inductive and capacitive parasitics that results in the optimum bandwidth, given a winding configuration. However, it has also been shown that in some cases, such as those presented in fig. 3.5, that when the primary winding inductance L_1 is much larger than L_{min}, t_{opt} is just the maximum dielectric thickness, t_{max} that can be used. In this case, choosing a dielectric thickness less than t_{max} has negligible effect on bandwidth. The dielectric thickness must thus be chosen such that it is less than or equal to t_{max}, and at the same time be able to withstand the voltage difference across it, depending on the application. It may be noted that should t_{opt} (or t_{max}) be smaller than the minimum dielectric thickness needed for breakdown, a better dielectric material may be chosen to prevent such a breakdown.

The minimum feasible primary winding inductance L_{min} for a given transformer configuration, to be used for optimisation has been derived in this chapter. Using a winding inductance that is equal to or greater than this value ensures that the optimum dielectric thickness derived results in a leakage inductance that is smaller than the winding inductance. This helps to ensure that only practically possible design solutions are derived. Furthermore, it has been shown that when the winding inductance is much greater than L_{min} (at least 10 times), the closed form expressions of t'_{opt} and f'_{max} can be used since there is convergence.

It has been discussed that in certain practical cases, optimisation of the dielectric thickness cannot be taken advantage of, due to the bandwidth limitations of the core material, as a result of non-linear losses. This work is therefore more useful for high frequency applications that take into account transformer bandwidth, wherein

the bandwidth is entirely dependant on the capacitive and inductive parasitics and not the core material.

Concerning the transformer volume, the winding volume can be significantly reduced when the optimum dielectric thickness is chosen; by extension the core volume is also reduced when the core is designed with both flux saturation and dielectric thickness optimisation in mind. However, the improvement in power density is not always guaranteed because the dielectric thickness is primarily optimised for bandwidth and not for reduction of volume, which could result in a higher-than-expected optimum thickness. This being said, it is possible to derive a solution where the optimum thickness is lower by adjusting the track width of the conductors appropriately in accordance with fig. 3.6.

Although the bandwidth was derived based on the circuit model chosen in chapter two, it may be noted that other circuit models would give approximately the same bandwidth and optimum dielectric thickness values through similar expressions. This is expected to be true as long as the circuit model is able to capture the knee-point frequency accurately. It can therefore be argued that the bandwidth and optimum thickness expressions derived in this chapter are generalised to planar transformers, given the constraints and assumptions mentioned in this dissertation.

Finally, this chapter has shown that the dielectric thickness of a planar transformer can be optimised such as to present the best bandwidth possible for a given winding configuration. Analytical expressions have been derived for the optimum dielectric thickness and the bandwidth, such as to lessen the burden of iterative simulations of planar transformers for bandwidth optimisation.

Chapter 4

Conclusion

With the conclusion of this research, planar transformers can now be optimized for frequency bandwidth by choosing of an optimum dielectric thickness; the power density can also be optimised as a result. The following contributions have been made:

- A suitable lumped electrical circuit model has been proposed, taking into account the constraints and assumptions made in chapter 1. The currents and voltages within the circuit have been shown to match with that of simulation results in FEKO.
- The theoretical bandwidth of the transformer has been defined as the frequency beyond which the transformer no longer exhibits ideal transformer behaviour; that is to say that currents and voltages of the secondary side no longer follow the transformer turns ratio.
- The effect of capacitive and inductive parasitics on the theoretical bandwidth have been analysed by analytically defining the bandwidth as a function of dielectric thickness.
- A method of designing transformers with optimum bandwidth and optimum dielectric thickness has been found and described.

The research objectives defined in chapter one have thus been accomplished, and the research question has been answered. The results are strongly believed to be valid within the framework of assumptions and constraints considered.

It was stated in chapter one that there is a need to choose the optimum dielectric thickness for planar transformers. It was decided to analytically solve for the optimum dielectric thickness value, as such a solution would allow for convenient designing of planar transformers, which would otherwise require either trial and error construction of lab prototypes or time-consuming iterative electromagnetic simulations.

Due to the importance of finding an analytical closed-form solution, it was decided in chapter two to work with a suitable model of a planar transformer. A lumped electrical model of a planar transformer was thus chosen as each component of the circuit can be analytically derived, and the circuit itself can be inherently analytically analysed by deriving mesh equations. A proposed circuit model was presented and was shown to be closely matching a simulated planar transformer in FEKO simulation software.

Using the planar transformer model proposed in chapter two, the theoretical bandwidth of the transformer was described in chapter three analytically, as functions of the capacitive and inductive parasitics, which are both functions of dielectric thickness. The optimum dielectric thickness was then analytically derived by analysing its influence on the frequency bandwidth of the transformer. It has also been found that for a given winding configuration, the winding inductance must be carefully chosen such that there exists an optimum thickness and bandwidth which is physically realisable. This physically unrealisable region exists because the analytical results have been derived from the circuit model, wherein the leakage inductance can be higher than the primary winding inductance; such a structure cannot be physically realised for obvious reasons.

In a design example in chapter three, it has been shown that by optimising the dielectric thickness of a 50W 4:1 planar transformer, the bandwidth can be improved by 384%, along with a power density improvement of 45%. It is thought that optimisation of dielectric thickness results in a bandwidth optimisation that cannot be taken advantage of in cases where the overall bandwidth is determined by the core's bandwidth, due to non-linear losses. However, applications that require a high bandwidth, that are not band-limited by the core, can benefit from the optimisation process. This research is thus useful where bandwidth is not restricted by the core. Furthermore, it may be noted that in cases where the optimum dielectric thickness would result in dielectric breakdown, a better dielectric material may be used to prevent such breakdown, if the goal is to design for optimum bandwidth; there always exists a possibility of developing/using better materials to resist dielectric breakdown in the future.

The results presented in this research are theoretical due to many idealistic constraints and assumptions made. Thus it is thought that the bandwidth of a real planar transformer with all the non-ideal characteristics would at best approach the theoretical bandwidth.

Finally, the research presented has shown that the dielectric thickness of a planar transformer with non-interleaved windings can be optimised such that the theoretical bandwidth of the transformer is optimised.

4.1 Recommendations For Future Work

It would be interesting to see whether the results presented in this research would compare when using a more practical transformer model that incorporates non-ideal characteristics such as core, winding and dielectric losses, and frequency dependant material permeability and permittivity.

A typical planar transformer has power transfer characteristics in the frequency range as shown fig. 3.7a (shown again in fig. 4.1 for convenience). It can be seen that the power-factor is low at low frequencies. It can be argued that this effect may not be a problem if the transformer is designed with the base frequency of the switching in mind (as described in chapter three). However, the base frequency could be much lower or higher in cases where random switching is used to dither the EMI. In this case the base frequency is not well defined, so something must be done to remove, or at least reduce this effect.

This apparent power can be reduced by placing a capacitor in parallel with the source. The placement of this capacitor will not affect the bandwidth of the transformer as the load power is only dependant on the capacitor at the load C_2 and the inter-winding coupling capacitance C_k. If possible, this capacitance can be made to arise out of the winding itself by adjusting the thickness of the dielectric in the primary winding. Future work can account for this frequency-based power factor and design a suitable capacitor to counteract this effect.

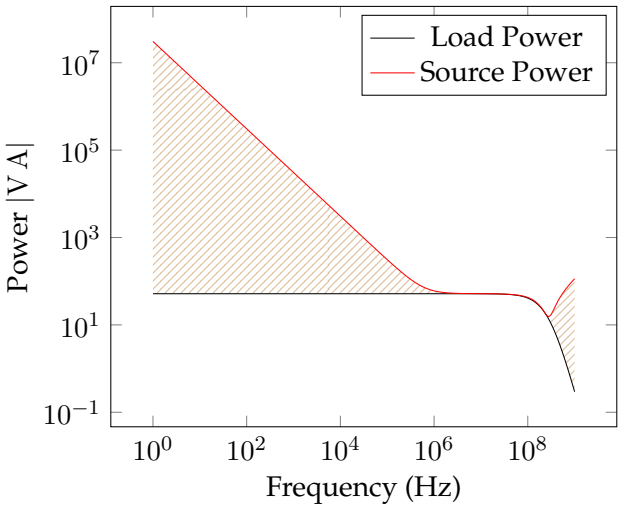


FIGURE 4.1: Plot showing the power transfer characteristics of source and load power in the frequency domain. Shaded region indicates area to be minimised to improve power-factor within the operating frequency range.

Furthermore, the dielectric thickness optimisation can be extended to include transformers with an interleaved winding arrangement. Since the intra-layer capacitance is also dependant on the thickness of the dielectric, future work can take into account the intra-layer capacitance together with the inter-layer capacitance to find the optimum dielectric thickness.

This research has considered transformers that are operating in continuous conduction mode. Further research is recommended to verify whether the results presented in this research are applicable to flyback coupled inductors.

4.2 Possible Future Implications

Since the work in this research has considered lossless windings, it may find useful application where the transformers are superconducting [45–48]. Although superconducting transformers exist in literature, none have taken a planar form factor. The core can be eliminated as the flux can be coupled and bounded using 'flux-lensing' by a superconducting tube, by taking advantage of the Meisner effect. Such an 'air-core' could help overcome the problem that ferrite cores have with bandwidth restriction due to non-linear losses. The air core must then be designed such as to present at least the minimum winding inductance L_{min} for optimum bandwidth and dielectric thickness, as discussed in chapter three. The design technique and assumptions presented in this research would thus directly relate to the lossless nature of such a superconducting transformer, due to the lossless planar transformer model from which the design techniques have been derived. The extent to which superconducting planar transformers can be used and their advantages, can be evaluated in future research.

Appendix A

Analytic Geometry Expressions for Dielectric Layer and Spirals

The geometry of a general planar dielectric layer is shown in fig. A.1. For a single-turn layer, the effective length l_t of the conductor is given by eq. (A.2). The lengths of D_l and D_w are given as shown in eq. (A.1a) & eq. (A.1b).

$$D_l = l_c + 2b_w \tag{A.1a}$$

$$D_w = l_w + 2b_w \tag{A.1b}$$

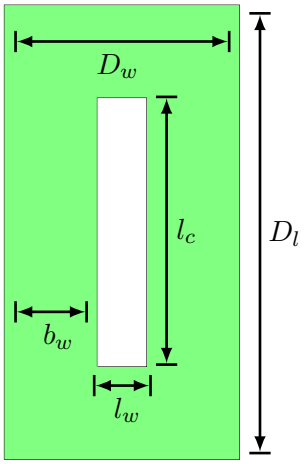


FIGURE A.1: Geometry of the dielectric layer.

$$l_t = 2(D_l + D_w) - 4b_w \tag{A.2}$$

The calculations of the leakage inductance, intra-winding capacitance and coupling capacitance are based on the geometry of the spiral windings. It is therefore important to have analytical approximations for various geometrical aspects of the spiral structure.

First, the track width is calculated for an arbitrary number of turns ($n >= 2$) in eq. (A.3a). The length of the first turn given in eq. (A.3b). Lengths of subsequent turns are given in eq. (A.3d) with each turn reduced by a constant amount u meters given in eq. (A.3c). The total length can then be found as the sum of all individual lengths as given in eq. (A.3e).

These approximations are compared to measured lengths of spiral conductors in table A.1. It may be noted that although the essence of the work in this document is theoretical, it was necessary to verify the accuracy of the analytical length expressions by producing spiral prototypes in the lab and measuring their spiral lengths. The author acknowledges that there might be uncertainties in the measurements themselves due to the accuracy of the measuring instrument (ruler) used. However, this accuracy is thought to be sufficient for comparative purposes.

$$w = \frac{(b_w - d(n-1))}{n} \tag{A.3a}$$

$$l(1) = 2(D_w + D_l) - 2(w + d) \tag{A.3b}$$

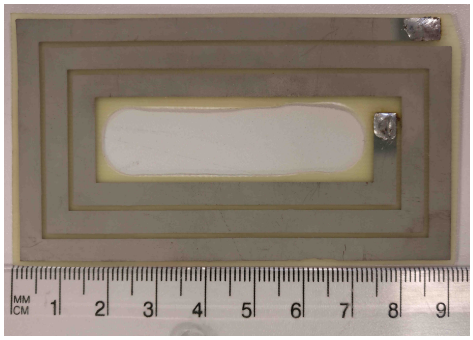
$$u = 10(w + d) \tag{A.3c}$$

$$l(k) = \sum_{k=2}^{n} l_{k-1} - u \tag{A.3d}$$

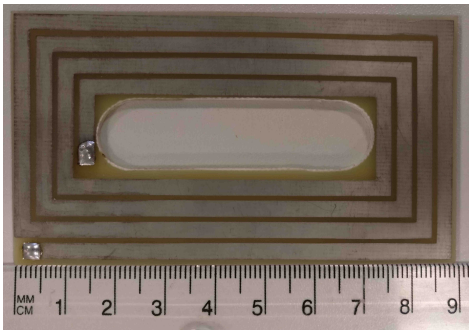
$$l_{t_s} = \sum_{k=1}^{n} l_k \tag{A.3e}$$

turns	d (mm)	D_w (mm)	D_l (mm)	b_w (mm)	Calculated l_{t_s} (mm)	Measured l_{t_s} (mm)	Error
3	1	50	86	16	680	640	5.9%
4	1	48	88	16	867	835	4.2%
7	0.5	48	88	16	1440	1436	0.28%
10	0.5	48	88	16	2010	2035	1.2%

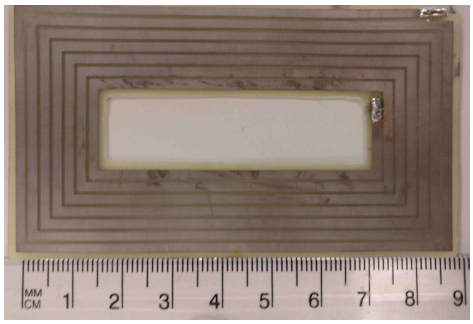
TABLE A.1: Comparison of measured and calculated spiral lengths. The calculated lengths of the spiral structures are compared to measured lengths of structures shown in fig. A.2.



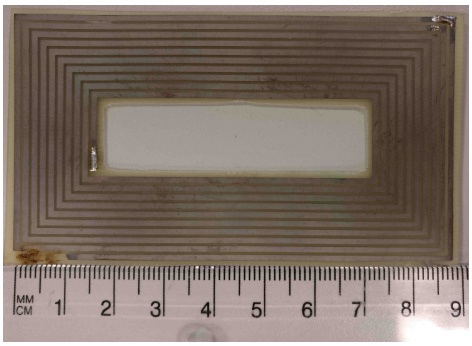
(a) 2-turn spiral, $d = 1\text{mm}$



(b) 3-turn spiral, $d = 1\text{mm}$



(c) 7-turn spiral, $d = 0.5\text{mm}$



(d) 10-turn spiral, $d = 0.5\text{mm}$

FIGURE A.2: Spiral layers with various turns and dielectric spacings constructed to validate length approximations.

Appendix B

Power & Auxiliary Expressions

The numerator and denominator terms of the original load power expression are given in eq. (B.1a) & eq. (B.1b) respectively; the turns ratios are chosen arbitrarily to show agreement for both step-up/down operation. The frequency knee-points of the load power are calculated by analytically finding the roots of ω in eq. (B.1b). The load power expression is given in eq. (B.1c).

$$\left|P_{L_{(num)}}(\omega)\right| = \left|R_L C_k^2 (L_1 L_2 - M^2)\omega^4 - 8R_L C_k M (L_1 L_2 - M^2)\omega^2 + 16M^2 R_L\right| \tag{B.1a}$$

$$\begin{aligned}\left|P_{L_{(denom)}}(\omega)\right| = \Big|&(C_2 C_k L_k R_L (L_1 L_2 - M^2))\omega^4 + jC_k L_k (L_1 L_2 - M^2)\omega^3 \\ &- (C_k L_k (L_1 - 2M) - (4C_2 + C_k)M^2 + (4C_2 + C_k))(L_1 + L_k)\omega^2 \\ &+ 4j(L_1 L_2 + L_2 L_k - M^2)\omega + 4R_L (L_1 + L_k))^2\Big|\end{aligned} \tag{B.1b}$$

$$|P_L(\omega)| = \left|\frac{P_{L_{num}}(\omega)}{P_{L_{denom}}(\omega)}\right| \tag{B.1c}$$

The approximated load power function is found by truncating the higher order terms that eventually tend to zero (3^{rd} & 4^{th} order terms in this case) in the denominator. The approximated load function is then given as eq. (B.2).

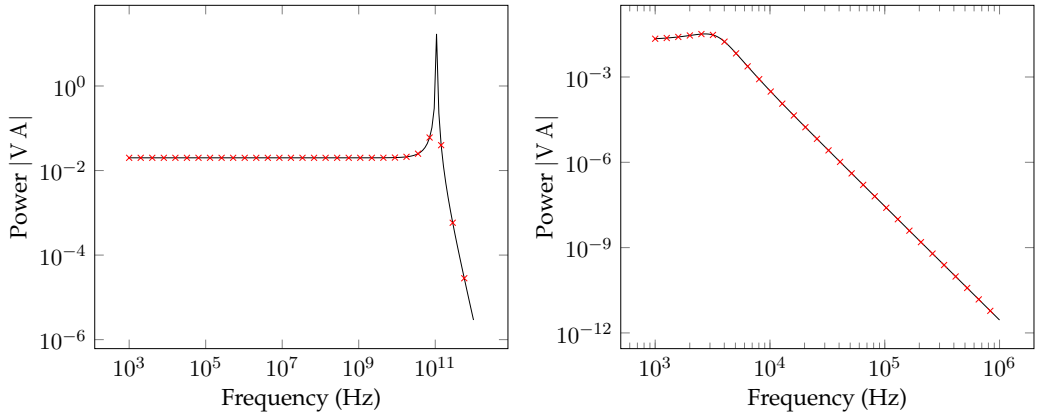
$$\left|P'_{L_{denom}}(\omega)\right| = \Big| -\Big((C_k L_k(L_1 - 2M) - (4C_2 + C_k)M^2 + (4C_2 + C_k))(L_1 + L_k)\omega^2 + 4j(L_1L_2 + L_2L_k - M^2)\omega + 4R_L(L_1 + L_k)\Big)^2\Big| \tag{B.2}$$

The approximated load power expression is plotted along with the original load power expression in fig. B.1. Inspection of these plots show that the approximation matches very well with the original expression.

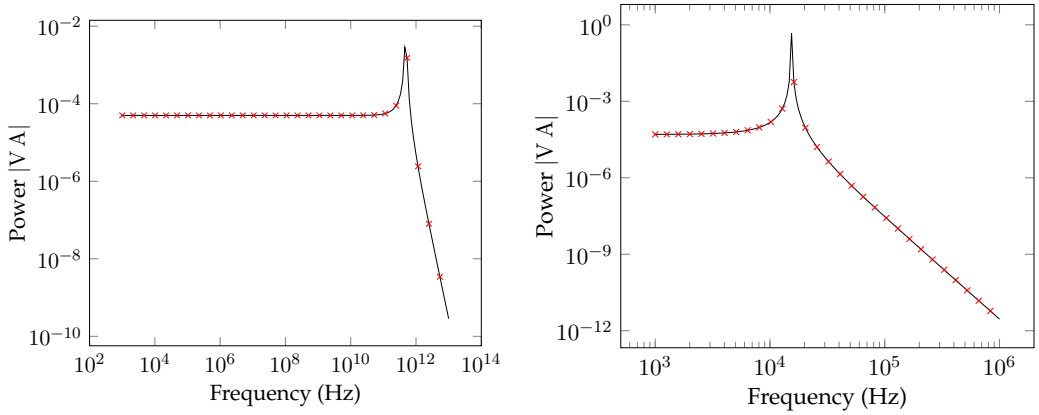
It may be noted that the load power expression is a complex expression. This is not expected as the power being dissipated is considered purely real as it is being dissipated by a resistor. However, insight into the mesh equations derived reveals that the load current expression (from which the load power expression is derived) has a phase angle that is caused due to the current being referred to the primary side of the transformer. This phase angle disappears when the current is referred to the secondary side of the transformer. The phase angle can thus be safely ignored for all calculations, and only the magnitude of the load current expression should be considered, assuming that all calculations are being referred to secondary side. Any subsequent expressions derived from the load current expression, such as the bandwidth, must thus have an absolute function applied to it to obtain the magnitude. Furthermore, this makes sense because it is meaningless to obtain a phase angle for the unit of frequency.

The poles of the load power expression can be found by considering the expression under the square operator in eq. (B.2). This expression is given in eq. (B.3).

$$0 = (C_k L_k (L_1 - 2M) - (4C_2 + C_k)M^2 + (4C_2 + C_k))(L_1 + L_k)\omega^2$$
$$+ 4j(L_1 L_2 + L_2 L_k - M^2)\omega + 4R_L(L_1 + L_k) \tag{B.3}$$



(a) $L_1 = L_k = 1\text{pH}$, $C_1 = C_2 = C_k = 1\text{pF}$, $Turns\ Ratio = 1:2$ (b) $L_1 = L_k = \text{mH}$, $C_1 = C_2 = C_k = 1\mu\text{F}$, $Turns\ Ratio = 1:2$



(c) $L_1 = L_k = 1\text{pH}$, $C_1 = C_2 = C_k = 1\text{pF}$, $Turns\ Ratio = 10:1$ (d) $L_1 = L_k = 1\text{mH}$, $C_1 = C_2 = C_k = 1\mu\text{F}$, $Turns\ Ratio = 10:1$

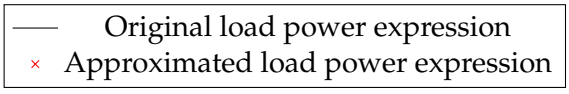


FIGURE B.1: Comparison of original load power expression and approximated load power expression.

The knee-point frequency or bandwidth can be calculated by finding the frequency roots of the load power expression which can be solved for from eq. (B.3). The coefficients of this expression has been re-written as a function of thickness t. This allows the frequency bandwidth to be analysed as a function of dielectric thickness. The coefficients of the expression of interest, eq. (B.4a), are given in eq. (B.4b). The frequency roots themselves are given in eq. (B.4c).

$$0 = a\omega^2 + b\omega + c \tag{B.4a}$$

$$\begin{aligned} a &= -(C_{k_c} L_{k_c} t(L_1 - 2M) - (4C_{2_c} + C_{k_c})(M^2 - L_2(L_{k_c} t + L_1)))R_L \\ b &= 4jt((L_{k_c} t + L_1)L_2 - M^2) \\ c &= 4t(L_{k_c} t + L_1)R_L \end{aligned} \tag{B.4b}$$

$$Frequency\ roots\ (rad/s) = \left| \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \right| \tag{B.4c}$$

The root that is of interest is the positive version of eq. (B.4c). The maximum frequency bandwidth in eq. (B.4c) is found by considering only the terms under the square root operator as given in eq. (B.6a), which can be simplified by gathering all coefficients of t as in eq. (B.6c); the coefficients of t in eq. (B.6c) are given in eq. (B.6b). A few important substitutions are made in eq. (B.5), where a_r is the turns ratio of the transformer.

$$L_2 = a_r^2 L_1 \tag{B.5a}$$

$$\begin{aligned} M &= \sqrt{L_1 L_2} \\ &= a_r L_1 \end{aligned} \tag{B.5b}$$

$$0 = b^2 - 4ac \tag{B.6a}$$

$$
\begin{aligned}
a_x &= -16L_1^2 L_{k_c}^2 a_r^4 \\
b_x &= 16(L_{k_c}^2(a_r^2(4C_{2_c} + C_{k_c}) - C_{k_c}(2a_r - 1)))L_1 R_L^2 \\
c_x &= 16(L_{k_c}(a_r^2(4C_{2_c} + C_{k_c}) - C_{k_c}(2a_r - 1)))L_1^2 R_L^2
\end{aligned} \tag{B.6b}
$$

$$0 = a_x t^2 + b_x t + c_x \tag{B.6c}$$

$$t_{opt} = \left| \frac{-b_x - \sqrt{b_x^2 - 4a_x c_x}}{2a_x} \right| \tag{B.6d}$$

The minimum inductance L_{min} is then found by considering the terms under the square-root operator in eq. (B.6d) as given in eq. (B.7a). Simplifying this expression and collecting the coefficients of L_1 gives a quadratic expression. This quadratic expression can be solved for L_1 to give eq. (B.7b).

$$0 = b_x^2 - 4a_x c_x \tag{B.7a}$$

$$L_{knee} = \left| \frac{R_L \sqrt{L_{k_c}(-4C_{2_c} a_r^2 - C_{k_c}(a_r^2 - 2a_r + 1))}}{2a_r^2} \right| \tag{B.7b}$$

Appendix C

Simulation Software and Setup

C.1 FEKO Simulation

FEKO is a simulation tool that can be used to simulate 3D electrical models in the frequency domain. The software currently only runs on Windows and Linux-based operating systems, and requires a license to run.

The core model that was constructed has the exact dimensions as the Ferroxcube PLT/E64 combination [49]. All simulations in FEKO used the same dielectric model and core model dimensions. The dimensions of the dielectric layer used are visualised in fig. C.2; the values of the dimensions are tabulated in table C.1. The default dielectric thickness of a layer is 0.4mm except when specified otherwise. The dielectric material permittivity and core material permeability is 5 and 1000 respectively unless specified otherwise. The range of permittivity and permeability values are arbitrarily chosen to validate FEKO simulation's agreement with analytical expressions at relatively 'extreme' values.

In order to simulate the transformers properly, the grounds of the secondary winding were connected to the grounds of the primary winding to a common ground plane as shown in fig. C.1. Simulation of the transformer requires a source port and a load port which are both defined as 'edge-ports' in FEKO. For leakage inductance measurements, the load port is shorted in-effect by defining the load as zero ohms.

It may be noted that illustrations of multiple simulation models are not presented. This is because it is sufficient to show the general structure of the simulation model, with variations of the geometry noted wherever necessary.

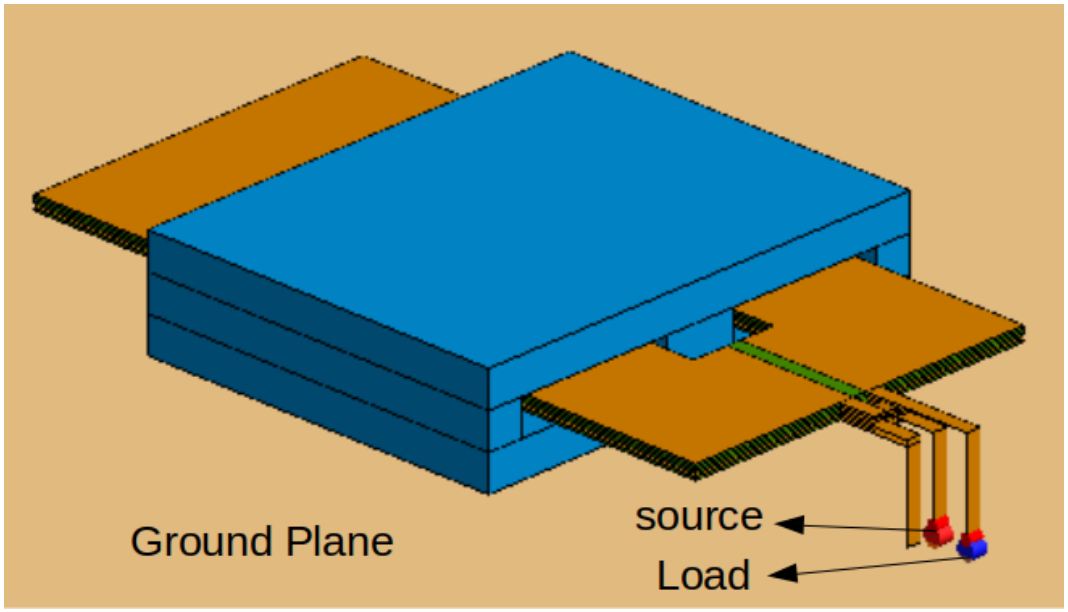


FIGURE C.1: Simulation model of a 2:4 transformer.

	Values (mm)
D_w	49.8
D_l	98.6
b_w	18.8
l_w	10.2
l_c	50.8

TABLE C.1: Dimensions of Dielectric Layer.

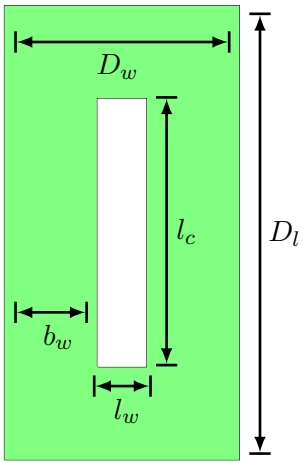


FIGURE C.2: Illustration of dimensions of the dielectric layer.

C.1.1 Comment on Meshing Requirements

In general, the simulation results agree with mathematical models derived in chapter two. Many minor discrepancies are attributed to insufficient meshing throughout the chapter. However, since the simulation and mathematical circuit models are in agreement, it can be argued that increasing the mesh density would allow the behaviour of both models to approach convergence; although it may be noted that the behaviour of a lumped model can never truly match that of a distributed electromagnetic model at high frequencies due to their fundamental differences. In this case, increasing the mesh density would require high computational resources and would ultimately result in diminishing returns from the simulation. The meshing used in the simulations in this dissertation are therefore considered to be sufficient for the purposes of this research; the mesh size and density being automatically chosen by FEKO.

C.1.2 Simulation Procedure

The following general rules must be followed to simulate structures properly in FEKO:

- The frequency range must be defined.
- The source port must be defined. A 'wire-port' or an 'edge-port' must be used.
- A source must be defined. Generally this is a voltage-source.
- A load port may be defined if a real or complex load is to be connected in series or parallel.
- Volume equivalence principle may be used to solve for structures where large dielectrics are defined. Surface equivalent principle may be used to solve for structures where thin dielectrics are defined.

- All structures constructed in FEKO must be 'unionised' if they are to be electrically connected.
- Electric or magnetic fields may be requested. The cross-section must be defined to be able to plot the field magnitude as a function of a physical dimension.
- The structures must then be meshed before the simulation is run. The mesh size is usually automatically chosen. However finer meshing is recommended near ports and dielectric layers, or where small geometrical details are present.

C.2 FEMM Simulation

FEMM is a free cross-platform simulation tool that can be used to simulate the electric and magnetic fields of two-dimensional structures. This software is used to measure the per-unit-length-capacitance between two adjacent strips of conductors. The electric field flux lines and equipotential lines can be requested. The software also has a convenient capacitance calculation tool, which can be used to directly calculate the capacitance.

The following procedure must be followed to simulate structures correctly in FEMM for an electrostatics problem:

- An electrostatics problem should be chosen on start-up
- The problem must be specified as planar and the depth must be specified as 1 meter.
- The vertices of the structure must be defined using nodes. The vertices can then be connected using segments.
- Specify voltages on segments.

- Materials such as air and FR4 must be defined. Block labels must then be places inside blocks. The property of the block label must then be set to the appropriate materials.
- A non-mesh block label must be defined to avoid meshing the entire region.
- The structure must then be meshed.

An example model to simulate a two dimensional cross section of a structure with two conductors is shown in fig. C.3.

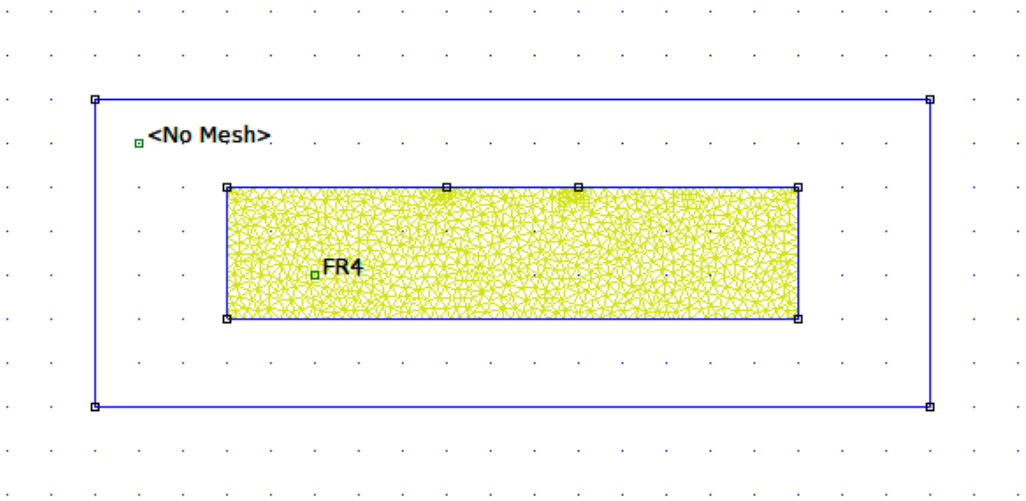


FIGURE C.3: Cross section view of a FEMM model to simulate fringing electric field between two adjacent strips of conductors on a dielectric.

C.3 NgSpice Simulation

NgSpice is a free cross-platform circuit simulation tool that can be used to simulate complex circuits.

In order to simulate an example transformer circuit, a '.circ' file must first be created. The first line of the file must be the name of the circuit model, after which components can be defined on each line followed by the nodes that they are connected to and then the component value.

In order to run and extract the requested currents and voltages, a '.control' section must then be created within the file. In this section the run command must be implemented. The output data must then be defined as ASCII. A 'wrdata' command must also be implemented in order to get the program to output the currents and voltages.

The type of analysis can then be defined. A frequency analysis is required in this case, so the '.ac' command is used. Finally '.end' command is used to define the end of the file. As an example, code used to simulate a transformer circuit is shown in listing C.1.

LISTING C.1: NgSpice code used to simulate a transformer circuit

```
Transformer Model
V1 1 0 AC 1
C1 1 0 50p
Lk 1 2 100n
Rs 2 3 1n
L1 3 0 10u
Ck 3 4 50p
L2 4 0 40u
C3 4 0 50p
R 4 0 50
k L1 L2 1
.control
run
set filetype=ascii
wrdata power_output_1 abs((v(4)^2)/50) abs(i(V1)*v(1))
.endc
.ac dec 200 1kHz 10e8
.end
```

References

[1] J. D. v. Wyk and F. C. Lee, "On a Future for Power Electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, Jun. 2013.

[2] Z. Ouyang and M. A. E. Andersen, "Overview of Planar Magnetic Technology –Fundamental Properties," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014.

[3] J. Qin, Z. Yu, K. Sun, P. Wei, and Z. Lan, "Analysis and Simulation of Parasitic Parameters for PCB Planar Transformer," in *2012 International Conference on Control Engineering and Communication Technology (ICCECT)*, Dec. 2012, pp. 241–244.

[4] Alexander Estrov, "Power transformer design for 1 mhz resonant converter," *High Frequency Power Conv. Conf. Rec.*, pp. 36–54, 1986.

[5] A. Estrov, "Low-profile planar transformer for use in off-line switching power supplies," U.S. Patent US5 010 314 A, Apr., 1991, u.S. Classification 336/198, 336/183, 336/200, 336/232; International Classification H01F27/32, H01F19/04, H01F5/02, H01F27/28; Cooperative Classification H01F27/2804, H01F41/043, H01F19/04, H01F5/02; European Classification H01F19/04, H01F5/02. [Online]. Available: http://www.google.com/patents/US5010314

[6] O. Oshiro, H. Tsujimoto, and K. Shirae, "Structures and Characteristics of Planar Transformers," *IEEE Translation Journal on Magnetics in Japan*, vol. 4, no. 5, pp. 332–338, May 1989.

[7] D. v. d. Linde, C. A. M. Boon, and J. B. Klaassens, "Design of a high-frequency planar power transformer in multilayer technology," *IEEE Transactions on Industrial Electronics*, vol. 38, no. 2, pp. 135–141, Apr. 1991.

[8] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC-DC Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.

[9] J. W. Lu, F. P. Dawson, and S. Yamada, "Analysis of high frequency planar sandwich transformers for switching converters," *IEEE Transactions on Magnetics*, vol. 31, no. 6, pp. 4235–4237, Nov. 1995.

[10] X. Margueron, A. Besri, Y. Lembeye, and J. P. Keradec, "Current Sharing Between Parallel Turns of a Planar Transformer: Prediction and Improvement Using a Circuit Simulation Software," *IEEE Transactions on Industry Applications*, vol. 46, no. 3, pp. 1064–1071, May 2010.

[11] C. Buccella, C. Cecati, and M. D. Domenico, "An accurate equivalent circuit of high power/high frequency planar transformers using FEM," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008*, Jun. 2008, pp. 1300–1305.

[12] W. Chen, Y. Yan, Y. Hu, and Q. Lu, "Model and design of PCB parallel winding for planar transformer," *IEEE Transactions on Magnetics*, vol. 39, no. 5, pp. 3202–3204, Sep. 2003.

[13] S. R. Cove, M. Ordonez, F. Luchino, and J. E. Quaicoe, "Applying Response Surface Methodology to Small Planar Transformer Winding Design," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 483–493, Feb. 2013.

[14] J. Ferrell, J. S. Lai, T. Nergaard, X. Huang, L. Zhu, and R. Davis, "The role of parasitic inductance in high-power planar transformer design and converter

integration," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04*, vol. 1, 2004, pp. 510–515 Vol.1.

[15] N. Dai, A. W. Lofti, C. Skutt, W. Tabisz, and F. C. Lee, "A comparative study of high-frequency, low-profile planar transformer technologies," in *Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994., Ninth Annual*, Feb. 1994, pp. 226–232 vol.1.

[16] O. Garcia, J. A. Cobos, R. Prieto, J. Uceda, and S. Ollero, "A standard design method for high frequency PCB transformers," in *Telecommunications Energy Conference, 1995., 17th International*, Oct. 1995, pp. 335–339.

[17] C. Hebedean, C. Munteanu, A. Racasan, C. Pacurar, and D. Augustin, "The influence of parameters on the parasitic capacitance values in a planar transformer," in *2015 9th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, May 2015, pp. 838–843.

[18] E. C. W. d. Jong, B. J. A. Ferreira, and P. Bauer, "Toward the Next Level of PCB Usage in Power Electronic Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 3151–3163, Nov. 2008.

[19] A. I. Maswood and L. K. Song, "Design aspects of planar and conventional SMPS transformer: a cost benefit analysis," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 3, pp. 571–577, Jun. 2003.

[20] R. Prieto, O. Garcia, R. Asensi, J. A. Cobos, and J. Uceda, "Optimizing the performance of planar transformers," in *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual*, vol. 1, Mar. 1996, pp. 415–421 vol.1.

[21] K. Zhang, T. X. Wu, N. Kutkut, J. Shen, D. Woodburn, L. Chow, W. Wu, H. Mustain, and I. Batarseh, "Modeling and design optimization of planar

power transformer for aerospace application," in *Proceedings of the IEEE 2009 National Aerospace Electronics Conference (NAECON)*, Jul. 2009, pp. 116–120.

[22] D. Bowen, A. Lee, C. Krafft, and I. D. Mayergoyz, "Design Control of Performance in Nested and Interleaved Winding Printed Circuit Board Transformers for Ethernet Applications," *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 4013–4016, Jul. 2013.

[23] C. Panchal and J. W. Lu, "High Frequency Planar Transformer (HFPT) for Universal Contact-Less Battery Charging Platform," *IEEE Transactions on Magnetics*, vol. 47, no. 10, pp. 2764–2767, Oct. 2011.

[24] R. Ambatipudi, H. B. Kotte, and K. Bertilsson, "High performance planar power transformer with high power density in MHz frequency region for next generation switch mode power supplies," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 2139–2143.

[25] S. E. Saravi, A. Tahani, F. Zare, and R. A. Kordkheili, "The effect of different winding techniques on the stray capacitances of high frequency transformers used in flyback converters," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, Dec. 2008, pp. 1475–1478.

[26] M. A. Saket, N. Shafiei, M. Ordonez, M. Craciun, and C. Botting, "Low parasitics planar transformer for LLC resonant battery chargers," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 854–858.

[27] W. A. Roshen, "A Practical, Accurate and Very General Core Loss Model for Nonsinusoidal Waveforms," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 30–40, Jan. 2007.

[28] Y. Ma, P. Meng, J. Zhang, and Z. Qian, "Detailed losses Analysis of High-Frequency Planar Power Transformer," in *2007 7th International Conference on Power Electronics and Drive Systems*, Nov. 2007, pp. 423–426.

[29] J. Aime, B. Cogitore, G. Meunier, E. Clavel, and Y. Marechal, "Numerical Methods for Eddy Currents Modeling of Planar Transformers," *IEEE Transactions on Magnetics*, vol. 47, no. 5, pp. 1014–1017, May 2011.

[30] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, Jan. 1994.

[31] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms," in *30th Annual IEEE Power Electronics Specialists Conference, 1999. PESC 99*, vol. 1, Aug. 1999, pp. 580–585 vol.1.

[32] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 964–973, Feb. 2012.

[33] J. Reinert, A. Brockmeyer, and R. W. A. A. D. Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055–1061, Jul. 2001.

[34] "FEKO - EM Simulation Software." [Online]. Available: https://www.feko.info/

[35] M. David, "Finite Element Method Magnetics: HomePage." [Online]. Available: http://www.femm.info/wiki/HomePage

[36] "Ngspice circuit simulator - NEWS." [Online]. Available: http://ngspice.sourceforge.net/index.html

[37] N. Julai, S. P. Chew, and K. A. Hamid, "Modeling Analysis Planar Transformer for Power ICs Application," in *TENCON 2006 - 2006 IEEE Region 10 Conference*, Nov. 2006, pp. 1–4.

[38] J. Li, Y. Shi, Z. Niu, and D. Zhou, "Modeling, simulation and optimization design of PCB planar transformer," in *2005 International Conference on Electrical Machines and Systems*, vol. 3, Sep. 2005, pp. 1736–1739 Vol. 3.

[39] A. Ammouri, T. B. Salah, and F. Kourda, "Modeling and simulation of a high-frequency planar power transformers," in *2015 4th International Conference on Electrical Engineering (ICEE)*, Dec. 2015, pp. 1–6.

[40] L. A. R. Tria, D. Zhang, and J. E. Fletcher, "High-Frequency Planar Transformer Parameter Estimation," *IEEE Transactions on Magnetics*, vol. 51, no. 11, pp. 1–4, Nov. 2015.

[41] Z. Ouyang, J. Zhang, and W. G. Hurley, "Calculation of Leakage Inductance for High-Frequency Transformers," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5769–5775, Oct. 2015.

[42] L. Zhao and J. D. v. Wyk, "Wideband modeling of integrated power passive structures: the series resonator," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 523–530, Mar. 2004.

[43] L. N. T. Tobin A. Driscoll, *Schwarz-Christoffel mapping*, 1st ed., ser. Cambridge monographs on applied and computational mathematics 8. Cambridge University Press, 2002.

[44] H. Hancock, *Elliptic integrals*, 1st ed. Nabu Press, 2010.

[45] M. Hu, D. Hu, Y. W. Ye, W. J. Guo, R. Y. Jia, J. Q. Wang, Z. Li, Z. Hong, and Z. Jin, "Characteristic Tests of GdBCO Superconducting Transformer With Different Iron Core Structures," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–5, Jun. 2017.

[46] A Berger, S Cherevatskiy, M Noe, and T Leibfried, "Comparison of the efficiency of superconducting and conventional transformers," *Journal of Physics: Conference Series*, vol. 234, no. 3, p. 032004, 2010.

[47] V. S. Vysotsky, S. S. Fetisov, V. V. Zubko, S. Y. Zanegin, A. A. Nosov, S. M. Ryabov, N. V. Bykovsky, G. G. Svalov, E. P. Volkov, L. S. Fleishman, and E. A. Dzhafarov, "Development and Test Results of HTS Windings for Superconducting Transformer With 1 MVA Rated Power," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–5, Jun. 2017.

[48] A. Fevrier, T. P. Tavergnier, Y. Laumond, and M. Bekhaled, "Preliminary tests on a superconducting power transformer," *IEEE Transactions on Magnetics*, vol. 24, no. 2, pp. 1477–1480, Mar. 1988.

[49] Ferroxcube, "Ferroxcube E64/PLT." [Online]. Available: http://www.ferroxcube.com/FerroxcubeCorporateReception/datasheet/e641050.pdf