

The development of a burn-in test station for the ATLAS Tile Calorimeter Low Voltage Power Supplies for phase II upgrades

by

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Declaration

I, Thabo James Lepota, (Student no. 568571) declare that this thesis titled, “The development of a burn-in test station for the ATLAS Tile Calorimeter Low Voltage Power Supplies for phase II upgrades”, which is submitted in fulfilment of the requirements for the Degree of Masters of Science, at University of the Witwatersrand, Johannesburg. I hereby declare that this dissertation was written based entirely on my own research, except where other people’s work has been explicitly cited. I further declared that it has not been previously included in a thesis, dissertation, or report submitted to this University or to any other institution for a degree, diploma or other qualifications.



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Abstract

It is planned that the High Luminosity (HL) function of the Large Hadron Collider (LHC) will begin operation in 2027 with an integrated luminosity of 4000 fb^{-1} . By using the HL-LHC scientists will be able to investigate new physics beyond the Standard Model (SM), examine electroweak symmetry in more detail, and examine the characteristics of the Higgs boson. The ATLAS Tile Calorimeter's on and off detector electronics will be completely redesigned during phase II upgrade, run 3. Due to the high radiation levels, trigger rates, and high pile-up conditions associated with the HL-LHC era, it will be necessary to accommodate its acquisition system. The Institute of Collider Particle Physics is responsible for developing and manufacturing over a thousand transformer-coupled buck converters, known as Bricks, for the Low Voltage Power Supply (LVPS) system. The LVPS is critical to the TileCAL on-detector electronics as it powers them by converting 200 V high voltage to 10 V. The Bricks are located within the inner barrel, they can only be accessed once a year. If an LVPS box fails, it can be down for up to a year, causing the Front-End electronics it supports to remain offline for the same amount of time. As a result, the Bricks' reliability is of critical concern that must be addressed throughout their manufacturing process. In addition to the burn-in test station, the Bricks that pass the quality assurance tests are sent to the European Organization for Nuclear Research (CERN), to be installed in the ATLAS detector. In this manuscript, we show how we programmed the Peripheral Interface Controller (PIC) firmware, which is an integral

part of the Brick Interface board functionality in the burn-in test station. We further give detail as to how the software framework (LabVIEW) used as a control program was modified and used to operate the burn-in test station during the burn-in process. The purpose of the test results discussed is to demonstrate the burn-in test station is functional according to the preliminary protocols prescribed for Bricks.

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Molantoa Aaron Lepota: 1976 - 2016

Your teachings and advises will continue to play a role in my life and loved ones.

Until we meet again, Maana nong, nongwana e kgolu nkgodikgodi.

Glossary

ADC Analogue-To-Digital Converters. 4, 34, 75

ALICE A Large Ion Collider Experiment. 8

ALU Arithmetic Logic Unit. 77

ANSI American National Standards Institute. 83

ASCII American Standard Code for Information Interchange. 89

ATCA Advanced Telecommunications Computing Architecture. 41

ATLAS A Toroidal LHC Apparatus. ii, 1

BI Brick Interface. 65

BT Barrel Toroid. 24

CCP Capture/Compare/PWM. 76

CCS Custom Computer Services. 84

CERN European Organization for Nuclear Research. ii, 1

CMS Compact Muon Solenoid. 1

COTS Commercially accessible Off-The-Shelf. 36

CPM Compact Processing Modules. 41

CPU Central Processing Unit. 74

CS Central Solenoid. 24

CU Control Unit. 77

DAC Digital-to-Analogue Converter. 69

DAQ Data AcQuisition. 55

DCS Detector Control System. 36

DEMUX Demultiplexer. 67

DL Dummy Loads. 65, 70

EB Extended Barrel. 38

ECT End Cap Toroid. 24

EEPROM Electrically Erasable Programmable Read-Only Memory. 76

EF Event Filter. 36

ELMB Embedded Local Monitoring Board. 44

EM ElectroMagnetic calorimeter. 30, 31

EPROM Erasable Programmable Read-Only Memory. 75

FCAL Forward CALorimeter. 23, 31

FE Front-End. 27

FELIX Front End LINK eXchange. 41

FENICS Front-End electroNICS. 39

FET Field Effect Transistor. 49

FPGA Field-Programmable Gate Array. 41

FTDI Future Technology Devices International. 67, 90

GPIO General Purpose Interface Bus. 56

GPR General Purpose Registers. 78

HEC Hadronic End-Cap. 17, 31

HEX Hexadecimal. 85

HL High Luminosity. ii

HLT High Level Trigger. 36

HV High Voltage. 40, 42

I/O Input/Output. 74

I2C Inter-Integrated Circuit. 81

IBL Insertable B-Layer. 27

ICSP In-Circuit Serial Programming. 76

ID Inner Detector. 25

IDE Integrated Development Environment. xxiv, 82, 85, 86

IP Inner Pixel. 26

IPE Integrated Programming Environment. 85

LabVIEW Laboratory Virtual Instrument Engineering Workbench. iii

LAr Liquid Argon. 22

LCD Liquid Crystal Display. 76

LHC Large Hadron Collider. ii, 1

LI Load Interface. 65, 69

LV Low Voltage. 43

LVPS Low Voltage Power Supply. ii, 2, 3, 43

MB Main Board. 65, 67

MCU Microcontrollers. 73, 74

MD Micro Drawers. 39

MDTs Monitored Drift Tubes. 32

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 50

MU Memory Unit. 77

NIEL Non-Ionizing Energy Loss NIEL. 51

OCP Over Current Protection. 50

OpAmp Operational Amplifier. 70

OVP Over Voltage Protection. 50

PCBs Printed Circuit Boards. 74

PIC Peripheral Interface Controller. ii, 67, 75

PMTs Photo Multiplier Tubes. 34

POL Point-Of-Load (POL). 44

PSP Parallel Slave Port. 76

RAM Random-Access Memory. 75

RISC Reduced Instruction Set Computer. 76

ROD Read-Out Driver. 35

ROI Regions of Interest. 37

ROM Read Only Memory. 75

RTS Request-To-Send. 67

RW Read/Write. 75

Rx Reciever. 69

SCT Semi-Conductor Tracker. 25

SEE Single Event Effects. 51

SFR Special Function Registers. 78

SM Standard Model. ii, 4

SPI Serial Peripheral Interface. 81

SSP Synchronous Serial Port. 76

TDAQ Trigger and Data AcQquisition System. 34

TID Total Ionizing Dose. 51

TileCAL Tile Calorimeter. 32

TRIS Tri-State. 79

TRT Transition Radiation Tracker. 25

Tx Transmitter. 68

UART Universal Asynchronous Receiver/Transmitter. 67, 80

USART Universal Synchronous/Asynchronous Receiver/Transmitter. 76

VI Virtual Instrument. 92, 133

VISA Virtual Instrument Software Architecture. 91

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Chapter 1

Introduction

The Large Hadron Collider (LHC) [25] at European Organization for Nuclear Research (CERN) is the world's largest and most powerful particle accelerator. It was built with the help of the global community, the same society that now runs the six large experiments and eagerly seeks new physical discoveries and answers to critical unanswered issues in particle physics. The LHC collides proton beams at a hitherto uncharted range of energy, far higher than any prior experiment, allowing researchers to examine particle interactions in previously unknown territory.

At the LHC, A Toroidal LHC Apparatus (ATLAS) is one of two general-purpose detectors. It looks at a wide range of physics topics, from the quest for the Higgs boson to additional dimensions and dark matter particles. It employs distinct technological solutions and a different magnet-system architecture than the Compact Muon Solenoid (CMS) experiment but has the same scientific objectives.

Collisions of particles from the LHC clash at the ATLAS detector's center, resulting in collision debris in the form of new particles that shoot out in all directions from the collision site. The trajectories, velocity, and energy of the particles are

recorded by six distinct detecting subsystems placed in layers surrounding the impact spot, allowing them to be recognized individually. The pathways of charged particles are bent by a massive magnet system, allowing their momenta to be measured.

The interactions in the ATLAS detectors result in a massive data flow. The ATLAS employs an innovative “trigger” mechanism to inform the detector which events to capture and which to disregard to break down the data. The collision occurrences are then analyzed using complex data-acquisition and computation technologies. The 7000-tonne ATLAS detector is the world’s biggest volume particle detector, measuring 46 meters long, 25 meters high, and 25 meters wide. It is located in a cavern 100 meters below earth near the main (CERN) complex in Meyrin, Switzerland.

1.1 Motivation

This study focuses on developing a burn-in test station that can evaluate Low Voltage Power Supply (LVPS) durability under a stressful environment similar to the one found in detectors. In order to power the front-end electronics of the ATLAS tile calorimeter, LVPS is required. Due to their location in the ATLAS detector’s inner barrel, the LVPS boxes are only accessible once a year. Thus, any failure of the LVPS will result in an offline module. In addition, collision data cannot be collected for the same amount of time as before. LVPS dependability therefore plays an imperative role. The dependability of a produced item, such as an LVPS, might differ from its projected design reliability due to quality variances such as component nonconformity. A significant risk of early failure results from these variances. To solve these infant mortality issues, all LVPS devices will be burn-in-tested before

being placed on detectors, boosting their reliability. This is accomplished by forcing LVPS that would otherwise fail early in the TileCal to fail during burn-in testing. Burn-in testing is submitting the LVPS to a burn-in cycle in which they are subjected to suboptimal operating circumstances that excite failure mechanisms. To facilitate the burn-in cycle, a unique burn-in device is necessary. With the planned increase to the luminosity by 5-fold, implies has made difficult for the current system to be able to function optimally this necessitated the ATLAS tile calorimeter's Phase II upgrading program, which aims to compensate for faster stacking rates, higher radiation levels, and the aging of the present electronics. The readout electronics have been replaced with a completely digital trigger system, which sends digital data with full granularity to devices outside the detector. The new design improves timing and energy resolution while being less susceptible to out-of-time pileup.

1.2 Overview of the manuscript

In this chapter, we will look at the main features of the LHC and the most anticipated discoveries. Next, we will look at the two general-purpose detectors installed in the LHC, as well as their design and common problems. Finally, we will look at ATLAS and its properties. In chapter 2, provides an overview of ATLAS experiment with its subsystems and also provides details on the ATLAS tile calorimeter phase II upgrades and their importance within the system. In chapter 3, focuses on the Low Voltage Power Supply (LVPS) with an overview of the Brick design. It also discusses the enhancement to the current prototype in the LVPS Brick including thermal management and real-time monitoring with capabilities to measure and provide: input/output voltage, input/output current and temperature measurements from two places inside the device. LVPS brick verification process and measurements of its temperatures using the test bench are also presented. In chapter 4, shows the crucial

role played by the burn-in to ATLAS TileCal in order to reduce the early life failures of LPVS Bricks. Interventions to replace the failed units is complicated by the fact of the difficult access to TileCal electronics of the ATLAS detector, the existing radiation and the strong magnetic field in the cavern. He also describes each component of the burn-in test station (Main Board, Brick Interface board, Load interface board and Coolant System). In chapter 5, summarises software contributions of developing an application for the burn-in test station with the main goal to provide monitoring, control and data collection capabilities. Microcontrollers are also incorporated in the main board and interface boards to carry out a wide range tasks according to the particular PCB relay messages. Simulations were performed to ensure that the Analogue-To-Digital Converters (ADC) in the circuit are properly functioning. Provide some preliminary results using the burn-in for one Brick undergoing burn-in process. Last chapter is conclusion on the work done and future prospects on the project.

1.3 The LHC

1.3.1 Uncover possibilities

The main aims of the LHC proton-proton physics program are to test and verify predictions of Elementary Particle Physics theories, and to search for new physics. Elementary Particle Physics attempts to describe how the universe works by studying the most fundamental constituents of matter and their interactions. To date, the Standard Model of Particle Physics is the most complete theory describing the fundamental interactions and classifying all the known elementary particles.

The Standard Model (SM) illustrates the microscopic universe as a series of interactions between matter particles involving forces that act via the interchange of in-

STANDARD MODEL OF ELEMENTARY PARTICLES



Figure 1.2: Schematic depiction of the Standard Model of Particle Physics. To the left: three generations of matter. To the right: gauge bosons, the Higgs boson and the still undiscovered graviton [78].

that must be fine-tuned to fit the observations. Many of our observations in nature hint to a hypothesis other than SM. Here are few selected examples:

- Neutrinos are projected to have no mass in the SM because they do not couple to the Higgs field. However, oscillations between the three various forms of neutrinos, or “flavors”, have been recorded [2], demonstrating that neutrinos are really heavy. These oscillations may indeed be explained if neutrinos have mass eigenstates that differ from their flavor eigenstates. As expansions to the SM, mechanisms for the neutrino to gain mass are thus necessary [13].
- There is currently compelling cosmological evidence that the universe’s energy content, as well as its pace of expansion, cannot be described only by the SM. To explain these facts, some theories propose cold dark matter [12] and repulsive dark energy [63], which would account for a considerable amount of our universe’s energy content.

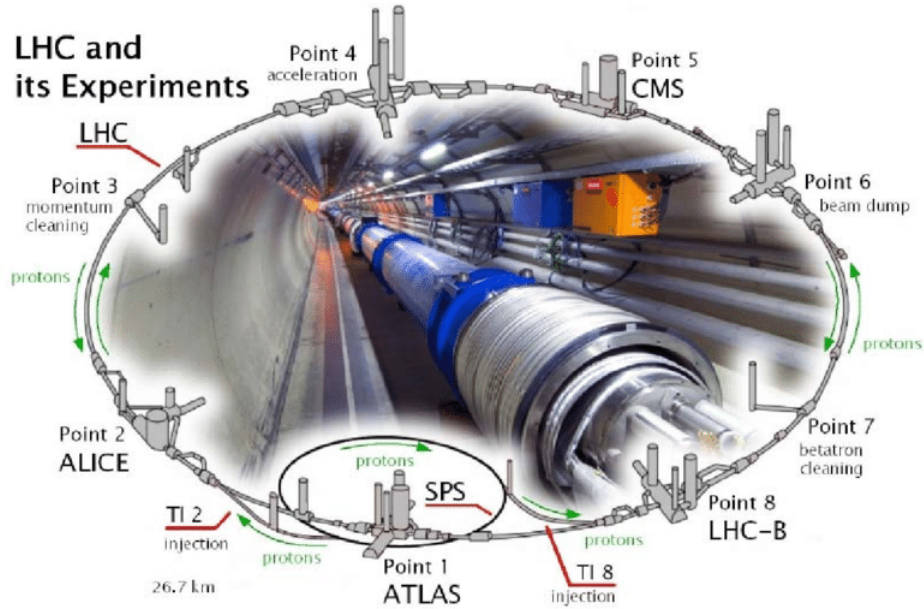


Figure 1.3: Experiments at the LHC and their location [15].

- It is reasonable to hypothesize that there should be a theory that connects the electroweak and strong forces, just as it has been demonstrated that the weak and electromagnetic forces are expressions of the same gauge invariant theory that is subject to symmetry breaking. This is only one of many convincing reasons why a Grand Unified Theory (GUT) of basic forces should include our SM of particle physics [33].

The LHC's ATLAS detector attempts to test our knowledge of the SM and hunt for evidence of beyond SM physics. The LHC is upgraded to the High Luminosity (HL-LHC) in order to boost the sensitivity of the detectors on its ring to uncommon processes. The ATLAS detector and its extension, which will run concurrently with the LHC, are discussed in the upcoming sections.

1.3.2 The LHC Experiments

All experiments are encased at the LHC as shown in Figure 1.3. The recent discoveries are most likely the result of the two general-purpose detectors the ATLAS

and CMS. The additional trials are intended for more focused research: A Large Ion Collider Experiment (ALICE) will be the results of the Pb-Pb collision, such as the predicted quark-gluon plasma property. Instead, LHCb (LHC beauty) will focus on the physics of B-mesons. TOTEM (TOTal Elastic and diffractive cross section Measurement) and LHCf (LHC forward) are smaller detectors that examine soft collision characteristics and are linked to CMS and ATLAS, respectively.

ATLAS and CMS are LHC general-purpose particle detectors that can detect electrons, photons, muons, hadrons, and jets generated when particles collide or decay. The detectors may also determine the presence of neutrinos if they cover a large solid angle around the collision point using the missing transverse impulse approach if they cover a big solid angle around the collision point. The fact that two detectors are meant to examine the same sort of phenomenon may appear redundant; yet, this trait is extremely beneficial since it allows for cross-checking of potential discoveries with separate methodologies. The similar function and operating conditions shape the two detectors almost identically; nonetheless, the particular design of each detector and the choice of magnet system are so different that each one has a distinct personality. After three years of operation, these two experiments announced the discovery of a new elementary mass particle with a mass of 125 GeV, as predicted by the 50-year-old Higgs Boson (SM) [27]. The LHCb is intended to explore CP (Conjugation and Parity) violation in the bottom quark sector, whereas ALICE is intended to study quark-gluon plasma from heavy ion, lead-lead, and lead-proton collisions [16].

1.4 Plans for LHC and ATLAS detector upgrades

1.4.1 The High Luminosity LHC

The LHC is intended to collision protons at 14 TeV center of mass energy and deliver a total integrated luminosity of 300 fb^{-1} to each of its two general purpose detectors, ATLAS and CMS. Figure 1.1 depicts the LHC flow chart. It has so far hit 13 TeV and provided over 100 fb^{-1} of data. Data gathered at the LHC since 2010 have resulted in some of the most accurate measurements of SM parameters and toughest constraints for beyond SM values, when combined with the discovery of the Higgs boson. However, without a considerable rise in instantaneous luminosity beyond 2020, the LHC's statistical gain will be minimal, and it will take ten years to half the statistical error in the data. The LHC will be updated during Long Shutdown 3 (LS3) 2024-2026 to increase its discovery potential and retain statistical benefit from running for a longer length of time. This increase results in an instantaneous brightness that is roughly 5 to 7 times more than the initial design value, enabling for the collection of 3000 to 4000 fb^{-1} collision data over the following 10 to 12 years [9].

1.4.2 The ATLAS detector upgrade plan

In addition to the LHC, numerous upgrades for the ATLAS detector are planned in order to ensure appropriate physical performance with a greater instantaneous luminosity and to deal with the impacts of long-term radiation exposure owing to the increased integrated luminosity. These improvements are carried out during the lengthy downtime periods of LS1, LS2, and LS3.

The ATLAS detector's Phase-II modifications will be undertaken during LS3. A significant improvement to the trigger and data collecting system is in the works. The

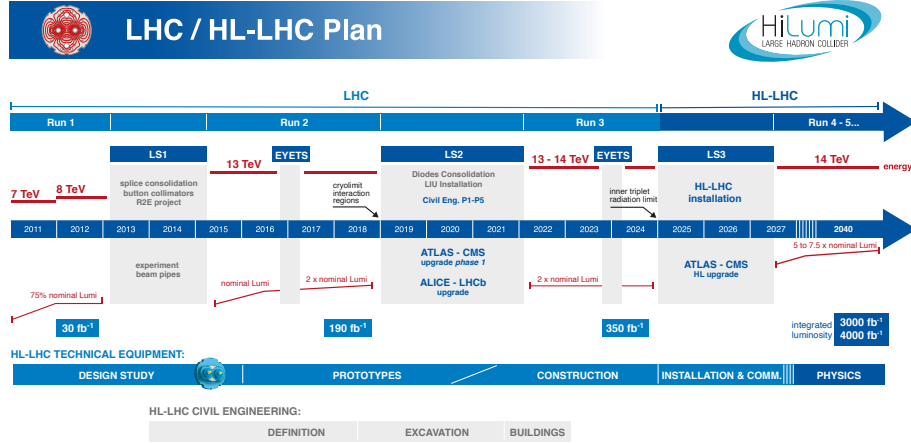


Figure 1.4: LHC upgrading strategy [39]. The collision energies of the center of gravity are represented in red, the current brightness in green, the integrated luminosity in fb^{-1} , the Long Shutdown (LS) periods, LS1, LS2, and LS3, and the Extended Year-End Technical Stop in blue (EYETS).

L1 trigger is divided into two levels: a L0 level that will continue to use the same topological algorithms established in Phase-I, and a new L1 trigger with a higher latency budget and access to the full granularity of Has information from the calorimeter system. This necessitates a thorough refurbishment of the calorimeter's front and back end electronics. The new electronics must match the criteria of the level 1 trigger system, including a 1 MHz trigger, higher resilience to ambient radiation, and enhanced performance under high pile-up situations.

1.5 Principles of calorimetry

The readout signal for calorimeters is created in the active material by ionization, excitation, or Cherenkov radiation from the shower process, depending on the type. Calorimeters are crucial in high-energy physics because of the following characteristics:

- As the energy of the incoming particle increases, the calorimeter's energy resolution improves.
- Calorimeters are systems that can detect the energy of both neutral and charged particles.
- Calorimeters offer accurate location readings when precisely segmented.
- Calorimeters provide good particle identification thanks to longitudinal segmentation.

The final element is really beneficial and can also help to lower the experiment's cost. Homogeneous and sample calorimeters are the two types of calorimeters. The active and passive materials are equivalent in the first scenario, and the entire shower contributes to the signal creation. The scanning calorimeter in the second scenario is made up of alternating active and passive materials, with the active section being read out to provide a scanned signal of the deposited energy. The longitudinal summation can be used to recreate the energy. The longitudinal shower data can be used to identify certain particles at a low cost.

1.6 Basics of the Calorimetry

1.6.1 General

Particle detection methods are mostly dependent on their interactions with matter. In all calorimeters, these sensitive materials are employed. Only the electromagnetic and strong relevant interactions are significant among the four fundamental interactions. The key trait of increased resolution with rising particle energy and the restoration of missing transverse energy is exploited in current calorimeters for particle detection. Because the energy in colliders are rapidly growing, the first attribute in particular holds considerable potential for the future. Only the energy loss

due to electromagnetic and strong interactions is explained in the following since it is the most important. There is an excellent discussion on this topic in the review of particle physics [47], notably in chapter 27. updated on reference [35].

1.6.2 Energy loss by electromagnetic interaction

The Bethe-Bloch equation is a suitable description for phenomena in which charged particles with high energy collide with matter. We may express the Bethe-Bloch formula in its entirety using E as the particle energy and x as the distance a particle travels in an absorber:

$$-\frac{dE}{dx} \simeq 4\pi r_e^2 m_e c^2 N_A z^2 \phi \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 T_{max}}{I^2 (1 - \beta^2)} - \beta^2 - \frac{\delta}{2} \right]. \quad (1.1)$$

The symbol e stands for electron. The symbols r and m stands for the classical electron radius and mass respectively, z and Z for the incoming particle and absorber core charge, N_A and A for the Avogadros number and relative atomic mass of the absorber respectively, as well as for the mass density, ϕ and density effect correction of the ionization, δ , whereas T_{max} stands for the maximum kinetic energy that may be transmitted to a free electron in a single collision, and energy loss, $\beta = v/c$. Figure 1.5 shows how a charged particle loses energy as a result of several forms of electromagnetic interactions. Ionization is the most common way for electrons and positrons to lose energy.

Lower energies are used in e^-e^+ annihilation and Bhaba scattering. The photoelectric effect, Compton and Rayleigh scattering, and photonuclear absorption all help low-energy photons lose energy. For charged particles with a smaller mass, the bremsstrahlung process begins to dominate as β rises. Except for electrons, where there is an inverse mass dependency, it is irrelevant at energies below 1 TeV.

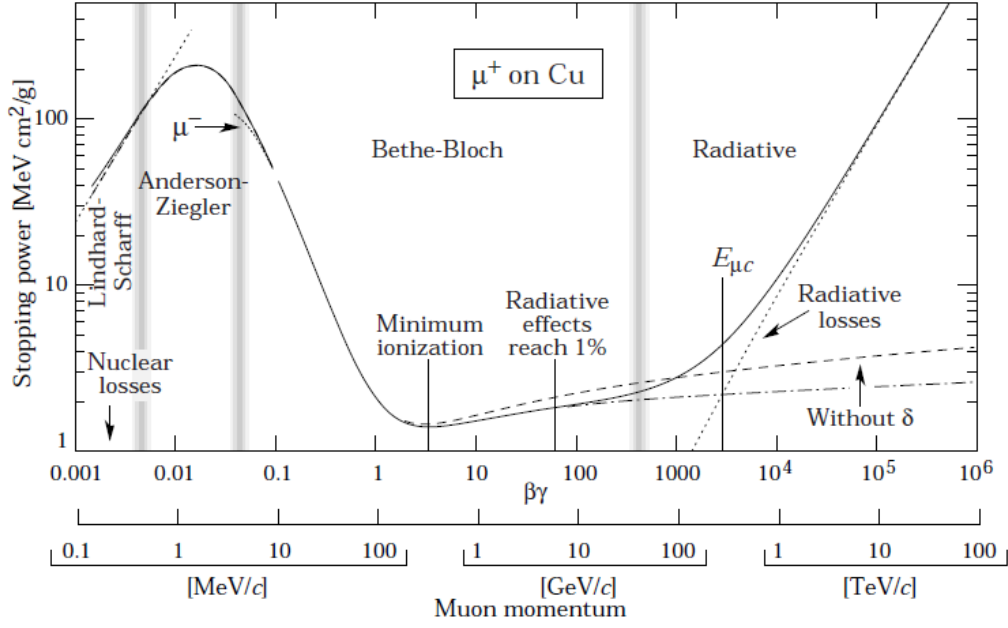


Figure 1.5: Energy loss of a muon in Cu [35]. There are shown influences to energy loss by some processes and the critical energies.

We can expect energy loss in the e^-e^+ pair generation when dealing with high-energy photons. Ref. [66] has further discussion.

1.6.3 Energy loss by strong interaction

The theory of Quantum ChromoDynamics (QCD) has been very successful in explaining all strong interaction processes, but there is no full explanation for the process of hadrons losing energy when they collide with matter. Monte Carlo simulations, which employ cross section data to model various processes, are a good approach. Above the nuclear resonance, the cross-section for hadron-nucleus collisions display a mild energy dependency [66]. We may define the probability $p(x)$ for a high-energy hadron traversing matter of distance x without encountering absorber cores, taking into account the core integration length λ_I for proton-nucleon interactions [47]:

$$p(x) = \exp\left(-\frac{x}{\lambda_I}\right), \lambda_I \simeq 35 \cdot \frac{A^{\frac{1}{3}}}{\phi} \frac{g}{cm^2}, \quad (1.2)$$

where ϕ is the density of the absorber.

1.6.4 Electromagnetic and hadronic shower cascades

When high-energy particles move through matter, they cause a so-called *shower cascade*, which is caused by various interactions between the particles inside the substance (the absorber of the calorimeter). This process is continued by the second generation of particles, which establishes new interactions. When the energy of the last secondary side surpasses the particle production limit, the cascade comes to an end. It's important to distinguish between the electromagnetic and hadronic showers. Electromagnetic showers are just briefly described due to their larger relevance for hadronic showers.

1.6.4.1 Electromagnetic shower cascades

A shower is formed by high-energy photons losing their energy in a e^-e^+ pair formation, in which the electrons release bremsstrahlung photons, and lasts until one of these instances occurs: The energy loss from ionization and excitation via bremsstrahlung begins to dominate, or the energy of the photons falls below the pair formation limit, and the Compton effect begins to dominate. A useful parameterization is given in [65], which states that the length of: contains 98% of the incident particle energy:

$$L(98\%) = 2.5X_O \left[\ln \left(\frac{E}{E_c} \right) + C \right], \quad (1.3)$$

where E and E_c are the incoming and critical energy (of the absorber), respectively. The factor C contains $+0.5$ for photons and -0.5 for electrons/positrons. Using the Molliere-Radius R_M it is possible to express the transverse extension of an electromagnetic shower [47]:

$$R_M = \frac{m_e c^2 \sqrt{\frac{4\pi}{\alpha}}}{E_c} X_O \approx 21 \text{ MeV} \frac{X_O}{E_c}, \quad (1.4)$$

where X_O again is the radiation length of the absorber. In a calorimeter, 95% of the shower energy is deposited in a cylinder with radius $2R_M$ around the axis of the showers incident particle. The expansion of the shower decreases with materials with high Z . It is useful to use such materials in electromagnetic calorimeters.

1.6.4.2 Hadronic shower cascades

As previously stated, high-energy hadrons generate shower cascades that persist until the energy necessary for future hadron creation is lowered. Hadron showers do not occur in a purely hadronic state because they have an electromagnetic component. It is assumed that each interaction generates around two-thirds charged pions and one-third neutral pions. We also assume that the mean multiplicity is simply proportional to the output energy, thus the lowest order slow variation may be ignored. The creation of π^0 is an irreversible portion of the shower, as it decays into photons instantaneously. Photons form an electromagnetic shower with a characteristic length scale X_0 that is often shorter than λ , causing π^0 to exit the shower fast. The charged pions are responsible for the deeper energy transmission. The weak decays of hadrons, as well as the ionization and excitation of the absorber material, contribute to the electromagnetic component. The percentage of this electromagnetic component is primarily responsible for the huge variations. The average path taken by a hadron after it has deposited 95% of its starting energy is as follows:

$$\lambda_{95\%} \equiv \left[0.4 \cdot \ln \left(\frac{E}{\text{GeV}} \right) + 39 \right] \text{ cm} \cdot \frac{\lambda_I}{\lambda_I(\text{Fe})}. \quad (1.5)$$

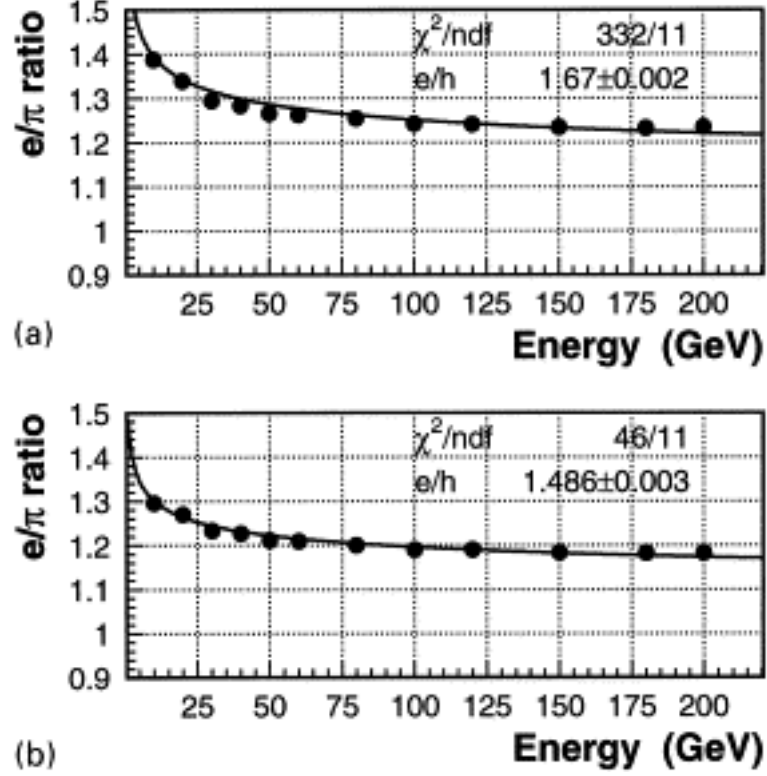


Figure 1.6: The Hadronic Endcap Calorimeter's e/π ratio, as observed in a separate beam test [30].

The interaction length λ_I is typically larger than the radiation length X_O [48] (a factor 6 for LAr and 10 for Cu). It comes out that a hadronic cascade is about one order of magnitude higher than the electromagnetic one.

1.6.5 Energy reconstruction

In a cascade, the number of secondary particles produced is precisely proportional to the incident energy of the parent particles. As a result, all contributions may be summed to obtain the total signal in the medium, which is proportional to the energy as $E = \alpha \cdot \text{signal}$, where the proportionality constant is set by calibration. The constant in electromagnetic showers is independent of energy, while the case in hadronic showers is more difficult to answer. Two significant consequences must be

considered: (a) the energy of a hadron is not totally deposited in the calorimeter, and (b) only a portion of this energy is transformed into an electronic (read) signal. The first scenario is commonly referred to as energy loss. The second instance is mostly caused by particles that are halted in an insensitive absorber layer, energy from nuclear bond breakage, and the fraction of neutrons created in nuclear processes that do not contribute to the signal. When these effects are combined, the energy becomes invisible.

As a result, the energy response of a pure hadronic shower has a significantly larger distribution than the energy response of an electromagnetic shower of the same energy, and the responses of these two showers are often different:

$$\frac{e}{h^{intr}} > 1. \quad (1.6)$$

The ratio $\frac{e}{h^{intr}} > 1$ is the response of a calorimeter to EM and hadronic components of a cascade and is energy independent. If the previous inequality holds it is referred to a *non-compensating* calorimeter. The measured sampling ratio for electrons, $e = E_{vis}/E_{beam}$ is equivalent to $1/\alpha_{EM}$ is not like the one for hadrons (π) which is energy dependent due to the energy dependence of the electromagnetic component. For the special case of Hadronic End-Cap (HEC) the e/π is shown in Figure 1.6 [10].

1.6.6 Energy resolution

The quantity of secondary particles generated in a shower is proportional to the signal, resulting in an energy resolution $\sigma/E \approx 1/\sqrt{E}$ in close proximity [34]. By incorporating the three most essential terms in the parameterization of a sample calorimeter's resolution, we get:

$$\frac{\sigma}{E} = \frac{a}{\sqrt{E}} \oplus b \oplus \frac{c}{E}. \quad (1.7)$$

The first term, known as the sampling term, accounts for the inherent shower fluctuations. The second term is a constant component that includes the energy loss in the calorimeter, calorimeter inhomogeneity and incorporating inhomogeneity $\frac{e}{h^{intr}} \neq 1$. The third term accounts for electronic noise, which should be the same for all energies. As a result, the $1/E$ dependence exists.

1.7 Electromagnetic Calorimeters

To detect electrons and photons, electromagnetic calorimeters were invented. Quantum electrodynamics (QED) represents the relation of these particles quite adequately [36]. Electrons and photons behave quite differently when they contact with matter. While the energy of the electrons is lost without destroying the electrons, photons are often transformed into other particles. As a result, the interaction of electrons is defined in terms of energy loss per unit length, whereas that of photons is characterized in terms of cross-sections. Figure 1.7 depicts the numerous mechanisms that contribute to the energy degradation of electrons interacting with the material as a function of electron energy. Figure 1.7 (Left) depicts the graphs obtained for electrons and photons that interact with lead. Figure 1.7 (Right) depicts the photon interaction cross sections as a function of photon energy.

Electrons with energies larger than roughly 10 MeV lose energy mostly owing to bremsstrahlung [52], whereas photon interactions in this energy range primarily form electron-positron couples. When secondary photons, electrons, and positrons reach a sufficient energy, they can interact through the same mechanisms that produce the shower. Ionization and thermal excitation for electrons and Compton

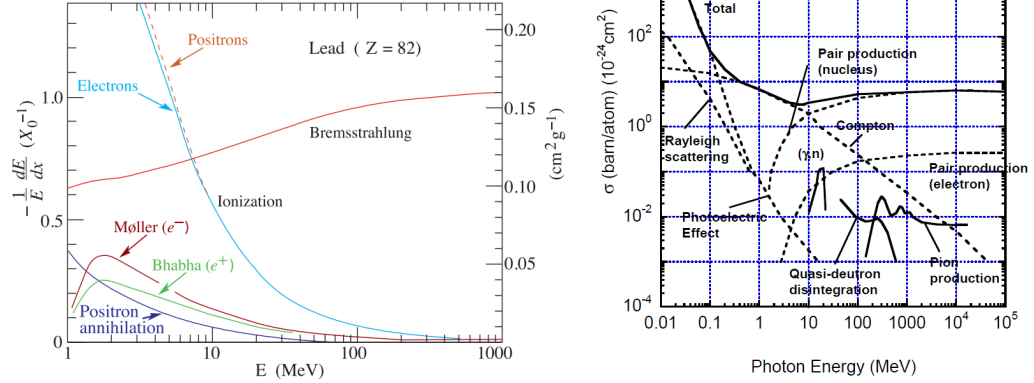


Figure 1.7: LEFT: Contribution of several mechanisms to energy loss per unit length of electron interacting in lead as a function of electron energy [52]. RIGHT: Cross-sections of several photon interaction mechanisms in lead as a function of photon energy [52].

scattering and photoelectric effect for photons are the key interaction events below the critical energy. Taking these phenomena and general calorimeter dimensions into consideration, the interaction length X_0 provides an appropriate scale. A radiation length for electrons specifies the rate at which electrons lose energy due to bremsstrahlung. In reality, a radiation length is the average distance travelled by an electron in a substance to lower its energy to $1/e$ of its starting energy:

$$E(x) = E_0 \exp\left(\frac{x}{X_0}\right). \quad (1.8)$$

Similarly, the radiation length of a photon beam describes the rate at which the intensity of the beam is diminished via pair creation. In this example, the photon beam intensity is lowered to $1/e$ of its starting intensity after a radiation length of $9/7$ of the typical quantity of matter.

$$I(x) = I_0 \exp\left(\frac{x}{\frac{9}{7}X_0}\right). \quad (1.9)$$

The radiation length is determined by the material's properties and may be evaluated as [32]:

$$X_0 \simeq \frac{716}{Z(Z+1) \ln \frac{287}{\sqrt{Z}}} \frac{A}{g} \text{ cm}^{-2}, \quad (1.10)$$

where A and Z are the mass and, as a result, the atomic numbers of the medium. There are two definitions for critical energy for electrons: it is often thought to be the energy at which bremsstrahlung energy losses are identical to ionization energy losses, or it is the energy at which ionization losses per radiation length are equal to electron energy; these definitions are equivalent within the approximation:

$$\left(\frac{dE}{dx} \right)_{\text{bremsstrahlung}} \simeq \frac{E}{X_0}, \quad (1.11)$$

where X_0 is the radiation length.

The critical energy ϵ is determined by the material's properties and may be approximated by [32]:

$$\epsilon \simeq \frac{610}{Z + 1.24} \text{ MeV (solids)} \quad \epsilon \simeq \frac{710}{Z + 0.92} \text{ MeV (gases)}. \quad (1.12)$$

In lead, $\epsilon \simeq 7 \text{ MeV}$ is depicted in Figure 1.7. When stated in $4 X_0$, equations 1.8 and 1.9 reveal that the physical scale on which a shower forms for incoming electrons and photons is comparable and irrespective of the kind of material. As a result, electromagnetic showers may be generically characterized by simple functions of radiation length. The normal longitudinal size of electromagnetic calorimeters at the LHC is around $25 X_0$, and the average energy that passes beyond the material is less than 1% for this dimension.

1.8 Hadronic Calorimeters

Energy depletion of hadrons occurs in the same way that electromagnetic showers do, by increasing the number of (mainly) strong interactions with the calorimeter material. The precise explanation of the formation of a hadron shower, on the other hand, is far more complex than that of an electromagnetic shower. The hadronic interactions may be reduced by categorizing the processes into two types of effects. In the first class, we have processes in which incident hadrons with GeV energies create secondary hadrons with the same order of energy and a mean free path (interaction length) of $\lambda = 35A^{1/3} \text{ gcm}^{-2}$ [32]. Collisions with middle nuclei in the second grade result in a variety of processes like as spallation, nucleon evaporation, and so on, with particles with energy on the MeV scale lingering behind and absorbing a significant portion of the original energy.

Chapter 2

The ATLAS experiment

2.1 ATLAS subsystems

For each particle created in a collision, data from the tracking, calorimeter and muon spectrometer components is integrated to determine the particle's identity and describe it (Figure 2.1). ATLAS magnet system measures the momentum and energy of charged particles by bending their paths in a specified magnetic field. To measure muon energy, a system of superconducting toroidal magnets in the muon spectrometer produces a field of 0.6 T that creates a field of exact momentum and charge measurements. This instrument consists of a high-granularity Pixel Detector for precise vertex reconstruction, a semiconductor strip tracker for high density track measurement near the beam pipe, and a straw-tube tracker for large-radius tracking and particle identification from the Inner Detector system

Neither calorimeter uses high-density materials to absorb electrons, photons, or hadrons, but both use active materials that generate a signal that is proportional to secondary particles and particle cascades deposited in the calorimeter. A layer of Liquid Argon (LAr) is layered between layers of absorbing material lead and layers of active

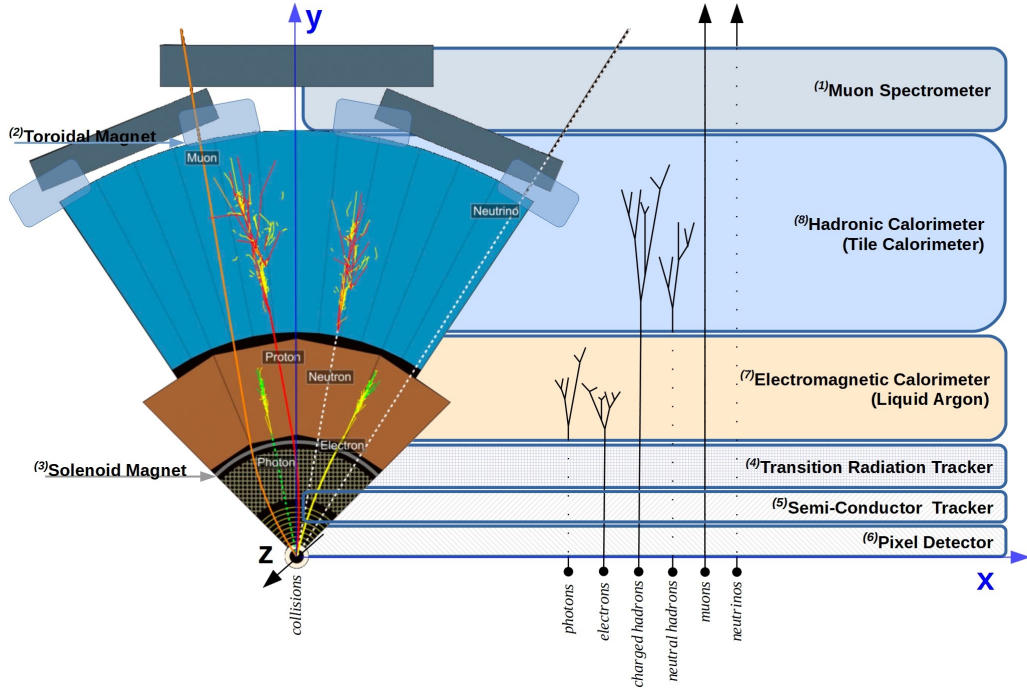


Figure 2.1: Particle paths in the ATLAS detector [55].

material LAr. In addition to the electromagnetic barrel calorimeter, LAr consists of electromagnetic end-caps and hadronic end-caps, including the Forward CALorimeter (FCAL). It is highly detailed, with about 2,00000 channels, enabling measurement of electron and photon energy and location. In order to achieve optimum heat transfer, the outer calorimeter (TileCAL) is made from steel sheets covered with scintillating plastic tiles. As a result, TileCAL's granularity is less than LAr's, with approximately 10,000 photomultiplier channels that monitor scintillating light produced by hadrons and hadronic jets.

In ATLAS, the Muon Spectrometer is the most distant detector. A total of 1200000 channels are available in this sub-detector, which is comprised of three massive air-core toroid systems with gas-filled tracking chambers to monitor muons bending radius as they leave the detector. A high muon momentum resolution is also provided by the subsystem, which enables muons to be distinguished from cosmic rays and collisions.

2.1.1 Magnet System

The magnet system consists of a Central Solenoid (CS) in front of the electromagnetic calorimeter and three air core toroids on the ATLAS detector's outer surface, one in the cylinder section, Barrel Toroid (BT) and two on the End Cap Toroid (ECT). The magnetic field at the transition area is produced by the superposition of the BT and ECT fields. The center solenoid generates a nominal 2 T magnetic field in the inner detector region, with a peak of 2.6 T near the coil. It is designed to use as little material as possible and shares a vacuum vessel with the electromagnetic calorimeter, removing two barriers. The three toroids are made up of eight coils placed radially and symmetrically around the beam axis.

Each coil in the BT is contained in its own cryostat (which takes the forces between the coils), and the toroidal structure is completed by connecting parts that give mechanical stability. A cryogenic ring connects the eight cryostats to a service cryostat and provides access to the power supply, helium refrigerator, vacuum system, and control system. Instead, the eight coils in the ECT are contained within a single cryostat, and the internal stresses are absorbed by a cold structure between the elements. The coils are mounted on a rail to provide simple access to the detector's inside. Helium flows at 4.5 K and is forced through pipes soldered to the windings' casing to cool the magnets indirectly. Furthermore, the CS is conditioned by a dewar connected to the refrigerator, whereas the BT and ECT are cooled by a cold helium pump. The four magnets share a cooling capacity.

2.1.2 Inner detector

The detector's interior is dedicated to the reconstruction of charged particle paths (tracks) with their momentum, as well as the reconstruction of interaction nodes and the identification of electrons. These needs are satisfied by accurate trace measure-

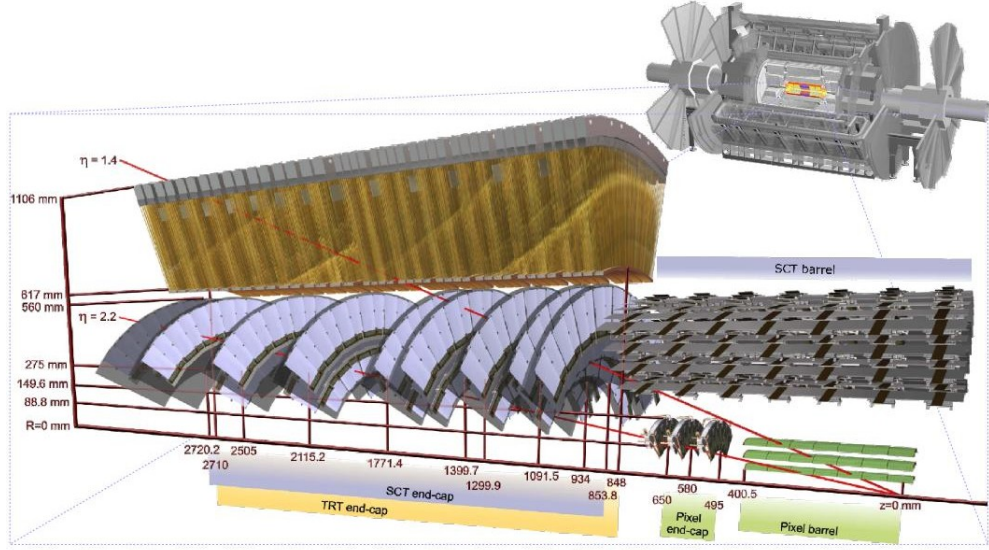


Figure 2.2: The inner detector [53].

ment, which the combination of pixel and Semi-Conductor Tracker (SCT) provides near the site of interaction with a Transition Radiation Tracker (TRT) for greater radii. The core magnetic coil, which creates a 2 T magnetic field, surrounds the inner detector. The bending of tracks in the presence of a magnetic field is used to extract the momentum of charged particles.

Figure 2.2 depicts the Inner Detector (ID) layout and design architecture. There are two types of Three ID sub-detectors. The cylinder with a low η consists of concentric cylinders around the beam axis, whereas the end caps with a high eta are organized in disks perpendicular to the beam axis. This arrangement provides maximal eta coverage of up to $|\eta| < 2.5$ for the pixels and SCT and up to $|\eta| < 2.0$ for the TRT while covering the whole ϕ range. Aside from the cover, the stem and end cap designs reduce material bulk. Indeed, particle escape from the inner detector is crucial in order to avoid repeated scattering, which would impair the precision of position and momentum measurements in the ID and energy resolution in the calorimeters. Aside from two peaks near $|\eta| \simeq 1.5$ and $|\eta| \simeq 3$, the radiation length is dominated by

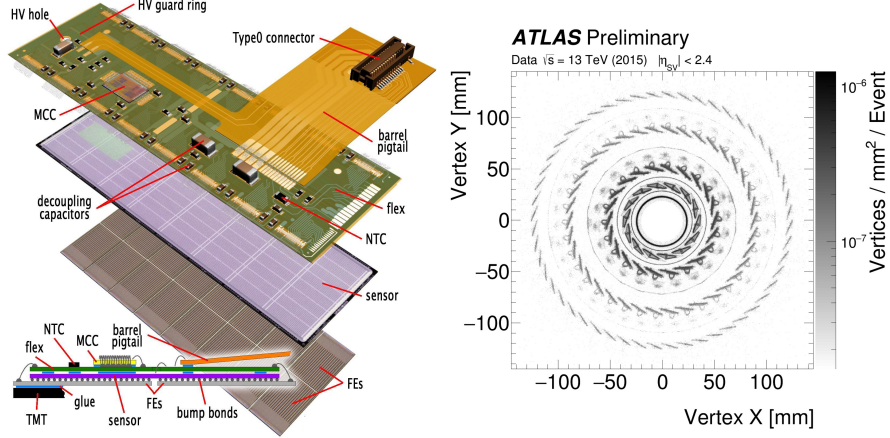


Figure 2.3: Left: The ATLAS pixel module layout [49]. Right: The pixel detector is depicted in this plot using reconstructed vertices corresponding to material interaction in data acquired with the ATLAS detector at $s = 13$ TeV [24]. It emphasizes the geometry of the pixels as well as the layout of the staves [21].

the TRT in the central area of the inner detector and by the pixel support tube for greater eta due to the end plates of the cylinder and end cap.

2.1.2.1 The Pixel Detector

The Inner Pixel (IP) detector is the device nearest to the site of contact. Because of its high spatial resolution, it is possible to monitor the route trajectory in close proximity to the IP with great precision. As a result, it provides the highest accuracy for detecting displaced vertices, which is critical for algorithms based on the identification of long-lived particles, such as b -tagging. The pixel detector is the device nearest to the IP. Because of its high spatial resolution, it is possible to monitor the route trajectory in close proximity to the IP with great precision. As a result, it provides the highest accuracy for detecting displaced vertices, which is critical for algorithms based on the identification of long-lived particles, such as b -tagging. The IP detector is constructed using silicon semiconductor technology. The ionization charge deposit of charged particles passing in a p-n junction is collected by each pixel. The rapid shift from an n-bulk to a p-bulk is compensated for by oxygen n-doping on the

backside and n+ implants on the read-out for improved charge collection. The sensor is made up of 47232 of these pixels, which are bump-bounded to 16 Front-End (FE) processors with 2880 read-out channels each.

This assembly is known as a module, and it is depicted in Figure 2.3 (Left). The FE chip pitch limits the size of 90% of the pixels. Others are longer in order to provide some gap between neighbouring chips. The staves are made up of 13 modules that are parallel to the beam axis. To retain the cylindrical form and assure complete azimuthal coverage, each layer consists of 14, 22, 38, 52 staves arranged from innermost to outermost with an inclination in ϕ . Figure 2.3 (Right) depicts a cross-section of the pixel layers in the transverse plane to exhibit the geometric design and stave arrangement. Reconstructed traces are utilized in this picture to identify vertices that are consistent with material interactions. After that, all of the vertices are projected onto the transverse plane. Table 2.1 summarizes the pixel detector parameters. The inner detector meets the $|\eta|$ coverage criteria and provides extremely excellent hit position resolution, particularly the Insertable B-Layer (IBL), which is closer to the IP and has smaller pixels.

The old layers of the pixel detector are chilled to -10 °C using C_3F_8 gas to retain a very high output over time and to prevent radiation damage. The cooling technique was chosen, because of its radiation resistance. The pixels are encapsulated with N_2 gas to prevent moisture collection. The IBL benefits from a CO_2 gas cooling tube, which provides the same performance as the other layers while shortening the radiation length of this layer.

Table 2.1: Parameters and intrinsic resolution of the inner detector components in the barrel and end-cap regions.

Barrel layer	r (mm)	N (modules)	Pixel size (μm^2)	Intrinsic resolution (μm^2)
Insertable-B-Layer	33.2	280	50×250	$8(r \cdot \phi)40(z)$
B-Layer	50.5	280	50×400	$10(r \cdot \phi)115(z)$
Layer-1 and -2	88.5, 122.5	280	50×400	$10(r \cdot \phi)115(z)$
End-cap	Z (mm)	N (modules)	Pixel size (μm^2)	Intrinsic resolution (μm^2)
Disk $\times$ 3	495, 580, 650	48	50×400	$10(r \cdot \phi)115(R)$

2.1.2.2 The Semiconductor Tracker

The SCT [1] is situated in the vicinity of the pixel detector. The subsystem is responsible for measuring eight parameters per lane that contribute to velocity calculations, impact parameter calculations, and vertex position computations. In order to support its cooling systems, the SCT's four cylinder modules are mounted on carbon fiber tubes, and its end caps consist of nine annular discs at each end of the cylinder area. This 6.2 million-channel configuration provides hermetic azimuthal coverage of $|\eta| \leq 2.5$, with a radial coverage of approximately 30 to 52 cm. Each module comprises four unidirectional silicon p-on-n detectors. Two detectors are wired together in strips on each side of the module. The electronics are placed above the detectors and two of these strips are connected in a back-to-back arrangement separated by a heat transfer plate. The pixel detector and SCT both require very good dimensional stability, somewhat cool detector operation (-7°C), and adequate heat dissipation from both detector leakage and electronics.

2.1.2.3 The Transition Radiation Tracker

With a diameter of 30 mm, a gold-plated tungsten sensor wire is embedded in the center of the straw, and the surface is constructed of conductively coated Kapton. The cathode holds the sensor wire at a high voltage of negative polarity focusing

light on it. A gas mixture of 70% Xe, 27% CO_2 , and 3% O_2 is filled between the straw layers to increase X-ray absorption, quench photons and increase electron drift speed. Polypropylene sheets or fiber emitters between the straw layers are used to enhance electron drift speed. As the electrons move through the nested radiators, a series of X-rays are created, which provide additional distinction between hadrons and electrons.

2.1.2.4 Inner Detector Alignment

The tracking performance is strongly reliant on the accuracy of the internal detector alignment. To fix the misalignment, translations and rotations along each axis may be used to reposition each component of the ID in its local frame. Several layers of alignment are carried out:

- Level 1: Alignment of four separate blocks: IBL, pixel detector, SCT, and TRT.
- Level 2: Each detector's layers and slices are aligned independently. The layers of the TRT are made up of 32 modules apiece.
- Level 2.7: Alignment of each stave separately
- Level 3: During this final stage, there are 701,696 degrees of freedom for each IBL module, pixel, SCT detector, and TRT straw.

The inner detector is aligned using muons from cosmic rays and collision data gathered in 2015 [20]. As a reference, the TRT is used and recorded. In increasing order of precision, the detector components are aligned using each plane progressively. When a suitable alignment is obtained, the procedure for that layer is terminated.

2.1.3 The Calorimeter system

The ATLAS calorimeter system [6] is designed to absorb and quantify the energy of particles emitted by the collision point, with the exception of muons, neutrinos,

and potentially previously unknown weakly interacting particles. ATLAS calorimeters are divided into two layers to monitor different types of particles, as electromagnetic particles shower and lose energy faster than hadrons. During their travel through matter, photons, positrons, and electrons of the Electromagnetic Calorimeter experience bremsstrahlung and pair production. These processes continue until there is not enough energy to continue them. As particles pass through the Hadronic Calorimeter, hadrons interact with atomic nuclei to produce particle showers. It is possible to calculate the entering particle energies from the energy that is deposited by the cascades the particles generate. The Electromagnetic Calorimeter covers a region corresponding to pseudo rapidity of $|\eta| \leq 3.2$, whereas the hadronic barrel calorimeter covers $|\eta| \leq 1.7$, ended-cap calorimeters cover $1.5 \leq |\eta| \leq 3.2$, and forward calorimeters cover $3.1 \leq |\eta| \leq 4.9$.

2.1.3.1 Electromagnetic Calorimeters

The ElectroMagnetic calorimeter (EM) is a type of calorimeter used to sample liquid argon. It employs lead plates as absorbers and Kapton electrodes in an accordion shape with ϕ symmetry; this arrangement is highly ATLAS-like. The material in front of the calorimeter is about $2.3 X_0$ at $\eta = 0$ and grows with pseudo speed owing to particle angle of incidence. In the $\eta < 1.8$ range, where the most accurate measurements are required, a presampling calorimeter is placed in front of the electromagnetic calorimeter to compensate for energy loss in the upstream material. The pre-sampling calorimeter is augmented by a scintillator plate put into the crack between the calorimeter parts of the cylinder and end cap at the transition area when the material thickness exceeds $7 X_0$ in front of the calorimeter. The cylinder section is made up of two identical half-cylinders, denoted by the letter “a”. There is a 6 mm gap at $z = 0$, and the end cap calorimeters are made up of two coaxial wheels

($1.375 < |\eta| < 2.5$, $2.5 < |\eta| < 3.2$). The EM calorimeter has a total thickness of $24 X_0$ in the barrel and $26 X_0$ in the end caps [30].

2.1.3.2 Hadronic Calorimeters

The ATLAS hadronic calorimeter has a large enough coverage of the area $|\eta| < 4.9$ to offer high resolution of the missing transverse energy. The large angle is made feasible by three major distinctions: forward calorimeter, end cap calorimeter, and tile calorimeter. The hadronic calorimeter is the outer layer of the ATLAS calorimeter, therefore it must be as absorbent as possible to limit muon spectrometer hits; the radiation length necessary for this is around 10 radiation length. The overall diameter of the hadronic calorimeter is approximately 9λ , with 7.4λ instrumented and 1.8λ instrumented in the electromagnetic calorimeter. However, the total amount of material traversed is 11λ .

- The LAr FCAL covers the area closest to the beam pipe, $3.2 < |\eta| < 4.9$, the calorimeter should deliver at least 9 material in as little space as possible; the fact that it is moved back from the electromagnetic end cap to reduce albedo further reduces this space; the solution is a high density material. The FCAL was built as three metal matrices on either side of the detector, one filled with copper rods and tubes and the other two with tungsten, the active material (liquid argon). When the FCAL was created, tungsten was still a relatively new material.
- The LAr Hadronic End-Cap (HEC) calorimeter measures temperatures ranging from $1.5 < |\eta| < 3.2$. It is made up of two copper wheels, each having an outer radius of 2.03 m and double the thickness of the inner one. Each wheel is split into 32 modules. In the gap, there are three parallel electrodes, one for reading and two for high-voltage carriers; the gap is then filled with liquid argon as the active material.

- The Tile Calorimeter (TileCAL) will be covered in the next section.

2.1.4 The Muon Spectrometer

When muons traverse the enormous air-core toroidal magnets at the outer radius of the ATLAS detector, high precision tracking chambers detect them. The field produced by the barrel toroid ($|\eta| < 1$), end-cap toroids ($1.4 < |\eta| < 2.5$), or a superposition of the two ($1 < \eta < 1.4$) is virtually everywhere perpendicular to the particle direction and bends the particles, enabling momentum and energy measurements. Monitored Drift Tubes (MDTs) can measure eta over a wide range, but at high pseudorapidities and at the contact point, Cathode Strip Chambers (CSCs) with better granularity are favoured due to the greater number of tracks in those regions. The geometric configuration is the same as for the other detectors, with concentric cylinders in the barrel and parallel plates in the end-caps; precision measurements are made along the z direction in the barrel and the R direction in the transition and end-cap region, but measuring only one direction is reductive for ATLAS purposes; the trigger system supplements this measurement with a second orthogonal to that of the high precision chambers. In actuality, the trigger system is made up of Resistive Plate Chambers (RPCs) in the barrel and Thin Gap Chambers (TGCs) in the end-caps, which can monitor energy in one direction, recognize bunch crossing, and offer a trigger with a well-defined pT cut-off in moderate fields. The backdrop that has an impact on the muon spectrometer

2.2 The Tile Calorimeter

The TileCAL [6] is an uncompensated sample calorimeter composed of steel and scintillating tiles in a 4 to 1 absorber/active material ratio. Its primary responsibility is to locate rays and quantify their energy and direction, as well as to contribute to

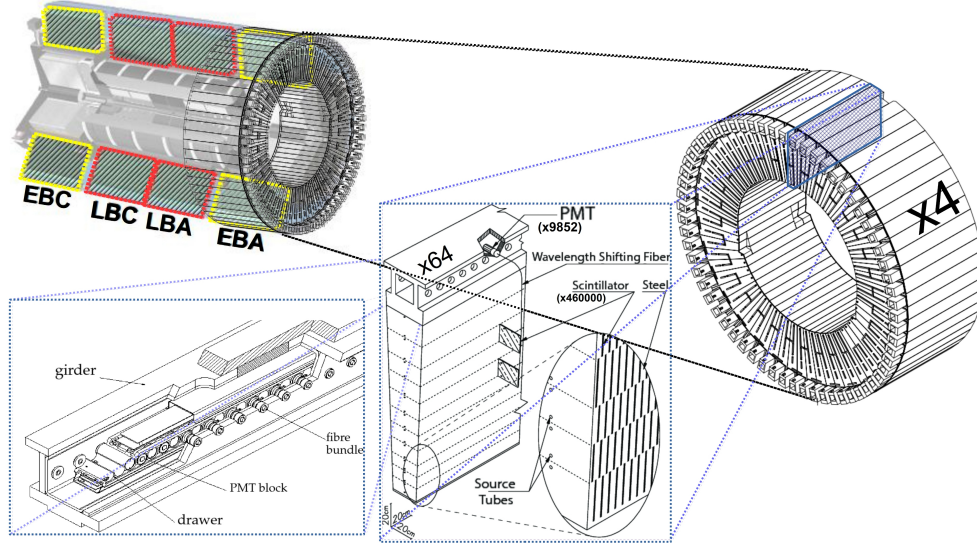


Figure 2.4: The ATLAS Hadron Calorimeter. It is split into three sections: a barrel in the center and two elongated barrels on either side. Each portion is made up of 64 separate azimuthal modules [6].

accurate E_T^{miss} measurement. This is not a straightforward feat at the LHC, because the huge energy center of gravity (14 TeV) necessitates good performance throughout an extraordinarily wide dynamic range, ranging from a few GeV deposited by crossing muons to several TeV per cell owing to jets.

The TileCAL absorbs a considerable portion of the radiation created by the high contact rate, which is in the order of magnitude of 10^9 interactions per second per collision point. As a result, the materials utilized and the FE electronics must be radiation-tolerant to the projected dosage in order for the experiment to operate during its full life cycle.

The calorimeter also improves the particle recognition capabilities of the electromagnetic calorimeter. The segmentation of $\delta\eta \times \delta\phi = 0.1 \times 0.1$ allows for an efficient hadron leakage current cut, which is essential for electron and photon identification. The granularity of the calorimeter also allows for the reduction of effects due to

non-compensation and the restoration of linearity of the energy response to hadron showers to a level of 1-2% using weighting techniques.

Each TileCal disc (Figure 2.4) is made up of alternating layers of low carbon steel absorber plates and scintillating plastic tiles. Calorimeter cells are formed by combining groups of scintillating tiles within each disc. Figure 2.5 depicts the TileCAL's Tiefen-Ann segmentation. Particle showers are created when hadronic particles moving through TileCAL hit with the absorber plates. Showers' charged particles stimulate the plastic scintillator tiles, causing them to produce photons. Neutral pions decay into photon pairs, resulting in electromagnetic showers that may be observed by scintillators. Wavelength shifting fibers situated on each side of each scintillation plate read out the light emitted in the calorimeter cells. Each cell's Wave-Length Shifting (WLS) fibers are bundled and read by two independent Photo Multiplier Tubes (PMTs) in the TileCAL FE electronics. The twofold readout architecture boosts system redundancy and improves the smoothness of the scintillating tiles' response. TileCAL has a total of 5,182 calorimeter cells that are read by 9,852 PMTs.

The detector's FE electronics are housed in special mechanical drawers (super-drawers) that slot into the outside area of each TileCAL disk. The light collected by the PMTs is transformed into analogue electrical signals, which are then transmitted to the FE board, where they are amplified and shaped before being digitized with a 10-bit Analogue-To-Digital Converters (ADC) at 40 MHz. Various low gain signals from multiple FE boards are delivered to an adder board, which averages the inputs and transmits them to the ATLAS Trigger and Data AcQquisition System (TDAQ) for Level 1 muon and Hadron triggers. The digitized samples are placed in pipelined memory buffers, resulting in a 25 microsecond delay, while the TDAQ processes the stage 1 trigger following the accepted sample. This set of samples is prepared and

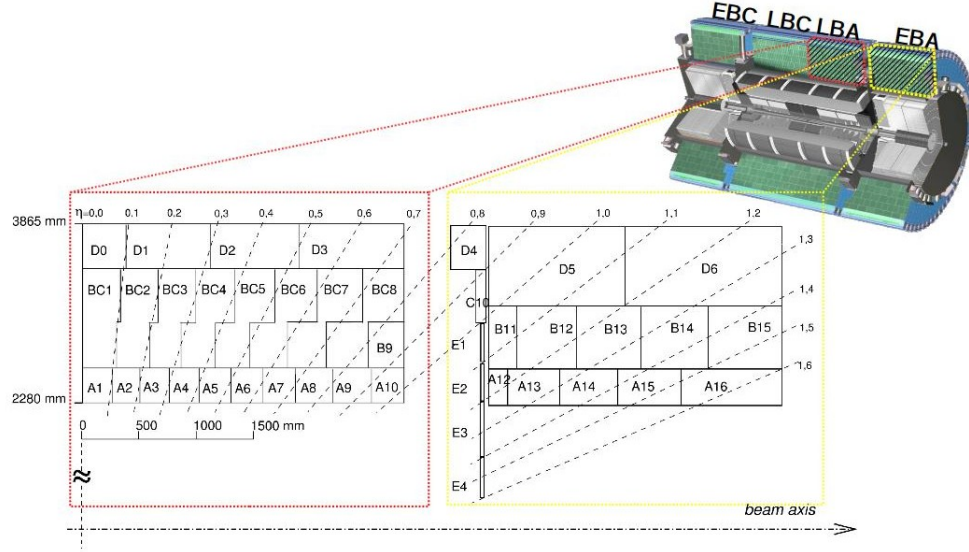


Figure 2.5: TileCAL slice depth and eta segmentation for half of a long barrel (left) and an extended barrel (right). Calorimeter cells are spaced uniformly around the contact site [6].

transmitted to the back-end electronics' Read-Out Driver (ROD) for further processing. Signals that are not selected from level 1 may be overridden by freshly received data. The ROD is the connector between TileCAL's front and back-end electronics [17]. The ROD is responsible for a variety of tasks, including initial on-line energy reconstruction of PMT pulses, calibration adjustments, integrating various FE sources into a single data link, and formatting data and metadata for DAQ.

2.3 Trigger and Data Acquisition

The ATLAS detector is capable of detecting up to a billion proton-proton collisions per second but due to technical limitations it is simply not possible to read and keep all the generated data. The LHC operates at a packet crossover frequency of 40 MHz translating to a raw data rate of Peta bytes per second into the ATLAS detector. Interestingly, only a tiny percentage of these collisions have “interesting” features that might lead to new physics discoveries. As a result of the trigger selection process the data rate is significantly reduced. The ATLAS test employs a multi-layer

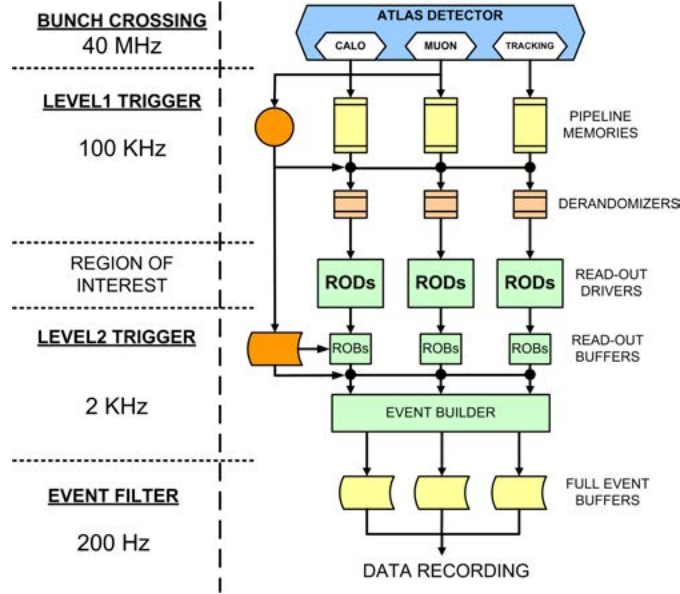


Figure 2.6: ATLAS trigger and data acquisition system [11].

processing network to lower the data rate from 40 MHz to 1.5 kHz, resulting in a more manageable data rate. The DAQ routes the data collected by the detectors trigger system to storage.

ATLAS's current trigger system consists of three stages of event selection (Level 1, Level 2, and the Event Filter (EF)) [3]. The Level 1 trigger mechanism is built on customer-specific hardware designed specifically for the ATLAS experiment. The Level 2 trigger and EF combine to produce the High Level Trigger (HLT), which is mostly made up of Commercially accessible Off-The-Shelf (COTS) components. Figure 2.6 is a TDAQ system which conveys data from the detector front-end to the mass-storage, reducing the event rate from the LHC nominal collision rate of 40 MHz down to 200 Hz. In addition to the event display, the DAQ system allows you to configure, manage, and monitor the ATLAS detector. The Detector Control System (DCS) is used to handle detector services such as power supplies and gas cooling systems.

2.3.1 Level 1 Trigger

The Level 1 trigger [28] was designed to look for the traces of electrons, photons, jets, muons with high- p_T values and τ -leptons that decay into hadrons. Events with a high E_T^{miss} and transverse total energy are also chosen for [3]. For high p_T muons, the Level 1 decision-making procedure is based on decreased granularity data provided by the RPC and TGC. Calorimeter data for jets, electromagnetic clusters, τ -leptons, E_T^{miss} , and big E_T were used for level 1 selection. The level 1 trigger has the ability to lower the event rate from 40 MHz to a more manageable 100 kHz. Trigger decisions at level 1 must be performed within a $2.5\,\mu s$ interval and received by the readout electronics. During this time event data will be stored in pipeline memory on the FE electronics pending trigger selection.

2.3.2 Level 2 Trigger

The Level 2 trigger [3] refines the event options further by examining the Regions of Interest (ROI). RoIs are locations inside the detector that the Level 1 trigger detects as potential trigger objects within an event. The data for these RoIs is evaluated at the granular and precision levels. While the Level 2 trigger is processing RoIs, they are stored in Read-Out Buffers (ROBs) in the EF Farm. The Level 2 trigger algorithm uses RoI information such as energy, coordinates, and signature type to lower the event rate below 3.5 kHz in an average processing time of 40 ms.

2.3.3 Event Filter

The EF is in charge of the final stage of trigger selection [3]. The EF is responsible for processing the data of entire events produced in the Event Builder system. While the EF is processing events, they are stored in the complete event buffers. Selected events are transferred to the CERN data center, where they are permanently archived

and utilized for physical analyses afterwards. The EF was initially planned to lower the event output for Run 1 (2010-2012) to around 200 Hz, however it could only do so at 800 Hz, while the recording rate for Run 2 was 1 kHz.

2.4 ATLAS TileCAL phase II Upgrades for the HL-LHC

Radiation creates new challenges for TileCAL's electronics. The upgraded TileCAL's electronic components must survive up to a 1000 Gy ionizing dose, a dense fluence of 1 MeV neutrons of $\sim 2 \times 10^{13} n_{eq}/cm^2$, and a 20 MeV hadron flux of $\sim 10^{12} hadrons/cm^2$, including safety factors. Due to the new TDAQ design, as well as the much higher radiation values, TileCAL's readout electronics have to be completely replaced and redeveloped. The most exposed 10% of PMTs will be replaced by new PMTs, with the remaining optics remaining unchanged. A revision of the distribution and control systems for low and high voltage is necessary to mitigate rising radiation levels.

2.4.1 Mechanics

Located at $0.8 < |\eta| < 1.7$ and $|\eta| < 0.8$, the three cylinders of TileCAL form an azimuthal pattern around the beam axis. Each segment contains 64 wedges or modules that are arranged in a diagonal pattern along the axis. Two super-drawers contain 45 PMTs and components required to read an LB module. These super-drawers are located on the calorimeter's outskirts. 32 PMTs are needed to read an Extended Barrel (EB) module, and 32 PMTs are required to read an EB module. For redundancy, there are 9852 PMTs in total, and virtually all calorimeter cells are read by two PMTs.

Figure 2.7 (Left) shows how the super drawers are constructed with mechanically

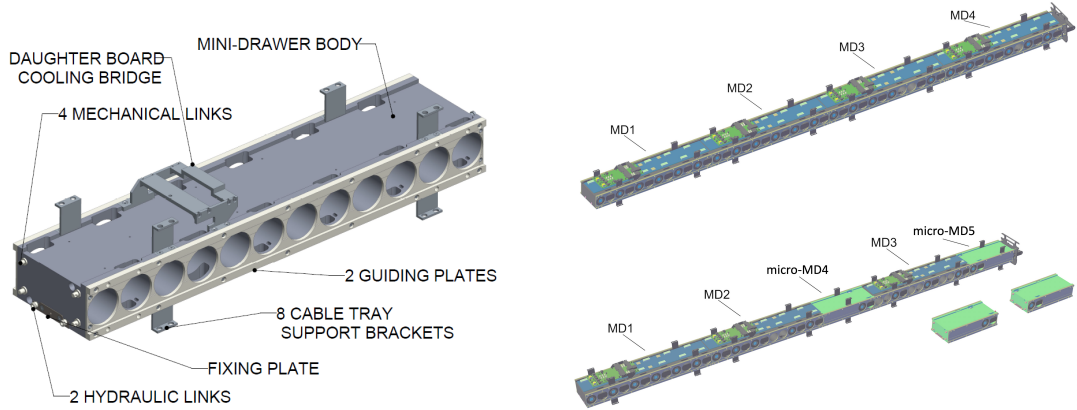


Figure 2.7: Left: Design of the Mini-Drawer, with the Daughter Board placed for electronic readout. Right: Arrangement of the MDs in long and extended barrel modules (top and bottom) [22]

connected Micro Drawers (MD) which contain the PMTs as well as the detector's electronics. Each MD contains 12 PMTs and is electrically independent from any other MD. Figure 2.7 (Right) illustrates the difference between the LB- and EB-super-drawers. An LB superdrawer contains four MDs, while an EB superdrawer only requires three. In the EB superdrawer, two MD keep PMTs in their proper place. The MDs contain no digital electronics. In this modular architecture, aluminium and high-density polyethylene are used to make MDs. A cooling bridge and a water cooling channel inside the metal frame maintain cool temperatures within the electronics.

The TileCAL readout electronics in Figure 2.8 are separated into on-detector electronics, which must be exposed to high levels of radiation, and off-detector electronics, which are housed in subterranean counting chambers around 100 meters away from the detector. The electronics outside the detector do not require radiation hardness.

2.4.2 PMT blocks

As a result of aging, 10% of PMTs in PMT blocks will be replaced, with their Front-End electroNICS (FENICS) boards, which are used to improve PMT's analogue

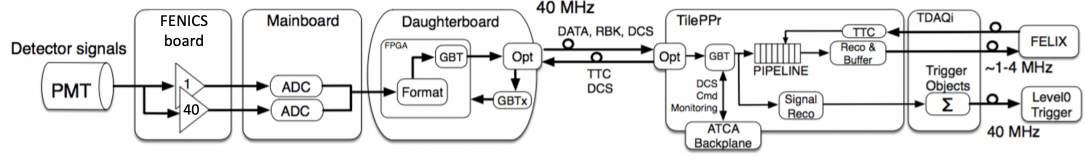


Figure 2.8: Left to right with the on-detector electronics, which consists of PMTs, FENICS, a main board and daughter board, as well as the off-detector electronics in the right part of the picture, which consists of the tile pre-processor and TDAQ interface [11].

signals by amplifying and moulding them. For calorimeter calibration with a ^{137}Cs source and luminosity measurement [23], the “slow integrator readout” integrates PMT current, and for physics, the “rapid readout” runs in two distinct gains to span a dynamic range of 200 fC (MiPs) up to 1000 pC. FENICS will enhance accuracy and performance in terms of noise. A thorough validation has been conducted for the radiation levels expected at the HL-LHC and prototypes are now in pre-production. The PMTs, FENICS, and High Voltage (HV) dividers are housed inside the metal cylinders. Section 2.4.6 discusses the HV-dividers.

2.4.3 Main Boards

A single main-board digitizes data from up to 12 PMTs per MD. The rapid readout employs 24, 12-bit ADCs operating at 40 Msp/s, while the integrator readout uses 12, 16-bit successive approximation register based ADCs. The main board sends data to the daughter board and provides digital control of the FENICS, such as configuring it for calibration or physics. The main-board has been thoroughly validated for the anticipated radiation environment at the HL-LHC and is in pre-production. Both the main board and the daughter board have been designed to have two electrically separate portions for robustness considerations. Because each calorimeter cell is read by two PMTs, the two PMTs are linked to the two halves.

2.4.4 Daughter Boards

Each MD includes a daughter-board that communicates high-speed (4.8-9.6 Gbit/s) data with detector-independent electronics. This boards sends accurate data, slow control data, and monitors data from the detector electronics. Each daughter-board contains two Kintex Ultrascale Field-Programmable Gate Array (FPGA)s which receive LHC clock signals and pass them to the detector electronics [67]. On previous design iterations, Kintex Ultrascale Plus caused single-event latch-ups on the HL-LHC hadronic. Kintex Ultrascale was used on the latest design iteration and exhibited no latch-up on an FPGA dual sample. It is crucial to properly test the final prototype in the radiation field [68].

2.4.5 PreProcessor and TDAQi

Data from the subpanel is received by TileCAL PreProcessor, which applies a digital filter to determine how many pulses to count and how long to store the pulses until ATLAS is turned on. After a trigger accepts signal is received [8], data is sent to the Front End LINK eXchange (FELIX) system. The preprocessing system consists of an Advanced Telecommunications Computing Architecture (ATCA) carrier board and four Compact Processing Modules (CPM), which are capable of processing data from two TileCAL modules. The CPM is a Double Mid Size Advanced Mezzanine Card with a Kintex Ultrascale FPGA. Monitoring data is collected from the data stream using a specific system chip and transmitted over Ethernet to the ATLAS detector control system. The TDAQ Interface (TDAQi) is an add-on module that calculates triggers such as B using cell energy. A completely adjusted total cell energy from the calorimeter to move to the ATLAS trigger's head level. Carrier dashboards and CPMs have been widely prototyped and are being actively implemented in large-scale demos (see section 2.4.8). The high-speed connection with the prototype back module was successfully validated in the lab.

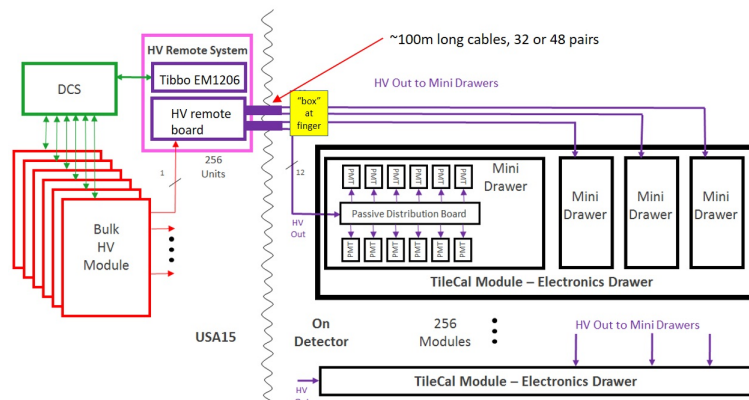


Figure 2.9: The TileCAL HL-LHC upgrade for the high voltage system design [22].

2.4.6 High Voltage Distribution and Regulation

The High Voltage (HV) delivered to the 8-dynode PMTs must be steady within 0.5 V in the 600-900 V range to obtain a 1% accuracy on the energy scale in TileCAL. To ensure linearity, active dividers must deliver better than 1% linearity due to the high PMT current at high brightness. In the most exposed cells, this current exceeds 40 A. To ensure linearity, current dividers use transistor dividers. The active divider PMT system's linearity was successfully tested in an environment meant to imitate physical pulses as well as continuous pile-up activity. After being rigorously validated in irradiation testing, the active splitters have just finished pre-production. A HV control from beneath the counting rooms is carried out using special supply boards and remote control boards. Each control board manages a TileCAL module, see Figure 2.9 for more details. The prototypes of full-size panels have been tested and have been found to satisfy HV stability specifications. The supply boards are now being tested with the control boards in full-scale prototypes. Along with the control boards, the power boards are currently being tested in full-size prototypes. Long connections from the counting room to each module, as well as passive splitters, are other passive components. Prototypes of passive distributors have been successfully constructed and tested in automobiles. The cables are in a difficult location

due to the limited area available and the rigorous material safety criteria required by ATLAS and CERN.

2.4.7 Low voltage distribution

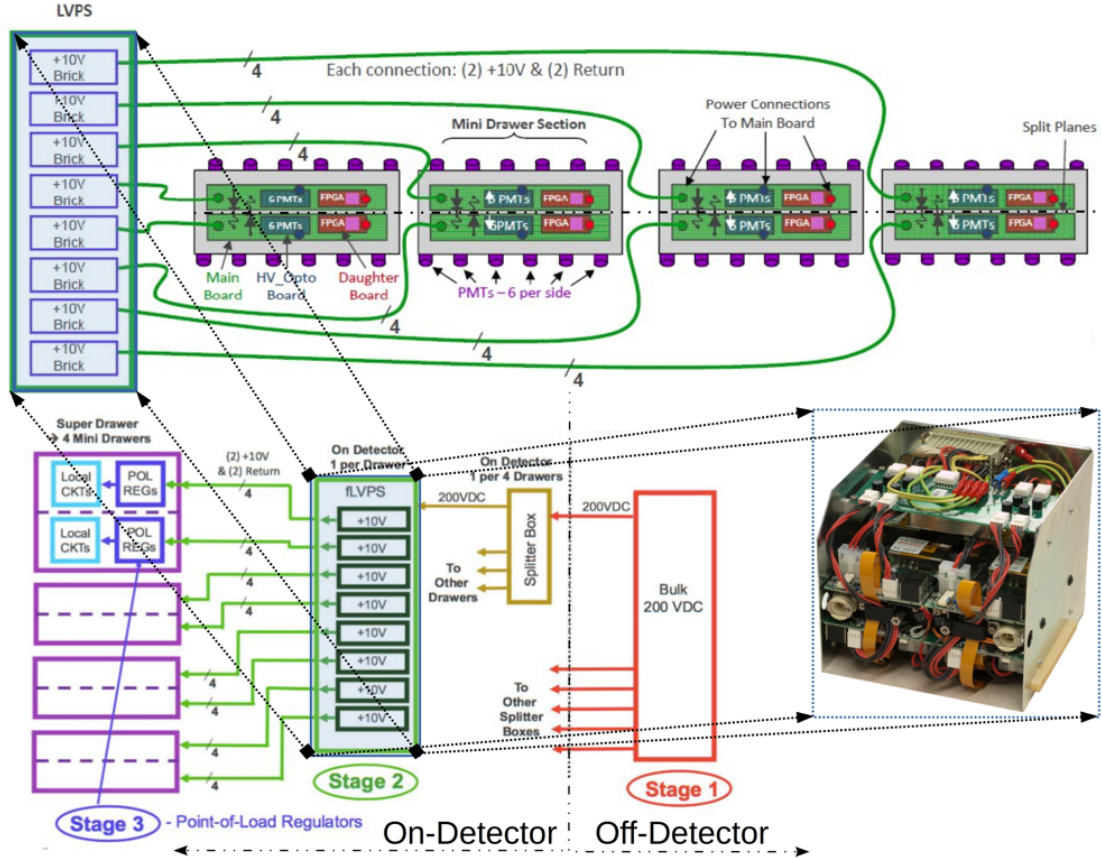


Figure 2.10: TileCAL HL-LHC update power distribution system design. This shows how the power is distributed from the off-detector to the on-detector circuitry and the location of the LV box which houses the transformer-coupled buck converter which converts 200 V DC to 10 V DC. Third-stage upgrades include POI regulators [22].

The Tile Calorimeter’s Low Voltage Power Supply (LVPS) technology powers all of the TileCAL’s FE electronics. In contrast to the present two-tiered Low Voltage (LV) distribution system, the upgraded LV distribution system has three levels as illustrated in Figure 2.10. The LVPS is the TileCAL component most exposed to radiation due to its position in the detector, and many radiation test campaigns were

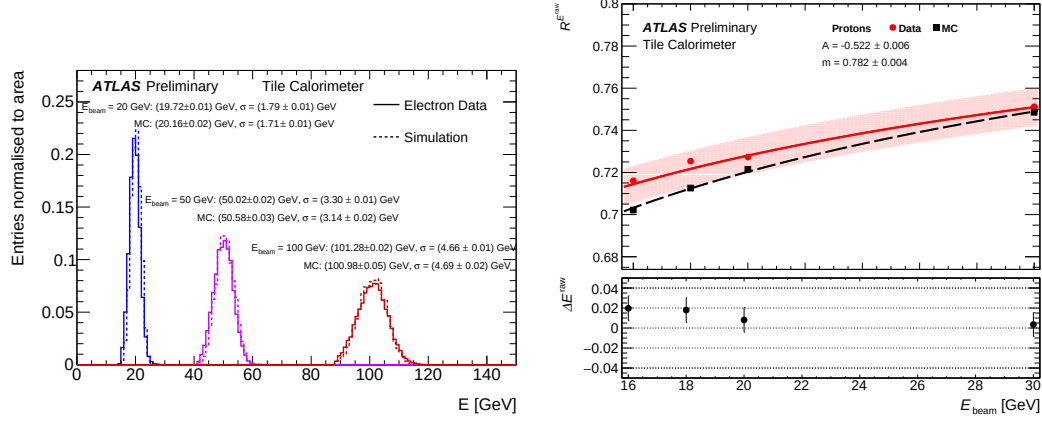


Figure 2.11: Left: Energy deposited in TileCAL demonstrator by electron beams. Right: Energy response, $R^{<E^{raw}>} = \frac{\langle E^{raw} \rangle}{E_{beam}}$ [80]. After calibration with charge injection and a ^{137}Cs source, the shower's energy, E^{raw} , was obtained by summing the TileCAL cells with signals greater than two times the electronic noise [81]. Copyright 2020 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license.

done to identify the ideal material. A circuit supply situated in the USA15 cavity provides 200 V input voltage to the LVPS transformer-coupled buck converters, which are then converted to 10 V by **P**oint-**O**f-**L**oad (POL) (POL) regulators in order to power the FE electronic equipment. The devices are monitored by an Embedded Local Monitoring Board (ELMB) [59] housed inside the LV box, and it is developed with increased reliability, lower noise, and radiation resistance. Individual MDs may be controlled by the control system, and each main-board and daughter-board half is supplied by a separate converter for further resilience. The ELMB motherboard also supplies power to the ELMB2. The ELMB motherboard has been rebuilt to be compatible with the new LVPS coupled transformer control technique. The LV system was fully prototyped and tested using both the on and off detector components in the vertical slice test. The LVPS will be covered in further detail in the following chapters.

2.4.8 Results of the Testbeam and Demonstrator

CERN conducted five test beam campaigns with the TileCAL upgrade demonstrator equipped with HL-LHC electronics. Since the test beam, the majority of hardware advances have been focused on replacing particular components to assure radiation hardness. Figure 2.11 (left) depicts the TileCAL reaction to electron beams, allowing the pC-to-GeV scale to be measured and linearity checked. Figure 2.11 (right) illustrates the response to hadrons as a function of beam energy in Geant-4 data and simulations [5]. The demonstrator was deployed in ATLAS in July 2019, and its reading was successfully integrated and validated across the ATLAS data flow.

Chapter 3

The Low Voltage Power Supply System

3.1 Introduction

TileCAL's aim towards integrated electronics is paramount. It's also important to note that a malfunction in a module's electronic components can result in a significant loss of information from the module, which can result in a significant loss of information for the entire detector. It's exciting to see how the electronics are powered and how energy molecules can be built to perform dependably within the



Figure 3.1: LVPS box assembled.

detecting environment using this assumption.

The first is in an underground hall reserved for ATLAS services and electronics (USA15 or Underground Service ATLAS cavern), where the high power supplies (HPS1) convert 230 V AC to 200 V DC. From there, power is distributed first to the distribution boxes (one per four drawers), then to the 256 LVPS boxes in the ATLAS cavern [31].

Each LVPS box shown in Figure 3.1, serves one drawer and is made up of eight modules, transformer-coupled buck converters referred to as Bricks, that are managed by an ELMB, which also acts as a control and monitoring signal interface with the outside world. The second conversion stage occurs in the buck coupled transformers, where 200 V DC is transformed to the low voltage DC levels required by the FE electronics, digitizers, and motherboard, as well as the HV distribution system that powers the PMTs. A scheme arrangement of the power distribution system is shown in Figure 2.10.

The detector environment, as discussed in earlier chapters, imposes significant limits on the LVPS boxes. Working within TileCAL entails dealing with high amounts of radiation, being submerged in the magnetic field of the BT, and having limited space. Despite these limitations, LVPS are built with just commercially available components.

Drake et al. [31], investigated whether the Bricks (V6.5.4) failed spontaneously because to an increase in detector luminosity. The current version of the Bricks (V7.5) would exhibit a similar issue with a five - fold increase in luminance.. The five-fold rise in luminosity poses a series of issues for the detector's circuitry. This incident

affects the data obtained from the module for a few minutes, resulting in significant data loss for the calorimeter and, as a result, the ATLAS detector. With the LHC's rising luminosity, there was a need for a solution; a redesign work that was already ongoing at the time focused on this. Even though the Bricks were still functional but the glaring issues necessitated for the upgrades. The version 7 Bricks were produced using the V7.5.0 Bricks installed in TileCAL to fix this issue and make design modifications influenced by experiences with the V6.5.4 Bricks. The V7.5.0 Bricks will be used in TileCAL until the TileCAL Phase II upgrade, after which the V8 Bricks will be used.

A Brick in Figure 3.2 is a transformer-coupled buck converter, it functions to step down 200 V DC to 10 V DC, which is then distributed to the FE electronics [22]. With its twin transistor forward converter [60]. The overall design of the LVPS Bricks will be discussed in this chapter, beginning with the detector's environmental restrictions and how these informed the design. Then we will go through how the new version of the Bricks has improved. The production phases will be the focus of this chapter, particularly the checkout technique used at the University of the Witwatersrand and iThemba LABS.

3.2 Overview of the Brick design

The HL-LHC requires the upgraded LVPS Brick's higher radiation hardness requirements. The installation of a three-stage system for power distribution to the FE electronics is one of the most significant enhancements to the distribution system. The tri-state functionality is also being introduced [22]. The present LVPS Bricks

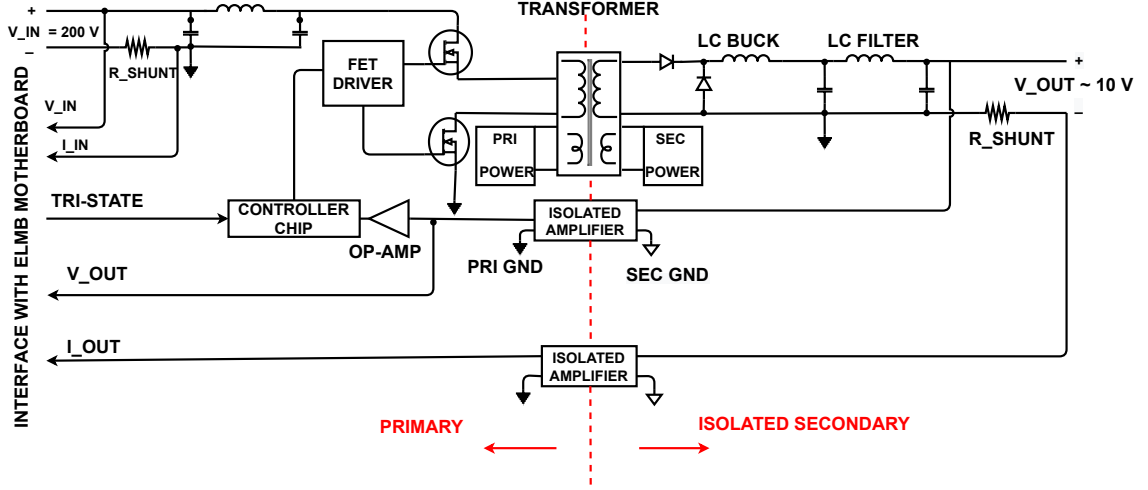


Figure 3.2: Functional block diagram of an LVPS Brick [31].

(V7.5.0) are a highly developed bespoke design that has undergone several modifications over the last few years. All modified LVPS Bricks have the same design criteria, which makes final production testing easier. LVPS Brick requirements are stricter, including strong radiation compatibility; small packaging to match the available area for LVPS; operation in a magnetic field; efficiency better than 80% nominal; output power 230 W, 2.3 A at rated load of 10 V. Figure 3.2 depicts the circuit's LVPS block diagram. The LT1681 driver chip [29], a direct-drive controller, lies at the heart of the design. A two-transistor synchronous relay capable of generating an inverter pulse at 300 kHz with an output duty cycle of 45%. A feedback circuit controls the pulse width based on the device's output voltage values.

This input helps us to verify that the rated voltages and currents are maintained indefinitely. The LT1681 signal is sent to the Field Effect Transistor (FET) drivers, IR2110 [41]. These are transistor drivers with enough current and voltage drive to power the high side. Switch-mode power supplies are devices that can generate DC signals with low voltages relative to the input signal while dissipating relatively little power. When the output clock is high, both the high-side and low-side transistors switch on and conduct simultaneously, and both are off when the clock is low. When

the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) conduct, current travels through the transformer's main windings, transferring energy to the secondary windings. On the secondary side of the transformer, a step-down converter turns the signal into a constant voltage for the output. For noise filtering, the outputs should preferably include an extra combination of Inductors (I) and Capacitors (C), IC stage. The optocouplers give voltage feedback to adjust the output voltage. Voltage feedback is provided by optocouplers to regulate the output voltage. They convert the electrical signal into a digital signal at the input stage and send this signal to the output through the pulsed light signal, where it is converted back to an electrical signal.

Besides the two shunt resistors to monitor the output current, the design contains an optocoupler to provide back the voltage. This Brick incorporates three types of safety circuits, controlled by the reference voltage coming from the central controller in the LVPS box and the ELMB shown in Figure 3.3. During operating conditions where over voltage and over current occur, Over Voltage Protection (OVP) and Over Current Protection (OCP) are integrated into the Brick's primary side. The third feature, over-temperature protection, monitors the low-side transistor's temperature on the main side.

In addition to this circuit, the LT1681 design incorporates a tri-state connection that will control the upgrading Brick through a single Brick on/off switch. With the Brick's starting voltage level set to 15V DC and the high impedance signal driving the LM9074M regulator on the LVPS Brick, the power supply drives the tri-state control lines. Disabling the LM9074M regulator on the LVPS device by connecting the disable state signal to ground will shut down the device [44].

3.3 Location Limitations

On the outside edge of the drawers, the LV boxes feature a special shield that decreases the amount of radiation received as well as the influence of magnetic fields. However, the shield does not provide complete protection. As a result, there is a residual magnetic field of about 0.02 T, which impacts components such as transformers and ferrite chokes. As a result of ATLAS Radiation Estimation Task Force calculations using LHC 4 ab^{-1} radiation simulations, the highest dose observed is 80 Gy of Total Ionizing Dose (TID) radiation, $3.5 \times 10^{10} n/cm^2$ of Non-Ionizing Energy Loss NIEL (NIEL), and $6.3 \times 10^{11} p/cm^2$ of Single Event Effects (SEE) [26].

Safety parameters must be included for the simulated figures, according to the ATLAS radiation guideline. TID's safety factors for simulation uncertainty are 1.5, lot-to-lot variation is 4, and low dose rate effects are 5. The safety factor from low dose rate effects can be ignored if the panels can be annealed at the highest feasible temperature for one week following irradiation. Without annealing, the radiation tolerance threshold for TID equals 2400 Gy. Because the TileCAL LV Bricks' technology is not intended to withstand 2400 Gy, the chosen method of radiation validation necessitates annealing, allowing a TID of 480 Gy to be evaluated. For NIEL and SEE, the safety factors are 2 for simulation uncertainty and 4 for lot-to-lot variance. As a result, NIEL's radiation tolerance limits are $4.8 \times 10^{12} n/cm^2$ and SEE is $2.5 \times 10^{12} p/cm^2$.

Radiation-resistant components were chosen to be able to tolerate this radiation exposure for long periods; large-scale testing was done to determine the best ones [40]. The metal barrier protects the Bricks, but it encloses them, increasing the difficulty of dissipating heat. Due to small dimensions of the Brick, heat is created in a very limited area; under this conditions, a good cooling system is essential. Through the center of the LV box is a water cooled plate, which is connected to each Brick via

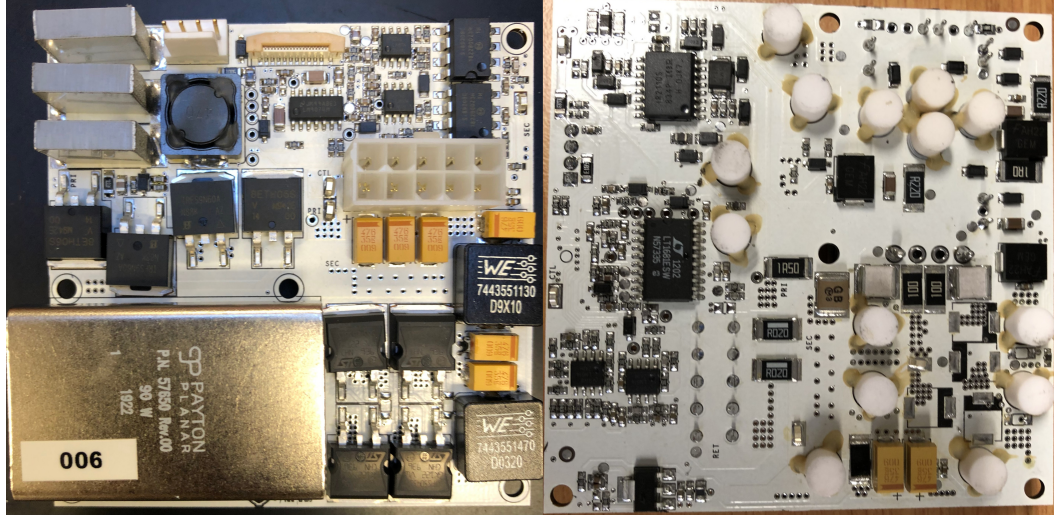


Figure 3.3: Both sides of The LVPS Brick V8.4.2 prototype showing both sides.

ceramic posts located strategically across its bottom.

Because of these circumstances, it was chosen to employ switching power supplies rather than linear power supplies, because the latter would not operate effectively in the magnetic field and would have bigger dimensions that would not fit into the drawer's limited area. Furthermore, switching supplies are more efficient, resulting in reduced heat loss. Maintenance of the LVPS is challenging owing to stringent space constraints and minimal access to the detector, therefore operating dependability and stability are strict requirements. External trimming of the output voltage has been established through the use of a reference voltage to handle fluctuations in output voltage owing to natural deterioration.

3.4 Improvements on the current prototype

The improvements in the LVPS Brick includes the following:

- Thermal management - In the new design, a ceramic posts containing Aluminum Oxide provides thermal coupling. While the progress has been tremen-

dous, there are two areas where the LT1681 converter and FET driver position remain extremely hot during operation. As a result, these chips are connected to the plate on the bottom using the Bergquist gap pad to further minimize the temperature. Following that, these chips are connected to the board on the bottom using the Bergquist gap pad to further lower the temperature on the two crucial components responsible for the heat build-up in the power supply.

- Real-time monitoring - The LVPS Brick includes remote control capabilities and can measure and provide six analogue signals, including input/output voltage, input/output current, and two temperature measurements from two places inside the device detected by thermistors. Monitoring and controlling the construction pieces may be done both manually and automatically using custom software developed in LabVIEW.
- Noise - Additional filtering has been incorporated because some regions of the output stage, optoisolator power pins, and inputs still exhibit noise. Differential approaches have also been used to design track tracks with limited regions, tight loops, and feedback signals. The OCP and OVP are completely differentiated down to the last comparator in the most recent version of the Bricks. The changes increased the noise intensity by a factor of five.

The use of a radiation resistant readout electronics design to support the increased trigger rate (> 1 MHz) and larger event buffer ($> 10 \mu s$) is one of the significant Tile-CAL upgrades associated with the FE electronics. This involves removing the detectors' buffers and pipelines and reading at 40 MHz. Increase reliability by using redundancy to reduce the impact of component failures. This includes changing from a 2-stage to a 3-stage power distribution system, which is discussed in Section 2.4.7 and Figure 2.10. As part of the upgrades, the new LVPS box will use a uniform 10 V voltage to power the circuitry of the FE electronics, simplifying maintenance in the

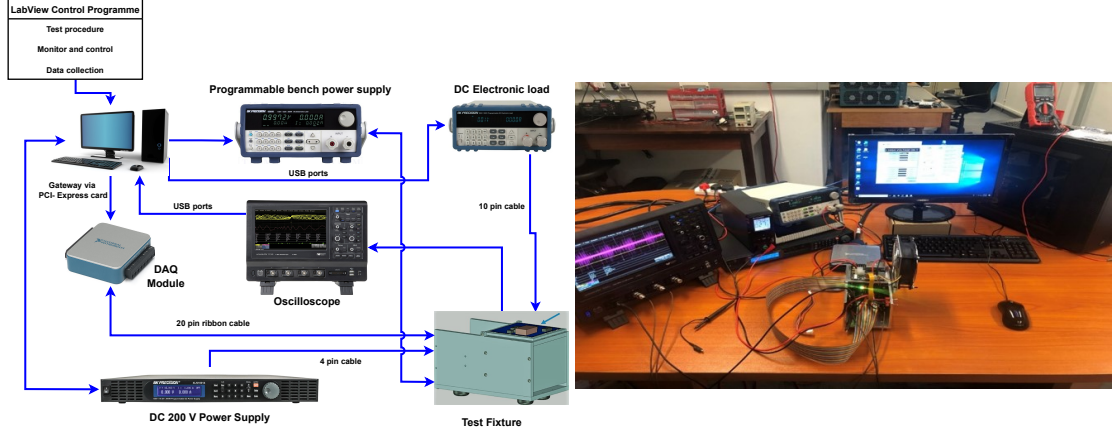


Figure 3.4: The test-bench used to do initial testings on the Brick to check if it passes the required specifications. Left: Functional diagram of the test bench. Right: Actual test bench setup.

event of a failure.

3.5 Vetting process on the LVPS Bricks

3.5.1 Quality Assurances

The issue of reliability is paramount when dealing with the LVPS Bricks due to inaccessibility of them once they are installed in the Inner-barrel of the ATLAS detector. Access to the Bricks is just once in a year, so if they experience failure (inability to provide power to the FE-electronics leading to replacements needed). Due to manufacturing processes the bricks can have different defects, which would require a Quality Assurance (QA) testing for each individual brick. The QA procedure involves a series of steps namely, an automated visual inspection, x-ray scanning, initial testing, burn-in and final testing [54].

Once the manufacturing is complete, a Brick is received by the assembly house, and it is tagged with a unique identification serial number which is essential for monitor-

ing throughout quality assurance testing and maintenance requirements once at the detector, there is a dedicated database for this monitoring purposes. The Bricks are next subjected to an X-ray scan to detect any possible solder outgassing that may have occurred during the reflow process between particular components, such as the primary-side switching MOSFETs, and the ceramic post to which they are linked. The motive for identifying these voids is their potential to decrease thermal conductivity at the thermal contact between the electronic component tab and the ceramic post. The same test apparatus and procedure are used for initial and final testing. They are so named because of their appearance before and after burn-in process [61]. Ithemba LABS and Wits University will have a reception area where the Bricks will be housed and ready for pickup. There will be a over 1000 of Bricks that will require extensive checkout process. These operations are all carried out at Ithemba LABS and Wits University.

3.5.1.1 Description of the Brick checkout test-bench

The test bench was created to assess the functioning of the LVPS Bricks once they were manufactured. Test bench operators can run independent parametric and functional tests (input current, charge pump operation, and feedback loop parameters) and create results that are stored in a database for future reference. An LVPS device and a power control interface board are connected to the test bench through a test fixture. The series of automated tests on an LVPS Brick are run using LabVIEW control software [57]. Running through the tests takes only a few minutes, and it ensures approximately 80% functionality of the system. A National Instruments Data Acquisition (DAQ) module[58] serves as the key component of the system for reading and controlling the control software. The DAQ module interfaces with the computer via a peripheral component interconnect express card [42], which connects the PC and the DAQ module. Aside from the data gathering module, the test bench includes sev-

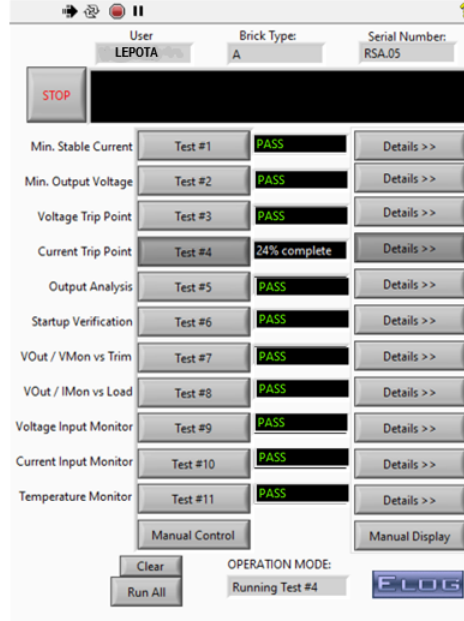


Figure 3.5: Left: A test panel for running a multitude of tests to confirm the LVPS Brick’s functioning. Right: A manual control panel that is used to monitor the test panel [62].

eral other instruments, including an electronic load meter with programmable load to check the updated devices’ performance. A configurable power supply is utilized to deliver +5 V to the interface card’s peripheral circuitry, including temperature sensor biasing and tri-state voltages for a startup. A high voltage programmable power supply is employed to deliver the 200 V required to run the gadget under test. Finally, a digital oscilloscope is employed to read out waveforms, clock, and output voltage dynamics. These instruments are read and controlled through a USB/RS232 or General Purpose Interface Bus (GPIB) interface.

A real-time application was altered to read the status and internal test results of each Brick examined. In addition, the testing program may examine the data read for each test and apply cuts to decide whether the measurements fulfill the acceptance standards. The software is developed visually in a National Instruments LabVIEW framework shown in Figure 3.5, using commercial instrument drivers and methods

for interfacing with the DAQ module. The application examines the operation of the LVPS Bricks (current, voltages, and temperature), assesses the Bricks operation and checks data gathered by commercial equipment used to carry out the procedure. It also saves the results of each Brick test. The technique is completed by eleven different tests, each of which communicates with several instrumentation equipments. Figure 3.4 depicts the entire test bench configuration. The test bench is built on a computer that controls and reads a variety of commercially available test equipment. The technique is completed by eleven different tests, each of which communicates with several instrumentation equipments. The Brick is required to pass all tests mentioned in Figure 3.5, before they can undergo another checkout procedure called burn-in. The program has the capability to evaluate the data read for each test, and applies cuts to determine whether the measurement meets acceptance criteria. The program also saves data files for each Brick.

The Brick measures and sends six analogue signals to the ELMB motherboard: input voltage and current, output voltage and current, and temperature readings from two points on the Brick (primary and secondary side switches) measured with thermistors. The ELMB motherboard sends an enable signal and a start pulse to the Brick. The start pulse briefly powers the device's control circuitry, causing it to turn on. If the Enable signal is high, the Brick will turn on after a short delay after the start pulse is received. The Brick has a rated output current of 3 A, is capable of delivering twice the rated current (6 A), and includes automatic over current protection (at 10.5 A) and over temperature protection (at 70 °C). along with addition to over voltage safeguards (at 12 V). Each Brick is tested using a specific procedure and must meet various criteria. These criteria for the LVPS building blocks are listed in Table 3.1.

Parameters	Values
Threshold Stable Load	2.3 A
Over Voltage Protection	12.5 A
Over Current Protection	10.5 A
Output Voltage Ripple @ Nominal Load	10 V
Duty Cycle @ Nominal Load	2.1 Hz
Frequency @ Nominal Load	9.8 Hz
Efficiency @ Nominal Load	11.5
Input Power (current) @ Nominal Load	10.5 A
Over Temperature Protection	72 ° C

Table 3.1: Test Parameters used to validate the LVPS Brick using test stations [22].

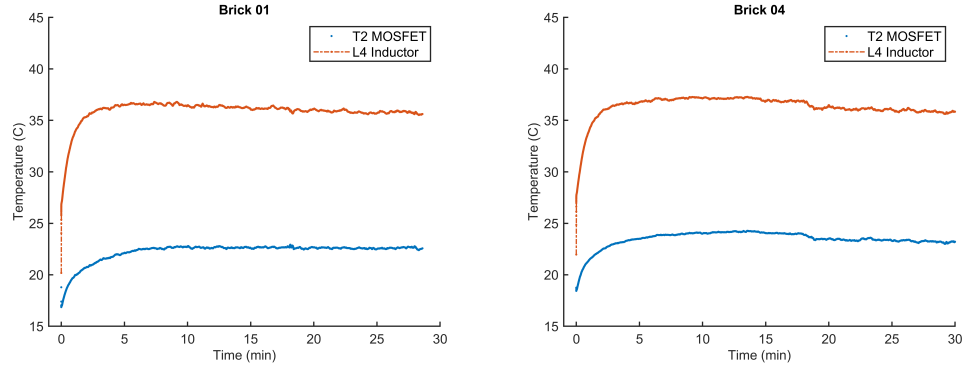


Figure 3.6: A 30 minute measurement of the LVPS Brick temperatures was taken on the current prototype V8.4.2 using the test bench [62].

3.6 Initial test bench results

The LVPS Brick protect circuitry is evaluated by analyzing two metrics: the clock’s jitter and its impact on system stability. In addition to validating the Brick’s features, this test bench also measures its protective circuitry, which protects it from overheating, overcurrent, and overvoltage. If the output voltage, current, or temperature of the Brick exceeds the allowed range, it can cause damage to both the Brick and its power components. Overly high temperatures or output voltages may cause system components to malfunction and reduce the Brick’s lifespan. Figure 3.6 depicts two Bricks that were tested on the test bench. The temperature variations in two regions are depicted in this plot. This plot depicts the temperature variations at

two locations on the Brick that have the highest temperatures (MOSFET - T_2 and L4 - inductor - T_3). Using the test parameters in Table 3.1, it is observed that the temperatures are significantly lower than the over temperature protection and lower than 40°C, which is the nominal temperature on the burn-in test station.

Chapter 4

The Burn-in test station

4.1 Introduction

Components must fulfill their intended purpose for an expected duration of time in all potential field situations. The assessment of a system failure rate includes intermittent functioning and poor performance. Under all conditions, a high failure rate is unacceptable. Field failures can result in expensive repairs, product recalls, and customer unhappiness, all of which harm a manufacturer's bottom line and profitability. Manufacturers have devised methods to enhance the possibility of delivering the best possible reliability to the end-user in response to this expectation. Perhaps the simplest way to accomplish this aim is to run a quick but better test case of the device in the actual field loading environment, basically confirming the performance signature of the field circumstances.

When done across a wide sample size of identical device types, this environmental effect burn-in test allows the manufacturer to acquire a statistically based picture of the device's field performance. Any device that performs atypically will be withdrawn from the lot and will not be supplied to the client. A burn-in test subjects

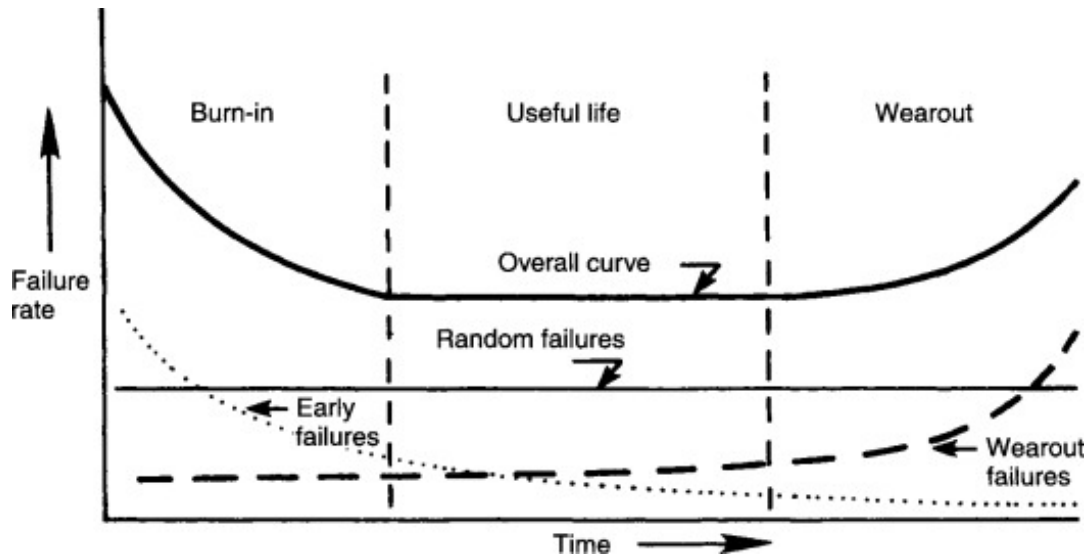


Figure 4.1: Bathtub-curve used to indicate, where electronics usually experience infant mortality [70].

components to normal working circumstances in a controlled environment, causing faulty items to fail before reaching the end-user. By removing questionable products from the field population, the probability that components will function to the degree of dependability required by consumers improves significantly. A continual burn-in test plan is also required for statistically-based process control management of the manufacturing line.

4.1.1 Elimination of early deficiency

The failure rate of electronic components follows a pattern known as the bathtub curve over time. The term is derived from the graph's shape, which is created by graphing the failure rate of parts against their service life. The resultant curve looks like a bathtub cross-section, with steep curves at either end and a flat bottom.

The bathtub curve is caused by the constraints of the manufacturing techniques and equipment options used in the device's production. Irregularities that occur throughout the manufacturing process produce a high likelihood of early failure. Device

manufacturing process requirements are pushed to their resolution and tolerance limitations as system application needs grow more sophisticated. An excellent example is a demand for high-bandwidth channels in modern communications networks for video streaming and ultra-fast data transmission. These systems need greater operating frequencies, which cause device geometries and line spacing to reduce. As production processes and equipment approach their tolerance limits, there is an unavoidable rise in the rate of early failure. Extrinsic processes unrelated to device production, such as packaging and connection, are also major causes of early-stage failures. Processes and device parameters may be adjusted at critical production phases over time and with data from burn-in testing to minimize all sections of the failure rate bathtub curve.

The period when the failure rate is constant is represented by the flat region of the curve. This is sometimes referred to as the component's useful life. The failure rate for the device population in this part of the bathtub curve is determined by the application's utilization of environmental parameters. When compared to a more benign setting, severe conditions have a greater failure rate. The right-hand rising slope of the curve happens as the combined voltages force the gadget to its practical power limit over time. Reduced performance causes further degradation till the end of life is reached. Accelerated Life Testing is commonly used to generate a statistically based forecast of projected wear life, and it should be demonstrated to be made much beyond the estimated life requirement of the end user's application [18].

4.1.1.1 Deficiency through stressing components

The goal of a burn-in test is to reduce the percentage of devices that fail prematurely before meeting the estimated market lifespan requirements. The components are screened out of weaker devices by subjecting them to settings meant to expose

the samples to improved field environments to uncover abnormal performance elements. Elevated temperatures and voltages present additional stresses that might cause breakdowns. Test specialists can find non-compliant devices without affecting the lifespan of the other test devices by placing the components in specially constructed test benches that subject them to properly calibrated adverse circumstances.

4.1.1.2 Reliability over volume

Traditional destructive testing is still widely utilized to evaluate failure rates throughout the stable (bottom of the bathtub curve) and wear-out periods (end of the bathtub curve) [50]. In contrast to off-the-shelf items, these tests are often done on standard evaluation circuits used to monitor different batches of chips. Burn-in tests on application-specific deliverables can be used to trigger out-of-character performance indications without degrading correctly functional ones. Burn-in detects and eliminates the probable early high failure population. The advantage of this strategy is that it allows for the field distribution of a statistically more dependable product population to the client.

4.1.1.3 Incorporating burn-in testing

Manufacturers can conduct burn-in testing in a variety of configurations depending on the application. The component is subjected to increased voltage and temperature during the static burn-in process; yet, the device runs under unusual operating circumstances. A high temperature reverse bias test is an example of this. During a dynamic burn-in, the device is subjected to more realistic operating circumstances than it will face in its field use. This may involve RF biasing for wireless-enabled devices.

In most cases, a mix of static and dynamic burn-in yields the greatest results. One

of the most important advantages of burn-in is the collecting of performance data. A well-designed burn-in can assist enhance future testing processes by meticulously logging the conditions and timing of each failure. Each batch produced should result in more statistically relevant data that provides a more accurate picture of the devices' failure likelihood over time. This more certain picture of dependability may then be used to drive changes in the production process, resulting in higher quality devices or much greater product yields.

In the case of validating the LVPS Bricks we used burn-in, in this section we will discuss the burn-in test bench created at Wits University and elaborate its significance to the Bricks.

4.1.2 Importance of burn-in testing to TileCal

The primary goal of burn-in is to reduce the early life failures (mostly described in the infant mortality region on the bathtub curve) of the components, in this case LPVS Bricks. The failure rate of the Bricks is critical because they are difficult to access once on the ATLAS detector due to factors such as radiation and a strong magnetic field. Access to the LVPS box containing the Bricks is granted only once in a year of operation. This necessitates that the devices be extremely reliable when powering up the FE electronics, and any failure on them implies the loss of data for that specific module until the next maintenance cycle. Early failures in the burn-in region, as shown in Figure 4.1, are usually associated with a high failure rate of the electronics. To reduce the failure rate, the Bricks are subjected to accelerated ageing, which involves exposing them to a stressed environment with increased temperature and load.

4.2 Burn-in test station

Depending on the design and specification of Bricks at the time, the burn-in test station has evolved in various ways over the years. The first iteration of their cooling system used water as the coolant; later, an attempt was made to use an air-driven convection cooling system, but there were too many inconsistencies with the fans, and the system overheated. This prompted us to return to using a water-based cooling system as the framework. The current burn-in is similar to the Brick in that it can apply a burn-in cycle. Because there is little left to do after the burn-in process, a burn-in cycle makes it user-friendly. The user would only be included in the monitoring. The burn-in is composed of the following parts:

- Cooling system (cooling plates, hoses, and water cooler) for active cooling of Bricks and dummy load boards. It also enables the Bricks' operating temperature to be controlled.
- The electronics are housed in a test bench (chassis), which also provides thermal and electrical isolation. Figure 4.2 depicts how the electronic devices are connected to each other Main Board (MB), eight Brick Interface (BI) boards, two Load Interface (LI) boards, two Dummy Loads (DL) boards, power supply).
- A software application (LabVIEW) for controlling and monitoring the electronics.

During the burn-in process, the burn-in station can record the following parameters from the Brick: input/output voltage, input/output current, and two temperatures. Efficiency and failure rate for each Brick can be calculated using these parameters. The station can turn on and off a three-state logic Brick, which controls the 200 V DC input from the DC power supply. The electronics are fed a standard voltage from a socket and converted to meet the needs of the respective circuit board.

4.2.1 Justification of burn-in design

The current burn-in station is the third version, the first version utilizing the mechanism of cooling system as in the current version [64], which is water based whereas the other version employed the forced air convection as its cooling mechanism [37]. The need to revert back to the water-based cooling system was necessitated by the fans overheating overtime hindering them to provide enough cooling during the burn-in. To move from water-based cooling system was motivated by concerns of water spillage and inadequate heat sink at the time but all those issues in the current iteration of the cooling system are resolved. With MOSFETs able to operate with temperatures above $100^{\circ}C$ and good thermal posts within the Bricks, issues of the heat sink is resolved. Another reason that made us select this version was due to the space constraints of the printed circuit boards which after modifications and removing components which were redundant and obsolete necessitated the reduction of the boards surface area. This also implied the cost of production of this boards will be reduced significantly.

4.2.2 Burn-in components

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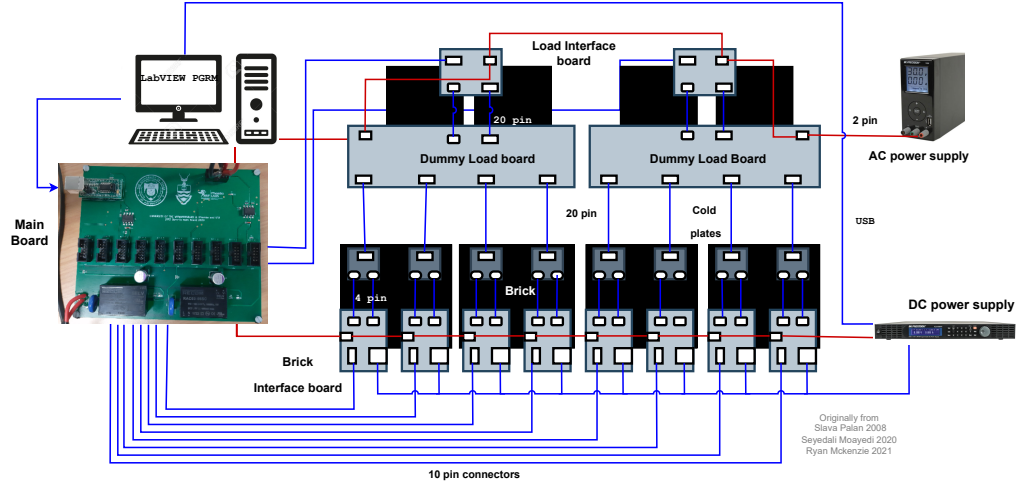


Figure 4.2: The burn-in test station components.

the printed circuit boards which after modifications and removing components which were redundant and obsolete necessitated the reduction of the boards surface area. This also implied the cost of production of this boards will be reduced significantly.

4.2.2.1 Main Board

Figure 4.3 depicts a simplified schematic of MB containing only the essential components. The LabVIEW control programme uses Universal Asynchronous Receiver/-Transmitter (UART) to communicate with each individual Peripheral Interface Controller (PIC) microcontroller. An Future Technology Devices International (FTDI) on board circuit is used to establish communication via a serial connection RS232 over the USB virtual com port. To accomplish this, Main Board (MB) only serves as a multiplexer for each individual readout board. The LabVIEW control programme achieves this multiplexing by asserting the UM232's Request-To-Send (RTS) signal and transmitting the address of the required interface card with which the programme wishes to communicate, followed by deasserting the RTS flag. PIC generates a conditional instruction that reads a signal receiver from the UM232 transmitter line and modifies the states of the digital outputs reading to the demultiplexer's (MC14514) data lines [69]. A Demultiplexer (DEMUX) or data splitter is a circuit that allows

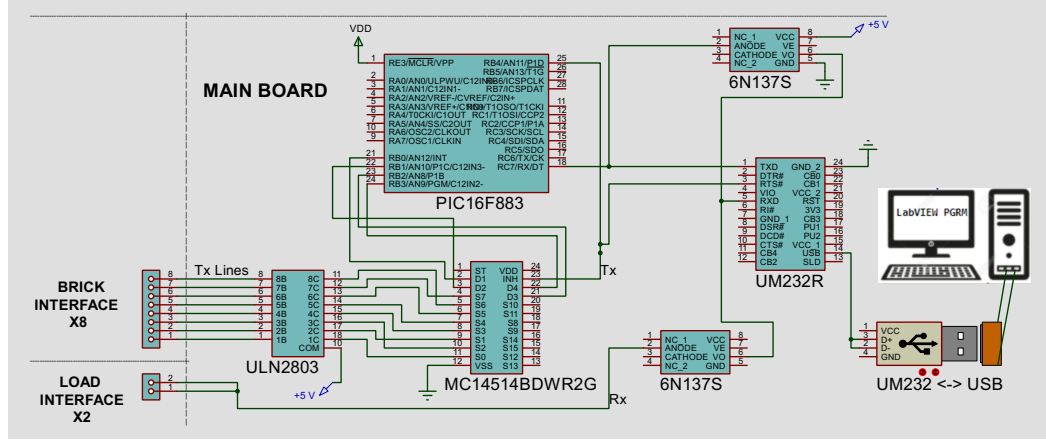


Figure 4.3: Mainboard (MB) schematic diagram.

Figures/System/mbp.jpg

Figure 4.4: Mainboard (MB) prototype.

multiple outputs to be distributed or output from a single input. After this address initialization, all bytes sent by the programme are passed directly to the appropriate readout board, with no interference from the MB. The Transmitter (Tx) of each BI card's UART is linked together.

4.2.2.2 Brick Interface board

Figure 4.5 depicts the main components on the board and their connections on the BI functional schematic. The BI board's primary function is to digitise data from the various inputs of each Bricks 20-pin ribbon cable and transmit it to the computer. The BI board's heart is a 16-channel ADC (LTC2449) [73]. All Brick behaviour parameters, including input/output (voltage and current) and two temperature readings, are measured. For control and monitoring, each building block has its own identical and corresponding BI board. Aside from digitising all analogue signals. The BI board in Figure 4.6 also controls the digital logic circuitry (SN74LVC) [45] and switches the 200 V input supply on and off via a high side MOSFET. A dual solid state switch (LBA716) [19] is used to switch to +15 V DC via the Bricks tristate input. A tristate denotes three voltage levels that can be used to start an ELMB's

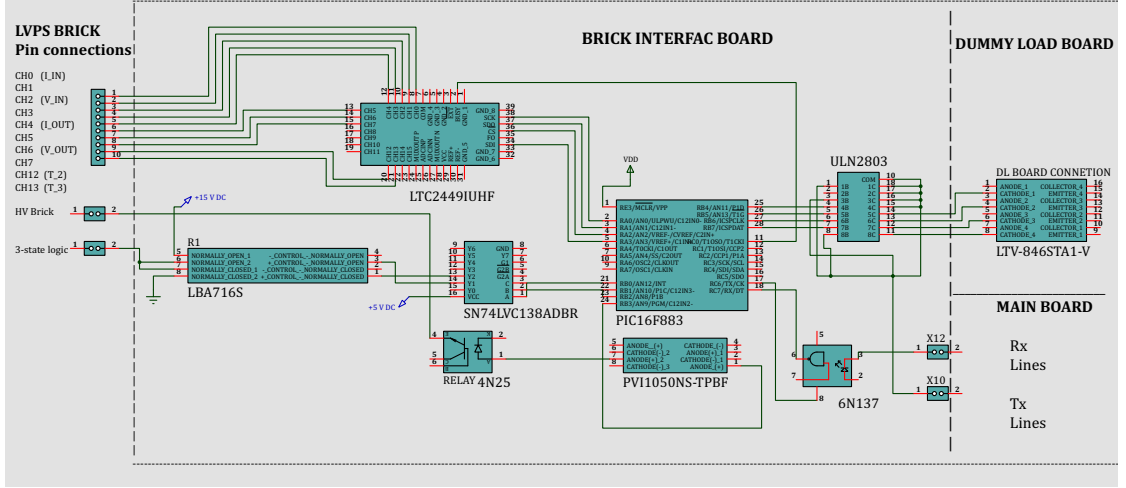


Figure 4.5: Schematic of interface board.

Bricks. However, only the external 0 V DC and +15 V DC signals are required to start and stop controlling the Brick during the burn-in process. To avoid temperature drift of the thermistor voltage divider circuit, the BI also includes a voltage divider for the thermistors located on the Brick.

4.2.2.3 Load interface board

The Load Interface (LI) board prototype is similar to the BI board in that the LTC2449 ADC senses the Brick output voltage and current measured on the DL board. The load current of the devices is managed by the LI boards shown in Figure 4.7 by sending digital commands from the LabVIEW control application to the DL boards' Digital-to-Analogue Converter (DAC) (TLV5620TDR) [43]. A serial signal generated by the LabVIEW control application identifies a specific task that the PIC must complete. The digital outputs of the PIC are used to drive the DATA, CLK, LOAD, and LDAC signals of the DAC. On the LI board, data acquisition entails reading eight differential inputs representing voltage and current measurements. The serial bit stream, which represents an analogue value, is returned to the MB Receiver (Rx) input for monitoring and data logging in the LabVIEW control application.

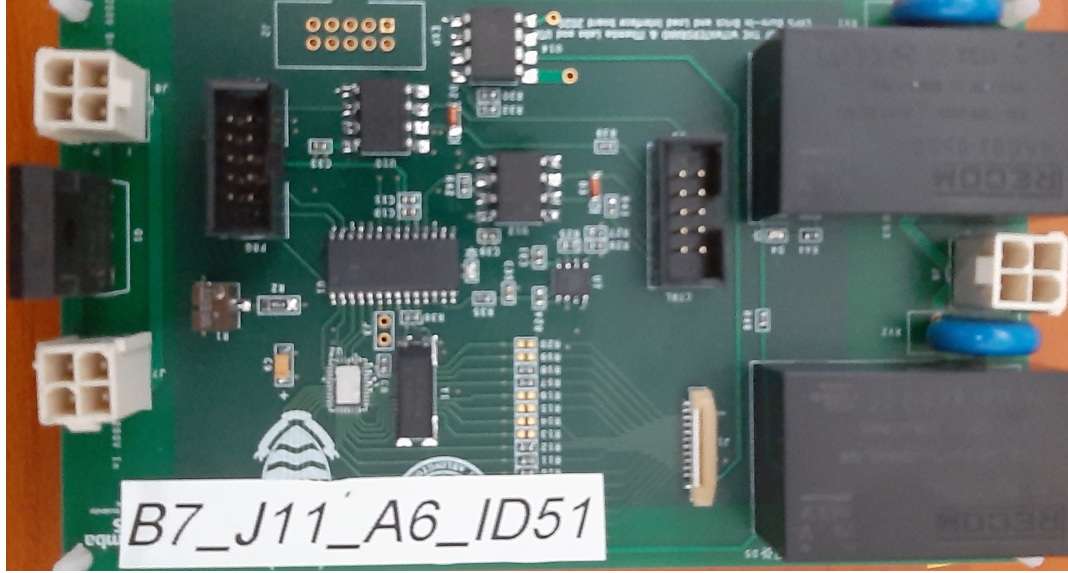


Figure 4.6: Prototype of the BI board.

4.2.2.4 Dummy Load board

The Dummy Loads (DL) board prototype is shown connected to the LI board in Figure 4.8. The burn-in station contains two circuit boards. Each DL board has four independently programmable power loads for four Bricks. They use an **Operational Amplifier** (OpAmp) Operational Amplifier (OpAmp) and enhancement-mode MOSFETs in the N-channel area. The zone is defined as the area between the source and drain terminals. It has four terminals with connections for the gate, drain, source, and body. The drain and source are n+ doped regions in this type of field effect transistor, and the substrate or body is P-type. According to the equation $R_{DS} = V_{DS}/I_D$, where R_{DS} is the on-resistance, V_{DS} is the voltage drop across the drain-source, and I_D is the source current [38], this MOSFET can pull a voltage of 200 V while a current of approximately 50 A flows with an on-resistance of 4Ω . The OpAmp always tracks the Brick load current versus the DAC output voltage in this configuration, which is inherently current mode control.

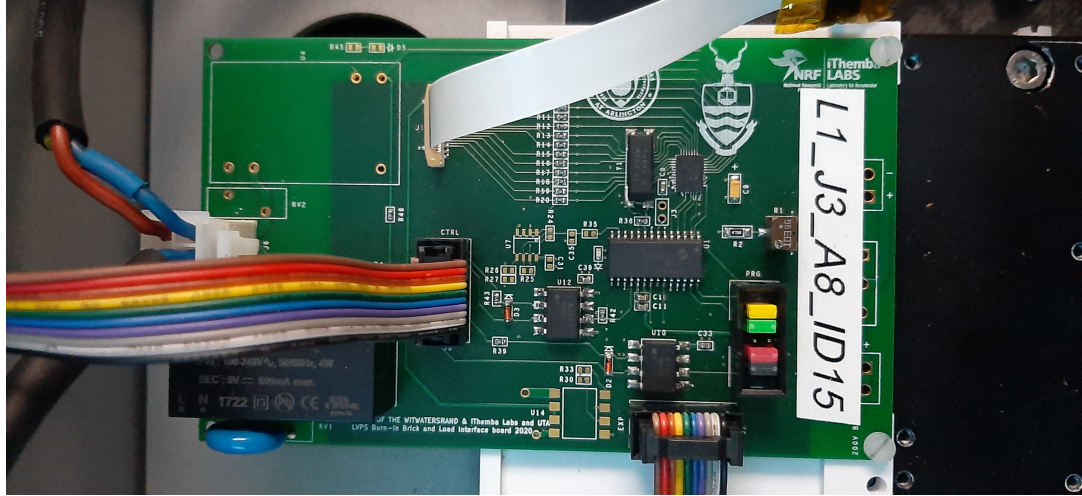


Figure 4.7: LI board prototype.

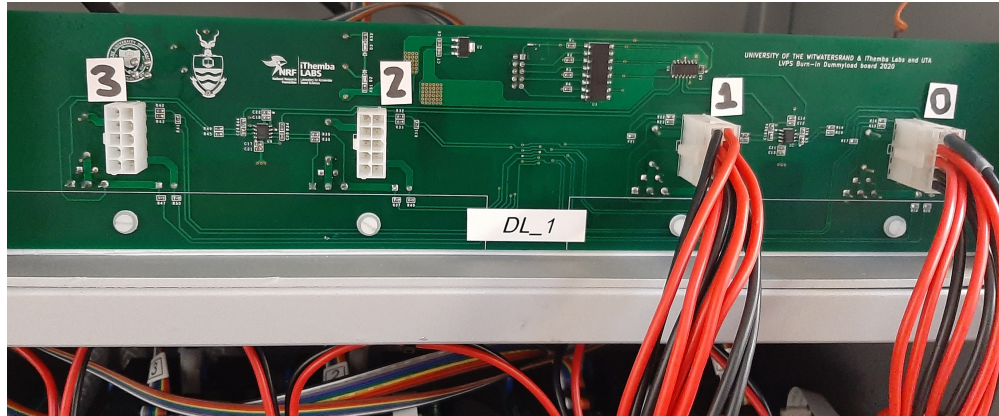


Figure 4.8: DL board prototype.

4.2.2.5 Coolant System

The heat from the Bricks and the DL MOSFETS requires to be dissipated to keep the components from being damaged by overheating. Eight Bricks are attached to the four cold plates as shown in Figure 4.2 and two DL boards are attached to the other four plates. The Brick dissipate the heat from the MOSFET and inductor via the thermal posts which are the ones attached to the cooling plates and the heat on the DL is dissipated via the MOSFETS to the cooling plates. To maintain a uniform temperature on the system, Water Chiller shown in Figure 4.2 is used and water

circulates from it to the cooling plates via the hoses. The distribution of water to each of the cooling plates is done by the water manifolds.

4.2.2.6 Burn-in operation

Table 4.1: The burn-in test station operational parameters and safe guards.

Framework	Burn-in	Nominal	trip points (Protection)
Working temperature	60 ° C	~ 35-40 ° C	70 ° C
Brick Load	5.0 A	2.3 A	< 7 A
Operating time	~8 hrs		

Each LVPS Brick would be subjected accelerated aging as part of the production testing, whereby a Brick is subjected to stressed environment where temperature and load are elevated. These settings stress the electronics under test, causing components that would otherwise fail prematurely to degrade fast throughout the test before they can be fabricated and put on the TileCAL. The Table 4.1 is used to operate the burn-in test station and the following measures are utilized to show the Bricks' behaviour: temperature, efficiency, input and output voltages, and current.

Chapter 5

The Burn-in test station software

5.1 Introduction

Microcontrollers (MCU) are well-known for their widespread application in industrial automation. Automation was formerly accomplished by the use of mechanical and electrical contractors, as well as relays, prior to the development of microprocessor-based systems. They were incredibly complicated, having a plethora of connections and components. If a change or addition was necessary, the majority of these connections had to be updated. Most of the time, this was far more difficult than constructing a new one. With the evolution of microprocessor-based systems, needed alterations may now be achieved entirely through software updates, eliminating the need for hardware adjustments. As a result, systems that are simple to create with fewer components have surpassed earlier systems with more components and a greater failure rate. If no automation system is employed, switching equipment, such as energizing a heater or turning off the power supply, can only be done by an operator. Timing is critical in some applications, and no mistakes are tolerated. However, the operator may be to blame for some errors or delays. A MCU-based control device can be used to lessen the likelihood of these events occurring and to reduce reliance

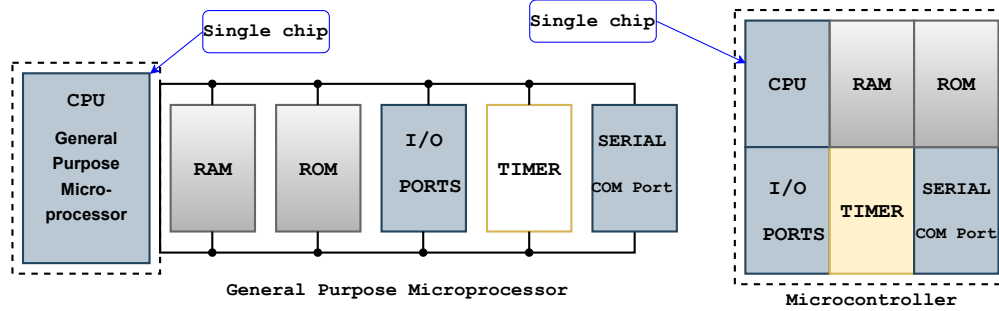


Figure 5.1: Left: The general purpose microprocessor system. Right: MCU system.

on him.

In this project, MCU are incorporated in the Printed Circuit Boards (PCBs), i.e. main board, interface boards which are used to carryout vast range tasks according to the particular PCB relay messages to/from the control programme LabVIEW commands.

5.2 Mircocontrollers

5.2.1 General

A digital computer's three major components are the Central Processing Unit (CPU), program and data memory, and an Input/Output (I/O) system. The CPU controls the flow of data between the various computer components. It also processes the data using digital procedures. A microprocessor is a single-chip semiconductor device that incorporates a CPU. Microprocessors are general-purpose electrical devices that may be utilized for a wide range of tasks. An MCU is a single-chip computer. The I/O and memory subsystems of an MCU specialize in these devices so that they can connect with hardware and control application functions. MCUs, which are strong digital processors, provide a high level of control and programmability, which considerably increases application effectiveness. MCUs are frequently embed-

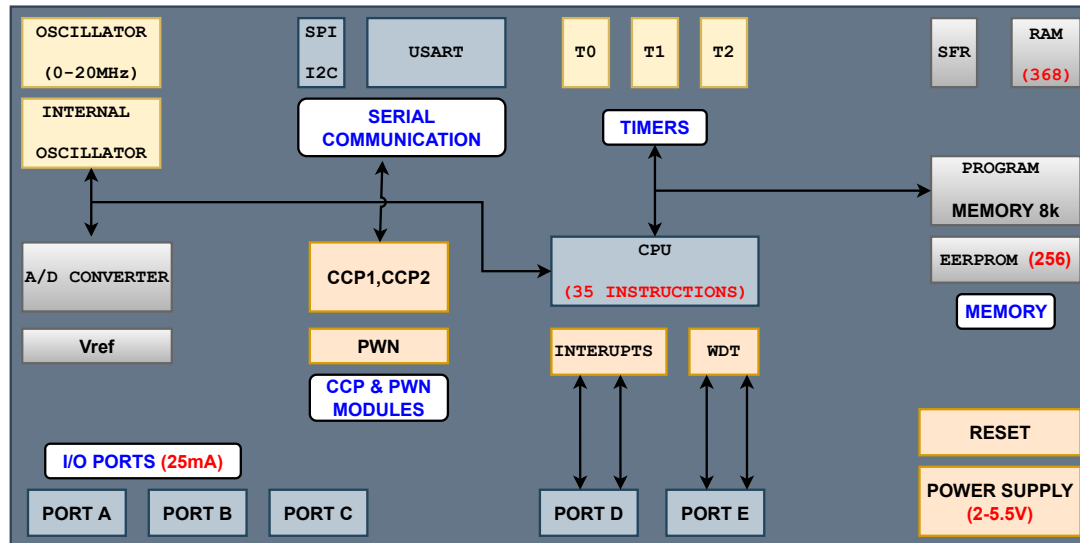


Figure 5.2: Architecture of PIC MCU.

ded devices that are utilized to control an application. To run programs, they include several on-chip capabilities such as serial ports, parallel input-output ports, timers, counters, interrupt control, Analogue-To-Digital Converters (ADC), Random-Access Memory (RAM), and Read Only Memory (ROM). Figure 5.1 depicts a comparison between the microprocessor-based system and the MCU-based system. The majority of MCUs feature an 8-bit word size, at least 64 bytes of Read/Write (RW) memory and one kilobyte of ROM. The number of I/O lines varies greatly, from 16 to 40. Most of these devices, however, are difficult to program unless they contain an Erasable Programmable Read-Only Memory (EPROM) chip.

5.2.2 PIC Microcontrollers

General Instrument Corporation created the Peripheral Interface Controller (PIC) micro in 1980 as a tiny, quick, and inexpensive embedded MCU with robust I/O capabilities. The PICmicro's promise was recognized by General Instrument, which later spun off Microchip to manufacture and commercialize the device. The PICmicro outperforms previous chips like the Intel 8048/8051/8052 and its descendants, the

Motorola MC6805/6hHC11, and many others in a wide range of applications [46]. Its unique architecture makes it perfect for controlling embedded devices. Nearly all instructions take the same number of clock cycles to execute, making timing control a breeze. The PICmicro is Reduced Instruction Set Computer (RISC) design with only thirty-odd instructions to memorize; its code is exceptionally efficient, allowing the PIC to run with significantly less program memory than its larger competitors.

PICmicro processors can be found in a wide range of items. Remote controls, display panels, autos, appliances, weather stations, ham radio equipment, clocks, motor controllers, sensors, programmable thermostats, robots, toys, battery chargers, computer peripherals, and nearly anything else that uses programmable logic are all examples of programmable logic [7]. PIC MCUs are the smallest MCUs on the market, and they may be programmed to do a wide range of activities. Many electronic devices, such as phones, computer control systems, alarm systems, embedded systems, and so on, use MCUs. MCUs come in a variety of shapes and sizes, but the best are found in the GENIE family of programmable MCUs [77]. Circuit-wizard software is used to program and simulate these MCUs.

Every PIC MCU design consists of certain registers and a stack, where the registers serve as RAM and the stack stores the return addresses. RAM, flash memory, Timers/Counters, Electrically Erasable Programmable Read-Only Memory (EEPROM), I/O Ports, Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Capture/Compare/PWM (CCP), Synchronous Serial Port (SSP), Comparator, ADC, Parallel Slave Port (PSP), Liquid Crystal Display (LCD), and In-Circuit Serial Programming (ICSP) are the primary characteristics of PIC MCUs (in-circuit serial programming) as shown in Figure 5.2. Based on internal design, the 8-bit PIC MCU is categorized into four types: Base line PIC, mid range PIC, enhanced mid

PIC16F883/884/886/887

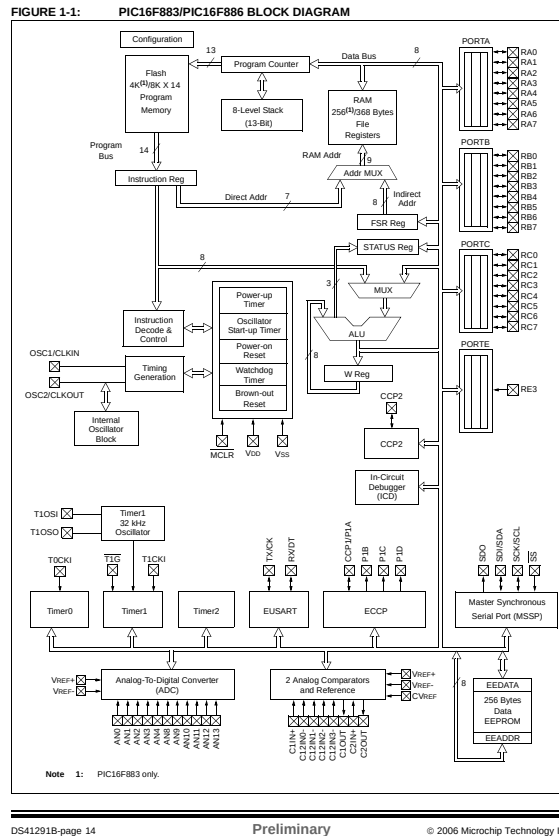


Figure 5.3: Internal architecture of PIC16F883 chip [75].

range PIC, and PIC18. The CPU, I/O ports, memory organization, A/D converter, timers/counters, interrupts, serial connection, oscillator, and CCP module are all part of the PIC MCU architecture [4].

5.2.3 PIC16F883 architecture

The block diagram of the PIC16F883 is shown in Figure 5.3. The RISC architecture underpins the PIC16883 MCU. Its memory architecture is based on the Harvard pattern of distinct memories for program and data, each with its own bus.

- CPU: The PIC MCU CPU is similar to other MCU CPUs in that it includes the Arithmetic Logic Unit (ALU), Control Unit (CU), Memory Unit (MU),

Accumulator, and so on. The arithmetic logic unit is primarily utilized to perform arithmetic operations and make logical decisions. Memory is where instructions are stored after they have been processed. The internal and external peripherals are controlled by a control unit linked to the CPU, and the results and other operations are stored in the accumulator.

- **Memory Organization:** RAM, ROM, and STACK comprise the memory module of the PIC MCU design.
- **RAM:** RAM is a sort of volatile memory that is used to store data in its registers for a limited duration. RAM is separated into two banks, each with its own set of registers. RAM registers are classified into two types: Special Function Registers (SFR) and General Purpose Registers (GPR) are two types of registers.
 - GPR: These registries, as the name implies, are exclusively used for general reasons. Assume we wish to use the PIC MCU to multiply two numbers. In general, we multiply integers with registers and store the results in other registers. As a result, these registers have no particular purpose; the CPU can easily access the data stored in the registers.
 - SFR: These registries, as the name implies, are only used for specialized purposes. These registers can only be used for the functions that have been assigned to them and cannot be utilized as ordinary registers. When the STATUS register, for example, cannot be used to hold data, these registers are used to signify the program's activity or status. As a result, the user cannot modify the SFR's function; the function is set by the dealer at the time of production.
- ROM is a form of stable memory that can retain data indefinitely. The architectural ROM of the PIC MCU architecture carries the instructions or program,

and the MCU executes by the program. The user creates the program for the MCU in ROM, also known as program memory, and stores it permanently before it is executed by the CPU. The MCUs performance is determined by the instruction being performed by the CPU.

- EEPROM: We can only write the program once in the regular ROM, and we cannot utilize the MCU many times. However, in the EEPROM, the ROM may be programmed many times.
- Flash memory is a form of programmable read-only memory (PROM) that can be read, written, and erased thousands of times. PIC MCUs use this sort of ROM.
- Stack: When an interrupt occurs, the PIC MCU must handle both the interrupt and the current process address first. The stack is then used to store the executed code. After finishing the interrupt execution, the MCU activates the process and runs it using an address saved on the stack.
- I/O Ports
 - The PIC16 series has five ports: Port A, Port B, Port C, Port D, and Port E.
 - Port A is a 16-bit port that can be used as an input or output port based on the state of the Tri-State (TRIS)A register.
 - Port B is an 8-bit port that can accept and send data.
 - Port C is an 8-bit port, and the condition of the TRISC register determines whether the port as input or output.
 - Port D is an 8-bit slave port for connecting to the microprocessor's BUS.

- Port E is a 3-bit port that also serves as a control signal for the analogue-to-digital converter.
- The BUS protocol is used to deliver and receive data between peripherals. It is classified into two types: data buses and address buses.
 - A data bus is simply used to send or receive data.
 - The address bus is where memory addresses from peripheral devices are sent to the CPU. I/O pins are used to connect to external peripherals; Universal Asynchronous Receiver/Transmitter (UART) and USART are serial communication protocols that are used to connect to serial devices such as GSM, GPS, Bluetooth, IR, and etc.
- ADC's primary function is to convert analogue voltage values to digital voltage values. The PIC MCU ADC module includes 5 inputs for devices with 28 pins and 8 inputs for devices with 40 pins. The ADC's operation is managed by the special registers ADCON0 and ADCON1. The upper bits of the converter are recorded in the ADRESH register, while the lower bits are saved in the ADRESL register. A 5 V analogue reference voltage is required for this procedure.
- Timers/Counters The PIC MCU has four timer/counters, one of which is an 8-bit timer, while the others may function in either 8- or 16-bit mode. Timers are used to create certain actions like B. Adding time lags between two tasks.
- Interrupts: The PIC MCU contains 20 internal interrupts and three external interrupt sources that are coupled to different peripherals like as ADCs, USARTs, timers, etc.
- Serial communication is the process of systematically sending data one bit at a time through a communication channel.

- USART is a serial communication device that supports two protocols. It sends and receives data bit by bit across a single link using clock pulses. PIC MCUs have two pins, TXD and RXD. These pins are utilized for serial data transmission and reception.
- SPI Protocol: Serial Peripheral Interface (SPI) is an abbreviation for Serial Peripheral Interface (SPI). This protocol communicates data between the PIC MCU and peripherals like SD cards, sensors, and shift registers. The PIC MCU supports three-wire SPI communication between two devices sharing a clock source. The SPI protocol transmits data at a quicker rate than the USART standard.
- I2C Protocol: Inter-Integrated Circuit (I2C) (Inter-Integrated Circuit) is a serial protocol used to link low-speed devices such as EEPROMs, MCUs, A/D converters, and so on. PIC MCUs provide two-wire I2C communication between two devices that can function as masters and slaves.
- Oscillators: Timing is achieved by the use of oscillators. PIC MCUs employ external oscillators such as RC oscillators or crystal oscillators. The crystal oscillator is attached between the two oscillator pins in this example. The capacitor value is connected to each pin and defines the oscillator's mode of operation. There are three options to choose from: crystal mode, high-speed mode, and battery save mode. In the case of RC oscillators, the resistor and capacitor values regulate the clock frequency, which ranges from 30 kHz to 4 MHz.
- The CCP module's name stands for capture/compare/PWM, and it operates in three modes: capture mode, comparison mode, and PWM mode.
 - Capture mode records the time of arrival of a signal, or in other words, it records the value of Timer1 when the CCP pin goes high.

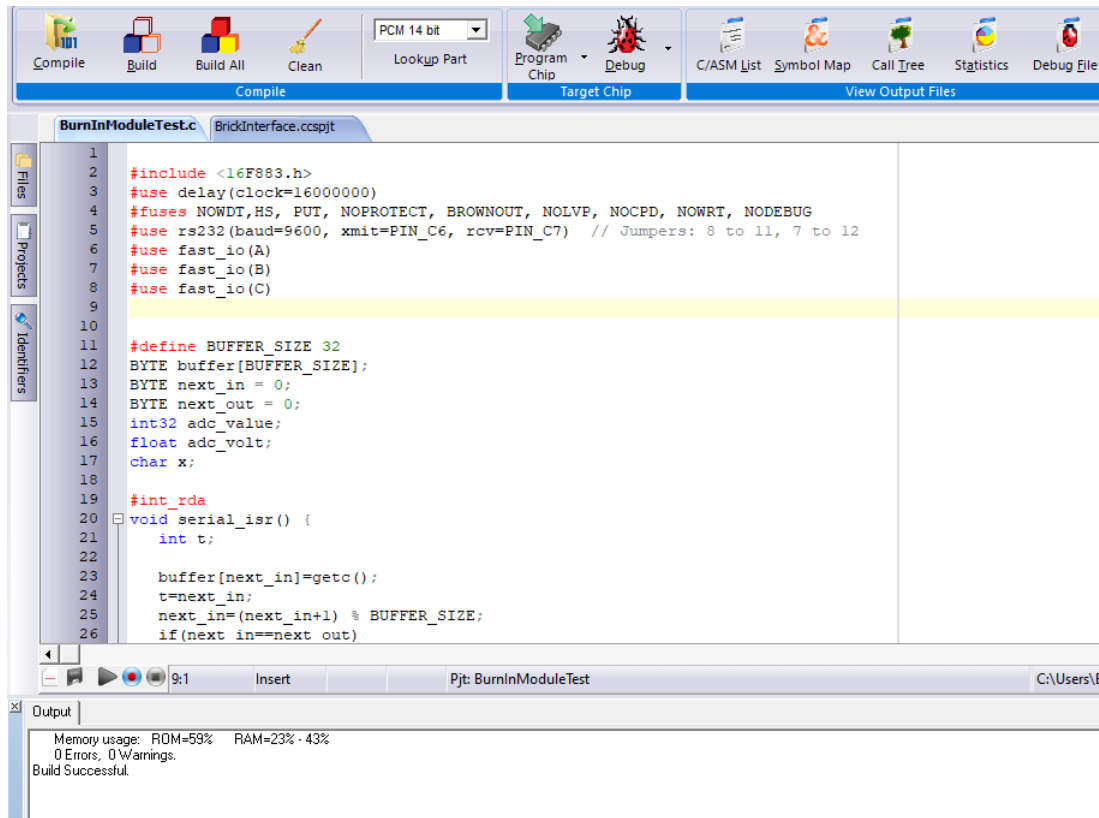


Figure 5.4: Screenshot of MPLAB X IDE after successfully building and compiling the machine code (.HEX file).

- Compare Mode: This mode functions as an analogue comparator. When the timer1 value hits a specific threshold, an output is generated.
- The PWM mode generates pulse width modulated output with a 10-bit resolution and customizable duty cycle.

5.2.4 PIC firmware project

During the execution of a PIC MCU program, the machine code instructions are decoded and executed in a sequential order, resulting in data transfer between registers as well as arithmetic and logical operations. The MCU reset starts execution at address zero, and instructions are executed in address order until a branch is decoded, at which time the instruction yields a new destination address. A decision is made whether to take the branch or continue the sequence based on the results of a

bit-state test.

As a result, machine code is created from assembly code, with each instruction having an easily remembered mnemonic form, such as B. MOVF05, W (move data on port A to the working register). The program might be written in raw binary code, but this would require manual instruction set interpretation. This low-level language works well for simple applications but takes too long for more complex ones. Furthermore, the assembly language is limited to a specific type of CPU and hence is not portable. A higher degree of abstraction is necessary, which necessitates the usage of a high-level programming language. C has established itself as the de facto programming language for MCU. It enables direct control of MCU memory and peripherals while simplifying peripheral configuration, computations, and other software tasks.

A processor-specific compiler turns standard syntax into machine code that is optimized for a particular processor. Furthermore, the compiler package may include a collection of function libraries that implement the most often used operations. The syntax of library functions varies depending on the compiler, but the fundamental rules stay the same.

The compiler's primary role is to convert a source file "BurnInModuleTest.C" to machine code "BurnInModuleTest.HEX". After that, the hex file may be downloaded to the PIC MCU. The source file must be prepared in the proper format, according to both American National Standards Institute (ANSI) C-norms and the compiler dialect. Appendix A.1 shows the program code used for this project.

This may be put into any text editor, although we usually use the MPLAB editor, which is part of Microchip's standard development system software package. This

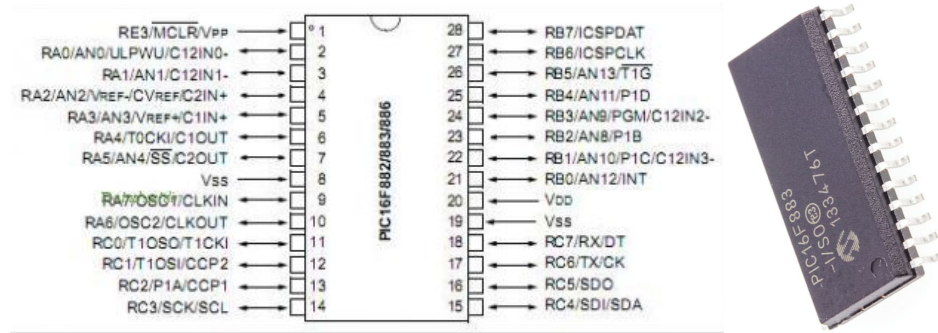


Figure 5.5: PIC16F883 MCU and its pin-out schematic diagram.

free download from microchip website includes file management, a compiler interface, and debugging options for PIC projects [74]. The compiler must also be installed before beginning work. In MPLAB, the compiler file path is specified by choosing Project, Set Language Tool Locations. The compiler can then be chosen from the Project, Select Language Tool Suite menu [74].

Look for the instruction “include 16F883.h” in the original code shown in the Appendix A.1. This specifies the chip for which the program is being written and points to a header file included with the compiler. This file is required since it provides information on the chip register addresses, labels, and so on. The file should be transferred from the Custom Computer Services (CCS) compiler C-program files folder’s device folder to the project folder. By right-clicking on the Header Files folder, it may then be added to this project. We can now build the program by selecting the Compile option from the MPLAB main toolbar. The compiler run dialog will show shortly, followed by a build success message as shown in Figure 5.4.

5.2.5 PIC16F883 Programming Development Tools

The PIC16F883 MCU shown in Figure 5.5 is critical in that it receives signals from the board-mounted ADC chip and transmits the data to the mainboard. The PIC also got digital communication for the mainboard as well as the LabVIEW con-

trol software as an expansion. This communication allows the Brick interface cards to control the functions listed above. It accomplishes this by employing its core processor to analyze data received from its input/output (I/O) peripherals. Through the LabVIEW control application, the BI boards offer control and data acquisition of devices and their automated operations. The MCU stores temporary information in its data memory, which the processor reads and utilizes instructions from its program memory to interpret and apply the incoming data. It then communicates with its I/O peripherals and takes the required action. Sections 4.2.2.1 and 4.2.2.2 provide a full overview of how data is delivered and gathered. MPLAB-X is one of the numerous software programs required to program an MCU. To write and configure code, an Integrated Development Environment (IDE) is utilized. It is used in conjunction with the CCS software compiler, which creates the code and compiles it into a Hexadecimal (HEX) source file. The HEX file contains settings, configuration data, and other information. The MCU only understands the hex file as machine code, allowing it to send and receive orders from other components. The hex file is then flashed into the PIC16F883 MCU using the MPLAB-X Integrated Programming Environment (IPE) and PICKIT 4, allowing debugging and programming of the Microchip PIC [71].

MCU PIC16F883 programming is a simple three-step process:

1. Writing the code
2. Compiling/ debugging the code
3. Uploading the code to the MCU

Figure 5.6 depicts the steps and tools necessary to develop an MCU-based application. The software development process begins with modifying an assembly language program for the target MCU (or its C language equivalent), compiling it, and uploading the resultant binary code file (typically in hexadecimal form) to the MCU

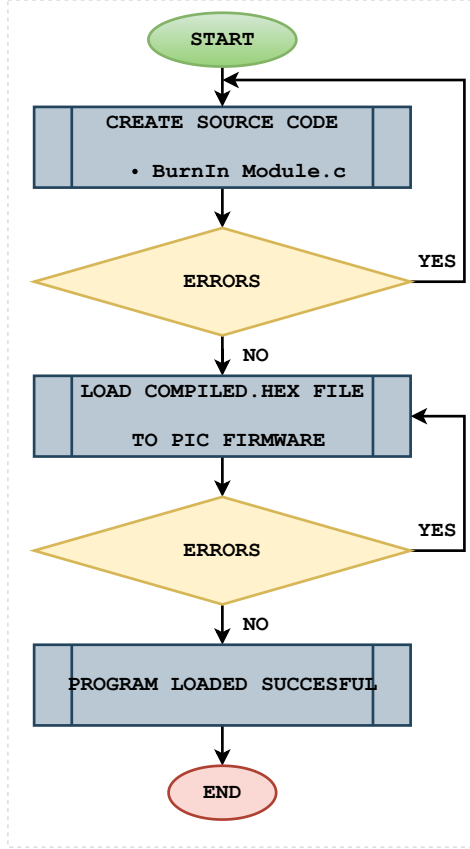


Figure 5.6: The MCU development tools (MPLAB X). The code is written to the MCU memory (EPROM or Flash) by a MCU programmer.

with the assistance of an MCU programmer. Each step may necessitate the usage of a certain tool from a set of options. We programmed the PIC16F883 MCU used on all burn-in station PCBs except the DL boards for this project. We programmed a PIC using the MPLAB-X software package, which comprises two development tools (IDE and IPE) [76]. Along with this fast start guide, a PIC16F883 datasheet [75] is used to confirm all pin connections. It is recommended to refer to the PICKIT-4 start guide, which covers the methods necessary to flash your program into the PIC MCU.

A $10\text{k}\Omega$ resistor shown in Figure 5.7 is placed between the programming voltage, V_{PP} and the supply voltage, V_{DD} to act as the circuit's pull-up register. you could

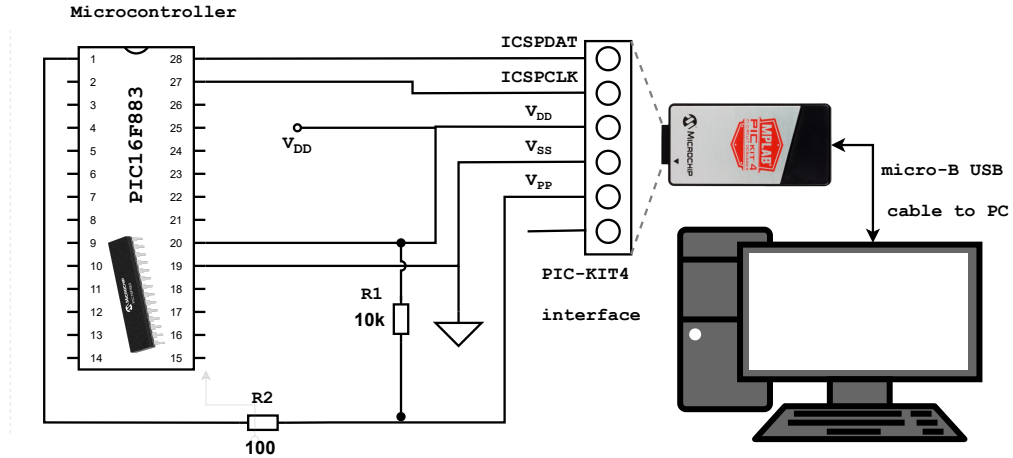


Figure 5.7: Block diagram for flashing program code to the PIC16F883 MCU.

program It is possible to program your target device without using this resistor. However, due to an unstable voltage, the PICKIT-4 may sometimes fail to program the target device successfully. As a result, this pull-up resistor guarantees that you have a constant voltage level when programming the PICs. The 100Ω resistor protects the PIC from voltage damage. Adding a resistor to a line can prevent catastrophic current flows that might otherwise result from brief, high-voltage transients such as electrostatic discharge.

5.3 Simulations

We performed simulations to ensure that the ADC (LTC2449) in the circuit functioned properly. To run the simulations, we used the Proteus software environment. Proteus is a software suite intended for industrial and educational uses for modeling MCUs and simulating virtual systems [72]. Proteus incorporates circuit simulation, animated components, and microprocessor models to enable collaborative modelling of completed MCU-based designs. Proteus enables concepts to be designed and tested prior to the creation of a physical prototype [79].

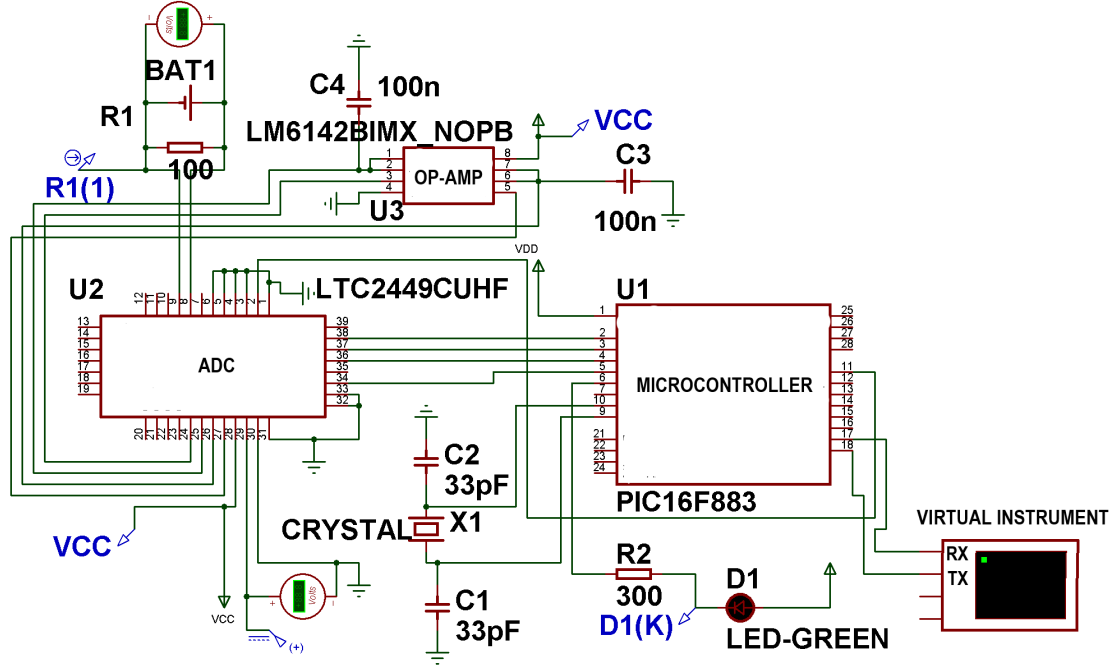


Figure 5.8: The BI board diagram with selective components used to simulations on the proteus framework.

To begin, we utilized the BI board schematic design to pick critical components, allowing us to concentrate on the signal flow between the PIC and the ADC. One of the reasons for doing this was to ensure that the Hex source file we developed from the source C-code (Listing A.1) stated in Appendix A works properly with the BI board's needed capability. To begin this process we used the schematic diagram shown in Figure A.1 of the BI board and selected essential components that enables us to focus on the signal flow between the PIC and ADC. One of the reasons for this was to check if the Hexadecimal source file we created from the source C-code listed in the appendix is functioning according to the required functionality of the BI board. The simulations were carried out in the manner that we would send analogue signal which mimics the actual measurements we would receive from the Bricks and will be converted by the ADC and be displayed on the virtual terminal (see Figure 5.8) for the circuit used.

The American Standard Code for Information Interchange (ASCII) characters provided in Table 5.1 are used to request signals from a specific channel of interest. We utilize the circuit in Figure 5.8 and Table 5.1 to send random values to simulate signals from the Bricks; a similar test would be performed using the real firmware. Finally, before being read and processed by the MCU, the outputs are transformed to digital form. The ADC, which samples the analogue waveform at regular time intervals, assigns a digital value to each sample. The digital value emerges at the converter's output in binary-encoded format, which is subsequently read and processed by the MCU. The terminal software transmits ASCII data in UART format. When you input a character, the ASCII equivalent is sent. The characters are transferred at the rate at which they are typed. They are not sent at predetermined periods. The ADC, which serves as the brains of this BI board, gathers and converts all behavioural characteristics like voltages, current, and temperature for the MCU to read and transmit.

To confirm that the machine code (.HEX file) was functioning to expectations, we used serial communication software, whereby we passed analogue signals to the BI board and received digital signal outputs, see results in Table 5.1. It should be noted that the results were not the main objective, instead it was the ASCII characters in Table 5.1 were recognised.

5.4 LabVIEW control program

The LabVIEW graphical programming environment is used to develop the PC's central software, which interfaces with all burn-in circuit boards and visually records data points. LabVIEW is a graphical programming language that allows you to construct apps with icons rather than lines of text. Unlike text-based programming languages, in which sentences dictate program execution, LabVIEW employs data-

Table 5.1: ASCII characters were sent to ADC to verify the functionality of each channel using the serial communications software package.

ASCII characters	Function	ADC Channels	Output results
1	Brick 15 V on	CH0-CH1	-1.36 V
2	Brick 15 V off	CH2-CH3	-0.65 V
3	Brick 200 V on	CH4-CH5	-0.75 V
4	Brick 200 off	CH6-CH7	-0.44 V
r	Brick Start (Run_IN)	CH8-CH9	0.04 V
o	Brick Stop (Run_IN)	CH12-Ch13	1.15 V
g	Read Brick input current	CH8-CH9	0.59 V
i	Read Brick output current	CH15-CH16	1.031 V
t	Read Brick input voltage	CH0-CH1	0.81 V
p	Read Brick output voltage	CH2-CH3	1.25 V
e	Read Brick temp 1	Ch4-CH5	1.05 V
f	Read Brick temp 2	CH6-Ch7	0.69 V
q	Read back address	CH8-CH9	0.89 V

flow programming, in which data flow governs execution. You may construct a user interface in LabVIEW using a range of tools and components. The user interface is referred to as the front panel. Then you add code to manipulate the front panel items by utilizing graphical representations of functions. This code may be found in the block diagram. The block diagram is comparable to a flowchart in several ways [14].

The PC LabVIEW control program communicates with all eleven microprocessors in the burn-in station through a single UART layer link passed over a USB bus. UART communication is suitable for embedded system to PC-based microprocessor communications [51]. A FTDI integrated circuit is a USB to UART interface used to connect main board with a computer. The current of the software is the revised version that was created by “B. Phalan” at CERN for burn-in the Bricks (V7.5) [64] that are currently installed on the detector. This new version takes account of the modifications that are implemented in the latest version of the Bricks (V8.5.0).

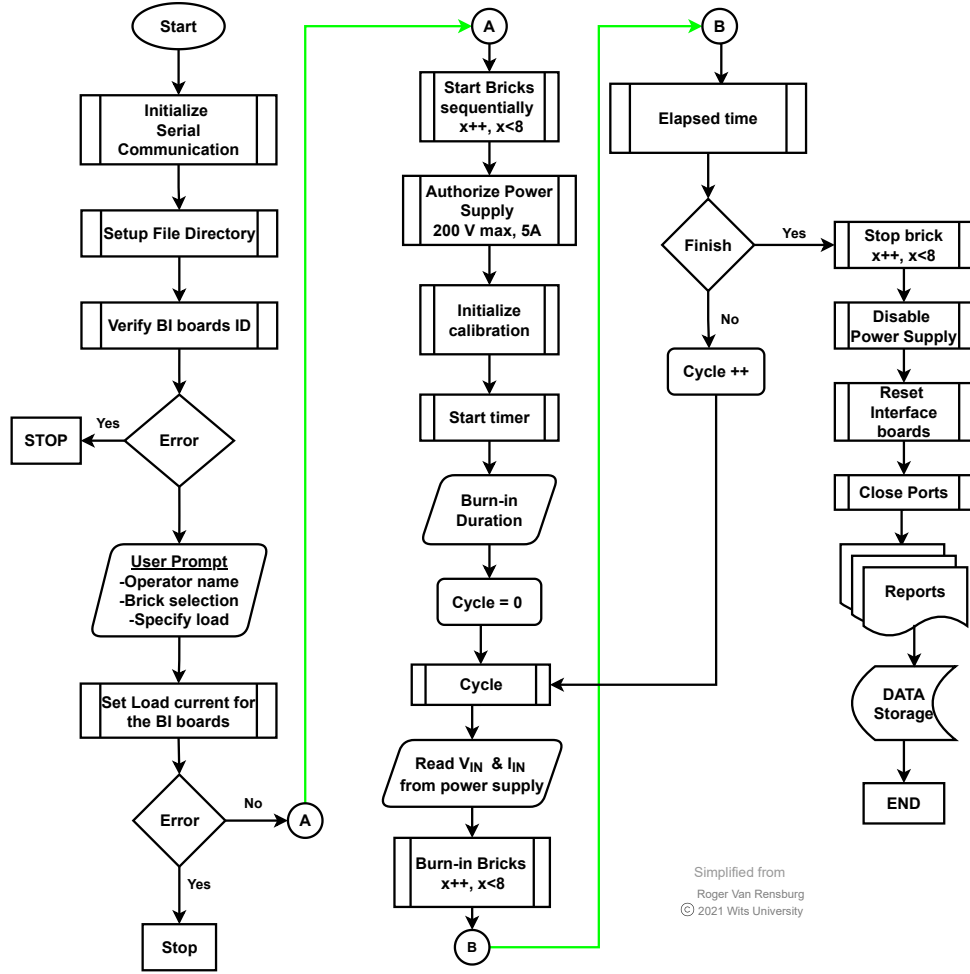


Figure 5.9: LabVIEW control and execution diagram.

A custom application for the burn-in test station is developed using LabVIEW graphical development from the National Instrument Corporation [14]. This application provides monitoring, control and data collection capabilities. It allows for the automated implementation of the burn-in procedure with minimal input from the user. There's also a custom LabVIEW drivers which are developed to communicate the DC power supply with the burn-in electronics via the LabVIEW Virtual Instrument Software Architecture (VISA) communications layer, over Ethernet.

LVPS Bricks are usually mounted and connected before the LabVIEW program runs, this is for safety reasons to the user. The LabVIEW control program starts by ini-

tializing all the communication from the main board and BK Precision power supply. Once that is done it then setups file directory in which “CARD_BURNIN4.TXT” file should be present, this file provides information about location ID of the interface boards . The program will check all hardware of boards and verify their IDs. If all the control are answering, the will display message OK and all the LED’s indicating the boards are functional. The program will ask the user to enter Brick IDs for all eight occupied positions, all positions are equal and universal. The burn-in LabVIEW control program can handle testing of less then eight Bricks. Also the user will be required to enter load. The program then will initialize the loads using the “Init_LOADS.vi.”, this is a Virtual Instrument (VI) which distributes the load current from the user, whereby each LI board will send address to DEMUX to communicate to LI board according to the specified address. The VI are used to create visual algorithm within a program. For Bricks to LI board a consecutive strings for load control are sent. Similar process is done on the other LI board. Once loads are acceptable the program will initiate a Brick startup sequence. An address is send to DEMUX to communicate to BI board, an ASCII character “**3**” shown in Table 5.1 is send to turn-on 200 V on the Brick using output high (PIN_B3), another ASCII character “**1**” to then power the Brick using output high (Pin_B0) and finally ASCII character ‘**r**’ to then start Brick. The same process will continue according to the number of Bricks present and according to the sequence in which they are connected. The program then enables power supply with maximum voltage set at 200 V DC at a current of 5 A.

The next step in the program is to initialize calibrations and start a timer for the burn-in. It is required to specify the burn-in time duration. During the burn-in of the Bricks they will undergo a cycle according to the specification set out by the user. During the cycle, the program will read both input voltage (V_{IN}) and input current

(I_{IN}) from the power supply by sending standard commands for programmable instruments. To subject the Bricks to the burn-in process, first address to DEMUX is send to communication to the BI board, to get the Brick values the loads are set and read from the DL boards. This works in such a way that an address will be selected according to the Brick position that address is sent to DEMUX, whereby a string is send to read DL boards analogue measurements, then after they're scaled, this is for conditioning and calibration of signals received by the ADC. Then the measurements (load metrics) are logged. To read information on the Bricks, an address to DEMUX is send to communication to either one of the LI boards, then consecutive characters are send to read from each of the BI boards according to commands specified on the program. Furthermore there is scaling that takes place to condition and calibrate signals received by ADC. Eventually the Brick performance metrics is logged. This process happens for every Brick present during burn-in. Once that is done, the actual time taken for the burn-in according to what the user specified, then the program proceed and initiate a Brick stop sequence. To do that process, an address is send to DEMUX to communicate to BI boards, then it sends ASCII character "0" to output low (Pin_B2) to stop the Bricks, another ASCII character "4" is send to turn-off 200 V DC on output low (Pin_B0). This is done in all the Bricks that underwent burn-in. Lastly power supply is disabled and the interface boards are reset, followed by closing of ports and a report is compiled automatically and data is logged into a text file. Figure 5.10 indicates the GUI for the burn-in LabVIEW control program, whereby you can monitor and control the burn-in, this is vital as there is also a graphical representation of the data to immediately deduce if the process is going according to the expectations and requirements set-out.

WITS_MAIN_PR.vi
 C:\Users\Electronics LAB\Desktop\Wits_Burnin_Station_1\LabVIEW\WITS v8.4\WITS_MAIN_PR.vi
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 Printed on 3/2/2022 at 3:27 PM

Front Panel

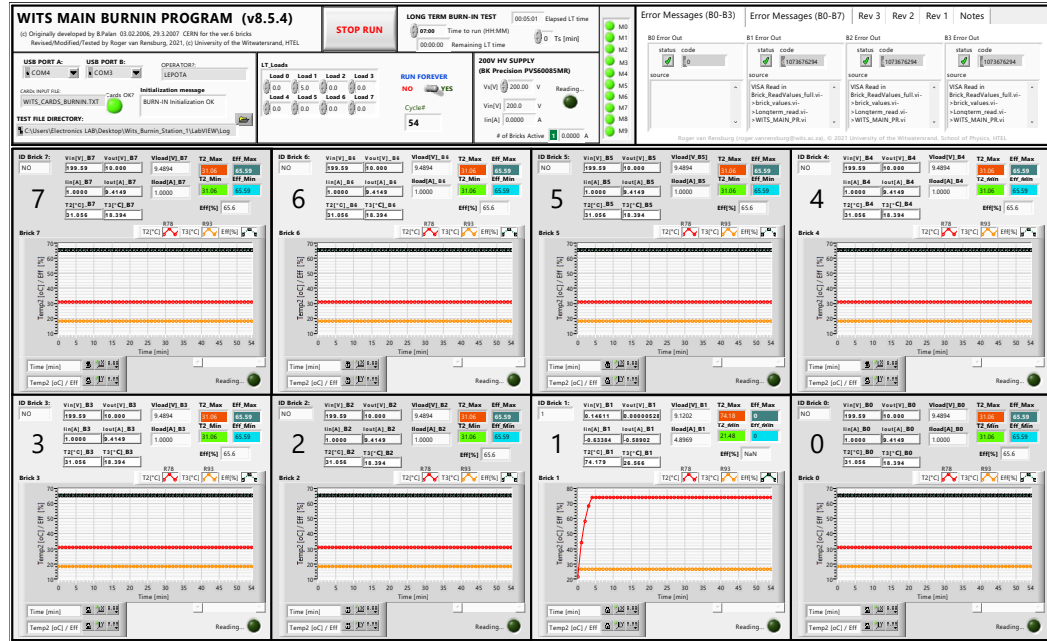


Figure 5.10: LabVIEW Graphical User Interface (GUI) used for monitoring and control of the burn-in test station.

5.5 Preliminary results

In Figure 5.11 (left), a thermograph of a functional burn-in station with only one Brick undergoing burn-in can be observed in the lower right corner. The hotspot directly above the Brick's hotspot is caused by the dummy load MOSFETs converting the electrical energy received from the Brick into thermal energy that must be dissipated. The burn-in temperature parameter is reached in the same, Figure 5.11 with the detected hot spot emanating from the primary-side MOSFETs. It is worth mentioning that the thermistor (Temp2) utilized for on-brick measurements is located adjacent to these MOSFETs and is used in the bricks OTP circuit. The external thermocouple confirms the temperature obtained by the thermal imager. Figure 5.11 (right) depicts the critical sections of the LVPS bricks, such as the primary-side

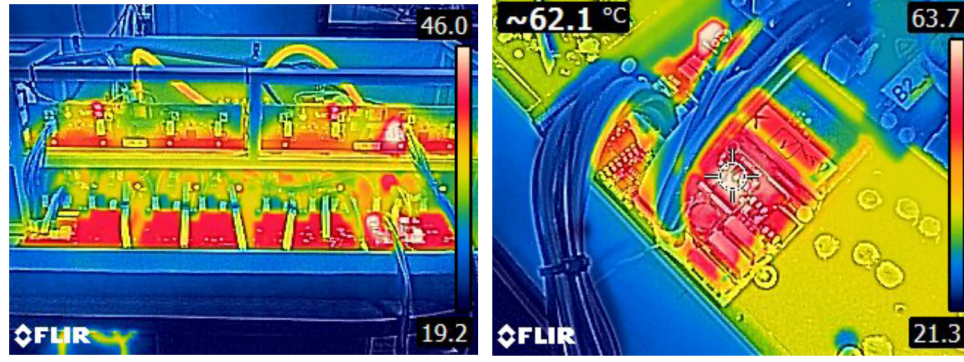


Figure 5.11: A thermograph of a burn in station performing a brick burn-in (left), Thermal depiction of a Brick undergoing burn in, with the focus on the major side MOSFETs (right).

switching MOSFETs (Temp2) and dummy load power MOSFETs (Temp3). The average temperature from thermography is 62.12°C , and the mean value is 60.65°C recorded by the LabVIEW control program, representing a 2.40% discrepancy. It should be noted that this results obtained burn-in one Brick as seen in Figure 5.11, reason being delays encountered in manufacturing and population of the Bricks due to the adoption of the halogen-free PCBs and moving away from flat laminated composite (polycarbonate substrates). The results shown in Table A.2 in the appendix A are represented graphically in Figure 5.12, 5.14 and 5.13. Figure 5.12 depicts a graphical depiction of the two important locations on the brick during the burn-in process based on the operating circumstances stated in Table 4.1. Figure 5.12 depicts a build-up region caused by the brick thermistors acclimating to the burn-in station conditions. These duration lasts roughly 10 minutes under elevated settings. The mean temperature for Temp2 is 60.65°C with a standard variation of 0.19%, while the highest and lowest temperatures recorded on the brick are 61.10°C and 38.27°C , respectively. The mean temperature for Temp3 is 49.47°C with a standard variation of 0.23%, while the highest and lowest temperatures recorded on the stone are 49.93°C and 38.83°C , respectively.

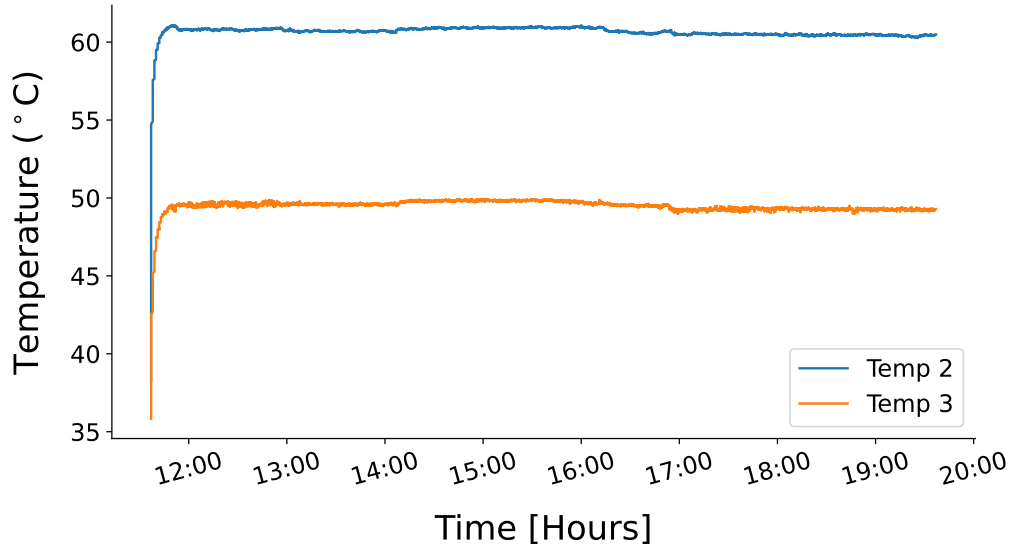


Figure 5.12: The temperature measurements which are located in the two positions on the Bricks spanning for 8 hours during the burn-in process.

Figure 5.13 depicts an input current received from the Dummy-Load board. During the buildup stage as temperature increases, current exhibits similar trend and eventually starts to decrease slightly as the Brick reaches the stability during the burn-in process. Figure 5.14 depicts the efficiency of the Brick undergoing the burn-in. The efficiency starts high during the build up stage before the brick gets accustomed to the stressed environment where its parameters are outlined in Table 3.1. At the minimum temperature of 60.29°C , the efficiency of the Brick is measured to be 70.41% and at the maximum temperature where temperature is 61.06°C , the efficiency is at 74.67%. Overall the mean value of the efficiency is 72.4% with standard deviation of 0.99%. It can be seen that with time the efficiency in Figure 5.14 is starting to have a positive slope, this indicates the Bricks will have high efficiencies with time even though they are under elevated temperatures and currents, which is a positive outcome.

As part of quality check, to see all the criteria listed in Table 3.1 must be passed on all the Bricks before they're shipped to CERN for assembly, where the LVPS Brick,

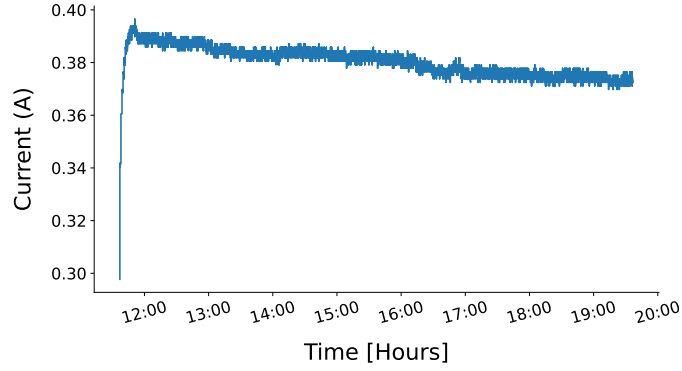


Figure 5.13: Input current drawn by the Brick spanning for 8 hours during burn-in process.

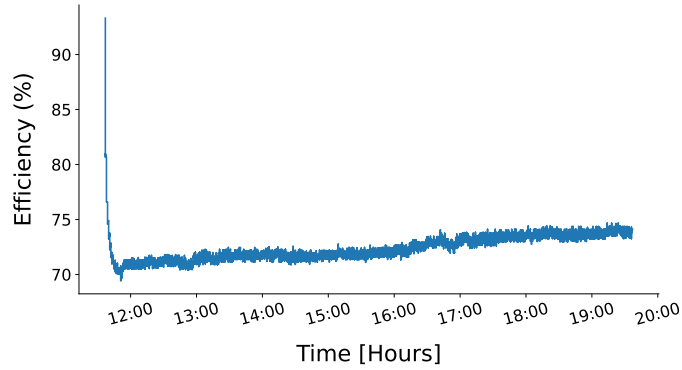


Figure 5.14: Efficiency of the brick spanning for 8 hours during the burn-in station

which will be enclosed in the LVPS Box will be tested in vertical slice test. The vertical slice test will involve a realistic load, i.e., Main board and Daughter board, the fuse board, and the ELMB mother board prototypes. For quality assurances, we will perform pre-production, which involves around 100 Brick prototypes which will help in having a clear production line and setup and sort out any issues that may arise before we head to main production. In the main production there will be over thousand Bricks which will be required to be tested according to criteria listed in Table 3.1.

This findings while preliminary, suggests that the Brick underwent a successful burn-in process and passed all the requirement according the both Table 4.1 and 3.1.

Appendix A

Supplementary Information

The schematic of the BI board provided in Figure A.1 was instrumental in creation of the actual eight boards and also with simulations. It is vital to check out if the pins of the PIC16F883 corresponds with what is written on the code. Therefore, it we used Table A.1 as a reference. The Table describes what each pin function it is, and the data type it receives (input) or transmits (output). We also show the graphical representation of the preliminary results of the burn-in process.

Table A.1: PIC16F883 pinout description

Name	Function	Input Type	Output Type	Description
RA0/AN0/ULPWU/C12IN0-	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
RA1/AN1/C12IN1-	RA1	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	AN1	AN	—	A/D Channel 1 input.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
RA2/AN2/VREF-/CVREF/C2IN+	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2.
	VREF-	AN	—	A/D Negative Voltage Reference input.
	CVREF	—	AN	Comparator Voltage Reference output.
	C2IN+	AN	—	Comparator C2 positive input.
RA3/AN3/VREF+/C1IN+	RA3	TTL	—	General purpose I/O.
	AN3	AN	—	A/D Channel 3.

	VREF +	AN	—	Programming voltage.
	C1IN+	AN	—	Comparator C1 positive input.
RA4/T0CKI/C1OUT	RA4	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	T0CKI	ST	—	Timer0 clock input.
	C1OUT	—	CMOS	Comparator C1 output.
RA5/AN4/SS/C2OUT	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4.
	SS	ST	—	Slave Select input.
	C2OUT	—	CMOS	Comparator C2 output.
RA6/OSC2/CLKOUT	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Master Clear with internal pull-up.
	CLKOUT	—	CMOS	F OSC /4 output.
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	External clock input/RC oscillator connection.
RB0/AN12/INT	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12.

	INT	ST	—	External interrupt.
RB1/AN10/P1C/C12IN3-	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10.
	P1C	—	CMOS	PWM output.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
RB2/AN8/P1B	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8.
	P1B	—	CMOS	PWM output.
RB3/AN9/PGM/C12IN2-	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9.
	PGM	ST	—	Low-voltage ICSPTM Programming enable pin.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
RB4/AN11/P1D	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.

	AN11	AN	—	A/D Channel 11.
	P1D	—	CMOS	PWM output.
RB5/AN13/T1G	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN13	AN	—	A/D Channel 13.
	T1G	ST	—	Timer1 Gate input.
RB6/ICSPCLK	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/ICSPDAT	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSPTM Data I/O.
RC0/T1OSO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	T1OSO	—	CMOS	Timer1 oscillator output.
	T1CKI	ST	—	Timer1 clock input.
RC1/T1OSI/CCP2	RC1	ST	CMOS	General purpose I/O.
	T1OSI	ST	—	Timer1 oscillator input.

	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/P1A/CCP1	RC2	ST	CMOS	General purpose I/O.
	P1A	—	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/SCK/SCL	RC3	ST	CMOS	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
	SCL	ST	OD	I 2 C TM clock.
RC4/SDI/SDA	RC4	ST	CMOS	General purpose I/O.
	SDI	ST	—	SPI data input.
	SDA	ST	OD	I 2 C data input/output.
RC5/SDO	RC5	ST	CMOS	General purpose I/O.
	SDO	—	CMOS	SPI data output. ¹
RC6/TX/CK	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
RC7/RX/DT	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	EUSART asynchronous input.

	DT	ST	CMOS	EUSART synchronous data.
RE3/MCLR/V PP	RE3	TTL	—	General purpose input.
	MCLR	ST	—	Master Clear with internal pull-up.
	V PP	HV	—	Programming voltage.
V SS	V SS	Power	—	Ground reference.
V DD	V DD	Power	—	Positive supply.
Legend: • AN = Analog input or output • TTL = TTL compatible input • OD = Open Drain • HV = High Voltage • XTAL = Crystal • CMOS = CMOS compatible input or output • ST = Schmitt Trigger input with CMOS levels				

This marco runs in the MPLAB X IDE and CCS compiler, it is used to create a machine code (.Hex file), which is dumped into PIC firmware to pass instructions. The code is developed in the embedded C programming language. C is a high level language, and one of the advantages of adopting a high-level programming language is that it is simple to comprehend. Header files (defined by the ‘.h’ on the end of the filename) are used to define and addresses that are used across several different files. Instead of defining these variables in each file, we put them all into a header file and just ‘include’ the header (using the statement `#include`) on the top of each file. The header file always placed at the top, see the marco A.1. This is known as a preprocessor directive and it tells the compiler to include certain definitions specified in another file. We have configuration bits used as attributes in PIC MCU, and they simply tells how the PIC is affected and they can be found in a datasheet of the PIC16F883 [4]. When we use embedded C, we have one main program that starts and takes the shape of any other C function. The first word in any function specifies the function’s output. The main function is contained within a while loop and is executed using case structures.

```
1
2  #include <176F883.h>
3  #use delay (clock=16000000)
4  #fuses NOWDT,HS, PUT, NOPROTECT, BROWNOUT, NOLVP, NOCPD, NOWRT,
   NODEBUG
5  #use rs232 (baud=9600, xmit=PIN_C6, rcv=PIN_C7) // Jumpers: 8 to 11,
   7 to 12
6  #use fast_io (A)
7  #use fast_io (B)
8  #use fast_io (C)
9
```

```

10
11 #define BUFFER_SIZE 32
12 BYTE buffer[BUFFER_SIZE];
13 BYTE next_in = 0;
14 BYTE next_out = 0;
15 int32 adc_value;
16 float adc_volt;
17 char x;
18
19 #int_rda
20 void serial_isr() {
21     int t;
22
23     buffer[next_in]= getc();
24     t=next_in;
25     next_in=(next_in+1) % BUFFER_SIZE;
26     if(next_in==next_out)
27         next_in=t;           // Buffer full !!
28 }
29
30 #define bkbhit (next_in!=next_out)
31
32 BYTE bgetc() {
33     BYTE c;
34
35     while(!bkbhit) ;
36     c=buffer[next_out];
37     next_out=(next_out+1) % BUFFER_SIZE;
38     return(c);
39 }
40
41 /*-----*/
42 /* LTC2449 drivers */

```

```

43  /*-----*/
44
45
46  #define ADC_CLK  PIN_A0
47  #define ADC_DOUT PIN_A1
48  #define ADC_DIN  PIN_A3
49  #define ADC_CS   PIN_A2
50
51
52  void ADCInit() {
53      output_high(ADC_CS);
54      output_low(ADC_CLK);
55  }
56
57  int ADC_Is_Busy(void)
58  {
59      byte b;
60      b=input_c();
61      return(bit_test(b,0));
62  }
63
64  #define ADC_CS_Low()  output_low(ADC_CS)
65  #define ADC_CS_High() output_high(ADC_CS)
66
67  byte ShiftDataByte(byte x)
68  {
69      int i,j;
70      byte dout;
71      byte din;
72      byte b;
73
74      din=x;
75      dout=0;

```

```

76     delay_us(2);
77     for(i=8; i>0; i--) {
78         j=i-1;
79         if(bit_test(din,j))
80             {
81                 output_high(ADC_DIN);
82             }
83         else
84             {
85                 output_low(ADC_DIN);
86             }
87         b=input_a();
88         if(bit_test(b,1))
89             {
90                 bit_set(dout,j);
91             }
92         else
93             {
94                 bit_clear(dout,j);
95             }
96
97         delay_us(2);
98         output_high(ADC_CLK);
99         delay_us(50);
100        output_low(ADC_CLK);
101        delay_us(50);
102    }
103    return(dout);
104 }
105
106 void ADC_Mux_Set(byte x)
107 {
108     byte din_mode;

```

```

109     byte  din_speed;
110     byte  data1 ,data2 ,data3 ,data4;
111     byte  sign;
112
113
114     din_mode=x & 0x1f;
115     din_mode|=0xA0;
116     din_speed=0x80;
117     /*
118     printf(" Mode  %x\n\r",din_mode);
119     printf(" Speed  %x\n\r",din_speed);
120     */
121     while(ADC_Is_Busy());
122
123     ADC_CS_Low();
124
125     data4=ShiftDataByte(din_mode);
126     data3=ShiftDataByte(din_speed);
127     data2=ShiftDataByte(0);
128     data1=ShiftDataByte(0);
129
130     /*
131     data4=ShiftDataByte(0xaa);
132     data3=ShiftDataByte(0xaa);
133     data2=ShiftDataByte(0xaa);
134     data1=ShiftDataByte(0xaa);
135     */
136
137     ADC_CS_High();
138     /*
139     printf(" Data 1  %x",data4);
140     printf("%x",data3);
141     printf("%x",data2);

```

```

142     printf("%x\n\r",data1);
143     */
144     sign=0;
145     if (!bit_test(data4,5))
146     {
147         data1=~data1;
148         data2=~data2;
149         data3=~data3;
150         data4=~data4;
151         sign=1;
152     }
153
154     bit_clear(data4,7);
155     bit_clear(data4,6);
156     bit_clear(data4,5);
157     /*
158     printf("Data 2 %x",data4);
159     printf("%x",data3);
160     printf("%x",data2);
161     printf("%x\n\r",data1);
162     */
163     adc_value=data4;
164     adc_value<<=8;
165     adc_value|=data3;
166     adc_value<<=8;
167     adc_value|=data2;
168     adc_value<<=8;
169     adc_value|=data1;
170
171     adc_value>>=13;
172     adc_volt=(2.5*adc_value)/65535;
173     if (sign==1) adc_volt*=-1.0;
174

```

```

175     }
176
177     void ADCCConvert(void)
178     {
179     }
180
181     void PrintADC(void)
182     {
183         char s[10];
184         int i;
185         char sum;
186         ADCCConvert();
187
188         sprintf(s, "%02.6f ", adc_volt);
189         for (i=0; i<8; i++) sum+=s[i];
190         sum&=0x7;
191         s[8]=sum|0x30;
192         s[9]=0;
193         printf("%s", s);
194     }
195
196     void PrintADC_U(void)
197     {
198         ADCCConvert();
199         printf("%02.8f\n\r", adc_volt);
200     }
201
202     void ReadADCDiff(byte x)
203     {
204         byte addr=0;
205
206         if (bit_test(x,0)) addr=8;
207         x>>=1;

```



```

208     x&=0x7;
209     addr|=x;
210     ADC_Mux_Set(addr);
211 }
212
213 void ReadADC(byte x)
214 {
215     byte addr=0;
216
217     if (bit_test(x,0)) addr=8;
218     x>>=1;
219     x&=0x7;
220     addr|=x;
221     addr|=0x10;
222     ADC_Mux_Set(addr);
223 }
224
225 void DACInit()
226 {
227     setup_timer_2(T2_DIV_BY_1, 0x3f, 1);
228     setup_ccp1(CCP_PWM);
229     setup_ccp2(CCP_PWM);
230     set_pwm1_duty(0);
231     set_pwm2_duty(0);
232 }
233 #define TLV_DATA_L() output_high(PIN_B4)
234 #define TLV_DATA_H() output_low(PIN_B4)
235
236 #define TLV_CLK_L() output_high(PIN_B5)
237 #define TLV_CLK_H() output_low(PIN_B5)
238
239 #define TLV_LOAD_L() output_high(PIN_B6)
240 #define TLV_LOAD_H() output_low(PIN_B6)

```

```

241
242 #define TLV_LDACL() output_low(PIN_B7)
243 #define TLV_LDACH() output_high(PIN_B7)
244
245 #define DACTIME 500
246
247 void TLVDACInit()
248 {
249     TLV_LDACH();
250     TLV_DATA_L();
251     TLV_CLK_L();
252     TLV_LOAD_H();
253     delay_us(DACTIME);
254     delay_us(DACTIME);
255 }
256
257 void TLVDACOut(byte addr, byte data)
258 {
259     int i;
260     // Address send
261     if (bit_test(addr, 1))
262     {
263         TLV_DATA_H();
264     }
265     else
266     {
267         TLV_DATA_L();
268     }
269     delay_us(DACTIME);
270     TLV_CLK_H();
271     delay_us(DACTIME);
272     TLV_CLK_L();
273     delay_us(DACTIME);

```

```

274
275     if ( bit_test ( addr , 0 )
276     {
277         TLV_DATA_H() ;
278     }
279     else
280     {
281         TLV_DATA_L() ;
282     }
283     delay_us ( DACTIME ) ;
284     TLV_CLK_H() ;
285     delay_us ( DACTIME ) ;
286     TLV_CLK_L() ;
287     delay_us ( DACTIME ) ;
288     // RNG bit is zero
289     TLV_DATA_L() ;
290     delay_us ( DACTIME ) ;
291     TLV_CLK_H() ;
292     delay_us ( DACTIME ) ;
293     TLV_CLK_L() ;
294     delay_us ( DACTIME ) ;
295     // Data send
296     for ( i = 8 ; i > 0 ; i -- )
297     {
298         if ( bit_test ( data , i - 1 ) )
299             TLV_DATA_H() ;
300         else
301             TLV_DATA_L() ;
302         delay_us ( DACTIME ) ;
303         TLV_CLK_H() ;
304         delay_us ( DACTIME ) ;
305         TLV_CLK_L() ;
306         delay_us ( DACTIME ) ;

```

```

307     }
308
309     TLV_LOAD_L();
310     delay_us(DACTIME);
311     TLV_LOAD_H();
312     delay_us(DACTIME);
313     TLV_LDACL();
314     delay_us(DACTIME);
315     TLV_LDACH();
316     delay_us(DACTIME);
317 }
318
319 int GetXChar(byte *x)
320 {
321     long timeout;
322     timeout=100;
323     *x=0;
324     while(! bkbhit)
325     {
326         delay_ms(1);
327         timeout--;
328         if (timeout==0) return(0);
329     }
330     *x=bgetc();
331     return(1);
332 }
333
334
335 #define SetOutputVoltage(x) set_pwm2_duty(x)
336 #define SetTrimVoltage(x) set_pwm1_duty(x)
337
338 #define BrickPowerOn() output_high(PIN_B0)
339 #define BrickPowerOff() output_low(PIN_B0)

```

```

340
341 #define BrickTermoOn() output_high(PIN_B1)
342 #define BrickTermoOff() output_low(PIN_B1)
343
344 #define Brick200VOn() output_high(PIN_B3)
345 #define Brick200VOff() output_low(PIN_B3)
346
347 #define BrickStart() output_low(PIN_B2)
348 #define BrickStop() output_high(PIN_B2)
349
350 #define TestLEDOn() output_high(PIN_A4)
351 #define TestLEDOff() output_low(PIN_A4)
352
353 void main()
354 {
355
356
357 setup_adc_ports(NO_ANALOGS);
358 setup_adc(ADC_OFF);
359
360 setup_spi(FALSE);
361 setup_timer_0(RTCC_INTERNAL|RTCC_DIV_1);
362
363 setup_timer_1(T1_DISABLED);
364 setup_timer_2(T2_DISABLED,0,1);
365
366 enable_interrupts(GLOBAL);
367 enable_interrupts(INT_RDA);
368
369 set_tris_a(0x22);
370 set_tris_b(0x0);
371 set_tris_c(0x81);
372 output_b(0);

```

```

373
374     ADCInit();
375     DACInit();
376     TLVDACInit();
377
378     while (1)
379     {
380         /*
381         ReadADC(0);
382         delay_us(100);
383         */
384         while (!bkbhit);
385         x=bgetc();
386         switch (x) {
387             case '1': BrickPowerOn(); break;
388             case '2': BrickPowerOff(); break;
389             case '3': Brick200VOn(); break;
390             case '4': Brick200VOff(); break;
391             case '5': BrickTermoOn(); break;
392             case '6': BrickTermoOff(); break;
393             case 'r': BrickStart(); break;
394             case 'o': BrickStop(); break;
395             case 'l': TestLEDOn(); break;
396             case 'h': TestLEDOff(); break;
397             case '9':
398                 if (GetXChar(&x)) output_b(x);
399                 break;
400             case 'a':
401                 if (GetXChar(&x)) SetOutputVoltage(x);
402                 break;
403             case 'b':
404                 if (GetXChar(&x)) SetTrimVoltage(x);
405                 break;

```

```

406         case 'g': /*Brick input current*/
407             ReadADCDiff(1);
408             ReadADCDiff(1);
409             PrintADC();
410             break;
411         case 'i': /* Current from 15V startup */
412             ReadADCDiff(14);
413             ReadADCDiff(14);
414             PrintADC();
415             break;
416         case 'p': /* Brick output voltage */
417             ReadADCDiff(6);
418             ReadADCDiff(6);
419             PrintADC();
420             break;
421         case 't': /* Brick input voltage */
422             ReadADCDiff(2);
423             ReadADCDiff(2);
424             PrintADC();
425             break;
426         case 's': /* Brick output current */
427             ReadADCDiff(4);
428             ReadADCDiff(4);
429             PrintADC();
430             break;
431         /*      case 'e': /* Temp 1 */
432             ReadADCDiff(10);
433             ReadADCDiff(10);
434             PrintADC();
435             break; */
436         case 'f': /* Temp 2 */
437             ReadADCDiff(12);
438             ReadADCDiff(12);

```

```

439         PrintADC();
440         break;
441     case 'm': /* Temp 3 */
442         ReadADCDiff(8);
443         ReadADCDiff(8);
444         PrintADC();
445         break;
446     case 'z':
447         if (GetXChar(&x)) TLVDACOut(0,x);
448         break;
449     case 'x':
450         if (GetXChar(&x)) TLVDACOut(1,x);
451         break;
452     case 'c':
453         if (GetXChar(&x)) TLVDACOut(2,x);
454         break;
455     case 'v':
456         if (GetXChar(&x)) TLVDACOut(3,x);
457         break;
458     case 'n':
459         TLVDACOut(0,0);
460         TLVDACOut(1,0);
461         TLVDACOut(2,0);
462         TLVDACOut(3,0);
463         break;
464         break;
465     case 'G': /*Brick input current*/
466         ReadADCDiff(1);
467         ReadADCDiff(1);
468         PrintADC_U();
469         break;
470     case 'I': /* Current from 15V startup */
471         ReadADCDiff(14);

```



```

472         ReadADCDiff(14);
473         PrintADC_U();
474         break;
475     case 'P': /* Brick output voltage */
476         ReadADCDiff(6);
477         ReadADCDiff(6);
478         PrintADC_U();
479         break;
480     case 'T': /* Brick input voltage */
481         ReadADCDiff(2);
482         ReadADCDiff(2);
483         PrintADC_U();
484         break;
485     case 'S': /* Brick output current */
486         ReadADCDiff(4);
487         ReadADCDiff(4);
488         PrintADC_U();
489         break;
490     /*case 'E': /* Temp 1 */
491         ReadADCDiff(10);
492         ReadADCDiff(10);
493         PrintADC_U();
494         break;*/
495     case 'F': /* Temp 2 */
496         ReadADCDiff(12);
497         ReadADCDiff(12);
498         PrintADC_U();
499         break;
500     case 'M': /* Temp 3 */
501         ReadADCDiff(8);
502         ReadADCDiff(8);
503         PrintADC_U();
504         break;

```

```

505     case 'd':
506         if (GetXChar(&x))
507             {
508                 ReadADC(x);
509                 ReadADC(x);
510                 PrintADC();
511             }
512         break;
513     case 'D':
514         if (GetXChar(&x))
515             {
516                 ReadADCDiff(x);
517                 ReadADCDiff(x);
518                 PrintADC();
519             }
520         break;
521     case 'w':
522         if (GetXChar(&x))
523             {
524                 ReadADC(x);
525                 ReadADC(x);
526                 PrintADC_U();
527             }
528         break;
529     case 'W':
530         if (GetXChar(&x))
531             {
532                 ReadADCDiff(x);
533                 ReadADCDiff(x);
534                 PrintADC_U();
535             }
536         break;

```

```

537         case 'q': /* Module Address, should change and be unique for
each module 1-63 */
538             printf("39");
539             break;
540         default ;;
541     }
542     x=0;
543
544 }
545
546 }

```

Listing A.1: C-code used to create .Hex file that is flashed to PIC for burn-in Interface Board

Table A.2: The preliminary results from the burn-in test station with one Brick operation. There are 11 parameters recorded during each test. The measurements were recorded over a span of eight hours with 2 seconds sampling rate.

T2[°C]	T3[°C]	VinHV[V]	VinBrick[V]	IinBrick[A]	VoutBrick[V]	IoutBrick[A]	VoutLoad[V]	Iload[A]	Iset[A]	Eff[%]
20.36	17.52	200	200.97	0.29	11.01	5.11	11.076	4.98	5.0	93.59
21.46	17.97	200	200.97	0.30	11.01	5.10	11.06	4.97	5.0	92.77
22.83	18.49	200	200.97	0.30	11.01	5.10	11.08	4.96	5.0	92.66
24.08	18.95	200	200.97	0.30	11.01	5.10	11.08	4.97	5.0	91.95
25.17	19.35	200	200.97	0.30	11.01	5.10	11.08	4.96	5.0	91.92
26.13	19.71	200	200.97	0.30	11.01	5.09	11.08	4.96	5.0	91.84
26.93	20.02	200	200.97	0.30	11.01	5.09	11.08	4.96	5.0	91.85
27.66	20.32	200	200.97	0.30	11.01	5.09	11.08	4.96	5.0	91.77
28.31	20.59	200	200.98	0.30	11.01	5.09	11.08	4.96	5.0	91.78
28.89	20.83	200	200.98	0.30	11.01	5.09	11.08	4.95	5.0	91.04
29.41	21.06	200	200.98	0.30	11.01	5.09	11.08	4.95	5.0	91.01
29.87	21.27	200	200.98	0.30	11.01	5.08	11.08	4.96	5.0	91.078
30.29	21.47	200	200.98	0.30	11.01	5.08	11.08	4.95	5.0	90.37
30.67	21.65	200	200.97	0.30	11.01	5.08	11.08	4.95	5.0	89.66

31.02	21.83	200	200.98	0.30	11.01	5.08	11.08	4.95	5.0	89.70
31.34	21.98	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	88.38
31.63	22.12	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	88.28
31.89	22.26	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	87.64
32.13	22.40	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.54
32.36	22.52	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	87.61
32.57	22.64	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.55
32.77	22.75	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	88.22
32.95	22.86	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	88.95
33.12	22.97	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	88.88
33.28	23.07	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	88.84
33.44	23.16	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	88.303
33.60	23.24	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	86.90
33.73	23.33	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	86.90
33.86	23.40	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.54
33.98	23.48	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.54
34.10	23.56	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.54

34.21	23.64	200	200.97	0.31	11.01	5.08	11.08	4.94	5.0	87.58
34.32	23.71	200	200.97	0.31	11.01	5.08	11.08	4.95	5.0	87.66
34.43	23.77	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.33
34.53	23.84	200	200.97	0.32	11.01	5.08	11.09	4.95	5.0	86.40
34.63	23.91	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.67
34.72	23.96	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.33
34.80	24.02	200	200.97	0.31	11.01	5.08	11.09	4.94	5.0	86.97
34.90	24.08	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.61
34.98	24.15	200	200.97	0.32	11.01	5.08	11.09	4.95	5.0	85.76
35.06	24.19	200	200.97	0.31	11.01	5.08	11.09	4.95	5.0	87.01
35.14	24.25	200	200.97	0.31	11.01	5.08	11.09	4.94	5.0	86.87
35.21	24.31	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.31
35.29	24.36	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.28
35.36	24.41	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.73
35.43	24.46	200	200.97	0.32	11.01	5.08	11.09	4.95	5.0	86.39
35.49	24.51	200	200.97	0.31	11.01	5.08	11.09	4.94	5.0	86.88
35.56	24.56	200	200.97	0.31	11.01	5.08	11.09	4.94	5.0	86.89

35.62	24.61	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.29
35.69	24.66	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.03
35.75	24.68	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.71
35.81	24.73	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.11
35.87	24.77	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.75
35.92	24.81	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.11
35.98	24.84	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.75
36.03	24.87	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.08
36.08	24.90	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.27
36.14	24.93	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.12
36.18	24.97	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.15
36.23	25.00	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.72
36.27	25.02	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.76
36.32	25.06	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.28
36.37	25.09	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.12
36.41	25.11	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.66
36.45	25.14	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.66

36.49	25.17	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.66
36.53	25.19	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.06
36.56	25.21	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	86.32
36.60	25.25	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.70
36.64	25.26	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.63
36.68	25.30	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.67
36.71	25.32	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.14
36.75	25.35	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.17
36.79	25.37	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	84.57
36.83	25.38	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	84.57
36.87	25.41	200	200.97	0.33	11.001	5.08	11.10	4.94	5.0	83.97
36.90	25.42	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	84.57
36.93	25.43	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	84.53
36.97	25.45	200	200.97	0.32	11.01	5.08	11.09	4.94	5.0	85.04
36.99	25.46	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.11
37.02	25.49	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.14
37.06	25.50	200	200.97	0.33	11.01	5.08	11.10	4.94	5.0	83.87

37.09	25.53	200	200.97	0.33	11.01	5.08	11.10	4.94	5.0	83.94
37.12	25.54	200	200.97	0.33	11.01	5.08	11.10	4.94	5.0	83.91
37.14	25.56	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	84.47
37.16	25.58	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.10
37.19	25.59	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.05
37.22	25.61	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.05
37.25	25.62	200	200.97	0.32	11.01	5.08	11.10	4.94	5.0	85.19

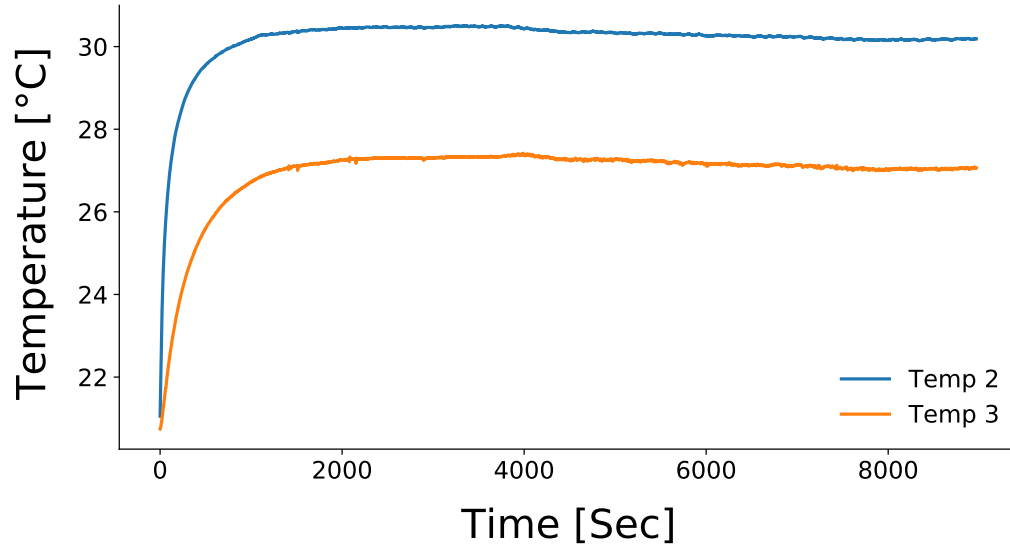


Figure A.2: Temperature measurements at two regions on the Brick during burn-in process

The results shown in Table A.2 are just a sample, as it not feasible to include the entire data, however they represented graphically in the following Figures: A.2, A.3 and A.4.

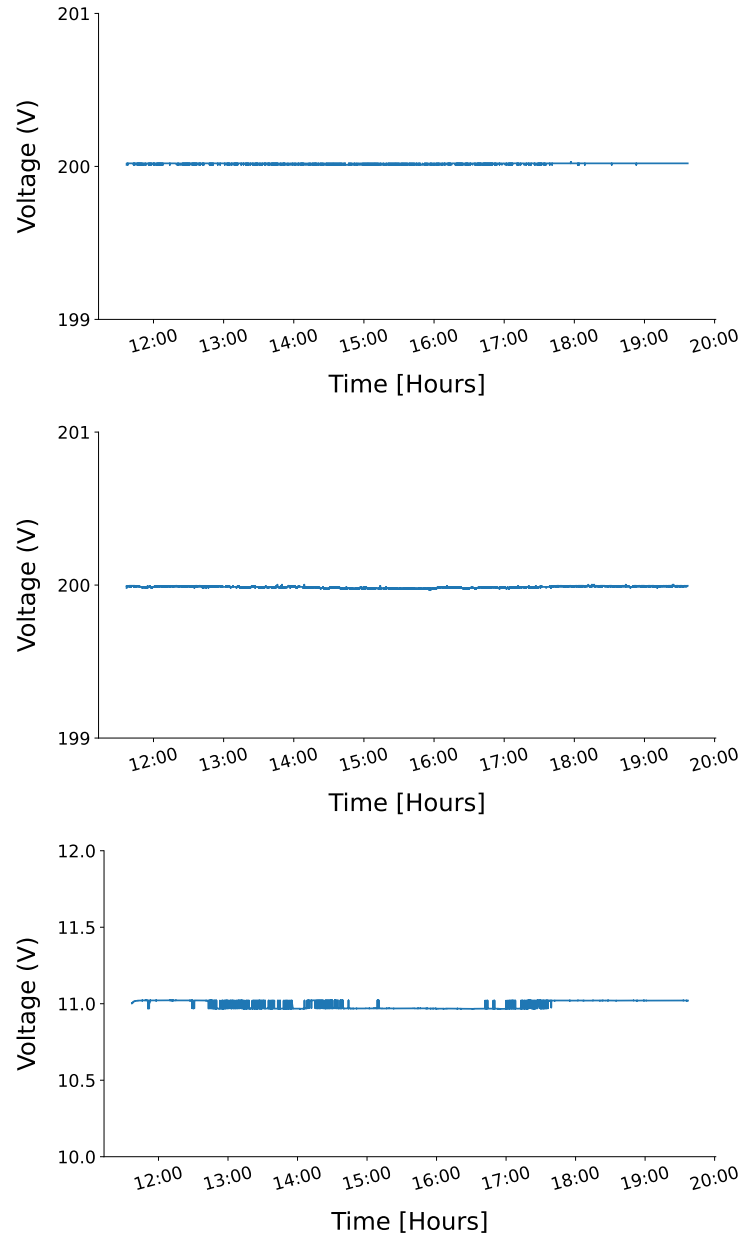


Figure A.3: Graphical representation of the data recorded during the burn-in of a Brick. Top: Input voltage delivered to the LVPS Brick from the power supply. middle: Input voltage from the Brick and received by the BI board. Bottom: Output voltage from the load.

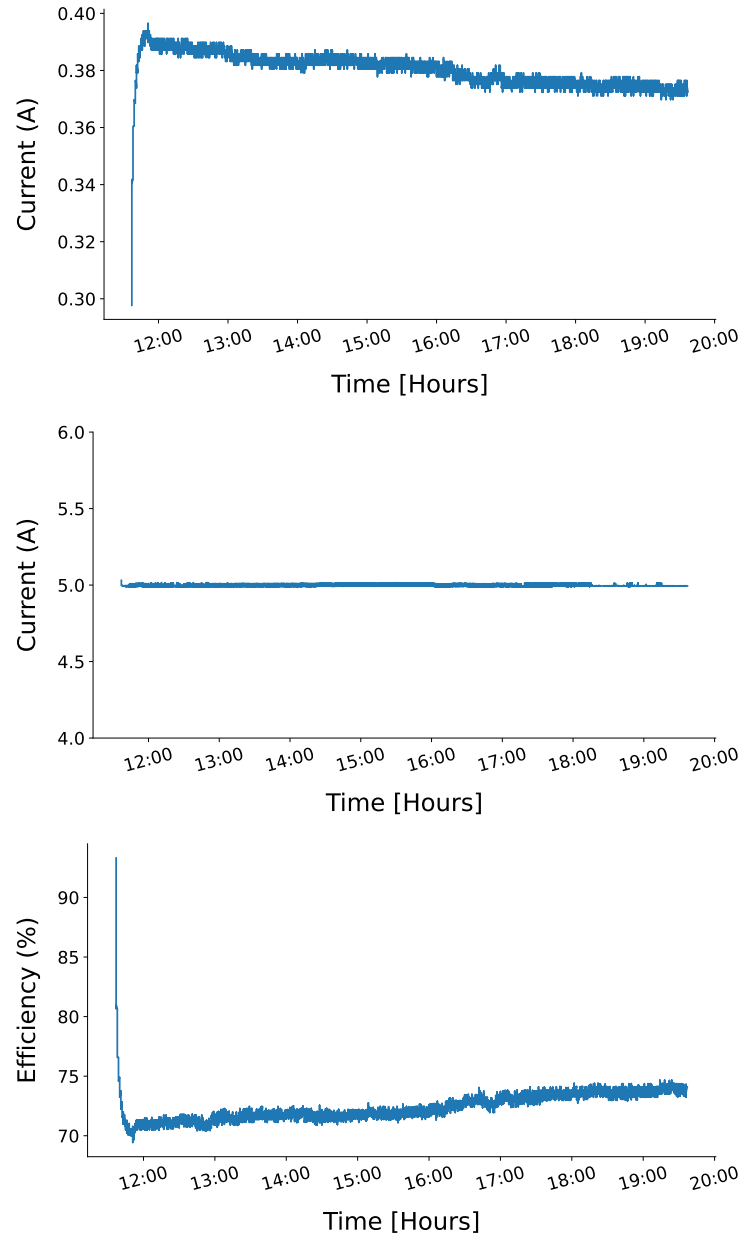


Figure A.4: Graphical representation of the data recorded during the burn-in of a Brick. Top: Input current the Brick receives from the Brick interface board. Middle: Output current sent from the dummy load board to load interface board. Bottom: The efficiency of the Brick.

Appendix B

The LabVIEW basics

LabVIEW programs are called Virtual Instrument (VI)s. Each VI contains three main components:

- Front Panel - How the user interacts with the VI
- Block Diagram - The code that controls the program
- Icon/Connector - means of connecting a VI to other VIs

When the software is running, the Front Panel is used to interact with the user. The software can be controlled, inputs can be changed, and data can be updated in real time. On the block diagram, each front panel control or indicator has a corresponding terminal. Values from controls move through the block diagram, where they are employed in the functions on the diagram, and the results are provided to other functions or indicators when a VI is run. The VI's user interface is the front panel. Controls and indicators, which are the VI's interactive input and output terminals, respectively, are used to construct the front panel. Knobs, push buttons, dials, and other input devices are examples of controls. Graphs, LEDs, and other displays are examples of indicators. Controls are used to replicate instrument input devices and provide data to the VI's block diagram. Indicators represent instrument output de-

vices and display data acquired or generated by the block diagram.

This graphical source code can be found in the block diagram. On the block diagram, front panel items show as terminals. The block diagram also includes functions and structures from the LabVIEW VI libraries. Each node on the block diagram, including control and indicator terminals, functions, and structures, is connected by wires. A terminal is created on the Block Diagram when you create an object on the Front Panel. From the Block Diagram code, these terminals provide access to the Front Panel objects. Each terminal includes information about the Front Panel object to which it is assigned. The data type, for example, is determined by the colour and symbols. Orange terminals and the initials DBL are used to signify double precision floating-point numbers. The True/False (TF) writing on the Boolean terminals is green. In general, orange terminals should be connected to other orange terminals, green terminals to green terminals, and so on. This isn't a hard-and-fast rule; for example, LabVIEW will let you link a blue (integer) terminal to an orange (fractional) terminal. In most circumstances, though, seek for a colour match. Controls have a thick border and an arrow on the right side. Indicators feature a small border and a left-hand arrow. In LabVIEW, logic principles apply to wiring: Each wire must have one (but only one) source (or control) and many destinations (or indicators).

For running VIs, LabVIEW uses a dataflow model. When all of the inputs to a block diagram node are available, it executes. When a node finishes its execution, it sends data to its output terminals and then to the next node in the dataflow pipeline. The control flow concept of program execution is used by Visual Basic, C++, JAVA, and most other text-based programming languages. The execution order of a program is determined by the sequential sequence of program elements in control flow. In the block diagram, the LabVIEW source code is read from left to right. All LabVIEW

	Scalar	1D Array	2D Array		Cluster
Numeric				Orange (floating point)	 Brown
				Blue (integer)	 Brown
Boolean				Green	 Pink
String				Pink	 Pink
Path				Dark Green	 Pink
Reference				Dark Green	 Pink
Hardware Resource				Purple	 Pink
Variant				Purple	 Pink
Waveform				Brown	 Pink
Class				Red	 Pink

Figure B.1: Wiretypes for the LabVIEW control software.

programming elements, such as controls, indicators, and functions, are connected in the block diagram. This is accomplished through the use of "wires" shown in Figure B.1. These wires can be thought of as conduits for data.

Note: The colour of a class wire is customizable. The table above shows its default appearance.

Each wire has a single data source, but it is possible to wire it to many VIs and functions that read the data. Wires are different colors, styles, and thicknesses, depending on their data types as shown above. They may be:

- Numeric integer (Blue)
- Numeric floating-point (Orange)
- Boolean (Green)

The appearance of the wire indicates whether it is a scalar, a 1D array, or a 2D array.

B.0.0.1 Block diagram

Block diagram objects include terminals, sub-VIs, functions, constants, structures, and wires, which transfer data among other block diagram objects. The list below shows components and description that makes up the block diagram:

- **Terminals** - The entry and exit ports that communicate information between the front panel and the block diagram are known as terminals. You may save space by seeing terminals as icons.
- **Nodes** - When a VI runs, nodes are block diagram objects with inputs and/or outputs that conduct operation. In text-based programming languages, nodes are similar to statements, operators, functions, and subroutines. Functions or structures can be nodes
- **VI that runs on the block diagram of another VI.** They have a front panel and block diagrams. Any VI can function as a subVI. The front panel and block diagram open when you double-click a subVI.
- **Icon** - VIs are represented graphically by icons. As the icon that shows when you position the subVI on a diagram, use the icon from the upper-right corner of the front panel.
- **Connector Pane** - The connection pane is a diagram of a VI's inputs and outputs. The connection pane terminal relates to the VI's front panel controls and indicators. The connection pane is not accessible from the block diagram window.
- **Express Vi** -Express VIs are a type of subVI that you conjure with dialog boxes. Icons for the Express VIs appear on the block diagram as icons surrounded by a blue field

B.0.0.2 Dataflow

Data flow is the movement of data through the nodes of a block diagram. In textual languages, things tend to go sequentially from top to bottom depending on the order that they're written in the line of text. In LabVIEW, things go sequentially from top to bottom according on the order that they're written in the line of text. It's all about how things are connected together in LabVIEW.

There are two rules:

1. When nodes get all of their required inputs, they execute.
2. When a node executes, the output data is passed on to the next node.

We also use error wires to connect different nodes so that we may figure out the data flow of the program as needed. When hovering over a subVI, the needed terminals are shown in bold in the context assistance box. Recommended or optional for terminal inputs and outputs means that even if the recommended or optional terminals are not wired, the block diagram on which the subVI is placed can run. Optional terminals are not explicitly listed in the context help box.

The schematic of the BI board provided in Figure A.1 was instrumental in creation of the actual eight boards and also with simulations. It is vital to check out if the pins of the PIC16F883 corresponds with what is written on the code. Therefore, it we used Table A.1 as a reference. The Table describes what each pin function it is, and the data type it receives (input) or transmits (output). We also show the graphical representation of the preliminary results of the burn-in process.

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