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A high throughput ADC system for the PROMETEO test-bench of the ATLAS Tile Calorimeter



Matthew Spoor
University of the Witwatersrand

A thesis submitted for the degree of
Master of Science

Johannesburg, 2020

Declaration

I declare that this Dissertation is a result of my own work, except where explicit reference is made to the work of others. It is being submitted for the Degree of Master of Science at the University of the Witwatersrand, Johannesburg. It has not been submitted before for any qualification or examination at any other University.

Related research output:

- M Spoor, B Mellado, "The ATLAS Tile Calorimeter Hybrid Demonstrator", SAIP 2014, pp. 257-262, 2014, ISBN: 978-0-620-65391-6.
- O. Kureba, X. Ruan, M. Spoor, M. Govender, I. Hofsajer, and B. Mellado, "An electronics test-bench for the certification of the Tile Calorimeter of the ATLAS detector", SAIP, 2015, ISBN: 978-0-620-70714-5.
- M. Spoor, O. Kureba, and C. Sandrock, "Development of a high data-throughput ADC board for the PROMETEO portable test-bench for the upgraded front-end electronics of the ATLAS TileCal", J. Phys.: Conf. Ser., vol. 645, no. 012027, pp. 7, 2015, ISBN: 978-0-620-70714-5.
- M. Spoor and ATLAS Collaboration, "Upgrade of the ATLAS Tile hadronic calorimeter for high-luminosity LHC run", Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 845, pp. 537-541, 2017.



Matthew Spoor, 18^{th} of November 2020 in Johannesburg.

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Abstract

The Large Hadron Collider (LHC) is preparing for the High Luminosity upgrade (HL-LHC). The HL-LHC will give physicists the ability to probe new physics beyond the Standard Model (SM), examine electroweak symmetry in greater detail and to measure the properties of the Higgs boson and SM. During the Phase-II upgrade, the ATLAS Tile Calorimeter will need to undergo a complete redesign of its on and off-detector electronics. The PROMETEO (A Portable ReadOut ModulE for Tilecal ElectrOnics) stand-alone test-bench is under development to be used for the full certification of the new on-detector electronics of the TileCal. The test-bench has been designed to readout the digitised samples coming from the on-detector electronics to assess data quality in real-time and diagnose system malfunctions or errors. The system uses a Xilinx VC707 as a mainboard with a QSFP+ FMC module for the readout and control of the TileCal electronics. Functions performed by PROMETEO are provided by multiple custom daughterboards: High Voltage Board, LED Driver Board and a 16 channel ADC board. The ADC board is used to digitise the analog signals used for Level 1 Trigger system coming from the TileCal on-detector adder boards at bunch crossing frequency. This dissertation presents a custom ADC trigger board I designed and produced for the PROMETEO test-bench of the ATLAS TileCal. This includes the physical hardware design and production as well as the firmware needed to manage and readout the board on the FPGA of the VC707.

Contents

1 CERN, LHC and the ATLAS experiment **1**

1.1 CERN . . . 1

1.2 Large Hadron Collider . . . 2

1.2.1 LHC experiments . . . 4

1.3 The ATLAS Experiment . . . 5

1.3.1 The Inner detector . . . 6

1.3.1.1 Pixel detector . . . 7

1.3.1.2 Semiconductor Tracker . . . 8

1.3.1.3 Transition Radiation Tracker . . . 8

1.3.2 Calorimeters . . . 9

1.3.2.1 Electromagnetic Calorimetry . . . 10

1.3.2.2 Tile Calorimeter . . . 11

1.3.3 The Muon Spectrometer . . . 14

1.3.4 Magnetic Field . . . 15

1.3.5 The ATLAS Trigger and Data Acquisition System . . . 16

1.3.5.1 Level 1 Trigger . . . 16

1.3.5.2 Level 2 Trigger . . . 17

1.3.5.3 Event Filter . . . 18

2 The ATLAS Tile Hadronic Calorimeter Upgrade **19**

2.1 The HL-LHC . . . 19

2.2 ATLAS Trigger and data acquisition architecture . . . 21

2.3 TileCal Upgrade . . . 23

2.3.1 Current readout architecture . . . 24

2.4 Upgrade readout architecture . . . 25

2.4.1 Hybrid Demonstrator Module . . . 26

2.5 On-detector Electronics . . . 27

2.5.1 Front-end boards . . . 27

2.5.2 Mainboard . . . 29
2.5.3 Daughterboard . . . 30
2.6 Off-detector electronics . . . 32
2.6.1 Tile PreProcessor . . . 32
2.6.2 Tigger and DAQ interface . . . 33

3 Tile Calorimeter Test-Bench 34
3.1 Test-benches . . . 34
3.2 MobiDICK . . . 35
3.3 PROMETEO . . . 36
3.3.1 Mainboard . . . 37
3.3.2 Mini PC . . . 38
3.3.3 High Speed readout . . . 39
3.3.4 High Voltage board . . . 39
3.3.5 LED driver Board . . . 40
3.3.6 ADC Trigger board . . . 40
3.4 Front-end electronics tests . . . 42

4 ADC trigger board for the ATLAS TileCal PROMETEO 45
4.1 Study objectives . . . 45
4.2 Problem identification . . . 45
4.3 ADC Trigger Board Overview . . . 48
4.4 Circuit Design . . . 49
4.4.1 Power stage . . . 49
4.4.2 Analog stage . . . 50
4.4.3 Digital stage . . . 51
4.4.4 Reference Clock . . . 52
4.4.5 Printed Circuit Board . . . 53
4.5 Firmware . . . 55
4.5.1 Firmware Outline . . . 57
4.5.2 Firmware layout . . . 60
4.5.2.1 ISERDESE modules . . . 60
4.5.2.2 Configuration Module . . . 60
4.5.2.3 Alignment module . . . 62
4.5.2.4 Word Alignment . . . 62
4.5.2.5 Bit Alignment . . . 63
4.5.2.6 FIFO and IPBus . . . 64

4.6 ADC Prototyping and Testing 65
4.6.1 Firmware Simulations 67
4.6.2 System verification 70
4.6.2.1 ADC setup, configuration and signal alignment . . . 71
4.6.2.2 ADC channels analysis 73

5 Conclusions **81**
5.1 ADC trigger board 82

List of Figures **85**

A **89**

Chapter 1

CERN, LHC and the ATLAS experiment

Chapter 1 will introduce CERN, the Large Hadron Collider and the ATLAS experiment. A short description of the ATLAS subs-detectors will be discussed.

1.1 CERN

CERN (Organisation Européenne pour la Recherche Nucléaire) is the European Organisation for Nuclear Research. The organisation was established in 1952 with a mandate to establish a fundamental physics research organisation in Europe. CERN's main area of research is particle physics, the study of the fundamental components of matter and the forces that act upon them. Situated on the French-Swiss border near the city of Geneva, CERN is currently the largest particle physics laboratory in the world. The organisation is composed of 22 member states, 2633 permanent staff and accommodates over 12000 scientists, engineers, associates and fellows from around the world [1].

The most notable discoveries attributed to CERN are the W and Z bosons in 1984

and more recently the Higgs boson. In July 2012 the ATLAS and CMS experiments announced its discovery. A new sub-atomic particle with a mass approximately 125 GeV had been discovered [2]. The following year March it was confirmed to be the long theorised Higgs Boson. The boson was named after the physicist Peter Higgs. In 2013 Francis Englert and Peter Higgs received the Nobel prize in physics for the theoretical discovery of the Borut-Englert-Higgs mechanism, confirmed by the CMS and ATLAS experiments in 2012 [3][4].

1.2 Large Hadron Collider

The large Hadron Collider (LHC) [5], situated at CERN, is the worlds largest and most powerful particle accelerator. The LHC is housed in a circular tunnel 27 km in circumference, buried approximately 100 m below ground level, passing under the French-Swiss border near Geneva. The LHC ring comprises of two beam-pipes containing particles travelling in opposite directions, held in place using super-conducting magnets. Beams are accelerated up to and energy of 7 TeV and are collided at a total centre-of-mass energy of $\sqrt{s} = 13$ TeV, which delivers an instantaneous luminosity of $\mathcal{L}$=1 x $10^{34}\text{cm}^{-2}\text{s}^{-1}$. While the LHC is operating at peak luminosity there are 2808 bunches each containing $O(10^{11})$ protons that collide every 25 ns (40 MHz bunch crossing frequency) [6].

The LHC is the final stage in a chain of accelerators that incrementally increase the energy of the proton beams. Figure 1.1 shows the layout of the accelerator complex at CERN. Linac2 and the PS Booster form the first stage of the proton accelerator complex where beams reach an energy of 1.4. GeV. This beam is injected into the Proton Synchrotron (PS) to achieve an energy of 25 GeV. Next the beam is received by the Super Proton Synchrotron (SPS) where it is further accelerated

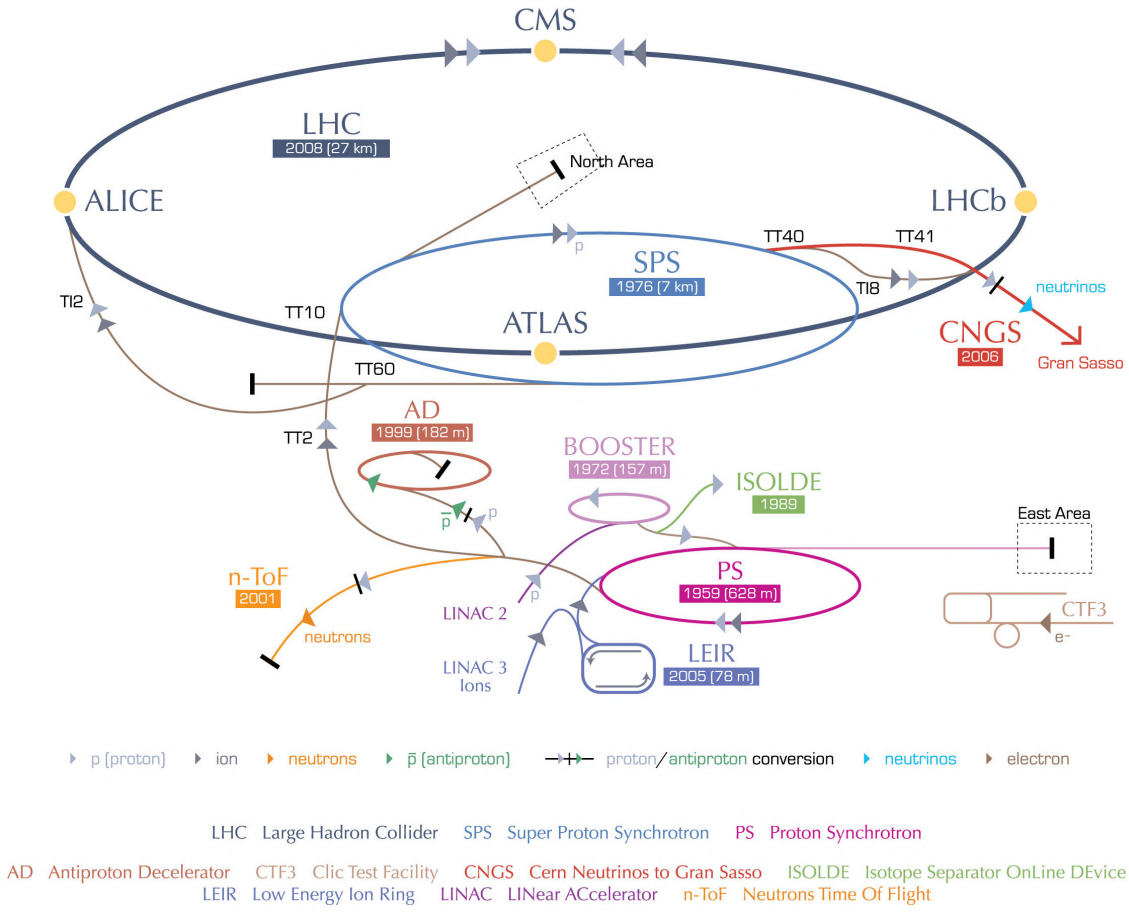


Figure 1.1: CERN Accelerator complex [7].

before finally being injected into the LHC ring with an energy of 450 GeV [5]. Within the LHC ring, beams are accelerated in two separate beam pipes to their maximum energy of 7 TeV using the Radio Frequency (RF) system. The particle beams are guided around the accelerator ring using strong magnetic fields (8 Tesla) that are maintained by a series of super-conducting electromagnets. The electromagnets are created using coils of specialised cable that can function in a superconducting state when cooled to exceptionally low temperatures. To maintain these temperatures the LHC is connected to a liquid helium distribution system which is able to keep the magnets at -271.1°C.

1.2.1 LHC experiments

There are a total of seven experiments installed around the LHC that are used to analyse particles produced during collisions. There are four interaction points along the LHC where the two beams-lines meet and particles are able to collide, corresponding to the four major experiments: ATLAS (A Toroidal LHC Apparatus), CMS (Compact Muons Solenoid), ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty).

ATLAS: ATLAS [8] is one of two general purpose proton-proton experiments at the LHC. The experiment was developed to exploit the full potential of the LHC at a TeV scale in order to study physics beyond the standard model. The design allows the experiment to measure the characteristics of strong and electroweak forces with a high degree of precision. A detailed description of ATLAS can be found in section 1.3.

CMS: CMS [9] is the second general purpose particle detector and it is found at the opposite side of LHC ring to ATLAS. The two experiments CMS and ATLAS shared the same design goals but were developed independently of one another. This allows the experiments to in verify any new results or discoveries that are made.

ALICE: ALICE is a experiment dedicated to measurement of heavy ions collisions in an effort to understand the phase of matter called quark-gluon plasma [10].

LHCb: LHCb was designed to investigate the differences between matter and antimatter in the universe [11].

Other Experiments: The three smaller experiments at the LHC include: TOTEM (TOTal Elastic and diffraction cross-section Measurement), LHCf (LHC forward) and

the MoEDAL (Monopole and Exotics Detector at the LHC). The TOTEM experiment is located near CMS and used to perform high-precision measurements of the total cross section, elastic scattering and diffraction dissociation [12]. LHCf is located near ATLAS and studies particle generated in the forward region of particle collisions. The detector is used to measure the energy and total number of neural pions produced in collisions in an effort to simulate cosmic rays in laboratory conditions [13]. MoEDAL is located on the walls of the CMS cavern and actively search for magnetic monopole and highly ionising massive particles. The detector was upgraded in 2015 but has been unable to detect magnetic monopole.

1.3 The ATLAS Experiment

The ATLAS (A Toroidal LHC Apparatus) experiment is the largest particle detector at the LHC [14]. The detector is approximately 45 meters in length, 25 meters in height and with a overall weight of about 7000 tonnes. It was designed as a general purpose detector that would detect proton-proton collisions at a centre-of-mass energy of 14 TeV at a bunch crossing frequency of 40 MHz. The general purpose design of ATLAS means that it should be able to measure the unique trace of any particle decay states that would occur during proton-proton collisions [6]. Primarily this would include: charged particles such as electrons, hadrons and muons; energy deposited through showering in the calorimeter systems; and track of muons leaving the detector.

The ATLAS detector uses a cylindrical design with end-caps on each end to enable complete coverage of the products of the collisions (Figure 1.2). The detector is comprised of four major components, each containing multiple sub-detectors that are positioned around a central interaction point (IP) where the two particle beams

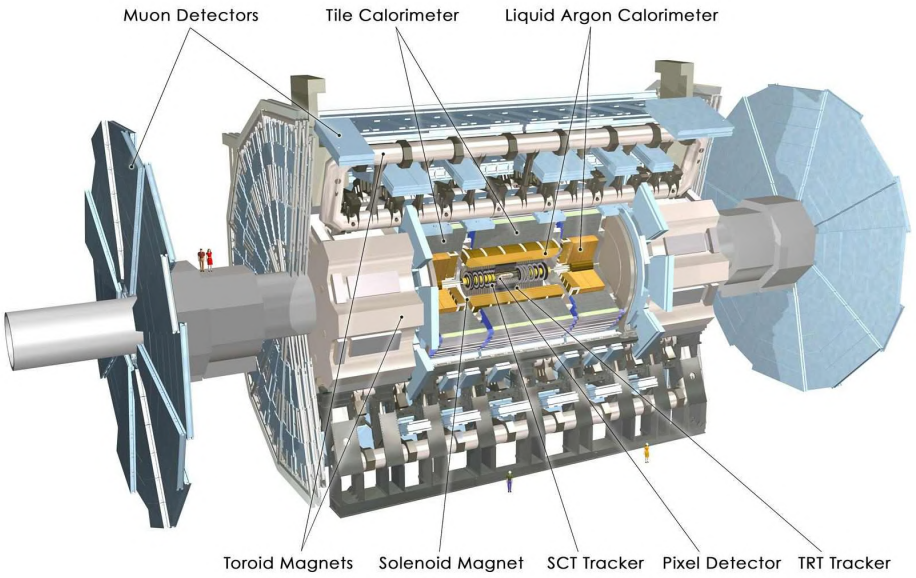


Figure 1.2: A schematic drawing of the ATLAS detector [15].

collide. The sections are of follows: Inner detector (ID), Calorimeters (Liquid Argon and Hadronic Tile Calorimeter), the Muon Spectrometer (MS) and the Magnet system. Descriptions of each components are given in the following subsections.

The ATLAS experiment uses the right-handed Cartesian coordinate system. The origin corresponds to the IP at the centre of the detector, the x-axis is points from the IP to the centre of the LHC ring, the z-axis or beam axis points along the beam line and the y-points upwards. When describing properties of the detector th following terms are used: Transverse Plane (x-y plane), Azimuthal angle ϕ (angle around the beam axis) and Pseudorapidity η = -ln(tan $(\theta/2)$) (θ is the polar angle between the beam-axis and particle). Figure 1.3 demonstrates the coordinate system in respect to the detector.

1.3.1 The Inner detector

The ID is located in the innermost section of ATLAS, spanning 7.0 m in length and 2.3 m in height figure 1.4. The detector encapsulates the beam-pipe, covering the

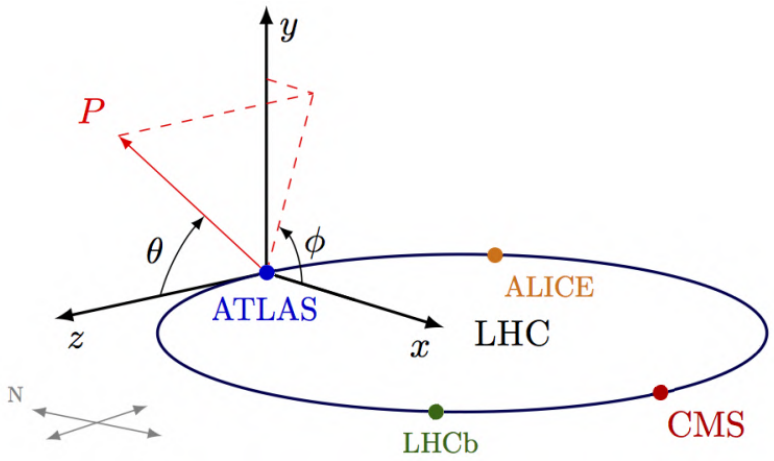
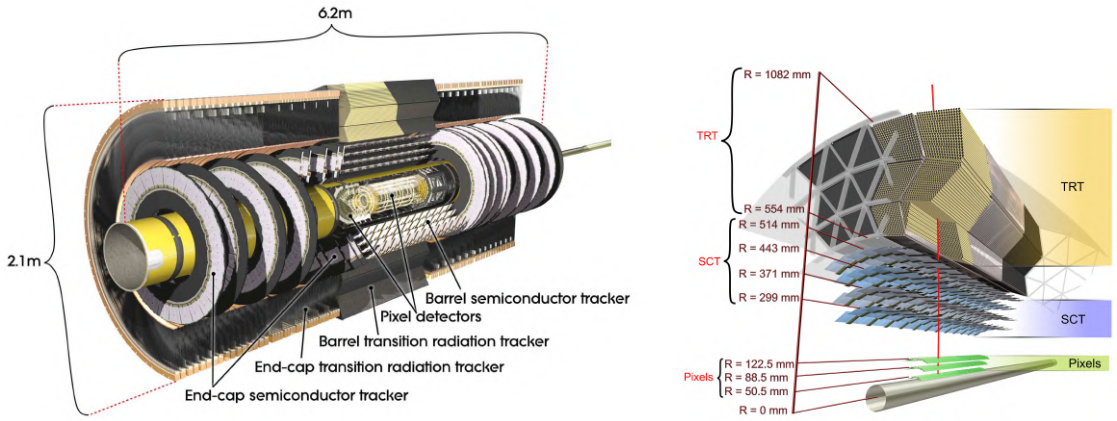


Figure 1.3: The right handed ATLAS coordinate system.

pseudorapidity range of -2.5 < η < 2.5 with full coverage in ϕ. Designed to reconstruct the trajectories and decay vertices of charged particles generated through collisions with high efficiency [16]. The ID is seated within a massive solenoidal magnet that generates 2 Tesla magnetic field. The curvature of the particle trajectories due to the magnetic field is used calculate their momentum. The three parts of the ID are: the Pixel detector, semiconductor Tracker (SCT) and the Transition Radiation TRacker (TRT).

1.3.1.1 Pixel detector

The Pixel Detector sits at the centre of the ATLAS detector, closest to the particle interaction point. The pixel detector has 3 layers of barrel detector and two end-caps with three pixels disks each, leading to approximately 80 million readout channels [17]. The Pixel detector is a hybrid pixel detector in which each module is composed of a sensor and a readout chip bonded together by iridium bump bonds. The size of the pixels in the first layer is 50 x 250 μm and 50 x 400 μm in the other 3. Each pixel detector module is able to produce precise position measurements of the charged particle tracks and is useful in locating the points of secondary decay vertices. As of Run 2 of the LHC an additional forth layer was installed between the current pixel



(a) (b)

Figure 1.4: a) The ATLAS Inner detector b) Exploded view of the Inner detector, showing the different layers of the sub-detector [20].

detector and the beam pipe, called the IBL [18]. The new layer allows for better pattern recognition and b-tagging and track reconstruction.

1.3.1.2 Semiconductor Tracker

The SCT is positioned around the Pixel Detector. It consists of 4 cylindrical barrel layers and 9 end-cap disks on each end of the barrel. In total there are 4088 planar p-in-n silicon micro-strip detectors in the SCT, adding up to 63 m^2 of total surface area and 6.3 million readout channels. The micro-strip detectors are spaced μm apart to allow for a position resolution of 17 μm transverse to the micro-strips. The design of the sub-detector was such that energetic charged particles will pass through a minimum of four layers within the acceptance region [19].

1.3.1.3 Transition Radiation Tracker

The outer-most section of the inner detector is the TRT, covering a pseudorapidity range of $|\eta|<0.7$. The TRT is made up of 370 000 drift-tubes (straws), arranged in three layers, parallel to the beam-pipe. The straws are 144cm long, 4mm diameter Kapton tubes coated with a conductive layer and kept at a high voltage of negative

polarity. The straws act as cathodes while in the centre of each tube there is a 30 μm diameter gold plated tungsten wire that acts as an anode. The tubes are filled with a gas mixture of Xenon (70%), CO_2 (27%) and O_2 (3%). Photons are generated by electrons traversing the TRT through transition radiation. As electrons produce more charge than heavier particles the tracker is useful at discerning the two. The solenoid magnet that surround the ID produces a 2 T uniform magnetic field needed for particle tracking [21].

1.3.2 Calorimeters

The calorimeters are used to measure the energy of hadrons, taus, jets and any missing transverse energy generated during collisions. After particles have passed through the tracking systems of the ID they will reach the calorimeters 1.5. The calorimetry sub-detectors of the ATLAS experiment consist of an ElectroMagnetic (EM) calorimeter that covers a pseudorapidity range of $| \eta | < 3.2$, a barrel hadronic calorimeter $| \eta | < 1.7$, Hadronic End-Cap calorimeters (HEC) $1.4 < | \eta | < 3.2$ and Forward Calorimeters (FCal) $3.2 < | \eta | < 4.8$. Particles that travel through dense materials such as steel, will interact with matter according to their radiation and interaction lengths, and produce a hadronic or an electromagnetic shower. The energy from these particles will be deposited within the calorimeters and measured. As electromagnetic and hadronic matter behave differently during this process two separate calorimeter systems were needed. The EM calorimeter, HEC, FCal are all based on lead/liquid-Argon (LAr) detector technologies. The hadronic barrel calorimeter (TileCal) [22] uses a sampling technique together with plastic scintillator plates (tiles) sandwiched between steel absorbers.

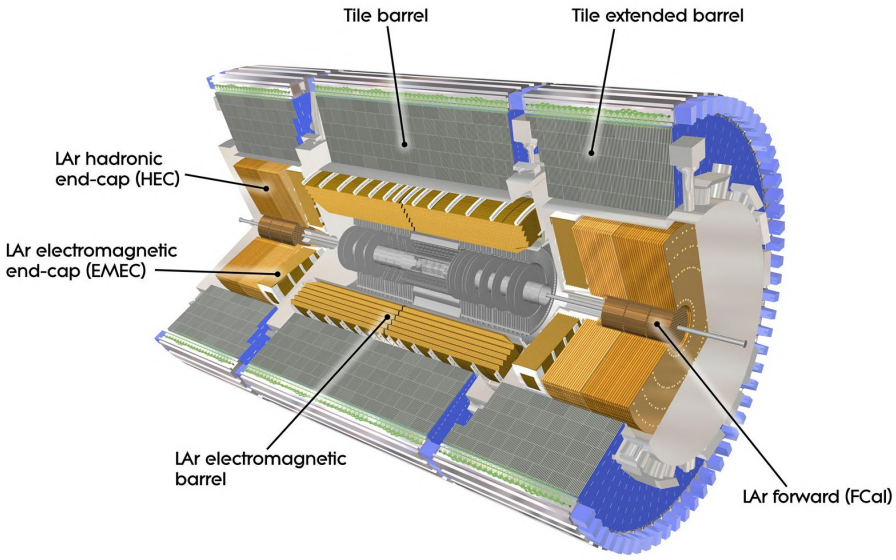


Figure 1.5: Diagram of the ATLAS calorimeter systems [23].

1.3.2.1 Electromagnetic Calorimetry

Areas of the detector with high pseudo-rapidity will require greater radiation resistance and thus the radiation-hard LAr technology is used. EM calorimeters are only capable of measuring the energy of particles that interact electromagnetically such as electrons, photons and positrons.

The EM calorimeter is a LAr detector that is arranged in an accordion geometry. The EM calorimeter consists of two mirrored half barrels covering the range $|\eta|<1.4$. Each half of the barrel is divided into 16 modules, which in total comprise of 1024 accordion-shaped absorbers and alternating readout electrodes, positioned for θ symmetry about the beam-axis. Each pair of absorbers is separated by two liquid argon gaps with readout electrode in the centre. The HEC and ElectroMagnetic EndCap (EMEC) are situated in the endcap cryostat and use the same detection techniques as the the EM calorimeter. HEC has copper absorber plates and uses a parallel geometry. FCAL provides EM and hadronic coverage in the forward region of the detector

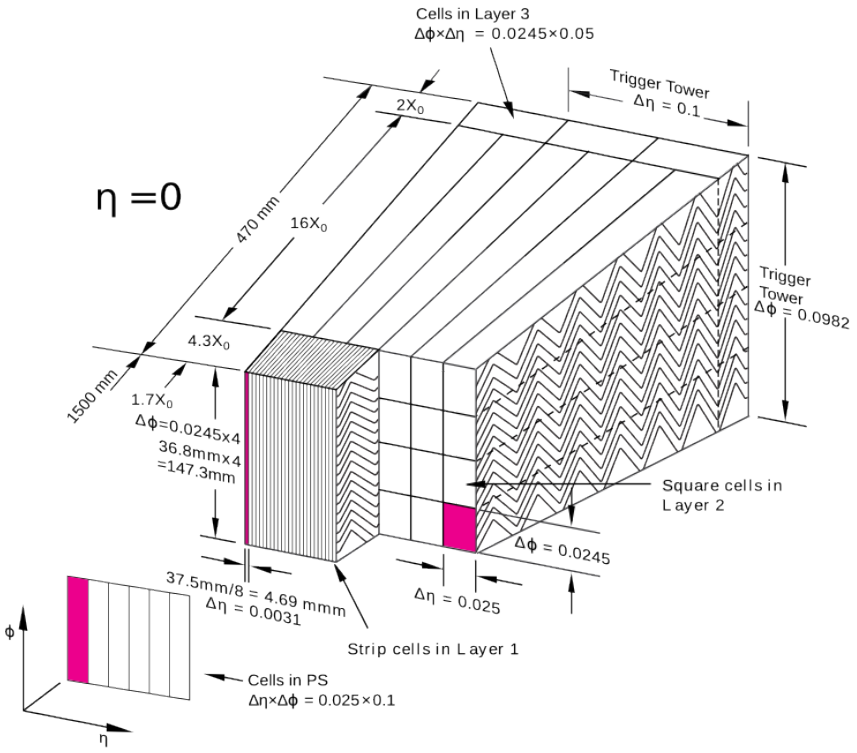


Figure 1.6: Diagram LAr EM calorimeter module [24].

by using both copper and tungsten absorber [24].

1.3.2.2 Tile Calorimeter

Hadronic calorimetry within the ATLAS detector is primarily designed to determine the energy and direction of jets and to measure the E_T^{miss}. The Tile Calorimeter (TileCal) [14] [25] serves as the central hadronic calorimeter sub-detector of the ATLAS experiment spanning a pseudorapidity region of $|\eta| < 1.7$ behind the EM calorimeter. The sub-detector is divided into 4 barrel partitions, two central barrels also called Long Barrel (LB) ($|\eta| < 1.0$), 5.6 meters in length, and two extended barrels (EB) on either end of the LB ($-0.8 < \eta < 1.7$), 2.6 meters in length. The TileCal barrels can be seen in figure 1.5 as the outer grey and blue areas of the calorimeter system. The barrels are further partitioned into 64 azimuthal slices (figure 1.7 a) of size $\Delta\theta \sim 0.1$ about beam-axis. Is total there are 256 slices within TileCal, leading to a combined weight of 2,600 metric tons for the entire sub detector.

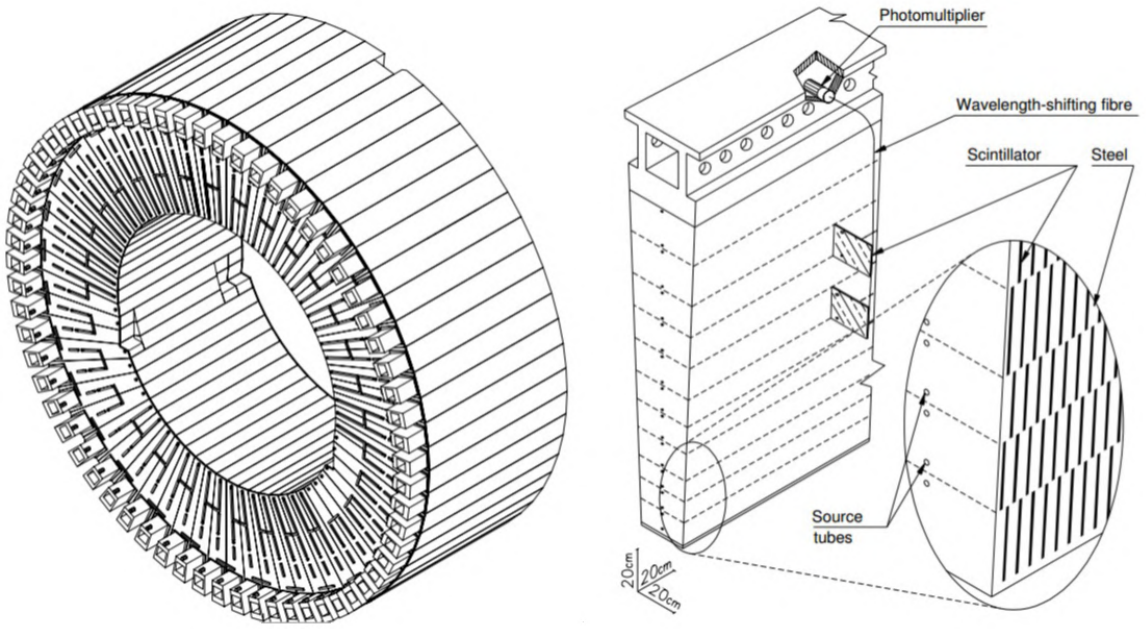


Figure 1.7: a) TileCal Barrel b) TileCal Slice [26].

Each TileCal slice (Figure 1.7 b) is made up of alternating layers of low carbon steel absorber plates and plastic scintillating tiles. Groups of scintillating tiles within each slice are combined to form calorimeter cells. Figure 1.8 shows the depth an η-segmentation of the TileCal. Hadronic particles that travelling through TileCal will collide with the absorber plates leading to particle showers. The charged particles generated from showers will excite the plastic scintillator tiles causing them to emit photons. Neutral pions will decay to photon pairs leading to EM showers which can then be detected by the scintillators. Light produced in the calorimeter cells is readout by Wave Length Shifting fibres, found on either side of each scintillating tile. WLS fibres form each cell are bundled together and readout by two separate Photomultiplier tubes (PMTs) found in the TileCal front-end electronics. The double readout design adds to the systems redundancy and improves the response uniformity from the scintillating tiles. In total there are 5,182 calorimeter cells readout by 9,852 PMTs in TileCal.

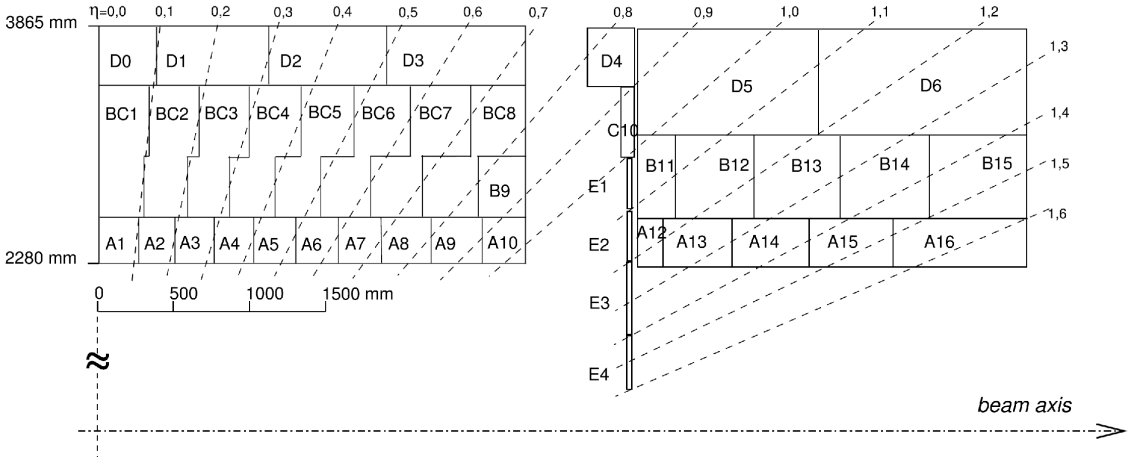


Figure 1.8: Segmentation of TileCal slices in depth and η for half of a long barrel (left) and for an extended barrel (right). Calorimeter cells are distributed evenly about the interaction point [26].

The front-end electronics are found on the detector within special mechanical drawers (Super-drawers) that fit into the outer section of each TileCal slice. Light received by the PMTs is converted into analog electrical signals which is sent to Front-end board (FEBs), where the signals are amplified and shaped before being digitised with 10 bit ADC at 40 MHz. Several low gain signals from the multiple FEBs are sent to a adder board which sums the inputs and sends them to the ATLAS Trigger and Data Acquisition System (TDAQ) to be used for the Level 1 muon and hadron triggers. The digitised samples are stored within pipeline memory buffers to create a $25\mu s$ delay while the Level 1 trigger is being processed by the TDAQ. If a Level 1 acceptance signal is received for a sample, a data window of samples will be collected with samples from both before and after the accepted sample. This collection of samples will be formatted and sent to the back-end electronics Read-Out-Driver (ROD) for further processing. Signals that are not selected by Level 1 will be eventually overwritten by new data being received. The ROD forms the link

between the front- and back-end electronics [27] of TileCal. The ROD performs several functions such as: Initial online energy reconstruction of PMT pulses, Calibration corrections, combining multiple front-end sources into a single data link; formats data and metadata for DAQ.

1.3.3 The Muon Spectrometer

The ATLAS Muon spectrometer [28] is a tracking detector designed to measure the momenta of muons generated during collisions. The Muon spectrometer is the largest sub-detector and it positioned the furthest away from the central interaction point. Figure 1.9 displays the position and size of the muon spectrometer. It was constructed to make efficient use of the magnetic fields and cover a pseudorapidity range of $| \eta | < 3$. The spectrometer is made up of three regions: barrel region $| \eta | < 1.05$, transition region $1.05 < | \eta | < 3$ and end-cap region $| \eta | > 1.4$. Different designs and technologies were used depending on spatial and timing resolution, expected radiation requirements of each section.

The types of detector used: Monitored Drift chambers (MDT), Cathode Strip chambers (CSC), Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC). The RPC and the TGC are used as trigger detectors, while the MDT and the CSC are used for precise tracking measurements. These detectors work through the ionization of gas. The CSC uses CO_2, Ar, CF_4; Ar for the MDT; SF_6, $C_2H_2F_4$, C_4H_{10} for the RPC and n-pentane for the TGC. The muon spectrometer together with the Calorimeter systems are used to estimate the amount of missing energy that takes the form of undetectable particles such as neutrinos or even non-interacting particles like dark matter.

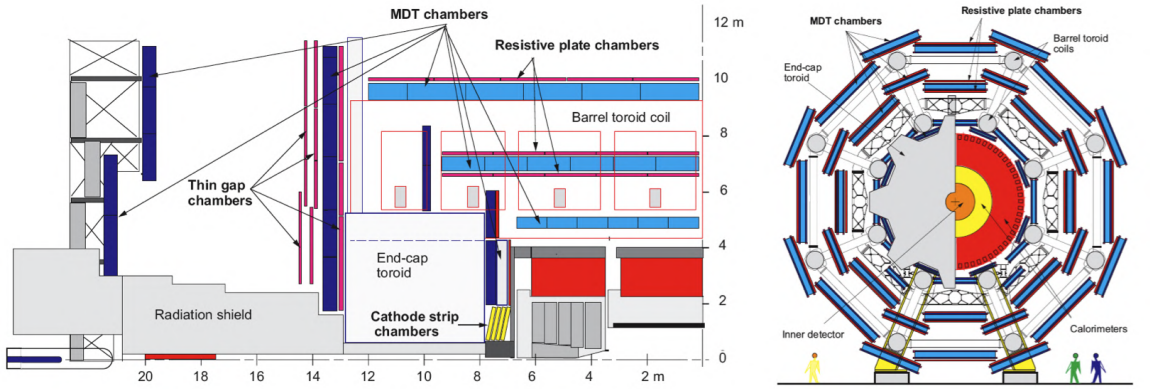


Figure 1.9: Diagram of the ATLAS Muon Spectrometer [28].

1.3.4 Magnetic Field

ATLAS uses strong magnetic fields to bend the path charged particles as they move through the detector so that their momenta can be measured. The magnet field systems were designed to optimise the identification power of the different sub-detectors while minimising scattering effects [29]. The magnetic fields are produced using superconducting magnet systems: Central Solenoid (CS), air-core Barrel Toroid (BT) and two End-Cap Toroid (ECT). The CS is built from a single layer coil that generates a uniform two tesla magnetic field that surrounds the ID. The uniform magnetic field strength allows the ID to make extremely precise measurements. The outer toroidal magnet system (BT and ECT) is produced by eight large superconducting barrel loops and two end-cap toroidal magnets weighing 1300 tons. The BT extends to a length of 26 m, 20 m in diameter and total volume of 8000 m^3. The BT and ECT fall outside the calorimeters and inside the muon spectrometer, producing a non-uniform magnetic field ranging from 2 to 8 Tesla The magnet system implements Nb-Ti superconductors in a copper matrix technology, which is cooled to 4.5 K. The current BT and ECT uses 20 kA and the CS uses 7 kA.

1.3.5 The ATLAS Trigger and Data Acquisition System

The ATLAS detector has the potential to probe up to a billion proton-proton collisions per second but due to technological constrains it is simply not possible to readout and store all data produced. The LHC runs at a bunch crossing frequency of 40 MHz leading to a raw data rate in the Peta bytes per second range within the ATLAS detector. Thankfully, only a small percentage of these collision events are seen to have "interesting" characteristics that would lead to new physics discoveries. The data rate is therefore reduced drastically through the process of trigger selection. The ATLAS experiment uses a multi-layered computing network to reduce the data rate of 40 MHz to a more manageable rate <1.5 kHz. Data selected by the trigger systems is channelled from the detectors to storage through the Data AcQuisition System (DAQ).

The current trigger system used by ATLAS is composed of three levels of event selection (Level 1, Level 2 and the Event Filter (EF)) [30]. The Level 1 trigger system is based on custom hardware designed for the ATLAS experiment. The Level 2 trigger and EF work together to form the High-level Trigger (HLT) and are primarily based off commercially available off-the-shelf (COTS) components. A diagram of ATLAS Trigger and Data AcQuisition system (TDAQ) can be seen in figure 1.10. In addition to event readout, the DAQ system also provides a means to configure, control and monitor the ATLAS detector. The Detector Control System (DCS) is used to supervise the detector services, such as the power supplies and the gas cooling systems.

1.3.5.1 Level 1 Trigger

The Level 1 trigger [32] is designed to search from signatures of electrons, photons, jets, high-p_T muons and τ-leptons that decay into hadrons. Events with large E_T^{miss}

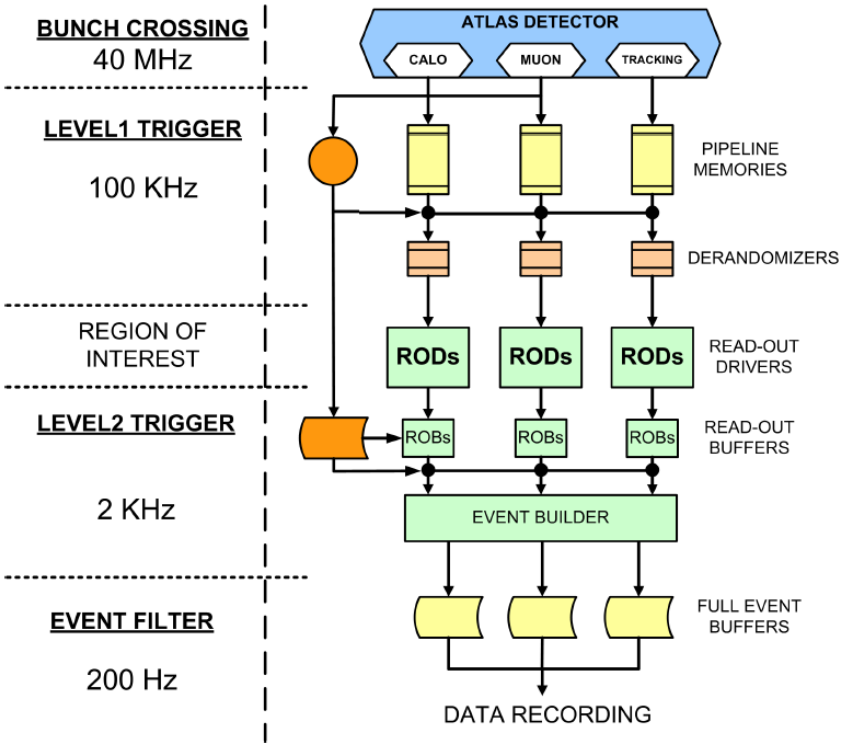


Figure 1.10: ATLAS trigger and data acquisitions system data flow [31].

and large total transverse energy are also selected for [30]. The Level 1 decisions process is based off of reduced-granularity data produced by the Resistive Plate chambers (RPC) and Thin-Gap Chambers (TGC) for high-p_T muons. Data from the calorimeters is used for the Level 1 select for jets, electromagnetic clusters, τ-leptons, E_T^{miss} and large E_T. The Level 1 trigger is able to reduce the event rate from 40 MHz to a more manageable 100 kHz. As Level 1 trigger decisions need to be completed and received by the readout electronics within a 2.5 μs window. In that time, event data will be stored within pipeline memories on the frontend electronics while it waits for a trigger select.

1.3.5.2 Level 2 Trigger

The Level 2 [30] trigger further refines the event selections by looking into Regions of Interest (RoI). RoIs are defined as regions within the detector that the Level 1 trigger

identified as possible trigger objects within an event. Data for from these RoIs is analysed using full-granularity and full-precision. While RoIs are being processed by the Level 2 trigger they are stored in Read-Out Buffers (ROBs) in the Event Filter Farm. RoI information such as energy, coordinates and the type of signature are used by the Level 2 trigger algorithm to reduce event rate below 3.5 kHz in an average processing time of 40 ms.

1.3.5.3 Event Filter

The final stage of trigger selection is preformed by the EF [30]. The EF processes the data of complete events built in the Event Builder (EB) system. While events are being processed by the EF, they are stored within the Full Event buffers. Selected events are sent CERN computing centre where they will be permanently stored and later used for physics analysis. The EF was originally designed to reduce event output to approximately 200 Hz for Run 1 (2010-2012) but was only able to reduce the output to 800Hz and for Run 2 the recording rate was 1 kHz.

Chapter 2

The ATLAS Tile Hadronic Calorimeter Upgrade

Chapter 2 discusses the High Luminosity LHC upgrade and how it affects the ATLAS TileCal readout electronics.

2.1 The HL-LHC

The LHC was completed in 2010 to run proton-proton collisions with a 7 TeV centre-of-mass energy. In April 2012 until the end of Run 1 in 2013 the centre-of-mass energy was increased to 8 TeV, and following the first Long Shutdown (LS1) in 2013-2014, this was further increased to 13 TeV for Run 2 [33]. In order to support and further enhance the LHCs discovery potential it will undergo a major upgrade at the start of 2027 that will be that will be preceded by a Phase-I upgrade that will take place in 2019-2021 during the LS2, in which the TDAQ network and muon detectors will be upgraded.

After the Phase-II upgrade the accelerator will be called the High Luminosity LHC (HL-LHC) and will extend the operation life of the experiment by another decade.

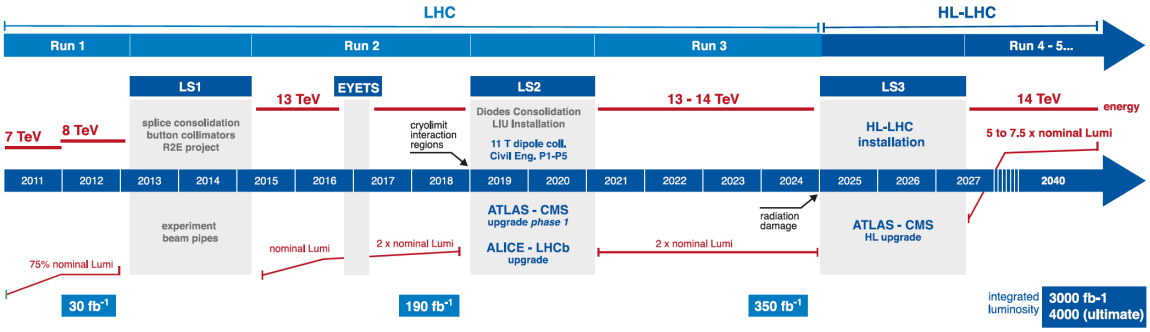


Figure 2.1: The planned LHC upgrade schedule for next decade. It includes scheduled shutdowns, dedicated upgrades and increases in energy and luminosity [37].

The HL-LHC will give physicists the ability to probe physics beyond the standard model, examine electroweak symmetry in greater detail and to measure the properties of the Higgs boson. During its expected lifespan the HL-LHC will deliver an integrated luminosity 10 times greater (3000–4000 fb^{-1}) than the combined LHC Runs 1-3 [34]. For the LHC to reach this level of integrated luminosity within a reasonable time frame, an instantaneous luminosity of up to 7.5 $\times 10^{34}\text{cm}^{-2}s^{-1}$ is needed. This is a 7.5 times increase in the original LHC design luminosity, leading to a total centre-of-mass energy of 14 TeV [35].

The upgrade presents many design challenges as electronics will need to withstand a much higher radiation dose as well as an increased demand for data throughput. The upgrade of the calorimeters and the inner detector [36] for the HL-LHC will take place during the LS3. An overview of the LHC upgrade schedule can be seen in figure 2.1.

2.2 ATLAS Trigger and data acquisition architecture

On average the current LHC produces approximately 25 simultaneous proton-proton interactions per bunch crossing, the HL-LHC is expected to have an average of 200 interactions per crossing, leading to high levels of pile-up. The term pile-up is used to describe the phenomenon when interaction rate is far higher than the bunch crossing rate. The ATLAS detector will need to work with finer granularity and precision when compared to the current system. The architecture of the ATLAS TDAQ system will be completely redesigned and replaced for the HL-LHC to address the new performance requirements, trigger rates and data quantities [38].

There are two design scenarios being considered for the HL-LHC TDAQ: a single-level (Level 0) trigger and a two-level (Level 0/Level 1) trigger system [35]. The single level design will be implemented first but will include the possibility of adapting to a two level trigger scheme in the future. The single level trigger design will include a hardware trigger called CTP and a software system called the Event Filter (EF). A block diagram of the proposed single level HL-LHC TDAQ system can be seen in figure 2.2.

The Level 0 trigger system will receive data from the LAr, TileCal and the muon systems at a event rate of 40 MHz and through the use of hardware based algorithms will reduce the event rate to 1 MHz. The calorimeters provide course-grained data to the Level 0 Calorimeter trigger system (L0Calo) to help identify electrons, taus, jets and to calculate E_T^{miss}. The Level 0 Muon trigger system (L0Muon) receives data in parallel from the muon subsystems and the external cells of the TileCal to identify muons [31]. Additional information from the TGCs and RPCs is received and used

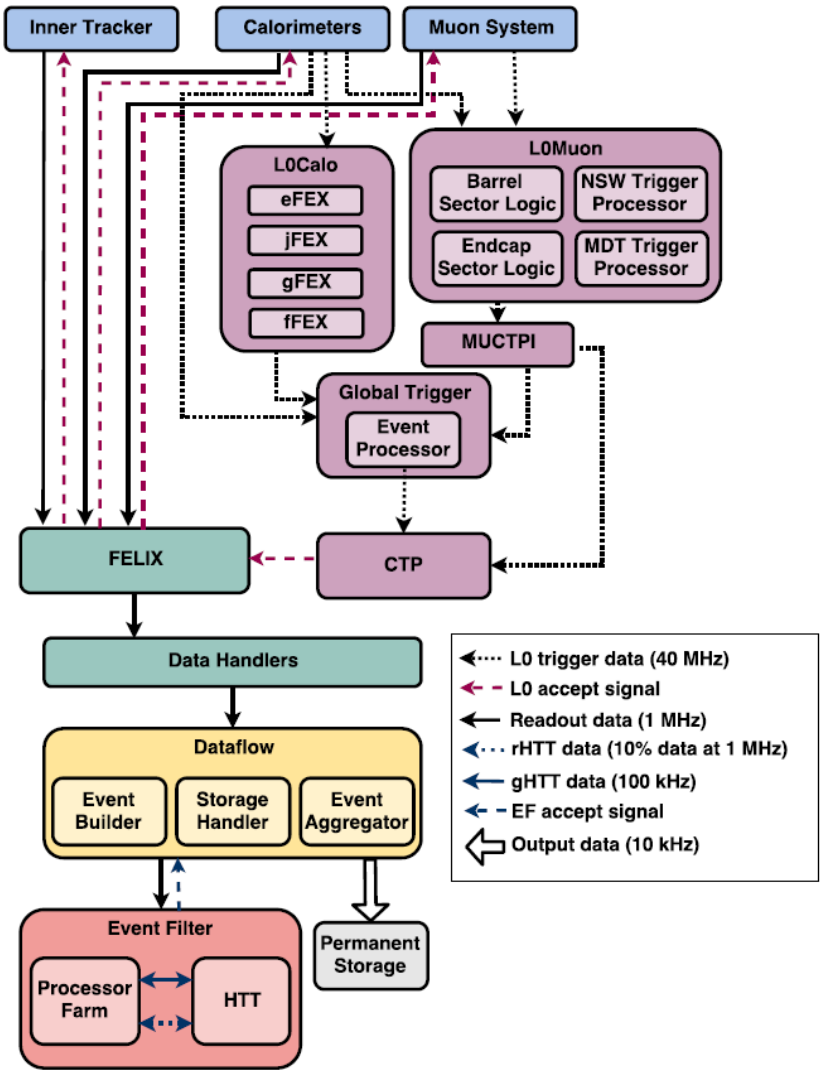


Figure 2.2: Overall baseline design of the upgraded Trigger/DAQ system single-level architecture for the HL-LHC. [39].

to improve muon trigger coverage. The L0Calo and L0Muon trigger systems will provide data of trigger objects to the Global Event system that will combine them to create higher level signatures. This information will forwarded to the Level-0 Central Trigger Processor (L0CTP) which will make the Level 0 trigger decisions based on multiple parameters.

Each of the sub-detectors will transmit data to a common readout system called

the Front-End LInK eXchange (FELIX) [40]. FELIX will send data selected by the Level 0 trigger to the Data Handlers where it will be formatted and placed within buffers. The buffered data will be transmitted to the Event Filter (EF) to undergo the final trigger algorithms. The EF is a software based trigger decision scheme that is able to reduce the event rate to 10 kHz. To fulfil the latency demands for the new TDAQ system and to leave some room for future changes, the system was designed to store 10 μs of data while the Level 0 trigger makes a decision.

2.3 TileCal Upgrade

The HL-LHC poses multiple design challenges for the readout electronics of ATLAS TileCal. Elevated ambient radiation within the ATLAS cavern will lead to an increase in Single Event Upsets (SEU) events causing electronics to malfunction and in some cases the total radiation dosage can lead to the complete failure of electrical components. A SEU is a bit flip (switching state 0 to 1 or vice versa) in a memory element in an electronic device, caused by a single ionizing particle (ions, electrons, hadrons etc) striking the device. The HL-LHC will have an increased event rate and thus the electronics will need to processes far greater data loads and will need to deal with out-of-time pile-up from previous events. The TileCal readout electronics will also need to be compatible with the new TDAQ trigger scheme that will be implemented within ATLAS for the HL-LHC. Finally, the TileCal sub-detector was designed over 25 years ago and many of he electronics had an expected operation life of 10 years. Many of the original electronic components used in TileCal are becoming obsolete and are no longer in production, making maintenance difficult and costly to perform.

The TileCal will therefore need to undergo a complete replacement of it's on and off detector electronics in order to meet the demands of the HL-LHC [34]. Since the

completion of the ATLAS detector in 2008 there have been major advances in FPGAs (Field Programmable Gate Array), ASICs, component radiation hardness and data processing, all of which will be used for the benefit of the new hardware architecture. Major changes to the TileCal readout architecture include: fully digitised signals to be sent to the Level 1 trigger at a bunch crossing frequency, additional levels of redundancy and modularity, shifting the pipeline memories to the off-detector electronics and the implementation of more efficient and radiation hard components.

2.3.1 Current readout architecture

The current on-detector electronics in operation are based on a four board configuration: 3-in-1 Front-End-Board (FEB), Digitiser Board, Interface Board and Trigger Summing Board. The signal flow can be seen in Figure 2.3.

The FEB amplifies (Bi-gain x1, x64) and shapes PMT signals as well as preform calibration functions. The first-level calorimeter trigger (L1Calo) uses analog signals that correspond to the pseudo-projective towers of 0.1 x 0.1 in $\Delta\eta$ x $\Delta\phi$ [35]. TileCal creates the towers signals by summing the analog signals from each FEB using the Trigger Sum Board. The sum outputs are sent off-detector to the trigger pre-processor system through 90 m cables.

The signals from the FEBs are digitised by the Digitiser board at bunch crossing frequency and stored on local pipeline memories pending a L1Calo Trigger accept. If data is selected by the L1Calo it will be transferred to the Interface board, placed in de-randomising buffers and sent off-detector to the Read-Out Driver (ROD). The ROD further formats the data before sending it to the Data Acquisition System (DAQ). The Level 1 trigger selection process reduces the data rate from 40 MHz at

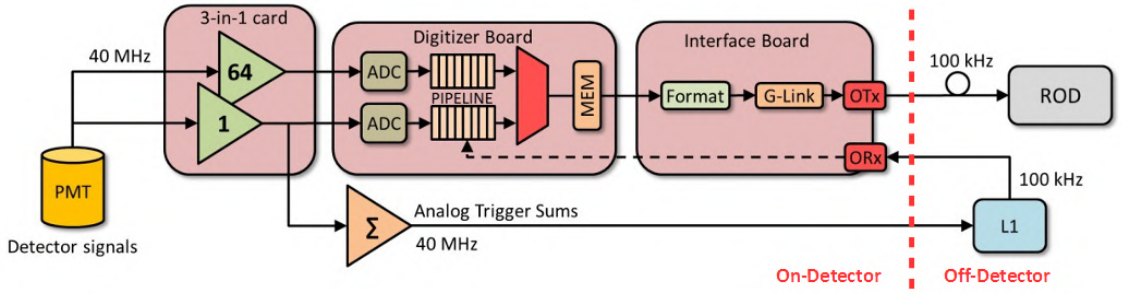


Figure 2.3: Block diagram of the signal flow in the current readout electronics of the ATLAS TileCal.

the PMT output to a more manageable 100 kHz after the interface board.

2.4 Upgrade readout architecture

The new readout architecture proposed for the HL-LHC will fully digitise all detector signals and send them off-detector via high speed optical links to the TileCal PreProcessor (TilePPr) [41]. The signal flow can be seen in Figure 2.4.

Full detector readout at 40 MHz will enable the trigger system to make better decisions by providing the maximum amount of information available, improving precision and granularity. Considerable developments in technology have lead to more advanced electronics able to provide faster and more precise measurements, while being able to withstand harsher radiation environments. Additional levels of redundancy and modularity have been introduced to the on-detector electronics and power systems, allowing for increased reliability and easier extraction during shut down periods [42]. A summarised comparison between the current and future readout systems can be seen in table 2.1.

Downlinks	Present	Upgrade
Number of fibres	256	2048
Link Bandwidth	80 Mbps	4.8 Gbps
Uplinks	**Present**	**Upgrade**
Number of fibres	256	4096
Link Bandwidth	800 Mbps	9.6 Gbps
Back-end red-out modules	32 (ROD)	32 (TilePPr)
Back-end crates	4 (VME)	4 ATCA
Back-end Input bandwidth	6.4 Gbps	625 Gbps
Back-end output bandwidth to DAQ	3.2 Gbps	40 Gbps (FELIX)
Back-end output bandwidth to Trigger	Analog front-end	∼500 Gbps

Table 2.1: Comparison between the current and HL-LHC readout systems

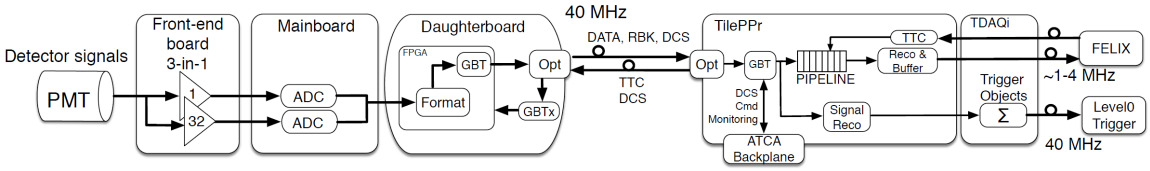


Figure 2.4: Block diagram of the TileCal readout architecture for the HL-LHC upgrade [35].

2.4.1 Hybrid Demonstrator Module

A hybrid demonstrator project was introduced in parallel to the development of the HL-LHC readout electronics to test and validate the new trigger and readout architecture of the HL-LHC. The Hybrid Demonstrator module contains the upgraded front-end electronics combined with the legacy analog interface from the Level 1 trigger system. This would enable the module to be compatible with the current architecture and allow for the testing of new electronics architecture.

The demonstrator module is readout and controlled by a prototype Tile PreProcessor (TilePPr). The TilePPr will store data samples in pipeline memories and transmit Level 1 selected data to the ROD modules enabling backwards compatibility with the current DAQ system [31]. The Hybrid Demonstrator Module will be

installed into the ATLAS detector replacing one of the current TileCal super-drawers.

Additionally, the new readout architecture will require a new test-bench system to be developed that would be compatible with both the new and current systems.

2.5 On-detector Electronics

The front-end electronics are housed in long insertable modules called super-drawers. The drawer provides a removable structure for PMTs, detector electrics and power systems to mounted, as well as provide cooling [43]. The 3 m long super drawers slide into girders located on outer edge of each TileCal slice. The current detector architecture has each super-drawer mechanically divided into two 1.4 m sections that are daisy chained together. The cooling lines, Low voltage power supplies and data-links are all shared between entire super-drawer.

The upgraded design now divides each super-drawer into four independent 70 cm modules called mini-drawers (Figure 2.5) [44]. Each mini-drawer will have completely independent power supplies and data-links to the back-end electronics. A mini-drawer will be able to accommodate up to 12 PMTs and FEB, Mainboard (MB), Daughterboard (DB) and High-Voltage board. The architecture was necessary to improve the reliability of the drawer cooling circuit and to aid with extraction and repair activities on the sub detector. An added benefit will be that the detector will not need to be opened as wide during servicing.

2.5.1 Front-end boards

There are currently three FEB designs proposed for the HL-LHC upgrade that are undergoing studies to test their feasibility. Each FEB option is capable of calibrating

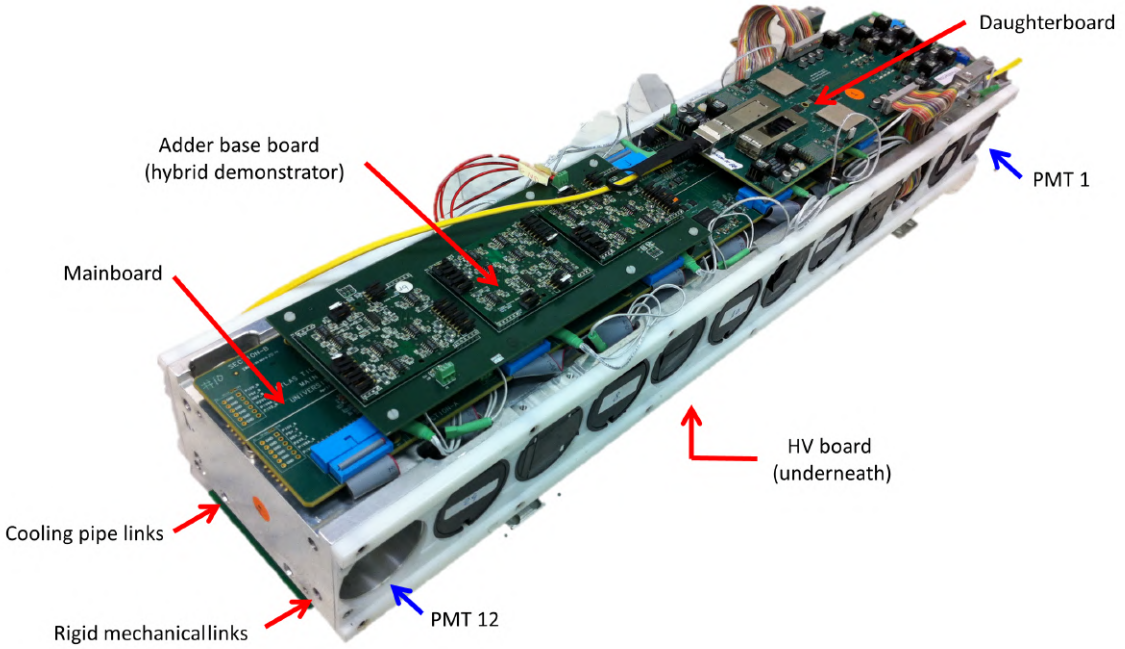


Figure 2.5: Labelled diagram of an ATLAS TileCal Mini-drawer [35].

the electronics, PMT gain and plastic scintillator response.The first two options use custom designed ASIC integrated circuits, Charge Integrator and Encoder (QIE) [45] and the Front-end ATLAS tiLe Integrated Circuit (FATALIC) [46].

The third option is based on a modified version of the current 3-in-1 FEB design [47]. The design uses Commercial Of The Shelf (COTS) components. The updated design includes a fast signal processing chain, a slow processing chain and calibration circuitry. The board has 17 bit dynamic range with improved linearity and lower noise the current version.

The fast signal processing circuit has a 7-pole passive LC shaper to widen the pulse from the PMT. The wide pulse is amplified using two clamping amplifiers (x1 and x32) to produce the high and low gain signals. The amplified signals are sent through a differential connection to the MB for digitisation. The slow processing chain uses

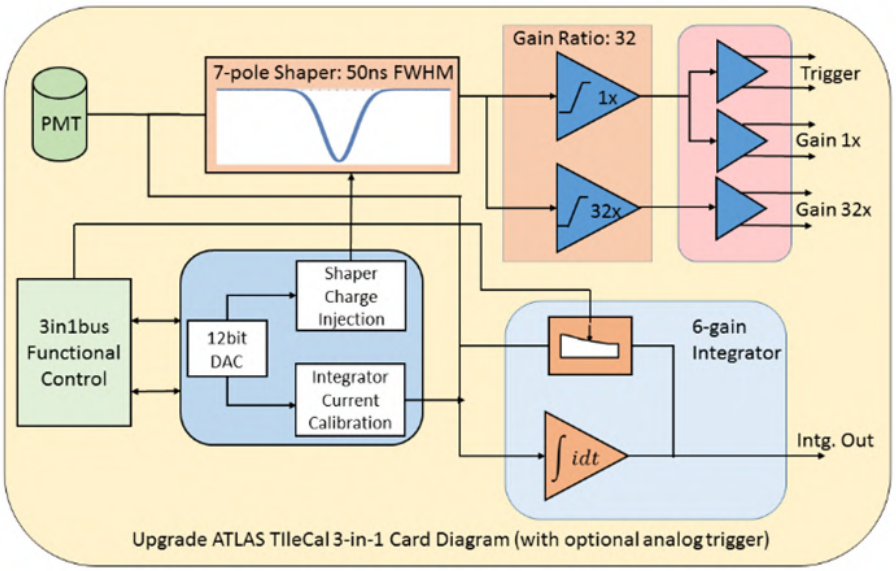


Figure 2.6: Functionality diagram of 3-in-1 card for the upgrade of the TileCal detector [35].

a 6-gain programmable slow integrator to monitor the minimum bias current of each PMT during events and charge Injection and Cesium calibrations.

The modified 3-in-1 FEB is currently used the in the Hybrid demonstrator due to is backwards compatibility with the current analog trigger electronics. The 3-in-1 can produce an analog signal that is received by Trigger sum board to produce the signals needed for the Level 1 trigger system. Figure 2.6 shows a block diagram of the functional blocks of the modified 3-in-1 card.

2.5.2 Mainboard

The MB connects [48] to 12 PMT modules, digitising analog signals, synchronising sampling clocks and forwarding the digitised data to the Daughterboard. Each mini-drawer will contain a single mainboard that measure 690 mm in length and 100 mm in width. The MB will be symmetrical along the length of the board with each side

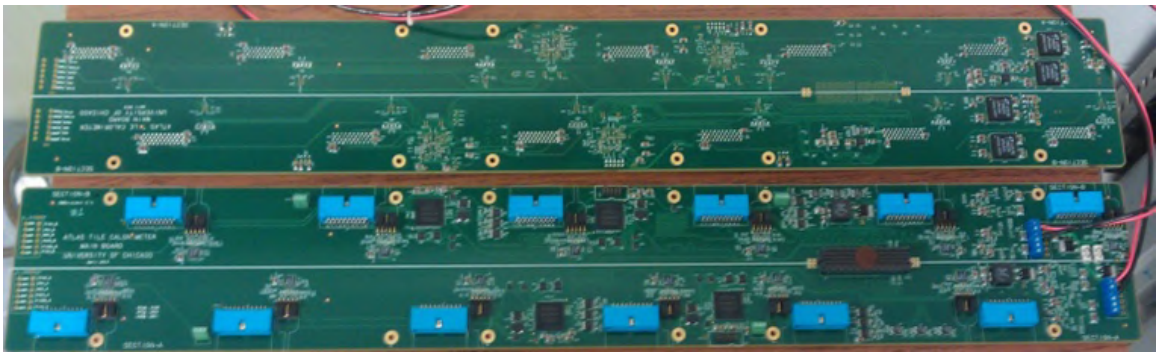


Figure 2.7: Picture of top and bottom sides of the Mainboard used for the 3-in-1 FEB option [35].

reading out 6 PMTs. Each side is functionally independent of one another for added redundancy. There are currently 3 separate MB designs that are being tested, corresponding to the 3 different FEB options.

The upgrade 3-in-1 compatible MB (Figure 2.7) design [49] is currently the system used in the demonstrator being tested at CERN. The MB circuit is divided into four sections each controlled and configured by a Altera Cyclone IV FPGA. The analog signals received from each PMT module are digitised using 12 bit bi-gain sampling system that results in two separate digitised signals, one low and one high. In addition to the bi-gain system, each FEB output is used for the analog integrator that is sampled at 50 KHz and readout by a I2C bus. The signal phase for the sampling clocks can be adjusted to allow compensation for path length delays to the DB. Data from the MB is transferred to the DB via a 2 bit serial bus at 560 Mbps.

2.5.3 Daughterboard

The daughterboard (DB) (Figure 2.8) acts as the high-speed communication interface between the TileCal front-end and the TilePPr modules in the counting rooms [35]. All communications with the on detector electronics are performed by the DB

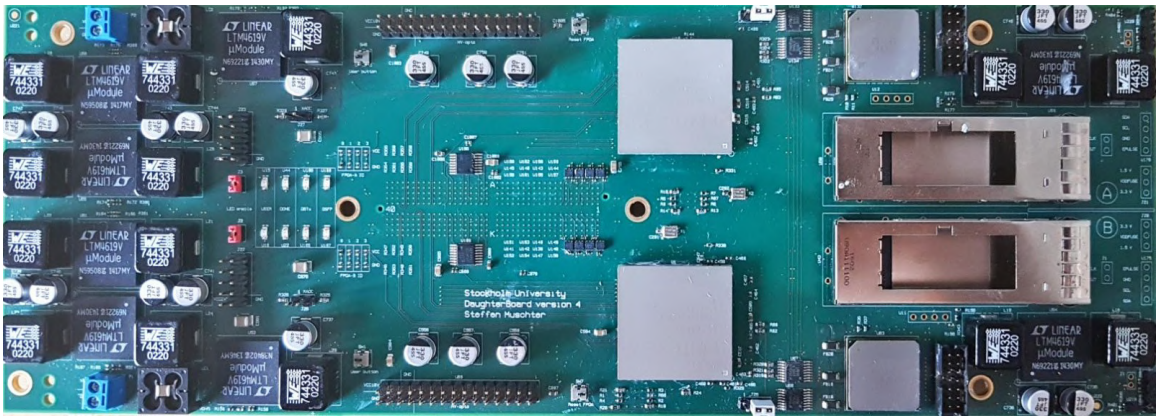


Figure 2.8: Picture the HL-LHC Daughterboard V4 [35].

through a pair of multi-gigabit optical links [50]. These optical links connect directly with the TilePPr. Run configuration commands sent from DCS are received by the DB through these links. The DB will interpret the commands and execute the required changes throughout the front-end electronics.

All data produced by the PMTs are stored in buffers on the DB before being packaged and sent to the TilePPr through the optical links. The data is uploaded to the TilePPr at a rate 9.6 Gbps. Data streams being sent to the DB for drawer configuration and timings are encoded in the GBT protocol and received at a rate 4.8 Gbps. The LHC clock that is used throughout ATLAS will be sent DB to be distributed to the rest of the mini-drawer for digitisation purposes.

High levels of redundancy were included within the design of the DB, redundant optical fibres and electro-optic modules where added to protect against link failures and like the MB the entire DB is split into two identical independent halves. Each half of the DB is managed by a Kintex-7 FPGA. The firmware used to configure the FPGA also includes additional redundancies with the logic.

2.6 Off-detector electronics

The off-detector electronics for the HL-LHC TileCal will consist of two distinct systems: The Tile PreProcessor modules and the Trigger and DAQ interface (TDAQi) boards. The two electronics are based on the Advanced Telecommunications Computing Architecture (ATCA) specifications. The ATCA framework is commercially available standardised platform for high-speed serial connections on a backplane that supports multiple I/O interface types.

2.6.1 Tile PreProcessor

The TilePPr [51] modules will receive and process all the digital data coming from the TileCal detector modules. Additionally, it will distribute the DCS and TTC information for synchronisation of the LHC clock with the on-detector electronics.

The TilePPr modules communicate directly with the FELIX system, transmitting selected data, integrator data and DCS information. The module will also produce reconstructed energy and time per cell that will be sent to the TDAQi boards. FELIX will provide the LHC clock, TTC commands and DCS configuration to the TilePPr modules [31].

The TilePPr will be in a ATCA carrier format with four Advanced Mezzanine Card (AMC) slots that host Compact Processing Modules (CPM). Each CPM will be able to readout and manage 8 mini-drawers, equivalent to two TileCal slices. The FPGAs on the CPMs will store data samples from the front-end in pipeline memories while they wait for the Level 0/Level 1 trigger acceptance signals. Once a trigger accept signal is received data will be moved from the memories, formatted and transmitted to FELIX. In total 32 TilePPr modules will be needed for the complete readout of

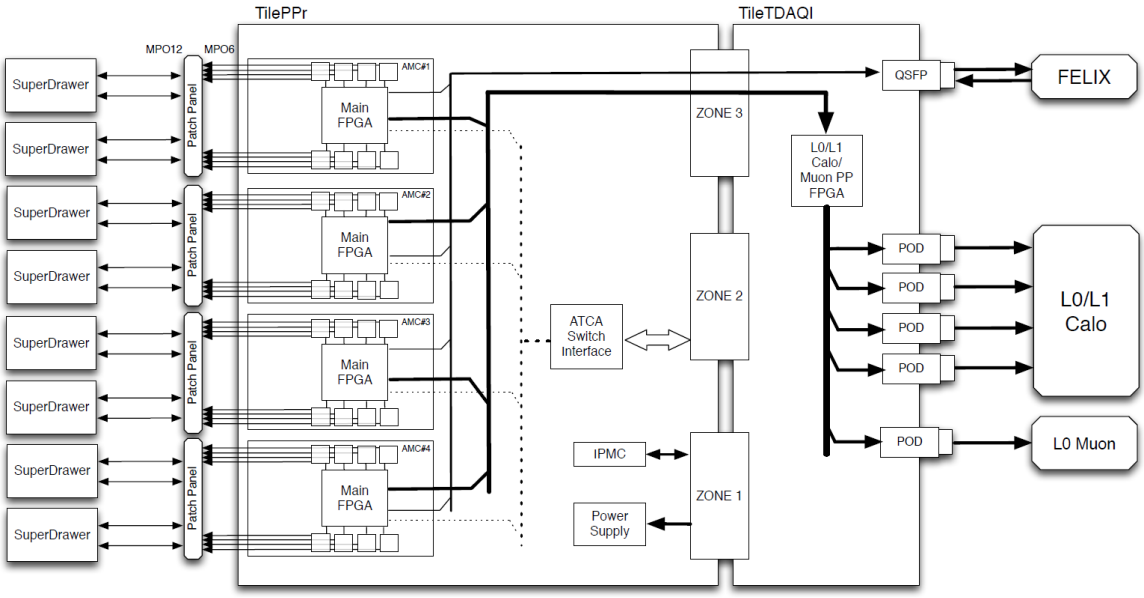


Figure 2.9: Block diagram of the final version of the TilePPr and TDAQi designs [31].

the TileCal sub-detector [31]. Figure 2.9 shows a block diagram of the TilePPr and TDAQi boards for the HL-LHC.

2.6.2 Tigger and DAQ interface

The TDAQi [52] Rear Transition Module (RTM) will act as the link between the TilePPr and the ATLAS TDAQi system. A FPGA on the TDAQi module will use the data provided by the TilePPr to calculate trigger objects with different granularity and energy resolution as well as preprocess the trigger data. This information is transmitted to the trigger systems through optical connections with fixed latency. The first version of the TDAQi was produced in 2018.

Chapter 3

Tile Calorimeter Test-Bench

This chapter will describe the test-bench systems used to validated the on-detector electronics of the ATLAS TileCal. A brief description of the current test-bench system, MobiDICK, will be presented followed by a more detailed look into the new test-bench, PROMETEO. PROMETEO is currently still under development and its design may change in the future. It is being developed for the purpose of fully certifying the on-detector electronics of the HL-LHC ATLAS TileCal.

The Chapter 4 will go into additional detail describing the development of the ADC board used in PROMETEO, which is the focus of this dissertation.

3.1 Test-benches

Test-benches for TileCal are being developed to validate and ensure Quality Assurance (QA) during the assembly of components into mini-drawers and their installation into the ATLAS detector [35]. TileCal has a total of 256 modules; each needs to be independently serviced and assessed for QA before any data taking periods take place.

The Mobile Drawer Integrity CheckKing (MobiDICK) test-bench has been in op-

erational service since 2003 and has since undergone several iterations to improved function, include new technologies, user friendliness and portability [53]. Due to the complete redesign of the TileCal readout architecture, a new test-bench is undergoing development to replace the MobiDICK 4 [54]. The Portable ReadOut Module for Tilecal ElectrOnics (PROMETEO) will serve as the replacement for the MobiDICK and will be fully compatible with the new HL-LHC electronics [55].

3.2 MobiDICK

The original MobiDICK test-bench was designed to be used in the commissioning of the modules in the test-beam of 2002 [56] [53]. The current version used for TileCal is named the MobiDICK 4 and has been in operation since 2013. MobiDICK 4 (Figure 3.2), was a redesign to increase the portability by the usage of commercial FPGA devices and custom PCBs (Printed Circuit Board). At the same time, it allowed to implement tests that were not available in previous versions. The system is able to carry out different sets of tests on the TileCal on-detector electronics during data taking conditions to certify their functionality. Previous versions of MobiDICK used commercial modules inside a NIM crate that was very heavy.

The core processor of MobiDICK is a Xilinx Virtex 5 FPGA found on a ML507 evaluation board [57]. The FPGA is configured with a 440 MHz PowerPC RISC microprocessor that has access to 256 MB of RAM, running a CERN Centos 7 Linux version. The ML507 has multiple I/O connections: 4.25 Gbps GTX transceiver, 1000 Ethernet, serial ports, SFP ports, USB, RJ45 and other additional peripheral connectors. The microprocessor runs an embedded Linux Kernel based on BusyBox and is connected to peripherals through a local bus. The GUI controls the multiple custom daughter-boards that provide the different functionalities to the motherboard.

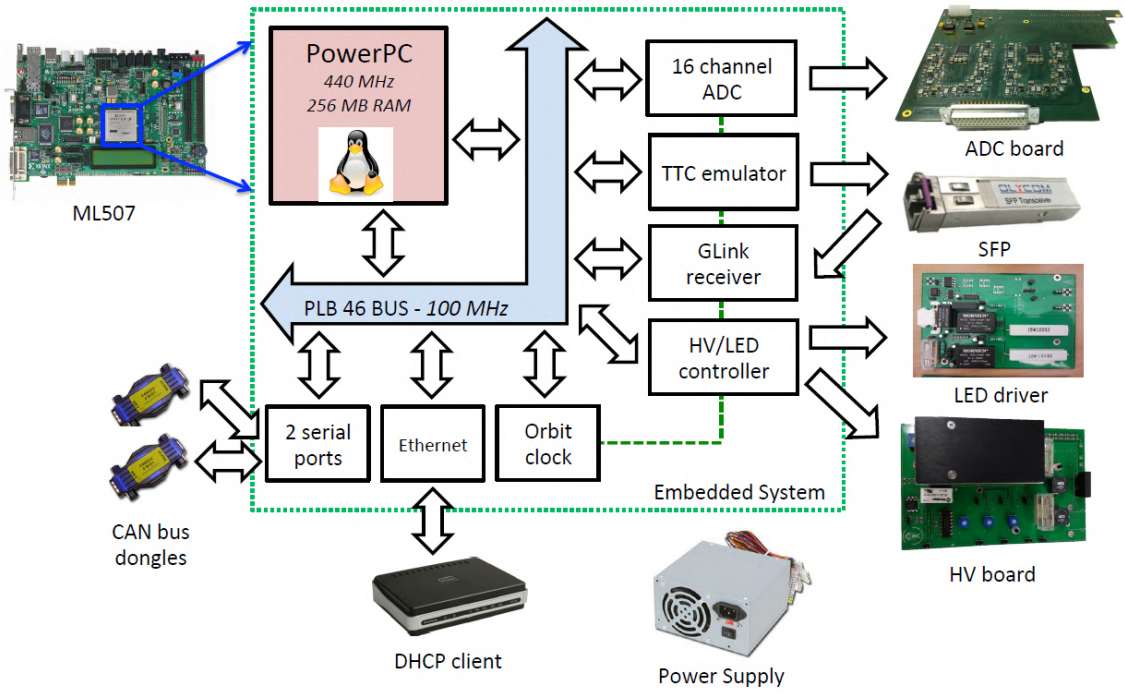


Figure 3.1: MobiDICK component overview [57].

The several custom PCBs designed for the test-bench interface with the motherboard through HDL firmware modules called IP cores within FPGA. Many of the IP Core are commercially available while others had to be written in custom HDL code. A custom ADC board digitises the analog trigger outputs (hadron and muon) from the super-drawers, with 12-bit precision at a rate of 40 MHz [58]. The ADC board, LED driver board and High Voltage driver board were all produced in South Africa.

3.3 PROMETEO

The Portable ReadOut Module for Tilecal ElectrOnics (PROMETEO) is the new test-bench in development for the full certification of the HL-LHC upgrade front-end electronics of the ATLAS TileCal [55]. It is the evolution of the previous test-bench MobiDICK, which has been in operation since 2003 [58]. The design of PROME-

TEO was inspired by the MobiDICK, with many of its feature and custom peripheral boards being incorporated into the new system. The PROMETEO system consists of Mainboard (Xilinx VC707), Readout board, High Voltage Board, ADC Trigger board, LED Board, ATX power supply, Ethernet router and a small form factor PC. A component digram of PROMETEO can be seen in Figure 3.2.

PROMETEO has been designed to interface directly with the front-end electronics, reading out and analysing data from 12 high throughput channels at LHC bunch crossing frequency. The test-bench is able to assess the quality of data in real-time, in addition to detecting and diagnosing errors and malfunctions in each mini-drawer [54]. The PROMETEO will be a fully independent portable test-bench system capable of being used within the tight confines of the ATLAS cavern. Components were chosen to be low-cost and easy to upgrade while being scalable for network usage.

The Hybrid Demonstrator (Section 2.4.1) that aims to test the new TileCal readout architecture will include the analog summation trigger boards from the original readout electronics. This will allow the demonstrator to be compatible with current analog calorimeter/muon trigger system and will provide both analog and digital trigger signals [59]. PROMETEO will therefore include an ADC Trigger board to digitise the analog Level 1 trigger signals and send TTC commands to the mini-drawer.

3.3.1 Mainboard

The current version (Figure 3.3) of PROMETEO uses a Xilinx VC707 [60] evaluation board with a Virtex 7 FPGA to emulate the TilePPr functionalities. The VC707 board and the TilePPr share the same Virtex 7 FPGA model and are able to share large portions of the same firmware [35].

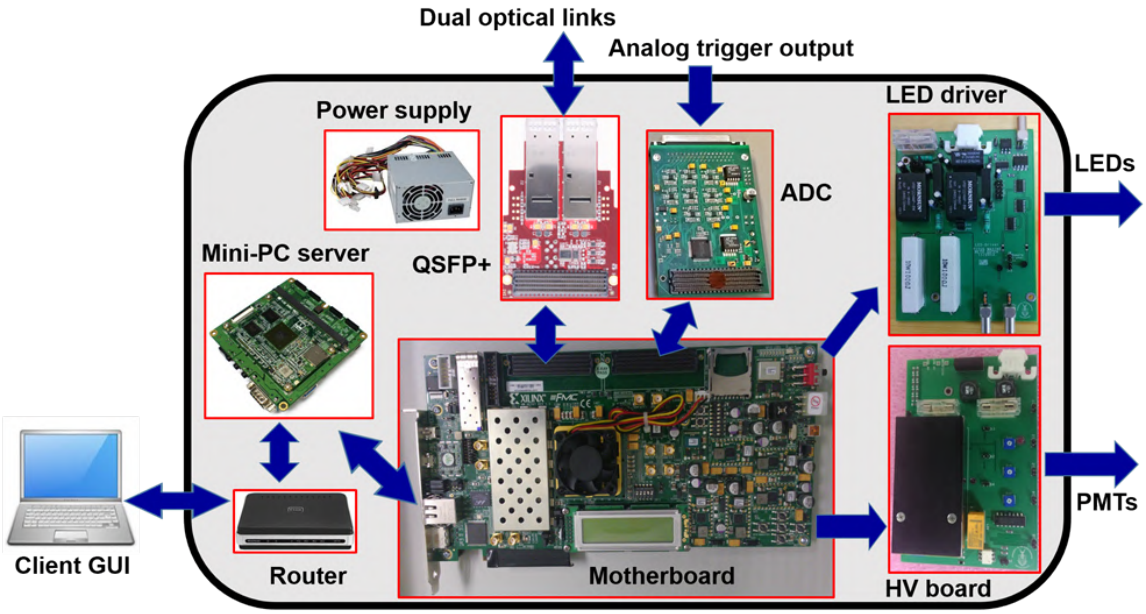


Figure 3.2: PROMETEO test-bench component overview.

The VC707 board has 1 GB DRR3 RAM and two FPGA Mezzanine Card (FMC) connectors which are used to connect a QSFP+ module and custom ADC Trigger board. IPBus protocol [61] is programmed to the on-board flash allowing data samples to be stored by memory address and retrieved via trigger request [55]. IPbus does not require an on-board operating system and is able to function with a users choice of client operating system. It is expected that the next iteration of the test-bench will use the TilePPr as its mainboard.

3.3.2 Mini PC

A small form factor computer or "mini-PC" is connected to the mainboard via Ethernet using IPBus protocol. In the current iteration of PROMETEO, the mini-PC has an Intel i5 processor with 8 GB of RAM. The mini-PC is used to host a Java based GUI webpage from which a user can perform tests, analyse data and view results done through PROMETEO. A router is used to broadcast the webpage on a local

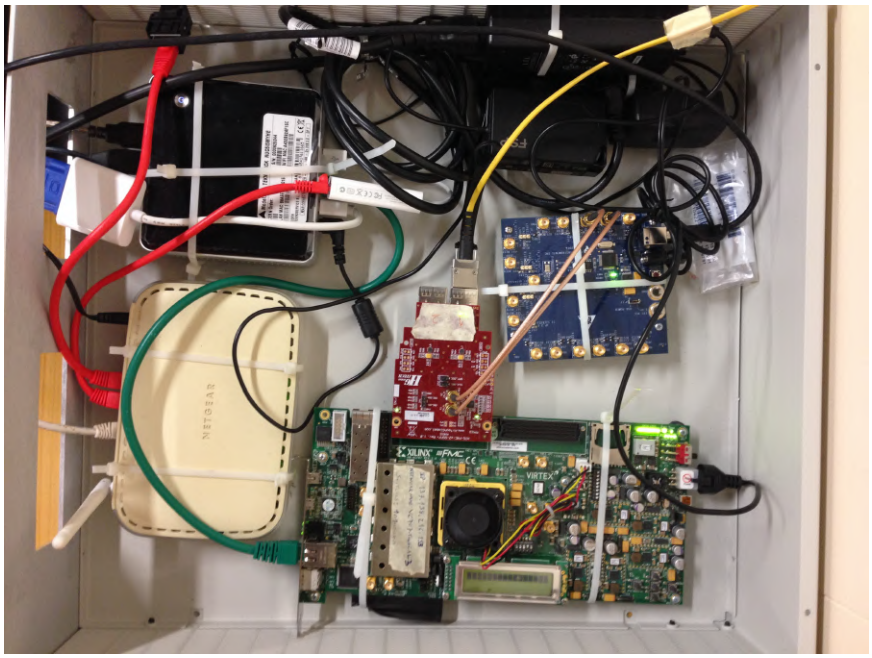


Figure 3.3: Image of PROMETEO in development.

wifi, allowing users to access the webpage on any wifi enabled device with a internet browser.

3.3.3 High Speed readout

A high speed Quad Small Form-factor Pluggable plus (QSFP+) (Figure 3.4) FMC is used to readout the 12 data channels coming off the front end as well as send control and configuration signals. The connection is able to operate at 40 Gb/s (totalling 80 Gb/s with redundancies), matching the design specifications of the TilePPr [54].

3.3.4 High Voltage board

A custom High Voltage board [53] was created originally for the MobiDICK4 but was upgraded and reused for the PROMETEO test-bench. The board is used to turn on a high voltage power supply, activated using a Transistor-Transistor Logic (TTL) controlled relay.

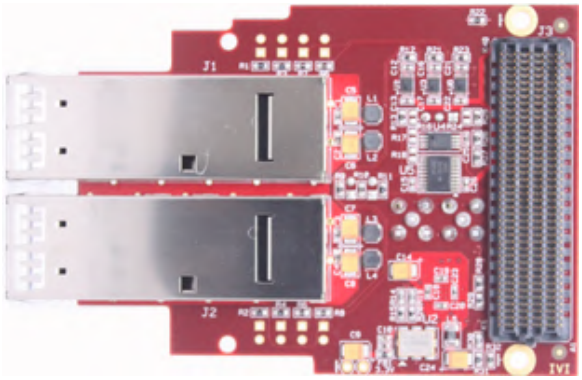


Figure 3.4: QSFP+ FMC module used in the PROMETEO.

It has a +24 V 1 A input that is converted to +5V 100 mA that supplies to a an internal DC/DC IQ2405SA converter. The board is activated by a (0 V and 3.3 V) TTL signal, that once active am Ultravolt module produces a -830 V output. The -830 V is used to power the the gain of the PMTs on the TileCal Front-end. A labelled diagram of the High Voltage board can be seen in figure 3.5.

3.3.5 LED driver Board

The LED [53] is used to produce two electrical pulses: 20 ns wide, 20 V_{pp} with a 70 ns time delay. The pulses are triggered on the rising edge of an input pulse using TTL logic (0 V and 3.3 V). The board is turned off by default due to reduce power consumption and the heating of components. The LED board can be powered via a 24 V or 12 V supply. The LED board is triggered by a +3.3 V input sent from the mainboard. A picture of the LED driver board can be seen in figure 3.6.

3.3.6 ADC Trigger board

A custom high-speed ADC board (Figure 3.7) was developed to digitise the analog trigger signals used for the L1Calo system [62]. The analog trigger signals are produced by the adder boards found on current the front-end electronics and the Hybrid demonstrator module. The adder boards are used to sum low gain analog signals

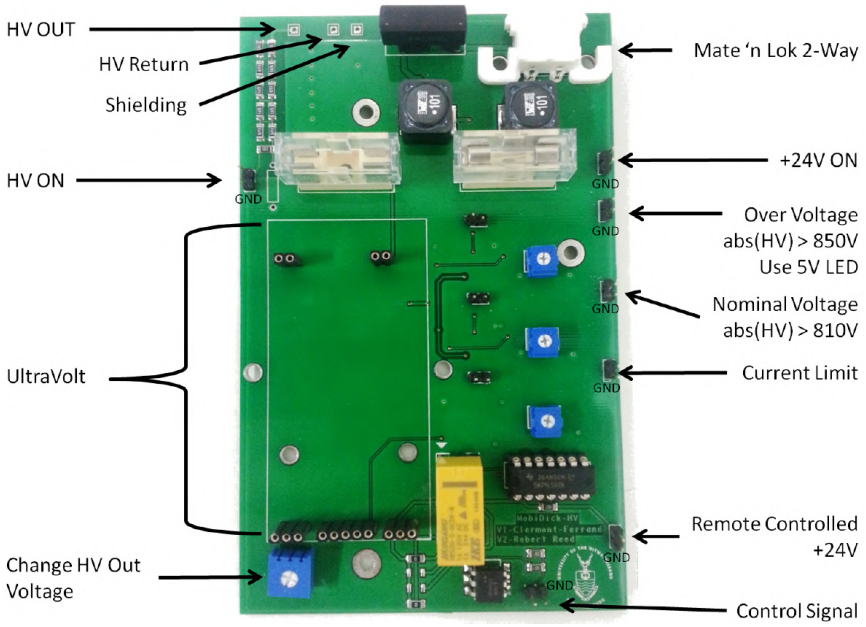


Figure 3.5: Labelled diagram of the High Voltage Board for the PROMETEO Testbench. Manufactured in South Africa

from several FEBs so that they can be used as a input for the Level 1 trigger.

The ADC board is responsible for conditioning and digitising 16 differential analog signals received from the adder boards. Two 12-bit ADC5271 8-channel ADC ASIC chips are used to sample the analog signals at bunch crossing frequency. The digitised signals are transmitted in a serial form through the FMC connector to the VC707 FPGA to be de-serialised and stored in de-randomising memories on the board. Each channel has a data rate of 480 Mbps resulting in a combined rate of 7.68 Gbps to the FPGA.

The ADC chips on the board are configured by the FPGA through an I^2C interface and 40 MHz clock produced by the FPGA to be used for sampling and synchronisation. The board is powered via a 12 V connection supplied through the FMC from which multiple voltage levels are created (+D3.3V, +-A3.3V and +-5V) to power differential amplifier and ADC chips on the ADC board.

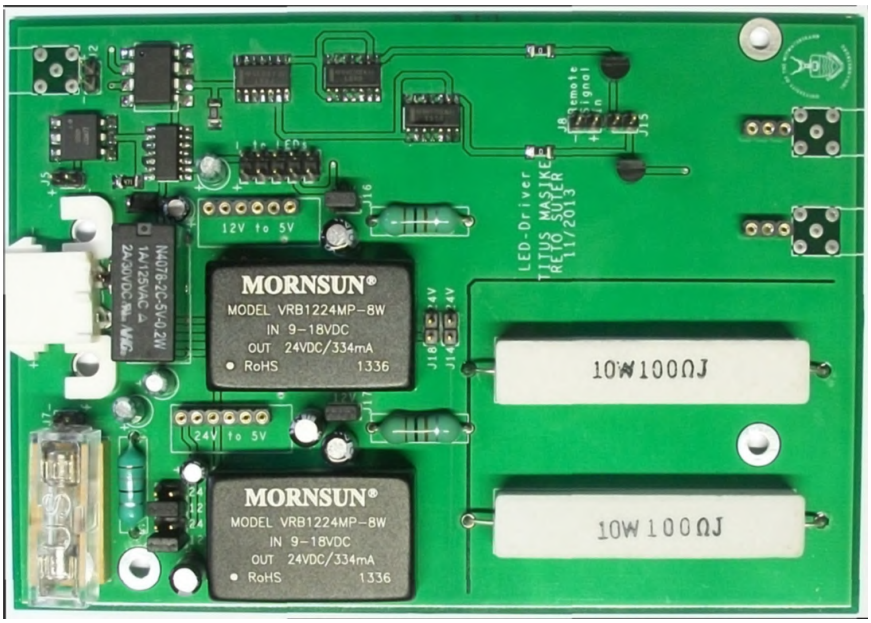


Figure 3.6: Picture of the LED Driver Board for the PROMETEO test-bench. Manufactured in South Africa

The Chapter 4 will go into detail about the the development and testing of the ADC Trigger board.

3.4 Front-end electronics tests

- **Data integrity test:** A set of tests used to test the digital readout of the TileCal front-end. In each test a single event is readout and the quality of data is assessed by performing a Cyclic Redundancy Check (CRC).

- **Digitiser shape:** This test is designed to check the two amplification circuits of the digital readout using the Charge Injection System on the 3-in-1 cards. The test begins by configuring the digitisers to auto-gain and readout modes. Two events are generated, one with a small charge that will be readout by the high gain samples, the second with a large charge to be readout by the low gain samples. The two events are evaluated separately. They are compared to the

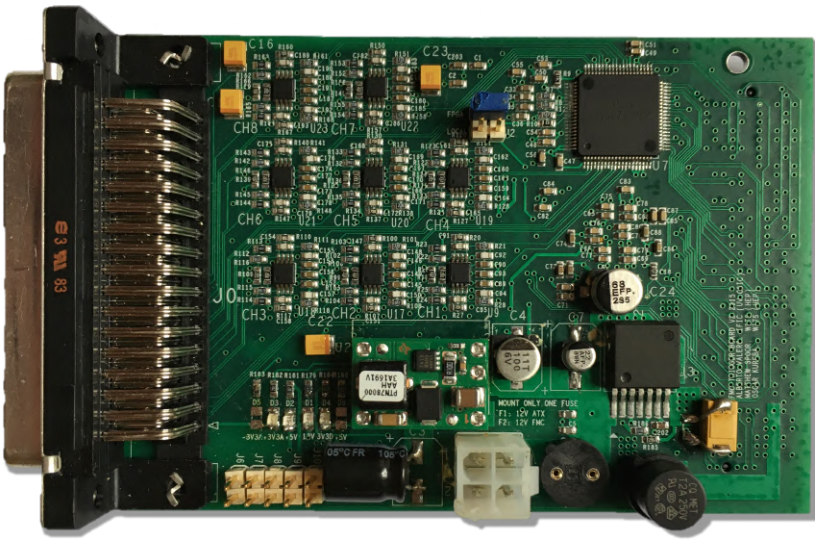


Figure 3.7: ADC Trigger board developed for the PROMETEO test-bench. Manufactured in South Africa.

expected pulse height and width for the provided charge.

- **Digital noise:** This test will analyse the average RMS of samples of each channel for N events.
- **Stress test:** Runs a simple CRC on the data as fast as possible.
- **Motherboard side communication:** Tests communications with the Mainboard in the drawer.
- **High voltage side communication:** Tests communications with the High voltage board.
- **Integrator linearity:** Checks the linearity and noise levels of the charge integrator circuits in the 3-in-1 cards.
- **Integrator HV:** Checks the noise and linearity levels with the high voltage distribution electronics and high voltage input enabled. This is performed on each 3-in-1 card sequentially.

- **Opto and NominalHV:** Checks the functionalities of the high voltage distribution electronics.

Chapter 4

ADC trigger board for the ATLAS TileCal PROMETEO

This chapter discusses the design, development and testing of the ADC trigger board used for the PROMETEO test-bench.

4.1 Study objectives

This project aimed to design, develop and test a high data throughput Analog-to-Digital-Converter (ADC) board and accompanied FPGA firmware for the new PROMETEO test-bench of the ATLAS Tile Calorimeter, as well as learn the skills required to perform the task.

4.2 Problem identification

The TileCal Hybrid demonstrator module and the current readout architecture provide analog sum outputs of the projective trigger towers and the amplified signal of the outer most radial layer (D-type cells) [53]. To test the hybrid demonstrator,

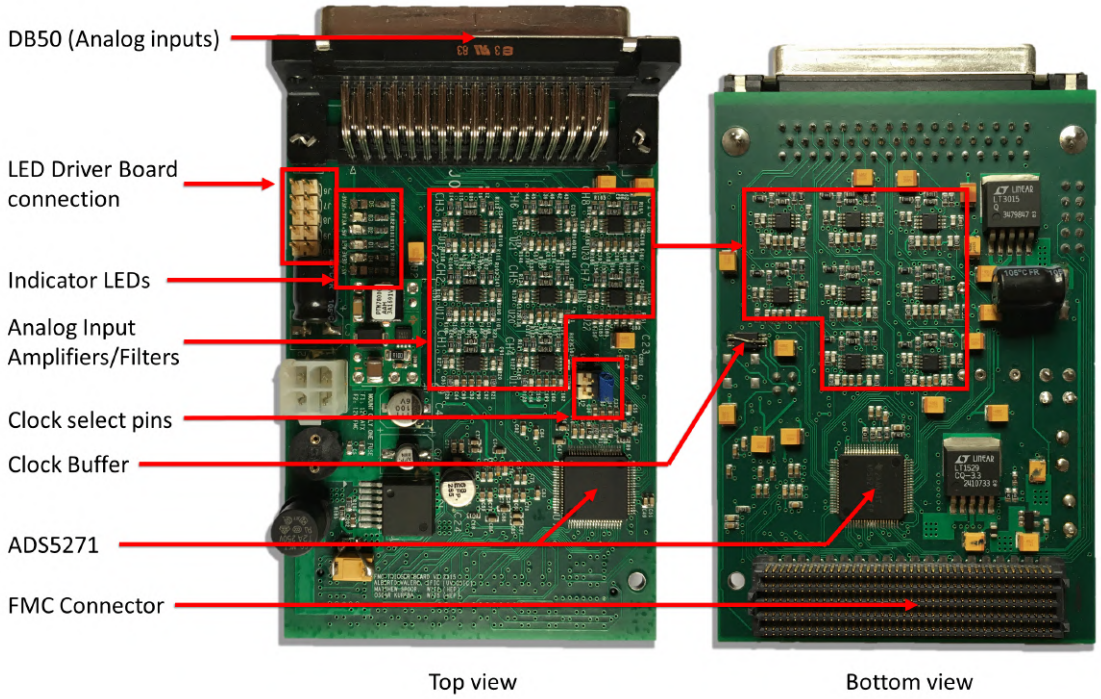


Figure 4.1: Labelled image of the final version of the ADC Trigger Board for PROMETEO.

PROMETEO needs to be able to read these analog signals and thus an analog-to-digital conversion needs to take place between the demonstrator and the PROMETEO mainboard.

By using the ADC system utilized in the MobiDICK-4 as a starting point, a new custom ADC Trigger board (Figure 4.1) was developed.

In addition to processing the Trigger signals from the front-end electronics, the new ADC board has new constraints and requirements based on the needs of the upgraded TileCal readout architecture and the Prometeo test-bench:

1. PCB size reduction: The ADC board needed to able to fit adjacent to the QSFP+ module when attached to the VC707 or future TilePPr. The ADC PCB physical dimensions were reduced to approximately one third the original

size (11cm x 8cm). Contribution: Matthew Spoor and Alberto Valero.

2. Circuit design revaluation and modernisation: The fundamental design of the new ADC board would remain the same but due the reduced size of the PCB and that some components had become outdated, the circuit diagram and part selection needed to be revaluated. Certain sections needed to be modified, redesigned, reused or removed. Contribution: Matthew Spoor.

3. Communication: Due to its availability on FPGA based platforms, versatility, compact size and ability to provide power, the FMC connector was selected as the route of communication between the ADC and FPGA. The FMC connection on the FPGA main board would provide ADC board with a means of data readout, control/configuration and power. Contribution: Matthew Spoor and Alberto Valero.

4. Power supply: The ADC board could now be powered directly from the FMC connection. The board power regulation circuits were completely redesigned to be compatible with new circuit design and FMC. Contribution: Matthew Spoor.

5. Firmware: The firmware used on the FPGA to manage and control the data readout and signal timings of the ADC was completely rewritten to be compatible with Virtex 7 FPGA system architecture found on the VC707 development board. The same FPGA is used on the TilePPr which should enable the ADC board and ADC firmware to be compatible with the TilePPr. Contribution: Matthew Spoor and Fernando Carrió.

6. LED driver board: Communication IO to the FPGA is limited on the VC707. As not all the resources on the FMC connection were used on the ADC board, it was decided that the extra IO would be used to create a connection for the

LED Driver board. This would allow the FPGA to communication to the LED driver board through a connection on the ADC board. Contribution: Matthew Spoor.

7. Visual Fault detection: A set of LEDs were added to ADC board as a simple visual means to determine ADC board was powered and working correctly. Contribution: Matthew Spoor.

4.3 ADC Trigger Board Overview

The ADC trigger board was created for the testing of the adder cards in the HL-LHC Hybrid Demonstrator module and the current TileCal front-end electronics. The ADC board conditions and digitises up to 16 differential analog channels coming from the front-end electronics [62]. These differential signals are sent to one of two 12-bit ADS5271 [63] 8-channel ADC ASICs to be digitised at 40 Mega Samples Per Second (MSPS). The 16 digitised signals are placed into a serial format and sent to the Xilinx Virtex 7 FPGA on the mainboard of the PROMETEO through the FMC connector.

A 40 MHz reference clock is produced by the FPGA and sent through the FMC to a Clock Buffer (Texas Instruments CDCLVC1102) on the ADC board to be distributed to the ADC5271 chips for digitisation, serialisation and synchronisation purposes. The serialised data produced by the ADS5271 is sent at a rate of 480 Mbps per channel, leading to a throughput of 3840 Mbps per ADC5271 and a total output of 7.68 Gbps for the ADC board.

The ADS5721 also produces a 40 MHz "Frame" clock and a 240 MHz "Bit" Clock that are sent to the Virtex 7 to be used for the de-serialisation and synchronization

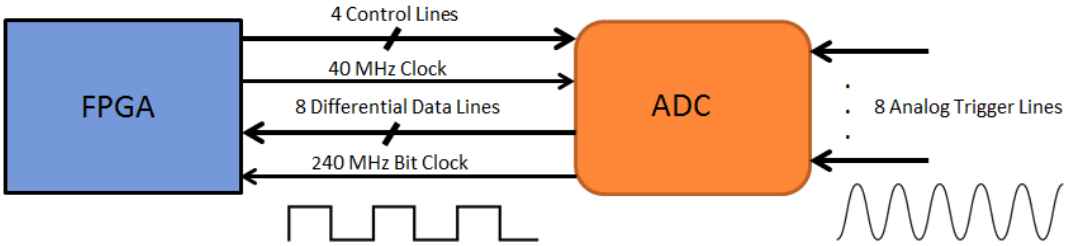


Figure 4.2: Communication layout between the Virtex 7 FPGA and a ADC271 ADC chip.

logic within the FPGA. Four control lines are used by the FPGA to configure the ADC chip. Figure 4.2 shows the communication lines between the FPGA and one of the ADC271 chips.

4.4 Circuit Design

The circuit design was completed using Cadence OrCAD capture. The design went through five iterations before the schematic was finalised. The full circuit design can be found in Appendix A.

4.4.1 Power stage

The ADC circuit was designed to be powered by a 12 V input. The 12 V can either be supplied externally through a 4 pin ATX connector or a directly from the VC707 board through the FMC connection. A power source can be selected by placing a fuse in one of the two fuse slots.

The 12 V supplies the power stage (See Figure 4.3) that comprises of multiple regulators used to provide the different voltages needed in the design. The digital and analog power regulators, traces, planes, and components were physical placed

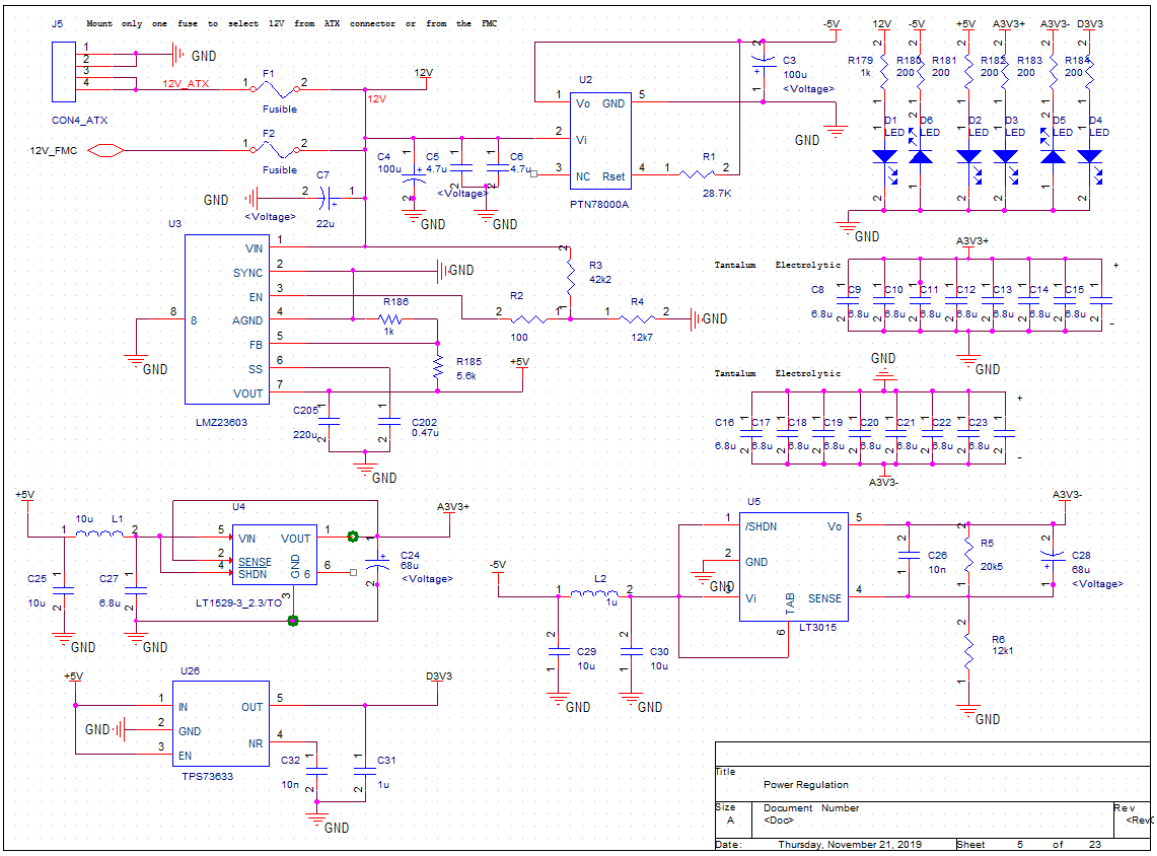


Figure 4.3: Power regulation circuit diagram of the ADC board.

apart from each other to prevent interference from the different domains.

Regulator	**Voltage**
LMZ23603	+5 V Analog
PTN78000A	-5 V Analog
LT1529-3	+3.3 V Analog
LT3015	-3.3V Analog
TPS73633	+3.3 V Digital

Table 4.1: Power regulators and their voltage outputs used for the different stages of the ADC board.

4.4.2 Analog stage

The analog stage of the ADC board is used to condition the muon and trigger differential signals so that they fall within the range of the ADC input threshold [53].

There are a total of 16 identical analog inputs (See Figure 4.4) on the board.

The board uses a 50 pin DB50 connector to receive the trigger inputs from TileCal drawers.

A THS4151 differential operational amplifier is used to set a gain of 0.5 using specific resistor values. The op-amp is also used to create active anti-aliasing filter with a cut off frequency of 20 MHz. A second pole is added to the circuit by adding a low pass filter set at the same frequency at the output of the circuit. This changes the transition from passing band to a stop band to -40 dB/dec.

Correct termination is used at the input and output of the analog stage to prevent signal reflections. The differential traces on the PCB were routed to have the same length to make sure all the analog channels would have the same delay.

4.4.3 Digital stage

The digital stage 4.5 of the ADC circuit uses two ADS5271 chips. The ADS5271 is an 8 channel 12-bit ADC that can sample analog signals up to 50 MSPS. The input signals from the analog stage arrives within the range of -1 V to +1 V on the differential lines. The ADC samples them and provides digital output with values ranging form 0 to 4095 in serial binary format. The digital outputs are differential and send data at a rate of 480 Mbps per channel.

The ADS5271 chip has 7 8-bit registers that are controlled through an I2C serial interface with 4 lines, SDA, ADCLK, CS, SCLK. One of these registers is used to configure the output settings of the ADC. The ADC outputs can be configured to a range of voltage ranges depending of the requirements of the FPGA. Additionally the ADC can be configured to produce specific training patterns that are used in

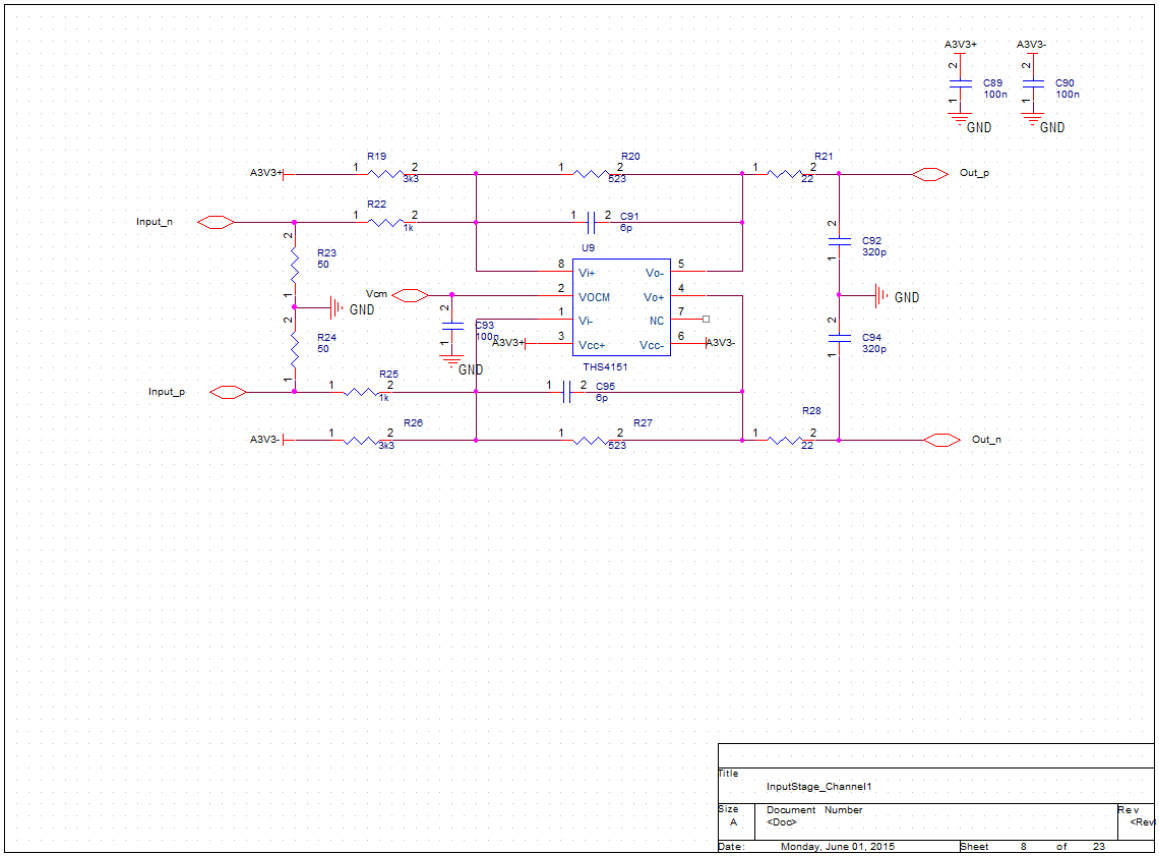


Figure 4.4: Analog circuit used to condition and filter a single trigger signal input before it is sampled by the ADC.

the start-up sequence with the FPGA to align bits and synchronise channels. The alignment and synchronisation process will explained in detail in the Firmware section 4.5.

4.4.4 Reference Clock

The reference clock used by the ADC for digitisation can be provided either from the mainboard (VC707) or a 40 MHz crystal oscillator mounted on the board (See Figure 4.6). It is not recommended to use the crystal oscillator due to the potential conflicting clock domains between the ADC and FPGA.

The clock can be selected using a set of pins on the ADC board (See Figure 4.6).

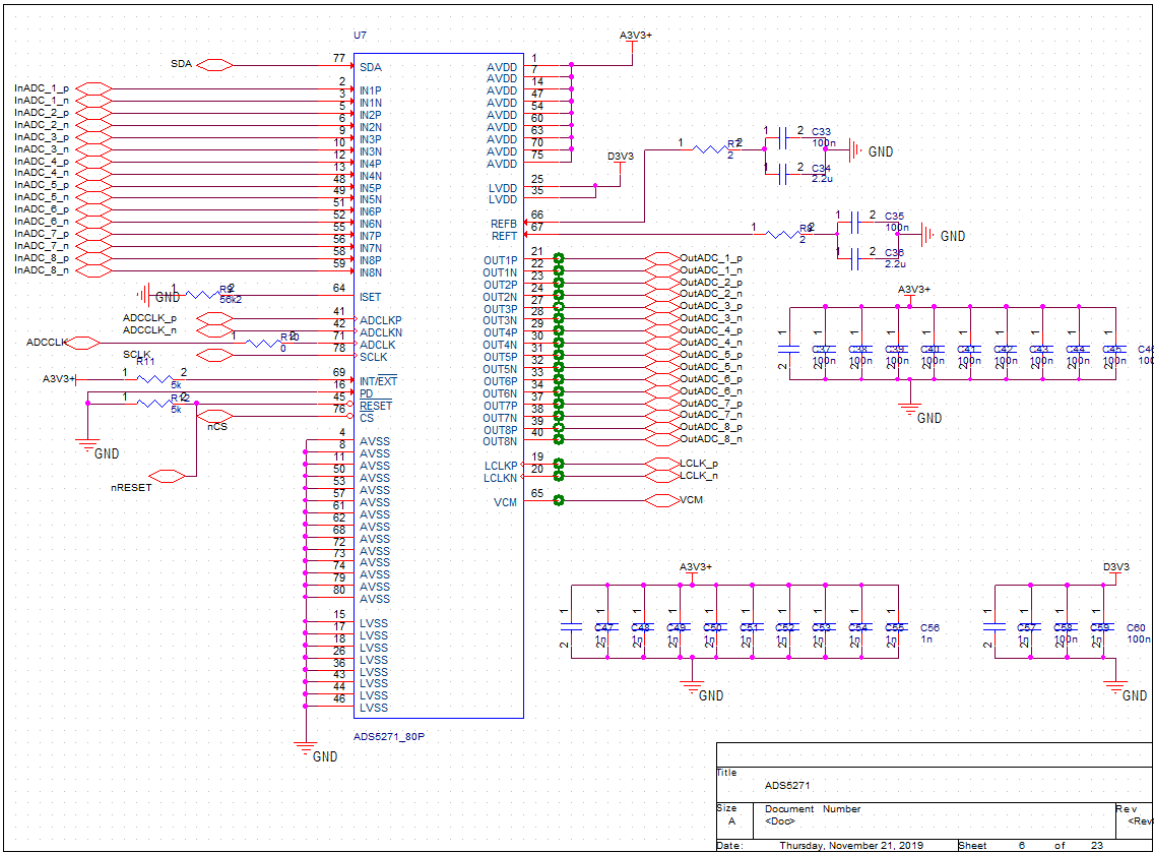


Figure 4.5: Power regulation circuit diagram of the ADC board.

The reference clock feeds a Texas Instruments CDCLVC1102 PW 8 3.3V LVCMOS clock buffer, which cleans the signal and adapts it to the correct logic levels before distributing it to the two ADC chips on the board. The ADS5271 chip uses the reference clock to produce two new clocks, a frame clock (40 MHz) and a bit-clock (240 MHz). These clocks are used to de-serialise the outputs of the ADC by the FPGA.

4.4.5 Printed Circuit Board

The Printed Circuit Board (PCB) layout for the ADC Trigger board was created using Cadence Allegro PCB designer. Once the circuit design was completed a full netlist of all the circuit interconnections could be generated and used to layout and route the schematic on the PCB.

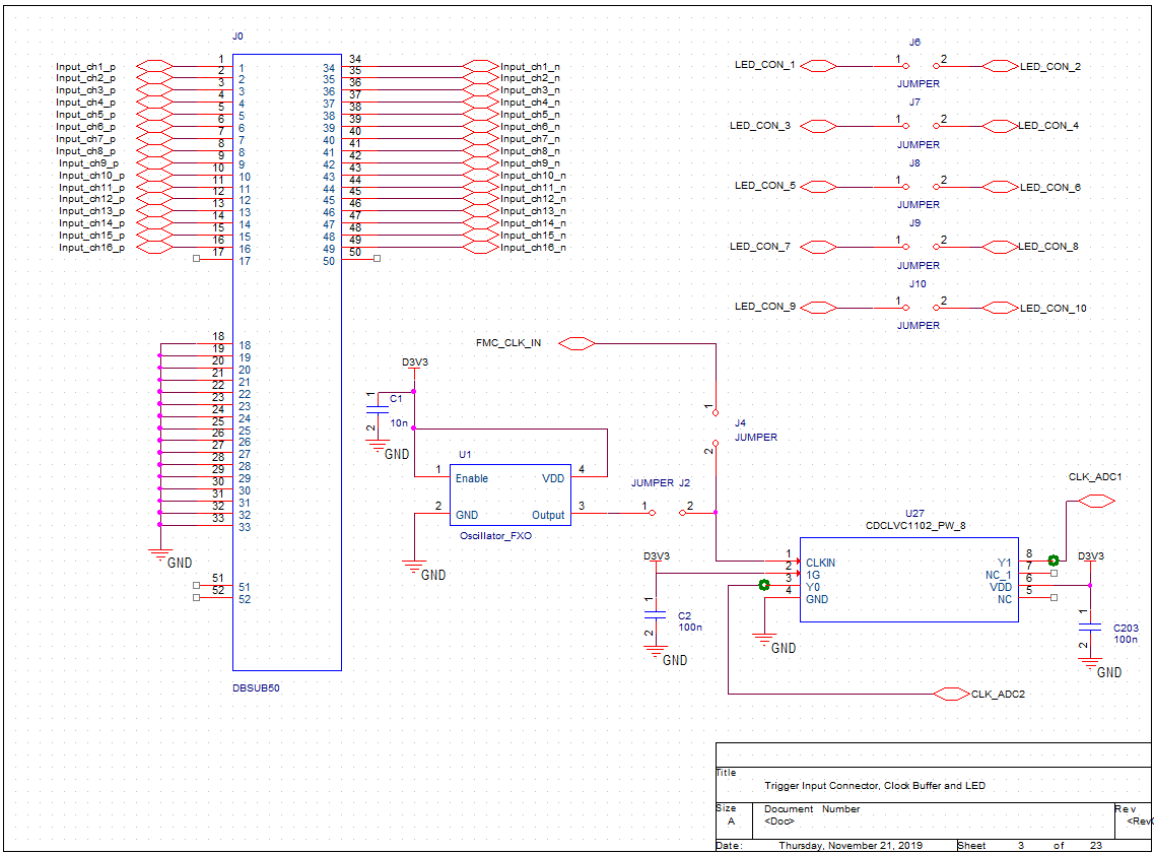


Figure 4.6: Circuit diagram: DB50 pinout (J0); Reference clock circuit (U1, U27); LED Driver Board connector.

The PCB was arranged into a four layer stack-up (See Figure 4.7). The TOP and BOTTOM layers were used to mount components and route the majority of the data signals. One internal layer (GND) is used as the ground plane for the analog circuity on the board. The second internal layer (POWER) is used to route the different supply voltages to the many components on the ADC board. All the signal traces are 300 micros thick and where designed to match the 50 Ohms characteristic impedance. Due to the size constraint of PCB it was difficult to equalise all the channel trace lengths. As mentioned later in Section 4.6.2 some channels exhibited possible timing issues that may be related to trace lengths.

The component footprint is the arrangement of pads used to physically mount component to the PCB. Footprints for each components had to sourced, with many being found in the Cadence libraries or online but several components had to have footprints created from scratch.

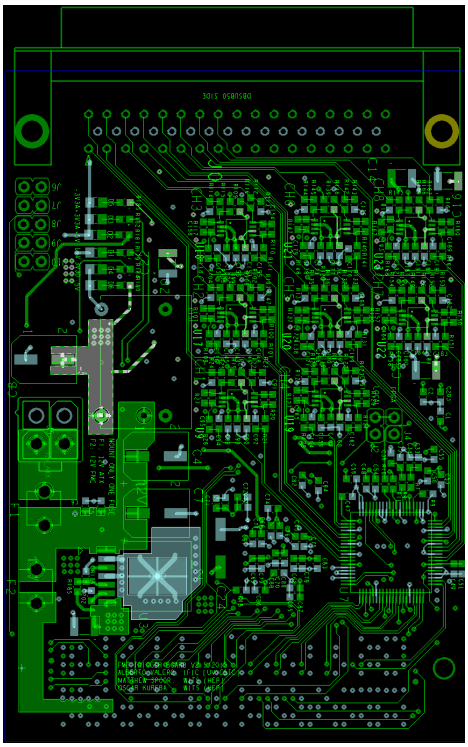
The digital and analog stages are deliberately separated as much as possible on the board to reduce signal interference where possible. The placement of the voltage regulators on the PCB can be problematic as they add to the Signal-to-Noise Ratio in the circuits. Extra care was needed when placing noise sensitive components and routing signals, especially clocks. The clock buffer and optional Crystal oscillator where placed on the bottom PCB layer farthest away from the power regulator circuits and had a common digital ground plane in the immediate PCB layer below. The clock tracks where also routed towards the edge of the board to avoid unnecessary signal interference.

The ADC board went through two prototype stages before a final design configurations was settled upon. Prototyping helped improve SNR throughout the board and we were able to discover several voltage regulation issues and improve board usability before it went for production. Six ADC boards were produced in South Africa and shipped to CERN. [1]

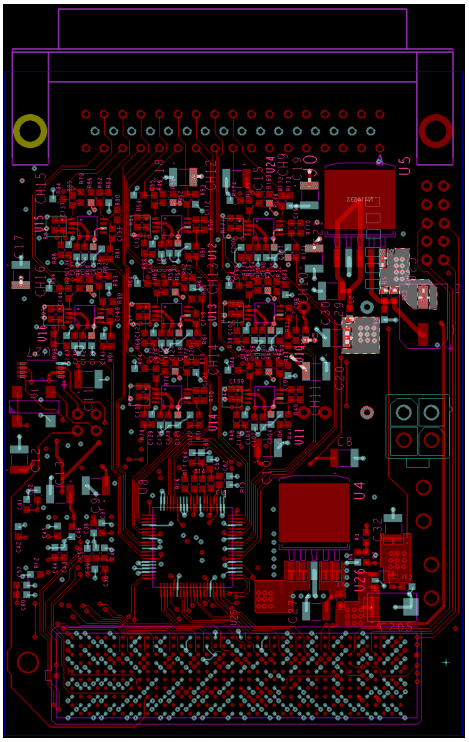
4.5 Firmware

All the hardware within the PROMETEO Test-bench is managed by the Xilinx Virtex 7 FPGA on the VC707 development board. Procedures such as data readout,

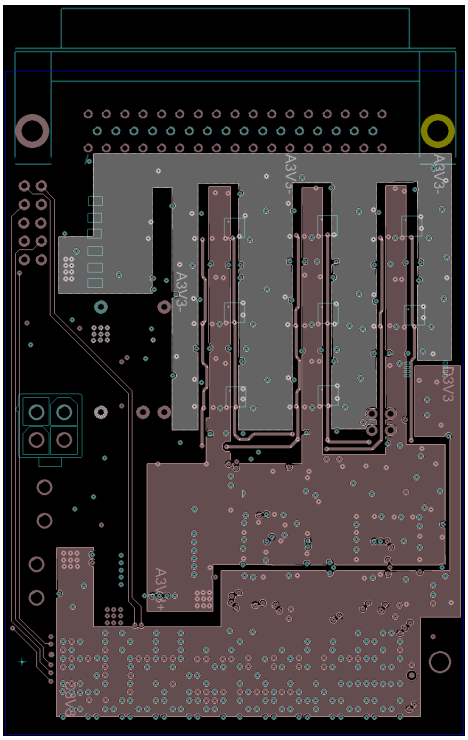
[1]The PCB was manufactured by Trax Interconnect (Pty) Ltd and assembled by Projects Concern (Pty) Ltd in South Africa



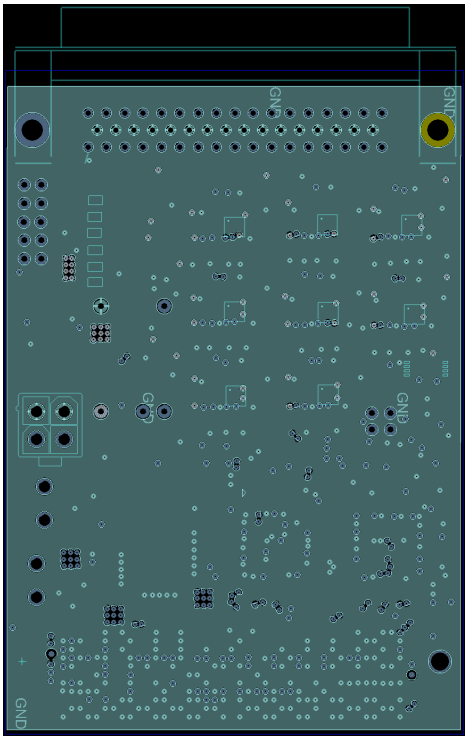
(a) Top Layer



(b) Bottom layer



(c) Power Plane



(d) Ground Plane

Figure 4.7: Four layer PCB design layout for the ADC board (Designed in Allegro PCB designer).

device configuration, device control, data storage and data packaging are managed by the FPGA.

Firmware enables engineers to describe the processes and structures that will be implemented within the logic of the FPGA, allowing FPGAs to repurposed to fit many electronic roles. The firmware language used to describe the logic within the PROMETEO FPGA was VHSIC Hardware Description Language (VHDL). The firmware code is interpreted by a compiler (Xilinx ISE) and is used to define the physical interconnections between logic within the FPGA.

4.5.1 Firmware Outline

The ADC board requires multiple firmware modules: de-serialisation module, configuration module (I2C interface), Storage in FIFO memories and IPbus module (See Figure 4.8).

There are a total of 16 digital differential channels produced by the ADC board, with each one needing its own readout module on the FPGA for data synchronisation and de-serialisation. The ADC board connects directly to I/O pins on the FPGA through the FMC connection on the VC707. The full Pinout table can be found in the appendix A.10.

The data from each channel comes in the form of a 12-bit binary (Range from 0 to 4096) that is sent serially (one bit at a time) at a rate of 480 MHz. This data stream of 1s and 0s needs to be de-serialised using by two ISERDESE (Serial/ De-serialiser) IPCore modules (See Figure 4.9) to create a single 12-bit Word. ISERDES modules are dedicated hardware logic within the FPGA designed to de-serialise a data stream.

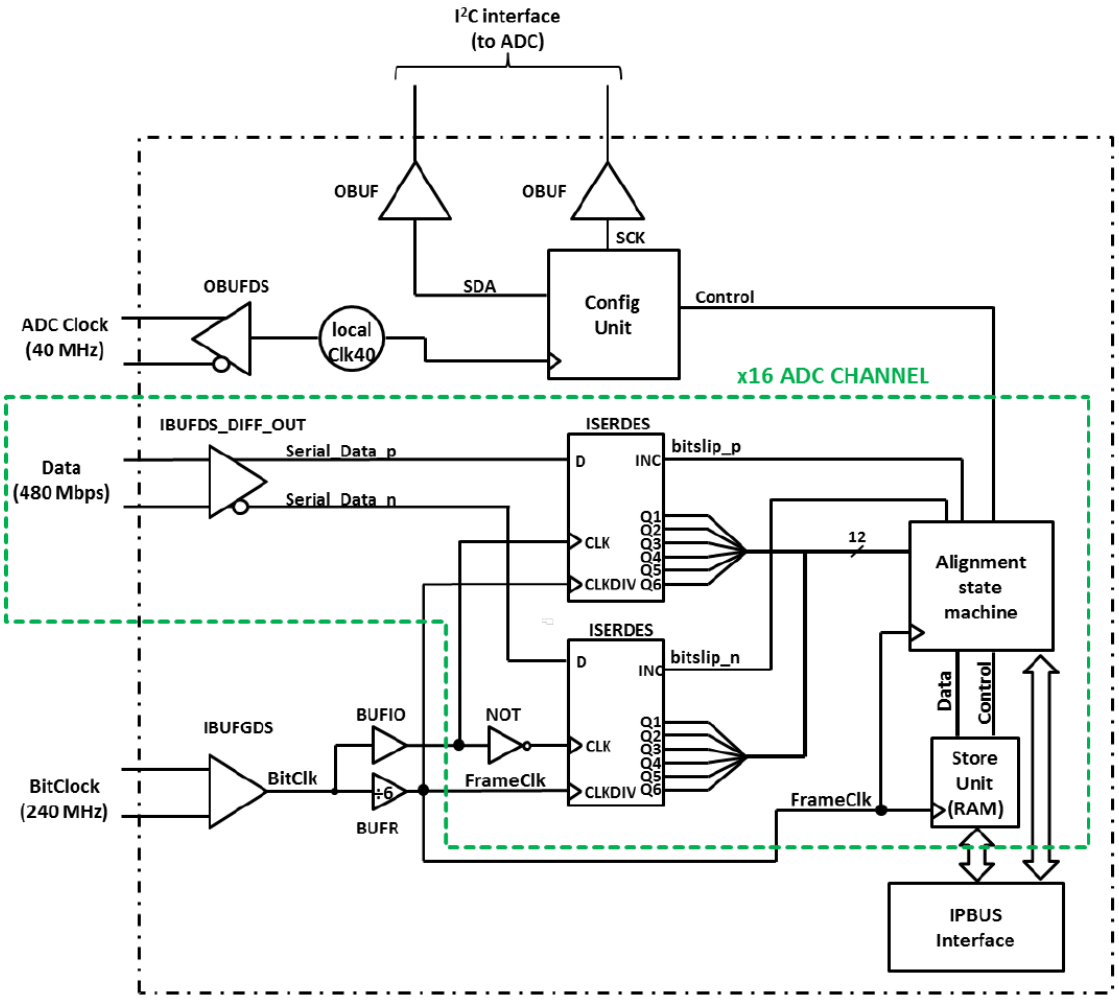


Figure 4.8: Block diagram of the firmware used for ADC trigger board of PROMETEO.

A challenge when building such a system arises when separating each 12-bit data sample from the one before or after (data frame), as there is no data header or gap between 12-bit data sample. Another issue is that the samples from the 16 channels do not all arrive at the SERDES modules at exactly the same time. This is often caused by different signal delays in each channels due to the routing on the ADC board and within the FPGA logic. To overcome this problem the ADCs on the trigger board need to be configured during the start up and reset to send specific test patters. These patterns will be used to find the correct data frame for each channel and to synchronise the timing of the 16 channels.

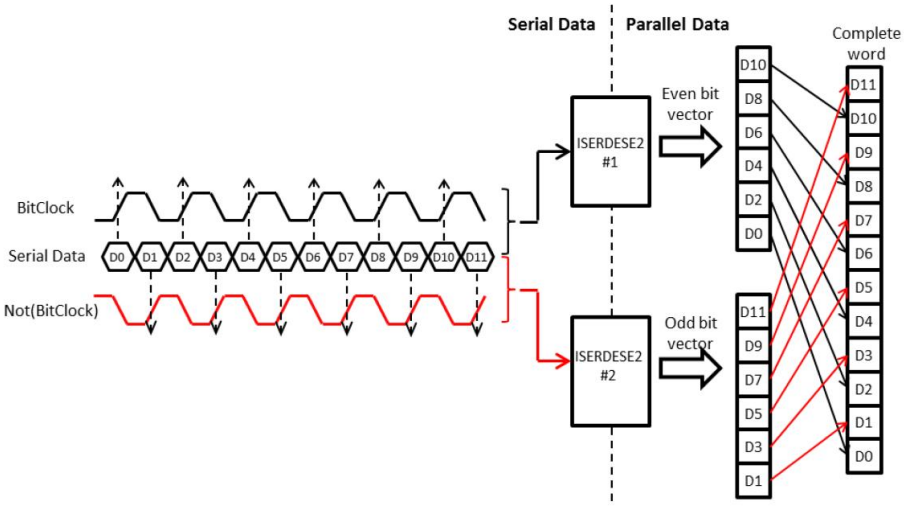


Figure 4.9: Two ISERDESE modules are used to de-serialise a data stream to create a complete 12-bit word. The data stream is divided into even and odd bits and shared between the SERDESE modules. The outputs are combined to create a single 12-bit word (data sample).

A set of Finite State Machines (FSM) within firmware are used to manage the processes within the FPGA and to configure the ADCs to allow channel synchronisation and alignment. Once channels have been synchronised and aligned, the ADC board is ready to begin receiving real data from TileCal front-end. Data from each channel is stored in First-In-First-Out (FIFO) memories on the FPGA. Each FIFO stores 128 samples, once that memory is full it will begin to overwrite the oldest sample. The number of samples per channel can be modified and is generally limited by the resources on the FPGA.

If the FSM receives a trigger request from PROMETEO user during a test procedure, samples stored in the FIFO memories will be sent to registers on the IPBus module [61] to be packaged and transferred through Ethernet to the PROMETEO mini PC. The data from ADC board will then be analysed and processed to be used to determine the functionality of the front-end electronics.

4.5.2 Firmware layout

As mentioned section 4.5.1, an assortment of firmware modules and IPcores are all managed by a complex FSMs within the FPGA firmware. This subsection will go into further detail of how the whole process takes place within firmware.

4.5.2.1 ISERDESE modules

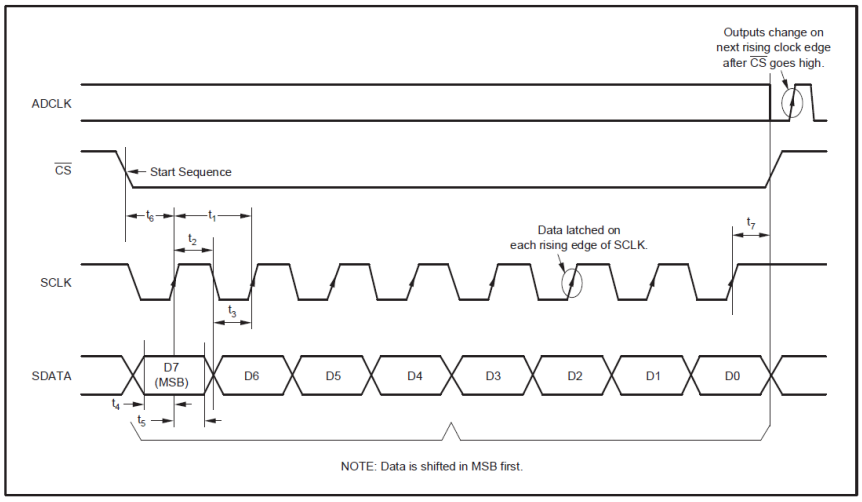
The data samples from each of the 16 ADC board inputs are 12-bits in length and arrive at a rate of 40 MHz, equivalent to 480 Mbps (Figure 4.9). Each data channel is mapped to specific I/O pins within the FPGA that are linked to two ISERDES2 [64] modules.

The samples arrive at the ISERDESE modules as a steam of bits (Serial data). The ADC produces a 240 MHz "Bit" clock that is used to synchronise the ISERDESE modules with the bit streams. By dividing the bit-clock by six a 40 MHz Frame clock is created to synchronise with data samples in the bit stream.

The system uses an interleaved method to divide the 12-bit data stream into EVEN and ODD bits that are shared between the two ISERDESE modules. This is done by having one ISERDESE module latching to the rising edge of the bit-clock and the other to the falling edge, essentially doubling the clock rate to 480 MHz. Each module is responsible for process 6 bits of the serial data sample. The outputs from the two modules are combined to form the complete 12-bit word.

4.5.2.2 Configuration Module

The FPGA can configure the ADS5271 chips through an I^2C interface via the FMC. An 8-bit configuration register on the ADCs determine the signals outputs that are



PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	50			ns
t_2	Serial SLK High Time	20			ns
t_3	Serial CLK Low Time	20			ns
t_4	Data Setup Time	5			ns
t_5	Data Hold Time	5			ns
t_6	$\overline{CS}$ Fall to SCLK Rise	8			ns
t_7	SCLK Rise to $\overline{CS}$ Rise	8			ns

Figure 4.10: I^2C Interface Timing for the ADS5721 [63].

sent to the FPGA. Each ADS5721 ASIC has 7 configuration registers that determine the behaviour of the ADC, e.g. signal output, differential connection type etc.

The config module is used to send configuration commands from the FPGA to the ADC board through a I^2C communication interface. These commands are used to initialise the ADC chips during start-up, reset and channel alignment. The config module sends the following signals to the ADC board: The ADC clock (40 MHz), Serial Clock (SCLK), SDATA and $\overline{CS}$.

The different signals, timing rules and signal tolerances needed to configure the ADC correctly are defined in the ADS5721 data-sheet [63]. The timing protocol used to send commands can be seen in figure 4.10 .

4.5.2.3 Alignment module

Every time the PROMETEO is powered on or reset the alignment module will start its FSM to get the ADCs and FPGA ready for data taking. A flowchart of the main alignment FSM can be seen in 4.11.

The process of alignment for each channel begins with the Word Alignment, where a test pattern are used to find the data Frame (beginning and end of a sample in a bit stream). If the Word Alignment process is successful then Bit alignment process will begin. Bit alignment is used to make sure the EVEN and ODD bits from the two SERDES modules are in the correct order.

If both alignment processes are successful, the ADCs will be configured to begin taking data samples from the analog inputs. At this stage the system is ready to begin normal PROMETEO testing operations. Data samples are stored in FIFO memories while they wait for a Trigger request form the PROMETEO user.

The system will remain in this state until a reset or Re-alignment command is received. A full flow chart of the Alignment FSM in firmware can be found the Appendix A.10 .

4.5.2.4 Word Alignment

The Word alignment FSM flowchart can be seen in figure 4.12. The process begins by signalling the config module to configure the ADCs to send the parity alignment pattern or "Synq" (111111000000) test pattern. The pattern allows the FPGA to easily determine the sample Frame of the bit stream.

The output from the SERDES modules is compared to the pattern to see if it

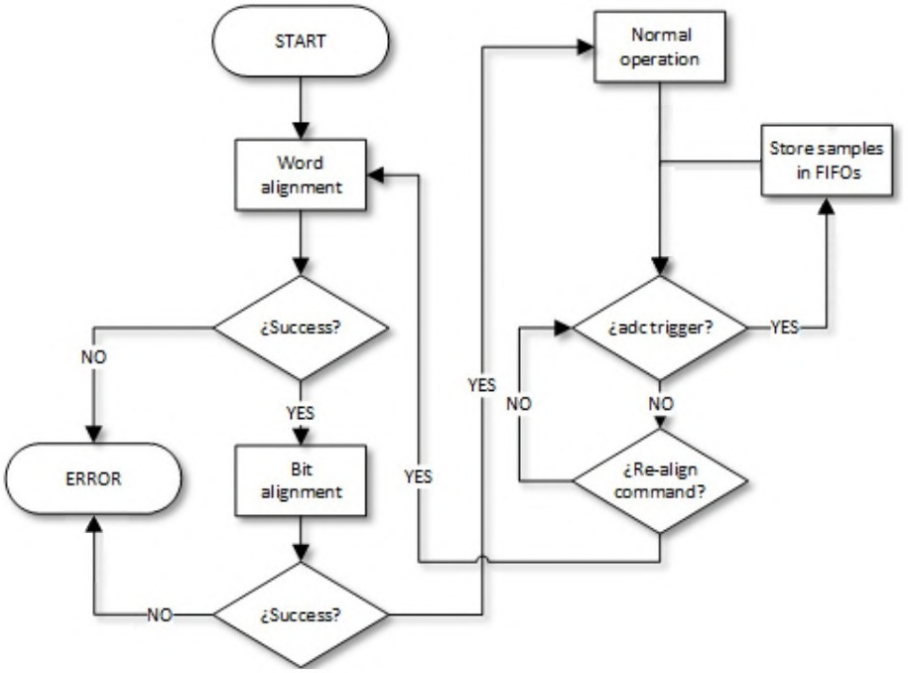


Figure 4.11: Alignment FSM flowchart.

has been correctly reproduced. In many cases the test pattern will not be correctly aligned and may look something similar to "111100000011", for example. This will require the bits of the output to be shifted (bitslip) one at a time until the pattern is correctly aligned, e.g. 111100000011 → 111110000001 → 111111000000. Once the correct pattern has been detected the Bit Alignment process can begin.

4.5.2.5 Bit Alignment

The Bit alignment FSM flowchart can be seen in figure 4.13. The process begins by signalling the config module to configure the ADCs to send the bit alignment pattern or "Deskew" (010101010101) test pattern. As the ISERDESE modules have been configured read ODD bits and EVEN bits separately, the respective outputs should be "111111" and "000000". If this is not the case such that the respective outputs are "000000" and "111111", the two outputs will be swapped.

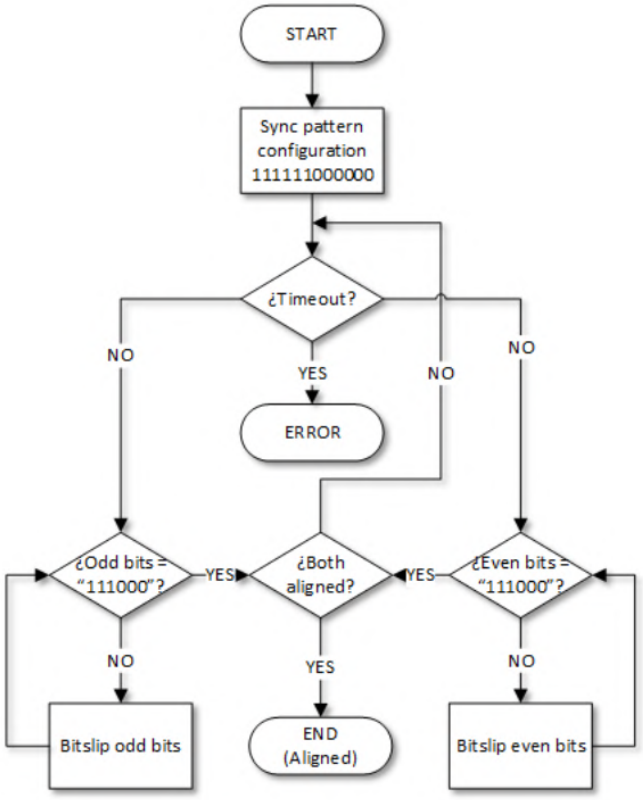


Figure 4.12: Word Alignment FSM flowchart.

Once this process is completed, the channel should be aligned and synchronised with the other channels. At this stage regular data sampling can now take place.

4.5.2.6 FIFO and IPBus

Once the alignment process has completed, Normal operation can begin. The process begins by signalling the config module to configure the ADCs to start taking data samples of the analog inputs from the board. The data samples for each channel will arrive at the FPGA, undergo de-serialisation and be stored in FIFO memories. The FIFO memories for each channel are designed to only hold 128 samples at a time. Once the memory is full it will begin to overwrite the oldest sample in the memory i.e. First In First Out.

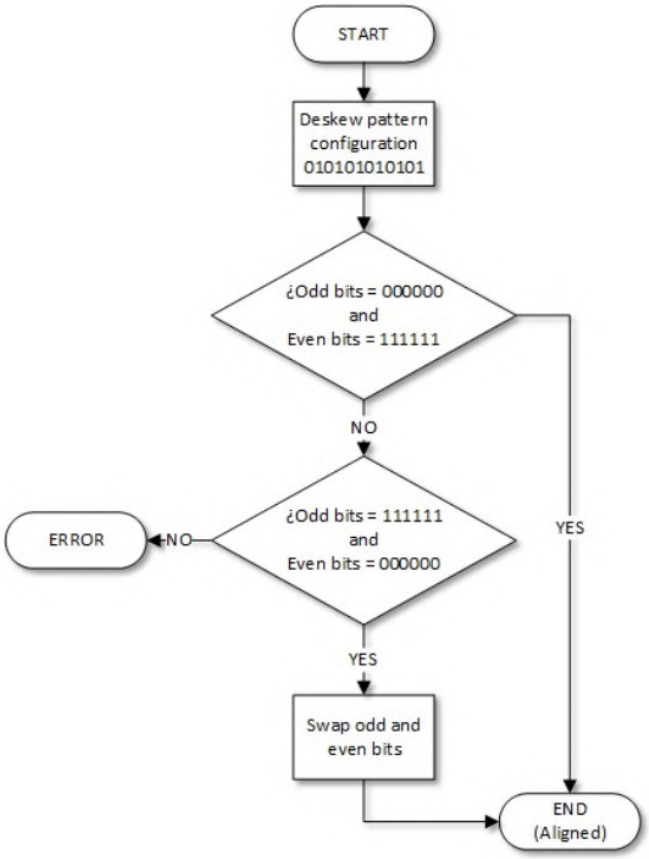


Figure 4.13: Bit Alignment FSM flowchart.

This process will continue until the FPGA receives a Trigger request from the PROMETEO user. After the request has been made, data from the FIFO memories will be moved to temporary buffers within the IPBus module. The IPBus module is pre-existing firmware module developed at CERN to standardise communications with FPGA enabled devices inside a closed network in a platform independent way [61]. The IPBus module will package the samples using IPBus protocol to be sent via Ethernet to the PROMETEO mini-PC for further processing.

4.6 ADC Prototyping and Testing

When first testing a new prototype board it must be visually inspected to see that all the components are in place and that they are correctly mounted to the PCB. After

this step it can be powered via an external power supply as to not damage FPGA. At this stage each power regulator must be checked to see that the output voltages are at the correct level. Next the input voltages for each component stage can be checked to see if they are receiving power and that it is at the correct voltage level. It is important when first powering the PCB board to pay attention to any excessive heating and the smell of burning. This is generally a clear sign of a sort circuit or a design problem. Only once it has been confirmed that the board voltages are correct and that each component is receiving the appropriate power should one consider connecting it to the FPGA development board. Fault on the ADC board could easily damage the FPGA development board. The same testing procedure will be repeated using the power supplied via the FMC connection. Once the ADC board is given the Ok, the testing of the digital communication between the FPGA and ADC can begin (Section 4.6.2.

The ADC circuit design went multiple iterations during development, making minor fixes and enhancements to the circuit as well as completely replacing certain sections. Many changes were made during prototyping but the most significant ones included the redesign of the power regulator circuit and the addition of the 10-pin signal output for the LED Driver. The physical ADC board went through two prototypes productions before a final layout was settled. The complete circuit design can be found in appendix A.

Early testing of the first prototypes found flaws in the ADC circuit design and the PCB. Issues with the voltage regulators were quickly discovered: overheating, unstable and signal noise generation within the analog and digital circuits. Temporary fixes were made on the first prototypes by replacing some of the regulators and attaching heat-sinks (See Figure 4.14 a), but in later designs the regulator had to be

replaced and their circuits redesigned. To assist with overheating, enlarged ground pads were added to some of the voltage regulators to conduct heat away from the circuit and to distribute it evenly around the PCB.

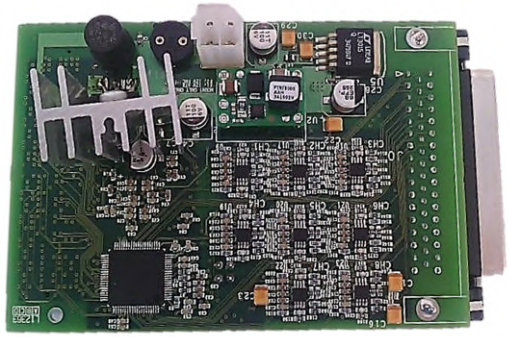
To make it easier to troubleshoot the Power stage, a set of LEDs were added to the next prototype that would illuminate if they were receiving current from their respective voltage regulators. Other smaller problems arose due to bad circuit layout, incorrect PCB footprints (See Figure 4.14 b), misplaced parts and miscommunication with the manufacturer.

In a second prototype, clock distribution problems were found causing one of the ADC chips to behave erratically. The 40 MHz reference clock that fed the ADCs was distorted (See Figure 4.14 c) due to bad signal routing and component mounting on the PCB. While troubleshooting sources of signal noise in analog channels, a prototype ADC board short circuited. Infrared photography was used to locate the damaged part so that it could be replaced (See Figure 4.14 d). Overall, prototyping was successful, several major problems were found, additional functionality was added and Signal-to-noise ratio was improved.

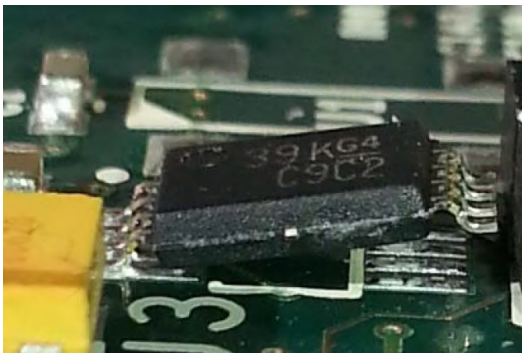
Once the PCB design had been finalised, six ADC boards were produced locally in South Africa and where shipped to CERN for use in PROMETEO.

4.6.1 Firmware Simulations

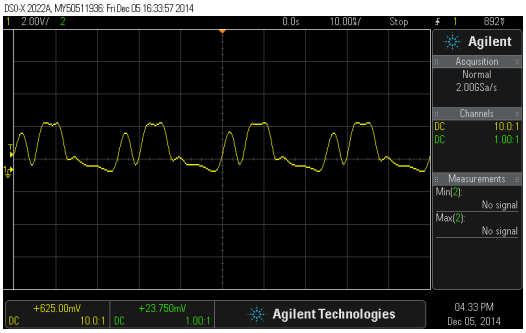
As introduced before, the firmware development and testing for the ADC board was done using Xilinx ISE design suite using the hardware description language VHDL. The firmware consists of simple modules and proprietary IPcore connected together to form larger more complex mechanisms. Modular firmware allows VHDL modules



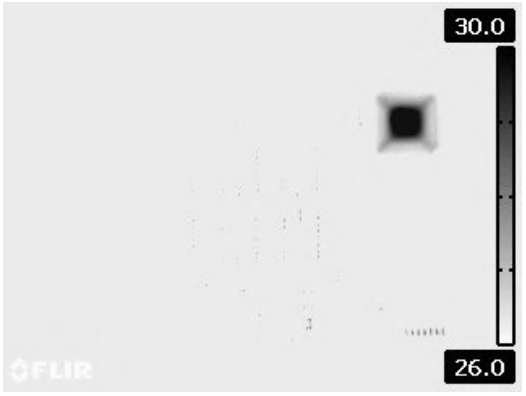
(a) Modified voltage regulator with heatsink.



(b) Incorrect Clock buffer PCB footprint.



(c) Distorted 40MHz ADC Clock.



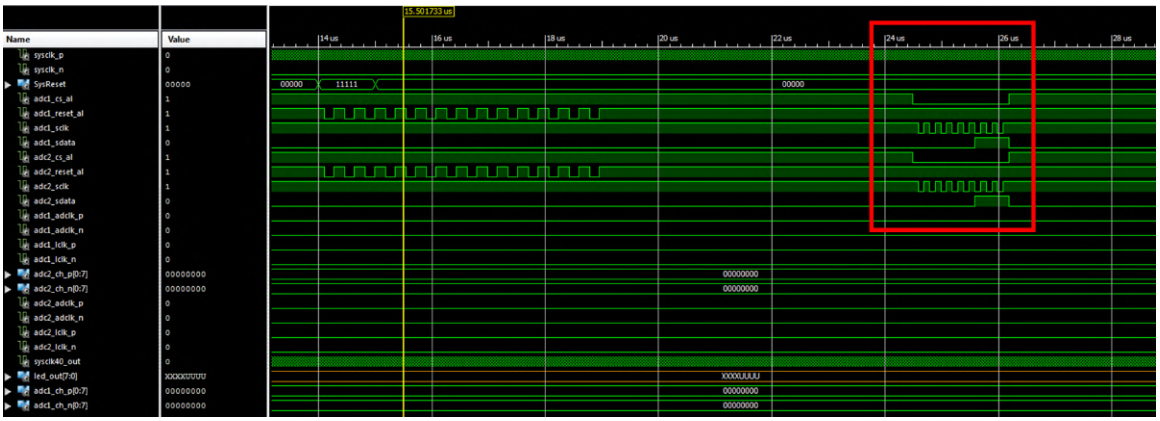
(d) Infrared image of ADC board with short circuited ADC.

Figure 4.14: PCB prototyping and testing issues.

to be tested independently in simulation before they are included in the Top level design of the project. Modularity also allows sections of code to be reused numerous times, e.g. ,the same readout module can be implemented several times for each of the 16 input channels.

Xilinx ISE ISim is a robust simulator tool within the ISE design suite. Users are able to build virtual test-benches within the ISim to simulate external signals, waveforms, firmware modules, clocks, etc. This enables one to analyse how the code functions as well as debug. Figure 4.15a is a successful simulation of the config module sending signals to the two ADC chips to reset them before configuring them to send the bit alignment (deskew) pattern. The red box shows the deskew configuration pattern sent to the two ADCs.

Figure 4.15b demonstrates the complete Alignment FSM used to configure an ADC with a single channel. The FSM begins firstly by resetting the ADC chip before requesting that the WORD alignment process begins. The Word Alignment process begins and the ADC is configured to send a parity alignment (synq) pattern (0b000000111111) to the FPGA. The sample pattern will generally arrive out of order, e.g. , 0b111000. The channel data output is shifted a bit at a time until the SYNQ pattern is seen, causing the DATA VALID flag be set, else an error flag will be set. Once the DATA VALID flag is seen the Bit Alignment process begins and the ADC is configured to send a DESKEW pattern (0b10101010101010) to check if the odd and even bits of the output are correct. If the FSM determines that odd and even bits are not in the correct position, they will be swapped. Again the DATA VALID flag will be set once the pattern is correct, else the Error flag will be set. The entire alignment process will happen simultaneously with each of the 16 channels in the full ADC system.



(a) Simulation: Config FSM with data signals to two ADC chips. Configure ADCs to produce Deskew pattern (Word Alignment).



(b) Simulation: Alignment FSM with data signals for one ADC with a simulated output of a single channel.

Figure 4.15: Simulations created in Xilinx ISE ISim to test ADC firmware.

4.6.2 System verification

System verification involves testing the ADC board, FPGA and FPGA firmware as a single unit. Initial testing mentioned in previous subsections involved examining the firmware and ADC board in isolation through simulations and prototyping. This subsection looks into viewing how the two systems interact by comparing simulations to actual data readouts done in the lab.

In order to troubleshoot processes and communications between the FPGA and

the ADC, one needs to be able to view the data signals that are sent and received. Many of the data signals, both analog and digital, are difficult or impossible to probe directly using a high-speed oscilloscope, because it will require additional bit decoding. Signals such as those sent directly between the ADC chips and the FPGA would need to have probes directly attached to the pins of the ADS5271, risking damage to the board and possible signal interference.

A simpler method to view these high frequency signals is to use the Xilinx ISE ChipScope Integrated Logic Analyser (ILA) module. The ChipScope ILA module allows users to view the real-time values of signals and memories within selected parts of the FPGA.

4.6.2.1 ADC setup, configuration and signal alignment

The process of configuring the ADC for data readout requires four commands to be sent successfully through I^2C: ADC reset, parity alignment (Synq), bit alignment (Deskew) and Data sampling commands. The process is controlled by a FSM defined in section 4.5 and the simulation of the process can be seen in Figure 4.15.

A Chipscope module was configured in firmware to monitor the primary signals used within the FSM. Figure 4.16 is a signal output from ChipScope Pro during the ADC setup/alignment process. The table displays the value data signal as time progresses. The important signals to note in the figure: ch1 to 16 are the digital outputs from each ADC channel displayed in Hexadecimal format; RESET_ADC, CS_ADC, SDATA_ADC and SCLK_ADC are the signals sent to configure the ADC chips.

The ADC setup in Figure 4.16 is divided into five phases:

1. The ADC has been reset; ADC channel outputs are unaligned.

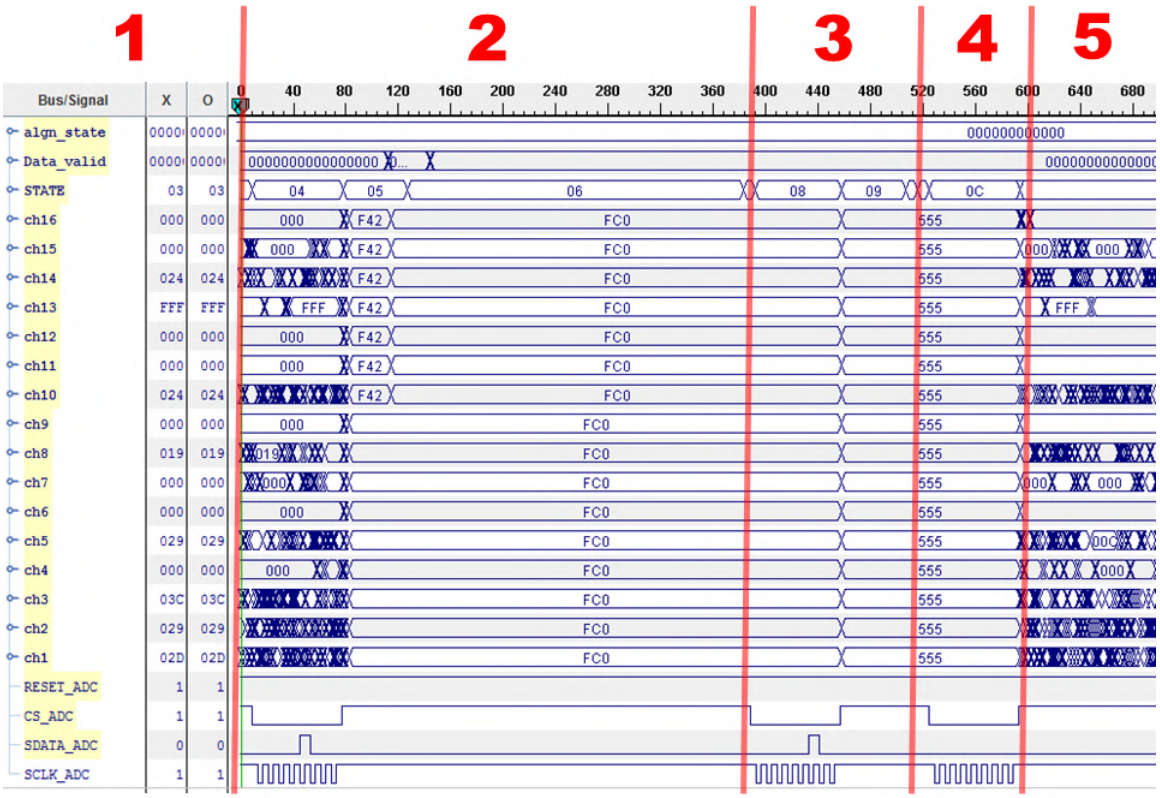


Figure 4.16: 16 channel ADC configuration viewed in Xilinx Chipscope Pro.

2. Word Alignment: The Synq command is sent to the ADCs; ADC outputs are configured to produce the Synq pattern; channel outputs are shifted; channel outputs match the correct pattern (0xFC0 → 0b111111000000); word Alignment is complete.

3. Bit Alignment: The Deskew command is sent to the ADCs; ADC outputs are configured to produce the Deskew pattern; channel outputs match the correct pattern (0x555 → 0b010101010101); bit Alignment is complete.

4. Normal operation: The alignment process has completed; ADC is configured to start sampling the analog inputs.

5. The ADC board is ready to begin taking data samples.

4.6.2.2 ADC channels analysis

Once it is confirmed that digital communications between the ADC and FPGA were working correctly such that the Alignment process is successful, the testing of the analog stage of the ADC can begin.

Figure 4.17 shows the ADC channels after alignment has completed and there is no analog input. It can be seen in the figure that despite the input signal being 0 V there is still minor variations due to possible noise generated by the ADC board and surrounding testing environment. Additionally each channel has a slight signal offset from zero.

Pedestal tests. Each ADC channel will have a certain signal offset such that if all the channels received the same signal, the recorded signal received by the FPGA will be slightly different. This can occur due to tiny differences in the signal routing, slight differences impedance or a combination of many effects. Even identical components may have tiny resistive differences or behaviours. Applying a constant voltage to a channel will clearly demonstrate the signal offset. These offsets can be recorded later subtracted from the signal to achieve a more consistent and accurate result.

The first pedestal test involved inserting a 0.5 V voltage signal to get a baseline for each channel. Figure 4.18 shows results of the 0.5 V test for ADC 1. Figure 4.19 shows results of the 0.5 V test for ADC 2. Table 4.2 shows a summary of the results from the pedestal test.

Overall the results where good and consistent throughout most of the channels. It can been seen from the table 4.2 however that Channel 13 is completely satu-

Channel	Average ADC Count
1	685
2	666
3	672
4	650
5	672
6	652
7	659
8	652
9	646
10	658
11	646
12	644
13	4000+
14	658
15	654
16	NA

Table 4.2: Table summarising the pedestal test results for each ADC channel. 0.5 V baseline

rated, reading the maximum possible ADC count. This probably occurred because the analog input of the ADC for that channel was above the 3.3V input threshold [63]. This could be due to a faulty component, PCB manufacturing error or design fault. Further analysis of the channel will be needed to correct the problem. Channel 16 demonstrates a timing issue. The sample frame used to separate individual samples received by the SERDES module on the FPGA is not synchronising correctly. Flaws within the timing constraints in the FPGA may cause the sample frame to shift causing single bits from next sample to be selected. This will cause the channel to have short stable moments before jumping erratically when a shift occurs. This issue can be corrected in subsequent firmware releases.

Frequency tests. The next set of tests involved inserting differential analog signals into the ADC board using a signal generator. All differential analog testing

signals were generated using a IFR 2025 9 kHz to 2.51 signal generator [65] provided by CERN. The analog inputs were injected directly into the DB50 connector on the ADC board one channel at a time.

Figures 4.20 and 4.21 show how the each channel responds to a 1 MHz sinusoidal wave (0.2 V_{pp} and 0.4 V offset). Table 4.3 summarises the results from this test. The maximum and minimum ADC count is used to calculate Root Mean Square (RMS) of the Sine wave. If we ignore channels 13 and 16 as they have been identified as being problematic, the RMS is consistent throughout the channels. With a maximum difference of less than 4 ADC counts. Again channel 13 was completely saturated and channel 16 demonstrated the same timing problems raised in the previous test.

Channel	**Min ADC Count**	**Max ADC Count**	**RMS**
1	224	644	148,5
2	218	641	149,6
3	235	653	147,8
4	206	629	149,6
5	218	635	147,4
6	206	629	146,6
7	211	632	148,8
8	209	632	149,6
9	206	629	149,6
10	212	633	148,8
11	202	627	150,2
12	203	627	149,9
13	NA	NA	NA
14	212	632	148,5
15	212	633	148,8
16	NA	NA	NA

Table 4.3: Table summarising the frequency test results for each ADC channel. 1 MHz sinusoidal wave (0.2 V_{pp} and 0.4 V offset)

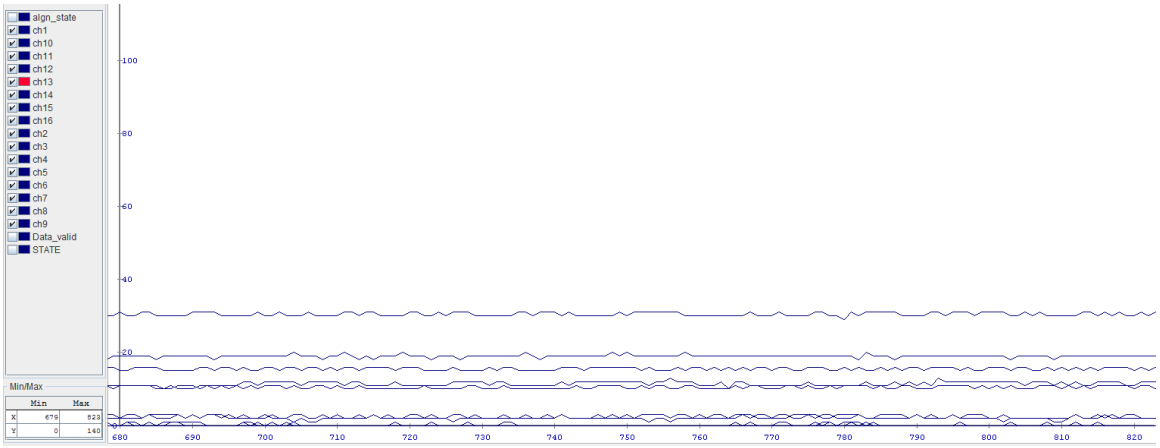


Figure 4.17: ADC channel outputs after alignment with no analog input (ADC counts VS Time ns).



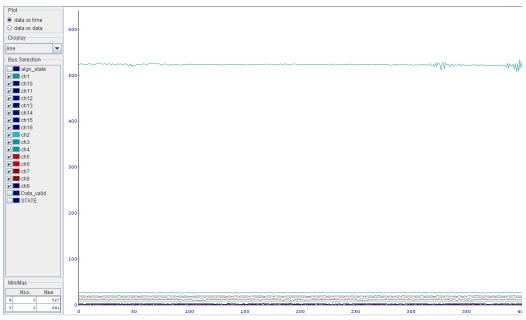
(a) Channel 1



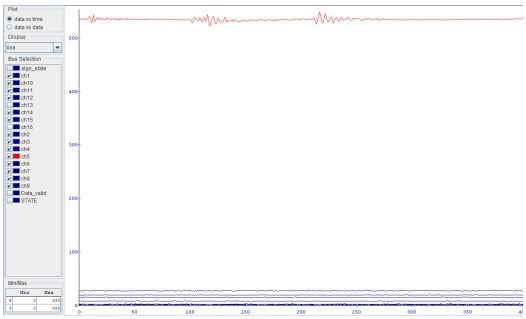
(b) Channel 2



(c) Channel 3



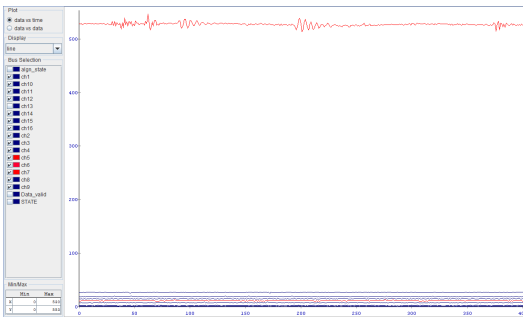
(d) Channel 4



(e) Channel 5



(f) Channel 6

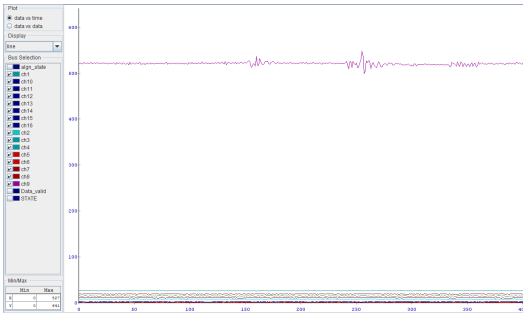


(g) Channel 7

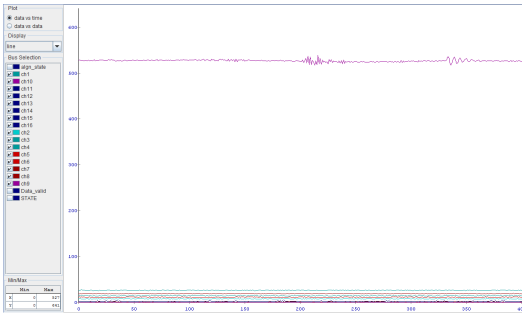


(h) Channel 8

Figure 4.18: Pedestal ADC 1 (0.5V).



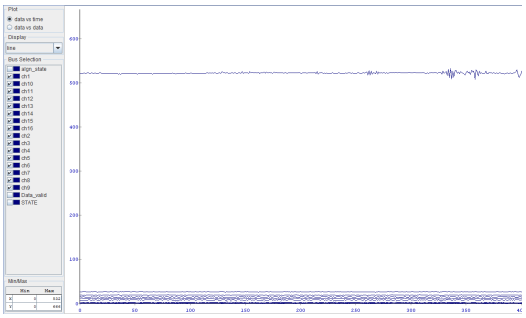
(a) Channel 9



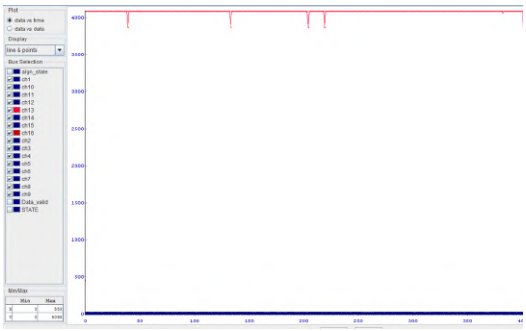
(b) Channel 10



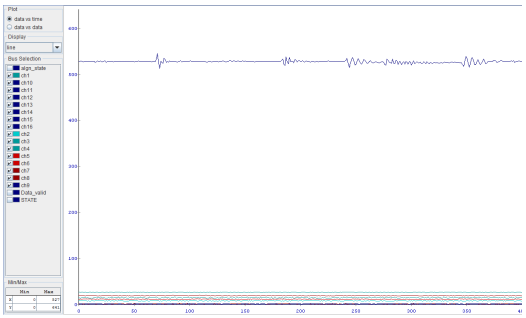
(c) Channel 11



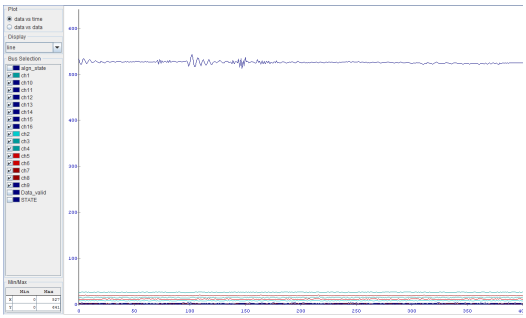
(d) Channel 12



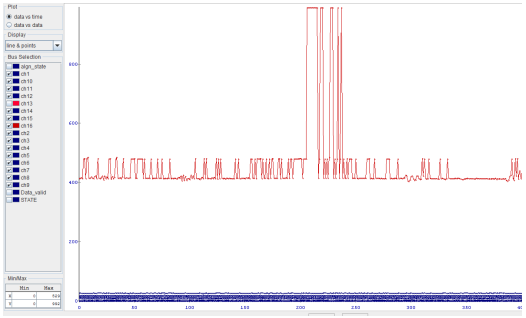
(e) Channel 13



(f) Channel 14

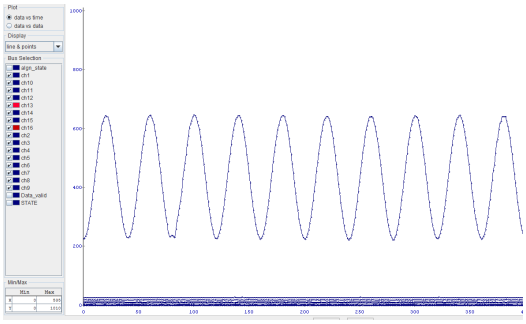


(g) Channel 15

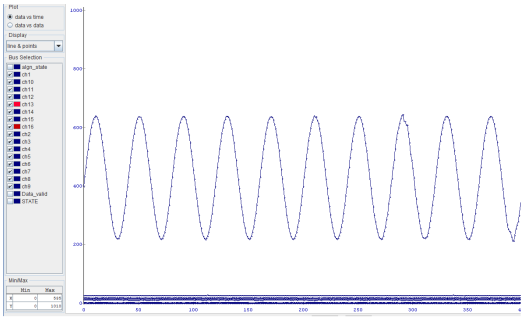


(h) Channel 16

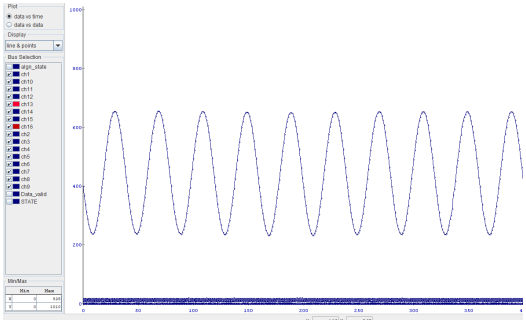
Figure 4.19: Pedestal ADC 2 (0.5V).



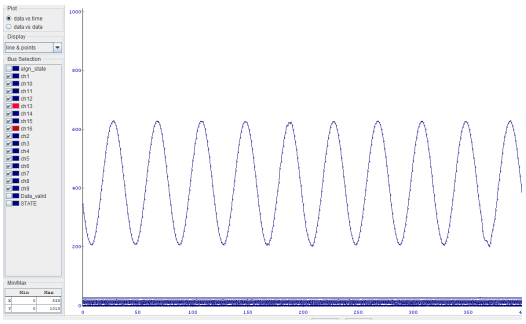
(a) Channel 1



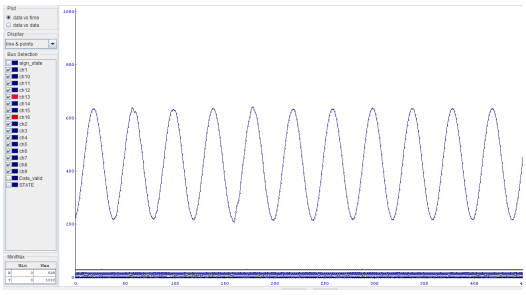
(b) Channel 2



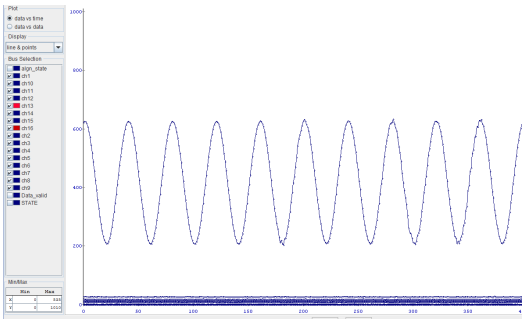
(c) Channel 3



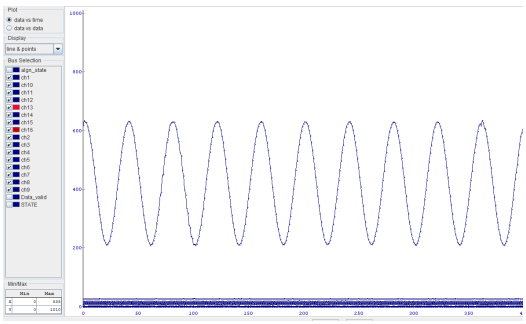
(d) Channel 4



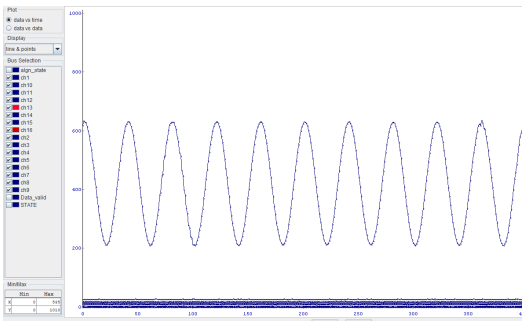
(e) Channel 5



(f) Channel 6

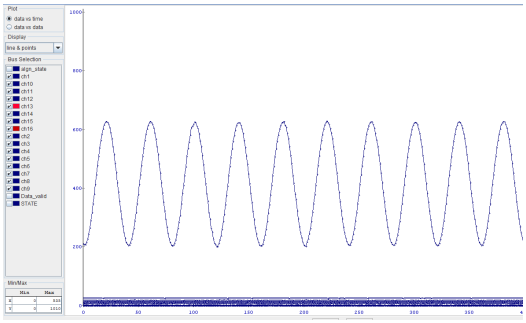


(g) Channel 7

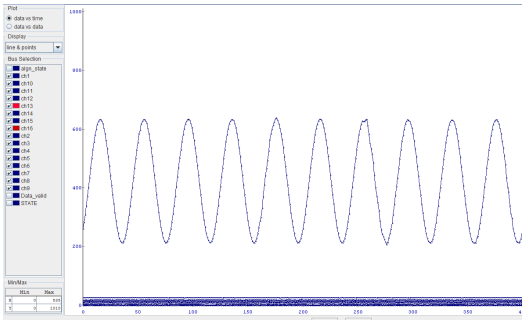


(h) Channel 8

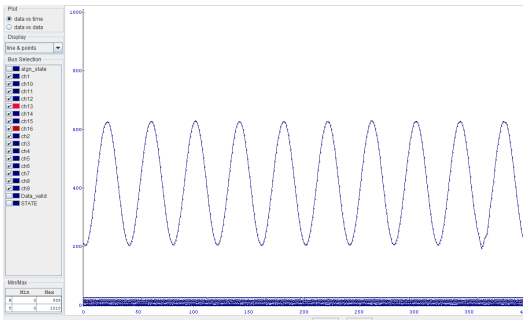
Figure 4.20: 1 MHz sinusoidal (wave 0.2 V_{pp} and 0.4 V offset) ADC 1.



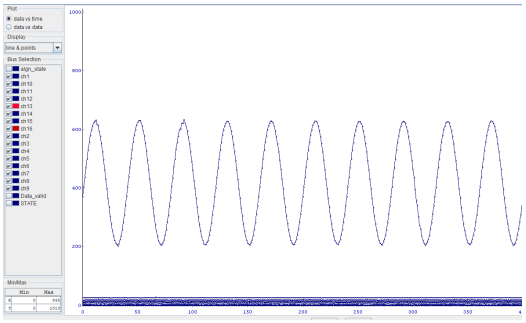
(a) Channel 9



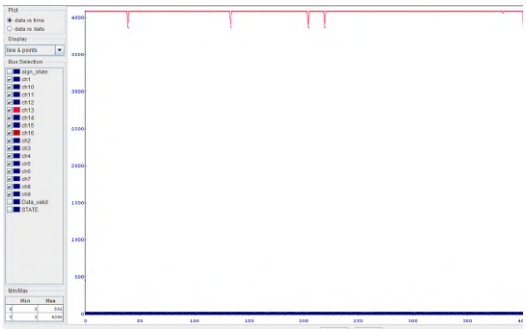
(b) Channel 10



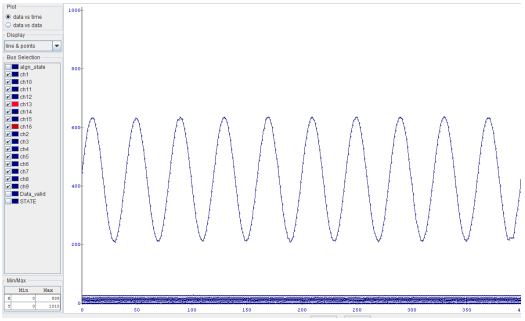
(c) Channel 11



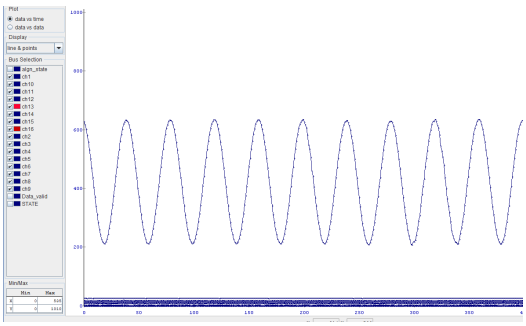
(d) Channel 12



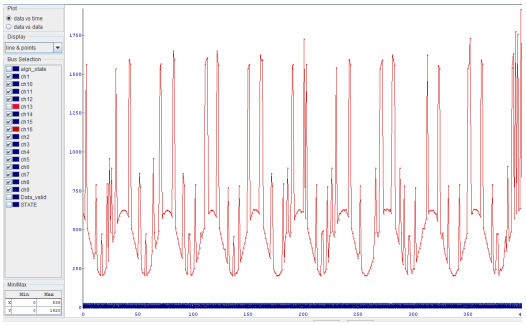
(e) Channel 13



(f) Channel 14



(g) Channel 15



(h) Channel 16

Figure 4.21: 1 MHz sinusoidal (wave 0.2 V_{pp} and 0.4 V offset) ADC 2.

Chapter 5

Conclusions

The first chapter of this dissertation describes CERN, the Large Hadron Collider, the ATLAS experiment and its internal sub-detectors. The description gives an overview of the LHC and how physics and engineering come together to create one of the world largest and most impressive scientific experiments. The description breakdown of ATLAS component sub-detectors helps place the TileCal into perspective.

Chapter 2 provides an introduction into the HL-LHC upgrade and the constraints it places on the ATLAS experiment, with an in-depth look into how the TileCal readout architecture will be enhanced to fulfil the new requirements. The outline of the TileCal upgrade provides a framework of all necessary systems and functions that the TileCal readout architecture provides.

Chapter 3 presents the test-bench systems that are currently in place for TileCal (MobiDICK) as well as the future system (PROMETEO) that are being developed for the full certification of the HL-LHC readout electronics. The electronic components of PROMETEO are described individually, demonstrating how the ADC trigger board falls into the grand scheme of the HL-LHC upgrade.

Finally, chapter 4 lays out in detail the development process that was used to produce a high-throughput ADC system for the PROMETEO test-bench of the ATLAS Tile Calorimeter.

5.1 ADC trigger board

This MSc dissertation is focused on the development and testing of a high throughput ADC trigger board for the PROMETEO test-bench of the ATLAS Tile Calorimeter in the HL-LHC. Another key aspect of the project was to learn scarce skills and techniques needed to perform each stage of the ADC board development.

The starting circuit outline was based on the ADC board schematic from the MobiDICK-4. This design was then modified and updated to be compatible with the PROMETEO system. One of the major changes to the circuit included redesigning the power stage circuits to be powered by a 12 V input from the FMC connection. Other major changes included modifying the communication interface to the FMC format and the addition of the LED driver board connection. Smaller modifications related to new board size constraints leading to alternative part sourcing and the modifications needed to the circuit to accommodate them. After 5 iterations of the circuit design the final schematic for the ADC trigger board was created in Cadence Orcad Capture.

The layout of the PCB was created from scratch using the circuit schematic netlist. The complete layout used just a third of the total surface area of the original MobiDICK-4 design. The placement of analog and digital stages of the design was careful done to reduce signal interference between the two. Signals traces for both

the analog and digital sections needed had to have their impedance and trace length matched. The ADC board had two sets of prototypes produced to debug the board and to locate any design flaws before the board would go to production. The PCB layout and design was created using Cadence Allegro PCB designer. In total 6 ADC Trigger board were produced in South Africa and where sent to CERN to be used in the PROMETEO test-benches.

The firmware used for the control and readout of the ADC board via a Xilinx Virtex 7 FPGA was created in VHDL using Xilinx ISE design suite. Before the firmware was finished the author completed two advanced training courses in VHDL design and development. The firmware modules went through extensive simulation testing in the ISE environment before a functional firmware version was possible.

Once the firmware was successfully created, it could be flashed onto the VC707 FPGA and the ADC board could be attached to the VC707. After much exercise of the scientific method, communication between the ADC and FPGA could be confirmed using the ChipScope Pro. The channel alignment and synchronisation process was able to be debugged and samples could be stored on the FPGA. Analog inputs could then be used to test the performance of each analog channel on the ADC board. Each channels was injected with an analog voltage to view how the it behaved and to calculate the pedestal offsets for each channel. The next set of tests involved injecting different sine functions into each channel to see if they behaved correctly.

Testing was able to detect that there were two faulty channels on the ADC system. One channel had a problem with signal delay causing samples to arrive during a clock rising edge leading to inconsistent results. The other had complete signal saturation which is likely due top a defect on the ADC board itself. The PROMETEO, luckily,

only requires 12 of the 16 channels to be functional for it perform its tests on the detector electronics. If there is a future production of the ADC board these issues can be corrected if needed.

Overall the project was successful: functional ADC board and accompanied FPGA firmware was designed, manufactured and tested. The Firmware and schematics related to the design can be found in the CERN technical documents repository (EDMS). The ADC trigger board can now be included in the complete PROMETEO test-bench system to assist with the verification of the HL-LHC TileCal readout electronics.

List of Figures

1.1 CERN Accelerator complex [7]. 3

1.2 A schematic drawing of the ATLAS detector [15]. 6

1.3 The right handed ATLAS coordinate system. 7

1.4 a) The ATLAS Inner detector b) Exploded view of the Inner detector, showing the different layers of the sub-detector [20]. 8

1.5 Diagram of the ATLAS calorimeter systems [23]. 10

1.6 Diagram LAr EM calorimeter module [24]. 11

1.7 a) TileCal Barrel b) TileCal Slice [26]. 12

1.8 Segmentation of TileCal slices in depth and η for half of a long barrel (left) and for an extended barrel (right). Calorimeter cells are distributed evenly about the interaction point [26]. 13

1.9 Diagram of the ATLAS Muon Spectrometer [28]. 15

1.10 ATLAS trigger and data acquisitions system data flow [31]. 17

2.1 The planned LHC upgrade schedule for next decade. It includes scheduled shutdowns, dedicated upgrades and increases in energy and luminosity [37]. 20

2.2 Overall baseline design of the upgraded Trigger/DAQ system single-level architecture for the HL-LHC. [39]. 22

2.3 Block diagram of the signal flow in the current readout electronics of the ATLAS TileCal. 25

2.4 Block diagram of the TileCal readout architecture for the HL-LHC upgrade [35]. 26
2.5 Labelled diagram of an ATLAS TileCal Mini-drawer [35]. 28
2.6 Functionality diagram of 3-in-1 card for the upgrade of the TileCal detector [35]. 29
2.7 Picture of top and bottom sides of the Mainboard used for the 3-in-1 FEB option [35]. 30
2.8 Picture the HL-LHC Daughterboard V4 [35]. 31
2.9 Block diagram of the final version of the TilePPr and TDAQi designs [31]. 33

3.1 MobiDICK component overview [57]. 36
3.2 PROMETEO test-bench component overview. 38
3.3 Image of PROMETEO in development. 39
3.4 QSFP+ FMC module used in the PROMETEO. 40
3.5 Labelled diagram of the High Voltage Board for the PROMETEO Test-bench. Manufactured in South Africa 41
3.6 Picture of the LED Driver Board for the PROMETEO test-bench. Manufactured in South Africa 42
3.7 ADC Trigger board developed for the PROMETEO test-bench. Manufactured in South Africa. 43

4.1 Labelled image of the final version of the ADC Trigger Board for PROMETEO. 46
4.2 Communication layout between the Virtex 7 FPGA and a ADC271 ADC chip. 49
4.3 Power regulation circuit diagram of the ADC board. 50

4.4 Analog circuit used to condition and filter a single trigger signal input before it is sampled by the ADC. 52
4.5 Power regulation circuit diagram of the ADC board. 53
4.6 Circuit diagram: DB50 pinout (J0); Reference clock circuit (U1, U27); LED Driver Board connector. 54
4.7 Four layer PCB design layout for the ADC board (Designed in Allegro PCB designer). 56
4.8 Block diagram of the firmware used for ADC trigger board of PROM-ETEO. 58
4.9 Two ISERDESE modules are used to de-serialise a data stream to create a complete 12-bit word. The data stream is divided into even and odd bits and shared between the SERDESE modules. The outputs are combined to create a single 12-bit word (data sample). 59
4.10 I^2C Interface Timing for the ADS5721 [63]. 61
4.11 Alignment FSM flowchart. 63
4.12 Word Alignment FSM flowchart. 64
4.13 Bit Alignment FSM flowchart. 65
4.14 PCB prototyping and testing issues. 68
4.15 Simulations created in Xilinx ISE ISim to test ADC firmware. 70
4.16 16 channel ADC configuration viewed in Xilinx Chipscope Pro. 72
4.17 ADC channel outputs after alignment with no analog input (ADC counts VS Time ns). 76
4.18 Pedestal ADC 1 (0.5V). 77
4.19 Pedestal ADC 2 (0.5V). 78
4.20 1 MHz sinusoidal (wave 0.2 V_{pp} and 0.4 V offset) ADC 1. 79
4.21 1 MHz sinusoidal (wave 0.2 V_{pp} and 0.4 V offset) ADC 2. 80

A.1 ADS5271 pinouts and decoupling capacitors (ADC 1). 89

A.2 ADS5271 pinouts and decoupling capacitors (ADC 2). 90
A.3 ADC 1 and 2 analog and digital pinouts. 90
A.4 FMC pinouts 91
A.5 Analog input stage for Channel 1. 91
A.6 DB50 trigger input pinouts, LED Driver board outputs, Clock select and buffer circuit. 92
A.7 Pinouts for each analog channel trigger input. 92
A.8 Power regulation circuits. 93
A.9 Full table of IO pins between Virtex 7 FPGA pin and ADC board pins. 94
A.10 Flow chart of the full FSM of the Alignment module. 95

Appendix A

ADC board circuit layout

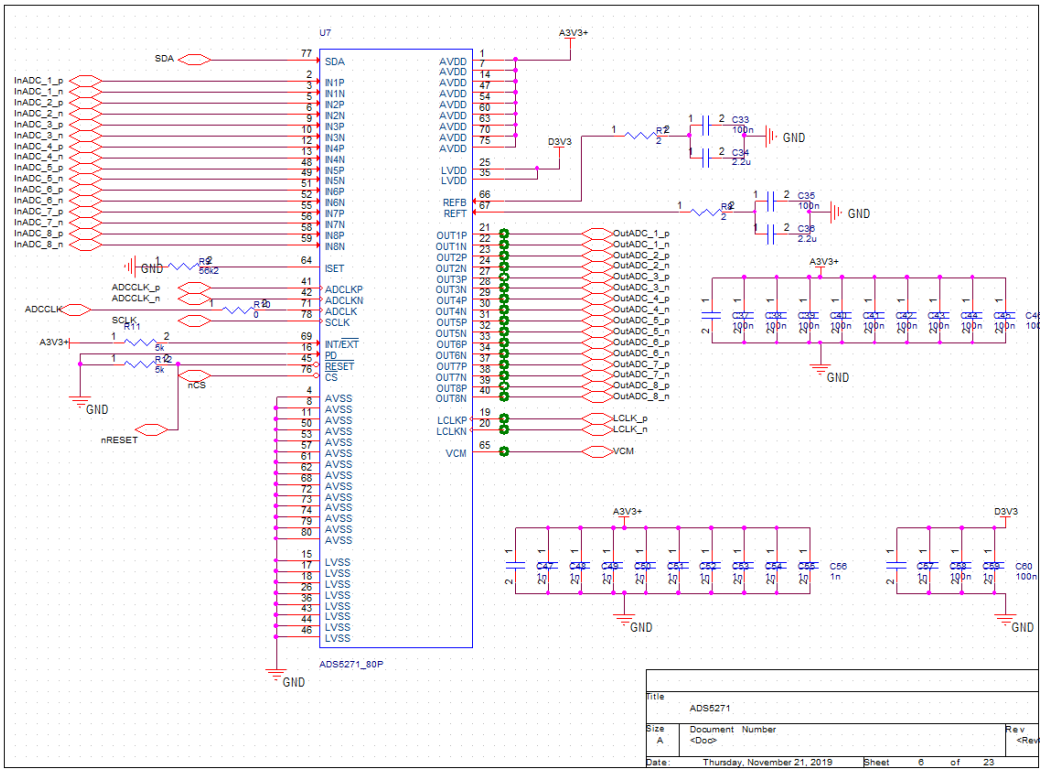


Figure A.1: ADS5271 pinouts and decoupling capacitors (ADC 1).

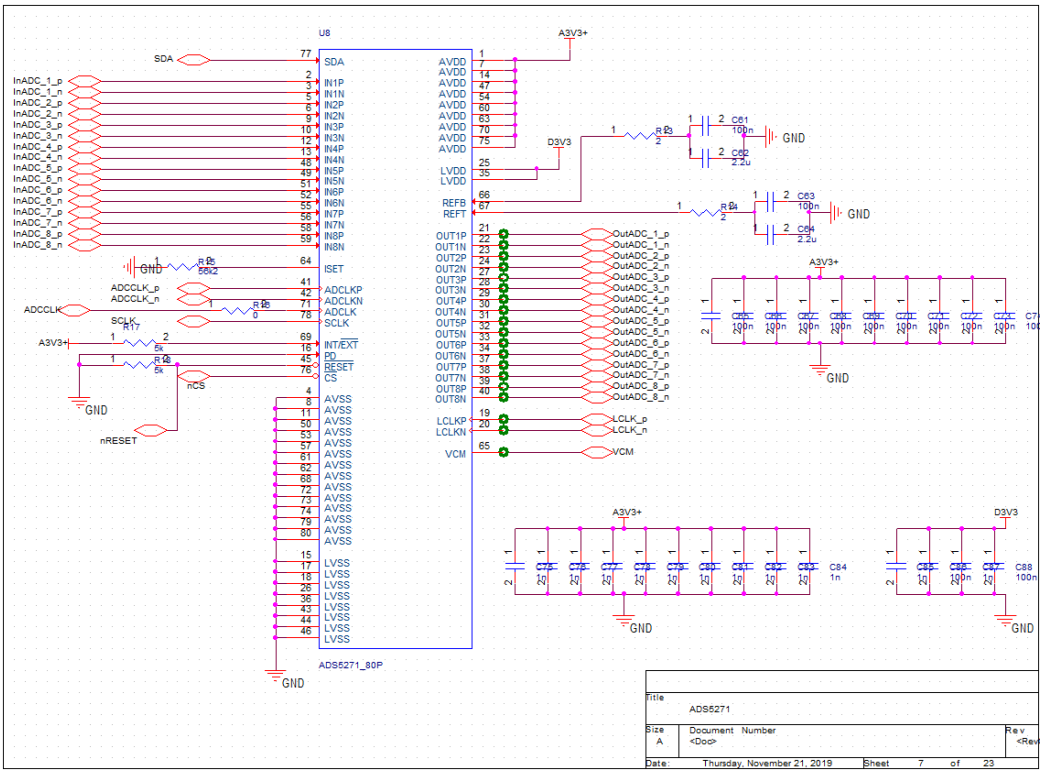


Figure A.2: ADS5271 pinouts and decoupling capacitors (ADC 2).

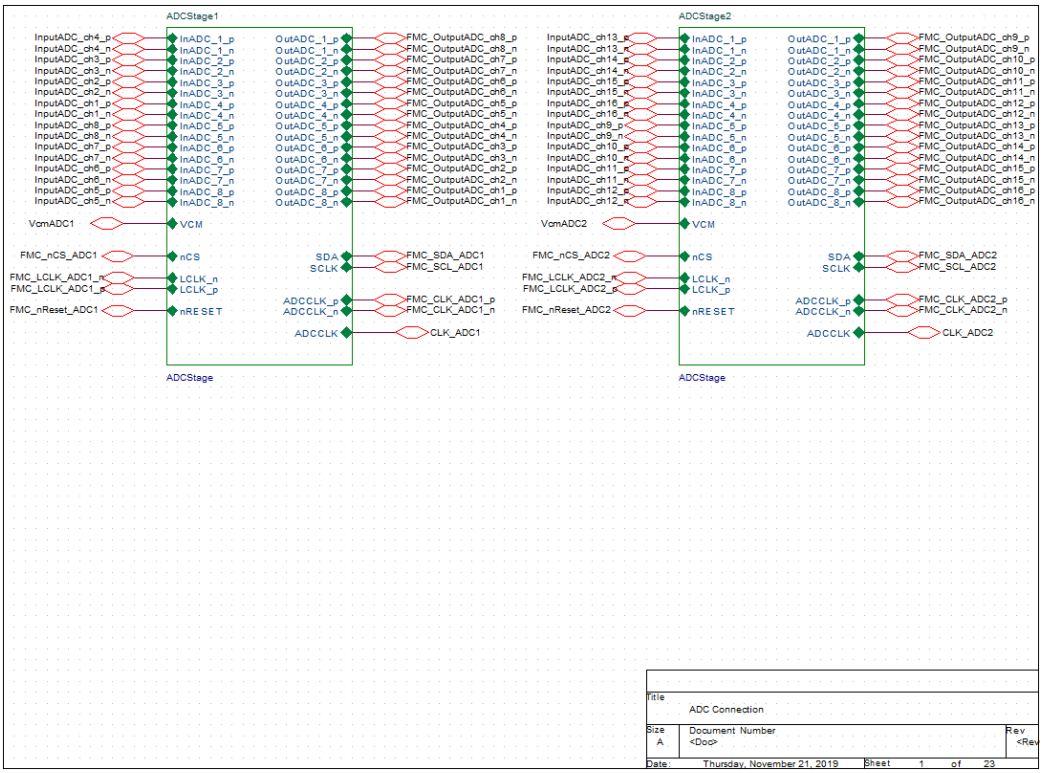


Figure A.3: ADC 1 and 2 analog and digital pinouts.

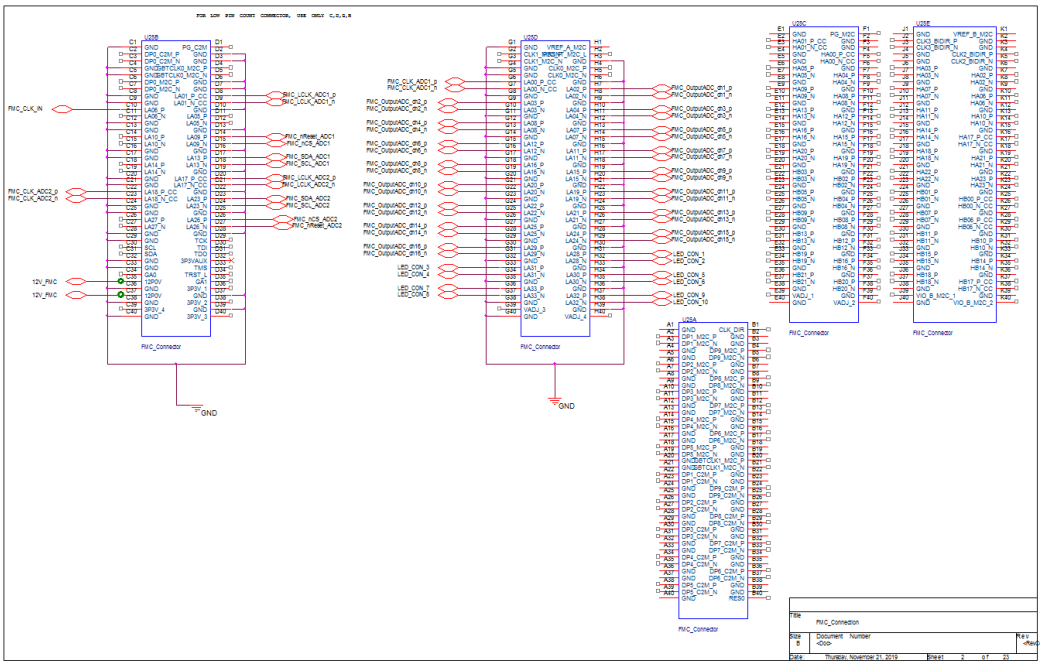


Figure A.4: FMC pinouts

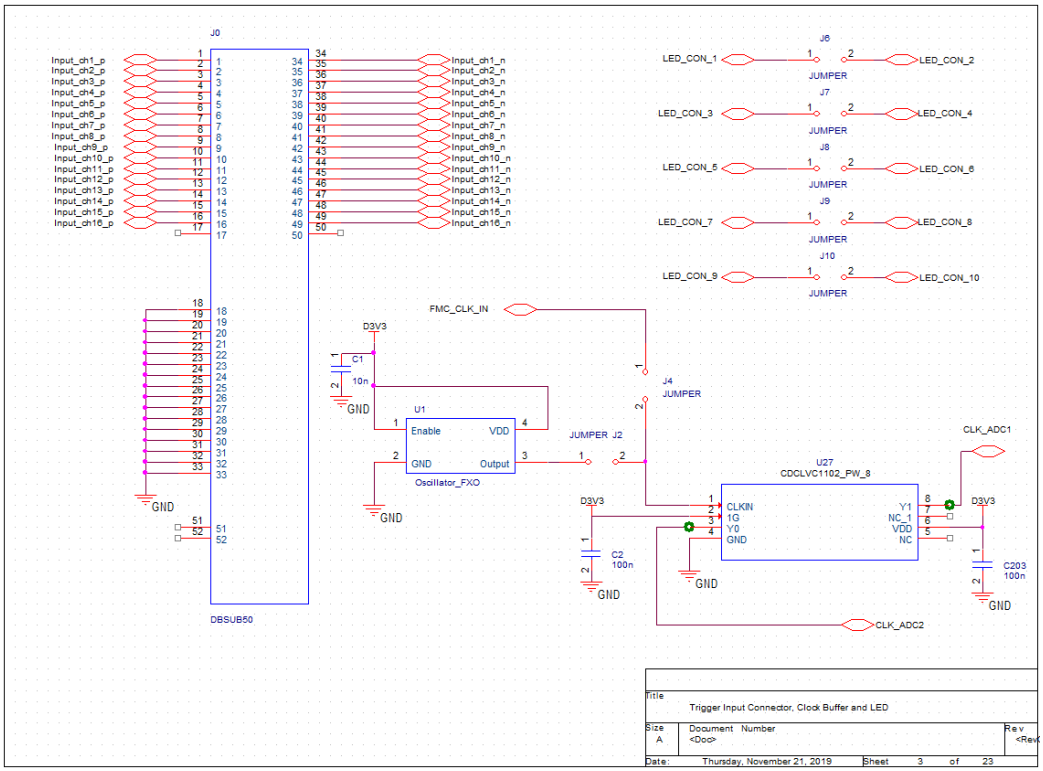


Figure A.5: Analog input stage for Channel 1.

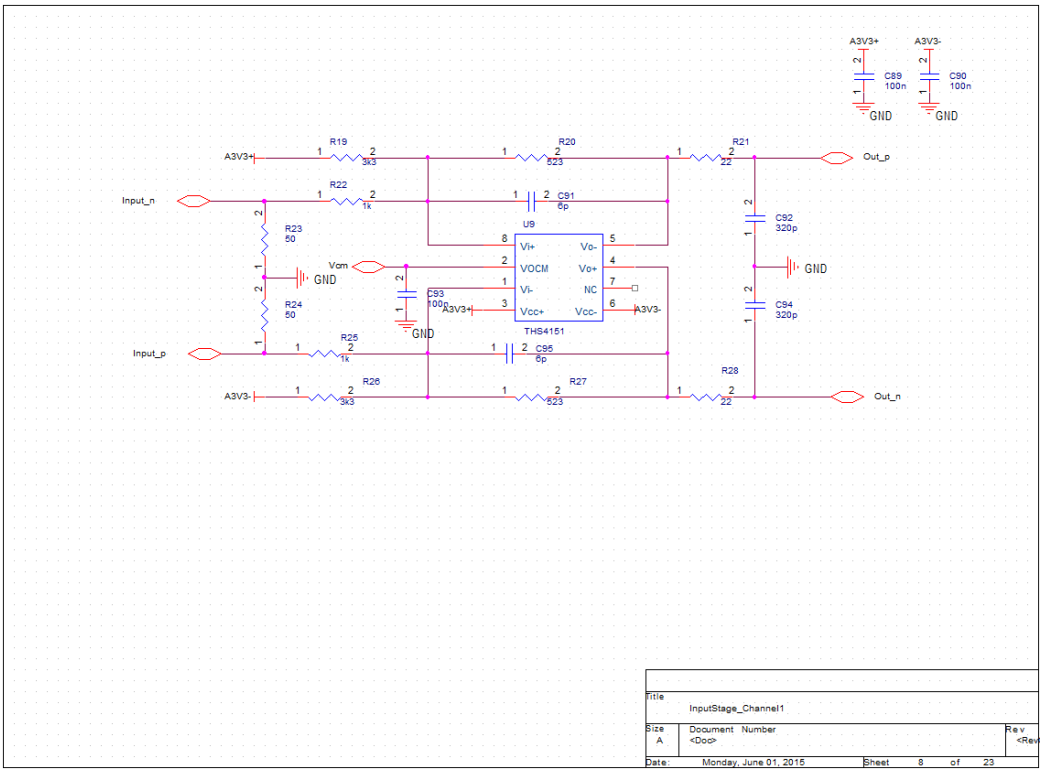


Figure A.6: DB50 trigger input pinouts, LED Driver board outputs, Clock select and buffer circuit.

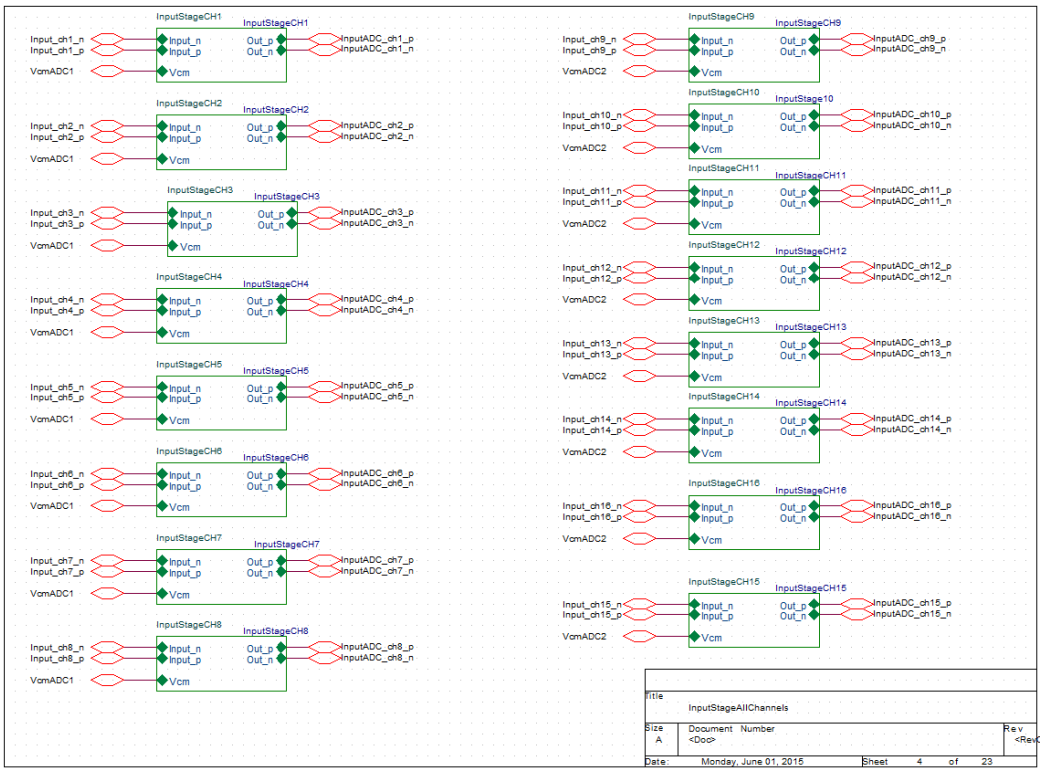


Figure A.7: Pinouts for each analog channel trigger input.

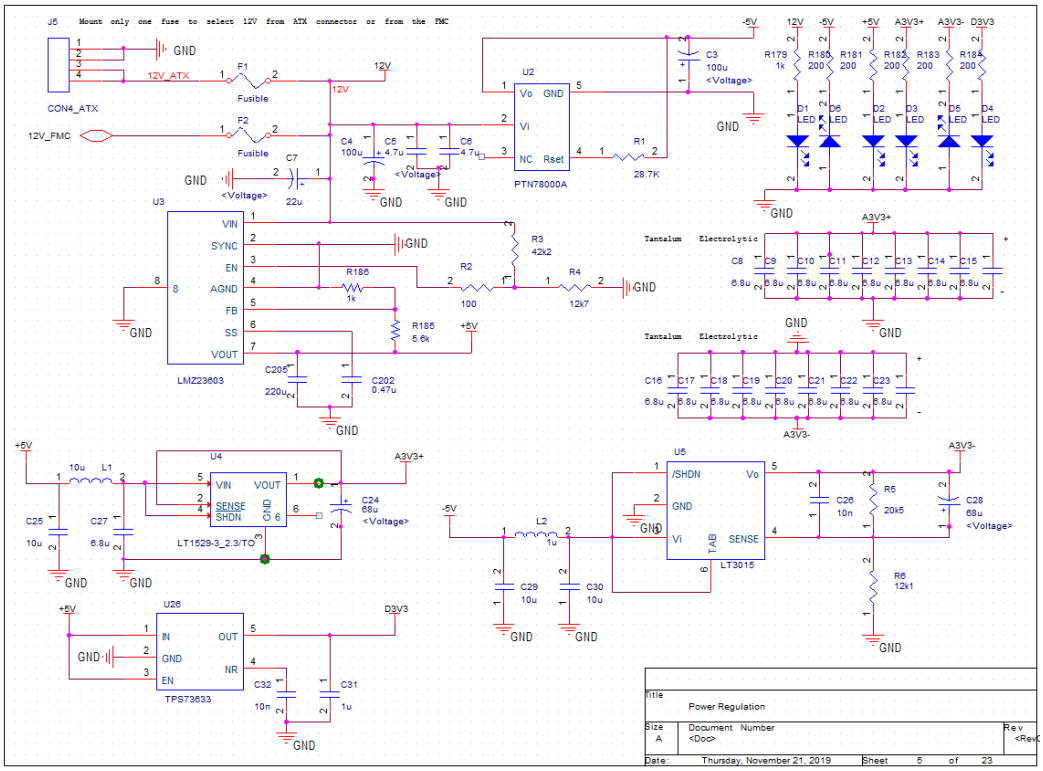


Figure A.8: Power regulation circuits.

		VC7070 Board					ADC BOARD		
Signal Discription	Direction	Signal Name	Pin LOC	Schematic Net Name	FMC PIN	IOStandard used	Signal Name	FMC PIN	Schematic Net Name
40 Mhz clock to both ADCs	ADC	sysclk40_out	K42	FMC1_HPC_LA06_P	C10	LVCMO18	FMC_CLK_IN	C10	LA06_P
Internal 200Mhz System clock		sysclk_p	E19			LVDS			
		sysclk_n	E18			LVDS			
ADC 1									
ADC1 Frame Clk	FPGA	ADC1_ADCLK_P	K39	FMC1_HPC_LA00_CC_P	G6	LVDS	FMC_CLK_ADC1_p	G6	LA00_P_CC
		ADC1_ADCLK_N	K40	FMC1_HPC_LA00_CC_N	G7	LVDS	FMC_CLK_ADC1_n	G7	LA00_N_CC
ADC bit clock	FPGA	ADC1_LCLK_p	J40	FMC1_HPC_LA01_CC_P	D8	LVDS	FMC_LCLK_ADC1_p	D8	LA01_P_CC
		ADC1_LCLK_n	J41	FMC1_HPC_LA01_CC_N	D9	LVDS	FMC_LCLK_ADC1_n	D9	LA01_N_CC
ADC1 reset	ADC	ADC1_RESET_al	R42	FMC1_HPC_LA09_P	D14	LVCMO18	FMC_nReset_ADC1	D14	LA09_P
ADC1 CS	ADC	ADC1_CS_al	P42	FMC1_HPC_LA09_N	D15	LVCMO18	FMC_nCS_ADC1	D15	LA09_N
ADC1 SDATA	ADC	ADC1_SDATA	H39	FMC1_HPC_LA13_P	D17	LVCMO18	FMC_SDA_ADC1	D17	LA13_P
ADC1 SCLK	ADC	ADC1_SCLK	G39	FMC1_HPC_LA13_N	D18	LVCMO18	FMC_SCL_ADC1	D18	LA13_N
Data channel 0	FPGA	ADC1_CH_p[0]	P41	FMC1_HPC_LA02_P	H7	LVDS	FMC_OutputADC_ch1_p	H7	LA02_P
Data channel 0	FPGA	ADC1_CH_n[0]	N41	FMC1_HPC_LA02_N	H8	LVDS	FMC_OutputADC_ch1_n	H8	LA02_N
Data channel 1	FPGA	ADC1_CH_p[1]	M42	FMC1_HPC_LA03_P	G9	LVDS	FMC_OutputADC_ch2_p	G9	LA03_P
Data channel 1	FPGA	ADC1_CH_n[1]	L42	FMC1_HPC_LA03_N	G10	LVDS	FMC_OutputADC_ch2_n	G10	LA03_N
Data channel 2	FPGA	ADC1_CH_p[2]	H40	FMC1_HPC_LA04_P	H10	LVDS	FMC_OutputADC_ch3_p	H10	LA04_P
Data channel 2	FPGA	ADC1_CH_n[2]	H41	FMC1_HPC_LA04_N	H11	LVDS	FMC_OutputADC_ch3_n	H11	LA04_N
Data channel 3	FPGA	ADC1_CH_p[3]	M37	FMC1_HPC_LA08_P	G12	LVDS	FMC_OutputADC_ch4_p	G12	LA08_P
Data channel 3	FPGA	ADC1_CH_n[3]	M38	FMC1_HPC_LA08_N	G13	LVDS	FMC_OutputADC_ch4_n	G13	LA08_N
Data channel 4	FPGA	ADC1_CH_p[4]	G41	FMC1_HPC_LA07_P	H13	LVDS	FMC_OutputADC_ch5_p	H13	LA07_P
Data channel 4	FPGA	ADC1_CH_n[4]	G42	FMC1_HPC_LA07_N	H14	LVDS	FMC_OutputADC_ch5_n	H14	LA07_N
Data channel 5	FPGA	ADC1_CH_p[5]	R40	FMC1_HPC_LA12_P	G15	LVDS	FMC_OutputADC_ch6_p	G15	LA12_P
Data channel 5	FPGA	ADC1_CH_n[5]	P40	FMC1_HPC_LA12_N	G16	LVDS	FMC_OutputADC_ch6_n	G16	LA12_N
Data channel 6	FPGA	ADC1_CH_p[6]	F40	FMC1_HPC_LA11_P	H16	LVDS	FMC_OutputADC_ch7_p	H16	LA11_P
Data channel 6	FPGA	ADC1_CH_n[6]	F41	FMC1_HPC_LA11_N	H17	LVDS	FMC_OutputADC_ch7_n	H17	LA11_N
Data channel 7	FPGA	ADC1_CH_p[7]	K37	FMC1_HPC_LA16_P	G18	LVDS	FMC_OutputADC_ch8_p	G18	LA16_P
Data channel 7	FPGA	ADC1_CH_n[7]	K38	FMC1_HPC_LA16_N	G19	LVDS	FMC_OutputADC_ch8_n	G19	LA16_N
ADC 2									
ADC2 Frame Clk	FPGA	ADC2_ADCLK_P	M32	FMC1_HPC_LA18_CC_P	C22	LVDS	FMC_CLK_ADC2_p	C22	LA18_P_CC
		ADC2_ADCLK_N	L32	FMC1_HPC_LA18_CC_N	C23	LVDS	FMC_CLK_ADC2_n	C23	LA18_N_CC
ADC2 bit clock	FPGA	ADC2_LCLK_p	L31	FMC1_HPC_LA17_CC_P	D20	LVDS	FMC_LCLK_ADC2_p	D20	LA17_P_CC
		ADC2_LCLK_n	K32	FMC1_HPC_LA17_CC_N	D21	LVDS	FMC_LCLK_ADC2_n	D21	LA17_N_CC
ADC2 reset	ADC	ADC2_RESET_al	H30	FMC1_HPC_LA26_N	D27	LVCMO18	FMC_nReset_ADC2	D27	LA26_N
ADC2 CS	ADC	ADC2_CS_al	J30	FMC1_HPC_LA26_P	D26	LVCMO18	FMC_nCS_ADC2	D26	LA26_P
ADC2 SDATA	ADC	ADC2_SDATA	P30	FMC1_HPC_LA23_P	D23	LVCMO18	FMC_SDA_ADC2	D23	LA23_P
ADC2 SCLK	ADC	ADC2_SCLK	N31	FMC1_HPC_LA23_N	D24	LVCMO18	FMC_SCL_ADC2	D24	LA23_N
Data channel 0	FPGA	ADC2_CH_p[0]	M36	FMC1_HPC_LA15_P	H19	LVDS	FMC_OutputADC_ch9_p	H19	LA15_P
Data channel 0	FPGA	ADC2_CH_n[0]	L37	FMC1_HPC_LA15_N	H20	LVDS	FMC_OutputADC_ch9_n	H20	LA15_N
Data channel 1	FPGA	ADC2_CH_p[1]	Y29	FMC1_HPC_LA20_P	G21	LVDS	FMC_OutputADC_ch10_p	G21	LA20_P
Data channel 1	FPGA	ADC2_CH_n[1]	Y30	FMC1_HPC_LA20_N	G22	LVDS	FMC_OutputADC_ch10_n	G22	LA20_N
Data channel 2	FPGA	ADC2_CH_p[2]	W30	FMC1_HPC_LA19_P	H22	LVDS	FMC_OutputADC_ch11_p	H22	LA19_P
Data channel 2	FPGA	ADC2_CH_n[2]	W31	FMC1_HPC_LA19_N	H23	LVDS	FMC_OutputADC_ch11_n	H23	LA19_N
Data channel 3	FPGA	ADC2_CH_p[3]	R28	FMC1_HPC_LA22_P	G24	LVDS	FMC_OutputADC_ch12_p	G24	LA22_P
Data channel 3	FPGA	ADC2_CH_n[3]	P28	FMC1_HPC_LA22_N	G25	LVDS	FMC_OutputADC_ch12_n	G25	LA22_N
Data channel 4	FPGA	ADC2_CH_p[4]	N28	FMC1_HPC_LA21_P	H25	LVDS	FMC_OutputADC_ch13_p	H25	LA21_P
Data channel 4	FPGA	ADC2_CH_n[4]	N29	FMC1_HPC_LA21_N	H26	LVDS	FMC_OutputADC_ch13_n	H26	LA21_N
Data channel 5	FPGA	ADC2_CH_p[5]	K29	MC1_HPC_LA25_P	G27	LVDS	FMC_OutputADC_ch14_p	G28	LA25_P
Data channel 5	FPGA	ADC2_CH_n[5]	K30	FMC1_HPC_LA25_N	G28	LVDS	FMC_OutputADC_ch14_n	G29	LA25_N
Data channel 6	FPGA	ADC2_CH_p[6]	R30	FMC1_HPC_LA24_P	H28	LVDS	FMC_OutputADC_ch15_p	H28	LA24_P
Data channel 6	FPGA	ADC2_CH_n[6]	P31	FMC1_HPC_LA24_N	H29	LVDS	FMC_OutputADC_ch15_n	H29	LA24_N
Data channel 7	FPGA	ADC2_CH_p[7]	T29	MC1_HPC_LA29_P	G30	LVDS	FMC_OutputADC_ch16_p	G30	LA29_P
Data channel 7	FPGA	ADC2_CH_n[7]	T30	FMC1_HPC_LA29_N	G31	LVDS	FMC_OutputADC_ch16_n	G31	LA29_N
Additional Signals									
LEDS		led_out[0]	AM39			LVCMOS18			
		led_out[1]	AN39			LVCMOS18			
		led_out[2]	AR37			LVCMOS18			
		led_out[3]	AT37			LVCMOS18			
		led_out[4]	AR35			LVCMOS18			
		led_out[5]	AP41			LVCMOS18			
		led_out[6]	AP42			LVCMOS18			
		led_out[7]	AU39			LVCMOS18			
BUTTONS		btnin[0]	AP40			LVCMOS18			
		btnin[1]	AR40			LVCMOS18			
		btnin[2]	AV39			LVCMOS18			
		btnin[3]	AU38			LVCMOS18			
		btnin[4]	AW40			LVCMOS18			
LED BOARD FMC CONNECTOR									
Connection 1			L39	FMC1_HPC_LA28_P	H31		LED_con_1	H31	LA28_P
Connection 2			L30	FMC1_HPC_LA28_N	H32		LED_con_2	H32	LA28_N
Connection 3			M28	FMC1_HPC_LA31_P	G33		LED_con_3	G33	LA31_P
Connection 4			M29	FMC1_HPC_LA31_N	G34		LED_con_4	G34	LA31_N
Connection 5			U31	FMC1_HPC_LA33_P	G36		LED_con_5	G36	LA33_p
Connection 6			T31	FMC1_HPC_LA33_N	G37		LED_con_6	G37	LA33_N
Connection 7			V30	FMC1_HPC_LA30_P	H34		LED_con_7	H34	LA30_P
Connection 8			V31	FMC1_HPC_LA30_N	H35		LED_con_8	H35	LA30_N
Connection 9			V29	FMC1_HPC_LA32_P	H37		LED_con_9	H37	LA32_P
Connection 10			U29	FMC1_HPC_LA32_N	H38		LED_con_10	H38	LA32_N

Figure A.9: Full table of IO pins between Virtex 7 FPGA pin and ADC board pins.

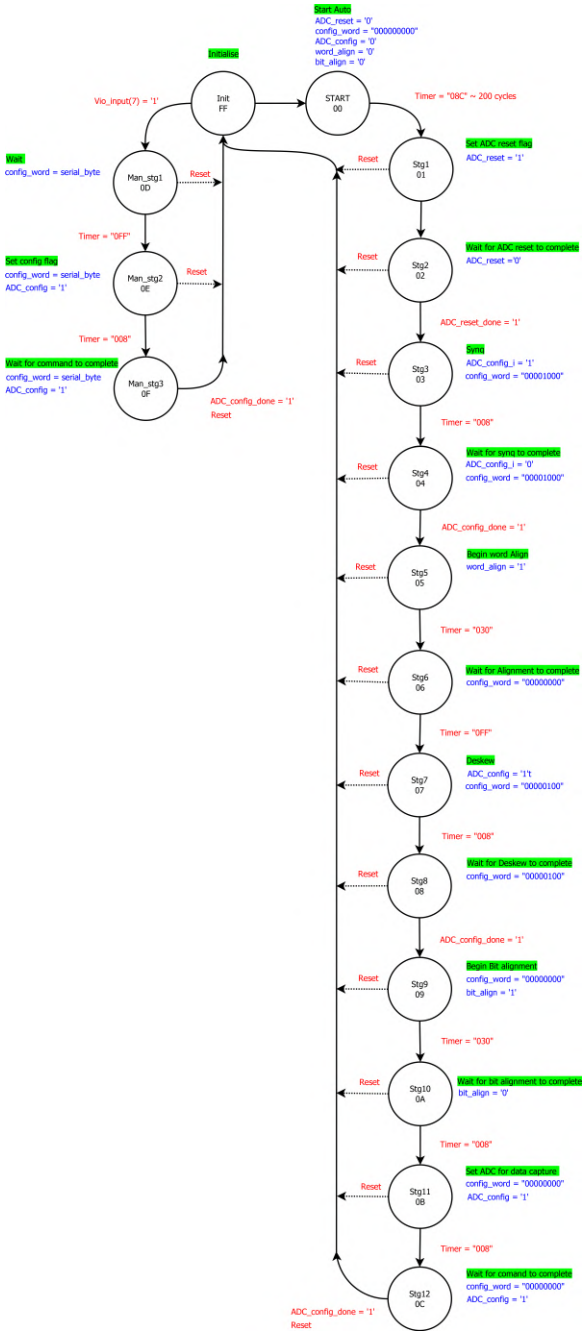


Figure A.10: Flow chart of the full FSM of the Alignment module.

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