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Feasibility Study of the Dual Active Bridge as a Low-Frequency Sine Wave Inverter

Kerren Mark Ortlepp

Master of Science in Engineering by research only

A dissertation submitted to the Faculty of Engineering and the Built Environment, University of Witwatersrand, Johannesburg, in fulfilment of the requirements for the degree of Master of Science in Engineering.

Johannesburg 2018

DECLARATION

I declare that this dissertation is my own unaided work. It is being submitted to the Degree of Master of Science to the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination to any other University.

. . . . . .

(Signature of Candidate)

. . . . . day of . . . . . year . . . . . .

Abstract

The conventional Sinusoidal Pulse Width Modulation (SPWM) inverter is limited by the fact that it does not allow for Zero Voltage Switching. This means that the switching frequency is kept low to reduce the switching losses. As a consequence of holding these switching frequencies low, the distribution of power over the frequency spectrum is kept closer to the fundamental frequency (compared to higher switching frequencies) leading to larger reactive components to filter out these harmonics. The use of high-frequency switching, Zero Voltage Switching, and different modulation schemes can lead to higher power densities. This research investigates under what conditions the use of these techniques in a Dual Active Bridge (DAB) inverter might lead to a higher power density than the SPWM.

Volumetric approximations for the different circuit components in the investigated inverter topologies are demonstrated. These approximations are used to design circuits using physical volume as the cost function where possible. Additionally, a loss model is derived to determine the expected efficiency of each topology being investigated. This model is related to the power density since it is directly proportional to the size of heat sink required to cool the inverter.

The techniques for improving power density mentioned above are presented, and the impact that they have on power density is shown using the volumetric approximation function. From this approximation, the volumes between the DAB and the SPWM are compared and investigations into where the DAB may have a higher power density have been performed. It was found that the DAB was not smaller than the SPWM for frequencies less than 72 kHz. When simulating the converters operating at different frequencies, the general trend is that the SPWM increases in volume as the frequency increases,

whereas, the DAB decreases in volume as the frequency increases. An exact frequency at which the DAB would be smaller than the SPWM was not found in this research. However, many conclusions have been drawn around the use of a DAB as an inverter and the strengths and shortcomings it provides. The modulation scheme would need to be modified to reduce the losses and provide a more competitive volume. Additionally, multi-level and multi-stage techniques could be used to reduce the volume further.

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List of Symbols

C_{o} The output capacitor. 17, 86, 87

D_{hs} The density of a heat sink used in volumetric approximation formulae. 18, 19, 60, 63, 66, 74, 100

$\boldsymbol{V}'_{\mathrm{o}}$ The time varying derivative of the output voltage of a converter. 84, 86

f_{c} The cut-off frequency for a filter. 38–40, 43, 44, 59, 61, 63, 71, 72, 74

$\boldsymbol{F}_{\mathrm{fil}}$ The volume of the filter in an SPWM inverter. 39, 43, 61

$\boldsymbol{F}_{\mathrm{hs}}$ The volume of the heat sink in an SPWM inverter. 60, 61

f_{o} The frequency of the output waveform from an inverter. 1, 2, 4–6, 25, 26, 31, 36, 39, 40, 42–45, 49, 50, 55, 58, 60, 63, 70, 72, 93, 94

f_{s} The switching frequency of a converter. 1, 2, 4–6, 12–16, 31, 36, 39–45, 58–61, 63, 70, 72, 74, 78, 80, 88, 93, 94, 96, 98–105, 110

f_{sw} The switching frequency of a MOSFET, effectively this is the frequency at which a MOSFET can switch on and off. 50, 97, 102, 103

$\boldsymbol{F}_{\mathrm{vol}}$ The total approximated volume of an SPWM inverter. 43, 60, 61, 63

$\boldsymbol{I}_{\mathrm{L}}$ The modified time varying current through an inductor. 49, 50, 55–58, 60, 63

$\boldsymbol{i}_{\mathrm{L}}$ The time varying current through an inductor. 42, 86, 93, 94, 99

$\boldsymbol{I}_{\mathrm{L(tri)}}$ The current through the leakage inductance of the DAB due to Triangular Modulation. 89, 93, 95

$\boldsymbol{i}_{\mathrm{o}}$ The time varying output current from a converter. 42

I_{sw} The current through a switch. 49, 51–53, 56, 58, 60, 63, 93

$\boldsymbol{I}_{sw}$ The current through a switch at a specific switching cycle. 50–53, 58, 60, 63, 93

P_{con} The conduction losses in a converter. 47, 55, 92, 95

P_{esw} The power losses due to the energy dissipated by switches over a period of time. 92, 94

$\boldsymbol{\phi}$ The time varying phase angle used in modulation calculations for the DAB. 79, 80

P_{in} The input power flowing into a converter. 25

P_{loss} The total losses of a converter. This is the combination of switching losses, conduction losses, etc. 47, 58, 92

P_{o} The output power from a converter. 78

$\boldsymbol{P}_{o}$ The time varying output power from a converter. 26, 79

P_{rcon} The losses due to the on resistances of a MOSFET. 56

P_{rr} The losses due to diode reverse recovery. 47

P_{sw} The switching losses in a converter, this is the power dissipated from all switching events in the circuit over a switching cycle. 47, 92, 93

P_{trans} The losses due to a transformer in the converter. 92

P_{v} The relative core losses in a transformer core. 102, 103

Q_{rr} The charge lost due to diode reverse recovery. 58, 60, 63

R The output load resistance. 26, 80, 86–88, 96

r_{on} The on resistance of a MOSFET. 55–58, 60, 63, 95, 99

$\boldsymbol{T}_1$ The period of time that the input or primary bridge is on, per switching cycle, in the DAB. 86–89, 93, 94

$\boldsymbol{T}_2$ The period of time that the output or secondary bridge is on, per switching cycle, in the DAB. 86–89, 94

T_o The period of the output waveform from an inverter. 26, 55–58, 60, 63, 93–95, 99

$\boldsymbol{T}$ The triangular waveform used when generating the SPWM output waveform. 32

t_{rr} The diode reverse recovery time. 58, 60, 63

T_s The switching period of a converter. This is otherwise referred to as the switching cycle.. 57, 86–88, 93, 94, 97

$\boldsymbol{u}_s$ A standard unit step. 4, 5, 88

$\boldsymbol{V}_A$ The time varying output waveform due to the positive control in the SPWM. 1, 4–6, 32, 36, 40, 70

$\boldsymbol{V}_B$ The time varying output waveform due to the negative control in the SPWM. 1, 4–6, 32, 36, 40, 70

V_{core} The volume of a transformer when taking the core and winding volume into account. 104, 105

$V_{D(on)}$ The standard diode on voltage. viii, 54–56

V_{in} The input voltage across a converter. 1, 2, 4–6, 25, 31, 32, 36, 40–43, 49, 51–53, 55, 57, 58, 60, 63, 78–80, 82, 86–88, 93, 94, 96, 97

$\boldsymbol{V}_L$ The time varying voltage across an inductor in a circuit. 49, 86

$\boldsymbol{V}_{L(tri)}$ The time varying voltage across the leakage inductance in a DAB due to Triangular Modulation. 89

$\boldsymbol{V}_o$ The time varying output voltage of a converter. 1, 3, 79, 80, 84, 86, 88, 93, 94

V_o The output voltage of a converter. 78, 82

$V_{o(p)}$ The peak sinusoidal output voltage used throughout this research. 1, 25, 26, 36, 40–43, 49, 55, 60, 63, 82, 96, 97

$\boldsymbol{V}_{SPWM}$ The SPWM output waveform. 1, 5, 49, 55

$\boldsymbol{V}_{out}$ The output voltage of the SPWM after filtering. 6, 32

V_{sw} The voltage drop across a switch. 49, 51, 53, 58, 60, 63, 93

$\boldsymbol{V}_{A}$ The voltage across the transformer of the input bridge of the DAB while using Triangular Modulation. 88, 89

$\boldsymbol{V}_{B}$ The voltage across the transformer of the output bridge of the DAB while using Triangular Modulation. 88, 89

W_{e} The energy density of an electric field. 20–22, 39, 43, 60, 63–65, 74

W_{m} The energy density of a magnetic field. 20, 21, 23, 39, 43, 60, 63, 64, 66, 67, 74, 111

$\boldsymbol{W}_{off}$ The energy dissipated during a switch-off event. 49, 50, 53, 58

$\boldsymbol{W}_{on}$ The energy dissipated during a switch-on event. 49, 50, 53, 58

$\boldsymbol{W}_{sw}$ The energy lost due to a sum of switching events. 49

Acronyms

DAB Dual Active Bridge. i, ii, 2, 3, 5, 6, 10–12, 15–17, 25–27, 76–78, 80, 82, 88–90, 93, 96, 98, 100, 105–114, 116, 117

GLBC Google Little Box Challenge. 1, 2, 8, 14, 25, 27, 82, 116

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 8, 17, 49, 53, 55–57, 59, 60, 98, 99, 117

PCB Printed Circuit Board. 1, 2

PhD Doctor of Philosophy. 111

PPP Partial Power Processing. 2, 9, 10, 112, 114

PSM Phase Shift Modulation. 77, 78, 82, 107, 111, 117

PWM Pulse Width Modulation. 12, 13, 29, 78, 80

SPWM Sinusoidal Pulse Width Modulation. i, ii, 1–7, 9, 11–13, 15, 25, 26, 29, 31, 32, 36, 38–40, 44, 45, 47, 49, 51, 57, 59, 60, 63, 65, 70, 71, 74, 89, 96, 107, 109–111, 113, 116, 117

SVM Space Vector Modulation. 112, 114

THD Total Harmonic Distortion. 7, 9, 25, 33, 36, 39, 40, 43–45, 71–73, 110

TriM Triangular Modulation. 17, 77, 81, 82, 88, 92, 107, 111, 113, 117

ZVS Zero Voltage Switching. i, 2, 3, 5, 6, 27, 92, 93, 108, 111, 112, 114, 116, 117

Introduction 1

There has been a focus over the last few years in the advancement of the power density of converters. A practical example of this advancement is the Google Little Box Challenge (GLBC), which involved the design and implementation of a 2 kW inverter, where the winning team was awarded $1,000,000 for having the highest power density while meeting requirements around frequency, voltage, and current (discussed in detail in Section 2.6). This demonstrates the relevance of the drive towards power density and that it is the direction in which industry is driving Power Electronics.

Kolar *et al.* have focused on increasing the power density of power converters for many years [1]–[3]. There are many reasons towards having a higher power density, cost and volume play a significant role. U.S. DRIVE, an industrial partnership with the United States Department of Energy, have set targets for DC-to-DC converters [4], [5]. In 2013, they set a target that the cost for a DC-to-DC converter should reduce from less than $60 per kW to less than $50 per kW in the year 2020 compared to 2015. More recently, in 2017, they added to target that the price should decrease to $30 per kW in 2025. Another target that they set is that the power density should increase from more than $2\,\mathrm{kW l^{-1}}$ to more than $3\,\mathrm{kW l^{-1}}$ between 2015 and 2020 and should reach $4.6\,\mathrm{kW l^{-1}}$ in 2025.

Furthermore, U.S. DRIVE report that the costs (projected) of the Printed Circuit Board (PCB), power silicon, thermal management, and capacitors com-

bined, make up 77% of the total cost of a power inverter[1] [4]. This implies that the cost can be reduced by decreasing the volume of the capacitors and heat sinks. Additionally, if the PCB size reduces, one may see a reduction in cost, however, the majority of the costs may lie in the components on the PCB as opposed to the size of the actual PCB itself.

The direction towards a higher power density leads to questions about how to achieve these densities and what affects the volume of a converter. In order to scope this research correctly, the GLBC is used as the baseline case study, this provides relevance for the case study and provides an operational point for all power converter designs [6].

The focus of this research is to establish relationships between power converter parameters and their effect on the volume of the converter, thus leading to the relationship between these parameters and the power density of these converters. These relationships can then be utilised to optimise the volumes of converters as they would show which factors have the most significant effect on power density.

The topological choices for power converters were considered, and these considerations are discussed in detail in Chapter 2. As a summary, the Dual Active Bridge (DAB) is used because it has many features such as the ability to apply different modulation schemes, Zero Voltage Switching (ZVS), reverse power flow, and Partial Power Processing (PPP) which is defined and discussed further in Chapter 2. The DAB is a DC-to-DC converter, however, in this research, it is used as a DC-to-AC converter. This choice was made because the functionality that the DAB provides is useful in DC-to-AC converters. The DAB has been used in DC-to-DC converters with high power densities, discussed in Chapter 2. This research aims to see if it could provide similar results in a DC-to-AC converter.

1.1 Research Question

The question being investigated in this research is, “Under what conditions does an inverter that contains a Dual Active Bridge using high-frequency switching techniques, Zero Voltage Switching, and standard modulation techniques have a higher power density compared to the conventional Sinusoidal

[1]The PCB includes the components that are mounted on the board.

Pulse Width Modulation converter?"

There are underlying questions that must be answered first before concluding on the main question mentioned. The research approach to answer this question is discussed below.

1.2 Research Approach

The use of high-frequency switching, ZVS, and certain modulation techniques should lead to the reduction in the size of the energy storage components and power losses. However, the underlying questions that need to be answered are,

- what the relationship of these effects are on the power density;
- whether they are linear;
- and which has the largest effect.

The knowledge and significance of this research is mainly found in the generic models derived that are used to approximate the volumes of the SPWM and DAB.

To find the effects on the power density of an inverter, a valid volumetric approximation method had to be established and can be seen in Chapter 2. This approximation is then be applied to the SPWM as well as the DAB to predict the power densities of each circuit under different conditions.
From this volumetric approximation, circuits are optimised according to the following specific requirements,

1. the switching frequency;
2. the use of Zero Voltage Switching;
3. the use of different modulation schemes;
4. the combination of the above requirements.

A comparison has been performed between the power densities of the optimised SPWM and the inverter containing the DAB under each of the requirements listed above and is discussed in Chapter 5. Conclusions are made from the comparisons between the volumes and trends of the SPWM and DAB.

An attempt has been made to generalise the techniques in Chapters 3 and 4 that are used to approximate the volumes of these converters. This is to allow for future work to occur where more topologies can be compared without having to remodel the topologies used in this research.

The research structure is demonstrated in Figure 1.1 below. In each chapter, this figure is used to demonstrate the knowledge areas covered and how each chapter fits into the entirety of this research. For each topology, a basic circuit is designed which leads to a first order volumetric approximation. The losses are calculated, and the final volumetric approximation is found. Since the losses contribute indirectly to the volume, an optimisation loop is added to find the lowest volume by adjusting the circuit design to reduce the loss.

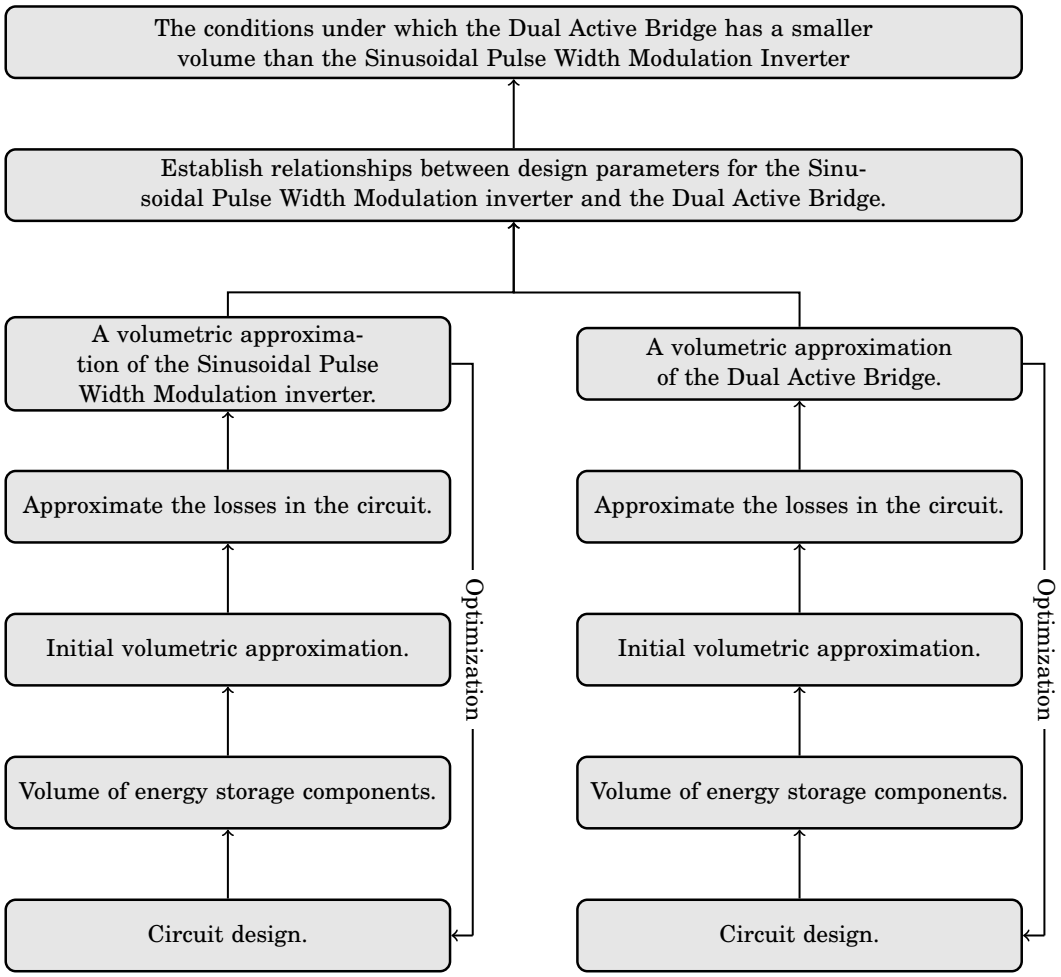


Figure 1.1: The argument flow that is used to find the conclusion to this research. Volumetric approximations are derived, and relationships are found from these approximations.

Literature Review 2

Many power converter topologies were investigated, and these are discussed in this chapter. The final choices are summarised in Section 2.1 below. Further depth and elaboration is provided in the sections following the summary.

2.1 Research Choices based on the Literature

After an investigation into the existing power converter topologies, the DAB was chosen as the topology that would be used throughout this research. The question may arise why a typical DC-to-DC converter is being used in a DC-to-AC application. It is assumed that the switching frequency is much higher than the fundamental output frequency, this means that over each switching period, the converter is effectively a DC-to-DC converter. Krishnamurthy and Ayyanar propose a topology that can be used for universal power conversion [7]. The input and output terminals of this topology may be connected in parallel and series, allowing for this topology to be utilised in many applications. This highly configurable and functional topology essentially contains a rectifier to a DAB, demonstrating the compatibility and functionality that the DAB topology provides. The major reasons for the choice to use the DAB [8], [9] is because it provides the following features,

- It allows for ZVS and, therefore, high-frequency switching.
- It provides isolation between the input and output ports.

- It allows for the transfer of power in both directions.
- It supports many modulation techniques.

The DAB shows much potential as a DC-to-DC converter and has been used to achieve extremely high power densities [3]. It has been applied in AC-to-AC converters and has shown promising results. Qin and Kimball demonstrate an AC-to-AC DAB that has an efficiency of over 90 % under full load conditions using a DAB topology with four-quadrant switches [10]. Furthermore, they have demonstrated the effectiveness of ZVS in this converter [11]. The use of the DAB as an AC-to-AC converter does not seem to progress from the contributions made by Qin and Kimball in 2009. Facchinello *et al.* [12] have published a paper in 2016 on a hybrid DAB which applies a similar DAB AC-to-AC converter in a multi-cellular (cascaded) fashion. Aside from this work, there hasn't been much movement to use the DAB in an AC application.

To approximate the volume of power converters, the energy storage devices, as well as the thermal management systems, are investigated as these significantly contribute to the volume [1]. The silicon components are assumed to use a negligible amount of volume, however, their real contribution to the volume of the circuit is in their losses which lead to larger heat sinks.

In the sections following, the choices that were made in this section are discussed in more depth and the volume of the reactive and thermal management systems are defined.

2.2 Existing Topologies

A number of reviews have been performed on many inverter topologies. This section outlines the important findings that these reviews present along with the relationships that they share.

2.2.1 Multi-Level Inverters

The design of power converters seems to be moving towards what is known as "multi-level" techniques. In the year 2000, Peng argued that there are

three types multi-level converters: “cascaded, diode-clamped, and capacitor-clamped” [13].

Multi-level diode-clamped and capacitor-clamped converters seem to focus more on switching networks, these networks allow for the output voltage to be changed depending on how the network is configured at that point in time.

Multi-level cascaded converters seem to focus on the use of many known conversion topologies that are cascaded together to form a new topology with additional functionality.

Rodríguez *et al.* indicate that industry is moving towards multi-level topologies [14], they present many of these topologies including a generalised diode-clamped model first proposed by Peng [13]. Daher *et al.* agree that industry is moving in this direction, however, balancing the capacitor voltages in these multi-level systems is complicated. They, therefore, disagree with the notion that industry will move to any systems that have more than three levels due to the practical implications involved when increasing levels from this point [15].

The aim of having multiple levels is to create a waveform that is closer to the required output. This reduces the stress on the output filter and leads to a decrease in the distortion of the filtered output waveform. As the number of levels increases, the output waveform gets closer to the required waveform. An inverter designer would take Peng’s “M-level” diode-clamped converter and try to increase M to as high a number as possible [13]. However, due to the control limitations mentioned by Daher *et al.* [15], one could conclude that a designer would not be able to implement this model with real circuitry and see Peng’s predicted results.

This is where multi-level cascaded topologies show promise. A good analogy to use for these topologies would be a comparison between a group of Dung Beetles and an army of Ants.

If a stone is to be moved, how many Ants would need to be used compared to the number of Dung Beetles?

Once these numbers have been established, the total volume of the number of Dung Beetles versus the army of Ants can be calculated. In some cases, the volume of the Ants may be less than the volume of the Dung Beetles,

and in other cases, may be the opposite. This is the same for multi-cellular topologies, the question of when it is beneficial to have multiple smaller cells working together to achieve the same output as fewer larger cells is asked.

Kolar *et al.* have shown that there are cases where having a number of smaller cells leads to extremely high power densities compared to other converters that currently exist [3]. They achieved a $2.2\,\mathrm{kW\,dm^{-3}}$ density using six cells. In this case, they found the power density to be higher using multiple cells compared to a single cell converter. Kasper, Bortis, and Kolar state that there is a relationship between the number of cells and the volume of the converter. This relationship is, ideally, exponential in nature as shown in Equation (2.1) [16],

$$\frac{V}{V_0} = \left(\frac{P}{P_0}\right)^{\frac{3}{2}} \tag{2.1}$$

where,

- V_0 volume of the original module;
- V volume of the smaller module;
- P_0 processed power of the original module;
- P processed power of the smaller module.

Although this is an ideal scaling law, it does show that there is a reason why multi-level cascaded systems may have higher power densities when compared to their single-level counterparts. Fundamentally, the cells that make up a multi-level cascaded system are the same as a single-level converter with lower requirements and specifications. Effectively, the power processed between each cell is reduced as the workload is spread between all of the cells.

In this research, the focus is put into optimising a single-level converter. However, the topological choice of the single-level converter is one that supports multi-level cascading because this could lead to higher power densities. What's important to note here is the fact that, when designing a multi-level cascaded system, the topology does not change in each cell and optimising the power density of a single cell would lead to a higher power density in the entire cascaded system.

2.2.2 Multi-Stage Converters

Xue *et al.* [17], as well as Kjaer *et al.* [18] provide reviews on inverter topologies. Kjaer *et al.* focus on grid-connected applications whereas Xue *et al.* focus on general single-phase inverter topologies. Both groups separate inverters into two categories, single-stage inverters and multistage inverters.

A single-stage inverter converts directly from DC-to-AC, whereas, a multi-stage inverter usually has a DC-to-DC converter and from that, a DC-to-AC converter follows. The benefit of having a multi-stage inverter is that it allows for a larger input voltage range because the DC-to-DC stage can adjust the output to what is required for the DC-to-AC stage. This comes at the cost of a higher component count and an increase in complexity.

Multi-stage inverters, in most cases, also offer isolation which can be beneficial when applying Partial Power Processing (PPP) techniques. PPP involves connecting the input and output terminal directly so, instead of processing all of the power, the PPP converter only processes the power required that is above or below the power being provided by the input. PPP is discussed further in Chapter 5. It was not investigated in this research, but it does provide benefits and should be considered in future work.

Xue *et al.* discuss the trend direction towards lower component counts in inverters and state that single-stage inverters offer lower component counts over multi-stage inverters [17]. Kjaer *et al.* disagree with this trend by stating that single-stage inverters, generally, should not be used unless no amplification is required from the input voltage [18]. The metrics used to evaluate the topologies reviewed are quite similar between groups. They both agree and emphasise the importance of soft-switching.The differences show where Xue *et al.* look at [17],

1. whether the topology is single-stage or multi-stage;
2. how power decoupling is achieved;
3. and whether isolation is possible.

Kjaer *et al.* use similar metrics but add to this theoretical analysis by demonstrating practical parameters such as efficiency and THD [18].

A single-stage or multi-stage inverter is a design choice, the importance here is in the way that Xue *et al.* and Kjaer *et al.* see value in converter isolation. The topological choice in this research takes this consideration into account by ensuring that isolation between the input and output terminals is possible. Not only does this agree with both groups, but it allows for the novel use of the DAB as a DC-to-AC converter.

2.2.3 Topological Considerations

Based on the previous sections, there are a number of important factors that were considered when choosing a topology to use for this research. The topology should,

- Support multi-level configurations with preference on a cascaded system over a diode-clamped or capacitor-clamped system.
- Provide the ability for soft-switching, thereby, allowing for the use of high-frequency switching (the need for high-frequency switching is discussed further in Section 2.5.1).
- Allow for a number of modulation techniques to be applied, thereby, allowing for many control methods to be implemented.
- Provide isolation between the input and output, thereby, supporting the PPP configurations and any other configurations that require isolation.

Based on these requirements, the decision was made to utilise the Dual Active Bridge. The concept of the Dual Active Bridge was published in 1992 by Kheraluwala *et al.* [8] and has been widely used since (mainly in DC-to-DC applications). It provides many benefits such as,

1. Soft-switching.
2. Isolation between the input and output terminals.
3. Control of the output voltage.
4. A large number of modulation scheme options to apply.

Steigerwald *et al.* review high power DC-to-DC converters [19]. The baseline comparison is the conventional H Bridge (discussed in Section 2.2.4). They found that the Dual Active Bridge is ideal for applications when bidirectional power flow is needed which allows for reactive output loads. Krismer adds to the work published by Kheraluwala *et al.* [8] by performing detailed analysis and modelling on the DAB [20] and outlines many loss models that can be applied, different modulation techniques, and optimisation methods.

Much work has been performed on the DAB, and it has shown promising results. Qin and Kimball demonstrate the effectiveness of the DAB as an AC-to-AC converter [11]. What is interesting to note here is that they aim to reduce the bulk of passive components and they have achieved that aim. However, what they have not shown is how the volume of these components change as the design parameters of the DAB changes. There is a need for knowledge development in this area. Not only can a comparison between the power density of DAB and the power density of the SPWM be shown, but the relationships between parameters and the volume of the DAB can be established.

It should be noted that the DAB in this research is used differently to the AC-to-AC converter made by Qin and Kimball. In this research, the DAB creates a full wave rectified sinusoidal output waveform. This waveform then enters a low-frequency inverter stage to form the positive and negative half-cycles. Qin and Kimball have an input voltage that moves between the positive and negative domain and they modify this waveform into the AC waveform that they require at the output.

2.2.4 Sinusoidal Pulse Width Modulation Inverter

The inverter that is used as the baseline comparison is the conventional H bridge, shown in Figure 2.1 below, that is modulated to form a sinusoidal output. This circuit uses a method of Sinusoidal Pulse Width Modulation (SPWM) over an LC filter to create an AC output [21], [22]. The H Bridge does not accommodate for soft switching because the direction of the current through the inductor does not change direction over a switching cycle. In other words, the current does not go from positive to negative or negative to positive, it remains positive or negative through the whole cycle. This means

that, when using this topology, the switching frequency is kept relatively low to reduce switching losses. This does, however, impose stress on the filter as the low frequency harmonic components are higher in magnitude compared to those in a higher frequency waveform. The stress on the filter leads to the need for larger inductive and capacitive components and this relationship is demonstrated in Section 3.1.1.2.

In order to reduce the stress on the filter, the switching frequency should be increased. There is a clear relationship between the filter stress and the switching losses in this circuit as well as the filter stress and volume of the filter (through the cut-off frequency of the filter). The SPWM is analysed and presented in Chapter 3.

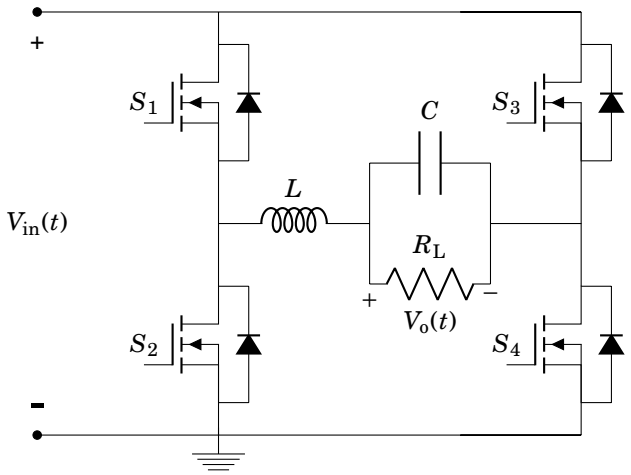


Figure 2.1: The conventional H Bridge circuit, this circuit applies Sinusoidal Pulse Width Modulation over the LC filter to create an AC output over R.

2.2.5 Modulation Techniques

Holmes and Lipo outline Pulse Width Modulation (PWM) in power converters in great detail [23]. There are three main methods that affect the switch-on times of a PWM waveform, these are naturally sampled, regular sampled, and measured directly. To give a brief outline, Holmes and Lipo define these methods as follows,

- Naturally sampled waveforms are PWM signals that trigger when the carrier waveform intercepts with the required output waveform.

- Regularly sampled waveforms are similar to the naturally sampled waveforms, however, the carrier waveform is sampled. In this case, the interception may be missed because the sample points are discrete, but this system would switch on when there was a crossover between the previously sampled point and the current one.
- Direct PWM integrates the required waveform and creates a pulse that shares the same area.

In the case of this research, regularly sampled PWM methods are used as the calculations are done digitally. The simulations use digital inputs into the switches and do not use comparators and other circuit components to form the output SPWM waveform. This allows for consistency between the calculated waveforms used in approximations and the simulation waveforms.

The SPWM waveform, in this case, is regularly sampled and the pulse widths and start and end times do not change over each output waveform period. It is a set waveform and does not change. A control technique could be applied to vary the switching times and pulse widths to ensure that the output waveform matches the required output. However, this introduces a number of complexities into the model. Instead of focusing on the circuit itself, the focus changes to the modulation technique which drastically increases the scope as a number of control techniques could be used. For this research, an open-loop system is used to manage the scope.

2.3 Physical Volume Approximation

The first-order physical volumetric approximations of each circuit component are based on pre-existing electromagnetic formulae. These formulae include approximations for capacitors, inductors, high-frequency transformers, and heat sinks. This chapter outlines these first-order approximations which are used throughout the research to determine the approximate volumes of each converter.

The work done by de Jong *et al.* [24] demonstrates how power electronic circuits can be printed and packaged to achieve high density packaging. It is

important to note that the volumetric approximation in this research does not consider the packaging of the circuit, but focusses on the individual volumes of each component in the circuit. The reason for this is because there are many ways to package the circuit in a 3-Dimensional space to optimise volume and the aim of this research is to look at the circuit itself and not the placement of each element.

2.3.1 Capacitors

The energy in a capacitor can be written as,

$$E_c = \frac{1}{2}CV^2 \tag{2.2}$$

where C is the capacitance of the capacitor and V is the voltage over the capacitor. If the capacitance is defined as the volume of the capacitor multiplied by the density [25],

$$C = C_{\text{vol}}C_{\text{den}} \tag{2.3}$$

where C_{vol} is the volume of the capacitor and C_{den} is the density of the capacitor. It can be seen that substituting Equation (2.3) into Equation (2.2) leads to,

$$\begin{aligned} E_c &= \frac{1}{2}V^2 C_{\text{vol}}C_{\text{den}} \\ C_{\text{vol}} &= \frac{2E_c}{V^2}\frac{1}{C_{\text{den}}} \end{aligned} \tag{2.4}$$

Equation (2.4) is utilised to determine the volume of the capacitor given a certain energy that must be stored. The capacitor density that is used in this equation is discussed and defined in Section 2.4.1 below.

From Equation (2.4) it can be seen that the volume of the capacitor is dependent on the energy stored by the capactor as well as the peak voltage requirement across the capacitor. In the case of this research, the voltage is chosen at a fixed value to match the GLBC reqiurements. The voltage, however, is parameterised throughout this research meaning that the output voltage could be changed the models would accomodate for this. Increasing the output voltage to decrease the volume of the capacitor was not considered in this research due to the aim to achieve the GLBC requirements.

2.3.2 Inductors

The energy stored by an inductor can be written as,

$$E_L = \frac{1}{2} L I^2 \tag{2.5}$$

where L is the inductance, and I is the current through the inductor.

$$\begin{aligned} L &= \frac{N^2}{\mathcal{R}} \\ \mathcal{R} &= \frac{l_c}{\mu_0 \mu_r A_c} \\ I &= \frac{H l_c}{N} \\ B &= \mu_0 \mu_r H \end{aligned} \tag{2.6}$$

where,

- N number of turns or windings;
- μ_0 the magnetic constant;
- μ_r the relative permeability;
- A_c the cross-sectional area of the core;
- l_c the length of the core;
- B flux density through the core;
- H magnetic field strength.

This leads to the equation,

$$A_\mathrm{c} l_\mathrm{c} = \frac{2\mu_0 \mu_\mathrm{r}}{B^2} E_L \tag{2.7}$$

where $A_\mathrm{c} l_\mathrm{c}$ is effectively the volume of the inductor (it is the volume of the core of the inductor without winding contribution). The alternative to calculating the volume of an inductor is similar to that mentioned in Section 2.3.1,

$$L_\mathrm{vol} = \frac{2E_L}{I^2} \frac{1}{L_\mathrm{den}} \tag{2.8}$$

where L_vol is the volume of the inductor and L_den is the energy storage density of the inductor. In this case, the volume of the inductor is seen to be related to the energy stored as well as the peak current through it. The peak current, I, is extremely important in this case because both the SPWM and the DAB have high frequency currents that move through the circuit and the peaks of these currents have an impact on the volume of the inductor. It should be

noted that the winding volume of the inductor is not considered in order to reduce complexity of the volumetric approximation by removing the dependence on the core shape. Taking the winding volume into account would reduce the magnetic energy storage density if it were considered but would introduce the need to calculate the number of turns each time an inductor is required in the circuit design. Instead, a standard inductive density is used, this density can be modified if the winding density needs to be considered. Considering the winding volume in the inductor design is discussed in further detail in Chapter 5.

The volume of the inductor can be calculated using Equation (2.8), and this equation is used throughout this research. The density of the inductor is discussed and defined in Section 2.4.2.

2.3.3 High-Frequency Transformer

The standard E-core may be defined using the dimensions presented in Figure 2.2 below [26]. In this case, the volume of the core can be calculated as,

$$V_{\text{core}} = 2d_1h_1w - 2h_2w(d_2 - d_3) \tag{2.9}$$

The windings contribute significantly to the volume of the core as well. Hurley, Gath, and Breslin [27] mention methods in which to minimise the losses in multilayer transformers. From their findings, one can establish the number of layers required to minimise the loss. This, however, adds additional complexity to the model. Instead of calculating the volume of the winding based on the number of layers required, it was decided to reverse the design flow. The E-core that can provide the required winding window size is chosen, and the winding volume is assumed to take up all of the window space. The reason that the full winding volume is assumed, is to reduce complexity and it means that the optimal E-core would be used during the design process. The additional space provided when windings are not there would not be considered as a reduction in volume, forcing the transformer designer to use a smaller core if the winding window is not utilised fully.

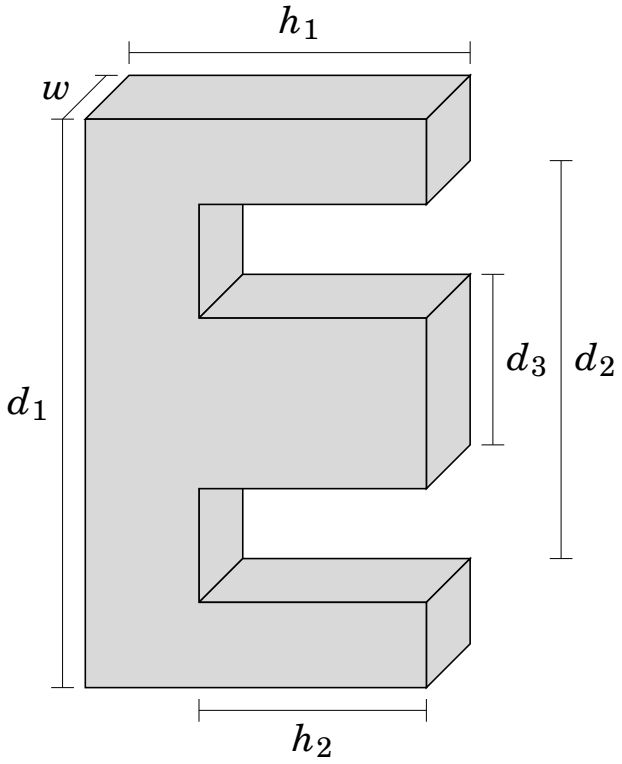


Figure 2.2: The dimensions used to calculate the volume of a standard E-core, provided by The International Magnetics Association [26].

As demonstrated in Appendix C, the smallest E-core that fits the winding requirement is chosen in the design of the DAB. This is discussed in more detail in Chapter 4. This simplifies the approximation of the volume of the transformer because the volume of the core, as well as the windings, can be calculated using the standard E-core dimensions. The volume of the windings is calculated as a cuboid that fits around the central arm and fills the winding window,

$$V_{\text{wire}} = 2\big(d_2 - d_3\big)h_2\big(w + d_2\big) \tag{2.10}$$

The final volume of the transformer is the combination of the core and the windings,

$$V_{\text{t}} = V_{\text{core}} + V_{\text{wire}} \tag{2.11}$$

The volumes of these standard E-cores are given in Table 2.1. These volumes will be used in the calculation of the volume of the DAB.

Table 2.1: The volumetric approximations calculated using standard E-core dimensions as well as an approximated winding window volume and cross-sectional area.

Name	V_{core}	V_{wire}	V_{tot}	A_{e}
	cm^3	cm^3	cm^3	cm^2
E13/4	0.419	0.735	1.154	0.137
E16/5	0.892	1.487	2.379	0.221
E20/6	1.733	2.815	4.548	0.348
E25/7	3.543	4.927	8.470	0.563
E32/9	7.032	11.464	18.496	0.903
E42/15	18.513	27.094	45.607	1.800
E42/20	24.684	30.039	54.723	2.400
E55/21	47.552	50.952	98.504	3.570
E55/25	56.610	54.349	110.959	4.250
E65/27	86.378	87.308	173.686	5.400

where,

A_{e} $= d_3 \times w$, the cross sectional area;

2.3.4 Heat Sink

There are many ways to configure a heat sink. For instance, in the same volume, a heat sink could contain five 1 mm thick plates with a 2 mm gap between each, or, three 1 mm thick plates with 5 mm gaps between them. There are many possibilities that could lead to the heat sink performing differently in this research. Due to this, the optimisation of the heat sink is out of the scope of this research.

Instead of performing this optimisation, the heat sink is parameterised as a volume that specifies the rate at which Watts are dissipated per second. Billings defines the thermal radiation properties of certain metals as a function of the heat sink temperature definition, which can be used to approximate the volume requirement of a heat sink [28]. In this case, matt painted aluminium with a 100 °C differential is just under $0.8\,\text{W}\,\text{in}^{-2}$. This property is for a metal plate that radiates heat on both sides. Metal fins on heat sinks vary in widths, additionally, the air gaps between them vary. Assuming that the fin and the air gap are about 2 mm wide, the heat sink density, D_{hs}, is approximately,

$$D_{\text{hs}} \approx 620\,\text{kW}\,\text{m}^{-3} = 0.62\,\text{W}\,\text{cm}^{-3} \tag{2.12}$$

Again, this is a very rough approximation, however, in the research that follows, the models are parameterised, and D_{hs} can change. Furthermore, the volumes of these models for different values of D_{hs} are investigated to demonstrate how volumes would change with a change in heat sink density. This means that the specific value of D_{hs} is not vital, provided that it is in the same order of magnitude as the real world, as it is changed to show how the volumes of these converters would change with improvements in its density. This density focuses on naturally cooled heat sinks, changing the cooling mechanism to use moving air or water would have a dramatic effect on the density. These other cooling mechanisms will not be considered in this research. However, since the density is parameterised as D_{hs}, it would be possible to see the effects of these cooling systems in the models derived throughout this research by substituting D_{hs} with the densities provided by these technologies. Figure 2.3 demonstrates the size of a heat sink that would be able to remove approximately 77.5 W from the system. This figure is solely used to demonstrate what $620\,\text{kW}\,\text{m}^{-3}$ represents in this research and what size the heat sink would be if it were ten times smaller or even one hundred times smaller.

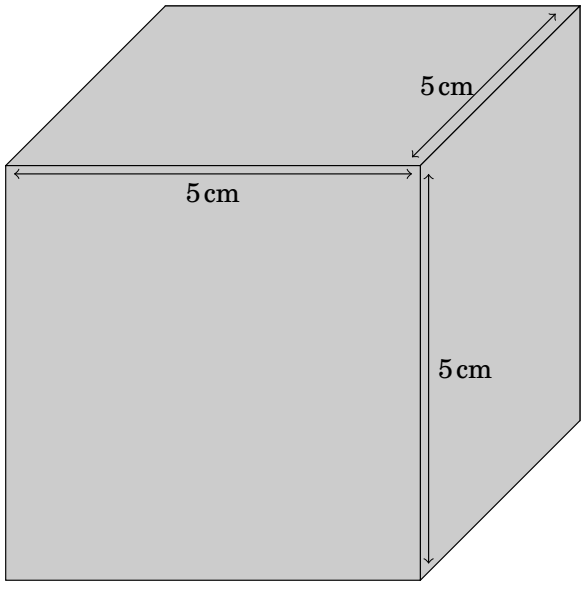


Figure 2.3: The size of a heat sink that would dissipate approximately 77.5 W. This heat sink is $125\,\text{cm}^3$ and is drawn to scale.

2.4 Energy Storage Potentials of Existing Technology

The energy storage potential of the filter components are calculated as,

$$E_{\mathrm{C}} = \frac{1}{2} C V_{\mathrm{C(p)}}^2 \tag{2.13}$$

$$E_{\mathrm{L}} = \frac{1}{2} L I_{\mathrm{L(p)}}^2 \tag{2.14}$$

where $V_{\mathrm{C(p)}}$ is the peak voltage over the capacitor and $I_{\mathrm{L(p)}}$ is the peak current through the inductor. Inductors and capacitors have different energy densities. Defining the energy density of the inductor as W_{m} and the energy density of a capacitor as W_{e}, Equation (2.13) can be written as follows,

$$\begin{aligned} E_{\mathrm{C}} &= C_{\mathrm{vol}} W_{\mathrm{e}} \\ C_{\mathrm{vol}} &= \frac{1}{2W_{\mathrm{e}}} C V_{\mathrm{C(p)}}^2 \end{aligned} \tag{2.15}$$

where C_{vol} is the physical volume of the capacitor, and W_{e} is the energy density of an electric field in a capacitor.

Additionally, Equation (2.14) can be written as,

$$\begin{aligned} E_{\mathrm{L}} &= L_{\mathrm{vol}} W_{\mathrm{m}} \\ L_{\mathrm{vol}} &= \frac{1}{2W_{\mathrm{m}}} L I_{\mathrm{L(p)}}^2 \end{aligned} \tag{2.16}$$

where L_{vol} is the physical volume of the inductor and W_{m} is the energy density of the magnetic field from an inductor.

The total volume of the filter is then determined using Equations (2.15) and (2.16),

$$\begin{aligned} F_{\mathrm{vol}} &= C_{\mathrm{vol}} + L_{\mathrm{vol}} \\ &= \frac{1}{2W_{\mathrm{e}}} C V_{\mathrm{C(p)}}^2 + \frac{1}{2W_{\mathrm{m}}} L I_{\mathrm{L(p)}}^2 \end{aligned} \tag{2.17}$$

Albert Eßer analyses energy densities for electric and magnetic fields in air. Given that the electric field breakdown voltage in air is about $3\,\mathrm{MV\,m^{-1}}$, he

finds the energy density of an electric field through air has a maximum value of [29],

$$W_{\mathrm{e}} \approx 40\,\mathrm{kJ\,m^{-3}} \tag{2.18}$$

Given that the maximum magnetic field strength is about 400 mT through air, the maximum density of a magnetic field through air is about [29],

$$W_{\mathrm{m}} \approx 64\,\mathrm{kJ\,m^{-3}} \tag{2.19}$$

In this case, the volume of the filter would be reduced if it were to have a large inductor and small capacitor. However, capacitors use dielectrics to increase the breakdown voltage between the plates. Additionally, inductors are not just air gaps, they contain cores with windings around them. The energy storage densities used during the filter design are discussed in Sections 2.4.1 and 2.4.2 below. In these sections, it is shown that capacitors have higher power densities than inductors when analysing current technology.

2.4.1 Capacitive Energy Density

A dielectric used in a capacitor changes the energy density due to the change in permittivity. The relative permittivity of a dielectric can be written in the following way,

$$\varepsilon_{\mathrm{r}} = \frac{\varepsilon}{\varepsilon_0} \tag{2.20}$$

where,

- ε_{r} relative permittivity of the dielectric;
- ε permittivity of the dielectric;
- ε_0 $\approx 8541878 \times 10^{-12}$, vacuum permittivity.

The energy density of a dielectric is calculated using the following equation,

$$W_{\mathrm{e}} = \frac{1}{2}\varepsilon_{\mathrm{r}}\varepsilon_0 E^2 \tag{2.21}$$

where E is the perpendicular electric field through the dielectric.

Chen investigated capacitors with the highest energy density in 2012 with the help of Page [30]. He found the Panasonic Series EE type A capacitor to

have the highest energy density (from the set of electrolytic capacitors) with a density of [30],

$$W_e = 656.5\,\mathrm{mJ\,cm^{-1}} = 656.5\,\mathrm{kJ\,m^{-3}} \tag{2.22}$$

Throughout this research, the value of $656.5\,\mathrm{kJ\,m^{-3}}$ is used as the energy density for a capacitor. The energy density of the capacitor is parameterised in the models which means that it can be changed as the densities in industry improve.

2.4.2 Inductive Energy Density

The inductor is designed using a toroid as the core with an air gap to store the magnetic energy. Current technologies utilise soft magnetic composites to form the core. These composites are ferrite particles that have a layer of insulation around them, this method of insulating individual particles reduces eddy current losses and reduces loss at higher frequencies [31]. This method effectively alters the permeability in the core. To model this effect, these composite ferrite cores are made to look like a pure ferrite core with an air gap in the following way,

$$V_c = V_{Fe} + V_{Air} \tag{2.23}$$

where,

- V_c volume of the composite core which is based on current technologies;
- V_{Fe} volume of pure ferrite in the model core;
- V_{Air} volume of the air gap in the model.

The weighted permeability of the actual core and the model needs to be the same which leads to,

$$\mu_c V_c = \mu_{Fe} V_{Fe} + \mu_{Air} V_{Air} \tag{2.24}$$

where,

- μ_c permeability of the composite core which is based on current technologies;
- μ_{Fe} permeability of pure ferrite in the model core;
- μ_{Air} permeability of the air gap in the model.

Substituting Equations (2.23) and (2.24) leads to the following relationship,

$$\frac{V_{\text{Air}}}{V_{\text{c}}} = \frac{\mu_{\text{Fe}} - \mu_{\text{c}}}{\mu_{\text{Fe}} - \mu_{\text{Air}}} \tag{2.25}$$

From this relationship, a method for calculating energy density of toroidal inductors based on current technology has been derived. Toroids manufactured by Ferroxcube are made from a number of compounds, however, the 4C65 material is an applicable material due to the relatively low permeability and relatively high saturation flux density compared to the other materials that Ferroxcube provides. The 4C65 material has a relative permeability of 125 and a saturation flux density of 380 mT [32]. Using the following permeability values,

$$\mu_{\text{c}} \approx 200\,\text{H}\,\text{m}^{-1} \tag{2.26}$$

$$\mu_{\text{Fe}} \approx 5000\,\text{H}\,\text{m}^{-1} \tag{2.27}$$

$$\mu_{\text{Air}} \approx 1\,\text{H}\,\text{m}^{-1} \tag{2.28}$$

the energy density of a core of this type would be,

$$\begin{aligned} W_{\text{m}} &= \frac{1}{2}\frac{5000-125}{5000-1}\frac{1}{(4\pi\times10^{-7})(1)}(380\times10^{-3})^2 \\ &\approx 56.03\,\text{kJ}\,\text{m}^{-3} \end{aligned} \tag{2.29}$$

TDK provides toroids made from the K1 material [33]. This material has a relative permeability of 80 and a saturation flux density of 310 mT. The energy density of this core is calculated as,

$$\begin{aligned} W_{\text{m}} &= \frac{1}{2}\frac{5000-80}{5000-1}\frac{1}{(4\pi\times10^{-7})(1)}(310\times10^{-3})^2 \\ &\approx 37.633\,\text{kJ}\,\text{m}^{-3} \end{aligned}$$

Throughout this research, the value of approximately $56.03\,\text{kJ}\,\text{m}^{-3}$ is used as the energy density for an inductor. Similarly to Section 2.4.1, the energy density is parameterised in the models throughout this research allowing for the value to change as these densities improve in industry.

2.5 Techniques for Increasing Power Density

Kolar *et al.* [2], as well as Mirjafari *et al.* [34], discuss the general limitations of power electronics and mainly consider the following aspects to be the most important,

1. Weight
2. Volume
3. Losses
4. Cost
5. Failure Rate

The limitations by both groups are found by applying Pareto Frontiers to circuit models. There is no contradiction between the two research groups in what they believe are the major limiting elements in power electronics. A slight difference between the two groups is that Mirjafari *et al.* focus more specifically on inverters, whereas, Kolar *et al.* discuss power electronics more generally. Mirjafari *et al.* discuss specific modules that make up an inverter and optimise the inverter on a component level. Once the design has been optimised, it is classified by the volume, weighted efficiency, and failure rate to find the optimal results. It can be seen from both cases that, although the power density depends on the volume of the circuit, many factors influence the overall power density and volume of the converter.

2.5.1 High-Frequency Switching

It is generally accepted that higher frequencies lead to smaller reactive components. Kolar *et al.* provide an optimisation graph where they demonstrate the the power density, ρ, increases as the switching frequency, f_{P}, increases [2]. As the switching frequency increases, the efficiency, η, decreases. What can be seen in their optimisation is that a switching frequency increase leads to an increase in power density but the power density begins to taper off at higher frequencies. One can conclude from their research that moving to higher switching frequencies is beneficial to an extent and after that point,

losses and other factors lead to the power density remaining the same (or possibly decreasing).

In this research, the switching frequency is limited to compare the topologies in the case study. More detail is discussed in Section 2.6.1 below.

2.6 System Specifications

The design of this inverter is based on constraints implemented by the GLBC due to its current relevance. The specifications that this inverter should either match or improve are presented in Table 2.2.

The comparisons between the SPWM and DAB are based on these specifications for this research. However, the models are parameterised for each topology so that these specifications can be adjusted to see their effects on the power densities of each converter.

The output frequency used in this research is 60 Hz. Although South Africa uses 50 Hz, this research uses 60 Hz to match the specifications of the GLBC. Again, the output frequency, f_o, is parameterised and can be changed to 50 Hz in the models if needed.

Table 2.2: The specifications on which designs throughout this research are based. These specifications mirror the Google Little Box Challenge [6].

Specification Name	**Specification Value**
Input Voltage, V_{in}	450 V (DC)
Input Power, P_{in}	2 kW
Peak Output Voltage, $V_{o(p)}$	339 V
Output Frequency, f_o	60 Hz
Total Harmonic Distortion (THD)	5 %
Output Current Ripple	5 %
Output Voltage Ripple	5 %

2.6.1 Switching Frequency Limitation

A comparison is made between the SPWM and the DAB as an inverter in this research. The simulated frequency ranges for the SPWM and the DAB were kept relatively similar in order for the models and comparisons to overlap. The SPWM is simulated between a range of 6 kHz and 72 kHz and the DAB is simulated between 24 kHz and 72 kHz. The reason for the discrepancy between the SPWM and DAB starting frequencies is due to the assumption that the most optimised SPWM volume would be at a relatively low range compared to the DAB. This assumption was verified in the research and can be seen in Chapter 5 where the SPWM reached a minimum volume at a low frequency and the volume of the DAB continued to decrease as the frequency increased. Appendices B and D show the simulation instructions as well as the simulation results and waveforms for the SPWM and DAB respectively.

2.6.2 Load Resistance

The load resistance used in this research is purely resistive to reduce the complexity of the models. It is chosen using the following formulae,

$$\begin{aligned} \boldsymbol{P}_{\mathrm{o}}(t) &= \frac{{V_{\mathrm{o(p)}}}^2}{R}\sin^2(2\pi f_{\mathrm{o}} t) \\ \langle \boldsymbol{P}_{\mathrm{o}}(t)\rangle &= \frac{{V_{\mathrm{o(p)}}}^2}{R}\frac{1}{T_{\mathrm{o}}}\int_0^{T_{\mathrm{o}}}\sin^2(2\pi f_{\mathrm{o}} t)\,\mathrm{d}t \\ \langle \boldsymbol{P}_{\mathrm{o}}(t)\rangle &= \frac{1}{2}\frac{{V_{\mathrm{o(p)}}}^2}{R} \\ R &= \frac{1}{2}\frac{{V_{\mathrm{o(p)}}}^2}{\langle \boldsymbol{P}_{\mathrm{o}}(t)\rangle} \end{aligned} \tag{2.30}$$

Using an ideal output power of 2 kW, the load resistance is found to be $R = 28.8\,\Omega$.

2.7 Summary

This chapter has provided the base knowledge required to approach this research. Figure 2.4 below demonstrates how this knowledge contributes to the entirety of the research at hand. The most important points to take from this chapter are,

- A number of topologies for inverters have been reviewed. The important factors that should be considered are,
  - Multi-level cascaded systems.
  - Soft-switching support which allows for high-frequency switching.
  - Isolation between the inverter input and output.
  - The ability to use different modulation schemes which allows for more forms of control to be applied.
- The DAB has been chosen as the topology that will be investigated for the relationships between volume and high-frequency switching, Zero Voltage Switching, and modulation schemes due to the functionality it offers as a DC-to-DC converter.
- When modelling the volume of capacitors, an energy density of $656.5\,\mathrm{kJ\,m^{-3}}$ is used.
- When modelling the volume of inductors, an energy density of $56.03\,\mathrm{kJ\,m^{-3}}$ is used.
- The heat sink density used in this research is $620\,\mathrm{kW\,m^{-3}}$ and focuses on naturally cooled heat sinks. Other cooling systems are not considered in this research, however, the heat sink density value can be changed to model these other systems.
- All density values are parameterised in the research to allow for them to change as industry progresses. This means that the models are not locked into current technologies and current energy densities.
- A frequency of 60 Hz is used in this research in order to fit the GLBC specifications even though South Africa would require a 50 Hz inverter.
- The load resistance used in the models throughout this research is chosen to be $28.8\,\Omega$ which is calculated as the optimal load for a 2 kW average output power that is sinusoidal at 60 Hz with a peak voltage of 339 V.

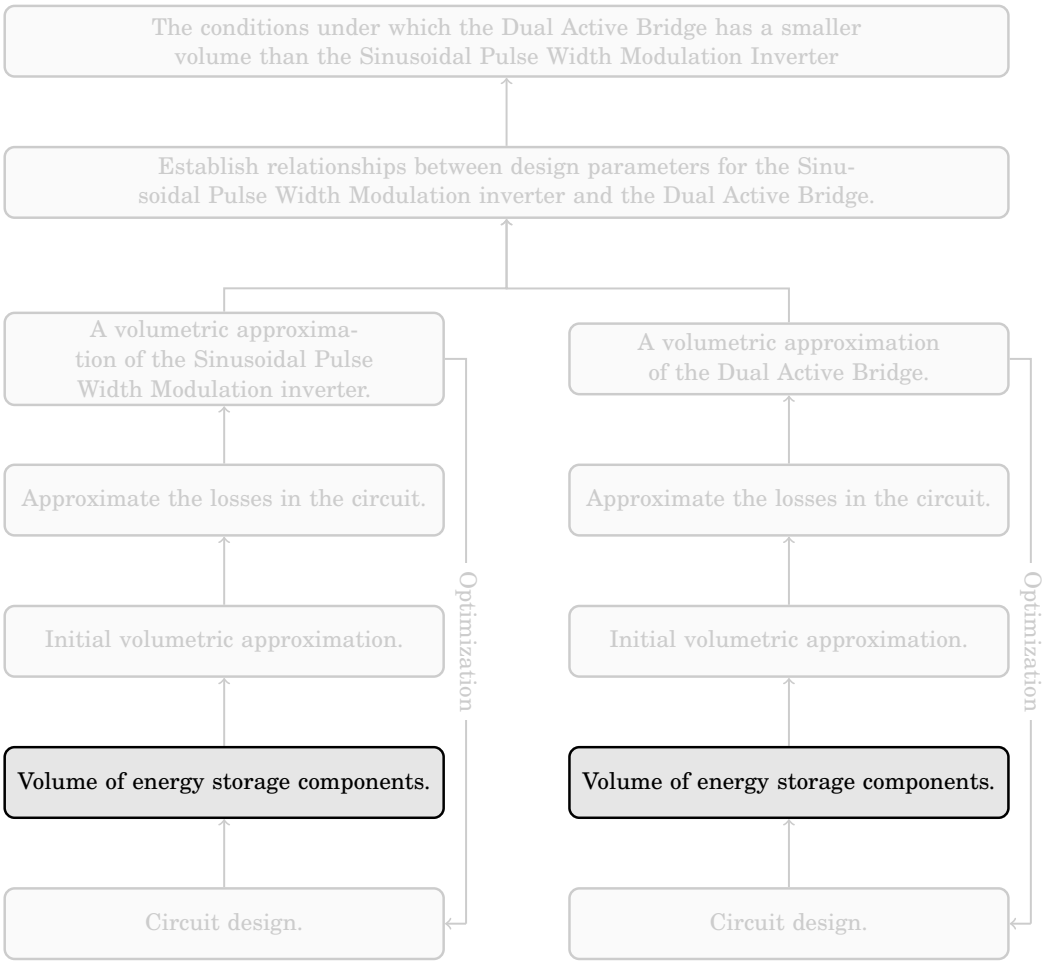


Figure 2.4: The contribution to the overall argument provided by Chapter 2.

The Sinusoidal Pulse Width Modulation Inverter 3

The Sinusoidal Pulse Width Modulation (SPWM) inverter varies the duty cycle of a PWM signal to average a sinusoidal waveform more closely than a square wave that is switching at the sinusoidal wave's fundamental frequency. This reduces the power in the lower harmonics, thereby, reducing the filter requirements on the output.

The chapter flow is demonstrated in Figure 3.1 below. The switching frequency is changed until the optimal volume for the SPWM inverter is found. The SPWM waveform generation, as well as the filter required to reduce the harmonic content of this waveform over the output is discussed in Section 3.1. Once the filter specifications have been found, the semi-conductive losses are found and this is covered in Section 3.2, losses due to the inductor aren't considered in the loss approximation to simplify the model. This allows for the relationships between the design parameters and the volume of the inverter to be established which is covered in Section 3.4. Finally, the "best of class" SPWM inverter that meets the system specifications mentioned in Table 2.2 is found and this model is used to compare to the topology discussed in Chapter 4.

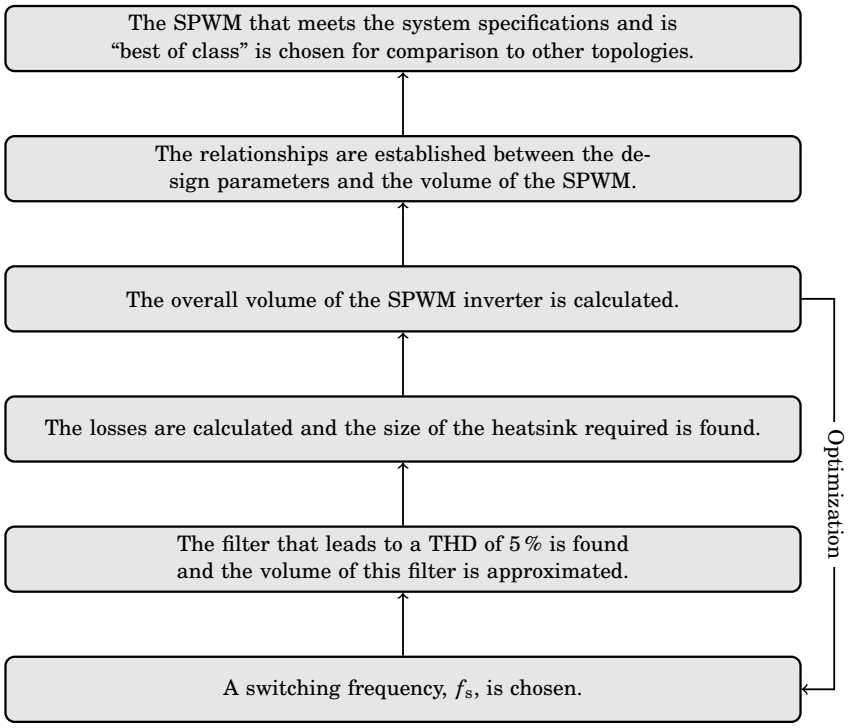


Figure 3.1: The process followed to approximate the SPWM inverter volume and find the SPWM inverter that has the smallest volume that meets the system requirements.

3.1 Ideal Model

The ideal model involves the volumetric approximation of the filter. No losses are taken into account in this model, the approximation that takes loss into account is described in Section 3.2.

3.1.1 Waveform

The unipolar SPWM works on a system of finding the points of intersection between a triangular waveform and two control signals. The first control waveform is the required output waveform and the second is the negative of the first. The second may also be described as the first with a phase difference of π radians. The triangular wave has the amplitude of the DC input voltage, V_{in}, and the frequency is the switching frequency, f_s, of the inverter. A graphical demonstration of these waveforms is given in Figure 3.2. It is important to note that the switching frequencies, f_s, used throughout this section are chosen to be integer multiples of the output frequency, f_o. In mathematical terms,

$$f_s = n f_o, \quad n \in \mathbb{W} \tag{3.1}$$

This ensures that the triangular waveform fits over the output waveform and is able to share the same period, allowing for the calculation of the intercept times using the methods defined in Section 3.1.1.1.

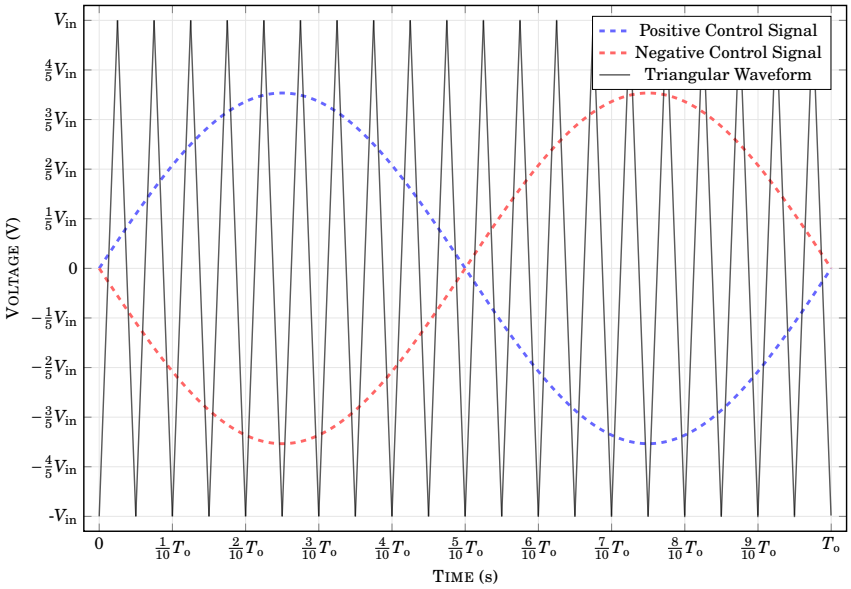


Figure 3.2: The control waveforms superimposed on a triangular waveform to form the PWM waveforms, $\boldsymbol{V}_A(t)$ and $\boldsymbol{V}_B(t)$. Image adapted from [21].

SPWM inverters use bipolar or unipolar techniques to modulate the output waveform. Given a DC input voltage, V_{in}, a bipolar SPWM inverter switches between $+V_{in}$ and $-V_{in}$ as seen in Figure 3.3, whereas the unipolar SPWM switches between $+V_{in}$ and 0 V for the first half-cycle and it switches between $-V_{in}$ and 0 V for the second half-cycle as shown in Figure 3.4.

The use of the unipolar technique effectively doubles the switching harmonic position in the frequency spectrum because there are effectively two pulses in a switching window instead of one. The frequency spectrum of the the unipolar and bipolar waveforms are demonstrated in Figure 3.5 to demonstrate this effect. The unipolar technique creates less of a strain on the filter allowing for smaller inductor and capacitor values at the cost of more complicated control of the switches. The SPWM modules modelled in this section are unipolar since they lead to a reduction on the filter requirements.

The square waveforms used to develop the SPWM output are determined by using the waveforms in Figure 3.4. The first square waveform, $\boldsymbol{V}_{\mathrm{A}}(t)$, is determined by finding the intersection times between the Positive Control Signal, $C_{\mathrm{A}}(t)$, and the triangular waveform, $\boldsymbol{T}(t)$ using the following equation,

$$\boldsymbol{V}_{\mathrm{A}}(t) = \begin{cases} V_{\mathrm{in}} & \boldsymbol{T}(t) \leq C_{\mathrm{A}}(t) \\ 0 & \boldsymbol{T}(t) > C_{\mathrm{A}}(t) \end{cases} \tag{3.2}$$

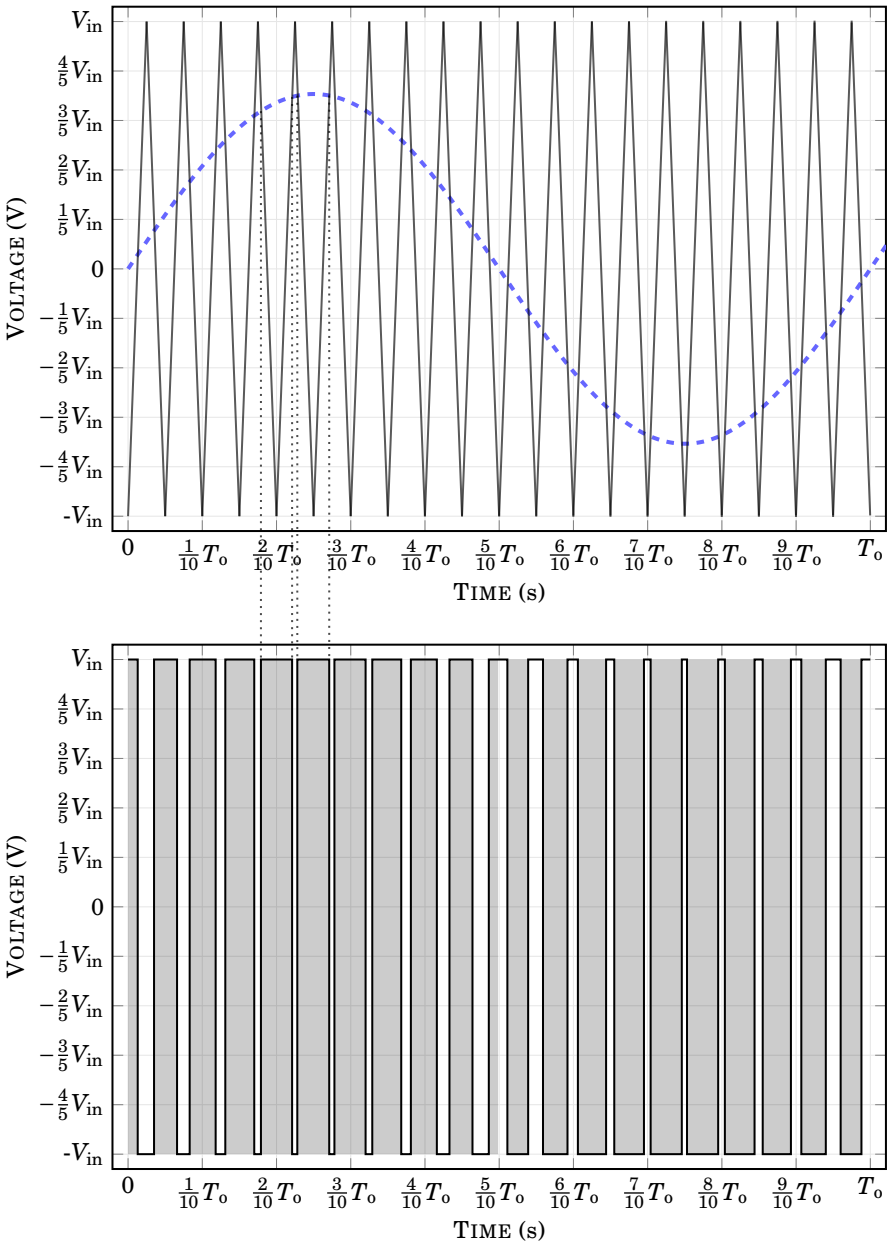


Figure 3.3: The creation of a bipolar SPWM waveform using a single control waveform and a triangular waveform. Adapted from [21].

The second square waveform, $\boldsymbol{V}_{\mathrm{B}}(t)$, is determined using the Negative Control Signal, $\boldsymbol{V}_{\mathrm{B}}(t)$, and the triangular waveform, $\boldsymbol{T}(t)$ using the following equation,

$$\boldsymbol{V}_{\mathrm{B}}(t) = \begin{cases} V_{\mathrm{in}} & \boldsymbol{T}(t) \leq C_{\mathrm{B}}(t) \\ 0 & \boldsymbol{T}(t) > C_{\mathrm{B}}(t) \end{cases} \tag{3.3}$$

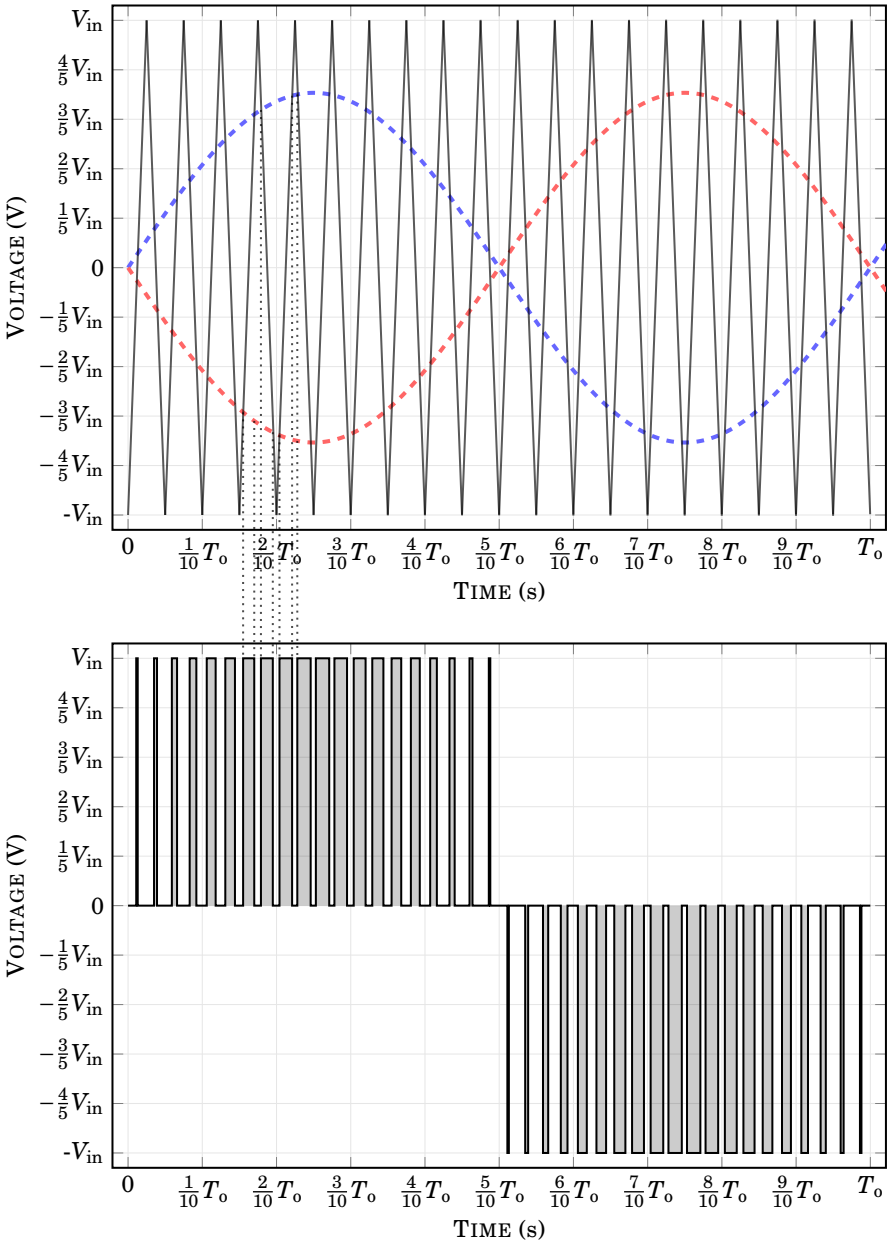
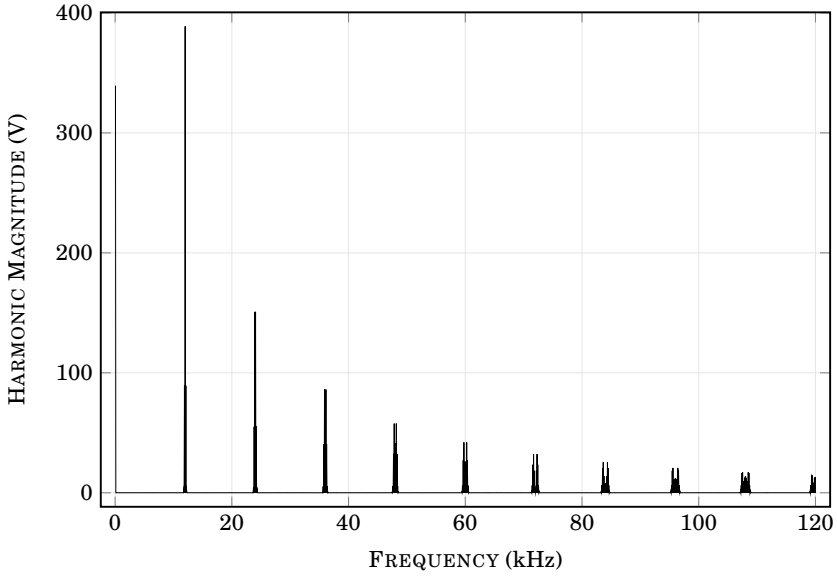
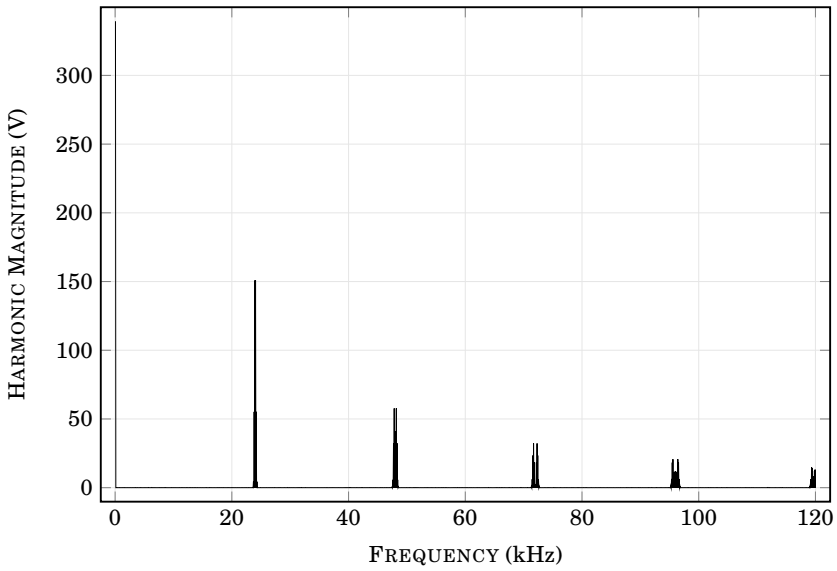


Figure 3.4: The creation of the unipolar SPWM waveform by using two control waveforms along with the triangular waveform. This modulation technique effectively doubles the switching frequency. The increase in switching frequency reduces the stress on the filter, thereby, reducing the size of the filter. Adapted from [21].



(a) Bipolar SPWM waveform frequency spectrum.



(b) Unipolar SPWM waveform frequency spectrum.

Figure 3.5: The frequency spectra of the bipolar and unipolar SPWM waveforms. In this case, $V_{\text{in}} = 450\,\text{V}$, $V_{\text{o}} = 240\,\text{V}_{\text{rms}}$, $f_{\text{o}} = 60\,\text{Hz}$, and $f_{\text{s}} = 12\,\text{kHz}$.

Finally, the SPWM waveform is created by combining Equations (3.2) and (3.3),

$$\boldsymbol{V}_{\text{out}}(t) = \boldsymbol{V}_{\text{A}}(t) - \boldsymbol{V}_{\text{B}}(t) \tag{3.4}$$

Equation (3.4) defines a continuous equation and the Fourier Series of this equation can be found. Finding the Fourier Series of this equation allows one to find the harmonics that dominate the waveform. There are two major benefits that this information provides,

1. The THD can be calculated using these harmonics.
2. The filter characteristic can be applied to these harmonics directly and the new THD can be found.

This enables the design of the filter to be based on the THD of the output waveform. This is a different technique to the conventional design method where the filter is chosen based on the output ripple. The process of finding the analytical solution in Equation (3.4) is completed in a number of steps, finding the analytical solution for Equations (3.2) and (3.3) is not simple and this process is described in Section 3.1.1.1.

3.1.1.1 Creating an Analytical SPWM Waveform

In order to calculate $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$, Equations (3.2) and (3.3), the intersection times between the control signals and the triangular waveform need to be found. The triangular wave can be generated using a piecewise model that is a combination of lines with positive and negative gradients. Given a triangular waveform of amplitude, V_{in}, and frequency, f_{s}, and the required output waveform being a sinusoid with an amplitude, $V_{\mathrm{o(p)}}$, and frequency, f_{o}, the piecewise breakdown of Figure 3.2 can be seen in Figure 3.6 below. Each line with a positive gradient as seen in Figure 3.6a, can be written in the following form,

$$\boldsymbol{T}_{\mathrm{p}}(t,k) = 4V_{\mathrm{in}}f_{\mathrm{s}}t - V_{\mathrm{in}}(4k+1), \quad k \in \mathbb{Z} \tag{3.5}$$

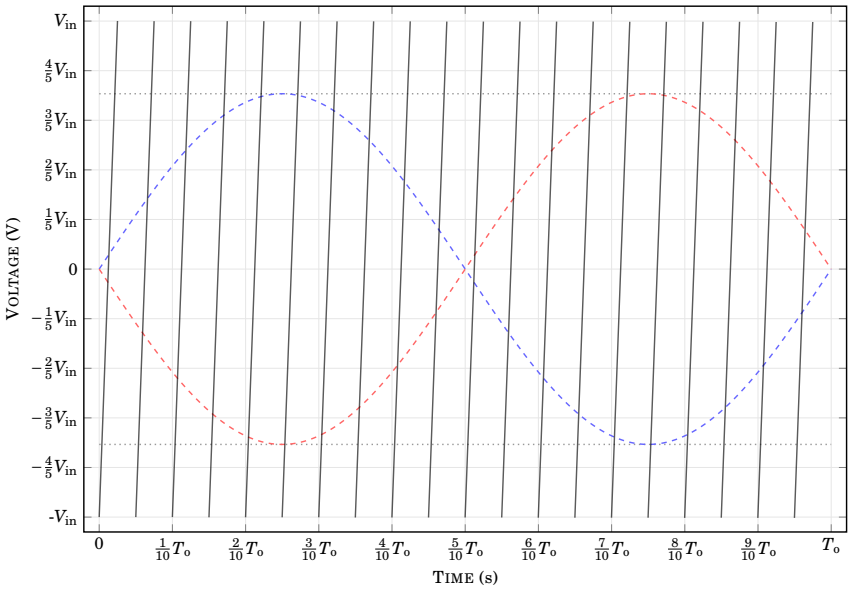
And each line with a negative gradient as seen in Figure 3.6b, can be written as,

$$\boldsymbol{T}_{\mathrm{n}}(t,k) = -4V_{\mathrm{in}}f_{\mathrm{s}}t + V_{\mathrm{in}}(3+4k), \quad k \in \mathbb{Z} \tag{3.6}$$

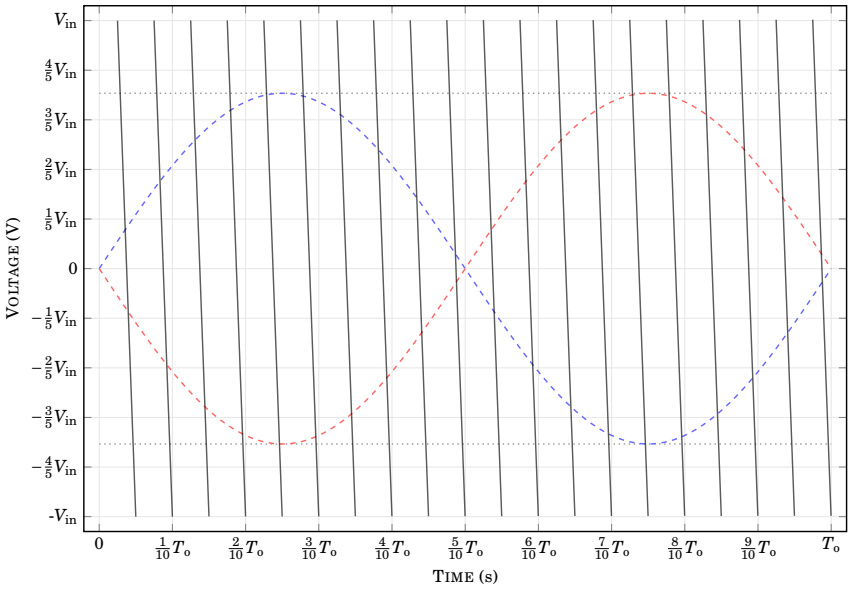
In both cases, the first line that is seen in Figures 3.6a and 3.6b is when $k = 0$. Each time k increases in Equations (3.5) and (3.6), the respective lines in Figures 3.6a and 3.6b are shifted to the right.

There is not a closed form solution to solve for the intercept points between a line and a sinusoidal waveform, since the possibilities could be infinite depending on the gradient of the line. However, in this case, the gradient is extremely high which means there is just one intercept point between each line

from the triangular waveform and the sinusoidal waveform. Kepler's Equation discussed in Appendix A demonstrates a solution that is extremely close to a closed form solution. The points of intersection are found with an error of less than 10^{-9} and are used to form $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$. As mentioned in Equation (3.4), this leads to the output SPWM signal.



(a) Positive Gradient Lines from the Triangular Waveform.



(b) Negative Gradient Lines from the Triangular Waveform.

Figure 3.6: A Piecewise Line Breakdown of the Triangular Waveform Superimposed over the Control Signals.

Once the SPWM output waveform has been established, the Fourier Series

can be used to determine the THD, this is explained in Appendix A.1. As mentioned previously, the use of the Fourier Series allows for the direct application of the filter characteristic to calculate the effect of the filter on the output THD which is discussed further in Section 3.1.1.2.

3.1.1.2 The Filter Characteristic

Figure 3.7 demonstrates the low pass filter that is used in the SPWM inverter. The filter is designed by determining a required cut-off frequency, f_c, and calculating the L and C values required to get this cut-off point. Comparing the transfer function from the LC filter in the inverter,

$$\boldsymbol{H}(s) = \frac{\frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{3.7}$$

to the generic second order filter transfer characteristic,

$$\boldsymbol{H}(s) = \frac{\omega_c^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{3.8}$$

where,

ω_c $= 2\pi f_c$, cut-off frequency;

ζ damping coefficient.

Reveals the following relationships,

$$\omega_c^2 = 4\pi^2 {f_c}^2 = \frac{1}{LC} \tag{3.9}$$

$$2\zeta\omega_c = 4\zeta\pi f_c = \frac{1}{RC} \tag{3.10}$$

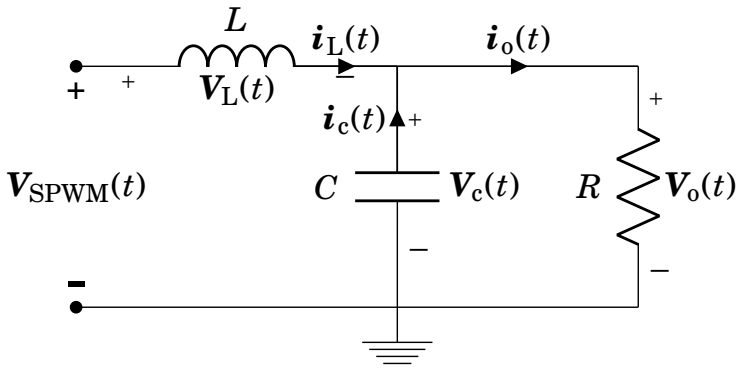


Figure 3.7: The current and voltage directions utilised in calculations used through the SPWM design.

It can be seen from Equation (3.9) that as f_c increases, the LC ratio decreases. This leads to less stress on the filter. As demonstrated in Section 2.3 the smaller L and C values reduce the volume of the filter. Equation (3.10) demonstrates that adjusting the damping coefficient, ζ, has an effect on the filter. Choosing values for f_c and ζ allows for the required L and C values to be determined,

$$C = \frac{1}{4\zeta\pi f_c R} \tag{3.11}$$

$$L = \frac{\zeta R}{\pi f_c} \tag{3.12}$$

The filter characteristic calculated using the L and C values from Equations (3.11) and (3.12) are applied to the Fourier Coefficients of the SPWM output and the Total Harmonic Distortion is calculated. It should be noted that the damping coefficient, ζ, is optimised uring this choice as it effects the volume of the filter. This optimisation is demonstrated and discussed later in this chaper in Equation (3.24). The number of coefficients used to calculate the Fourier Series is chosen to be,

$$N_c = 10\frac{f_s}{f_o} \tag{3.13}$$

where N_c is the number of coefficients used in the series. This means that the first ten harmonics of the switching frequency are included in the THD calculations. Looking at Figure 3.5b, it can be seen that these harmonics are not negligible and should be included in calculations. There are many parameters that have an effect on the THD and the filter requirements of the system and these are demonstrated in Table 3.1 below.

In order to find the SPWM inverter with the smallest volume, the filter that has the smallest volume needs to be selected, however, the filter also needs to ensure that the inverter meets design requirements for THD. In order to choose the smallest filter, all filters that allow for a THD of 5% or more are not considered and the optimization process continues. The volume of the filter is then determined using Equation (2.17) with the energy densities defined in Equations (2.22) and (2.29):

$$\begin{aligned} \boldsymbol{F}_{\text{fil}} &= \frac{1}{2W_e} C V_{\text{C(p)}}^2 + \frac{1}{2W_m} L i_{\text{L(p)}}^2 \\ &= \frac{C V_{\text{C(p)}}^2}{2(656.5 \times 10^3)} + \frac{L i_{\text{L(p)}}^2}{2(4.124 \times 10^3)} \end{aligned} \tag{3.14}$$

It can be seen from Equation (3.14) that it is still dependent on the peak voltage over the capacitor and the peak current through the inductor. The capacitor peak voltage is modelled ignoring the harmonics, in other words, it is assumed that the voltage from the capacitor is defined as,

$$\boldsymbol{V}_{\mathrm{c}}(t) = V_{\mathrm{o(p)}} \sin(2\pi f_{\mathrm{o}} t + \phi) \tag{3.15}$$

where ϕ is the phase caused by the capacitor and inductor that make up the low pass filter. Although the phase is shown in this equation, it is regarded as negligible for the approximations that follow, as these phase angles have been found to be very small and it simplifies the approximation when they are ignored.

Equation (3.15) ignores the voltage ripple and shows that the approximate peak voltage over the capacitor is $V_{\mathrm{o(p)}}$. The peak current through the inductor is modelled as the maximum current due to the 60 Hz sinusoidal output along with the ripple from the widest possible pulse width. Figure 3.8 demonstrates when the PWM signal would be on for the longest time. Since the output

Table 3.1: Parameter effects on Total Harmonic Distortion and their Effects on the Filter Specifications

Parameter	**Relationship**
V_{in}	As the input voltage increases, the SPWM signal changes because $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$ are on for shorter periods of time.
f_{s}	The switching frequency pushes the switching harmonics up as it increases because it allows for an increase in the cut-off frequency.
f_{c}	Increasing the cut-off frequency of the filter reduces the size requirements of the L and C components. This can have an adverse effect on the output waveform because frequencies below the cut-off frequency will not experience large attenuations, this means that if there are large harmonics close to the fundamental frequency, they will be seen in the output wave.
ζ	Changing the damping coefficient affects the response time of the filter and, therefore, has an effect on the harmonics. The value for the damping coefficient changes according to the THD as demonstrated in Figure 3.9.

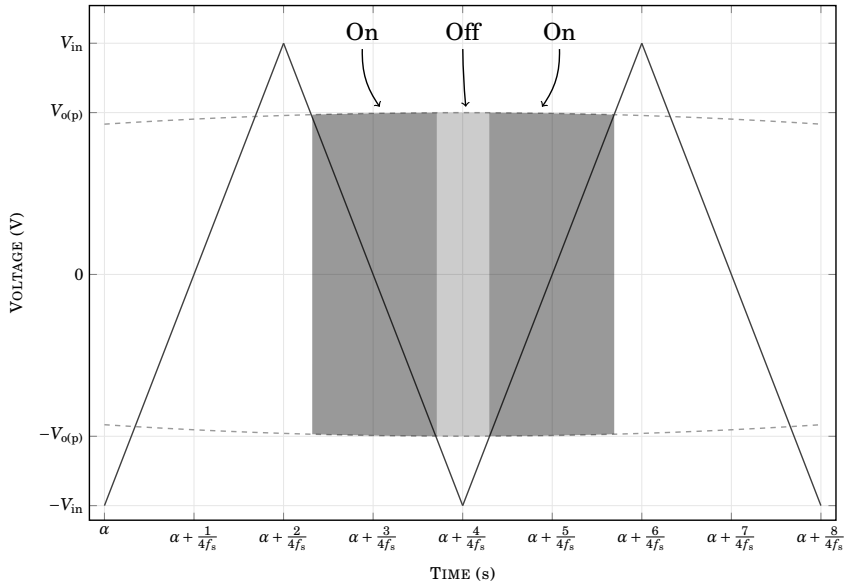


Figure 3.8: High-Frequency Triangular Waveform over the Peak of a Sinusoidal Waveform.

depends on both $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$, the longest possible time that the SPWM would be on for is when it is forming the peak output voltage. This time is related to the modulation index described in Equation (A.4) and is calculated as,

$$T_{\mathrm{on}} = \frac{m}{2f_{\mathrm{s}}} \tag{3.16}$$

As mentioned in Appendix A, the modulation index is calculated as,

$$m = \frac{V_{\mathrm{o(p)}}}{V_{\mathrm{in}}}$$

This leads to the maximum ripple current of,

$$\begin{aligned} i_{\mathrm{L(r-max)}} &= \frac{1}{L}\int_0^{\frac{m}{2f_{\mathrm{s}}}} V_{\mathrm{in}}\,dt \\ &= \frac{m}{2Lf_{\mathrm{s}}}V_{\mathrm{in}} \end{aligned} \tag{3.17}$$

Equation (3.17) demonstrates that as the switching frequency increases the ripple current decreases as expected. It also shows that the peak frequency is reliant on the input voltage, the inverse of the switching frequency and the inverse of the inductor. This means that the peak current could be decreased by increasing the switching frequency or increasing the size of the inductor.

The result of Equation (3.17) can now be added to the peak sinusoidal current through the resistor. The current through the inductor can be calculated using Kirchoff's Current Law, the current directions are presented in Figure 3.7,

$$\begin{aligned}\boldsymbol{i}_{\mathrm{L}}(t) &= \boldsymbol{i}_{\mathrm{o}}(t) - \boldsymbol{i}_{\mathrm{c}}(t) \\ &= \frac{V_{\mathrm{o(p)}}}{R}\sin(2\pi f_{\mathrm{o}}t) - C\frac{d}{dt}\left(V_{\mathrm{o(p)}}\sin(2\pi f_{\mathrm{o}}t)\right) \\ &= \frac{V_{\mathrm{o(p)}}}{R}\sin(2\pi f_{\mathrm{o}}t) - 2\pi f_{\mathrm{o}}CV_{\mathrm{o(p)}}\cos(2\pi f_{\mathrm{o}}t)\end{aligned} \tag{3.18}$$

From this equation, the peak current is calculated by finding the turning points by setting the derivative to zero,

$$\frac{\mathrm{d}\boldsymbol{i}_{\mathrm{L}}(t)}{\mathrm{d}t} = \frac{V_{\mathrm{o(p)}}}{R}2\pi f_{\mathrm{o}}\cos(2\pi f_{\mathrm{o}}t) + CV_{\mathrm{o(p)}}(2\pi f_{\mathrm{o}})^2\sin(2\pi f_{\mathrm{o}}t) \tag{3.19}$$

This leads to the following,

$$\begin{aligned}0 &= \frac{V_{\mathrm{o(p)}}}{R}2\pi f_{\mathrm{o}}\cos(2\pi f_{\mathrm{o}}t_{\mathrm{L(peak)}}) + CV_{\mathrm{o(p)}}(2\pi f_{\mathrm{o}})^2\sin(2\pi f_{\mathrm{o}}t_{\mathrm{L(peak)}}) \\ t_{\mathrm{L(peak)}} &= \frac{1}{2\pi f_{\mathrm{o}}}\arctan\left(\frac{-1}{2\pi f_{\mathrm{o}}RC}\right)\end{aligned}$$

Which leads to the peak sinusoidal current through the inductor,

$$\begin{aligned}I_{\mathrm{L(p-sine)}} &= \left|\boldsymbol{i}_{\mathrm{L}}(t_{\mathrm{L(peak)}})\right| \\ &= \left|\frac{V_{\mathrm{o(p)}}}{R}\sin\left(2\pi f_{\mathrm{o}}\frac{1}{2\pi f_{\mathrm{o}}}\arctan\left(\frac{-1}{2\pi f_{\mathrm{o}}RC}\right)\right)\right. \\ &\qquad \left. - 2\pi f_{\mathrm{o}}CV_{\mathrm{o(p)}}\cos\left(2\pi f_{\mathrm{o}}\frac{1}{2\pi f_{\mathrm{o}}}\arctan\left(\frac{-1}{2\pi f_{\mathrm{o}}RC}\right)\right)\right| \\ &= \frac{V_{\mathrm{o(p)}}}{R}\sqrt{1+\left(2\pi f_{\mathrm{o}}RC\right)^2}\end{aligned} \tag{3.20}$$

The peak current through the inductor is the combination of Equations (3.17) and (3.20) defined as,

$$\begin{aligned}i_{\mathrm{L(p)}} &= I_{\mathrm{L(p-sine)}} + i_{\mathrm{L(r-max)}} \\ &= \frac{V_{\mathrm{o(p)}}}{R}\sqrt{1+\left(2\pi f_{\mathrm{o}}RC\right)^2} + \frac{m}{2Lf_{\mathrm{s}}}V_{\mathrm{in}}\end{aligned} \tag{3.21}$$

The ripple current is calculated as the worst case scenario. It is unlikely for the current through the inductor to reach this value, however, it is possible

if the peak output voltage is equal to the input voltage demonstrated in Figure 3.8.

The final equation for approximating the volume of the filter is a combination of Equations (2.17), (2.22), (2.29), (3.15) and (3.21). Equation (2.17) is used as the basis for this approximation,

$$F_{\text{vol}} = \frac{1}{2W_{\text{e}}} C V_{\text{C(p)}}^2 + \frac{1}{2W_{\text{m}}} L I_{\text{L(p)}}^2$$

The values for $W_{\text{e}} = 656.5\,\text{kJ}\,\text{m}^{-3}$ and $W_{\text{m}} \approx 56.03\,\text{kJ}\,\text{m}^{-3}$ are taken from Equations (2.22) and (2.29). Finally, the peak values $V_{\text{C(p)}}$ and $I_{\text{L(p)}}$ are found using Equations (3.15) and (3.21) respectively. These substitutions lead to the formula used to approximate the volume of the filter as follows,

$$\boldsymbol{F}_{\text{fil}}(L, C, f_{\text{s}}, V_{\text{in}}) = \frac{C}{2} \frac{m^2 {V_{\text{in}}}^2}{W_{\text{e}}} + \frac{L}{2} \frac{\left(\frac{V_{\text{o(p)}}}{R} \sqrt{1 + \left(2\pi f_{\text{o}} R C\right)^2} + \frac{m}{2 L f_{\text{s}}} V_{\text{in}} \right)^2}{W_{\text{m}}} \tag{3.22}$$

Substituting Equations (3.11) and (3.12) into Equation (3.22) above shows the relationship with respect to the damping and the cut-off frequency. These values directly affect the volume in the following way,

$$\boldsymbol{F}_{\text{fil}}(\zeta, f_{\text{c}}, f_{\text{s}}, V_{\text{in}}) = \frac{1}{8\zeta\pi f_{\text{c}} R} \frac{m^2 {V_{\text{in}}}^2}{W_{\text{e}}} + \frac{\zeta R}{2\pi f_{\text{c}}} \frac{\left(\frac{V_{\text{o(p)}}}{R} \sqrt{1 + \left(\frac{f_{\text{o}}}{2\zeta f_{\text{c}}}\right)^2} + \frac{\pi m f_{\text{c}}}{2\zeta R f_{\text{s}}} V_{\text{in}} \right)^2}{W_{\text{m}}} \tag{3.23}$$

The local minimum of this equation is found with the following derivative,

$$\frac{\partial}{\partial \zeta} \boldsymbol{F}_{\text{vol}}(\zeta, f_{\text{c}}, f_{\text{s}}, V_{\text{in}}) = 0 \tag{3.24}$$

As described in Section 2.6.2, the load resistance is kept at a constant purely resistive value of 28.8 Ω. Since f_{s} and V_{in} are specified, only f_{c} is unknown in Equation (3.24) and the ζ that leads to the smallest volume (while still meeting the THD requirements), ζ^*, can be defined in terms of f_{c}. From Equation (3.23) it can be seen that the volume is non-linearly dependent on the cut-off frequency. As the cut-off frequency becomes very small or very large, the volume increases. This is found by looking at the powers of f_{c} in the numerator and the denominator. In the first term of Equation (3.23) there is $\frac{1}{f_{\text{c}}}$ and in the second term there is $\frac{f_{\text{c}}}{1}$. Ideally the cut-off frequency would be chosen to lead to the lowest volume, however, the THD could be higher

than 5% in this case. This means that not all values of ζ and f_c lead to a viable solution. It is possible to solve for the value of ζ^* in terms of f_c using Equation (3.24). However, the solution is extremely long and complicated and, although it works, it is less complicated to find the optimal point numerically using the following process,

1. Create a vector of ζ values.
2. Find the cut-off frequencies, f_c, that lead to a THD that meets the requirement.
3. Calculate the volumes of each option that meets the requirement and choose the value of ζ that leads to the smallest volume.

In its entirety, the process followed to find the optimal volume of the low pass filter used in a unipolar SPWM is defined below and is demonstrated visually in Figure 3.9.

1. Simulate the SPWM waveform based on the input voltage and switching frequency.
2. Find the Fourier Series of this waveform and ensure that the final harmonic is at a frequency greater than ten times that of the switching frequency, as mentioned in Equation (3.13).
3. Choose the lower and upper bounds for the cut-off frequency of the filter. Initially, these are chosen to be f_o and f_s respectively.
4. Set the cut-off frequency to the value between the upper and lower bounds.
5. Choose the damping coefficient, ζ, that leads to the smallest volume based using Equation (3.24).
6. Calculate the L and C values using Equation (3.11) and Equation (3.12).
7. Find the transfer characteristic of the filter and apply it to each harmonic amplitude.
8. Calculate the THD of output waveform using the following equation,

$$\text{THD} = \frac{1}{V_1}\sqrt{\sum_{i=2}^{N} V_i^2} \tag{3.25}$$

where V_i is the magnitude of the amplitudes of each harmonic in the Fourier Series.

9. See if the THD of the current SPWM inverter is larger than 5%, if that is the case, move the upper bound to the current cut-off frequency. If the THD is less than 5% then set the lower bound to the current cut-off frequency. If the THD is 5% then the correct cut-off frequency has been found, the volume is chosen as the ideal SPWM volume for the current input parameters and the process ends. Otherwise, the process is repeated from Step 4.

The work in this section outlines the process to follow to find the optimal volume of a low pass filter for a unipolar SPWM inverter. The model is parameterised which means that the input and output voltages may be varied provided that $m < 1$. The parameterised model gives a valid approximation provided that $f_\text{s} \gg f_\text{o}$. If this is not the case, the amplitude of the fundamental frequency does not reach f_o meaning that the THD adheres to the specifications but the output amplitude does not. This effect is seen and discussed in Section 3.5.

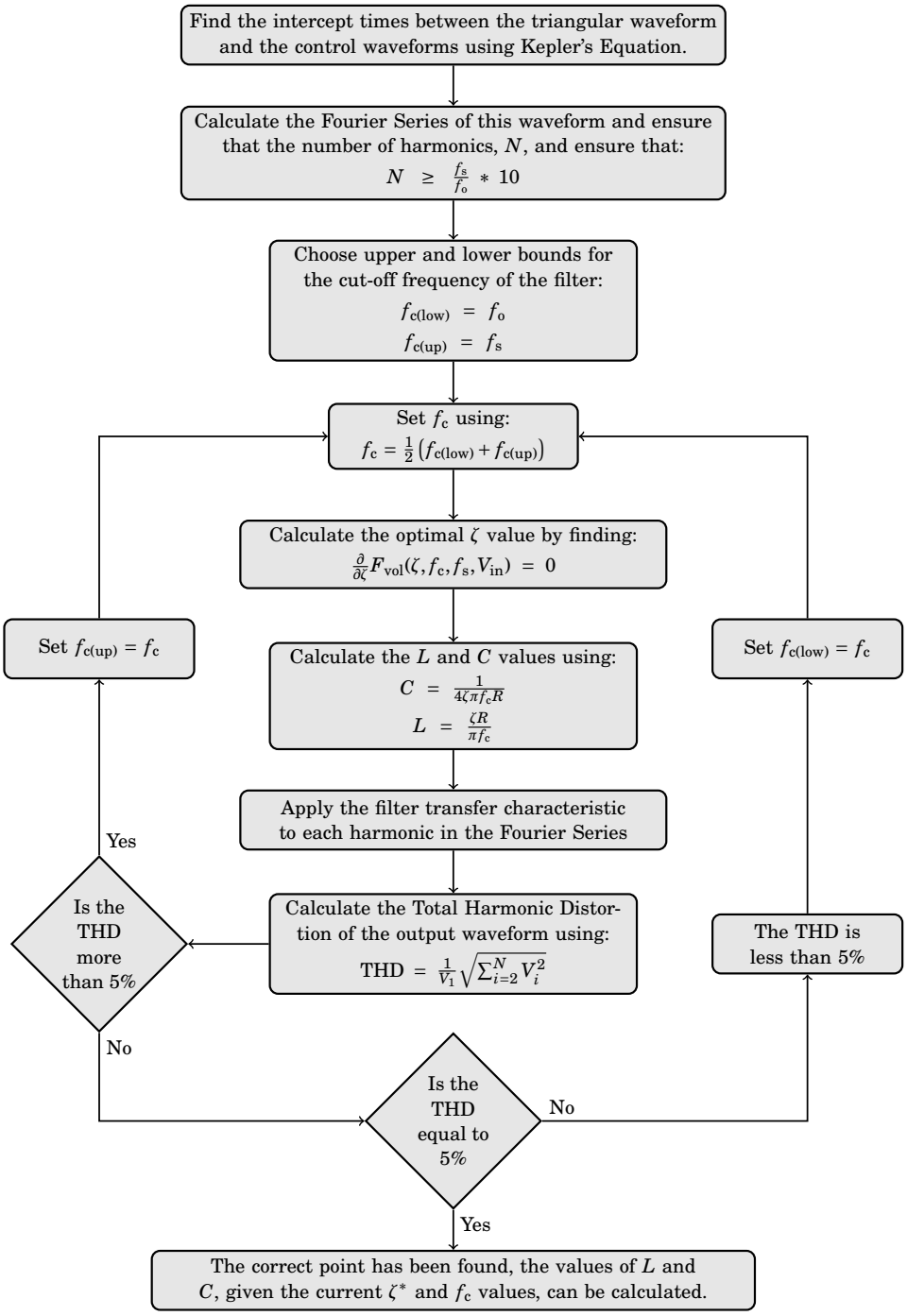


Figure 3.9: The flow diagram of the process used to find the optimal filter specification for an SPWM input waveform.

3.2 Loss Model

The non-ideal effects of the switches add to the losses of the SPWM inverter. The following losses are taken into account in the model,

- Switching losses, P_{sw}.
- Reverse recovery of the body diode, P_{rr}.
- Conduction losses, P_{con}.

The equation that describes the total loss approximation in the circuit is defined as follows,

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{con}} + P_{\text{rr}} \tag{3.26}$$

3.2.1 Current Flow Realisation

There are two conduction paths used in this SPWM and they are demonstrated in Figure 3.10. This naming convention is used throughout this section.

The modulation technique used to create the unipolar SPWM waveform is described in Figure 3.11 below. This figure is referred to during the calculation of the SPWM current waveforms. The naming convention is used when describing the switching and conduction losses throughout this chapter.

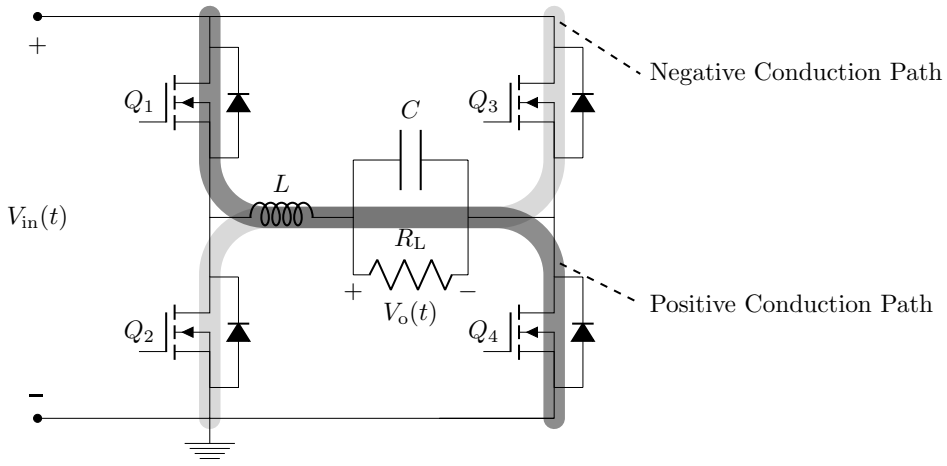
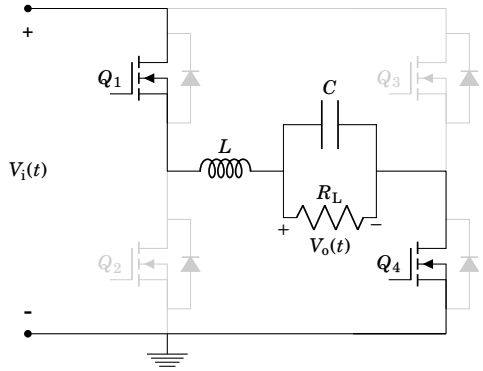
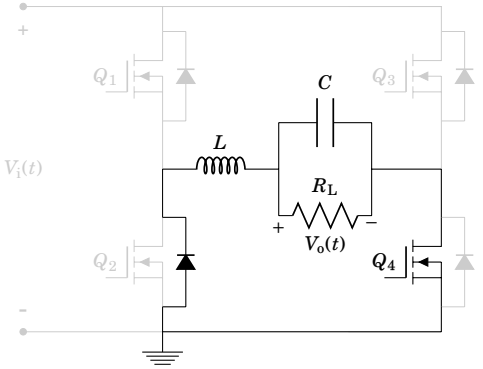


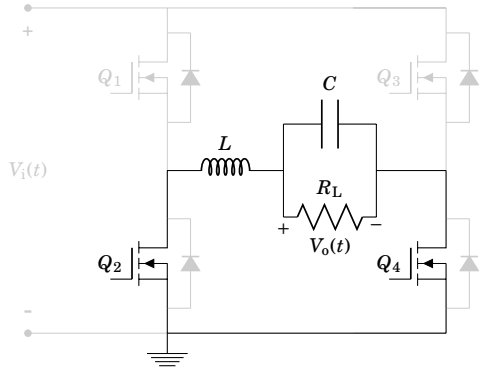
Figure 3.10: The naming of the arms and switches in the SPWM circuit.



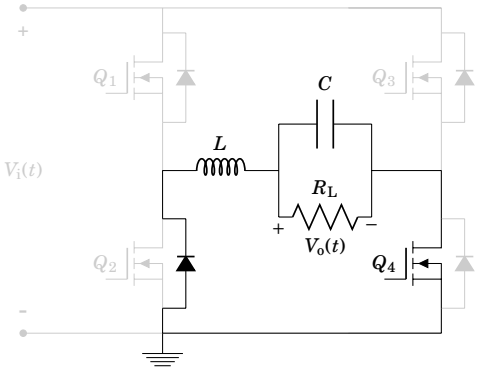
(a) The positive conduction path is conducting and current flows through the inductive load.



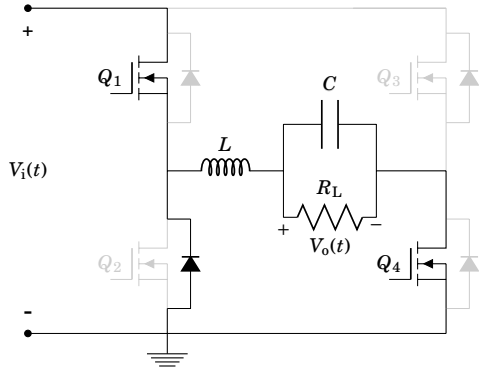
(b) The top switch of the positive conduction path, Q_1, switches off but the bottom switch, Q_4, is kept on. The inductor forces current to flow through the body diode of Q_2.



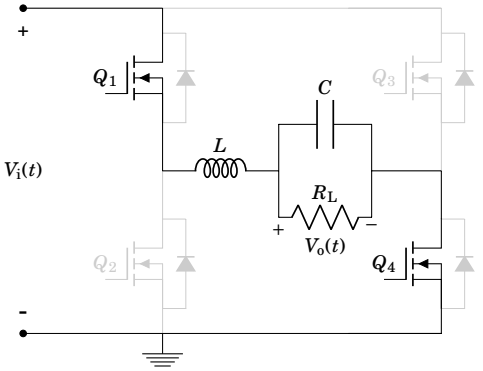
(c) Q_2 is turned on after the diode is forced to turn on, this prevents shoot-through by turning Q_2 on before Q_1 is fully turned off.



(d) Before Q_1 is turned on, Q_2 is turned off and the body diode of Q_2 begins to conduct again.



(e) Q_1 is turned on, but since the body diode of Q_2 is conducting, an effective path to ground is created. Current rushes through Q_1 and Q_2 and this continues until the minority charge in the body diode of Q_2 is depleted.



(f) Once the minority charge in the body diode of Q_2 is depleted, the diode switches off, leaving the positive conduction path conducting.

Figure 3.11: The method used to create the unipolar SPWM waveform by controlling the conduction paths throughout the switching cycle.

3.2.2 Switching Losses

By parameterising characteristics of the switch, a model has been made to approximate the switching loss. The rise and fall rates of the voltage drop across the switch are defined as $\frac{\mathrm{d}V_{\mathrm{sw}}}{\mathrm{d}t}$. The rise and fall rates of the current passing through the switch are defined as $\frac{\mathrm{d}I_{\mathrm{sw}}}{\mathrm{d}t}$. These rates are assumed to be the same magnitude in both directions, therefore, in mathematical terms:

$$\frac{\mathrm{d}V_{\mathrm{sw}}}{\mathrm{d}t} = \frac{\mathrm{d}V_{\mathrm{sw-rise}}}{\mathrm{d}t} = \left|\frac{\mathrm{d}V_{\mathrm{sw-fall}}}{\mathrm{d}t}\right| \tag{3.27}$$

$$\frac{\mathrm{d}I_{\mathrm{sw}}}{\mathrm{d}t} = \frac{\mathrm{d}I_{\mathrm{sw-rise}}}{\mathrm{d}t} = \left|\frac{\mathrm{d}I_{\mathrm{sw-fall}}}{\mathrm{d}t}\right| \tag{3.28}$$

Rates are used as opposed to rise and fall times as they simplify the mathematics and the approximation process when simulations are run. The rate is measured in the simulation and used to approximate the switching times of the MOSFET.

Utilising an SPWM waveform, the current through the switch changes over time, however, the voltage over the switch remains constant at V_{in}. In order to model the effects of the sinusoidal behaviour accurately, the inductor voltage and currents are modelled using the SPWM waveform in Equation (A.22). In this case, the switch current, $\boldsymbol{I}_{\mathrm{L}}(t)$, is defined using the following approximation,

$$\boldsymbol{V}_{\mathrm{L}}(t) = \boldsymbol{V}_{\mathrm{SPWM}}(t) - V_{\mathrm{o(p)}}\sin(2\pi f_{\mathrm{o}}t + \phi) \tag{3.29}$$

$$\boldsymbol{I}_{\mathrm{L}}(t) = \frac{1}{L}\int_0^t \boldsymbol{V}_{\mathrm{L}}(t)\,\mathrm{d}t \tag{3.30}$$

Switching events take place at discrete times throughout the output waveform period. Provided that $m < 1$, there will be two pulses in each switching cycle which is demonstrated in Figures 3.8 and 3.12. This means that the loss over each switching cycle for Q_1 or Q_3 is,

$$\boldsymbol{W}_{\mathrm{sw}}(k) = \boldsymbol{W}_{\mathrm{on}}(k) + \boldsymbol{W}_{\mathrm{off}}\left(\frac{4k+1}{4}\right) + \boldsymbol{W}_{\mathrm{on}}\left(\frac{4k+2}{4}\right) + \boldsymbol{W}_{\mathrm{off}}\left(\frac{4k+3}{4}\right) \tag{3.31}$$

Where k represents a switching event, $k = 0, \cdots, \frac{f_{sw}}{f_o}$ and $\boldsymbol{I}_{sw}(k)$ is the approximation of the current flowing through the switch at a given switching event and is approximated using,

$$\boldsymbol{I}_{sw}(k) = \boldsymbol{I}_L\left(\frac{k}{f_{sw}}\right) \tag{3.32}$$

As seen in Equation (3.31), four switching events that take place over one switching cycle. The values being sent into $\boldsymbol{W}_{on}(k)$ and $\boldsymbol{W}_{off}(k)$ are, $0, \frac{1}{4}, \frac{2}{4}, \frac{3}{4}, \cdots, \frac{f_{sw}}{f_o}$. One switching event happens relatively close to the start of the switching cycle, two close to the middle, and one close to the end (see Figure 3.12 for a simplified visual demonstration). The current that appears in $\boldsymbol{I}_L(t)$ changes from a minimum at the start of the switching cycle to a maximum at the end of the switching cycle (or from a maximum to a minimum if the overall sinusoidal current is decreasing). Using k, the switching events are taken as quarterly events which approximates this move from the minimum to the maximum current in a single cycle.

The switching loss incurred by the switch-off and switch-on events, $\boldsymbol{W}_{off}(k)$ and $\boldsymbol{W}_{on}(k)$, are derived in Sections 3.2.2.1 and 3.2.2.2 below.

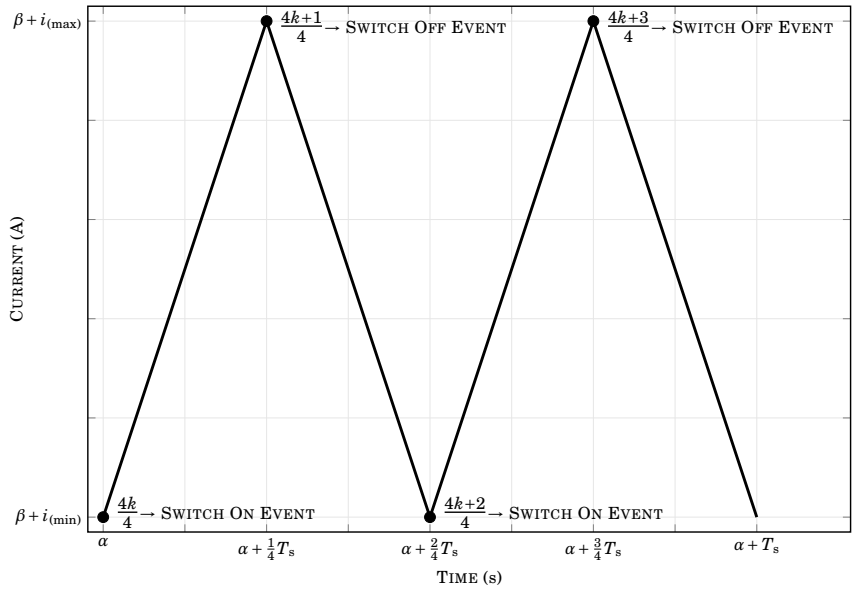


Figure 3.12: The four switching events that take place over each switching period, T_s. This is a simplified model where the current average remains the same between the start and end of the period. In reality, the current slightly increases or decreases over this period as it is being modulated to form a sinusoidal current.

3.2.2.1 MOSFET Switching Off Event

The switching loss is calculated based on a clamped inductive load model. In this case, when turning off a switch, the clamping diode's bias must reach 0 V before the current through the switch begins to decrease. The voltage across the switch increases linearly from 0 V to V_{sw}. For the SPWM, the voltage across the switch when it is off is V_{in}. It is assumed that the current through the inductor remains constant over this period of time due to the speed of this switching event. These approximate waveforms are demonstrated in Figure 3.13 below [35].

The time taken for the voltage over the switch to increase from 0 V to V_{in} is calculated as,

$$\Delta t_{\text{off-v}} = \frac{V_{\text{in}}}{\frac{\mathrm{d}V_{\text{sw}}}{\mathrm{d}t}} \tag{3.33}$$

Leading to the energy loss over this period calculated as a triangle with a base of $\Delta t_{\text{off-v}}$ and a height of $\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}}$ since it is assumed that $\boldsymbol{I}_{\text{sw}}(k)$ stays constant over this short period of time.

$$\begin{aligned} \boldsymbol{W}_{\text{off-v}}(k) &= \frac{1}{2}\Delta t_{\text{off-v}}\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}} \\ &= \frac{1}{2}\frac{\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}}^2}{\frac{\mathrm{d}V_{\text{sw}}}{\mathrm{d}t}} \end{aligned} \tag{3.34}$$

Once the voltage reaches V_{in}, the diode becomes forward biased and allows current to flow. The current through the switch linearly decreases to 0 A. The time taken for this is transition is calculated using,

$$\Delta t_{\text{off-i}} = \frac{\boldsymbol{I}_{\text{sw}}(k)}{\frac{\mathrm{d}I_{\text{sw}}}{\mathrm{d}t}} \tag{3.35}$$

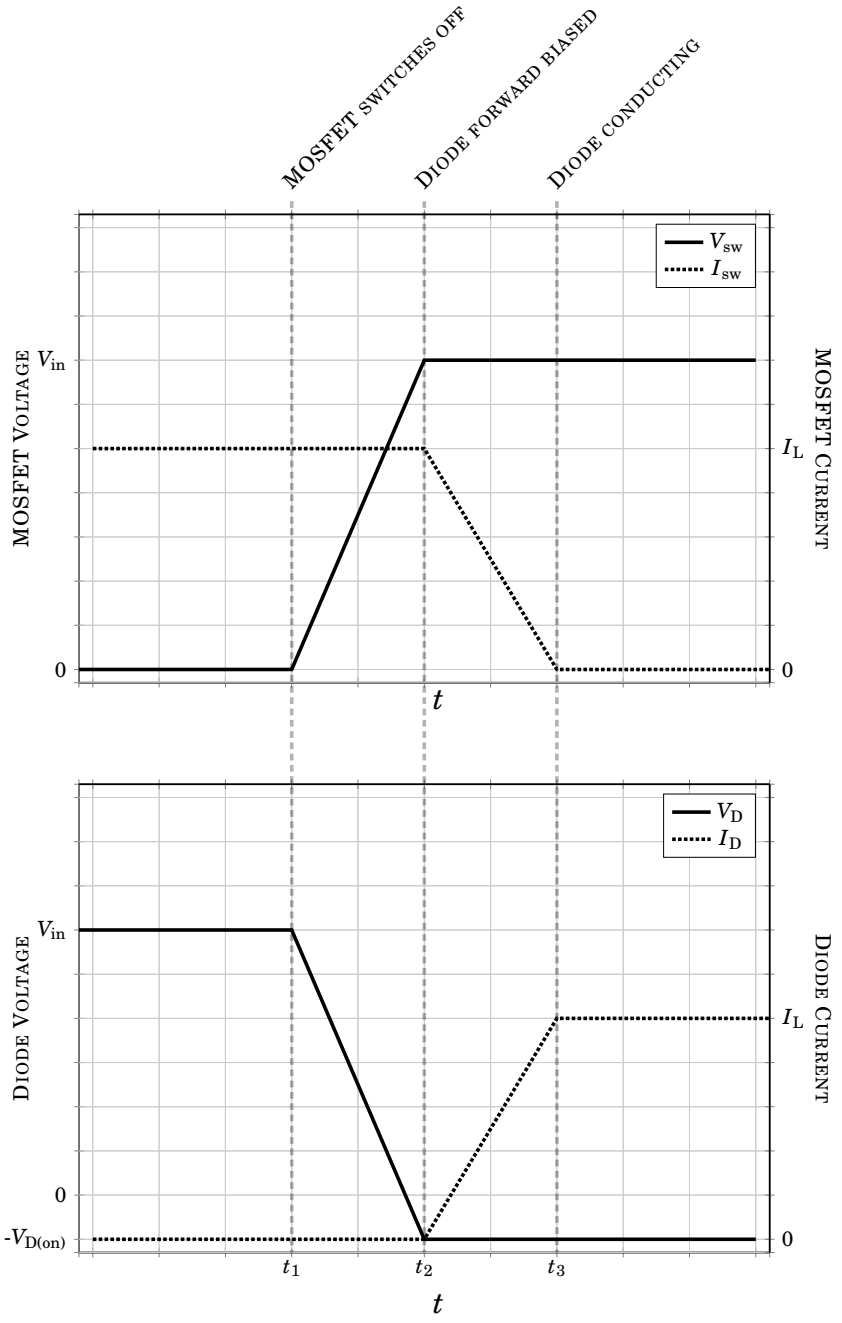


Figure 3.13: The current and voltage waveforms over the top switch of a phase arm of the SPWM as well as the body diode of the switch beneath it. These waveforms demonstrate when the top switch in the phase arm is turning off. The body diode from the switch below first becomes forward biased before conducting current. Adapted from [35].

In much the same way as the voltage change, the energy loss during this transition is calculated as,

$$\begin{aligned} \boldsymbol{W}_{\text{off-i}}(k) &= \frac{1}{2}\Delta t_{\text{off-i}}\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}} \\ &= \frac{1}{2}\frac{V_{\text{in}}\boldsymbol{I}_{\text{sw}}{}^2(k)}{\frac{\mathrm{d}I_{\text{sw}}}{\mathrm{d}t}} \end{aligned} \tag{3.36}$$

This leads to the total energy loss over the event of the switch turning off to be calculated as,

$$\begin{aligned} \boldsymbol{W}_{\text{off}}(k) &= \boldsymbol{W}_{\text{off-v}}(k) + \boldsymbol{W}_{\text{off-i}}(k) \\ &= \frac{1}{2}\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}}\left(\frac{V_{\text{in}}}{\frac{\mathrm{d}V_{\text{sw}}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}(k)}{\frac{\mathrm{d}I_{\text{sw}}}{\mathrm{d}t}}\right) \end{aligned} \tag{3.37}$$

3.2.2.2 MOSFET Switching On Event

When the top switch of either phase arm turns on, reverse recovery losses occur. This is because the body diode of the bottom switch in the opposing phase arm is conducting. When the switch above it turns on, a temporary path between the input source and ground is created. This creates a rush of current through the body diode and this current is blocked once the minority charge carriers have been removed. Figure 3.11 demonstrates the conduction loops that exist over a switching cycle and Figure 3.14 demonstrates the switching waveforms during reverse recovery.

There are two major stages, the first is a rush of current through the diode until it reaches its peak reverse recovery current, I_{rr}. The second is the return from the peak reverse recovery current to 0A. In most cases, the reverse recovery charge, Q_{rr}, is provided for the MOSFET in the datasheet. The reverse recovery time, t_{rr}, is defined as the time between intervals t_2 and t_4 in Figure 3.14 which is a simplified approximation of the reverse recovery waveform. The loss through the switch turning on during this switching event can be approximated as [35],

$$\boldsymbol{W}_{\text{on}}(k) = V_{\text{in}}\boldsymbol{I}_{\text{sw}}(k)t_{\text{rr}} + V_{\text{in}}Q_{\text{rr}} \tag{3.38}$$

The loss through the diode during the reverse recovery is regarded as negligible since the voltage over the diode effectively starts at 0 V and ends at V_{in}.

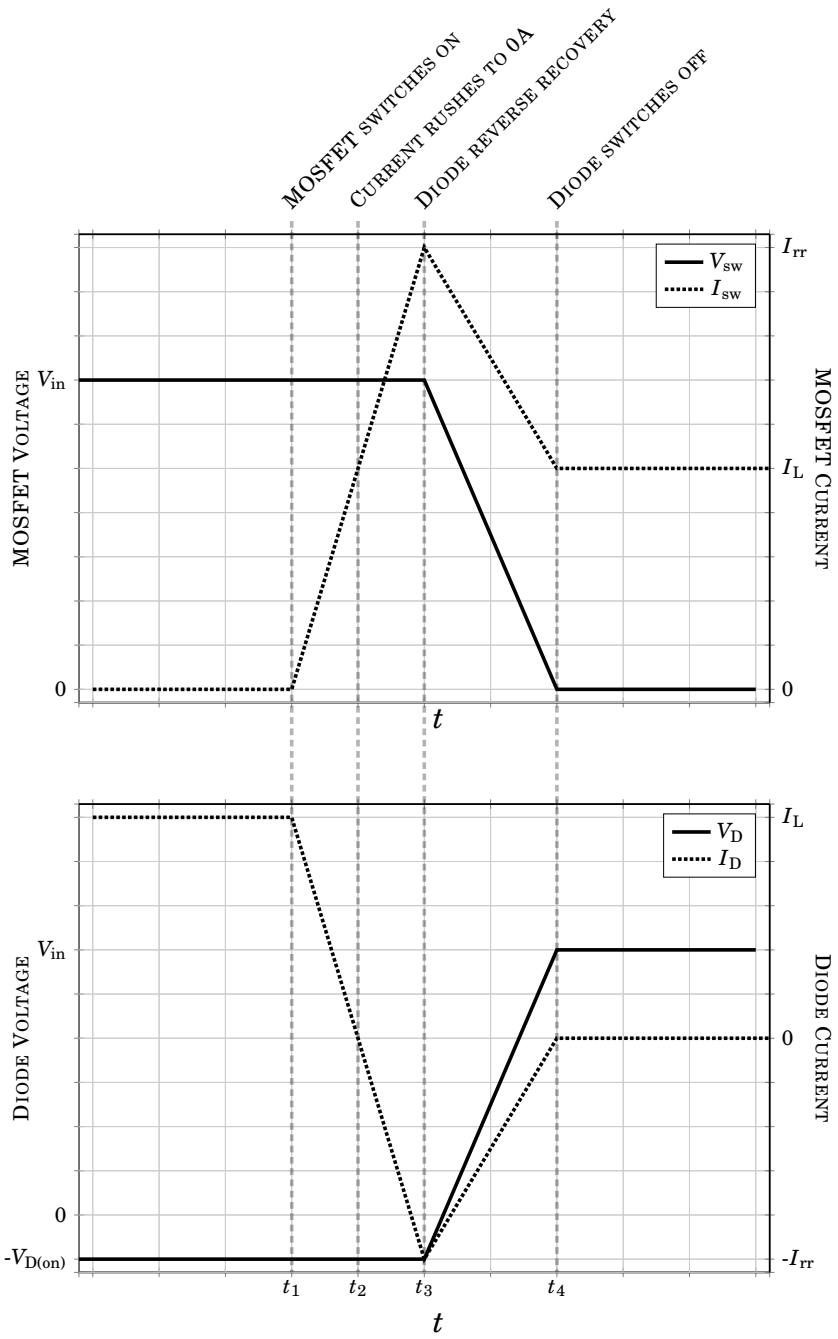


Figure 3.14: The losses incurred when turning on the MOSFET in the SPWM. The diode from the switch below the MOSFET turns off, however, there is an influx of current due to the reverse recovery of the diode which is demonstrated in this figure. I_{rr} is the peak reverse recovery current reached and $V_{\text{D(on)}}$ is the on voltage of the body diode.

3.2.3 Conduction Losses

As mentioned in Section 3.2.2, the current through the switches can be approximated using the following formula,

$$\boldsymbol{I}_{\mathrm{L}}(t) = \frac{1}{L}\int_0^t (\boldsymbol{V}_{\mathrm{SPWM}}(t) - V_{\mathrm{o(p)}}\sin(2\pi f_{\mathrm{o}} t + \phi))\,\mathrm{d}t$$

Due to symmetry, the conduction losses over a half-cycle can be calculated in order to calculate the total conduction losses. As seen in Figure 3.11, Q_4 is always conducting over a half-cycle, the conduction loss due to Q_4 is calculated as,

$$P_{\mathrm{con}} = \frac{2}{T_{\mathrm{o}}}\int_0^{\frac{T_{\mathrm{o}}}{2}} \boldsymbol{I}_{\mathrm{L}}{}^2(t) r_{\mathrm{on}}\,\mathrm{d}t \tag{3.39}$$

Conduction alternates between Q_1 and Q_4 and the loss due to these two switches is not as simple as Equation (3.39). The two switches alternate in conduction, this is demonstrated in Figures 3.11a, 3.11c and 3.11d. Section 3.2.3.1 discusses the change in conduction loss when the current through the MOSFET is reversed. The two switches have the following behaviours,

- Q_1 acts as a small resistor and the voltage drop over it is defined in Equation (3.43).
- Q_2 acts as a small resistor until the current through it causes the voltage across it to grow to the on voltage of the body diode, $V_{\mathrm{D(on)}}$. At this point the voltage saturates at around $V_{\mathrm{D(on)}}$. Section 3.2.3.1 discusses this effect in detail and defines the voltage characteristic across Q_2.

In order to model this loss, the following functions are needed,

$$\boldsymbol{U}_{\boldsymbol{Q_1}}(t) = \frac{\boldsymbol{V}_{\mathrm{SPWM}}(t)}{V_{\mathrm{in}}}\boldsymbol{I}_{\mathrm{L}}(t) \tag{3.40}$$

$$\boldsymbol{U}_{\boldsymbol{Q_4}}(t) = 1 - \boldsymbol{U}_{\boldsymbol{Q_1}}(t) \tag{3.41}$$

The $\frac{\boldsymbol{V}_{\mathrm{SPWM}}(t)}{V_{\mathrm{in}}}$ in Equation (3.40) acts as a sequence of unit steps that hold the value of 1 when Q_1 is conducting and 0 when it is not. Equation (3.41) is just the opposite of Equation (3.40). These two equations represent when Q_1 is on and when Q_2 is on respectively.

The conduction loss due to these two switches is the sum of the conduction losses contributed by each of them when they are on,

$$P_{\text{rcon}} = \frac{2}{T_{\text{o}}} \int_0^{\frac{T_{\text{o}}}{2}} \left(\boldsymbol{V}_{\text{sw(f)}}\left(\boldsymbol{I}_{\text{L}}(t)\right) \boldsymbol{I}_{\text{L}}(t) \boldsymbol{U}_{\boldsymbol{Q_1}}(t) + \boldsymbol{V}_{\text{sw(r)}}\left(\boldsymbol{I}_{\text{L}}(t)\right) \boldsymbol{I}_{\text{L}}(t) \boldsymbol{U}_{\boldsymbol{Q_4}}(t) \right) \mathrm{d}t \quad (3.42)$$

3.2.3.1 Model For Reverse Current Through MOSFET

Current is able to travel in both directions through the MOSFET. When current is flowing from the drain to the source, the voltage developed over the MOSFET is simply,

$$\boldsymbol{V}_{\text{sw(f)}}\left(I_{\text{sw}}\right) = I_{\text{sw}} r_{\text{on}} \quad (3.43)$$

Where $\boldsymbol{V}_{\text{sw(f)}}$ is the voltage across the switch when the current is moving in the the "forward" direction, in other words, when the current is flowing from the drain to the source. However, in the reverse direction, the body diode plays a role. As soon as the voltage in Equation (3.43) increases to the on-voltage of the body diode, the diode turns on and limits the voltage drop across the MOSFET. In this case,

$$\boldsymbol{V}_{\text{sw(r)}}\left(I_{\text{sw}}\right) = \begin{cases} I_{\text{sw}} r_{\text{on}}, & I_{\text{sw}} r_{\text{on}} < V_{\text{D(on)}} \\ V_{\text{D(on)}}, & I_{\text{sw}} r_{\text{on}} \geq V_{\text{D(on)}} \end{cases} \quad (3.44)$$

Where $\boldsymbol{V}_{\text{sw(r)}}$ is the voltage over the switch when the current is moving in the "reverse" direction, in other words, the current is moving from the source to the drain. Figure 3.15 demonstrates Equation (3.44) visually. This effect wouldn't be seen as much in low voltage blocking MOSFETs since they have a very low on-resistance and it would take a large current to get the voltage to be similar to the turn-on voltage of the body diode. When it comes to high voltage blocking MOSFETs such as the IRFP460 that is used in this research, the on-resistance is relatively high and a smaller current can lead to the body diode turning on.

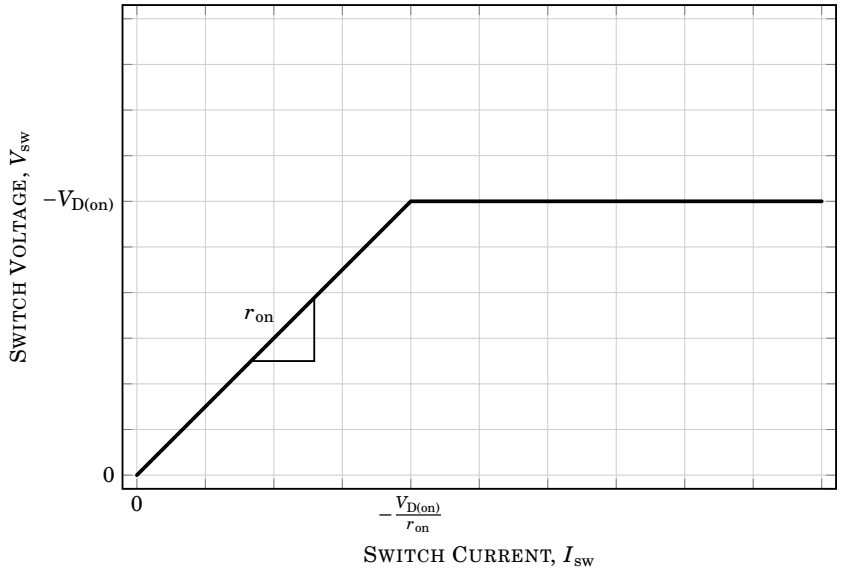


Figure 3.15: The voltage and current characteristic of a MOSFET when the current is flowing from the source to the drain. The MOSFET can no longer be modelled as a small resistor, its voltage drop is capped by the body diode.

3.2.4 Combined Loss Model Approximation

By combining the switching losses, along with the reverse recovery loss, the total switching losses for MOSFET switches are found. The SPWM waveform is symmetric over each half-cycle of the output waveform. The only change is from V_{in} to $-V_{in}$ as the output amplitude, Figure 3.4 demonstrates this symmetry and magnitude. This means that the power losses over half of the output period, T_o, is the same as the power loss over the whole output period. In this section, calculations are performed over a half period, $\frac{T_o}{2}$.

Q_4 is on for the entire half-cycle. The loss incurred by this switch is simply the conduction loss for this period of time,

$$P_{Q_4} = \frac{2}{T_o}\int_0^{\frac{T_o}{2}} \boldsymbol{I}_L{}^2(t) r_{on}\,\mathrm{d}t \tag{3.45}$$

Q_1 pulses according to the required SPWM waveform. Over each switching period, T_s, there are two switch-on events and two switch-off events as demonstrated in Equation (3.31). The losses due to these events are calculated as,

$$
\begin{aligned}
P_{Q_1} &= \frac{2}{T_\mathrm{o}} \sum_{k=0}^{k=\frac{f_\mathrm{s}}{2f_\mathrm{o}}} \left(\boldsymbol{W}_\mathrm{on}(k) + \boldsymbol{W}_\mathrm{off}\left(\frac{4k+1}{4}\right) + \boldsymbol{W}_\mathrm{on}\left(\frac{4k+2}{4}\right) + \boldsymbol{W}_\mathrm{off}\left(\frac{4k+3}{4}\right)\right) \\
&= \frac{2V_\mathrm{in}}{T_\mathrm{o}} \sum_{k=0}^{k=\frac{f_\mathrm{s}}{2f_\mathrm{o}}} \left\{ 2Q_\mathrm{rr} + t_\mathrm{rr}\left(\boldsymbol{I}_\mathrm{sw}(k) + \boldsymbol{I}_\mathrm{sw}\left(\frac{4k+2}{4}\right)\right) + \right. \\
&\quad \frac{1}{2}\left(\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+1}{4}\right)\left(\frac{V_\mathrm{in}}{\frac{\mathrm{d}V_\mathrm{sw}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+1}{4}\right)}{\frac{\mathrm{d}I_\mathrm{sw}}{\mathrm{d}t}}\right) + \right. \\
&\quad \left.\left. \boldsymbol{I}_\mathrm{sw}\left(\frac{4k+3}{4}\right)\left(\frac{V_\mathrm{in}}{\frac{\mathrm{d}V_\mathrm{sw}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+3}{4}\right)}{\frac{\mathrm{d}I_\mathrm{sw}}{\mathrm{d}t}}\right)\right)\right\}
\end{aligned}
\tag{3.46}
$$

The switching losses incurred in Q_2 are regarded as negligible compared to those in Q_1. This can be seen in Figure 3.13 since the voltage changes when the current is effectively 0 A and the current changes when the voltage is close to 0 V. Q_1 and Q_2 effectively form a single switch that is conducting for the full half-cycle. This loss is approximated using Equation (3.42).

The total losses over the half-cycle are, therefore, approximated as,

$$
\begin{aligned}
P_\mathrm{loss} &= \frac{2V_\mathrm{in}}{T_\mathrm{o}} \sum_{k=0}^{k=\frac{f_\mathrm{s}}{2f_\mathrm{o}}} \left\{ 2Q_\mathrm{rr} + t_\mathrm{rr}\left(\boldsymbol{I}_\mathrm{sw}(k) + \boldsymbol{I}_\mathrm{sw}\left(\frac{4k+2}{4}\right)\right) + \right. \\
&\quad \frac{1}{2}\left(\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+1}{4}\right)\left(\frac{V_\mathrm{in}}{\frac{\mathrm{d}V_\mathrm{sw}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+1}{4}\right)}{\frac{\mathrm{d}I_\mathrm{sw}}{\mathrm{d}t}}\right) + \right. \\
&\quad \left.\left. \boldsymbol{I}_\mathrm{sw}\left(\frac{4k+3}{4}\right)\left(\frac{V_\mathrm{in}}{\frac{\mathrm{d}V_\mathrm{sw}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_\mathrm{sw}\left(\frac{4k+3}{4}\right)}{\frac{\mathrm{d}I_\mathrm{sw}}{\mathrm{d}t}}\right)\right)\right\} + \frac{2}{T_\mathrm{o}} \int_0^{\frac{T_\mathrm{o}}{2}} {\boldsymbol{I}_\mathrm{L}}^2(t) r_\mathrm{on}\, \mathrm{d}t + \\
&\quad \frac{2}{T_\mathrm{o}} \int_0^{\frac{T_\mathrm{o}}{2}} \left(\boldsymbol{V}_{\mathrm{sw(f)}}\big(\boldsymbol{I}_\mathrm{L}(t)\big) \boldsymbol{I}_\mathrm{L}(t) \boldsymbol{U}_{\boldsymbol{Q_1}}(t) + \boldsymbol{V}_{\mathrm{sw(r)}}\big(\boldsymbol{I}_\mathrm{L}(t)\big) \boldsymbol{I}_\mathrm{L}(t) \boldsymbol{U}_{\boldsymbol{Q_4}}(t) \right) \mathrm{d}t
\end{aligned}
\tag{3.47}
$$

3.2.5 Loss Model Verification

In order to verify the loss model, different switching frequencies were modelled, and the loss model was compared to simulation results. The simulations were done using LTspice XVII [36]. Following the specifications mentioned in Table 2.2, the simulation results produced the results demonstrated in Table 3.2. The error remains below 10% between a switching frequency of 6 kHz

and 72 kHz. After this point, a number of non-ideal effects take place that lead to an error between the approximation and the actual loss, mainly,

- The initial and ending pulses of the SPWM waveform are at frequencies higher than what can be handled by the MOSFET drivers. This leads to missing pulses and a reduction in switching losses compared to the approximation.
- Minor delays in the switch-off time due to the parasitic gate-source capacitance start to show an effect. The delays lead to a change in the duty cycle which increases the current that flows through the circuit since the voltage pulses over the inductor stay on for a slightly longer period of time. This leads to higher conduction losses through the circuit compared to the approximation.

This means that the approximation is limited to a switching frequency of 72 kHz. Moving to higher frequencies would require a change in technology and possibly a change in topology. This, however, is not a concern as the frequencies of interest in this research are below this boundary and can be seen in Section 3.4.

Table 3.2: Verification of the loss model derived in this chapter against LTspice XVII simulations.

f_s	f_c	L	C	ζ	P_{loss}	P_{sim}[a]	err
kHz	Hz	mH	µF	unit	W	W	%
6	478	3.790	29.290	0.1975	33.0	33.2	0.8
12	885	1.984	16.303	0.1915	37.5	35.7	4.9
18	1330	1.321	10.841	0.1916	41.8	39.9	4.9
24	1841	0.967	7.724	0.1943	46.1	44.5	3.7
30	2297	0.775	6.197	0.1941	50.5	49.3	2.5
36	2789	0.641	5.080	0.1950	54.9	54.3	1.1
42	3260	0.549	4.343	0.1952	59.2	59.4	0.3
48	3753	0.478	3.762	0.1957	63.3	64.6	2.0
54	4221	0.425	3.345	0.1957	67.5	70.0	3.5
60	4699	0.382	3.003	0.1958	71.7	75.4	4.9
66	5179	0.347	2.722	0.1960	75.8	81.0	6.5
72	5663	0.318	2.487	0.1962	79.9	86.7	7.8

[a] P_{sim} is the loss found in simulations, it is defined in Equation (B.2).

3.3 Volumetric Approximation Model

Combining the ideal model found in Section 3.1 and the loss model found in Section 3.2, the final volumetric approximation can be found. The loss affects the size of the heat sink, which directly affects the overall volume. As mentioned in Section 2.3.4, to limit the scope of this research the heat sink is not optimised as there are many ways to configure a single volume to create a heat sink and each would perform differently. The heat sink density used in this research is a constant defined as D_{hs} and has the units $\text{W}\,\text{m}^{-3}$. The volume of the heat sink is then calculated as the product between the heat sink density and the loss approximation,

$$\boldsymbol{F}_{\text{hs}} = \frac{P_{\text{loss}}}{D_{\text{hs}}} \tag{3.48}$$

Combining Equations (3.22) and (3.48) leads to the final volumetric approximation of a specific SPWM inverter that uses MOSFETs as the switches as,

$$\begin{aligned}
\boldsymbol{F}_{\text{vol}} = &\frac{C}{2}\frac{m^2 {V_{\text{in}}}^2}{W_{\text{e}}} + \frac{L}{2}\frac{\left(\frac{V_{\text{o(p)}}}{R}\sqrt{1+\left(2\pi f_{\text{o}} RC\right)^2} + \frac{m}{2Lf_{\text{s}}}V_{\text{in}}\right)^2}{W_{\text{m}}} \\
&+ \frac{1}{D_{\text{hs}}}\Bigg[\frac{2V_{\text{in}}}{T_{\text{o}}}\sum_{k=0}^{k=\frac{f_{\text{s}}}{2f_{\text{o}}}}\Bigg\{2Q_{\text{rr}} + t_{\text{rr}}\left(\boldsymbol{I}_{\text{sw}}(k) + \boldsymbol{I}_{\text{sw}}\left(\frac{4k+2}{4}\right)\right) + \\
&\frac{1}{2}\left(\boldsymbol{I}_{\text{sw}}\left(\frac{4k+1}{4}\right)\left(\frac{V_{\text{in}}}{\frac{\text{d}V_{\text{sw}}}{\text{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}\left(\frac{4k+1}{4}\right)}{\frac{\text{d}I_{\text{sw}}}{\text{d}t}}\right) + \\
&\boldsymbol{I}_{\text{sw}}\left(\frac{4k+3}{4}\right)\left(\frac{V_{\text{in}}}{\frac{\text{d}V_{\text{sw}}}{\text{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}\left(\frac{4k+3}{4}\right)}{\frac{\text{d}I_{\text{sw}}}{\text{d}t}}\right)\right)\Bigg\} + \frac{2}{T_{\text{o}}}\int_0^{\frac{T_{\text{o}}}{2}} {\boldsymbol{I}_{\text{L}}}^2(t) r_{\text{on}}\,\text{d}t + \\
&\frac{2}{T_{\text{o}}}\int_0^{\frac{T_{\text{o}}}{2}}\left(\boldsymbol{V}_{\text{sw(f)}}\left(\boldsymbol{I}_{\text{L}}(t)\right)\boldsymbol{I}_{\text{L}}(t)\boldsymbol{U}_{\boldsymbol{Q_1}}(t) + \boldsymbol{V}_{\text{sw(r)}}\left(\boldsymbol{I}_{\text{L}}(t)\right)\boldsymbol{I}_{\text{L}}(t)\boldsymbol{U}_{\boldsymbol{Q_4}}(t)\right)\text{d}t\Bigg]
\end{aligned} \tag{3.49}$$

This equation is used to approximate the volume of the SPWM at different frequencies. Table 3.3 demonstrates the volumes of SPWMs between switching frequencies of 6 kHz and 72 kHz. Figure 3.16 is a plot of these volumes. It can be seen that the volume dips between 6 kHz and 12 kHz. In order to find the smallest SPWM, the frequency should vary between this range.

Table 3.3: The simulated volumes of the SPWM in a frequency range between 6 kHz and 72 kHz.

f_s	L	C	ζ	f_c	THD	P_{loss}	$\boldsymbol{F}_{fil}$	$\boldsymbol{F}_{hs}$	$\boldsymbol{F}_{vol}$
kHz	µH	µF	units	Hz	%	W	cm^3	cm^3	cm^3
6	3790	29.29	0.197	478	4.995	33.0	15.03	53.20	68.23
9	2589	20.70	0.194	688	5.004	35.2	9.93	56.74	66.68
12	1984	16.30	0.192	885	5.002	37.5	7.48	60.43	67.91
15	1635	13.90	0.188	1056	4.998	39.6	6.07	63.87	69.94
18	1321	10.84	0.192	1330	4.995	41.8	4.94	67.46	72.40
21	1108	8.87	0.194	1605	5.000	44.0	4.17	71.00	75.17
24	967	7.72	0.194	1841	5.000	46.1	3.64	74.40	78.04
27	860	6.88	0.194	2069	5.001	48.2	3.24	77.78	81.02
30	775	6.20	0.194	2297	4.995	50.5	2.91	81.48	84.39
33	701	5.58	0.195	2545	4.995	52.7	2.64	84.96	87.60
36	641	5.08	0.195	2789	5.003	54.9	2.41	88.49	90.91
39	591	4.68	0.195	3026	4.999	56.8	2.23	91.63	93.86
42	549	4.34	0.195	3260	4.996	59.2	2.07	95.50	97.57
45	512	4.04	0.195	3500	4.997	61.4	1.93	98.97	100.90
48	478	3.76	0.196	3753	4.999	63.3	1.80	102.11	103.91
51	450	3.54	0.196	3987	5.001	65.4	1.70	105.43	107.13
54	425	3.34	0.196	4221	5.001	67.5	1.60	108.93	110.53
57	402	3.16	0.196	4460	4.997	69.6	1.52	112.28	113.79
60	382	3.00	0.196	4699	4.996	71.7	1.44	115.70	117.14
63	363	2.85	0.196	4946	5.003	73.8	1.37	119.04	120.41
66	347	2.72	0.196	5179	4.996	75.8	1.31	122.18	123.49
69	332	2.60	0.196	5421	4.997	78.9	1.25	127.30	128.55
72	318	2.49	0.196	5663	5.001	79.9	1.20	128.92	130.12

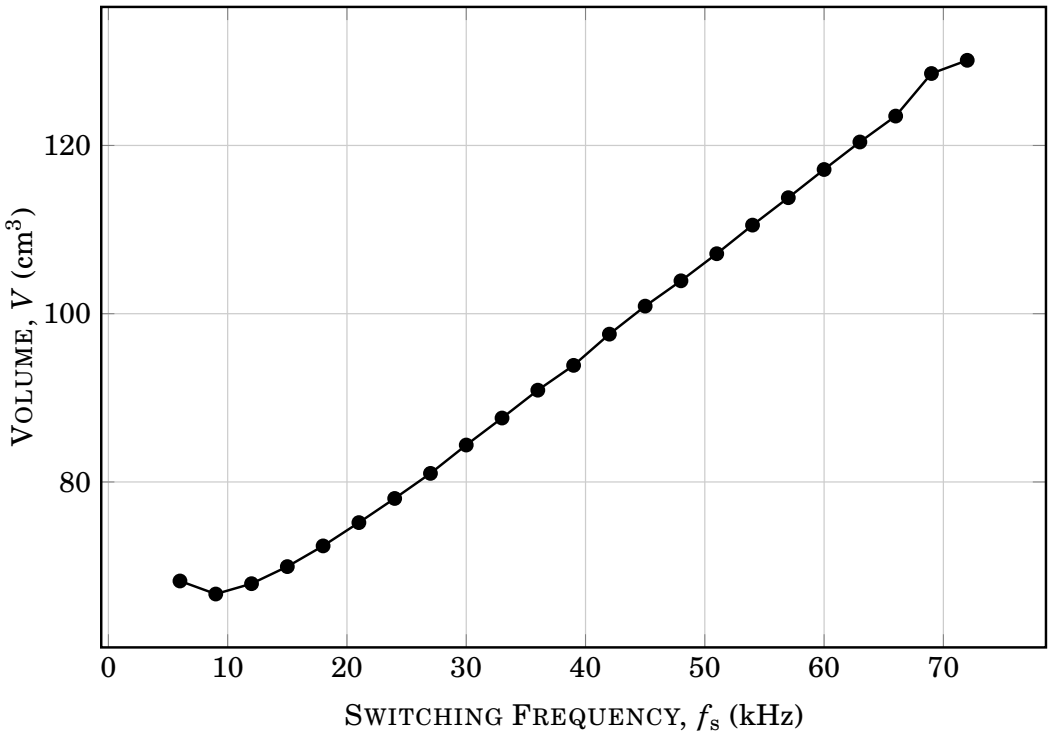


Figure 3.16: The volumetric approximations of the SPWM when simulated from 6 kHz to 72 kHz.

3.4 Relationships

Table 3.3 demonstrates the approximated volumes of the SPWM at different switching frequencies. It is important to note that the only decrease in volume is the dip between 6 kHz and 12 kHz. The relationships in this section focus around this point to see how small the volume could become given changes in technology.

Using numerical values from the volumetric approximation in Equation (3.49),

$$\begin{aligned}\boldsymbol{F}_{\text{vol}} = &\frac{C}{2}\frac{m^2 {V_{\text{in}}}^2}{W_{\text{e}}} + \frac{L}{2}\frac{\left(\frac{V_{\text{o(p)}}}{R}\sqrt{1+\left(2\pi f_{\text{o}} RC\right)^2} + \frac{m}{2Lf_{\text{s}}}V_{\text{in}}\right)^2}{W_{\text{m}}} \\ &+ \frac{1}{D_{\text{hs}}}\left[\frac{2V_{\text{in}}}{T_{\text{o}}}\sum_{k=0}^{k=\frac{f_{\text{s}}}{2f_{\text{o}}}}\left\{2Q_{\text{rr}} + t_{\text{rr}}\left(\boldsymbol{I}_{\text{sw}}(k) + \boldsymbol{I}_{\text{sw}}\left(\frac{4k+2}{4}\right)\right) + \right.\right. \\ &\frac{1}{2}\left(\boldsymbol{I}_{\text{sw}}\left(\frac{4k+1}{4}\right)\left(\frac{V_{\text{in}}}{\frac{\mathrm{d}V_{\text{sw}}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}\left(\frac{4k+1}{4}\right)}{\frac{\mathrm{d}I_{\text{sw}}}{\mathrm{d}t}}\right) + \right. \\ &\left.\left.\left.\boldsymbol{I}_{\text{sw}}\left(\frac{4k+3}{4}\right)\left(\frac{V_{\text{in}}}{\frac{\mathrm{d}V_{\text{sw}}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}\left(\frac{4k+3}{4}\right)}{\frac{\mathrm{d}I_{\text{sw}}}{\mathrm{d}t}}\right)\right)\right\} + \frac{2}{T_{\text{o}}}\int_0^{\frac{T_{\text{o}}}{2}} {\boldsymbol{I}_{\text{L}}}^2(t) r_{\text{on}}\,\mathrm{d}t + \right. \\ &\left.\frac{2}{T_{\text{o}}}\int_0^{\frac{T_{\text{o}}}{2}}\left(\boldsymbol{V}_{\text{sw(f)}}\left(\boldsymbol{I}_{\text{L}}(t)\right)\boldsymbol{I}_{\text{L}}(t)\boldsymbol{U}_{\boldsymbol{Q_1}}(t) + \boldsymbol{V}_{\text{sw(r)}}\left(\boldsymbol{I}_{\text{L}}(t)\right)\boldsymbol{I}_{\text{L}}(t)\boldsymbol{U}_{\boldsymbol{Q_4}}(t)\right)\mathrm{d}t\right]\end{aligned}$$

relationships can be established between different design parameters and the volume of the SPWM converter. By following the procedure defined in Figure 3.9, the first relationship that is seen is the linear relationship between the cut-off frequency, f_{c}, and the switching frequency, f_{s}, and is demonstrated in Figure 3.17. This relationship can be used to find the optimal filter size faster since L and C rely on f_{c}. By extrapolating this line, one can find the optimal volume by using a brute force method on ζ where a vector of values are used and the value of ζ that leads to the smallest volume is chosen as ζ^*.

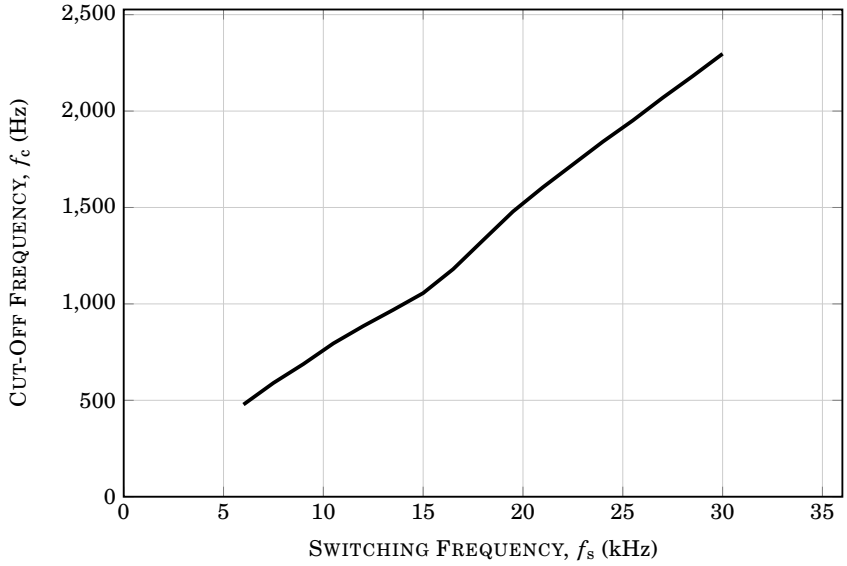


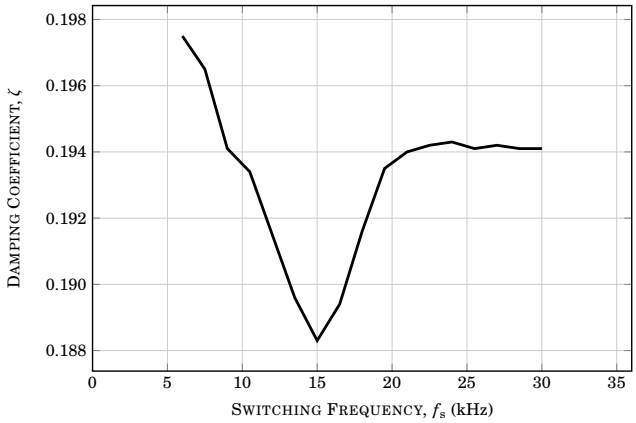
Figure 3.17: The linear relationship between f_c and f_s, based on the procedure defined in Figure 3.9.

The volume of the filter decreases as the switching frequency increases. The size of the capacitor and inductor constantly decrease as the switching frequency increases as can be seen by Figures 3.18b and 3.18c.

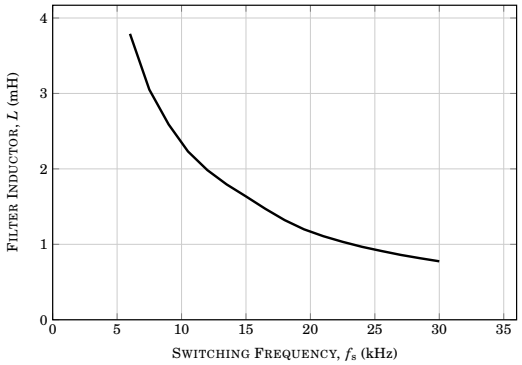
Although the volume of the filter decreases as the switching frequency increases, the switching losses increase which leads to a larger heat sink. This result agrees with the findings of Kolar *et al.* [2]. There is a balance between the volume of the filter and the volume of the heat sink and Figure 3.19 demonstrates this balance. Using current technology, the switching frequency that leads to the optimal volume is relatively low, this could change with an improvement in heat sink density which is discussed further on.

As the electric and magnetic energy densities increase, it can be seen that the volume of the inverter decreases. Figure 3.20 demonstrates the effect of the density changes on the volume of the inverter.

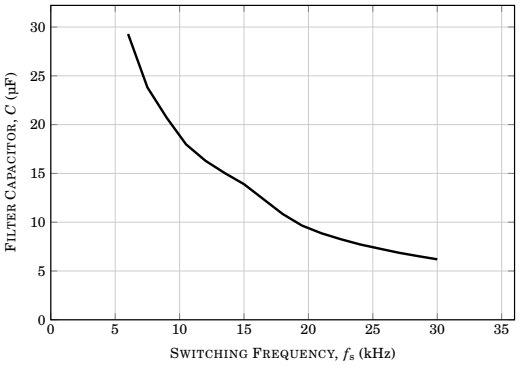
The changes in W_e and W_m do affect the volume of the inverter but W_e doesn't have as large an effect as W_m. It can be seen that the improvement in the magnetic field energy storage density of an inductor by a factor of 100 could effectively halve the size of the inverter. As mentioned in Section 2.3, the shape of the magnetic component is not considered. This could mean that



(a) The damping coefficient, ζ, changes with a change in the switching frequency, f_s. The change is extremely small and an approximation can be made for the optimal value of ζ based on this by choosing a value of ζ in this region.



(b) The size of the inductor decreases as the switching frequency increases.



(c) The size of the capacitor decreases as the switching frequency increases.

Figure 3.18: The size of the inductor and capacitor decrease exponentially with a change in the switching frequency, f_c. However, this is the only relationship that can be seen here, it does not provide insight into the smallest filter volume. Using this relationship, it can be seen that f_s should become as high as possible to reduce the size of the filter.

increasing the magnetic field energy storage density, realistically, would not have as great an effect as it stated here because the shape might limit the volumetric reduction, but this reduction in volume should not be overlooked.

The increase in W_e results a drastic increase in power density, however, there is another parameter that has a much greater effect on this power density. The density of the heat sink seems to have the largest effect on the power density of the inverter. Figure 3.21 shows that an increase in the density of the heat sink reduces the volume of the inverter by orders of magnitude. In

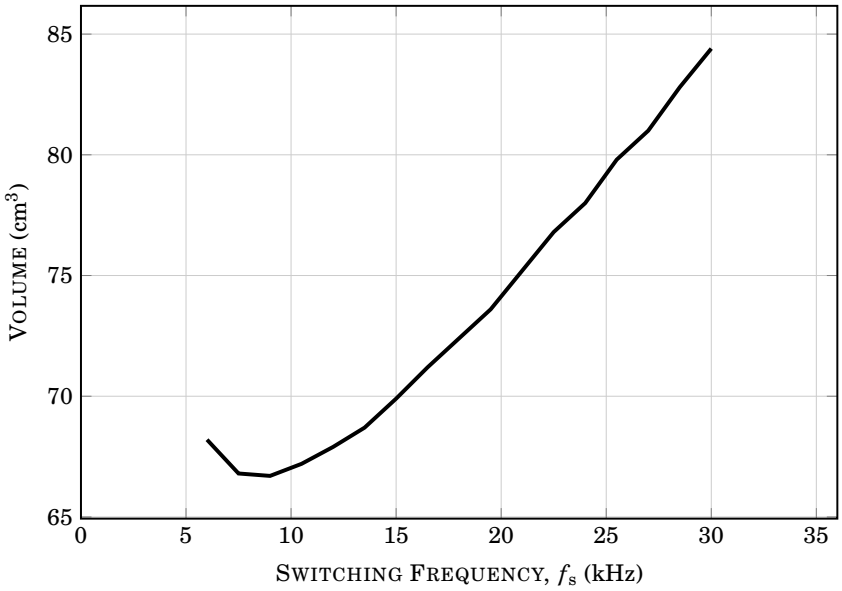
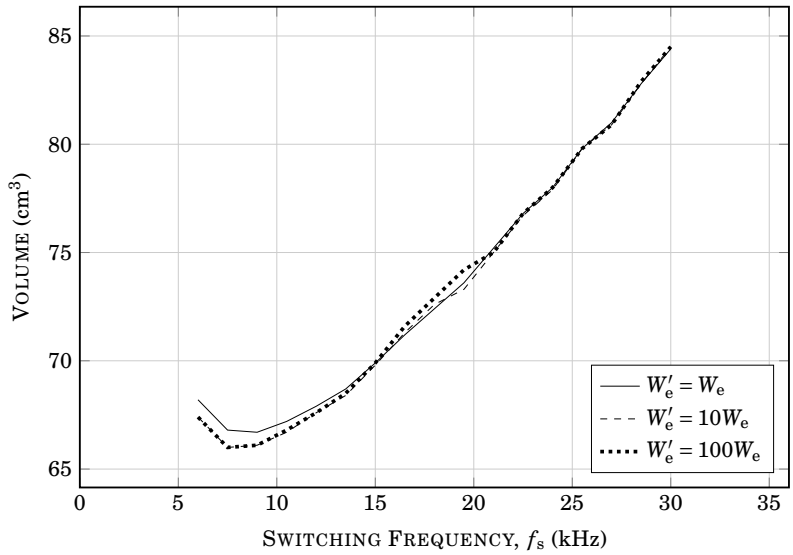


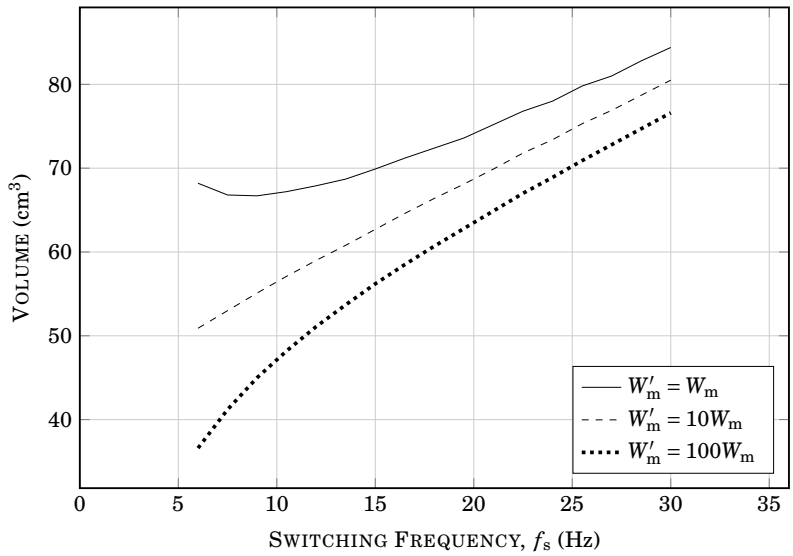
Figure 3.19: The volume of the inverter is parabolic and has a minimum point.

order to reduce the volume of the SPWM inverter, a major focus must be put in increasing the density of the heat sink. It can also be seen that the change in volume is logarithmic, this means that a small improvement in the density of the heat sink would lead to drastic reductions in volumes of the SPWM.

Figure 3.22 demonstrates the difference in volume if all of the densities, W_e, W_m, and D_{hs}, were to increase by a factor of 100. It should be noted that the volumetric ratio between Figures 3.22a and 3.22b is 100 times smaller and, based on Figures 3.20 and 3.21 this is mainly due to the increase in D_{hs} and W_m.



(a) As the electric field storage energy density, W_e, increases, the volume decreases. However, the decrease is not as drastic as the decrease in the magnetic field energy storage density.



(b) As the magnetic field storage energy density, W_m, increases, the volume of the filter drastically decreases. It can be seen that W_m is the bottleneck in trying to reduce the volume of the filter.

Figure 3.20: The comparison in volumetric change between the inverter and the electric and magnetic field energy storage densities, W_e and W_m.

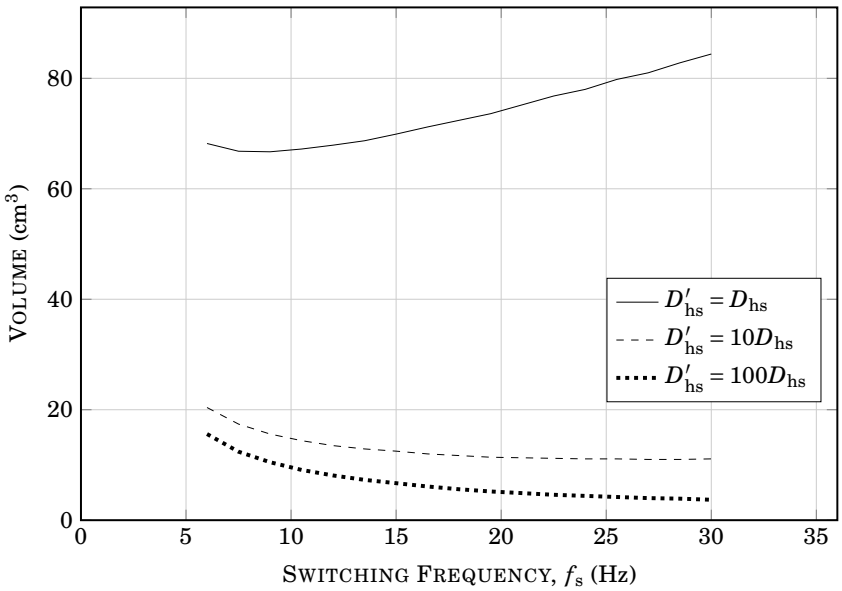
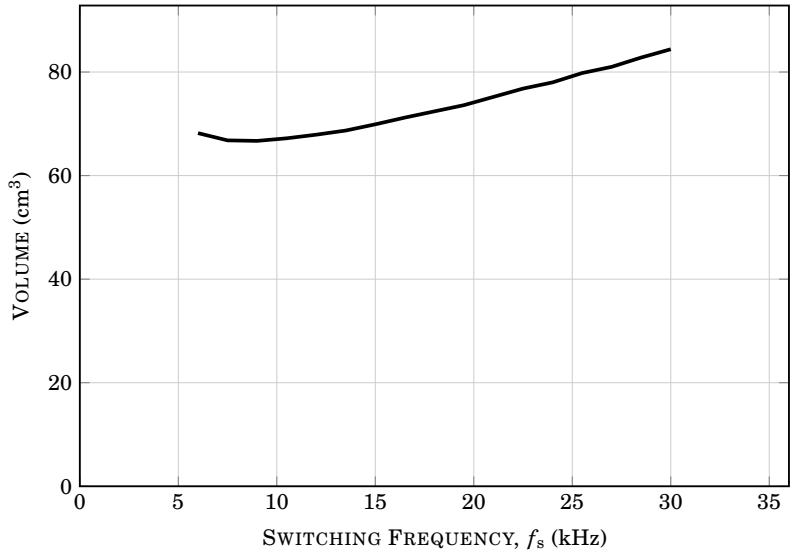
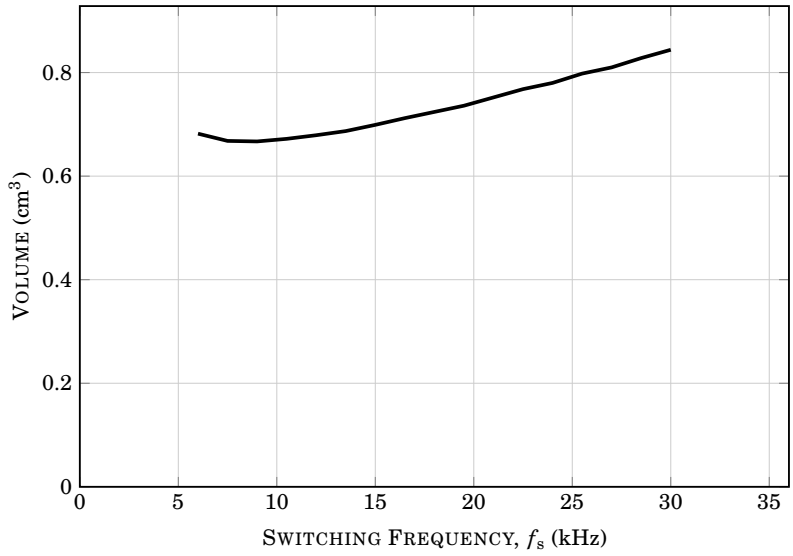


Figure 3.21: The change in the volume of the inverter as the heat sink density, D_{hs}, increases. The increase in the density of the heat sink drastically decreases the volume of the inverter compared to the changes in the energy storage densities, W_e and W_m.



(a) The volume of the SPWM inverter with current energy storage and heat sink densities.



(b) The volume of the SPWM inverter when the energy storage densities, as well as the heat sink densities, are all one hundred times larger.

Figure 3.22: The comparison in the volumetric change of the SPWM inverter as energy storage densities as well as heat sink densities improve. Notice the order of magnitude difference in the volume scales between the two graphs.

3.5 Simplified Example

To give an example of the entire process described above, a simple example is performed where the switching frequency, f_s, is four times the output frequency which adheres to the requirement specified in Equation (3.1). The required output waveform is $240\,V_{rms}$ at $60\,Hz$, and the input voltage is $450\,V$. The switching frequency, in this case, is $240\,Hz$. Figure 3.23 below demonstrates the control waveforms and the triangular waveforms that are applicable for these specifications. It should be noted that the outputs from this example are not practical as the switching frequency is not high enough and the filter adversely affects the output amplitude of the fundamental frequency, f_o. This is merely a demonstration of the method and allows for a visual representation.

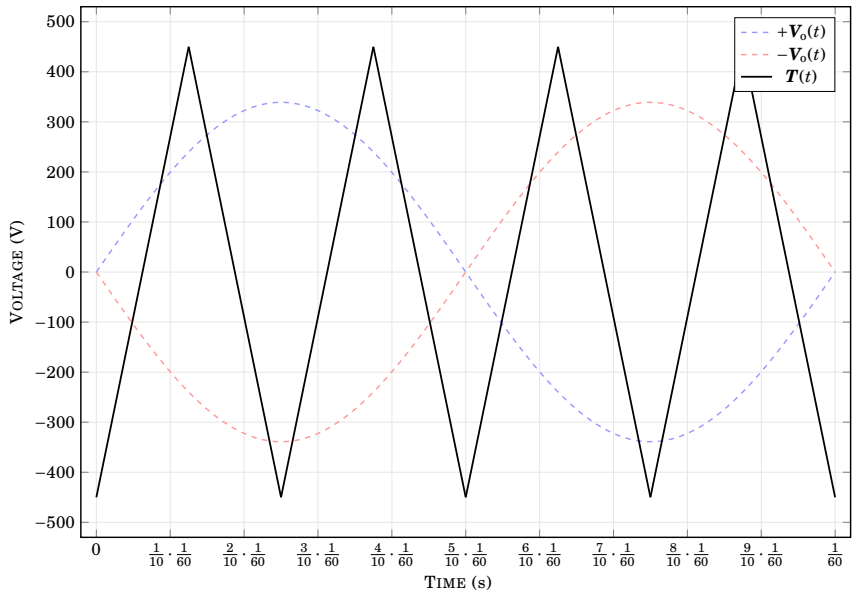
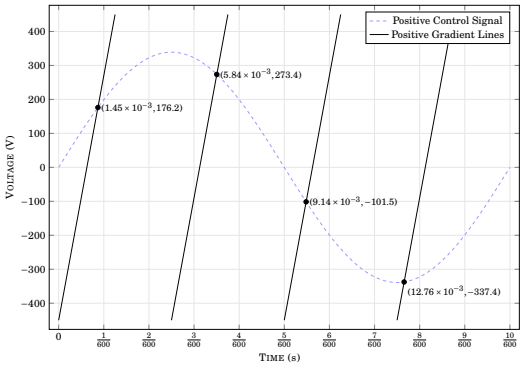
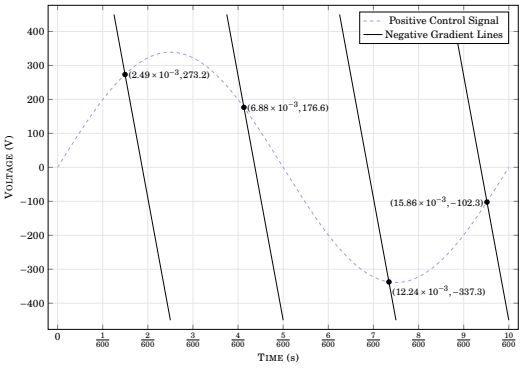


Figure 3.23: The sinusoidal control waveforms along with the triangular waveform used to calculate the $\boldsymbol{V}_A(t)$ and $\boldsymbol{V}_B(t)$ functions.

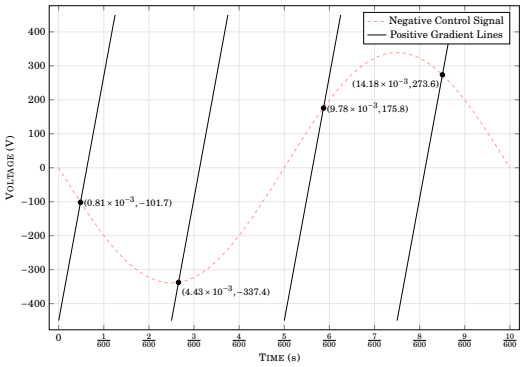
The intercept points are solved using Kepler's equation (see Appendix A) and these points are demonstrated in Figure 3.24 below. These intercepts are used to form the $\boldsymbol{V}_A(t)$ and $\boldsymbol{V}_B(t)$ waveforms from Equations (3.2) and (3.3). The $\boldsymbol{V}_A(t)$ waveform is formed using Figures 3.24a and 3.24b. The $\boldsymbol{V}_B(t)$ waveform is formed using Figures 3.24c and 3.24d. The final SPWM waveform is calculated using $\boldsymbol{V}_A(t) - \boldsymbol{V}_B(t)$. The $\boldsymbol{V}_A(t)$ waveform is demonstrated in Figure 3.25a, $\boldsymbol{V}_B(t)$ in Figure 3.25b, and the SPWM waveform in Figure 3.25c. Once the SPWM waveform has been calculated (Figure 3.25c), the Fourier Se-



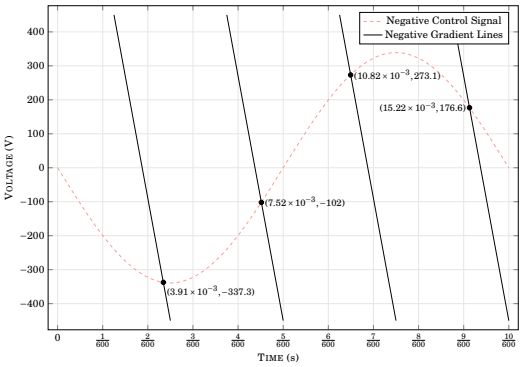
(a) Intercepts between the positive gradient lines and the positive control waveform.



(b) Intercepts between the positive gradient lines and the negative control waveform.



(c) Intercepts between the negative gradient lines and the positive control waveform.



(d) Intercepts between the negative gradient lines and the negative control waveform.

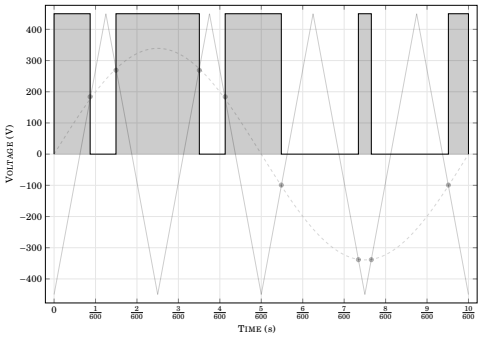
Figure 3.24: The points of intersection between the control waveforms and the triangular waveform.

ries is calculated to find the effects of the low pass filter on this waveform. During simulations, the first 40 harmonics are calculated for the Fourier Series, that means that the final harmonic is at a frequency[1] of 2.4 kHz. This allows for the first 10 harmonics of the switching frequency to appear in the series. The frequency spectrum of the SPWM waveform demonstrated in Figure 3.25c is plotted in Figure 3.26a. This figure demonstrates how the fundamental frequency has a higher magnitude than the others but there are still magnitudes that are significant at higher frequencies. The filter needs to reduce these frequencies in the output waveform in order to ensure that the THD is less than or equal to 5%. Before filtering the waveform the THD is approximately 81%. In order to get a THD of 5% the cut-off frequency is found to be 19.82 Hz with $\zeta^* = 0.32321$. The cut-off frequency, f_c, is less than the fun-

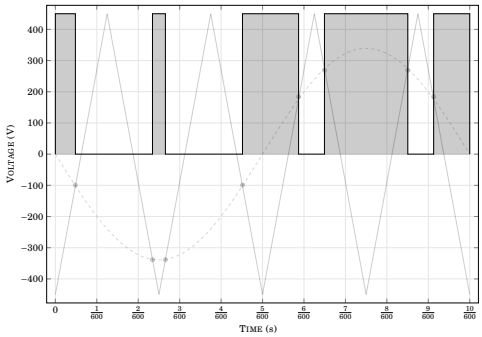
[1] Calculated as 60 Hz × 40.

damental frequency, f_o, and causes an adverse effect on the magnitude of the fundamental harmonic. The effect of the filter can be seen in Figure 3.26b. Although the THD meets the 5 % requirement, the system specifications are not met as the output amplitude is higher than $240\sqrt{2}$V. The value of f_c and ζ^* lead to the filter capacitance value being 431.37 µF and the inductance value being 149.51 mH.

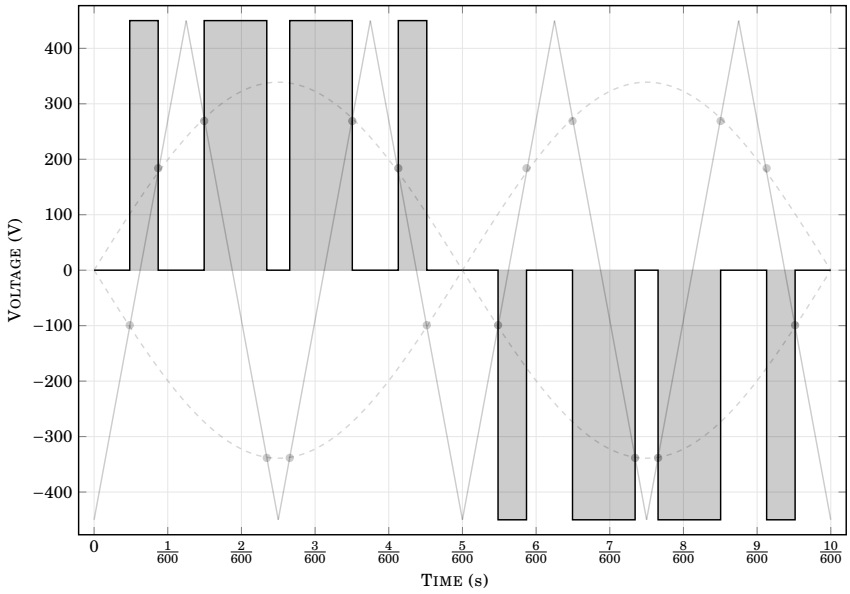
Finally, the loss is calculated as $P_{loss} = 0.92968$ W. Again, this value is not accurate as the cut-off frequency of the filter is too low and resonance is taking place which is not taken into account in the loss approximation (nor should it be when $f_s \gg f_o$).



(a) The $\boldsymbol{V}_A(t)$ function generated using Kepler's equation and the positive control waveform.



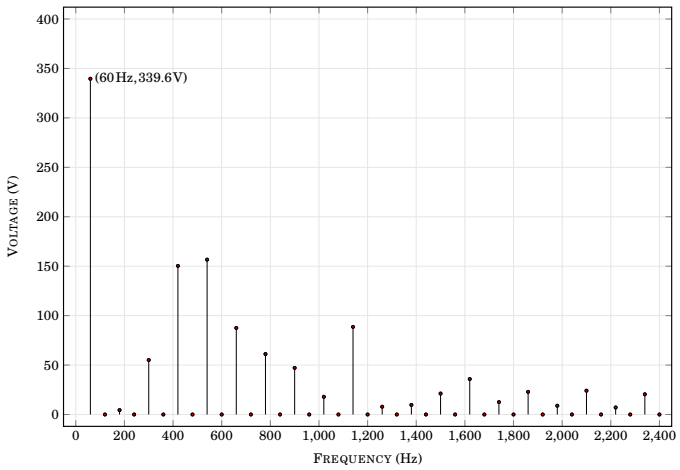
(b) The $\boldsymbol{V}_B(t)$ function generated using Kepler's equation and the negative control waveform.



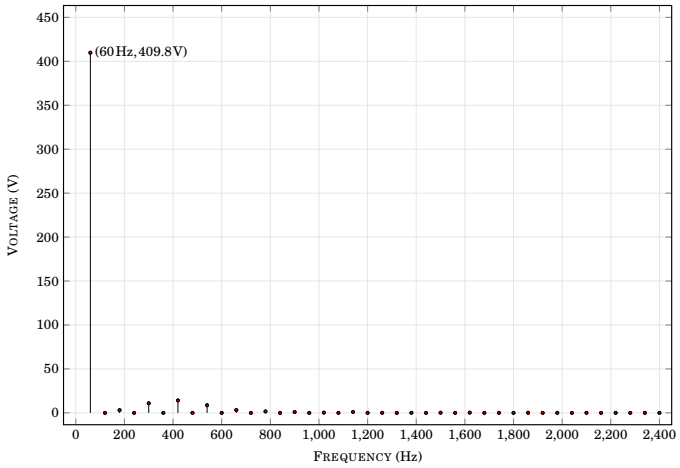
(c) The SPWM waveform, $\boldsymbol{V}_A(t) - \boldsymbol{V}_B(t)$.

Figure 3.25: Generating the SPWM waveform using $\boldsymbol{V}_A(t)$ and $\boldsymbol{V}_B(t)$.

This leads to the volume of the inverter being $4702\,\text{cm}^3$ which is the optimal volumetric approximation of an inverter that requires the switching frequency to be at 240 Hz and the THD to be at 5 %. Again, it should be noted that this system does not meet the system specifications as the output amplitude is incorrect, however, this example does demonstrate the design process in its entirety along with visual examples.



(a) The magnitudes of the first 40 harmonics in an SPWM waveform that has a switching frequency at 240 Hz.



(b) The magnitudes of the first 40 harmonics in an SPWM waveform that has a switching frequency at 240 Hz after passing through the low pass filter.

Figure 3.26: The harmonic magnitudes of the SPWM waveform before and after passing through the low pass filter.

3.6 Summary

The knowledge covered in this chapter is demonstrated in Figure 3.27 below. Under the system specifications mentioned in Table 2.2, the main points to take from this chapter are as follows,

- The SPWM is a common topology and is used as the baseline inverters to which others are compared in this research.
- Kepler's equation can be used to find the switch-on and switch-off times of the SPWM waveform at high accuracies.
- The relationship between the switching frequency, f_s, and the cut-off frequency, f_c, is linear.
- The optimal value of the damping coefficient, ζ^*, is almost constant at all values of f_s for set energy densities, W_e and W_m.
- The parameters that have a major effect on the volume of the inverter are the density of the heat sink, D_{hs}, and the magnetic field energy storage density, W_m.

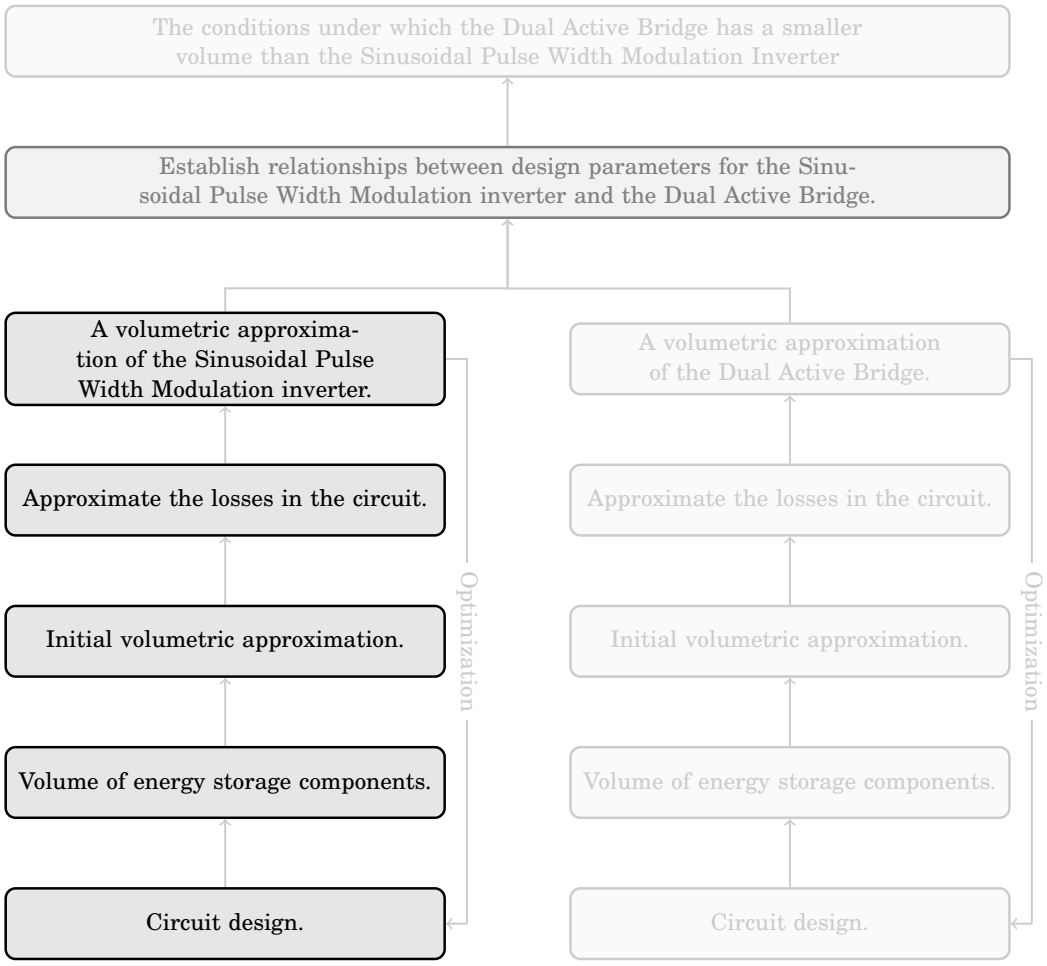


Figure 3.27: The contribution to the overall argument provided by Chapter 3.

The Dual Active Bridge 4

Krismer provides a lot of insight into the DAB through his PhD under Kolar [20]. Detail goes into modulation and modelling of the DAB under DC-to-DC conditions. However, Krismer does not look at using the DAB as an inverter. The modelling throughout this chapter is similar to that performed by Krismer, however, the current and voltage waveforms differ over the output waveform period. The DAB is presented in Figure 4.1 below, where the input voltage is DC and the output voltage is AC. As mentioned in Section 2.2.3, the DAB creates a full-wave rectified sinusoidal output waveform which must be passed through a low-frequency inverter to form the positive and negative half-cycles. The low-frequency inverter is ignored in the DAB models as it would be switching at 0 V and would contribute very little towards the losses compared to the high-frequency DAB bridges.

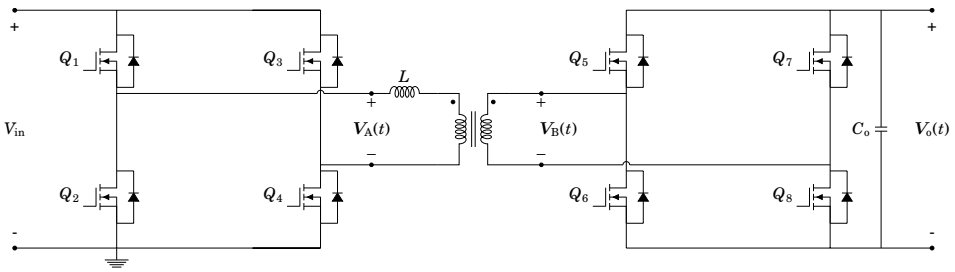


Figure 4.1: The circuit diagram of the Dual Active Bridge that is used in this research. The input voltage V_{in} is assumed to remain a constant DC input, and the output voltage is a time-varying AC waveform.

The models created throughout this chapter are based on Figure 4.1 above. This is the general DAB converter, there are cases where the leakage inductance is not lumped on the primary side and appears on both sides of the transformer. Either way, the outcome of the modelling is the same, as the transformer ratio is used to transform the secondary leakage inductance and lump it together with the primary leakage inductance.

4.1 Modulation Technique

The DAB provides the ability to use many modulation techniques. Three main modulation techniques are,

1. Phase Shift Modulation (PSM).
2. Triangular Modulation (TriM).
3. Trapezoidal Modulation.

These fundamental techniques form the grounds to create a number of current waveforms to fit the requirements of a DAB circuit. PSM and TriM were investigated in this research and are discussed in Sections 4.1.1 and 4.1.2 respectively. PSM was found to be relatively simple to implement but it did not work well in low load situations (details given in Section 4.1.1 below). TriM was more complicated to model and implement, however, it did provide the ability to control the output waveform at low load conditions.

4.1.1 Phase Shift Modulation

PSM is a modulation technique where the input and output bridges use a phase shift to determine the direction and magnitude of energy flow. The difference in phase causes a potential difference across the leakage inductance, thereby inducing a current. The effective voltage difference is demonstrated in Figure 4.2, where the input and output bridges are simplified to square wave voltage sources.

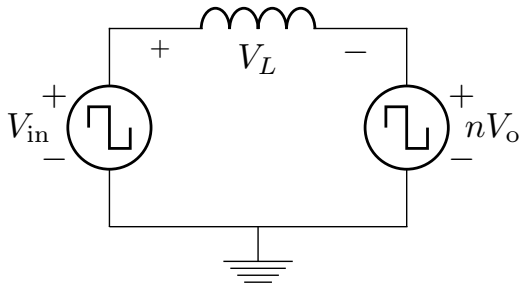


Figure 4.2: The approximated equivalent circuit of the DAB leading to a relatively simple method used to calculate the current through the leakage inductance at any given time.

The phase between the input and output bridges is defined as ϕ. As mentioned previously, changing this angle has an effect on the current through the leakage inductor. Figure 4.3 demonstrates a simplified example of the two bridges with a phase angle of ϕ between them, as well as the current through the transformer due to the leakage inductance. These bridges are phased using a PWM signal which is a realistic approach to building a PSM DAB.

Changing the phase angle, ϕ, the output power (and, therefore, output voltage) changes. The output power is controlled using the following equations [8], [20],

$$P_{\text{o}} = \frac{V_{\text{in}} V_{\text{o}}}{n\omega L}\phi\left(1 - \frac{|\phi|}{\pi}\right) \tag{4.1}$$

$$V_{\text{o}} = \frac{V_{\text{in}} R_{\text{L}}}{n\omega L}\phi\left(1 - \frac{|\phi|}{\pi}\right) \tag{4.2}$$

where,

- P_{o} output power;
- V_{in} DC input voltage;
- V_{o} output voltage;
- ω $= 2\pi f_{\text{s}}$, switching frequency in radians;
- n high-frequency transformer turns ratio;
- L DAB leakage inductance;
- ϕ phase difference between the bridges;
- R_{L} the output load resistance.

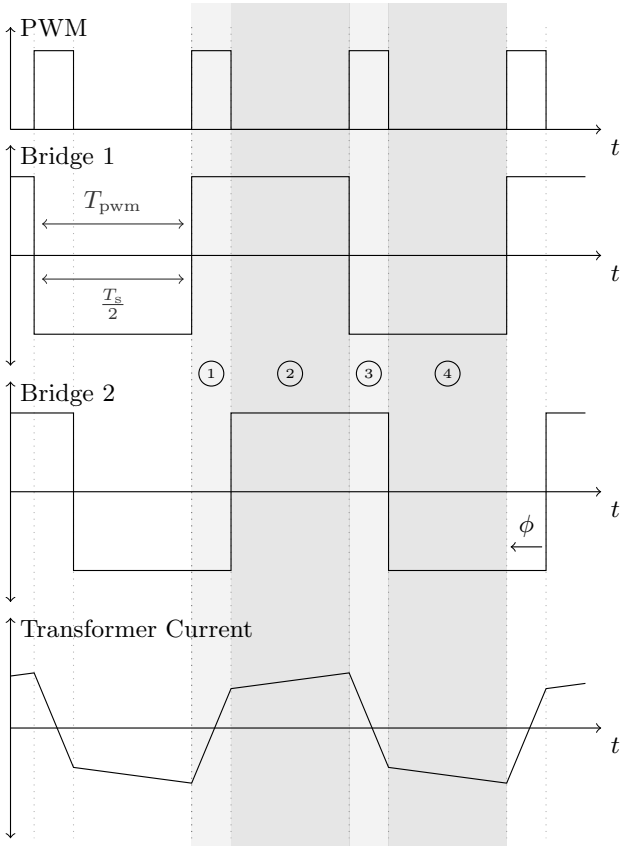


Figure 4.3: The method used to phase two bridges using a single PWM signal. This diagram demonstrates the switching period of the PWM signal, T_{pwm}, against the switching period of the bridges, T_{s}. There are four unique segments that contribute to the waveform and they are labelled accordingly. The phase, ϕ, between the bridges is related to the duty cycle of the PWM signal.

It was assumed that this could be converted into an AC equation by transforming the output power, output voltage, and phase angle to time-varying equations,

$$\boldsymbol{P}_{\text{o}}(t) = \frac{V_{\text{in}}\boldsymbol{V}_{\text{o}}(t)}{n\omega\boldsymbol{L}}\boldsymbol{\phi}(t)\left(1 - \frac{|\boldsymbol{\phi}(t)|}{\pi}\right) \tag{4.3}$$

$$\boldsymbol{V}_{\text{o}}(t) = \frac{V_{\text{in}}R_{\text{L}}}{n\omega\boldsymbol{L}}\boldsymbol{\phi}(t)\left(1 - \frac{|\boldsymbol{\phi}(t)|}{\pi}\right) \tag{4.4}$$

where,

- $\boldsymbol{P}_{\text{o}}(t)$ output power;
- $\boldsymbol{V}_{\text{o}}(t)$ AC output voltage;
- $\boldsymbol{\phi}(t)$ phase difference between the bridges.

Since the frequency being used would be higher than the output frequency, it was assumed that the output voltage would modulate according to the phase

angle using the equation below,

$$\phi(t) = \frac{\pi}{2} \pm \frac{\pi}{2}\sqrt{1 - 8\frac{nf_sL}{V_{in}R}V_o(t)} \quad , \quad \phi(t) \in \mathbb{R} \tag{4.5}$$

This means that there are some limitations in the design since it is possible for Equation (4.5) to move into the complex domain if $8\frac{nf_sL}{V_{in}R}$ is greater than 1. The design must, therefore, meet the requirement that,

$$4\frac{nf_sL}{V_{in}R}V_o(t) < 1 \tag{4.6}$$

From Equation (4.6) it can be seen that there is a limiting condition and there are three design parameters that may be changed to ensure that this condiditon is met,

- The turns ratio, n, may be increased or decreased. This, in turn, affects the currents through the circuit and, therefore, the conduction loss.
- The switching frequency, f_s, can be increased or decreased. This affects the current ripple as well as the switching loss of the circuit.
- The leakage inductance, L, can potentially be adjusted. The minimum leakage inductance depends on the transformer and cannot be changed. The total inductance can, however, be adjusted by adding more inductance in series with the transformer. In this research, L is referred to as the leakage inductance. This is not always the case as it is possible to add additional inductance if necessary.

In the case of this research, there is no direct impact on the design technique. However, it has been noted as it would be important when performing optimisation techniques and using new topologies (discussed in Chapter 5) where more parameters in the model will be considered.

Equations (4.1) to (4.6) do not consider the transient effects of the system and the response times to the changes in the phase angle. Additionally, both bridges are always on at a duty cycle of 50% as demonstrated in Figure 4.3 where the bridge waveforms are formed by a PWM signal[1], meaning that the current through the transformer cannot remain at 0A. At low loads, this

[1]Using a PWM signal to form the bridge waveforms is a realistic approach to implementing the DAB.

means that currents circulate through the converter but do not contribute to the output voltage. It also means that the phase angles need to be extremely small at low loads to ensure that only a small amount of energy is transferred from the primary side to the secondary side. This led to the need for a modulation technique that allows for more predictable low load output power. The Triangular Modulation technique was investigated and is discussed in Section 4.1.2 below.

4.1.2 Triangular Modulation

The TriM technique was considered because it allows for the current in the circuit to remain at 0 A in low load conditions since both bridges can be turned off, unlike PSM. The TriM technique gets its name from the fact that it forms triangular current waveform pulses as demonstrated in Figure 4.4. Krismer demonstrates that TriM can be used in many scenarios, both when $V_{\text{in}} > nV_{\text{o}}$ and $V_{\text{in}} < nV_{\text{o}}$ [20]. The application of TriM when $V_{\text{in}} > nV_{\text{o}}$ is most applicable for this research as $V_{\text{in}} > V_{\text{o(p)}}$ due to the specifications of the GLBC.

4.1.2.1 Modelling the Dual Active Bridge Switches using Triangular Modulation

The DAB using TriM can be modelled as six unique segments as demonstrated in Figure 4.4. These configurations are shown in Table 4.1 where a dot represents a switch being turned on and an empty space represents the switch being turned off.

Table 4.1: The switch configurations that form the six segments in Triangular Modulation. The switch names are based off Figure 4.1, and the segments are demonstrated in Figure 4.4 where the related circuit diagrams are demonstrated in Figure 4.5.

Segment	**Q_1**	**Q_2**	**Q_3**	**Q_4**	**Q_5**	**Q_6**	**Q_7**	**Q_8**
a	•			•	•			•
b		•		•	•			•
c		•		•		•		•
d		•	•			•	•	
e		•		•		•	•	
f		•		•		•		•

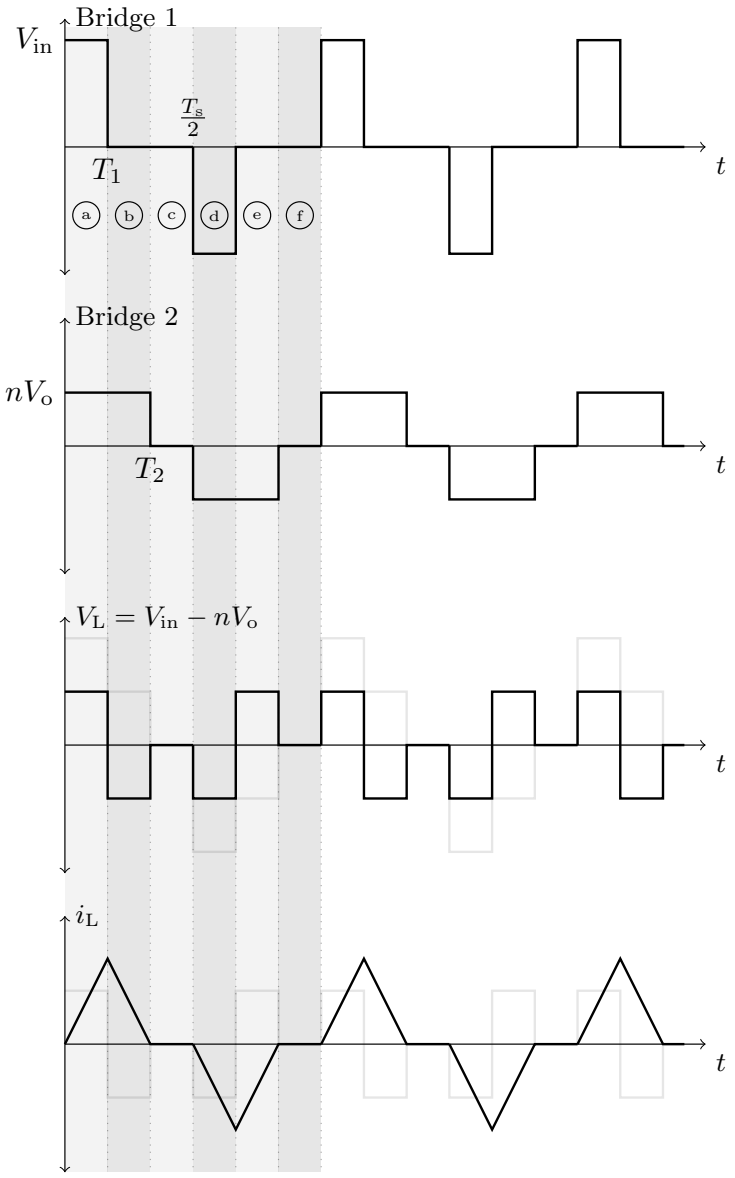
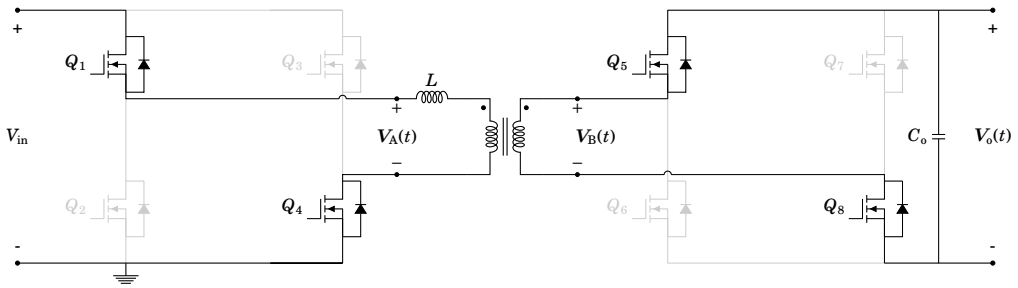
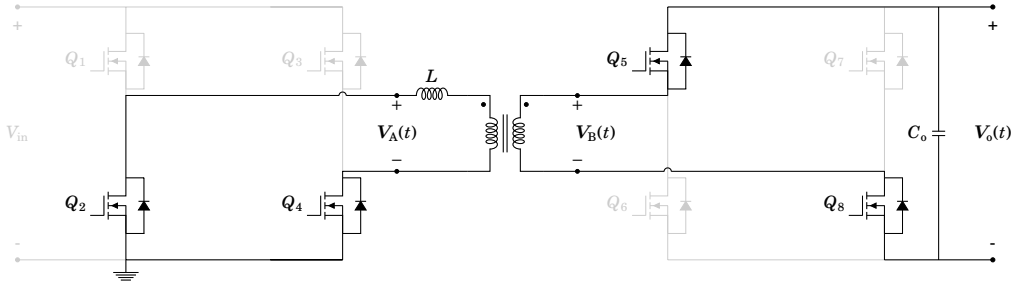


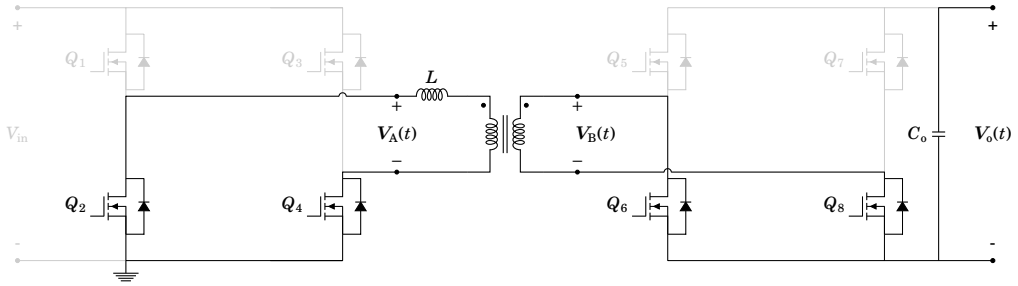
Figure 4.4: The current waveform, i_L, formed over the leakage inductance, L, using Triangular Modulation. Assuming that the primary bridge has a higher voltage than the secondary bridge (n can be adjusted to ensure this is the case), the primary bridge is kept on for a shorter period of time than the secondary. The secondary bridge is kept on until the current waveform reaches 0A and then it is switched off. Six unique segments make up the waveform and have been labelled in the figure.



(a) Both the input and output bridges are on, and power is flowing from the input to the output bridge. The current ramps up in the positive direction.

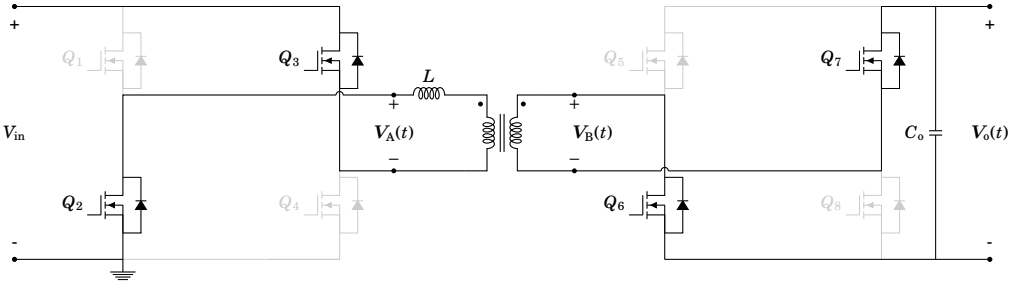


(b) The input bridge is switched off, and the energy stored in the leakage inductance is discharged until the current through the inductor reaches 0 A.

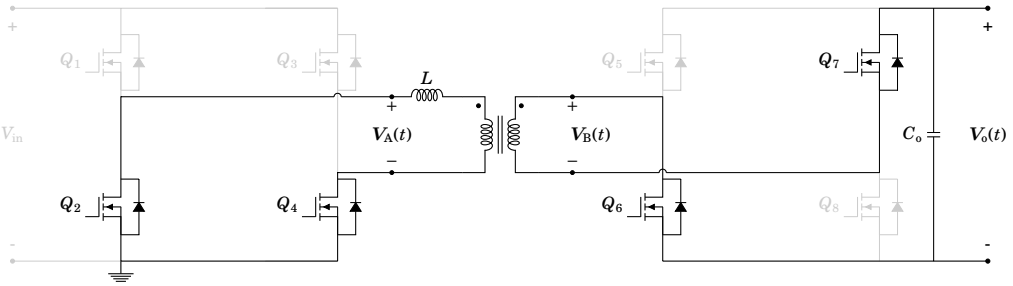


(c) The current through the leakage inductance is 0 A. At this point, both the input and output bridges are switched off and current flows into the output load from the output capacitor.

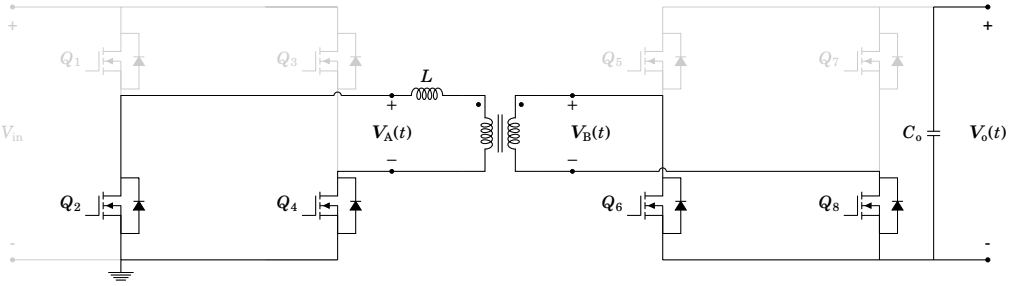
Figure 4.5: The current flow cycle through the DAB when using Triangular Modulation. The faded lines imply that no current is flowing through that path, therefore, the switches in these paths are off. This figure continues on the next page.



(d) Both the input and output bridges are switched in the reverse direction. This rectifies the current flowing into the output capacitor.



(e) The input bridge is switched off, and the energy from the leakage inductance discharges until the current through the leakage inductance reaches 0 A.



(f) The current through the leakage inductance has reached 0 A. Both the input and output bridges are switched off and the output load is powered through the output capacitance.

Figure 4.5: The current flow cycle through the DAB when using Triangular Modulation. The faded lines imply that no current is flowing through that path, therefore, the switches in these paths are off.

4.2 Triangular Modulation Mathematical Model

As demonstrated in Table 4.1 and Figure 4.5, six stages must be considered when modelling the DAB using TriM. Each stage is modelled and described below. Since the inversion of the bridges rectifies the signal, there are effectively three stages that are unique. All of the formulae are demonstrated below to reach this conclusion.

In the first stage, Figure 4.5a, both the input and output bridges are switched on, and power flows from the input to the output. The current through the leakage inductance ramps up leading to the start of the triangular waveform demonstrated in Figure 4.4. The formulae derived here form piecewise models for the output voltage, $\boldsymbol{V}_{\mathrm{o}}(t)$, and the derivative of the output voltage, $\boldsymbol{V}'_{\mathrm{o}}(t)$.

Before deriving the formula for each stage, the constants below should be defined, these constants were found during the derivations below and it increases legibility to use them from the start.

$$\gamma = \sqrt{L - 4C_{\mathrm{o}}R^2} \tag{4.7}$$

$$\alpha = \frac{\gamma}{C_{\mathrm{o}}R\sqrt{L}} \tag{4.8}$$

$$\beta = \frac{1}{2}\left(\frac{1}{RC_{\mathrm{o}}} + \alpha\right) \tag{4.9}$$

As demonstrated in Figure 4.4, there are two periods of time that should be defined, $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$. These are the periods of time that the primary and secondary bridges are on over each half-switching-cycle, $\frac{T_{\mathrm{s}}}{2}$.

Using the constants defined in Equations (4.7) to (4.9) as well as the time periods demonstrated in Figure 4.4, each stage is modelled. The equations obtained are labelled $\boldsymbol{V}_{\mathrm{a}}$ to $\boldsymbol{V}_{\mathrm{f}}$ and these voltages correspond to the output voltage for each stage in Figure 4.5. The differential equations that form the basis of $\boldsymbol{V}_{\mathrm{a}}$ to $\boldsymbol{V}_{\mathrm{f}}$ are found by calculating the voltage across the leakage inductance using the model in Figure 4.2. For instance, $\boldsymbol{V}_{\mathrm{a}}$ is calculated when

both bridges are switched on and are positive, in this case,

$$\boldsymbol{V}_{\mathrm{L}}(t) = V_{\mathrm{in}} - \boldsymbol{V}_{\mathrm{o}}(t)$$
$$L\frac{\mathrm{d}\boldsymbol{i}_{\mathrm{L}}(t)}{\mathrm{d}t} = V_{\mathrm{in}} - \boldsymbol{V}_{\mathrm{o}}(t)$$

This equation is then used to calculate the instantaneous value of $\boldsymbol{V}_{\mathrm{o}}(t)$. In all of the derived models below, there is a time shift to reduce complexity. The first stage is when both bridges are switched on as demonstrated in Figure 4.5a, defining $t_0 = t - kT_{\mathrm{s}}$, when time-shifted (to reduce complexity) the model for this stage is,

$$\begin{aligned}\boldsymbol{V}_{\mathrm{a}}(t) = \frac{1}{2n\gamma}e^{-\beta t_0}\Big(&2nRC_{\mathrm{o}}\boldsymbol{V}'_{\mathrm{o}}(0)\sqrt{L}\left(e^{\alpha t_0}-1\right) + \sqrt{L}\left(1-e^{\alpha t_0}\right)\left(V_{\mathrm{in}} - n\boldsymbol{V}_{\mathrm{o}}(0)\right)\\ &-\gamma\left(1+e^{\alpha t_0}-2e^{\beta t_0}\right)V_{\mathrm{in}} + \gamma\left(e^{\alpha t_0}+1\right)n\boldsymbol{V}_{\mathrm{o}}(0)\Big)\end{aligned} \tag{4.10}$$

The next stage is when the primary bridge is off and the secondary is on, as demonstrated in Figure 4.5b. Defining $v_{\mathrm{a}} = \boldsymbol{V}_{\mathrm{a}}(\boldsymbol{T}_1(k))$, $v'_{\mathrm{a}} = \boldsymbol{V}'_{\mathrm{a}}(\boldsymbol{T}_1(k))$ and $t_1 = t - \boldsymbol{T}_1(k)$, when time-shifted the model for this stage is,

$$\boldsymbol{V}_{\mathrm{b}}(t) = \frac{1}{2\gamma}e^{-\beta t_1}\left(2C_{\mathrm{o}}v'_{\mathrm{a}}\left(e^{\alpha t_1}-1\right)R\sqrt{L} + \left(e^{\alpha t_1}-1\right)v_{\mathrm{a}}\sqrt{L} + \left(e^{\alpha t_1}+1\right)\gamma v_{\mathrm{a}}\right) \tag{4.11}$$

After the stages defined in Equations (4.10) and (4.11), both bridges are switched off as demonstrated in Figure 4.5c. The output capacitor, C_{o}, discharges into the output load, R. Defining $v_{\mathrm{b}} = \boldsymbol{V}_{\mathrm{b}}(\boldsymbol{T}_2(k))$ and $t_2 = t - \boldsymbol{T}_2(k)$, the time-shifted voltage for this stage is modelled as,

$$\boldsymbol{V}_{\mathrm{c}}(t) = v_{\mathrm{b}}e^{-\frac{1}{RC_{\mathrm{o}}}t_2} \tag{4.12}$$

This discharge continues until half of the switching cycle, $\frac{T_{\mathrm{s}}}{2}$, and at that point, the primary bridge and secondary bridges are switched on in the reverse direction as demonstrated in Figure 4.5d. Defining, $v_{\mathrm{c}} = \boldsymbol{V}_{\mathrm{c}}\left(\frac{T_{\mathrm{s}}}{2}\right)$, $v'_{\mathrm{c}} = \boldsymbol{V}'_{\mathrm{c}}\left(\frac{T_{\mathrm{s}}}{2}\right)$ and $t_3 = t - \frac{T_{\mathrm{s}}}{2}$, the model for this stage is,

$$\begin{aligned}\boldsymbol{V}_{\mathrm{d}}(t) = \frac{1}{2n\gamma}e^{-\beta t_3}\Big(&2nRC_{\mathrm{o}}v'_{\mathrm{c}}\sqrt{L}\left(e^{\alpha t_3}-1\right) + \sqrt{L}\left(1-e^{\alpha t_3}\right)\left(V_{\mathrm{in}} - nv_{\mathrm{c}}\right)\\ &-\gamma\left(1+e^{\alpha t_3}-2e^{\beta t_3}\right)V_{\mathrm{in}} + \gamma\left(e^{\alpha t_3}+1\right)nv_{\mathrm{c}}\Big)\end{aligned} \tag{4.13}$$

The primary bridge then switches off leaving the secondary bridge to discharge the energy from the leakage inductance, as demonstrated in Figure 4.5e. Defining, $v_\mathrm{d} = \boldsymbol{V}_\mathrm{d}\left(\frac{T_\mathrm{s}}{2} + \boldsymbol{T}_1(k)\right)$, $v'_\mathrm{d} = \boldsymbol{V}'_\mathrm{d}\left(\frac{T_\mathrm{s}}{2} + \boldsymbol{T}_1(k)\right)$ and $t_4 = t - \left(\frac{T_\mathrm{s}}{2} + \boldsymbol{T}_1(k)\right)$, this stage is modelled as,

$$\boldsymbol{V}_\mathrm{e}(t) = \frac{1}{2\gamma} e^{-\beta t_4}\left(2C_\mathrm{o}v'_\mathrm{d}\left(e^{\alpha t_4} - 1\right)R\sqrt{L} + \left(e^{\alpha t_4} - 1\right)v_\mathrm{d}\sqrt{L} + \left(e^{\alpha t_4} + 1\right)\gamma v_\mathrm{d}\right) \tag{4.14}$$

Finally, both bridges switch off, as demonstrated in Figure 4.5f and the output capacitor, C_o, discharges into the output load. Defining $v_\mathrm{e} = \boldsymbol{V}_\mathrm{e}(\boldsymbol{T}_2(k))$ and $t_5 = t - \left(\frac{T_\mathrm{s}}{2} + \boldsymbol{T}_2(k)\right)$, the time-shifted voltage for this stage is modelled as,

$$\boldsymbol{V}_\mathrm{f}(t) = v_\mathrm{e} e^{-\frac{1}{RC_\mathrm{o}}t_5} \tag{4.15}$$

From these equations, it can be seen that the first three stages are effectively the same as the last three stages apart from the time-shift. This is due to the rectification process of both bridges inverting on the same stages.

4.2.1 Forming the Sinusoidal Waveform

The formulae derived in Equations (4.10) to (4.15) model the dynamics of the DAB and can be used to calculate how to form a sinusoidal waveform using the DAB and TriM. This is done by varying $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ on each switching cycle. These formulae allow one to dynamically calculate how the output voltage changes at any given time.

Using TriM, the values of $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ can be tied to the output voltage using the following equations [20],

$$\phi = \pi\sqrt{\frac{f_\mathrm{s}L}{n^2 R V_\mathrm{in}}\left(V_\mathrm{in} - n\boldsymbol{V}_\mathrm{o}(t)\right)} \tag{4.16}$$

$$\boldsymbol{T}_1(k) = \frac{\phi}{\pi f_\mathrm{s}}\frac{n\boldsymbol{V}_\mathrm{o}(t)}{V_\mathrm{in} - n\boldsymbol{V}_\mathrm{o}(t)} \tag{4.17}$$

$$\boldsymbol{T}_2(k) = \frac{\phi}{\pi f_\mathrm{s}} \tag{4.18}$$

The values of $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ are the required times for each bridge to be on to form the triangular waveform demonstrated in Figure 4.4. The variable,

k, is defined as the switching cycle and follows the same convention as k defined in Section 3.2.2. $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ can be any value less than or equal to $\frac{T_\mathrm{s}}{2}$, however, if these time periods are not determined using the above calculations, the waveform could be distorted and the current could change direction before returning to 0 A.

The stages that are defined in Equations (4.10) to (4.15) are non-linear and calculating what $\boldsymbol{V}_\mathrm{o}(t)$ would be after a switching cycle requires all six stages to be calculated. Defining a step function that exists for a period of time,

$$\boldsymbol{U}_\mathrm{s}(t, t_0, \boldsymbol{T}_1(k)) = \boldsymbol{u}_\mathrm{s}(t - t_0) - \boldsymbol{u}_\mathrm{s}(t - \boldsymbol{T}_1(k)) \tag{4.19}$$

Equations (4.10) to (4.15) can be combined to form the Piecewise Linear Models that would form the current through the leakage inductance,

$$\boldsymbol{V}_\mathrm{A}(t) = V_\mathrm{in}\boldsymbol{U}_\mathrm{s}(t, 0, \boldsymbol{T}_1(k)) - V_\mathrm{in}\boldsymbol{U}_\mathrm{s}\left(t, \frac{T_\mathrm{s}}{2}, \frac{T_\mathrm{s}}{2} + \boldsymbol{T}_1(k)\right) \tag{4.20}$$

$$\boldsymbol{V}_\mathrm{B}(t) = \boldsymbol{V}_\mathrm{o}(t)\boldsymbol{U}_\mathrm{s}(t, 0, \boldsymbol{T}_2(k)) - \boldsymbol{V}_\mathrm{o}(t)\boldsymbol{U}_\mathrm{s}\left(t, \frac{T_\mathrm{s}}{2}, \frac{T_\mathrm{s}}{2} + \boldsymbol{T}_2(k)\right) \tag{4.21}$$

where $\boldsymbol{V}_\mathrm{A}(t)$ is the modulated waveform from the input bridge, and $\boldsymbol{V}_\mathrm{B}(t)$ is the modulated waveform from the output bridge.

Equations (4.20) and (4.21) lead to the effective voltage over the leakage inductance of,

$$\boldsymbol{V}_\mathrm{L(tri)}(t) = \boldsymbol{V}_\mathrm{A}(t) - \boldsymbol{V}_\mathrm{B}(t) \tag{4.22}$$

Finally, the equation that can be used to calculate the current through the leakage inductance can be written as,

$$\boldsymbol{I}_\mathrm{L(tri)}(t) = \frac{1}{L}\int_0^t \boldsymbol{V}_\mathrm{L(tri)}(t)\,\mathrm{d}t \tag{4.23}$$

The numerical application of this can lead to minor errors where the current does not return to 0 A after each switching event. The approximation model does not take this into account and the error cascades over each event. In order to solve this problem, each switching cycle is multiplied by a unit step that starts at the beginning of the cycle and ends at the end of the cycle to

ensure that each current cycle ends at 0 A and the next event starts on 0 A.

The goal is to form a sinusoidal waveform at the output, however, it is not known what the value of ϕ should be after each switching cycle to achieve this. This is because the equations above focus on the DAB being in a steady state which is not always the case. A binary search algorithm is applied in much the same way as Figure 3.9 where the filter for the SPWM is found. This process is demonstrated in Figure 4.6. Using this method, each switching cycle has a calculated $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ that make it track a sinusoidal waveform.

The output from Figure 4.6 leads to a sinusoidal waveform, with ripple, that tracks an ideal output voltage waveform. Figure 4.7 demonstrates this output voltage and is coupled with LTspice XVII simulations to validate the results. It should be noted that the ideal output voltage and the approximation have very little error between them. The simulation output voltage has error due to losses, switching effects, and other non-ideal behaviours. These losses are modelled at a later stage, the main point to take from this figure is that it is possible to modulate a sinusoidal output waveform using a DAB and a DC input voltage.

4.3 Loss Model

A sinusoidal waveform can be created using the method mentioned in Section 4.2, the loss model is derived from this to approximate the requirements for building this inverter. The loss for the DAB could be summarised using,

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{esw}} + P_{\text{con}} + P_{\text{trans}} \tag{4.24}$$

where P_{trans} is the transformer loss and P_{esw} the loss dissipated during switch-on events.

4.3.1 Switching Loss

Figure 4.8 demonstrates the TriM current waveform that is formed by switching the input and output bridges. Points S_2 and S_5 point to high impact switching events since current is flowing through these switches as they are

turned off. There is the possibility of ZVS, however, the energy circulating through the system must be high enough to oscillate between the leakage inductance and the capacitance over the switches.

The losses at S_2 and S_5 must be considered. At these points, there is current

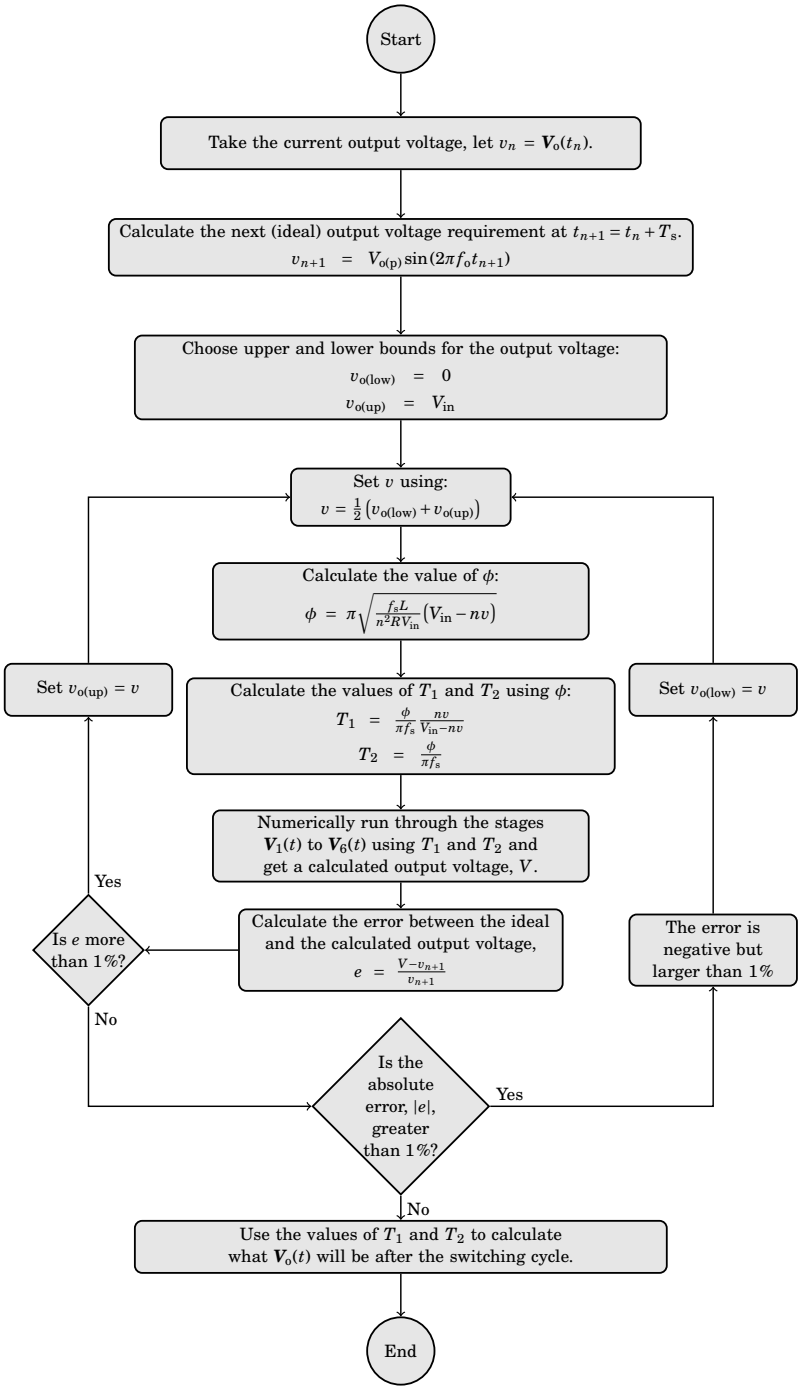
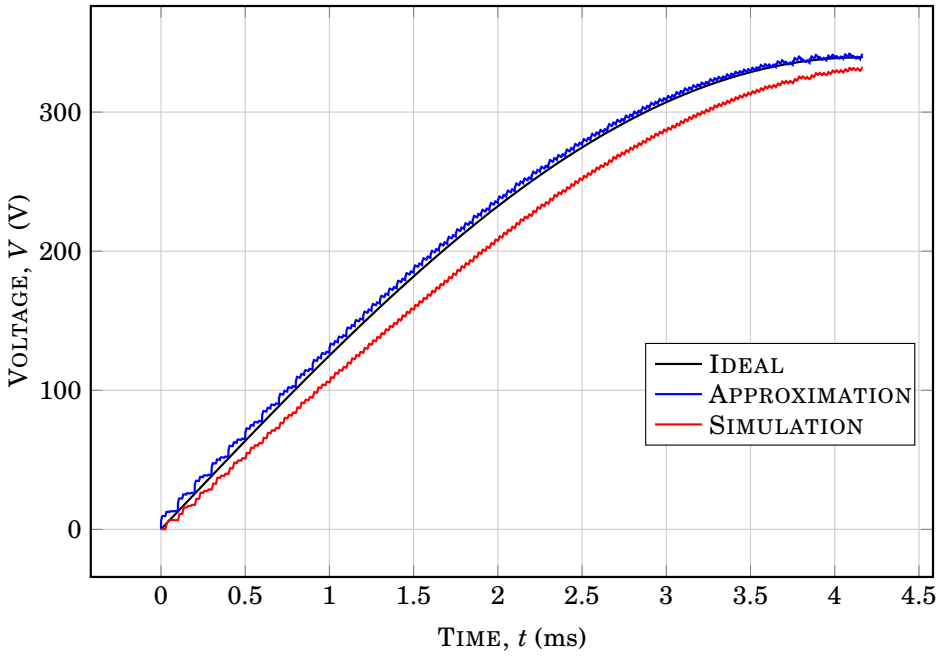
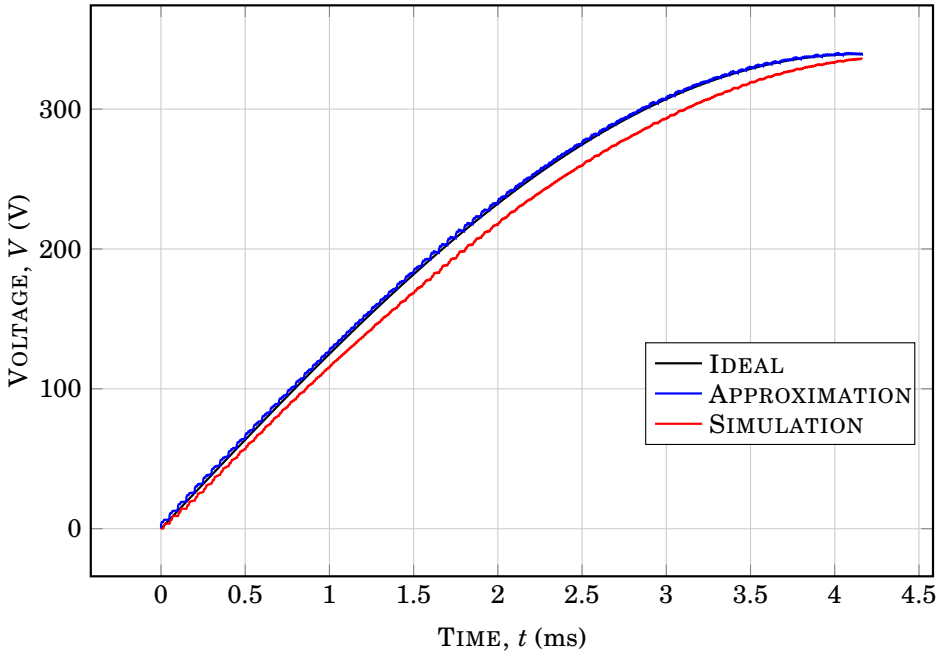


Figure 4.6: The method used to calculate the required value of ϕ that modulates the output voltage, $\boldsymbol{V}_o(t)$, according to a sinusoidal waveform.



(a) The DAB forming a modulated sinusoidal waveform at a switching frequency of 20 kHz.



(b) The DAB forming a modulated sinusoidal waveform at a switching frequency of 40 kHz.

Figure 4.7: The DAB forming the first quarter-cycle of the sinusoidal output voltage using TriM. These figures demonstrate the approximated (blue line) and simulated (red line) output voltages against the ideal output voltage (black line) at different switching frequencies.

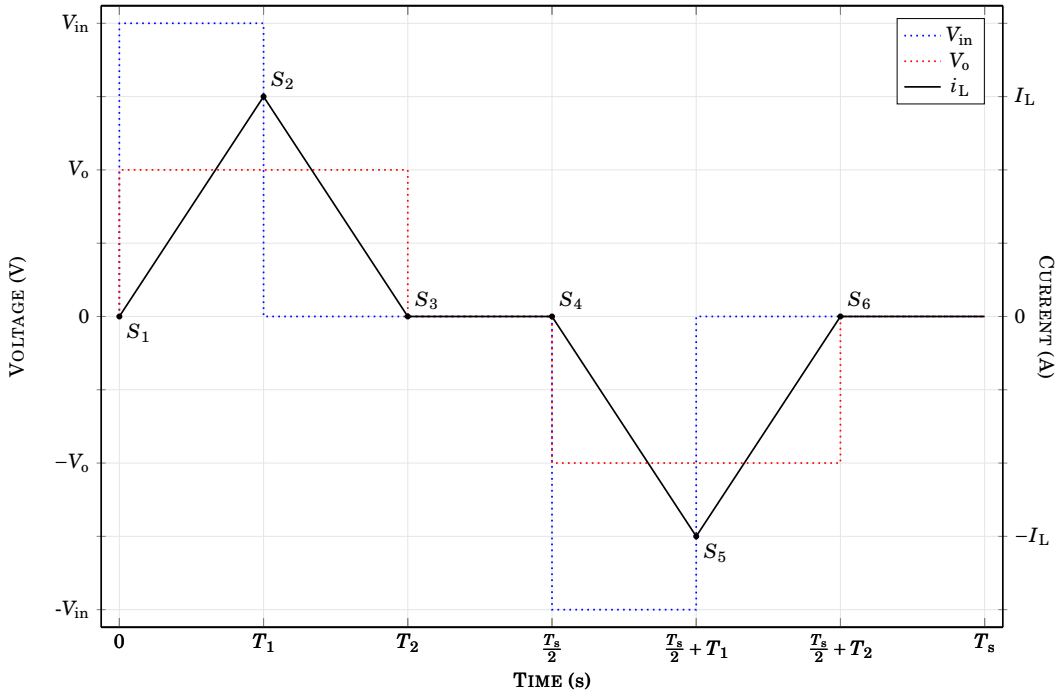


Figure 4.8: The switching events that take place in the Dual Active Bridge using Triangular Modulation. The solid black line represents the current through the leakage inductance, the dotted blue line represents the input bridge voltage, and the dotted red line represents the output bridge voltage.

flowing through the switches and a voltage across them. Since the output waveform is symmetric, the power loss can be calculated over a quarter of the waveform. The same method is used as Section 3.2.2.1 mentioned previously. In this case, $\boldsymbol{I}_{\text{sw}}(k)$ is defined as,

$$\boldsymbol{I}_{\text{sw}}(k) = \boldsymbol{I}_{\text{L(tri)}}\left(k\frac{T_{\text{s}}}{2} + \boldsymbol{T}_1(2k)\right) \tag{4.25}$$

Notice that k represents double the frequency of T_{s} which is why $2k$ is used when calculating $\boldsymbol{T}_1$. The switching loss for S_2 and S_5 can be approximated as,

$$P_{\text{sw}} = \frac{4}{T_{\text{o}}}\sum_{k=0}^{\frac{f_{\text{s}}}{2f_{\text{o}}}}\frac{1}{2}\boldsymbol{I}_{\text{sw}}(k)V_{\text{in}}\left(\frac{V_{\text{in}}}{\frac{\text{d}V_{\text{sw}}}{\text{d}t}} + \frac{\boldsymbol{I}_{\text{sw}}(k)}{\frac{\text{d}I_{\text{sw}}}{\text{d}t}}\right) \tag{4.26}$$

Furthermore, it is possible for ZVS to occur if there is enough energy in the leakage inductor to resonate with the capacitances over the switches in the primary bridge [8], [11], let,

$$\boldsymbol{\gamma}_{\text{ZVS}}(t) = 2\sqrt{\frac{C_{\text{s}}}{L}V_{\text{in}}\boldsymbol{V}_{\text{o}}(t)} \tag{4.27}$$

$$\boldsymbol{i}_{\mathrm{L}}(t) \geq \boldsymbol{\gamma}_{\mathrm{ZVS}}(t) \tag{4.28}$$

In order to utilise Equation (4.28), the relationship between time and k should be defined,

$$\boldsymbol{t}_{\mathrm{k}}(k) = k\frac{T_{\mathrm{s}}}{2} + \boldsymbol{T}_1(k) \tag{4.29}$$

At this point Equation (4.26) can be modified to ignore the switching loss that occurs when ZVS can take place. Equation (4.26) can, therefore, be modified to,

$$P_{\mathrm{sw}} = \frac{4}{T_{\mathrm{o}}} \sum_{\substack{k=0 \\ \boldsymbol{I}_{\mathrm{sw}}(k) < \boldsymbol{\gamma}_{\mathrm{ZVS}}(\boldsymbol{t}_{\mathrm{k}}(k))}}^{\frac{f_{\mathrm{s}}}{2f_{\mathrm{o}}}} \frac{1}{2} \boldsymbol{I}_{\mathrm{sw}}(k) V_{\mathrm{in}} \left(\frac{V_{\mathrm{in}}}{\frac{\mathrm{d}V_{\mathrm{sw}}}{\mathrm{d}t}} + \frac{\boldsymbol{I}_{\mathrm{sw}}(k)}{\frac{\mathrm{d}I_{\mathrm{sw}}}{\mathrm{d}t}} \right) \tag{4.30}$$

4.3.1.1 Switch-On Events

The switch-on events of the DAB at S_1 and S_4 are the major contributors to the loss in the circuit. Although the current flowing through the circuit at these switch on points is relatively low compared to the peaks at S_2 and S_5, there is still a large power loss that takes place at these events. The reason for this is because the (natural) capacitors over the switches need to charge and discharge at the switching events S_1 and S_4. Figure 4.9 demonstrates the event that takes place. The transition that causes the loss is when Q_1 is off and, Q_2 is on. The voltage across Q_1 is effectively V_{in} and Q_2 is 0V. At this point, Q_1 turns on, and Q_2 turns off. This causes the voltage across Q_2 to rapidly increase to V_{in} and the voltage across Q_1 to rapidly decrease to 0V. The energy required to charge and discharge these capacitors is dissipated through the Q_1 resistance. The capacitors do not charge and discharge entirely, this is because there is some current flowing through the leakage inductance that feeds into the capacitors during the event. This means that the energy lost is a function of the inductor current,

$$\boldsymbol{E}_{\mathrm{sw}}(t) = 2 \times \frac{1}{2} C_{\mathrm{s}} \boldsymbol{V}_{\mathrm{c}}(t)^2 = C_{\mathrm{s}} \boldsymbol{V}_{\mathrm{c}}(t)^2 \tag{4.31}$$

Where the capacitor voltage that is discharged is calculated as,

$$\boldsymbol{V}_{\mathrm{c}}(t) = V_{\mathrm{in}} - \sqrt{\frac{L}{2C_{\mathrm{s}}}} \boldsymbol{i}_{\mathrm{L}}{}^2(t) \tag{4.32}$$

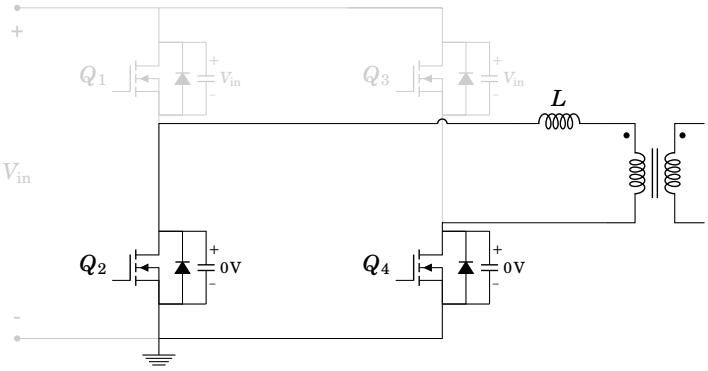
This equation is found by equating the energy in the leakage inductor to the energy shared by the two capacitors in question. The same equation applies to the output bridge, however, the voltage equation differs and is defined as,

$$\boldsymbol{V}_{\mathrm{co}}(t) = \boldsymbol{V}_{\mathrm{o}}(t) - \sqrt{\frac{L}{2C_{\mathrm{s}}}}\boldsymbol{i}_{\mathrm{L}}{}^{2}(t) \tag{4.33}$$

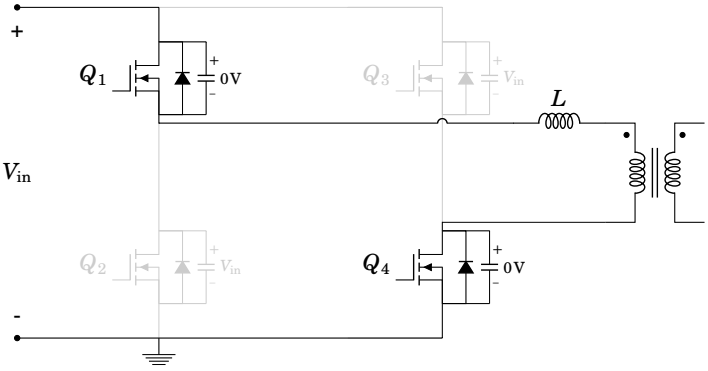
$$\boldsymbol{E}_{\mathrm{swo}}(t) = C_{\mathrm{s}}\boldsymbol{V}_{\mathrm{co}}(t)^{2} \tag{4.34}$$

The power lost due to these events is calculated as,

$$P_{\mathrm{esw}} = \frac{4}{T_{\mathrm{o}}}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{2f_{\mathrm{o}}}}\left(\boldsymbol{E}_{\mathrm{sw}}\left(k\frac{T_{\mathrm{s}}}{2}\right) + \boldsymbol{E}_{\mathrm{swo}}\left(k\frac{T_{\mathrm{s}}}{2}\right)\right) \tag{4.35}$$



(a) Switches Q_2 and Q_4 are on, causing the inductor current to flow through the loop until another switching event takes place. Although this current is low, it is not 0A. The voltage across switches Q_2 and Q_4 is effectively 0V, and the voltage across switches Q_1 and Q_3 is V_{in}.



(b) Switch Q_2 turns off, and Q_1 turns on. At this point, the voltage across the natural capacitor of Q_2 rapidly increases to V_{in}, and the voltage across the natural capacitor of Q_1 rapidly decreases to 0V. The energy required to charge and discharge the capacitances of Q_1 and Q_2 is dissipated through the resistance of Q_1.

Figure 4.9: An analysis of the switch-on events (S_1 and S_4) that cause substantial losses in the DAB circuit.

4.3.2 Conduction Loss

Since the current through the leakage inductance can be 0 A for extended periods of time, the conduction losses must be calculated based on the periods of time that the input and output bridges are on. During the time periods $\boldsymbol{T}_1(k)$ and $\boldsymbol{T}_2(k)$ both bridges will be conducting through two switches. Since the current and voltage waveforms are symmetric, the conduction loss can be calculated for a quarter of the output waveform, this is done using,

$$P_{\text{con}} = \frac{2}{T_{\text{o}}} \int_0^{\frac{T_{\text{o}}}{4}} \boldsymbol{I}_{\text{L(tri)}}{}^2(t)(n^2+1)r_{\text{on}}\,\mathrm{d}t \tag{4.36}$$

Since the current waveform follows that of Figure 4.4, there will be times when the conduction loss is very close to 0 W because the current is close to 0 A.

4.3.3 Output Capacitance

The ripple on the output waveform is reduced compared to the SPWM. This is because the waveform modulates around the required output waveform as opposed to modulating a square wave to form the sinusoidal wave when filtered. Using triangular modulation, the peak ϕ value in Equation (4.16) can be calculated as,

$$\phi_{\max} = \pi \sqrt{\frac{f_{\text{s}} L}{n^2 R V_{\text{in}}} \left(V_{\text{in}} - n V_{\text{o(p)}}\right)} \tag{4.37}$$

This would lead to T_1 at the peak being calculated as,

$$T_{1(\text{p})} = \frac{\phi}{\pi f_{\text{s}}} \frac{n V_{\text{o(p)}}}{V_{\text{in}} - n V_{\text{o(p)}}} \tag{4.38}$$

and the value of T_2 at the peak would be calculated as,

$$T_{2(\text{p})} = \frac{\phi}{\pi f_{\text{s}}} \tag{4.39}$$

Ideally, the triangular modulation should lead the current through the inductor to be 0 A after $T_{1(\text{p})} + T_{2(\text{p})}$, however, this is not the case because of the magnetising inductance. Additionally, the system is not in a steady state which introduces additional complexity in the modulation technique. The current flowing through the leakage inductance of the DAB can be approximated using the effective circuit demonstrated in Figure 4.2. As demonstrated in

Figure 4.5, both bridges are on during time, $T_{1(\mathrm{p})}$, the primary bridge is off, and the secondary is on during $T_{2(\mathrm{p})}$, and both bridges are off after $T_{2(\mathrm{p})}$ for the rest of the half-cycle.

During time $T_{1(\mathrm{p})}$, the current (ignoring the initial conditions) is,

$$\begin{aligned} \boldsymbol{i}_{\mathrm{L1}}(t) &= \frac{1}{L}\int_0^t \left(V_{\mathrm{in}} - nV_{\mathrm{o(p)}}\right) \mathrm{d}t \\ &= \frac{1}{L}\left(V_{\mathrm{in}} - nV_{\mathrm{o(p)}}\right)t \end{aligned} \tag{4.40}$$

During time $T_{2(\mathrm{p})}$, the current is,

$$\begin{aligned} \boldsymbol{i}_{\mathrm{L2}}(t) &= \boldsymbol{i}_{\mathrm{L1}}(T_{1(\mathrm{p})}) - \frac{1}{L}\int_0^t nV_{\mathrm{o(p)}}\,\mathrm{d}t \\ &= \boldsymbol{i}_{\mathrm{L1}}(T_{1(\mathrm{p})})t - \frac{1}{L}nV_{\mathrm{o(p)}}t \end{aligned} \tag{4.41}$$

For the rest of the half-cycle, the current would remain constant at $\boldsymbol{i}_{\mathrm{L2}}(T_{2(\mathrm{p})})$. The ripple current can be calculated as the area under Equations (4.40) and (4.41) as well as $\boldsymbol{i}_{\mathrm{L2}}(T_{2(\mathrm{p})})$ until $\frac{T_{\mathrm{s}}}{2}$. The ripple charge is, therefore,

$$\begin{aligned} Q_{\mathrm{L}} &= \int_0^{T_{1(\mathrm{p})}} \boldsymbol{i}_{\mathrm{L1}}(t)\,\mathrm{d}t + \int_0^{T_{2(\mathrm{p})}} \boldsymbol{i}_{\mathrm{L2}}(t)\,\mathrm{d}t + \int_0^{\frac{T_{\mathrm{s}}}{2}-T_{1(\mathrm{p})}-T_{2(\mathrm{p})}} \boldsymbol{i}_{\mathrm{L2}}(T_{2(\mathrm{p})})\,\mathrm{d}t \\ &= \boldsymbol{i}_{\mathrm{L1}}(T_{1(\mathrm{p})}) - \boldsymbol{i}_{\mathrm{L1}}(0) + \boldsymbol{i}_{\mathrm{L2}}(T_{2(\mathrm{p})}) - \boldsymbol{i}_{\mathrm{L2}}(0) + \left(\frac{T_{\mathrm{s}}}{2} - T_{1(\mathrm{p})} - T_{2(\mathrm{p})}\right)\boldsymbol{i}_{\mathrm{L2}}(T_{2(\mathrm{p})}) \\ &= \frac{1}{2L}\Big(T_{2(\mathrm{p})}\left(T_{2(\mathrm{p})} - T_{\mathrm{s}}\right)nV_{\mathrm{o(p)}} + T_{1(\mathrm{p})}^2\left(nV_{\mathrm{o(p)}} - V_{\mathrm{in}}\right) \\ &\quad + T_{1(\mathrm{p})}\left(2T_{2(\mathrm{p})}nV_{\mathrm{o(p)}} + T_{\mathrm{s}}\left(V_{\mathrm{in}} - nV_{\mathrm{o(p)}}\right)\right)\Big) \end{aligned} \tag{4.42}$$

The required capacitance for the ripple is calculated using,

$$\begin{aligned} C_{\mathrm{o}} &= \frac{Q_{\mathrm{L}}}{\Delta V_{\mathrm{o}}} \\ &= \frac{Q_{\mathrm{L}}}{0.05V_{\mathrm{o(p)}}} \end{aligned} \tag{4.43}$$

4.3.4 Transformer Losses

The transformer loss can be approximated using the Steinmetz equation. It should be noted that there are many methods to approximate the loss in trans-

formers but in order to reduce complexity of the overall model, the Steinmetz equation is used. The equation is defined as [37],

$$P_{\text{core}} = V_{\text{core}} k {f_{\text{sw}}}^{\alpha} B_{\text{p}}^{\beta} \tag{4.44}$$

where,

V_{core}	volume of the core found in Table 2.1;
B_{p}	peak magnetic flux density;
k, α, β	Steinmetz parameters.

The parameters that are entered into this equation are uniquely defined in each case. Section 4.4.1 demonstrates the use of this equation to approximate the loss for each transformer core size used in this case study.

4.3.5 Loss Model Verification

Table 4.2 demonstrates the loss approximation compared to the simulations found in LTspice XVII which used MOSFET models provided by the suppliers. Further details on these simulations, along with the circuit and waveforms are presented in Appendix D. The loss from the simulations does not take the transformer into account, however, in the final model, the loss from the transformer has been added to arrive at the final loss value for each DAB model. The transformer loss depends on the transformer volume, and the details of this are outlined in Section 4.3.4 above.

Given that the loss approximation has been verified in Table 4.2, more data points have been generated in Table 4.3 below along with details around the output capacitance, peak currents and voltages, and the required copper cross-section area in order to handle the currents at each frequency. There are three parameters in Table 4.2 that have not been utilised at this point. The first is the peak current, $i_{\text{L(p)}}$, which is the highest peak current seen when forming the sinusoidal output voltage and is applicable for the wire area requirement. The wire area requirement, A_{w}, is the area of wire required to handle the previously mentioned peak current. This value takes into consideration the current density that the wire can withstand. The final value is the integral of the squared inductor current over a full-time period, ζ. This value can be multiplied by a resistance such as the MOSFET on-resistance, r_{on}, and the transformer wire resistance to determine the conductive losses.

Table 4.2: Verification of the loss model derived in this chapter against LTspice XVII simulations.

f_s	P_{loss}	P_{sim}	e
kHz	W	W	%
18	137.29	148.17	7.34
24	127.58	135.51	5.85
30	126.42	129.42	2.32
36	126.59	128.21	1.27
42	130.70	128.17	1.97
48	131.87	130.11	1.35
54	137.82	131.96	4.44
60	141.13	134.37	5.03
66	145.28	142.63	1.86
72	142.74	151.05	5.50

where,

P_{loss} approximated losses in the circuit;
P_{sim} simulated losses in the circuit;
e error between the approximation and simulation.

4.4 Volumetric Approximation

The loss approximation defined in Section 4.3 is used to approximate the size of the heat sink. Similar to Section 3.3, the heat sink is defined as a density, D_{hs}, that is multiplied by the loss to determine the volume.

4.4.1 Transformer Choice

As demonstrated in Table 2.1, the transformers used for this circuit would be standard E-cores, and it is assumed that they are designed to utilise all of the winding area. A relatively simplistic approach is taken to determine which transformer to use, the number of turns required can be calculated using the equation,

$$N_w \geq \frac{V \cdot D_{on}}{\Delta B A_e f_s} \tag{4.45}$$

In the case of the DAB, the values described in Table 4.4 can be used in this equation.

In order to reduce the effects of the skin effect in the high-frequency transformer, Litz wire is used. The gauge of the wire is chosen depending on the

Table 4.3: The loss approximation for different switching frequencies based on the loss model derived in this research.

f_s	$i_{L(p)}$	A_w	ζ	$V_{o(max)}$	C_o	P_{loss}
kHz	A	mm^2	A^2	V	µF	W
18	55.73	12.38	289.82	348.91	19.3	137.29
21	51.58	11.46	261.53	348.56	16.5	130.67
24	47.78	10.62	244.32	348.22	14.5	127.58
27	45.65	10.14	224.25	347.69	12.9	126.79
30	43.15	9.59	211.39	347.17	11.6	126.42
33	40.99	9.11	200.40	346.90	10.5	126.96
36	39.28	8.73	189.50	346.64	9.65	126.59
39	37.43	8.32	182.31	345.77	8.90	127.99
42	36.21	8.05	173.91	345.46	8.27	130.70
45	35.22	7.83	168.99	344.69	7.72	132.10
48	34.16	7.59	163.33	344.48	7.23	131.87
51	33.11	7.36	156.10	344.27	6.81	136.86
54	31.75	7.06	151.66	344.08	6.43	137.82
57	31.15	6.92	147.97	343.73	6.09	139.96
60	30.52	6.78	151.04	343.06	5.79	141.13
63	29.52	6.56	136.51	342.15	5.51	142.54
66	28.92	6.43	131.35	341.55	5.26	145.28
69	28.34	6.30	126.68	341.31	5.03	144.40
72	27.82	6.18	124.27	340.30	4.82	142.74

where,

$i_{L(p)}$ peak current through the circuit;
A_w required area of wire to handle the peak current;
ζ $= \frac{1}{T_o}\int_0^{T_o} \boldsymbol{i}_L{}^2(t)\,\mathrm{d}t$;
C_o output capacitance;
$V_{o(max)}$ peak voltage in the circuit taking the effects of the output capacitance into account.

Table 4.4: The values used to design the transformer used in the DAB for this case study.

Parameter	Value
V	450 V
ΔB	400 mT
D_{on}	$\frac{1}{2}$
A_e	Table 2.1

frequency, and the number of strands is chosen based on the current density required. The work presented by Sullivan and Zhang [38] can be used to de-

sign the Litz wire required. The area of wire required to allow for the current to flow through the wire without it reaching a temperature where the insulation melts can be calculated as follows,

$$A_{\mathrm{w}} = \frac{I_{\mathrm{max}}}{J} \tag{4.46}$$

where,

A_{w} required wire area;
I_{max} maximum current through the circuit;
J current density.

Based on Equation (4.46), a chosen value of $J = 4.5\,\mathrm{A\,mm^{-2}}$ the standard E-core size can be found[2]. This is done by determining what area of copper would allow for the conditions of J to be met. The number of strands of wire to use to form the Litz wire is determined by taking the area required divided by the area of the gauge of wire that is being used, leading to the equation,

$$N_{\mathrm{s}} = \frac{A_{\mathrm{w}}}{A_{\mathrm{wg}}} \tag{4.47}$$

where N_{s} is the number of strands required and A_{wg} is the area of the wire being used.

The length of the wire required is approximated using the circumference of the winding area multiplied by the number of turns,

$$l_{\mathrm{w}} = NC_{\mathrm{w}} \tag{4.48}$$

where l_{w} is the total length of wire required and C_{w} is the circumference of the winding area.

The wire area in Equation (4.46) multiplied by the number of turns leads to the total area required, A_{req}, the difference between the E-core winding window area and the required area is calculated to see if a core meets the requirements and Table C.1 shows the valid E-core sizes for each switching frequency, f_{s}. The top choices for each frequency have been summarised in Table 4.5 which led to the transformer choices for each frequency range demonstrated

[2]The choice of a current density of $4.5\,\mathrm{A\,mm^{-2}}$ is based off the transformer design examples by Billings and Morey where they often use $450\,\mathrm{A\,cm^{-2}}$ [28].

in Table 4.6.

Table 4.5: The results from Table C.1 summarised by selecting the core that would lead to the minimum transformer volume for each switching frequency.

Core	A_e	f_s	N	A_w	C_w	l_w	A_{req}	Diff
	mm^2	kHz	turns	mm^2	mm	m	mm^2	%
E65/27	1196.0	18	58	12.38	146.0	8.5	718.3	40
E55/21	849.2	24	66	10.62	120.0	7.9	700.8	17
E55/21	849.2	30	53	9.59	120.0	6.4	508.2	40
E42/20	589.0	36	66	8.73	102.0	6.7	576.1	2
E42/20	589.0	42	56	8.05	102.0	5.7	450.6	23
E42/15	589.0	48	66	7.59	92.0	6.1	501.0	15
E42/15	589.0	54	58	7.06	92.0	5.3	409.2	31
E42/15	589.0	60	53	6.78	92.0	4.9	359.5	39
E42/15	589.0	66	48	6.43	92.0	4.4	308.5	48
E42/15	589.0	72	44	6.18	92.0	4.0	272.0	54

Table 4.6: The choice of E-core given a certain switching frequency, f_s, in the Dual Active Bridge. The volumes of each E-core have been defined in Table 2.1.

Frequency Range	E-core	Volume
kHz		cm^3
$18 \leq f_s < 24$	E65/27	173.686
$24 \leq f_s < 36$	E55/21	98.504
$36 \leq f_s < 48$	E42/20	54.723
$48 \leq f_s \leq 72$	E42/15	45.607

4.4.2 Transformer Volume

The E-core manufacturer and ferrite choice affect the final size of the inverter. This is because the core losses differ based on the material choice. For this case, the core manufacturer EPCOS which is TDK in Europe is used. For their E-core selection, they provide three main materials: *n27* [39], *n87* [40], and *n97* [41]. The relative core loss, P_v, decreases from *n27* to *n97*.

As mentioned in Section 4.3.4, the Steinmetz Equation is used to approximate the loss of the transformer. By removing the core volume, V_{core}, from Equation (4.44), the relative core loss, P_{v}, is found. This loss is defined as,

$$\begin{aligned} P_{\text{v}} &= k {f_{\text{sw}}}^{\alpha} B_{\text{p}}^{\beta} \\ \log\left(P_{\text{v}}\right) &= \log\left(k\right) + \beta \log\left(B_{\text{p}}\right) + \alpha \log\left(f_{\text{sw}}\right) \end{aligned} \tag{4.49}$$

and is usually provided in the datasheet of power converter transformers. By graph fitting this, the Steinmetz equation parameters are found. The datasheet for the *n97* material defines,

- $P_{\text{v}} = 45\,\text{kW}\,\text{m}^{-3}$ at $f_{\text{s}} = 25\,\text{kHz}$, $B_{\text{p}} = 200\,\text{mT}$.
- $P_{\text{v}} = 300\,\text{kW}\,\text{m}^{-3}$ at $f_{\text{s}} = 100\,\text{kHz}$, $B_{\text{p}} = 200\,\text{mT}$.
- $P_{\text{v}} = 340\,\text{kW}\,\text{m}^{-3}$ at $f_{\text{s}} = 300\,\text{kHz}$, $B_{\text{p}} = 300\,\text{mT}$.

These values lead to the following simultaneous equations,

$$\log\left(45\right) = \beta \log\left(0.2\right) + \alpha \log\left(25\right) + \log\left(k\right) \tag{4.50}$$

$$\log\left(300\right) = \beta \log\left(0.2\right) + \alpha \log\left(100\right) + \log\left(k\right) \tag{4.51}$$

$$\log\left(340\right) = \beta \log\left(0.3\right) + \alpha \log\left(300\right) + \log\left(k\right) \tag{4.52}$$

This leads to the following coefficient values, $\alpha = 1.36848$, $\beta = -3.39923$, and $k = 1.81447 \times 10^{-4}$. These values form the approximate transformer core loss equation,

$$\begin{aligned} P_{\text{core}} &= V_{\text{core}} \left(1.81447 \times 10^{-4} \left(f_{\text{sw}}\right)^{1.36848} \left(B_{\text{p}}\right)^{-3.39923} \right) \\ &= V_{\text{core}} \left(1.81447 \times 10^{-4} \left(f_{\text{sw}}\right)^{1.36848} \left(200\,\text{mT}\right)^{-3.39923} \right) \end{aligned} \tag{4.53}$$

Although this seems counter-intuitive as the β value is negative, it does correctly model the losses of the transformer. Using Equations (4.45), (4.46), (4.48) and (4.53) the core losses are calculated, and the results of these losses are shown in Table 4.7.

Table 4.7: The approximate losses with the additional transformer losses calculated in this section.

f_s	Core	V_{core}	$i_{L(p)}$	A_e	N	C_w	l_w	A_w	R_w	ζ	P_w	P_{core}	P_{approx}	P_{loss}
kHz	A	cm^2	units	mm^2	mm	mm^2	mΩ	mm^2	mW	A^2	W	W	W	W
18	E65/27	86.38	55.73	540	58	146	8.47	12.38	11.8	289.82	3.41	2.48	137.29	143.18
21	E65/27	86.38	51.58	540	50	146	7.30	11.46	11.0	261.53	2.86	3.07	130.67	136.60
24	E55/21	47.55	47.78	357	66	120	7.92	10.62	12.8	244.32	3.13	2.03	127.58	132.74
27	E55/21	47.55	45.65	357	59	120	7.08	10.14	12.0	224.25	2.69	2.38	126.79	131.86
30	E55/21	47.55	43.15	357	53	120	6.36	9.59	11.4	211.39	2.41	2.75	126.42	131.58
33	E55/21	47.55	40.99	357	48	120	5.76	9.11	10.9	200.40	2.18	3.13	126.96	132.27
36	E42/20	24.68	39.28	240	66	102	6.73	8.73	13.3	189.50	2.51	1.83	126.59	130.94
39	E42/20	24.68	37.43	240	61	102	6.22	8.32	12.9	182.31	2.35	2.04	127.99	132.38
42	E42/20	24.68	36.21	240	56	102	5.71	8.05	12.2	173.91	2.12	2.26	130.70	135.09
45	E42/20	24.68	35.22	240	53	102	5.41	7.83	11.9	168.99	2.01	2.49	132.10	136.59
48	E42/15	18.51	34.16	180	66	92	6.07	7.59	13.8	163.33	2.25	2.04	131.87	136.15
51	E42/15	18.51	33.11	180	62	92	5.70	7.36	13.3	156.10	2.08	2.21	136.86	141.15
54	E42/15	18.51	31.75	180	58	92	5.34	7.06	13.0	151.66	1.97	2.39	137.82	142.19
57	E42/15	18.51	31.15	180	55	92	5.06	6.92	12.6	147.97	1.86	2.58	139.96	144.40
60	E42/15	18.51	30.52	180	53	92	4.88	6.78	12.4	151.04	1.87	2.76	141.13	145.76
63	E42/15	18.51	29.52	180	50	92	4.60	6.56	12.1	136.51	1.65	2.95	142.54	147.14
66	E42/15	18.51	28.92	180	48	92	4.42	6.43	11.8	131.35	1.55	3.15	145.28	149.98
69	E42/15	18.51	28.34	180	46	92	4.23	6.30	11.6	126.68	1.46	3.35	144.40	149.21
72	E42/15	18.51	27.82	180	44	92	4.05	6.18	11.3	124.27	1.40	3.55	142.74	147.69

4.4.3 Total Volume

The total volume for the DAB inverter is calculated as the sum of the transformer volume, V_{T}, the heat sink volume, V_{hs}, and the output capacitor volume, $V_{C_{\mathrm{o}}}$. Table 4.8 shows the final volumes of the DAB inverter between 18 kHz and 72 kHz. These volumes are plotted in Figure 4.10, there's a dramatic decrease in volume from 18 kHz to 36 kHz and after this point the effect of the heat sink is more apparent and the decrease in volume from the E-core does not have as large an effect.

Table 4.8: The approximate losses with the additional transformer losses calculated in this section.

f_{s}	Core	V_{core}	V_{T}	P_{loss}	V_{hs}	C_{o}	$V_{\mathrm{o(max)}}$	$V_{C_{\mathrm{o}}}$	V_{tot}
kHz		cm^3	cm^3	W	cm^3	µF	V	cm^3	cm^3
18	E65/27	86.38	173.69	143.18	230.94	19.3	348.91	1.79	406.41
21	E65/27	86.38	173.69	136.60	220.32	16.5	348.56	1.53	395.54
24	E55/21	47.55	98.50	132.74	214.10	14.5	348.22	1.34	313.94
27	E55/21	47.55	98.50	131.86	212.68	12.9	347.69	1.18	312.37
30	E55/21	47.55	98.50	131.58	212.23	11.6	347.17	1.06	311.79
33	E55/21	47.55	98.50	132.27	213.34	10.5	346.90	0.96	312.81
36	E42/20	24.68	54.72	130.94	211.19	9.65	346.64	0.88	266.79
39	E42/20	24.68	54.72	132.38	213.52	8.90	345.77	0.81	269.05
42	E42/20	24.68	54.72	135.09	217.88	8.27	345.46	0.75	273.35
45	E42/20	24.68	54.72	136.59	220.31	7.72	344.69	0.70	275.73
48	E42/15	18.51	45.61	136.15	219.60	7.23	344.48	0.65	265.86
51	E42/15	18.51	45.61	141.15	227.67	6.81	344.27	0.61	273.89
54	E42/15	18.51	45.61	142.19	229.33	6.43	344.08	0.58	275.52
57	E42/15	18.51	45.61	144.40	232.90	6.09	343.73	0.55	279.05
60	E42/15	18.51	45.61	145.76	235.10	5.79	343.06	0.52	281.22
63	E42/15	18.51	45.61	147.14	237.32	5.51	342.15	0.49	283.42
66	E42/15	18.51	45.61	149.98	241.91	5.26	341.55	0.47	287.98
69	E42/15	18.51	45.61	149.21	240.66	5.03	341.31	0.45	286.72
72	E42/15	18.51	45.61	147.69	238.20	4.82	340.30	0.43	284.24

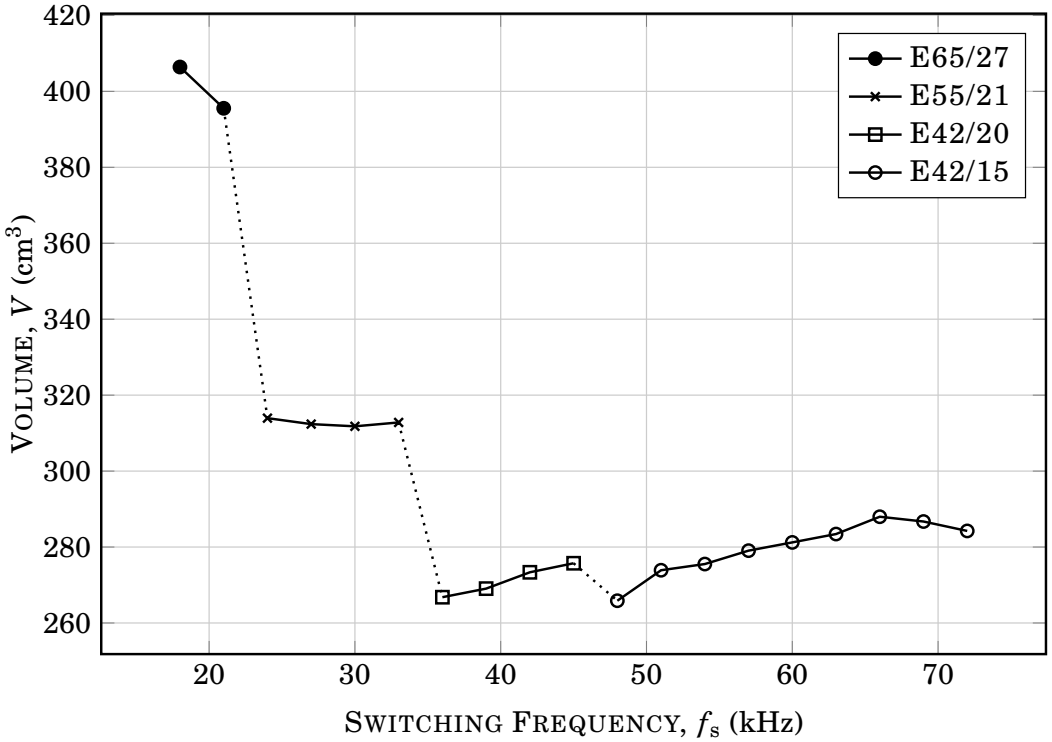


Figure 4.10: The volumetric approximations for the DAB between a frequency range of 18 kHz and 72 kHz. The plot has been divided into the different E-cores used depending on the frequency. It should be noted that there is a dramatic reduction in volume over each jump in E-core size until around 36 kHz, from this point it is more dependent on other factors such as the heat sink.

4.5 Relationships

Figure 4.11 demonstrates the effect that the density of the heat sink has on the final volume of the DAB. It can be seen that increasing the density by a factor of 10 can potentially halve the volume of the DAB inverter. After this point, a second increase by a factor of 10 (thereby increasing the initial density by a factor of 100), has a reduced impact on the volumetric decrease compared to the first density increase.

The change in E-core size also has a large effect on the change in volume. The aim, in this case, would be to use the E13/4 core which has a total volume of 1.154 cm^3 as opposed to the E42/15 core (required at a switching frequency of 72 kHz) with a volume of 45.607 cm^3. However, as seen in Table 4.8, the main aim should be to reduce the losses in the circuit. This is because the heat sink is much larger (over 200 cm^3) compared to the saving by changing the core to the E13/4 core.

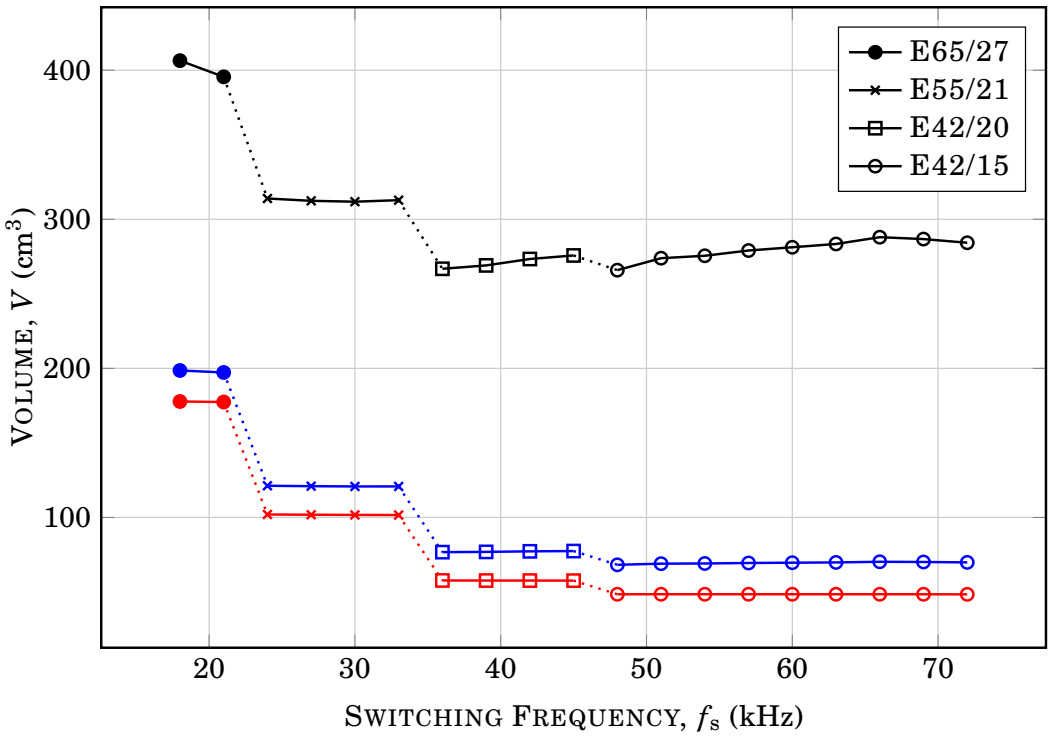


Figure 4.11: The volumetric approximations for the DAB as the heat sink density increases are demonstrated in this figure. The black line is the current heat sink density, D_{hs}. The blue line is when the heat sink density increases by a factor of 10 and the red line is when the density increases by a factor of 100. It can be seen that the volume almost saturates between the factor of 10 and 100 and the major contributor to volume at this stage is the transformer itself.

4.6 Summary

The knowledge covered in this chapter that contributes to the argument tree is demonstrated in Figure 4.12. The main points to take from this chapter are as follows,

- The DAB is a topology that is extremely versatile and the bridges can be modulated in many ways. This research covers PSM and TriM, and the volumetric approximations are based on the TriM scheme.
- The two major factors that contribute to volume in this model are the transformer core and the heat sink. The losses are larger in the DAB compared to the SPWM leading to larger heat sink requirements. The

heat sink contributes to the majority of the volume of the DAB in this model. Focus should be put into reducing the switching losses (which would lead to a smaller heat sink) before increasing the switching frequency (which would lead to a smaller transformer core).

- The major contributor to the loss in the DAB is the energy dissipated during the switch-on events of both bridges. This needs to be reduced in order to reduce the volume of the inverter.
- Even with ZVS, the switching losses are high due to the switch-on events mentioned in the previous point.

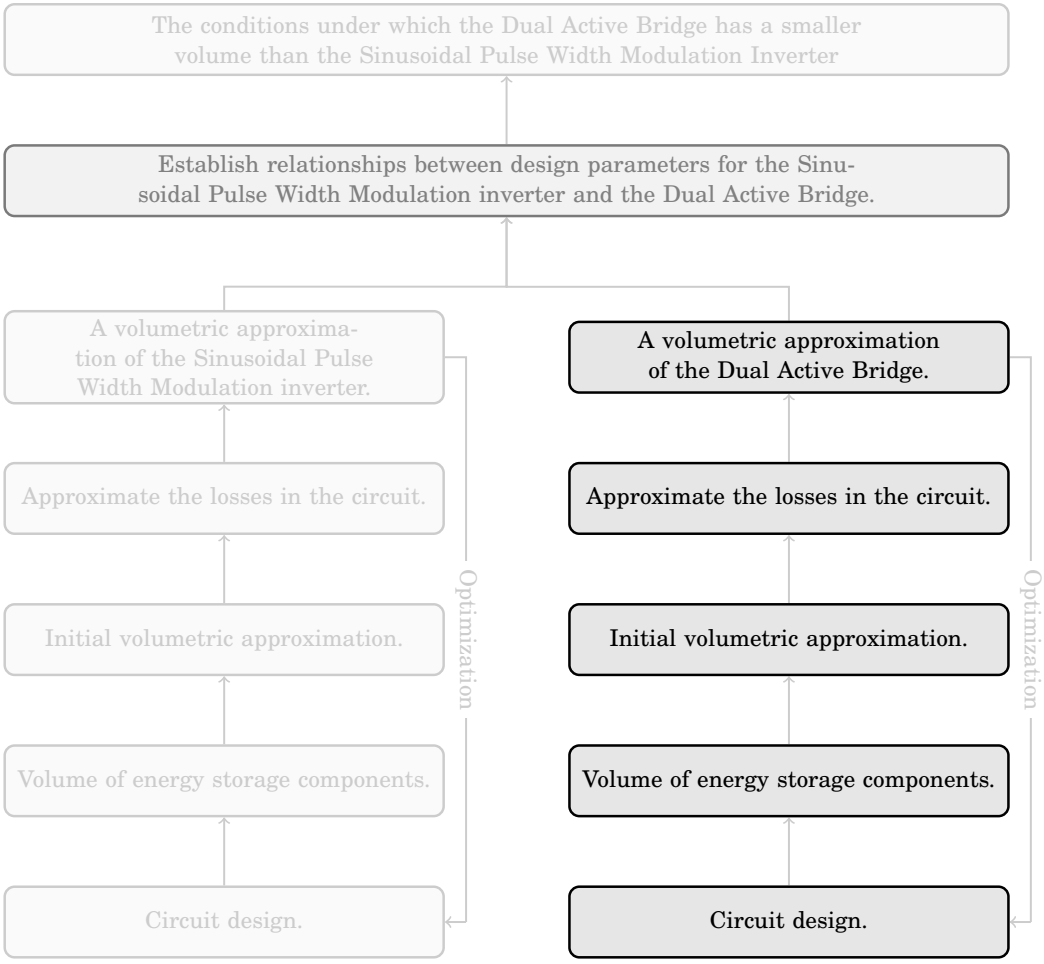


Figure 4.12: The contribution to the overall argument provided by Chapter 4.

Results, Research Conclusions, and Future Work 5

The volumetric comparison between the SPWM and DAB is demonstrated in Figure 5.1 below. It can be seen that, for this case study, the SPWM is volumetrically smaller than the DAB for all frequencies up to and including 72 kHz. The main reason for this is the difference in losses between these two topologies. The switching losses in the DAB are far more significant than the SPWM, and the transformer size does not compensate (at these frequencies) for the volume of the heat sink.

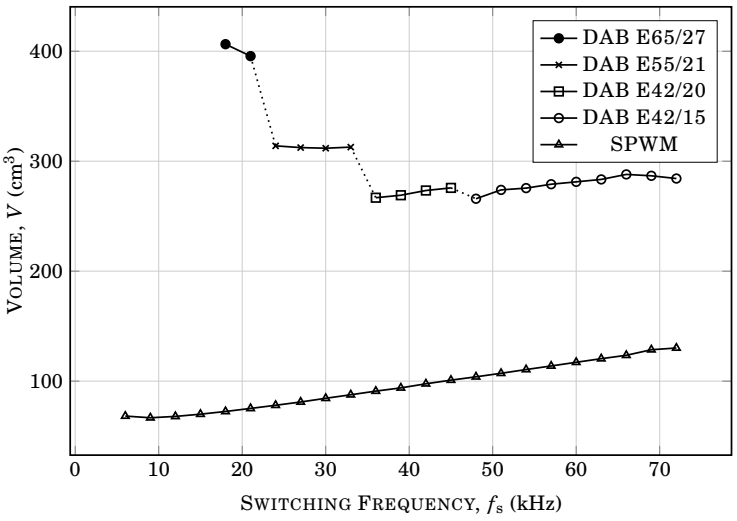


Figure 5.1: The comparison between the volumes of the SPWM and the DAB.

This means that the conditions under which the DAB is volumetrically smaller than the SPWM cannot be definitively specified based on the results found in this research. However, it can be concluded that the switching frequency, f_s, must be larger than 72 kHz in order for it to have the possibility of being smaller.

The methods that can be used to improve the power density of the SPWM are mentioned in Section 5.1 below. The improvements look at the implementation of the SPWM instead of the increase in switching frequency to increase power density. Increasing the accuracy of the volumetric approximation by considuring the winding volumes in inductors is also discussed in this section.

A number of conclusions can be drawn on the modulation technique that should be used in the DAB, and possible improvements that could be made around this discussion is presented in Section 5.2 below. Due to the scope of the research, additional topologies and configurations that could lead to smaller volumes were not investigated. This is because a volume for the standard DAB needed to be established before looking into more advanced configurations and schemes. The topologies that could lead to smaller volumes are discussed in Section 5.3 below.

5.1 Sinusoidal Pulse Width Modulation Techniques

The SPWM was implemented using open-loop control. In reality, a form of closed-loop control can be implemented to shape the waveform better and reduce THD. A closed-loop control system would introduce a lot of complexity into the SPWM model since switching times would be less predictable. This would, however, reduce the stress on the output filter meaning that the filter requirements could be reduced.

As mentioned in Section 2.3.2, the winding volume of the inductor is not considered in this research to reduce the complexity of the model. This is because ignoring the winding volume removes the need to consider core shape and the number of turns required when designing an inductor for the circuit. This

does, however, mean that the magnetic energy storage density of the inductor, W_{m}, in the models is higher than it would be in reality because the approximated volume is smaller when the windings are not considered. A trade-off between accuracy and complexity can be made here where the windings are considered which leads to a more accurate volumetric approximation of the inductor but a more complicated SPWM model.

5.2 Dual Active Bridge Modulation Techniques

Another conclusion can be drawn from this research regarding the DAB design, and that is on the modulation technique. Both PSM and TriM were used in this research as they are popular modulation techniques used in the DAB. PSM did not allow for ZVS for a large range of switching events and TriM has large switch-on event losses. When designing a DC-to-DC converter, these problems can be avoided. The choice of the turns ratio, n, would allow the effective voltages on either side of the transformer to remain very similar which means that ZVS would happen regularly. Sections 5.2.1 and 5.2.2 below outline the changes that could be made to improve the problems mentioned.

5.2.1 Extending Triangular Modulation

The PhD thesis by Dr Krismer [20] outlines the use of more complicated modulation schemes to achieve higher efficiencies. Krismer found the hard switching happening on the turn on events could be dealt with by extending the TriM scheme. Effectively, the currents are circulated during the switch-on events to enable ZVS. This is a trade-off between conduction losses and switching losses, and Krismer has found that this trade-off leads to higher efficiencies.

Referring to Figure 4.8 in the previous chapter, Krismer's extension of the TriM scheme can be explained. In the standard TriM scheme, the current should be relatively close to 0 A once switching has moved from S_1 to S_3. In other words, the current through the inductor between S_3 and S_4 is nearly 0 A. Krismer proposes that the current should not get close to 0 A between S_1 to S_3, but instead, it should rather stop at a current that would still allow for ZVS at the next switching event (refer to Equation (4.28)). This means that

the current between S_3 and S_4 would not be close to 0A, causing conduction losses, however, ZVS would occur at S_4 and this trade-off between conduction losses between S_3 and S_4 and ZVS at S_4 increases the efficiency of the converter.

5.2.2 Alternate Modulation Techniques

Krismer not only extends standard modulation techniques but also demonstrates that the DAB can be modulated in a number of different ways. In fact, since the input and output bridges can be controlled and pulsed in any way, one could conclude that there are a large number of ways that the DAB can be modulated. Dynamic schemes such as Space Vector Modulation (SVM) could be implemented where feedback is used to determine what the bridge should do next. Dynamic schemes could lead to changes such as,

- The time at which the input bridge and output bridges switch on.
- The length of time that each bridge is on for.
- The current flowing through the circuit when the bridges are switched off.
- The number of pulses from each bridge during a switching cycle.

5.3 Dual Active Bridge Topology

One of the benefits offered by the DAB is the isolation from the transformer. This allows for the input and output terminals to be connected in some way or for multiple DABs to be connected without grounding problems.

5.3.1 Partial Power Processing

As discussed in Section 2.2.2, a multi-stage approach such as Partial Power Processing could be used. PPP involves the use of a direct link between the input and output terminal in order to allow the free flow of energy without it being processed first [42]. Figure 5.2 is a demonstration of what the DAB would look like in the PPP configuration.

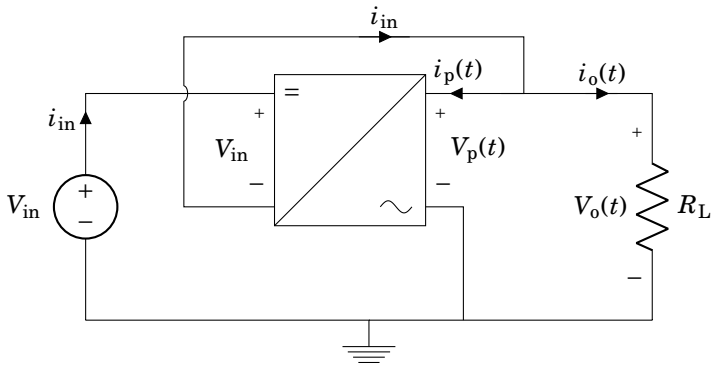


Figure 5.2: Generalised Partial Power Processing Black Box System where The Output Signal is AC.

The application of this topology has not been applied in this research, however, it has been listed here as a possible method to reduce the losses in the circuit. This is because the power processed is no longer the input power, it is the difference between the input power and the output power which reduces the amount of energy undergoing the conversion process.

5.3.2 Multi-Level Design

By connecting DABs in a topology similar to that of Figure 5.3, the load can be spread over each of the DABs in the string. As described in Section 2.2.1, this could potentially lead to a reduction in volume because of the exponential relationship between the number of cells and the overall volume.

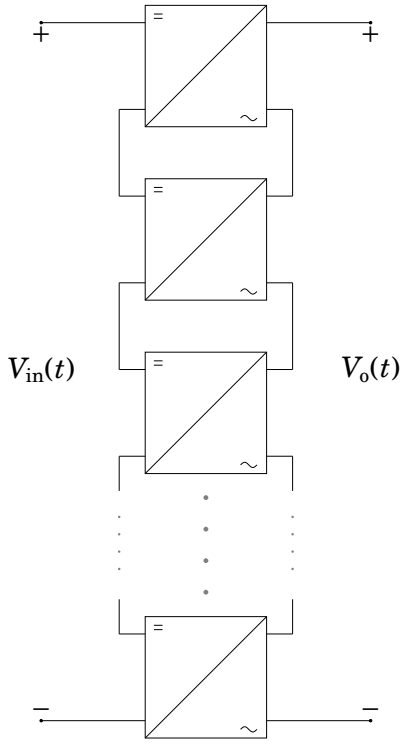


Figure 5.3: A potential topology that could be used to create a multicellular DAB inverter.

5.4 Summary

The details in this section lead to the conclusion in the argument tree demonstrated in Figure 5.4 below. Although the conditions cannot be definitively stated, it has been established that switching frequencies less than and equal to 72 kHz do not lead to volumetrically smaller DAB inverters. The knowledge established in this section is summarised as follows,

- The DAB using TriM is not smaller than the SPWM for switching frequencies less than or equal to 72 kHz.
- The switch-on events for the DAB are major contributors to the loss in the circuit, and this problem could be solved using alternate modulation techniques. Krismer presents possible solutions to this problem by trading off conduction losses with switching losses [20].
- It is possible that the application of a dynamic modulation scheme such as SVM could lead to a reduction in losses since the *cost* of the optimisation equation could focus on the power losses in the circuit. In this way,

it is likely that the modulation scheme would aim to ensure ZVS would take place where ever possible.

- The use of different DAB topologies could lead to a reduction in the losses and volume of the inverter. An example given in this chapter is the use of PPP which would only process the difference between the input and output power as opposed to the input power.
- The use of multi-level topologies could lead to a reduction in the volume of the inverter due to the scaling relationship defined by Kasper, Bortis, and Kolar [16].

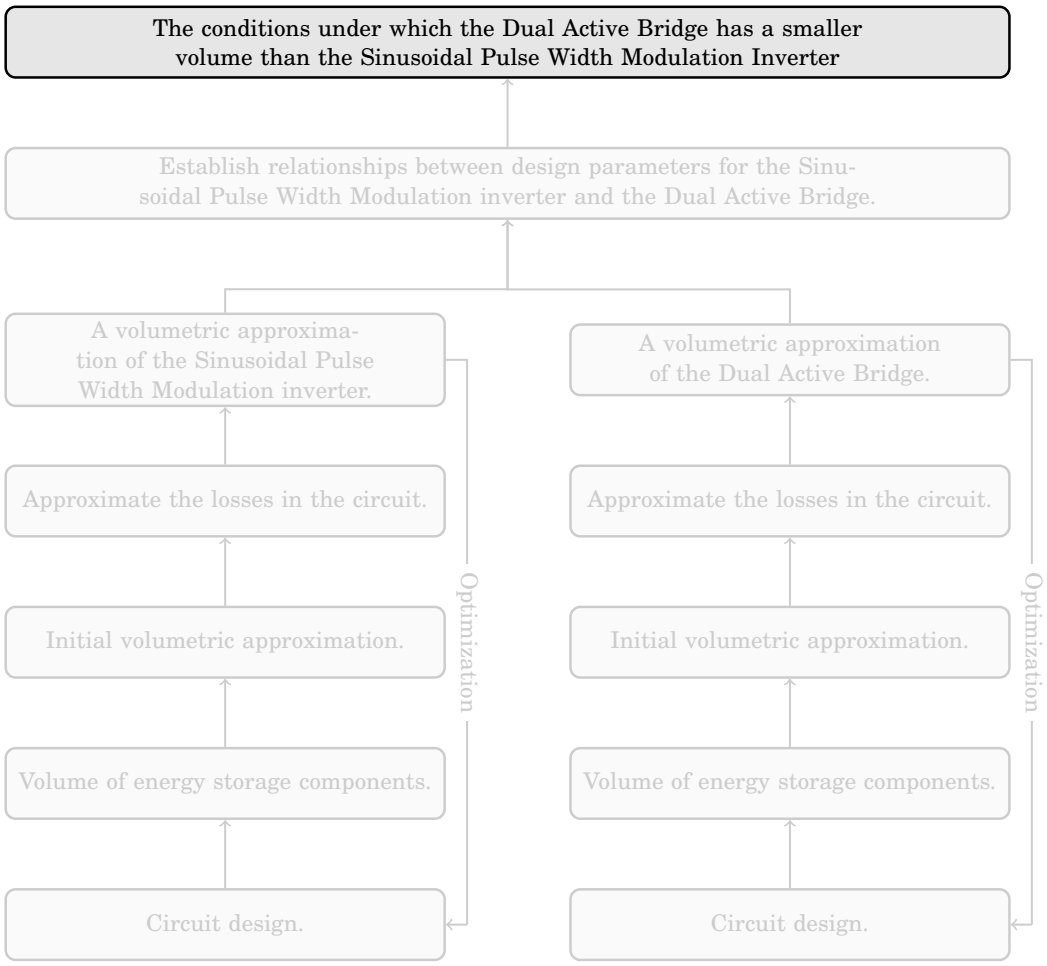


Figure 5.4: The contribution to the overall argument provided by Chapter 5.

Conclusion 6

The research conducted investigates the DAB under a case study for the GLBC. It has been found that the DAB can be used as a DC-to-AC converter, however, there are trade-offs and additional complexities that must be considered. The investigation on the effect of high-frequency switching, ZVS, and the use of a topology aside from the SPWM was conducted and conclusions are made in Chapter 5.

Future work and improvements are also discussed in Chapter 5, where suggestions on widening the scope of the DAB may lead to increases in power density and reductions in losses. These improvements do, however, increase the complexity of the circuit and there are too many possibilities to cover in this research.

6.1 Case Study Conclusion

The use of the DAB as an inverter was investigated as a replacement for the SPWM. The volume of the SPWM was found to decrease between 6 kHz and 12 kHz and only increase after this point. The volume of the DAB was found to decrease as the switching frequency increased. Although the volumes were found to perform oppositely, the SPWM was found to have a smaller volume at all switching frequencies investigated in this research. The frequencies investigated in this research were up to and including 72 kHz, after this point, the SPWM model begins to require unrealistic switching pulses that are below

rise and fall times of standard MOSFETs.

As discussed in Chapter 5, there are a number of conclusions that can be drawn around the DAB. One of the main conclusions is that the switching loss for the DAB in an inverter topology is too high when using modulation techniques like PSM and TriM. The modulation technique must be modified to ensure that ZVS takes place as much as possible, especially during the switch-on events as these cause the largest switching losses in the circuit.

Another alternative to decreasing the DAB is using a multi-stage or multi-cellular connection strategy to reduce the losses and volume of the circuit. These techniques were mentioned in Sections 2.2.1 and 2.2.2 and their applications using the DAB were summarised in Chapter 5.

In the case study presented in this research, a 2 kW inverter with an input voltage of 450 V and an output RMS voltage of 240 V at 60 Hz (see Table 2.2) was modelled. The DAB has been found to have a lower power density than the SPWM for frequencies below 72 kHz. This is not to say that the DAB will always have a lower power density than the SPWM. In fact, the trend of the DAB volume is to decrease as the switching frequency increases. The DAB can run at frequencies higher than 72 kHz, whereas, the SPWM begins to reach limits at this point. It can, therefore, be concluded that for an inverter that meets the requirements specified in Table 2.2, higher power densities cannot be achieved using a DAB when TriM is used in conjunction with the waveform model in Chapter 4 and switching frequencies under 72 kHz. The SPWM should be used at a switching frequency around 9 kHz or further investigations should be done around the DAB at frequencies higher than 72 kHz to find if and when the volume is below that of the SPWM.

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Kepler's Equation A

The SPWM waveform is defined as,

$$\boldsymbol{V}_{\mathrm{SPWM}}(t) = \boldsymbol{V}_{\mathrm{A}}(t) - \boldsymbol{V}_{\mathrm{B}}(t)$$

In order to find $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$, accurate intercept times need to be found between the output waveform,

$$\boldsymbol{V}_{\mathrm{o}}(t) = V_{\mathrm{o(p)}} \sin(2\pi f_{\mathrm{o}} t) \tag{A.1}$$

and the straight lines defined in Equations (3.5) and (3.6) (where $V_{\mathrm{o(p)}}$ is peak sinusoidal output voltage). In other words, the equations below need to be solved,

$$4V_{\mathrm{in}} f_{\mathrm{s}} t - V_{\mathrm{in}}(4k+1) = V_{\mathrm{o(p)}} \sin(2\pi f_{\mathrm{o}} t) \tag{A.2}$$

$$-4V_{\mathrm{in}} f_{\mathrm{s}} t + V_{\mathrm{in}}(3+4k) = V_{\mathrm{o(p)}} \sin(2\pi f_{\mathrm{o}} t) \tag{A.3}$$

In order to allow for a generic model, a modulation index, m, can be defined as,

$$m = \frac{V_{\mathrm{o(p)}}}{V_{\mathrm{in}}} \tag{A.4}$$

In order to solve these intercept times, Kepler's Equation is used. Kepler's Equation is defined as,

$$M = E - e \sin(E) \tag{A.5}$$

Kepler would use this equation for applications in celestial mechanics and approximations to the solution of this equation exist. Bessel provided a solution to finding E using the following equation [1],

$$E = M + \sum_{n=1}^{n=\infty} \frac{2}{n} \boldsymbol{J_n}(ne)\sin(nM) \tag{A.6}$$

where $\boldsymbol{J_n}(x)$ is Bessel Function of the First Kind.

The derivation to relate Equation (A.5) to Equation (A.2) is completed in the following way,

$$\begin{aligned} 4V_{\text{in}}f_{\text{s}}t - V_{\text{in}}(4k+1) &= mV_{\text{in}}\sin(2\pi f_{\text{o}}t) \\ t - \frac{4k+1}{4f_{\text{s}}} &= \frac{m}{4f_{\text{s}}}\sin(2\pi f_{\text{o}}t) \\ \frac{4k+1}{4f_{\text{s}}} &= t - \frac{m}{4f_{\text{s}}}\sin(2\pi f_{\text{o}}t) \\ \frac{\pi f_{\text{o}}(4k+1)}{2f_{\text{s}}} &= 2\pi f_{\text{o}}t - \frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\sin(2\pi f_{\text{o}}t) \end{aligned} \tag{A.7}$$

Comparing Equation (A.7) to Equation (A.5) the following is apparent,

$$M = \frac{\pi f_{\text{o}}(4k+1)}{2f_{\text{s}}} \tag{A.8}$$

$$E = 2\pi f_{\text{o}}t \tag{A.9}$$

$$e = \frac{m\pi f_{\text{o}}}{2f_{\text{s}}} \tag{A.10}$$

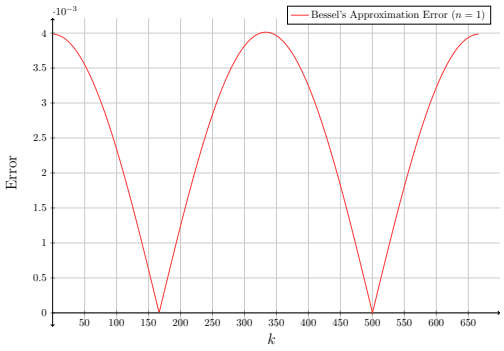
Substituting these values into Bessel's approximation function (Equation (A.6)) it is found that the time intercepts occur at,

$$\boldsymbol{T}_{\text{Pp}}(k) = \frac{(4k+1)}{4f_{\text{s}}} + \frac{1}{2\pi f_{\text{o}}}\sum_{n=1}^{\infty}\frac{2}{n}\boldsymbol{J_n}\left(n\frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\right)\sin\left(n\frac{\pi f_{\text{o}}(4k+1)}{2f_{\text{s}}}\right) \tag{A.11}$$

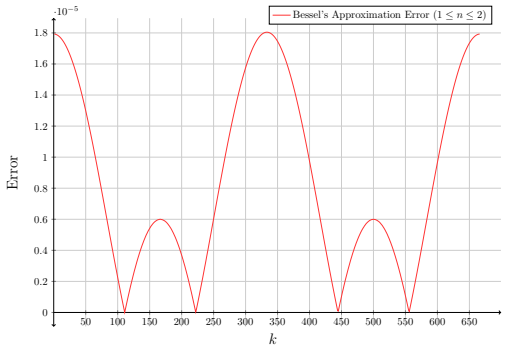
Where $T_{\text{pp}}(k)$ can be described as the time intercept of the positive control waveform with the k^{th} positive line in the sawtooth waveform. The intercept times are solved by setting $k = 0, \ldots, \frac{f_{\text{s}}}{f}$. As the number of terms used in Bessel's approximation increases, the overall error decreases. At a switching frequency of 20 kHz and a DC input of 400 V, the error as the number of terms increases is demonstrated in Figure A.1 below. The error is normalised using the following equation,

$$\boldsymbol{e}(t,k) = \left| \frac{\boldsymbol{V}_{\mathrm{o}}(t) - \boldsymbol{T}_{\mathrm{p}}(t,k)}{\boldsymbol{V}_{\mathrm{o}}(t)} \right| \tag{A.12}$$

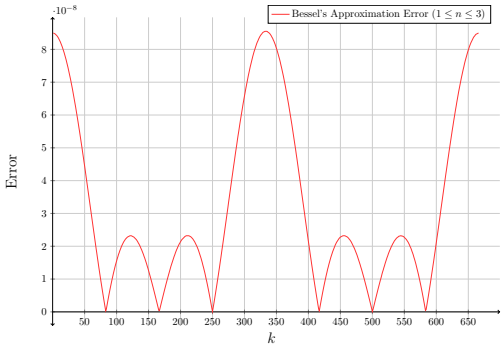
It can be seen from Figure A.1d that the error is in the order of 10^{-10} when $n = 1, \cdots, 4$. Since $10^{-8}\%$ is extremely small, it will be regarded as negligible.



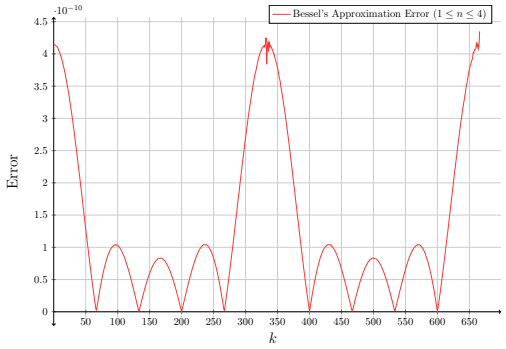
(a) Single Term used in Approximation.



(b) Two Terms used in Approximation.



(c) Three Terms used in Approximation.



(d) Four Terms used in Approximation.

Figure A.1: The error in Bessel's approximation of Kepler's Function as n (the number of terms in the approximation) increases.

Calculating the intercepts for the negative lines (Equation (3.6)) works in very much the same way. Although, it is stated that Bessel's Approximation converges when $0 \leq e \leq 1$, it has been found that convergence still occurs for $0 \leq |e| \leq 1$. This means that the intercept times for the negative lines can be found using the following derivation,

$$-4V_{\text{in}}f_{\text{s}}t + V_{\text{in}}(3+4k) = mV_{\text{in}}\sin(2\pi f_{\text{o}}t)$$
$$V_{\text{in}}(3+4k) = 4V_{\text{in}}f_{\text{s}}t + mV_{\text{in}}\sin(2\pi f_{\text{o}}t)$$
$$\frac{3+4k}{4f_{\text{s}}} = t + \frac{m}{4f_{\text{s}}}\sin(2\pi f_{\text{o}}t)$$
$$\frac{\pi f_{\text{o}}(3+4k)}{2f_{\text{s}}} = 2\pi f_{\text{o}}t + \frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\sin(2\pi f_{\text{o}}t) \tag{A.13}$$

Comparing Equation (A.13) to Equation (A.5) the following terms are found,

$$M = \frac{\pi f_{\text{o}}(3+4k)}{2f_{\text{s}}} \tag{A.14}$$

$$E = 2\pi f_{\text{o}}t \tag{A.15}$$

$$e = -\frac{m\pi f_{\text{o}}}{2f_{\text{s}}} \tag{A.16}$$

From these terms above, the negative intercept times can be approximated using,

$$\boldsymbol{T}_{\text{Pn}}(k) = \frac{3+4k}{4f_{\text{s}}} + \frac{1}{2\pi f_{\text{o}}}\sum_{n=1}^{\infty}\frac{2}{n}\boldsymbol{J_n}\left(-n\frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\right)\sin\left(n\frac{\pi f_{\text{o}}(3+4k)}{2f_{\text{s}}}\right) \tag{A.17}$$

For the negative control signal, the intercept times for the positive lines are calculated using,

$$\boldsymbol{T}_{\text{Np}}(k) = \frac{4k+1}{4f_{\text{s}}} + \frac{1}{2\pi f_{\text{o}}}\sum_{n=1}^{\infty}\frac{2}{n}\boldsymbol{J_n}\left(-n\frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\right)\sin\left(n\frac{\pi f_{\text{o}}(4k+1)}{2f_{\text{s}}}\right) \tag{A.18}$$

and for the negative lines the intercept times are calculated using,

$$\boldsymbol{T}_{\text{Nn}}(k) = \frac{3+4k}{4f_{\text{s}}} + \frac{1}{2\pi f_{\text{o}}}\sum_{n=1}^{\infty}\frac{2}{n}\boldsymbol{J_n}\left(n\frac{m\pi f_{\text{o}}}{2f_{\text{s}}}\right)\sin\left(n\frac{\pi f_{\text{o}}(3+4k)}{2f_{\text{s}}}\right) \tag{A.19}$$

The SPWM waveform can be defined using Equations (A.11) and (A.17) to (A.19) in the following way,

$$\boldsymbol{V}_{\text{A}}(t) = V_{\text{in}}\sum_{k=0}^{k=\frac{f_{\text{s}}}{f}}\left(\boldsymbol{u}_{\text{s}}(t-\boldsymbol{T}_{\text{Pn}}(k)) - \boldsymbol{u}_{\text{s}}(t-\boldsymbol{T}_{\text{Pp}}(k))\right) \tag{A.20}$$

$$\boldsymbol{V}_{\text{B}}(t) = V_{\text{in}}\sum_{k=0}^{k=\frac{f_{\text{s}}}{f}}\left(\boldsymbol{u}_{\text{s}}(t-\boldsymbol{T}_{\text{Nn}}(k)) - \boldsymbol{u}_{\text{s}}(t-\boldsymbol{T}_{\text{Np}}(k))\right) \tag{A.21}$$

Combining these equations leads to the function,

$$\boldsymbol{V}_{\mathrm{SPWM}}(t) = V_{\mathrm{in}} \sum_{k=0}^{k=\frac{f_{\mathrm{s}}}{f}} \Big(\boldsymbol{u}_{\mathrm{s}}(t - \boldsymbol{T}_{\mathrm{Pn}}(k)) - \boldsymbol{u}_{\mathrm{s}}(t - \boldsymbol{T}_{\mathrm{Pp}}(k)) + \boldsymbol{u}_{\mathrm{s}}(t - \boldsymbol{T}_{\mathrm{Np}}(k)) - \boldsymbol{u}_{\mathrm{s}}(t - \boldsymbol{T}_{\mathrm{Nn}}(k)) \Big) \tag{A.22}$$

This equation represents an ideal SPWM waveform that utilises Kepler's equation to calculate the intercept points numerically. From this, the $\boldsymbol{V}_{\mathrm{SPWM}}(t)$ equation can used in the transfer characteristic of the filter to calculate the output waveform. This forumla is what is used in this research to model the output waveform and switching losses of the SPWM.

A.1 The Fourier Series

The Fourier Series of the SPWM waveform is calculated using the switching times calculated in Appendix A. The Fourier Series form used for this application is,

$$f(t) = a_0 + \sum_{n=1}^{n=\infty} a_n \cos(2\pi f_{\mathrm{o}} n t) + \sum_{n=1}^{n=\infty} b_n \sin(2\pi f_{\mathrm{o}} n t) \tag{A.23}$$

and,

$$a_0 = \frac{1}{T} \int_0^T f(t)\, \mathrm{d}t \tag{A.24}$$

$$a_n = \frac{1}{2T} \int_0^T f(t) \cos(2\pi f_{\mathrm{o}} n t)\, \mathrm{d}t \tag{A.25}$$

$$b_n = \frac{1}{2T} \int_0^T f(t) \sin(2\pi f_{\mathrm{o}} n t)\, \mathrm{d}t \tag{A.26}$$

Since the SPWM output is the combination of $\boldsymbol{V}_{\mathrm{A}}(t)$ and $\boldsymbol{V}_{\mathrm{B}}(t)$, it can be written as the difference between the individual Fourier Series of each of these waveforms. Additionally, it is known that the SPWM signal is symmetric about the t axis which implies that a_0 = 0V (there is no DC offset). After defining the following functions:

$\boldsymbol{T}_{\mathrm{Pp}}(k)$ The intercept time between the positive control signal and the line k with a positive gradient.

$\boldsymbol{T}_{\mathrm{Pn}}(k)$ The intercept time between the negative control signal and the line k with a positive gradient.

$\boldsymbol{T}_{\mathrm{Np}}(k)$ The intercept time between the positive control signal and the line k with a negative gradient.

$\boldsymbol{T}_{\mathrm{Nn}}(k)$ The intercept time between the negative control signal and the line k with a negative gradient.

The Fourier Coefficients for $\boldsymbol{V}_{\mathrm{A}}(t)$ can be calculated as follows,

$$\begin{aligned} a_{\mathrm{A},n} &= \frac{1}{2T}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\int_{\boldsymbol{T}_{\mathrm{Np}}(k)}^{\boldsymbol{T}_{\mathrm{Pp}}(k+1)} V_{\mathrm{in}}\cos(2\pi f_{\mathrm{o}} n t)\,\mathrm{d}t \\ &= \frac{V_{\mathrm{in}}}{4\pi n}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\left(\sin(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Pp}}(k+1)) - \sin(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Np}}(k))\right) \end{aligned} \tag{A.27}$$

$$\begin{aligned} b_{\mathrm{A},n} &= \frac{1}{2T}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\int_{\boldsymbol{T}_{\mathrm{Np}}(k)}^{\boldsymbol{T}_{\mathrm{Pp}}(k+1)} V_{\mathrm{in}}\sin(2\pi f_{\mathrm{o}} n t)\,\mathrm{d}t \\ &= \frac{V_{\mathrm{in}}}{4\pi n}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\left(\cos(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Np}}(k)) - \cos(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Pp}}(k+1))\right) \end{aligned} \tag{A.28}$$

And the Coefficients for $\boldsymbol{V}_{\mathrm{B}}(t)$,

$$\begin{aligned} a_{\mathrm{B},n} &= \frac{1}{2T}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\int_{T_{\mathrm{pN}}(k)}^{\boldsymbol{T}_{\mathrm{Nn}}(k+1)} V_{\mathrm{in}}\cos(2\pi f_{\mathrm{o}} n t)\,\mathrm{d}t \\ &= \frac{V_{\mathrm{in}}}{4\pi n}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}} V_{\mathrm{in}}\left(\sin(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Pn}}(k+1)) - \sin(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Nn}}(k+1))\right) \end{aligned} \tag{A.29}$$

$$\begin{aligned} b_{\mathrm{B},n} &= \frac{1}{2T}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\int_{T_{\mathrm{pN}}(k)}^{\boldsymbol{T}_{\mathrm{Nn}}(k+1)} V_{\mathrm{in}}\sin(2\pi f_{\mathrm{o}} n t)\,\mathrm{d}t \\ &= \frac{V_{\mathrm{in}}}{4\pi n}\sum_{k=0}^{\frac{f_{\mathrm{s}}}{f}}\left(\cos(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Pn}}(k)) - \cos(2\pi f_{\mathrm{o}} n \boldsymbol{T}_{\mathrm{Nn}}(k+1))\right) \end{aligned} \tag{A.30}$$

The Fourier Series for the final SPWM output is, therefore,

$$\boldsymbol{V}_{\mathrm{out}}(t) = \sum_{n=1}^{n=\infty}(a_{\mathrm{A},n} - a_{\mathrm{B},n})\cos(2\pi f_{\mathrm{o}} n t) + \sum_{n=1}^{n=\infty}(b_{\mathrm{A},n} - b_{\mathrm{B},n})\sin(2\pi f_{\mathrm{o}} n t) \tag{A.31}$$

The alternative to this is to use the double Fourier Series presented by Holmes and Lipo [2].

Conclusion

The effects of each filter can be tested on the Fourier Series demonstrated in Equation (A.31) above and after applying the filter transfer characteristic, the THD can be calculated.

This Appendix demonstrates the use of Kepler's equation to approximate the switching points for the SPWM. These approximations have low errors and allow for numerical approximations of intercept times during simulations. A Fourier Series method can be used over this method and is presented in work performed by Holmes and Lipo [2].

References

[1] P. Colwell, "Bessel Functions and Kepler's Equation", *The American Mathematical Monthly*, vol. 99, no. 1, p. 45, 1992, ISSN: 00029890. DOI: 10.2307/2324547.

[2] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003.

Sinusoidal Pulse Width Modulation Simulation Setup B

The simulations run in Chapter 3 follow the Google Little Box Challenge specifications. The simulations were run in LTspice XVII using the IRFP460 MOSFET as the switch and the circuit was configured to match Figure 2.1. Internal losses due to the inductor and capacitor were ignored for the simulation. The IR2110 was used to drive each phase arm to create more realistic input pulses into the gates of the MOSFETs. Connecting an ideal voltage source directly to the gate caused a reduction in the Miller effect which changed the waveforms demonstrated in Figure 3.13. Instead of a delay between the switching events of the voltage and current waveforms, the waveforms overlapped which decreased the overall loss of the switch-off events.

The modulation technique used to drive the H Bridge is defined in Figure 3.11. The simulated loss, P_{sim}, is calculated by taking the average product of the current and voltage waveforms over the switches and adding them together. In mathematical terms,

$$\begin{aligned} P_{Q_1(\text{sim})} &= \langle \boldsymbol{i}_{Q_1}(t)\boldsymbol{v}_{Q_1}(t)\rangle \\ P_{Q_2(\text{sim})} &= \langle \boldsymbol{i}_{Q_2}(t)\boldsymbol{v}_{Q_2}(t)\rangle \\ P_{Q_4(\text{sim})} &= \langle \boldsymbol{i}_{Q_4}(t)\boldsymbol{v}_{Q_4}(t)\rangle \end{aligned} \tag{B.1}$$

are added together to find,

$$P_{\text{sim}} = P_{Q_1(\text{sim})} + P_{Q_2(\text{sim})} + P_{Q_3(\text{sim})} \tag{B.2}$$

In all cases, $\boldsymbol{i}_{Q_k}(t)$, is the current flowing through the switch, $\boldsymbol{v}_{Q_k}(t)$, is the voltage across the switch, and $P_{Q_k(\text{sim})}$, is the average power dissipated by the switch, where $k \in \mathbb{Z}$.

Figure B.1 below demonstrates the circuit used to simulate the SPWM. Figure B.2 is an example of the output waveforms in the SPWM simulations. When the pulsed waveform in Figure B.2a is put across the LC filter, there is a sinusoidal voltage output over the load resistance as shown in Figure B.2b. The current through the inductor has high-frequency ripple which is filtered out through the capacitor leading to a smooth current over the load resistor, as shown in Figure B.2c.

Conclusion

The simulations demonstrated in this Appendix are used to compare the approximated switching losses to those that are simulated. Figure B.2 demonstrates the simulated SPWM waveform and the output voltage and it can be seen that the sinusoidal output of 60 Hz and $240\sqrt{2}$V is achieved.

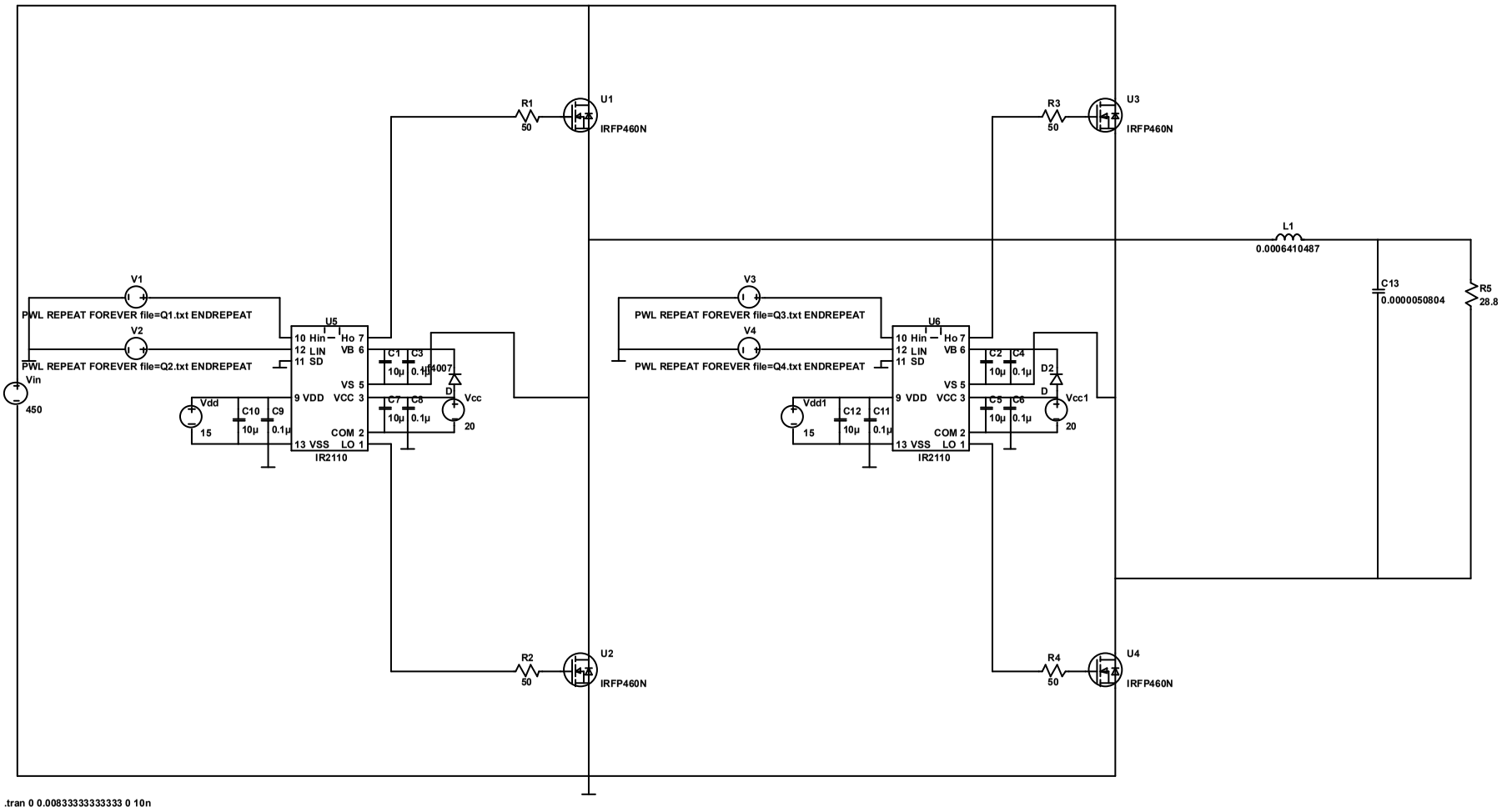
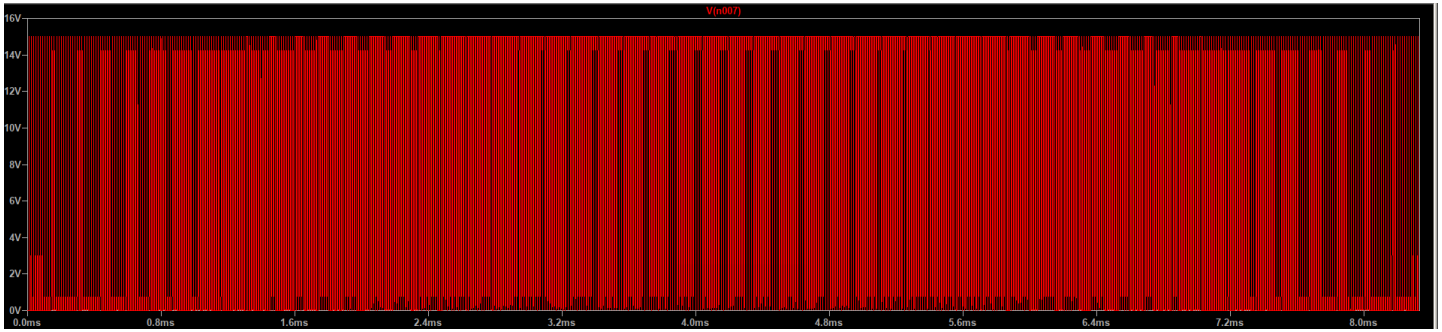
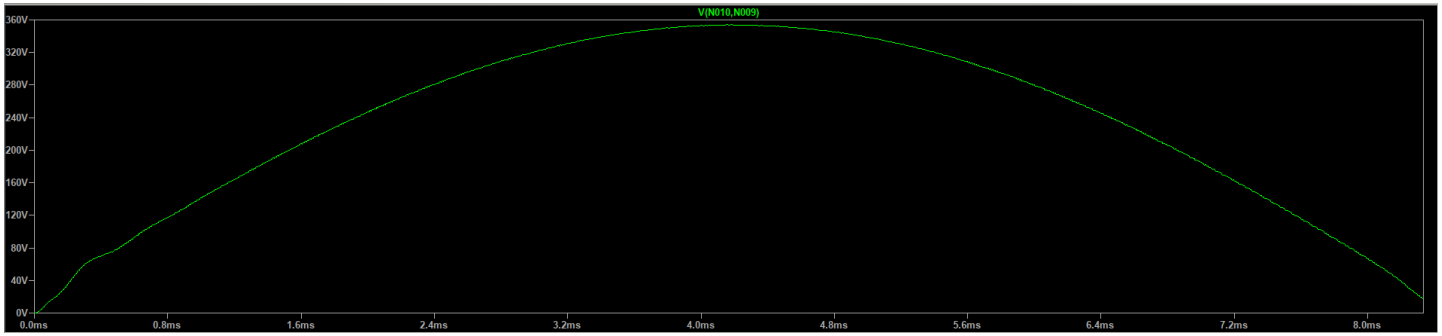


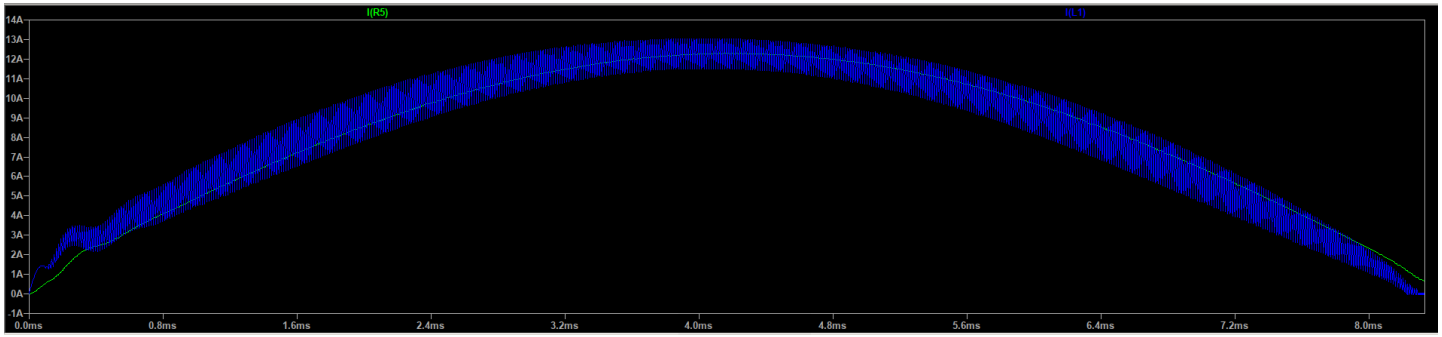
Figure B.1: The SPWM circuit used in LTspice XVII for simulations. The IR2110 drivers are used to drive IRFP460N MOSFETS. These are connected to an LC filter which, finally, connects to the load resistance, R.



(a) The voltage output across the LC filter in the SPWM.



(b) The output voltage over the load resistance.



(c) The current through the filter inductor, L (blue), and through the load resistance, R (green).

Figure B.2: The waveforms seen when simulating the SPWM LTspice XVII models.

E-Core Transformer Size Requirements in Dual Active Bridge C

Different E-core sizes can be used when designing the DAB. Ideally, the smallest core for the required switching frequency should be chosen. Table C.1 demonstrates the required number of turns, wire thickness, and other factors that influence the required core size. The percentage difference between the area that the core provides for winding and the actual winding area required is calculated and the core with the smallest positive percentage difference is chosen.

In Table C.1, A_{e} is the area of the winding window, f_{s} is the switching frequency that the DAB would be running at, N is the required number of turns for this switching frequency, A_{w} is the cross-sectional area of the wire required (this is achieved by using multiple strands of wire to reach this total area), C_{w} is the approximated circumference of a single loop or winding, l_{w} is the approximate total length of wire required to get N windings and A_{req} is the required winding area given the number of turns and the width of the wire. The “Diff” column shows the percentage difference between the actual winding area and the required winding area.

Conclusion

Table C.1 demonstrates the effective use of the winding window for different E-core configurations and parameters. When designing for a specific switching frequency, f_s, this table is used to determine which E-core best suits the circuit. This is then chosen as the core to use for that circuit design.

Table C.1: The comparison between the area for wires in an E-core and the required winding area given the peak current at each switching frequency. The difference between these two areas is calculated and the scenarios where the requirements are not met are marked in red.

Core	A_e	f_s	N	A_w	C_w	l_w	A_{req}	Diff
	mm^2	kHz	turns	mm^2	mm	m	mm^2	%
E13/4	55.7	18	2282	12.38	26.4	60.2	28260.8	-50656
E13/4	55.7	24	1711	10.62	26.4	45.2	18167.8	-32529
E13/4	55.7	30	1369	9.59	26.4	36.1	13128.1	-23478
E13/4	55.7	36	1141	8.73	26.4	30.1	9958.9	-17786
E13/4	55.7	42	978	8.05	26.4	25.8	7870.1	-14034
E13/4	55.7	48	856	7.59	26.4	22.6	6497.2	-11569
E13/4	55.7	54	761	7.06	26.4	20.1	5369.3	-9543
E13/4	55.7	60	685	6.78	26.4	18.1	4646.4	-8245
E13/4	55.7	66	623	6.43	26.4	16.4	4004.1	-7091
E13/4	55.7	72	571	6.18	26.4	15.1	3530.4	-6241
E16/5	89.1	18	1415	12.38	33.4	47.3	17523.7	-19576
E16/5	89.1	24	1061	10.62	33.4	35.4	11265.9	-12550
E16/5	89.1	30	849	9.59	33.4	28.4	8141.5	-9042
E16/5	89.1	36	708	8.73	33.4	23.6	6179.6	-6839
E16/5	89.1	42	607	8.05	33.4	20.3	4884.6	-5385
E16/5	89.1	48	531	7.59	33.4	17.7	4030.4	-4425
E16/5	89.1	54	472	7.06	33.4	15.8	3330.2	-3639
E16/5	89.1	60	425	6.78	33.4	14.2	2882.8	-3137
E16/5	89.1	66	386	6.43	33.4	12.9	2480.9	-2686

Core	A_e	f_s	N	A_w	C_w	l_w	A_{req}	Diff
	mm^2	kHz	turns	mm^2	mm	m	mm^2	%
E16/5	89.1	72	354	6.18	33.4	11.8	2188.7	-2358
E20/6	134.7	18	898	12.38	41.8	37.5	11121.0	-8157
E20/6	134.7	24	674	10.62	41.8	28.2	7156.7	-5214
E20/6	134.7	30	539	9.59	41.8	22.5	5168.8	-3738
E20/6	134.7	36	449	8.73	41.8	18.8	3919.0	-2810
E20/6	134.7	42	385	8.05	41.8	16.1	3098.1	-2200
E20/6	134.7	48	337	7.59	41.8	14.1	2557.9	-1799
E20/6	134.7	54	300	7.06	41.8	12.5	2116.7	-1472
E20/6	134.7	60	270	6.78	41.8	11.3	1831.4	-1260
E20/6	134.7	66	245	6.43	41.8	10.2	1574.6	-1069
E20/6	134.7	72	225	6.18	41.8	9.4	1391.2	-933
E25/7	193.2	18	556	12.38	51.0	28.4	6885.6	-3464
E25/7	193.2	24	417	10.62	51.0	21.3	4427.8	-2192
E25/7	193.2	30	334	9.59	51.0	17.0	3202.9	-1558
E25/7	193.2	36	278	8.73	51.0	14.2	2426.4	-1156
E25/7	193.2	42	238	8.05	51.0	12.1	1915.2	-891
E25/7	193.2	48	209	7.59	51.0	10.7	1586.4	-721
E25/7	193.2	54	186	7.06	51.0	9.5	1312.3	-579
E25/7	193.2	60	167	6.78	51.0	8.5	1132.8	-486
E25/7	193.2	66	152	6.43	51.0	7.8	976.9	-406
E25/7	193.2	72	139	6.18	51.0	7.1	859.4	-345
E32/19	342.2	18	347	12.38	67.0	23.2	4297.3	-1156
E32/19	342.2	24	260	10.62	67.0	17.4	2760.7	-707
E32/19	342.2	30	208	9.59	67.0	13.9	1994.6	-483
E32/19	342.2	36	174	8.73	67.0	11.7	1518.7	-344
E32/19	342.2	42	149	8.05	67.0	10.0	1199.0	-250
E32/19	342.2	48	130	7.59	67.0	8.7	986.7	-188
E32/19	342.2	54	116	7.06	67.0	7.8	818.4	-139
E32/19	342.2	60	104	6.78	67.0	7.0	705.4	-106
E32/19	342.2	66	95	6.43	67.0	6.4	610.6	-78
E32/19	342.2	72	87	6.18	67.0	5.8	537.9	-57
E42/15	589.0	18	174	12.38	92.0	16.0	2154.9	-266
E42/15	589.0	24	131	10.62	92.0	12.1	1391.0	-136

Core	A_e	f_s	N	A_w	C_w	l_w	A_{req}	Diff
	mm^2	kHz	turns	mm^2	mm	m	mm^2	%
E42/15	589.0	30	105	9.59	92.0	9.7	1006.9	-71
E42/15	589.0	36	87	8.73	92.0	8.0	759.4	-29
E42/15	589.0	42	75	8.05	92.0	6.9	603.5	-2
E42/15	589.0	48	66	7.59	92.0	6.1	501.0	15
E42/15	589.0	54	58	7.06	92.0	5.3	409.2	31
E42/15	589.0	60	53	6.78	92.0	4.9	359.5	39
E42/15	589.0	66	48	6.43	92.0	4.4	308.5	48
E42/15	589.0	72	44	6.18	92.0	4.0	272.0	54
E42/20	589.0	18	131	12.38	102.0	13.4	1622.3	-175
E42/20	589.0	24	98	10.62	102.0	10.0	1040.6	-77
E42/20	589.0	30	79	9.59	102.0	8.1	757.6	-29
E42/20	589.0	36	66	8.73	102.0	6.7	576.1	2
E42/20	589.0	42	56	8.05	102.0	5.7	450.6	23
E42/20	589.0	48	49	7.59	102.0	5.0	371.9	37
E42/20	589.0	54	44	7.06	102.0	4.5	310.4	47
E42/20	589.0	60	40	6.78	102.0	4.1	271.3	54
E42/20	589.0	66	36	6.43	102.0	3.7	231.4	61
E42/20	589.0	72	33	6.18	102.0	3.4	204.0	65
E55/21	849.2	18	88	12.38	120.0	10.6	1089.8	-28
E55/21	849.2	24	66	10.62	120.0	7.9	700.8	17
E55/21	849.2	30	53	9.59	120.0	6.4	508.2	40
E55/21	849.2	36	44	8.73	120.0	5.3	384.0	55
E55/21	849.2	42	38	8.05	120.0	4.6	305.8	64
E55/21	849.2	48	33	7.59	120.0	4.0	250.5	71
E55/21	849.2	54	30	7.06	120.0	3.6	211.7	75
E55/21	849.2	60	27	6.78	120.0	3.2	183.1	78
E55/21	849.2	66	24	6.43	120.0	2.9	154.3	82
E55/21	849.2	72	22	6.18	120.0	2.6	136.0	84
E55/25	849.2	18	74	12.38	128.0	9.5	916.4	-8
E55/25	849.2	24	56	10.62	128.0	7.2	594.6	30
E55/25	849.2	30	45	9.59	128.0	5.8	431.5	49
E55/25	849.2	36	37	8.73	128.0	4.7	322.9	62
E55/25	849.2	42	32	8.05	128.0	4.1	257.5	70

Core	A_e	f_s	N	A_w	C_w	l_w	A_{req}	Diff
	mm^2	kHz	turns	mm^2	mm	m	mm^2	%
E55/25	849.2	48	28	7.59	128.0	3.6	212.5	75
E55/25	849.2	54	25	7.06	128.0	3.2	176.4	79
E55/25	849.2	60	23	6.78	128.0	2.9	156.0	82
E55/25	849.2	66	21	6.43	128.0	2.7	135.0	84
E55/25	849.2	72	19	6.18	128.0	2.4	117.5	86
E65/27	1196.0	18	58	12.38	146.0	8.5	718.3	40
E65/27	1196.0	24	44	10.62	146.0	6.4	467.2	61
E65/27	1196.0	30	35	9.59	146.0	5.1	335.6	72
E65/27	1196.0	36	29	8.73	146.0	4.2	253.1	79
E65/27	1196.0	42	25	8.05	146.0	3.7	201.2	83
E65/27	1196.0	48	22	7.59	146.0	3.2	167.0	86
E65/27	1196.0	54	20	7.06	146.0	2.9	141.1	88
E65/27	1196.0	60	18	6.78	146.0	2.6	122.1	90
E65/27	1196.0	66	16	6.43	146.0	2.3	102.8	91
E65/27	1196.0	72	15	6.18	146.0	2.2	92.7	92

Dual Active Bridge Simulation Setup D

LTspice XVII is used to simulate the DAB to validate the loss model derived in this research. Figure D.1 demonstrates the circuit used in LTspice XVII to simulate the output voltage and current. Figures D.2 and D.3 are enlarged views of the primary and secondary side of Figure D.1 respectively. The MOSFETs are driven by IR2110 drivers which receive logical inputs that follow the Triangular Modulation methods described in Chapter 4. Simulating this circuit leads to the waveforms demonstrated Figures D.4 and D.5. Figures D.4a and D.4b demonstrate the pulsed waveforms across the transformer. These waveforms cause a potential difference across the leakage inductance of the transformer which induces a current. The current through the leakage inductance is demonstrated in Figure D.4c. The output bridge rectifies the waveform and passes it through the output capacitor, C_{o}. This leads to the voltage and current over the load demonstrated in Figure D.5.

Conclusion

Figures D.4 and D.5 demonstrate the use of the DAB as a sinusoidal inverter using LTspice XVII to simulate the output voltage. The simulated losses in are compared to the approximated losses in this research to ensure that the approximation is accurate.

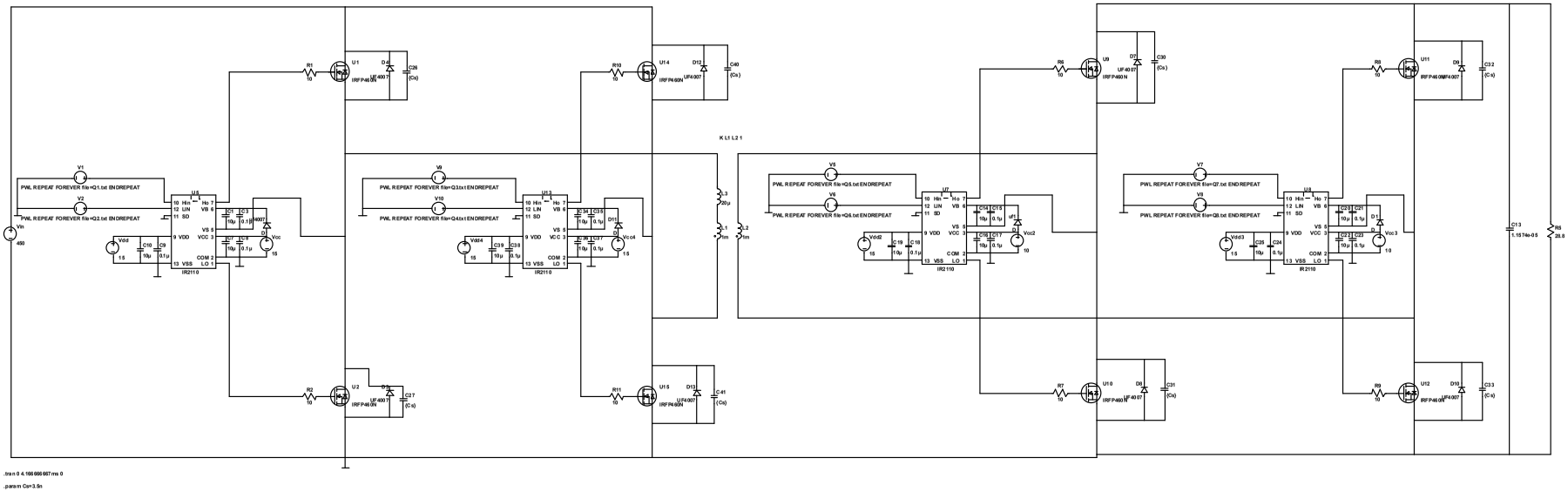


Figure D.1: The DAB circuit used in the LTspice XVII simulations. The IR2110 MOSFET drivers are used along with IRFP460 MOSFETs.

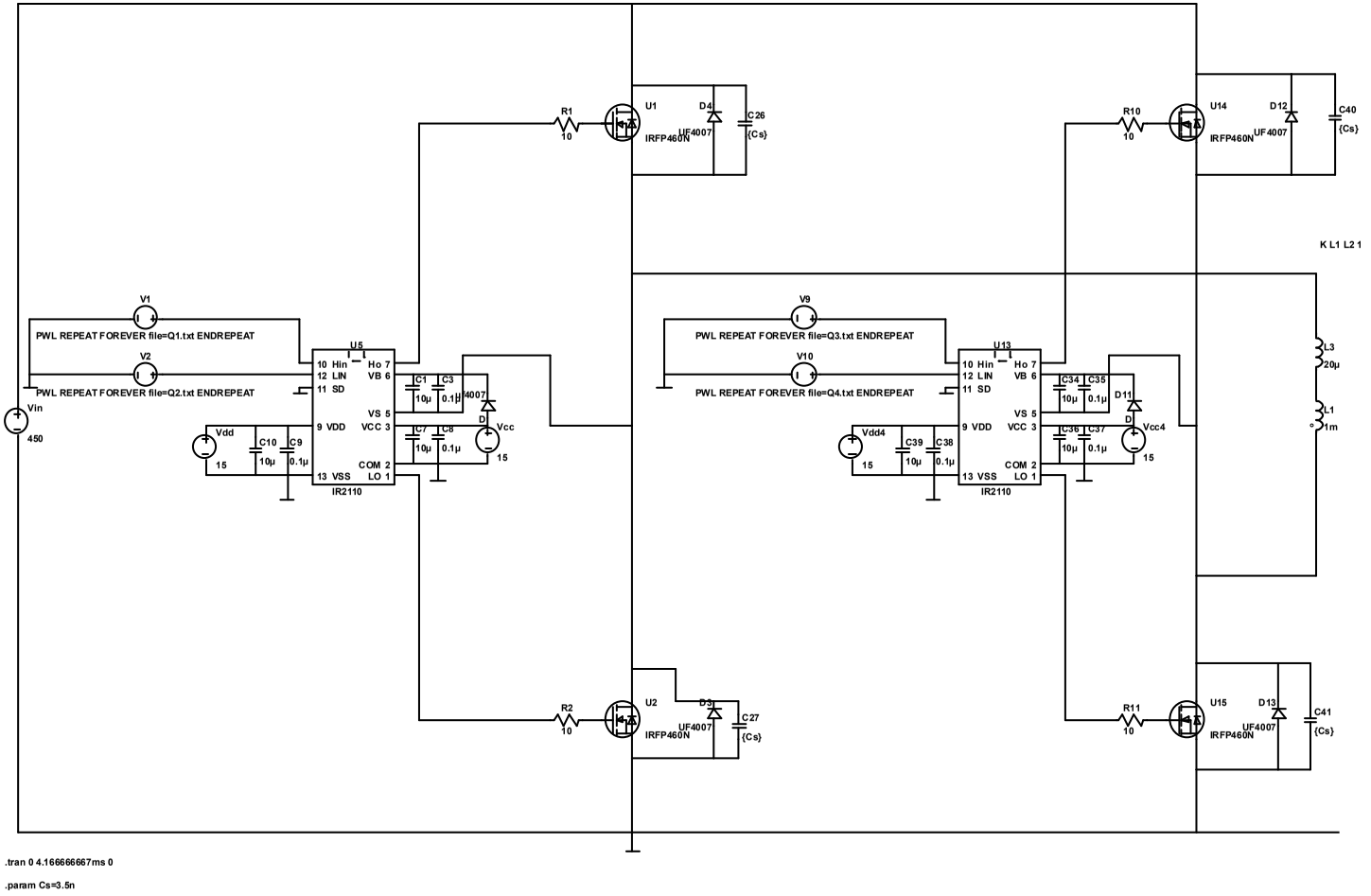


Figure D.2: The primary side of the DAB circuit used in the LTspice XVII simulations.

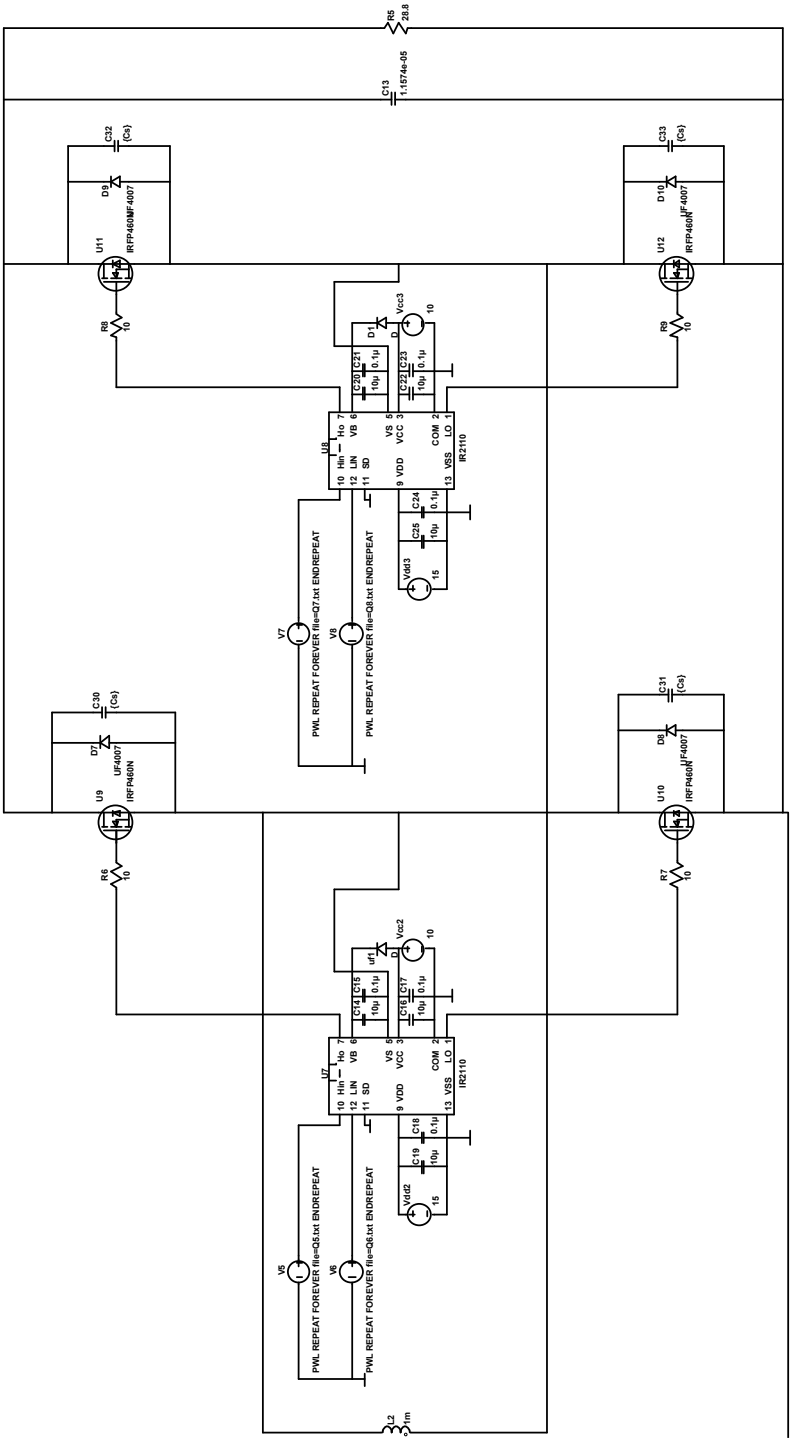
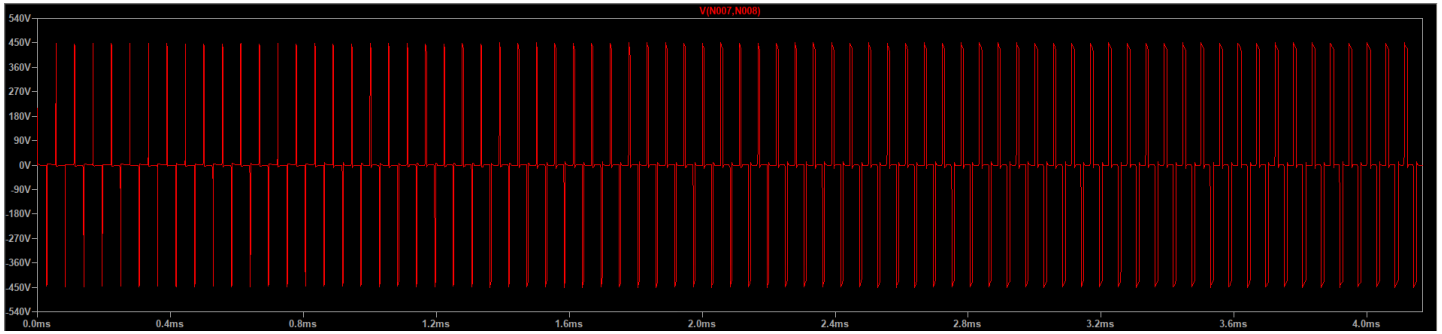
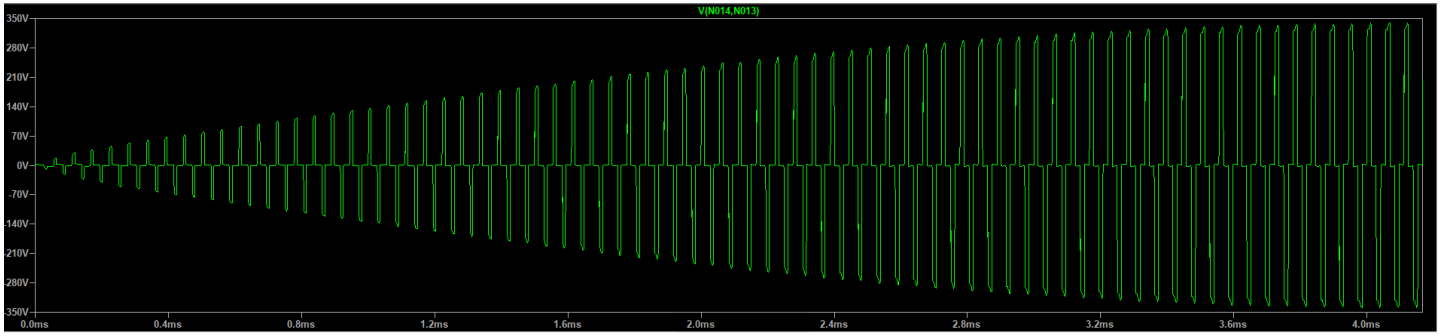


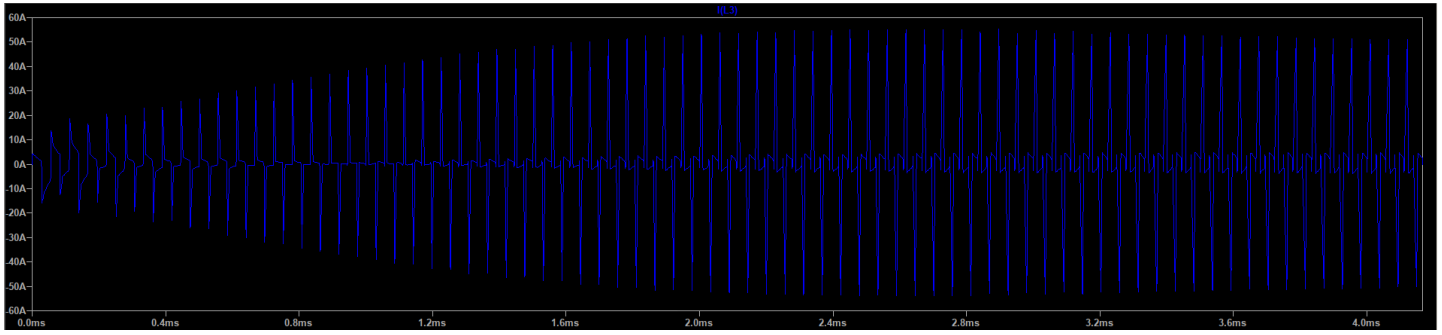
Figure D.3: The secondary side of the DAB circuit used in the LTspice XVII simulations.



(a) The modulated voltage across the transformer by the input bridge. The peak voltages remain constant at V_{in}.

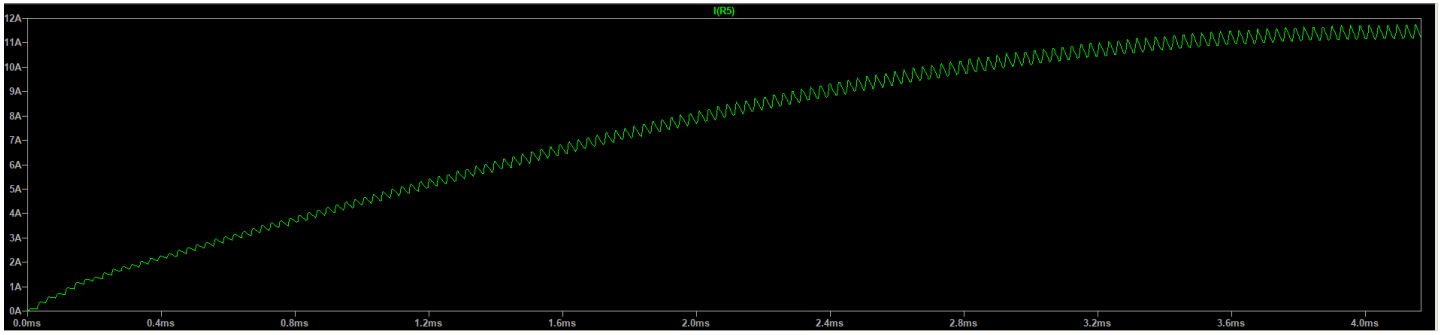


(b) The modulated voltage across the transformer by the output bridge. The voltage increases as the output voltage increases.

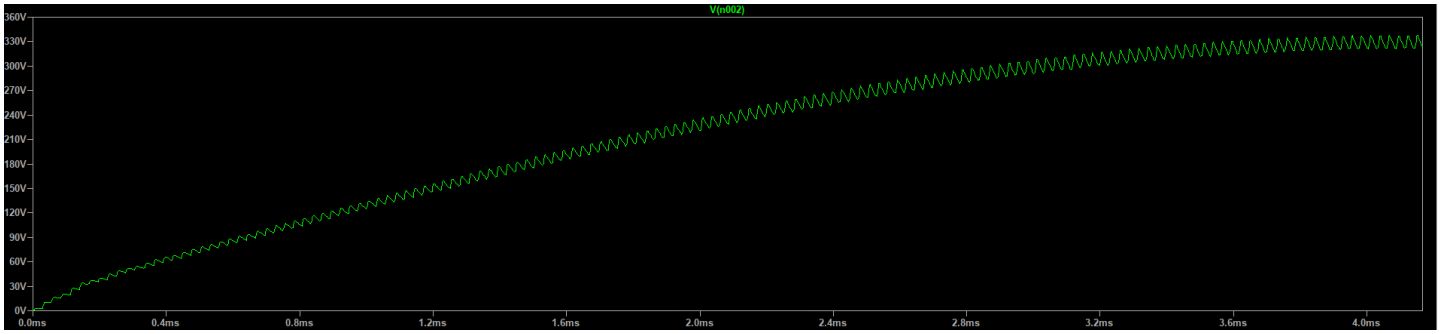


(c) The current through the leakage inductance of the transformer.

Figure D.4: The waveforms seen when simulating a quarter-wave of the DAB LTspice XVII models.



(a) The output current through the load resistance.



(b) The output voltage across the load resistance.

Figure D.5: The final output waveforms seen when simulating a quarter-wave of the DAB LTspice XVII models.