PERFORMANCE EVALUATION OF CURRENTLY AVAILABLE VLSI IMPLEMENTATIONS SATISFYING U-INTERFACE REQUIREMENTS FOR AN ISDN IN SOUTH AFRICA

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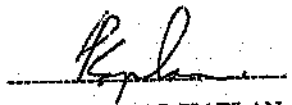
A project report submitted to the Faculty of Engineering, University of the Witwatersrand, Johannesburg, in partial fulfilment of the requirements for the degree of Master of Science in Engineering.

JOHANNESBURG, 1990

DECLARATION

I declare that this project report is my own, unaided work. It is being submitted for the Degree of Master of Science in Engineering in the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination in any other University.



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30th day of NOVEMBER 1990.

ABSTRACT

This project report examines the performance of three VLSI U-interface implementations satisfying the requirements of Basic Access on an ISDN.

The systems evaluated are the Intel 89120, Siemens PEB2090 and STC DSP144, operating on 2B1Q, MMS43 and SU32 line codes respectively.

Before evaluating the three abovementioned systems, a review of the underlying principles of U-interface technology is presented. Included in the review are aspects of transmission line theory, line coding, echo-cancellation, decision feedback equalisation, and pulse density modulation. The functional specifications of the three systems are then presented followed by a practical evaluation of each system.

As an aid to testing the transmission systems, an evaluation board has been designed and built. The latter provides the necessary functionality to correctly activate each system, as well as the appropriate interfacing requirements for the error-rate tester.

The U-interface transmission systems are evaluated on a number of test-loops, comprising sections of cable varying in length and gauge. Additionally, impairments are injected into data-carrying cables, in order to test the performance of each system in the presence of noise. The results of each test are recorded and analysed.

Finally, a recommendation is made in favour of the 2B1Q U-interface. It is shown to offer superior transmission performance, at the expense of a slightly higher transmit-power level.

DEDICATION

To my wife Evelyn who stood by me throughout, and my daughter Danielle who arrived in the middle.

ACKNOWLEDGEMENTS

I would like to thank Standard Telephones & Cables (SA) Limited, with a special mention being made to Mr. Les Devenish, for the assistance afforded me in respect of facilities, equipment and support.

I am also inde ed to Mr. Dave Fisher of STC (UK) for his invaluable technical advice on many aspects of the U-interface.

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NOMENCLATURE

ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
AWG	American Wire Gauge
BA	Basic Access
BER	Bit Error Rate
BT	British Telecom
CA	Correlation Algorithm
CCITT	Consultatif Committé International Telephonique et Telegrapfique
CF	Conversion Filter
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DEC	Decimation
DFE	Decision Feedback Equalisation
DSL	Digital Subscriber Loop
DSV	Digital Sum Variation
EC	Echo Canceller
EOC	Embedded Operations Channel
FDM	Frequency Division Multiplexing
FEBE	Far End Block Error
FEXT	Far End Crosstalk

HDLC	High-level Data Link Control
HPF	High Pass Filter
IOM	ISDN Oriented Modular
ISDN	Integrated Services Digital Network
ISI	Inter Symbol Interferance
ISO	International Standards Organisation
ISW	Inverted Synchronisation Word
LAP-D	Link Access Protocol on the D-channel
LED	Light Emitting Diode
LFSR	Linear Feedback Shift Register
LMS	Least Mean Squares
LPF	Low Pass Filter
LS	Least Squares
MS	Mean Square
MSE	Mean Squared Error
NEXT	Near End Crosstalk
NRZ	Non Return to Zero
NTU	Network Terminating Unit
NZREC	Non-Zero Reference Echo Canceller
OSI	Open Systems Interconnection
PAM	Pulse Amplitude Modulation
PCM	Pulse Code Modulation
PDM	Pulse Density Modultor/Modulation

PIC	Polyethelene Insulated Cable
PRA	Primary Rate Access
PSD	Power Spectral Density
PSI	Phase Shift Interpolation
PSTN	Public Switched Telephone Network
PSU	Power Supply Unit
RDS	Running Digital Sum
RZ	Return to Zero
S&M	Supervisory and Maintenance
SA	Sign Algorithm
SAPT	South African Posts & Telecommunications
SIA	Stochastic Iteration Algorithm
$\Sigma\Delta M$	Sigma Delta Modulator/Modulation
SR	Shift Register
SS7	Signalling System No. 7
STC	Standard Telephones & Cables
STL	STC Technology Limited
SW	Synchronisation Word
TCM	Time Compression Multiplexing
TDM	Time Division Multiplexing
TF	Transversal Filter
TR	Timing Recovery
UI	Unit Interval

VCXO	Voltage Controlled Crystal Oscillator
VLSI	Very Large Scale Integration
XTAL	Crosstalk
ZREC	Zero Reference Echo Canceller

1 INTRODUCTION

This project report focuses on a fundamental issue in the evolution towards an ISDN, viz; The U-reference point or U-interface, as it is more commonly known. Although the U-interface is but one facet of a large and sophisticated system, its development has been a challenge to design teams throughout the world. It is in fact only during the past two years that VLSI implementations of the U-interface have begun emerging.

Although a number of solutions have been proposed, some of which will be briefly covered in Chapter 5, one particular class of system has been opted for in the USA, Europe and Britain. These systems all rely on the technique of Echo Cancellation (EC) for separating the two directions of data-transmission. The principles of EC have been well understood for over a decade, yet it is only during the last three years that it has become technically and commercially viable to implement a complete U-interface on a chip or chip-set. The difficulty in the past can be attributed to the relatively large number of transistors (ie. ±80 000) needed to implement the Digital Signal Processing (DSP) functions. Using CMOS fabrication techniques with a feature size of 2μm or less, integrated EC technology has now become a welcome reality.

This report comprises eleven chapters, each of which encompasses a single topic. While every endeavour is made to ensure that each chapter is relatively self-contained, many instances arise where reference is made to concepts and principles developed during preceding chapters.

The expert reader may wish to skip certain chapters and concentrate specifically on areas relating to the transmission performance of each U-interface. In such a case, Chapters 2 to 6 may be omitted since the latter merely provide an overview of ISDN as well as techniques relevant to the implementation of a U-interface.

A brief introduction to each chapter now follows:

Chapter 2 examines an ISDN in its broadest sense; that of a telecommunication service provider. The various reference points, OSI layers and signalling system are discussed, giving the reader an overall picture.

Since the U-interface is designed to operate over standard twisted pairs normally used in the Public Switched Telephone Network (PSTN), Chapter 3 is devoted to a discussion of the SAPT's cable-plant and the characteristics of individual cable-pairs therein.

An important consideration in the design of a U-interface is the choice of line-code. Each of the 3 specifications mentioned above do in fact call for a different line code viz. SU32, MMS43 and 2B1Q. Chapter 4 introduces these line codes and evaluates their performance.

Chapter 5 presents a brief introduction to Non-EC separation techniques, followed by the underlying theory governing EC and DFE operation. The LMS algorithm and its variants are analysed, with a view to highlighting the relative trade-off between conversion time and residual echo.

A technique often neglected in a report of this nature is that of analogue-to-digital conversion, and conversely, digital-to-analogue conversion. All three U-chips evaluated use the same technique of Pulse Density Modulation (PDM), otherwise known as $\Sigma\Delta$-modulation, as their analogue-to-digital converter front-end. Chapter 6 introduces PDM as well as the decimating conversion-filter usually associated with a pulse-density-modulator.

Chapter 7 introduces and analyses three sets of U-interface specifications viz. those of British Telecom (BT), Deutsche Bundespost and ANSI T1. Each of the 3 U-interface chip-sets evaluated in this project report is designed according to one of these specifications.

Chapter 8 introduces the U-interface chip-sets under review. The architecture and theory of operation of each chip-set is presented, followed by a discussion of the salient differences between each system.

The chip-sets introduced in the preceding chapter perform all the functions required of a full-duplex synchronous transmission system. However, a considerable amount of external circuitry is needed to initiate each system's activation sequence, as well as perform data-rate conversion between the bit-error-rate tester and the chip-sets. Unfortunately, the interfacing problem is aggravated by the fact that each chip-set has a different interfacing and activation sequence requirement. Chapter 9 discusses the circuitry required to perform the above-mentioned functions.

Chapter 10 details the performance of each chip-set as observed in the laboratory. Various tests are performed to evaluate the transmission range, transmit-power and activation time of each system. In addition, various disturbing signals are injected into the cable in order to test transmission performance in the presence of noise.

Chapter 11 concludes this project report by recommending a commercially-available U-interface system suitable for a future ISDN in South Africa.

2 ISDN - A BRIEF OVERVIEW

2.1 Introduction

The concept of an Integrated Services Digital Network (ISDN) is a single network that provides universal communication facilities between a multitude of different user types. An ISDN features a common transmission system for all types of traffic as well as standard access to the network for all supported terminal equipment. Provision is also made to support existing non-compatible terminals through the use of terminal adapters.

Currently, the world's telecommunications authorities, including the SAPT, provide a range of voice and data services (eg. telephone, telex, facsimile, videotex, and other terminal-to-terminal data services) distributed across a number of different public networks. These networks are specialised, differing in terms of their transmission rates and characteristics due to being primarily dedicated to one type of service. For example, the telephone network is primarily designed for voice communications, whereas packet and circuit-switched data networks are designed to carry high-speed digital data in the relevant formats.

Paradoxically, some of the data services are provided on more than one network as shown in Figure 2.1. However, the terminal equipments differ, and in general, are mutually incompatible. This is due to the terminals being matched to their respective networks. Any interworking between two different networks can only be achieved using specialised "gateway" exchanges that adapt one form of transmission to the other.

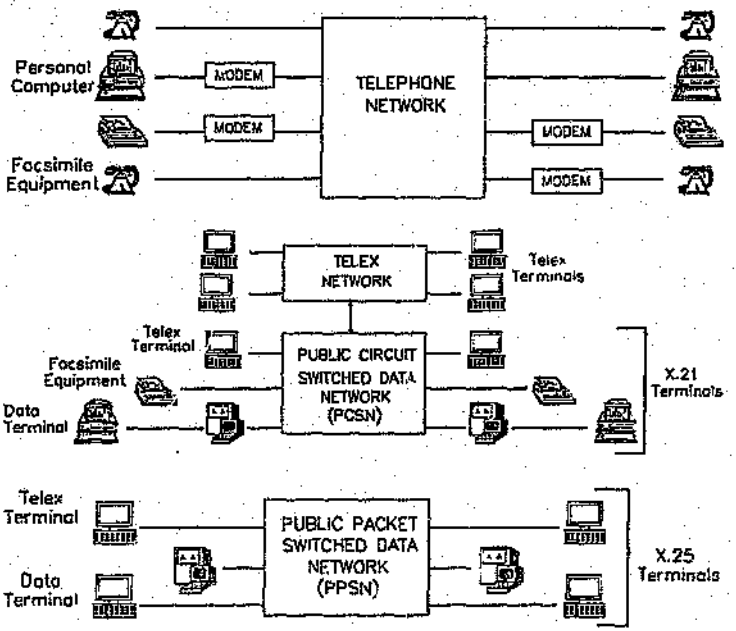


FIGURE 2.1 : PRESENT DAY COMMUNICATION NETWORKS

Figure 2.2 depicts ISDN as an "open systems interconnection and communication" network. This concept allows, in general, information-compatible terminals to communicate via a single network, regardless of differences in transmission parameters, ie. analogue or digital, bit-rates, or protocols. The transmission characteristics and speeds of non-compatible terminals are adapted to conform to the ISDN access by terminal adapters located at the subscriber's premises.

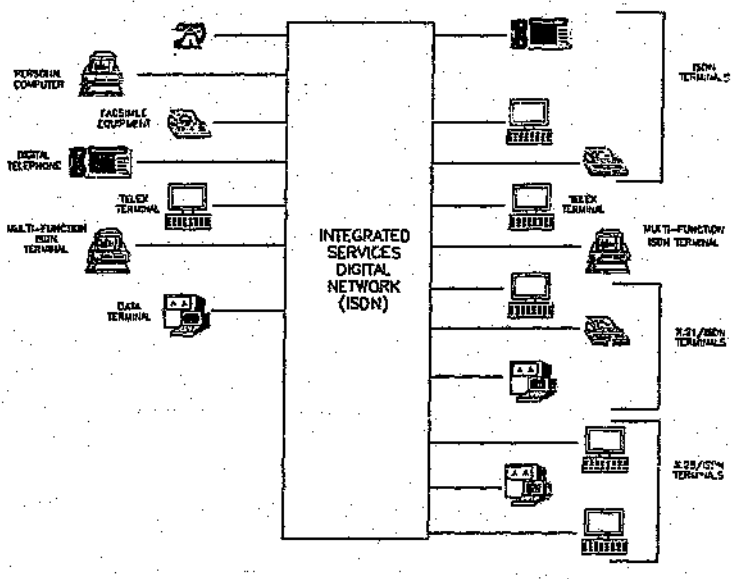


FIGURE 2.2 : ISDN NETWORK

The primary aim of an ISDN is to provide open systems interconnection and communication, and is the next inevitable stage in the evolution of the world's telecommunication networks. It is intended to rationalise today's networks, which have developed and evolved largely independently of one another, and bring together into one integrated network the range of services currently offered individually on the different types of public networks.

2.2 The OSI Reference Model

The Open Systems Interconnection (OSI) model was originally defined by the International Standards Organisation (ISO) as a reference model for data communication in open systems, with respect to computers and information processing. It has subsequently been adopted by the CCITT for ISDN in their X.200 [1] recommendations, and later in their I.320 recommendations [2].

The OSI reference model provides a basis for standardising open communication. It does not itself define the interfaces and protocols to be used but rather identifies the overall framework within which the interfaces and protocols can be developed and assigned.

Communication is a hierarchical process involving application functions at the higher levels, and purely information-transport functions (bearer services), at the lower levels. The

reference model is a pictorial representation of this hierarchical communication process, and identifies the levels at which the various applications and transport functions are performed, and hence where protocols and interfaces apply.

The OSI reference model, shown in Figure 2.3, defines seven independent hierarchical layers. Each layer defines the functions to be performed by the various building blocks of the system at that level, together with the type of protocols assigned to that layer. In addition, it identifies the interface functions required for communicating with the adjacent layers above and below.

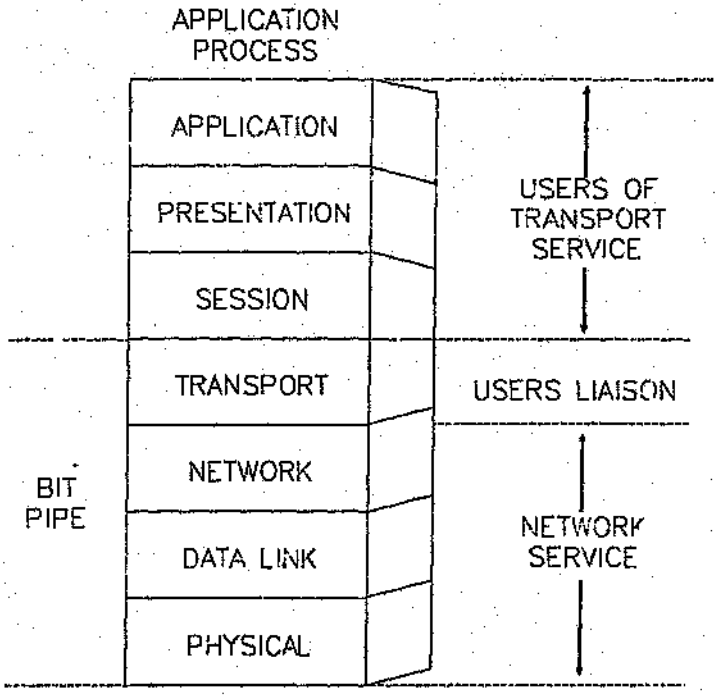


FIGURE 2.3 : OSI REFERENCE MODEL

For a communication session between two end-points of an ISDN (eg. person-to-person or terminal-to-terminal), successive layers of task-related functions each add their protocol messages to the information to be sent, and this collective data is then transmitted over the physical medium (eg. digital trunks of the network). At the receiving end, these protocol messages are interpreted at their appropriate layer and stripped off, with the balance of the information passed up to the next layer until the original information arrives at its intended destination.

Layers 1 to 4 of the OSI model refer to the "transport" protocols, ie. the protocols governing the reliable end-to-end transport of the information across the network, while layers 5 to 7 depict the application protocols ie. the protocols governing the exchange of information between the two end-terminals.

A definition of the functions provided by the OSI layers is not easy as the definitions are inherently vague. One should keep in mind that the seven layer OSI structure is a vehicle for allowing distributed user processes to interact gracefully via an intermediate communications network. In this sense, the seven layer model may be considered as a distributed operating system connecting the user processes via an imbedded telecommunications network.

Brief descriptions of the functional content of each layer are as follows:

LAYER 7 : APPLICATION LAYER - This is the upper layer and interfaces directly with user programs, which it supports. Tangible examples of functions included in this layer are the support of distributed databases, and support of distributed computing and distributed operating systems. The term distributed refers here to multiple user facilities communicating across the network.

LAYER 6 : PRESENTATION LAYER - This layer governs the information format and method of exchange. Examples of functions found in this layer are cryptographic transformations, text compression, file transfer and terminal handling.

LAYER 5 : SESSION LAYER - This layer defines the functions required for opening a communications session, exchanging the information in an orderly fashion, and terminating the session. Examples of functions found in this layer are identification of the call originator and logging-in at the remote end of the network. For packet switching, a potential function of Layer 5 or 6 is separating the data to be sent into packets, and re-assembling the packets into complete data blocks at the other end.

LAYER 4 : TRANSPORT LAYER - This layer performs the functions that establish a terminal-to-terminal error-free connection from one user to the other. It defines the logical connections across the network, in terms of originating the destination addresses of the two end-points (as opposed to the actual physical connections performed by network Layer 3). A single transport connection may include several physical call set-up sequences, for example, in the case of packet-switching. The Layer 4 functions are thus concerned with the administrative and supervisory aspects of call set-up, rather than the physical connections across the network. They also include end-to-end error checking and correction procedures.

LAYER 3 : NETWORK LAYER - This layer defines the mechanics of communications path assembly from a series of error-protected links between the various nodes of the network. Layer 3 includes the network signalling protocol that determines the routes taken through the network.

LAYER 2 : LINK LAYER - This layer defines the functions necessary to protect each link that forms part of the transmission path from errors. Thus each of the node-to-node links of the path detects and corrects errors, using techniques such as High-level Data Link Control (HDLC) procedures. HDLC organises the transmission of information in standard-format information frames, and provides retransmission and flow control.

LAYER 1 : PHYSICAL LAYER - This layer determines the physical transmission characteristics of a node-to-node link, eg. voltage and signalling conventions, but does not ude the physical medium for the transmission. It thus provides the basic transmission ...aracteristics for sending a stream of information via the physical transmission medium, but without error protection. The remainder of this project report is primarily concerned with the requirements of the physical layer.

It is particularly important to recognize that the set of levels involved in a given transaction can be different for the signalling phase and the user data-exchange phase. During the signalling phase, software functions belonging to Layers 1, 2 and 3 are included within the network nodes. During the exchange of user inform..tion, the number of network levels involved will depend on the call type. For packet type calls, Layers 1, 2 and 3 are involved; for circuit-switched calls, only Layer 1 applies.

2.3 Transmission Characteristics

Currently, a substantial part of the global telephone network as well as some other networks use a primary rate PCM digital transmission system for inter-exchange communications. Primary rate PCM systems are organised either as multiplexed 32-channel (Europe and South Africa) or 24-channel (United States) systems. For both systems, the fundamental channel rate is 64kbit/s, with total bit rates for the primary multiplex of 2,048Mbit/s or 1,544Mbit/s respectively. A good coverage of PCM is given in reference [3].

The CCITT decided to use the primary rate PCM standard as the basis for an ISDN. Using this standard, the administrations can choose to allocate speech, data and signalling to different numbers of channels appropriate to their needs. In general, a number of channels are allocated to speech and data, and one or more channels can be allocated to network signalling and maintenance information, together with a separate channel for synchronisation and control signals.

The network signalling protocol for inter-exchange signalling is to be the CCITT No. 7 Common Channel Signalling System (SS7). SS7 relies on the signalling information for a number of speech or data channels occupying a separate transmission channel which is then shared by the different speech and data channels. This differs from channel-associated or in-channel signalling, where each speech path carries its own signalling messages. SS7 is a fairly complex signalling system loosely based on the OSI model. It is beyond the scope of this report to cover the system in any detail, and the reader is referred to reference [4] and [5] (Q.701-Q.714) for a description and specifications respectively.

For the subscriber links to the ISDN exchanges, a decision had to be taken on the data and signalling content of the information exchanged, as well as the allocation of the different transmission channels. Also, these channels had to be defined in terms of their transmission bit-rates and protocols. As a result, CCITT has produced a number of additional channel definitions to supplement their existing ones. Currently, the main transmission channels defined by CCITT are:

* A-CHANNEL - which is the traditional analogue channel with a bandwidth of 3,1kHz.

* B-CHANNEL - which is the fundamental digital information channel operating at 64kbit/s and capable of carrying circuit- or packet-switched data.

* C-CHANNEL - which is primarily defined as a signalling channel carrying its information in "packet" form. Optionally, it may also be used for conveying low-speed user packet data. Currently, it is defined for two transmission rates of 16kbit/s and 64kbit/s, depending upon the type of ISDN access to be offered to the subscriber. It employs a unique layered signalling protocol called Link Access Protocol on the D-channel (LAP-D).

  Basically, LAP-D is a packet signalling protocol resembling CCITT X.25, but containing additional addressing information enabling it to work with point-to-multipoint configurations (ie. with multiple terminals on one link). LAP-D encompasses the Layer 2 functions and is built up from elements of the HDLC procedures. It ensures the reliable delivery of the Layer 3 signalling messages in the D-channel that set up the route for the information to be conveyed across the network. Figure 2.4 shows the composition of a Layer 2 information frame using the LAP-D protocol.

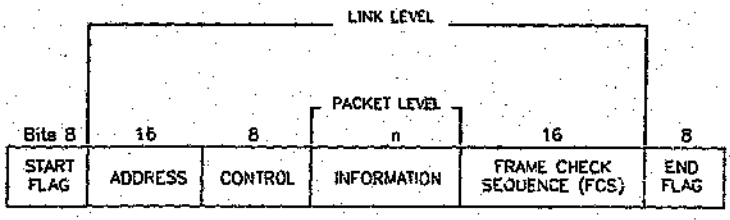


FIGURE 2.4 : LAYER 2 INFORMATION FRAME ON THE D-CHANNEL

* E-CHANNEL - which is an alternative type of 64kbit/s signalling channel, but based on the CCITT SS7 for its Layer 2 functions. The Layer 3 control procedures for circuit-switched connections are the same as those used for 64kbit/s D-channel signalling.

* H-CHANNELS - which are the higher transmission rate channels envisaged for use in wideband and broadband ISDN. Two types (H0 and H1) have thusfar been defined, and others are foreseen as follows:

  - H0-CHANNEL - which operates at 384kbit/s (6x64kbit/s).
  - H1-CHANNEL - comprising H1(1) at 1536kbit/s (24x64kbit/s), and H1(2) at 1920 .bit/s (30x64kbit/s).
  - H2-CHANNEL - to operate at approximately 30Mbit/s.
  - H3-CHANNEL - to operate at approximately 70Mbit/s.
  - H4-CHANNEL - to operate at approximately 140Mbit/s.

The inclusion of H-channels for wide band ISDN facilitates the provision of TV quality video signals.

2.4 Subscriber Access

Two types of subscriber access are defined by CCITT for narrowband ISDN - a Basic Access (BA) for conventional subscribers, and a Primary Rate Access (PRA) for subscribers with a high volume of traffic, such as digital PABXs, private Local Area Networks (LANs), and database providers.

A basic access comprises two duplex 64kbit/s B-channels for voice and data, and one associated duplex 16kbit/s D-channel for signalling (and optionally low-speed packet data), ie. BA=2B+D.

This provides a total usable data and signalling rate of 144kbit/s across the three channels allocated per subscriber. The basic access usually relates to a multipoint subscriber configuration, where a number of subscriber terminals are connected to the subscriber line in a bus or star arrangement, ie. the exchange to subscriber link is a point-to-multipoint access.

A primary rate access comprises 30 duplex 64kbit/s B-channels for voice and data, and one associated duplex 64kbit/s D-channel for signalling, ie. PRA=30B+D.

This provides a total usable data and signalling rate of 1984kbit/s across the 31-channels. Additionally, synchronisation, timing and control bits are added into the information stream to provide a total transmission rate of 2048kbit/s. This is equivalent to a 32-channel 2Mbit/s PCM link between the exchange and subscriber, where the B-channel data is carried in Channels 1 to 15 and 17 to 31, the D-channel signalling information is contained in Channel 16, and synchronisation, timing and control information in Channel 0.

The primary rate access relates only to the point-to-point configuration of an ISDN exchange with a large single subscriber, such as a digital PABX.

2.5 Subscriber Interfaces

At the subscriber's premises, a variety of different types of terminal equipment will require access to the ISDN. Initially, few of these terminals will have been designed to work with an ISDN, and hence a form of terminal adapter will be required to convert the interface and transmission characteristics of the terminals to those of an ISDN basic access. This involves adapting the transmission bit rates to B-channel 64kbit/s operation (with analog-to-digital PCM conversion where necessary), and converting the signalling protocols (eg. X.21, X.25, V.24) to the LAP-D protocol on the D-channel.

At the exchange, functions are required to terminate the subscriber line, extract and interpret the signalling information in the D-channel, and switch the B-channel data in order to route the calls into the network.

In order to ensure that the conversion of transmission characteristics, protocol conversions, and interface functions are performed consistently at the same points in the subscriber's terminal equipment and exchange equipment supplied by different manufacturers, CCITT have defined a number of functional protocol blocks and key interfaces. These apply on the basic access link between the subscriber, subscriber line, and ISDN exchange, as shown in Figure 2.5.

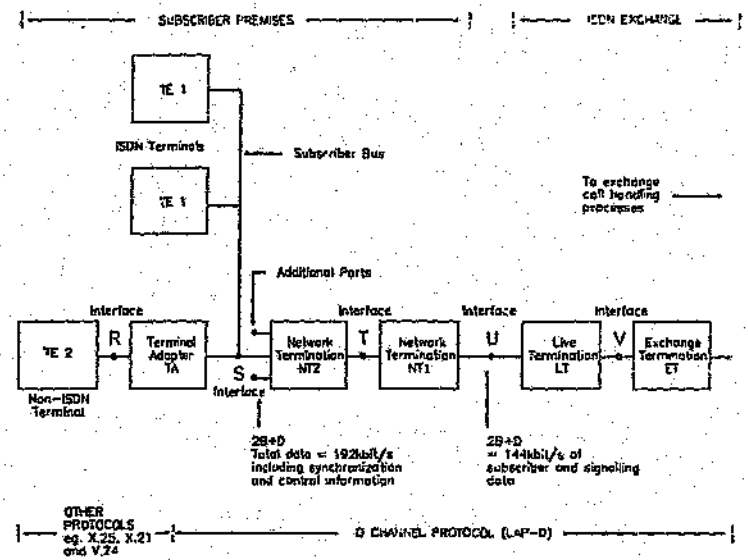


FIGURE 2.5 : BASIC ACCESS FUNCTIONAL BLOCKS & INTERFACES

The functional blocks define the equipment functions that must be performed between the interface reference points R,S,T,U and V, with these reference points representing the key physical interfaces between the blocks.

2.5.1 Functional Blocks

The Layer 1 functional blocks for a basic access are defined as follows:

* TE1 : TERMINAL EQUIPMENT TYPE 1 - which represents the functions of ISDN terminals, ie. single or multi-service terminals designed to comply with the CCITT user-to-network interface recommendations for an ISDN basic access.

* TE2 : TERMINAL EQUIPMENT TYPE 2 - which represents non-ISDN terminals, ie. those terminals currently in service that are not designed to the ISDN user-to-network interface recommendations. These terminals operate with a variety of transmission characteristics, protocols and formats. TE2 equipments require a terminal adapter to convert their operation for the ISDN user-to-network interface.

* TA : TERMINAL ADAPTER - which represents the functions that terminal adapter equipment must perform to adapt non-ISDN terminals to an ISDN user-to-network interface. To date, CCITT has identified three standard TAs for

the support of: X.21 and X.21bis circuit-switched terminals (I.461), X.25 packet terminals (I.462) and V-series terminals (I.463). However, further TAs may be produced for other types of TE2 equipment.

* NT1 : NETWORK TERMINATION 1 - which represents the equipment provided by the administrations to physically and electrically terminate the subscriber line.

* NT2 : NETWORK TERMINATION 2 - which represents the functions for switching and concentration of a number of subscriber terminals. Up to eight terminals may be connected to an NT2 S-interface port. As shown in Figure 2.5, NT2 has more than one port. When only a single port is required, the S- and T-interfaces coincide and the NT2 falls away.

* LT : LINE TERMINATION - which denotes the line termination function at the exchange end of the subscriber line.

* ET : EXCHANGE TERMINATION - which denotes the exchange termination functions of an ISDN exchange. These functions deliver the signalling information to the call handling processes of the exchange, which in turn initiate inter-exchange signalling.

2.5.2 Layer 1 Reference Points

The logical structure of reference points R,T and V are deducible from the preceding discussion about functional blocks, and therefore will not be mentioned any further in this section.

The U-reference point is responsible for transparent duplex transmission of 2B+D (ie. 144kbit/s) over a single twisted 2-wire cable. Its requirements and design are the subject of the major part of this report, and will be dealt with in later chapters. The S-reference point has been thoroughly specified by the CCITT (I.430), and will be briefly discussed at this point.

The S-reference point, or S-interface as it is generally called, supports a 4-wire physical transmission medium (ie. 2 wires for the NT-to-TE direction, and 2 wires for the TE-to-NT direction of transmission). Each direction carries data at 192kbit/s formatted in frames of 48 symbols. The line code on the S-interface is Alternate Mark Inversion (AMI), and hence each pseudo-ternary symbol represents a single binary digit. The frame duration is thus 250 μ s providing a 4kHz period.

The S-interface frame structure for the two directions is shown in Figure 2.6.

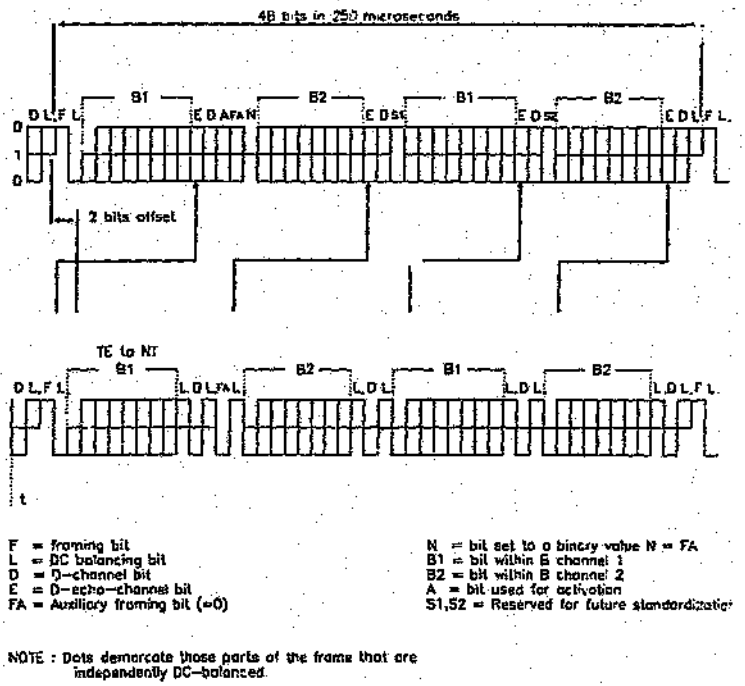


FIGURE 2.6 : FRAME STRUCTURE AT REFERENCE POINTS S&T

The balance bits serve to reduce residual DC which could otherwise accumulate, since the B1 and B2 bits are generated by independent transmitter sources.

The D-channel echo bits facilitate a collision detection protocol in the event of two or more terminals requiring simultaneous access to the D-channel.

The frame bit (F), auxiliary framing bit (FA), DC balancing bits (L) and N bits, form an AMI code violation sequence, which ensures framing independent of wiring polarity.

The activation bit (A) is used in the TE-to-NT direction to initiate activation of the U-interface.

2.6 ISDN in South Africa

This section is based on the proposals of Van Dijk and Stanier [6]. It aims to enlighten the reader on the intentions of the SAPT as regards an ISDN in South Africa, as well as a possible time-scale for the planned pilot phases.

Prior to ISDN implementation, a number of prerequisites must be met. These are summarised as follows:

* Fully digitalized telephone network end-to-end.
* Implementation of SS7 between exchanges.
* Interworking between the various networks (eg. Telephone, Saponet-C, Saponet-P, Telex, etc).
* A defined routing and numbering scheme.
* Inter-network timing synchronisation.

2.6.1 Digital Telephone Network

In digitalizing the telephone network, both exchanges and transmission systems must be considered. The SAPT has committed itself to the widespread introduction of digital public exchanges, and it is expected that by 1995, 69% of the total number of subscriber ports in South Africa will be connected to a digital exchange. It is also predicted that at this stage, 85% of all transmission circuits will be digital in nature.

2.6.2 CCITT Common Channel Signalling No. 7

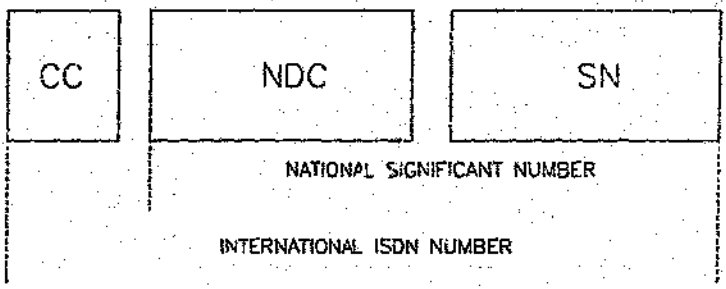
The present signalling system used in the South African digital telephone network consists of either line signalling or the CCITT recommended MFCR2 register signalling. These signalling systems would have to be replaced with SS7 before ISDN could become feasible. The SAPT is currently at the stage where the implications of introducing SS7 into the telephone network are being studied.

2.6.3 Network Interworking

Regarding interworking between the various networks, the SAPT favours a "maximum integration" scenario as specified by CCITT recommendation I.462. With maximum integration, the packet handler, in the case of a packet-switched data network, forms an inherent part of the ISDN, and accesses the packet network through an X.75 gateway. Similarly the other republic networks would also eventually be integrated into a single ISDN network.

2.6.4 Routine and Numbering Scheme

The routing and numbering scheme will follow along the lines of CCITT recommendation I.330 and E.164. A South African ISDN subscriber would have a single number of maximum length equal to 15 digits with the format [2] shown in Figure 2.7.



CC – COUNTRY CODE (27)
NDC – NATIONAL DESTINATION (ie. TRUNK) CODE
SN – LOCAL SUBSCRIBER NUMBER

FIGURE 2.7 : ISDN NUMBER STRUCTURE

2.6.5 Inter-Network Synchronisation

The master clock is Caesium based with duplicated tubes yielding a frequency stability in excess of $1 \in 10^{-11}$. Currently, all digital exchange clocks are connected to the master clock in a star network configuration. The other networks (ie. Diginet, Saponet-C and Saponet-P) have also recently been synchronised to the Caesium master clock.

2.6.6 ISDN Pilot Scheme

The proposed ISDN pilot scheme will comprise 3 phases as follows:

* PHASE 1 - Independent Siemens EWSD exchange to familiarise SAPT with the U-interface, LAP-D protocol and various terminal adapters.

* PHASE 2 - The incorporation of an Altech SAI28E exchange. The EWSD and SAI28E exchanges will be linked to form an ISDN. In this pilot phase, SAPT will evaluate end-to-end working between terminals connected to each exchange as well as SS7 between exchanges.

* PHASE 3 - Initiation of this phase is dependent on the successful outcome of Phases 1 and 2. This phase aims to evaluate the market potential of an ISDN in South Africa.

After all three phases of the pilot scheme have run their course, SAPT will make a decision based essentially on market-place viability, whether to proceed with an ISDN in South Africa.

3 THE SAPT CABLE-PLANT

3.1 Introduction

The design of any transmission system is heavily dependent on the characteristics of the transmission medium. In some instances the designer has a certain level of flexibility in choosing or specifying the salient parameters of the transmission medium. In the case of an ISDN U-interface, the designer has absolutely no control over this aspect of the system, and is forced to design a system capable of working within the constraints of a network which was never intended for digital transmission. The subscriber loop in the PSTN was obviously designed with voice telephony in mind, especially if one considers the latter's rather limited nominal bandwidth requirement of 3,1kHz and upper cutoff frequency of 3,4kHz. In contrast, practical digital transmission techniques rely on spectral components which are an order of magnitude or more higher in frequency than those of voice telephony.

With the above in mind, this chapter introduces the reader to the fundamental properties of a "typical" U-interface transmission line. Complicating matters somewhat, is the fact that a "typical" transmission line may consist of a variety of different cable types and gauges. This fact has been compensated for in most U-interface designs through the use of adaptive techniques which will be covered in a later chapter.

3.2 Basic Transmission Line Theory

A transmission line can be modelled by lumping together an infinite number of sections of the circuit shown in Figure

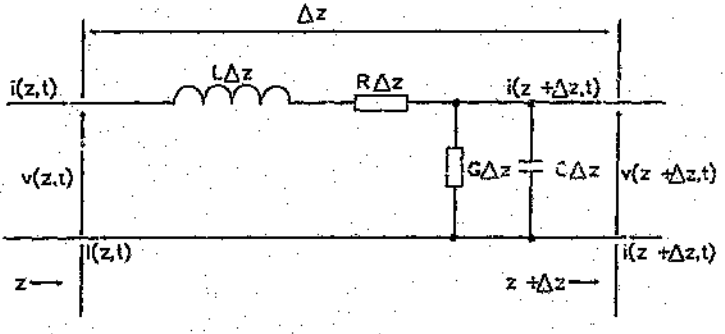


FIGURE 3.1 : EQUIVALENT CIRCUIT OF A TRANSMISSION LINE

ΔZ represents the incremental length of the section and L, R, G and C are known as the primary parameters which completely characterise the transmission line. L, R, G and C are defined as the inductance, resistance, conductance and capacitance per unit length respectively.

The voltage and current on the line is governed by the following set of partial differential equations:

$$\frac{\delta v(z,t)}{\delta z} = -Ri(z,t) - L\frac{\delta i(z,t)}{\delta t} \tag{3.1}$$

$$\frac{\delta i(z,t)}{\delta z} = -Gv(z,t) - C\frac{\delta v(z,t)}{\delta t} \tag{3.2}$$

Assume a transmission line driven by a voltage generator V_g with internal impedance Z_g, and terminated in a load impedance Z_L. For a sinusoidal signal, V_g, the steady state voltage and current on the line are given by:

$$v(z,t) = (A_1 e^{-\gamma z} + A_2 e^{\gamma z}) e^{j\omega t} \tag{3.3}$$

$$i(z,t) = \frac{1}{Z_0}(A_1 e^{-\gamma z} - A_2 e^{\gamma z}) e^{j\omega t} \tag{3.4}$$

A_1 and A_2 are constants dependent on V_g, Z_g and Z_L. The $e^{-\gamma z}$ terms represent harmonic waves travelling in the direction of increasing Z, diminishing exponentially in amplitude as it travels. Similarly, the $e^{+\gamma z}$ terms represent harmonic waves travelling in the direction of decreasing Z, ie. from load to source.

Z_0 and γ are known as the secondary parameters of the line. They are defined as follows:

$$Z_0 = \sqrt{Z/Y} = R_0 + jx_0 = characteristic\ \ impedance \tag{3.5}$$

$$\gamma = \sqrt{ZY} = \alpha + j\beta = propagation\ \ factor \tag{3.6}$$

$$Z = R + j\omega L = series\ \ impedance \tag{3.7}$$

$$Y = G + j\omega C = shunt\ \ admittance \tag{3.8}$$

α and β are known respectively as the attenuation and phase factors. In travelling forward a distance l metres, a wave will be attenuated by αl nepers and undergo a phase shift of βl radians.

The primary parameters of a line have thus far been assumed to be independent of frequency. Over a wide range of frequencies, this assumption does not hold true due to a number of effects, viz; skin effect, proximity effect, and eddy current losses (cf. [7] and [9]).

3.2.1 Skin Effect

The skin effect refers to the tendency of alternating current to concentrate towards the surface of a conductor. The effect can be attributed to a limited penetration of electromagnetic fields into the conductor. The skin effect causes an increase in conductor resistance as well as a decrease in conductor self-inductance with increasing frequencies.

For a plane conducting slab of infinite thickness, the nominal skin depth at an angular frequency W, is given by:

$$\delta = \left(\frac{2}{\omega\mu\sigma}\right)^{1/2} \qquad (3.9)$$

where μ is the conductor permeability and
σ is the conductivity

For a round conductor of finite diameter, the expression for δ is more complex, involving the Bessel functions ber, bei and their derivatives

The correction factor (T_{sr}) for the a.c. resistance (R_{ac}) of a round conductor, taking into account the skin effect, is given by:

$$R_{ac} = T_{sr} * R_{dc} \qquad (3.10)$$

where R_{dc} is the conductor's d.c. resistance.

T_{sr} is defined as:

$$T_{sr} = q/2 * F_r \qquad (3.11)$$

where $$q = \sqrt{2} * \frac{\text{conductor radius}}{\text{skin depth}} \qquad (3.12)$$

and $$F_r = \frac{BER(q)BEI'(q) - BEI(q)BER'(q)}{[BEI'(q)]^2 + [BER'(q)]^2} \qquad (3.13)$$

3.2.2 Proximity Effect

The skin effect factor described by equation 3.11, 3.12 and 3.13 is exact under the condition of uniform magnetic field intensity around the conductor surface. This condition is generally valid in the case of a coaxial cable and open wire line. In the case of a twisted-pair telephone cable, however, the close proximity of the return conductor causes field distortion. This in turn increases the a.c. resistance by a further factor, the proximity effect correction factor for resistance (T_{pr}).

(T_{pr}) can be approximated [10] by the following expression:

$$T_{pr} = \left(1 - \left(\frac{d}{s}\right)^2 a(q)\right)^{-1/2} \qquad (3.14)$$

where d is the conductor diameter,
s is the conductor centre-to-centre spacing.
q is the defined by equation 3.12, and
a(q) is approximated [11] by:

$$a(q) = 0{,}526\ [1 + \tanh\ (1{,}14 - 3{,}078/q)] \qquad (3.15)$$

Combining the skin and proximity effects results in an a.c. resistance given by:

$$R_{a.c.} = R_{d.c.} * T_{sr} * T_{pr} \qquad (3.16)$$

3.2.3 EDDY Current Losses

In a cable containing a large number of current-carrying pairs, additional losses in a particular pair can be attributed to eddy currents in surrounding pairs. The effect can be modelled by an additional component in the conductor resistance, yielding a final estimate for Ra.c. as shown below:

$$R_{a.c.} = R_{d.c.} * T_{sr} * T_{pr} + \Delta R_e \qquad (3.17)$$

ΔR_e has been approximated as follows [12]:

$$\Delta R_e = \Delta R/10 \quad for \quad q > 5$$

$$\Delta R_e = \Delta R/16 \quad for \quad 2{,}5 < q < 5$$

$$\Delta R_e = \Delta R/24 \quad for \quad q < 2{,}5 \qquad (3.18)$$

where $\Delta R = q * \frac{d}{s} * R_{d.c.}$ (3.19)

q, d and s having been previously defined.

3.3 Plotted Cable Characteristics

This section presents graphs of the primary and secondary parameters vs frequency of a variety of cable gauges and of a type typical of a SAPT subscriber loop. The figures quoted are based on those found in reference [13], and although these figures are simulated rather than recorded, they fairly closely approximate real telephony cables.

The SAPT cable-plant is comprised to a large extent of four cable gauges, viz; 26 A.W.G. (0,4mm), 24 A.W.G. (0,5mm), 22 A.W.G. (0,63mm) and 19 A.W.G (0,9mm). The insulating medium is also variable, depending on manufacturer and date of installation, the most common being Polyethelene Insulated Cable (PIC). For the purposes of this report, only PIC cable will be considered.

Figures 3.2 3.3 and 3.4 plot R, L and G versus frequency for the four wire-gauges. Figures 3.5 and 3.6 represent the magnitude of characteristic impedance ($|Z_0|$), while Figure 3.7 represents the phase of Z_0. Figures 3.8 and 3.9 are plots of attenuation (alpha) versus frequency. The graphs have thus far all been plotted at 'room temperature", ie. $21°C$. To gain insight into the effect of temperature variation, Figures 3.10 and 3.11 are plots of attenuation versus frequency, characterising cables at three distinct temperatures, viz; $-18°C$, $+21°C$ and $49°C$.

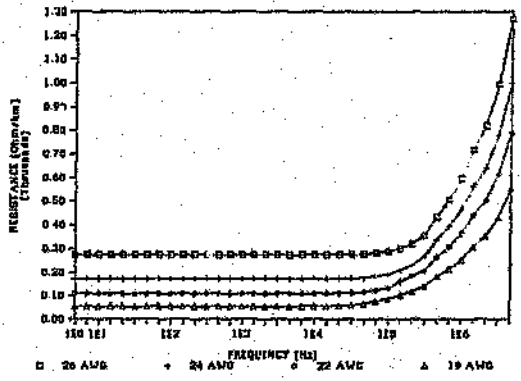


FIGURE 3.2 : PRIMARY PARAMETER "R" vs FREQUENCY

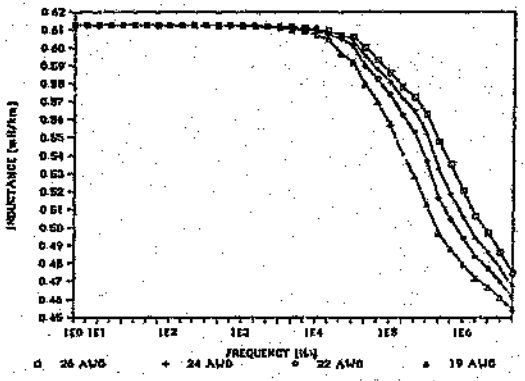


FIGURE 3.3 : PRIMARY PARAMETER "L" vs FREQUENCY

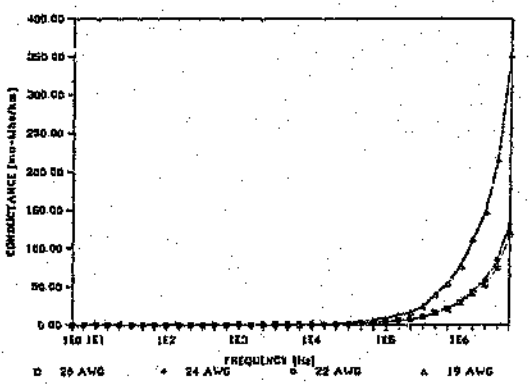


FIGURE 3.4 : PRIMARY PARAMETER "G" vs FREQUENCY

The primary parameters R, L and G as depicted in Figures 3.2, 3.3 and 3.4, all behave more or less as expected. Their values remain fairly constant until particular frequencies when effects such as Skin and Proximity come into play. "G" is seen to be low enough to be neglected at frequencies below 100kHz, whereafter it plays an increasingly more important role especially as regards the thicker gauges.

An important transmission line parameter is that of characteristic impedance as defined by equations (3.5), (3.7) and (3.8). Figures 3.5 and 3.6 depict the characteristic impedance magnitude, $|Z_o|$. Figure 3.5 leaves one in no doubt as to the enormous range of values Z_o can assume, albeit over a fairly broad frequency range of 1Hz to 5MHz. Figure 3.6 is plotted over a smaller frequency range, viz; 10kHz to 5MHz, yet $|Z_o|$ still takes on a considerable

spread in value. This fact, coupled to a substantial variability in the phase of Z_o as shown in Figure 3.7, causes the effectiveness of the impedance matching hybrid (covered in Chapter 5) to be severely limited.

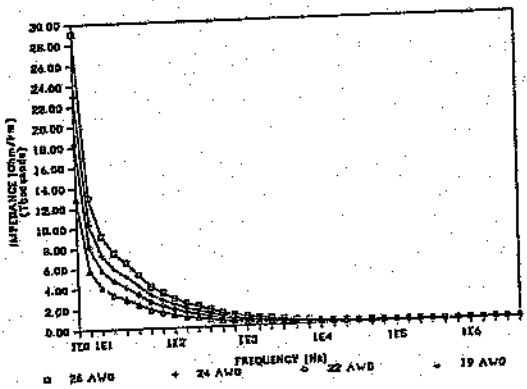


FIGURE 3.5 : |Zo| vs FREQUENCY 1Hz - 5MHz

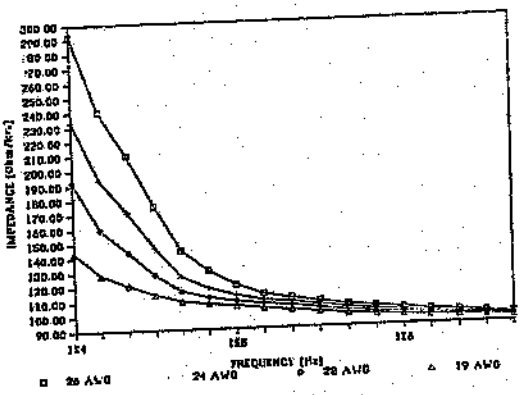


FIGURE 3.6 : |Zo| vs FREQUENCY 10kHz - 5MHz

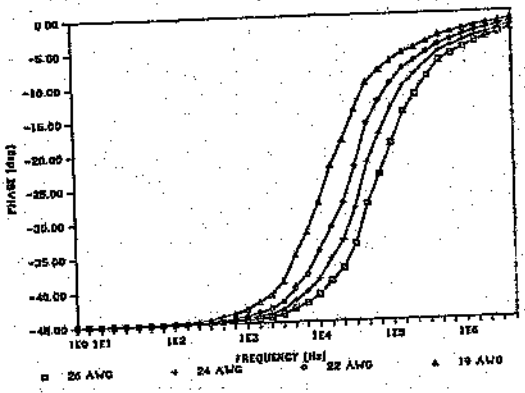


FIGURE 3.7 : PHASE OF Zo

Transmission line attenuation is a parameter of prime concern in the design of the U-interface or any other transmission system for that matter. The importance can be attributed to the fact that the maximum reach of a transmission system (within specific error-rate bounds) is strongly dependent on the attenuation of the transmission medium.

Figures 3.8 and 3.9 represents attenuation versus frequency at "room temperature", $21°C$. As expected, the attenuation is greater for the smaller cable-gauges (mainly as a result of larger values of "R"), and rises fairly sharply above 1MHz.

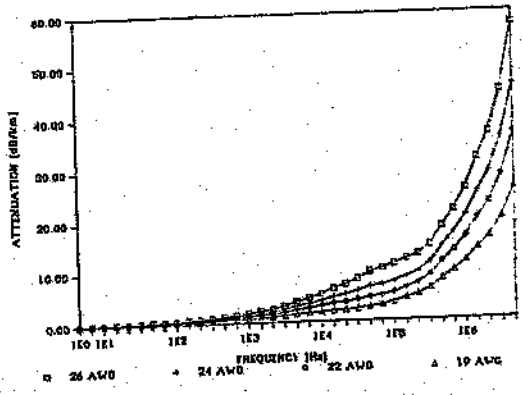


FIGURE 3.8 : ATTENUATION vs FREQUENCY 1Hz - 5MHz

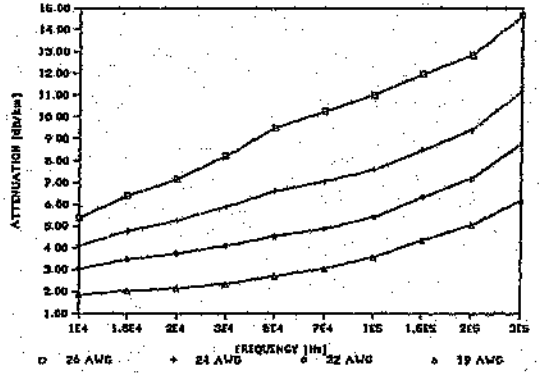


FIGURE 3.9 : ATTENUATION vs FREQUENCY 10kHz - 5MHz

Two approaches are possible when specifying the maximum transmission range or reach of a U-interface. The first involves a detailed specification of the cable-makeup including the primary parameters of each cable-section comprising the subscriber loop. This method is fairly precise but it has one drawback, viz; it requires the availability of cables which conform exactly to the tabulated cable parameters - a somewhat difficult requirement. The second method offers a less rigourous approach, in that precise cable characteristics are not specified. Rather, the maximum reach is specified in terms of the attenuation at a reference frequency over which the transmission system can attain a specified bit-error-rate (BER). The reference frequency most generally specified for the U-interface is 100kHz.

As an example, assume a U-interface is specified to operate with a maximum end-to-end attenuation of 50dB (at 100kHz). In order to appreciate the types of subscriber loops over which the system will operate, the nominal attenuation factors of each of the four common cable gauges must be provided. Table 3.1 quotes these values.

GAUGE [A.W.G.]	ATTENUATION [dB/km]
26	11.0
24	7.6
22	5.4
19	3.6

TABLE 3.1 : Attenuation @ 100kHz vs Cable Gauge

With reference to Table 3.1 therefore, a 50dB attenuation requirement can be met with the following example cable-makeups:

1. 4,5km @ 26 A.W.G.
2. 13,9km @ 19 A.W.G.
3. 2 km @ 26 A.W.G. + 2km @ 24 A.W.G + 2,4km @ 22 A.W.G.

Little consideration is usually given to the effects of temperature on transmission line performance, yet Figures 3.10 and 3.11 indicate that considerable variations in attenuation due to temperature can occur.

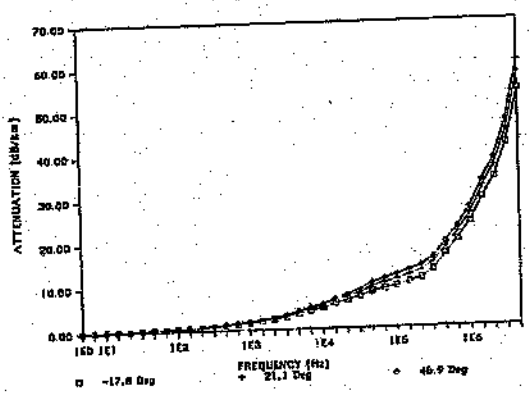


FIGURE 3.10 : ATTENUATION vs TEMPERATURE 1Hz - 5MHz

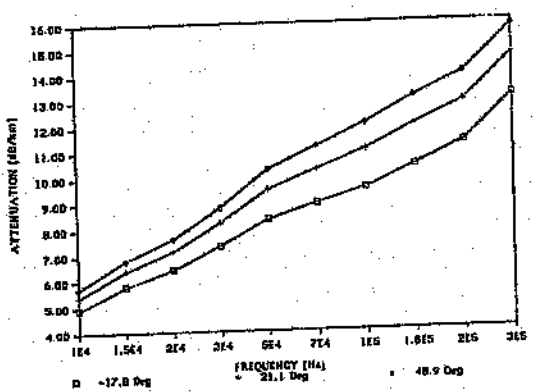


FIGURE 3.11 : ATTENUATION vs TEMPERATURE 10kHz - 5MHz

Table 3.2 lists the attenuation factors as functions of frequency for a 26 A.W.G. cable.

ATTENUATION @ 100kHz [dB/km]	TEMPERATURE [°C]
9,5	-17,8
11,0	+21,1
12,0	+48,9

TABLE 3.2 : Attenuation @ 100kHz vs Temperature

Using the previous example of 50dB of allowable attenuation, the following subscriber loop ranges would be possible (assuming a single length of 26 A.W.G. cable):

$-5,3km \quad @ \quad -17,8°C$

$-4,5km \quad @ \quad 21,1°C$

$-4,2km \quad @ \quad 48,9°C$

While the lower temperature is unlikely to be attained within the South African environment the higher temperature approaching $50°C$ is quite possible in certain areas. This is unfortunate as the maximum attainable range diminishes with increasing temperature. It is for this reason that a margin due to temperature be incorporated into a U-interface range specification.

3.4 The SAPT Subscriber-Loop Profile

An important prerequisite to accessing South Africa's U-interface requirements, is the availabil'ty of subscriber-loop data, viz; cable-makeup and attenuation. Unfortunately, only one survey is known to have been undertaken by SAPT to gather such data. The survey was extremely limited in that is involved the sampling of a mere 400 circuits in a single subscriber area, viz; Pretoria. The results of this survey are presented in the form of pie graphs, shown in Figures 3.12 and 3.13.

Figure 3.12 plots the percentage of sampled circuits which fall within the lengths shown on each slice of the graph. The plot is somewhat incomplete in that no information regarding the make-up of each circuit is provided. Notwithstanding this limitation, the graph shows that 96,7% of all circuits are equal to or less than 5km in length and 92,7% are no greater than 4km in length.

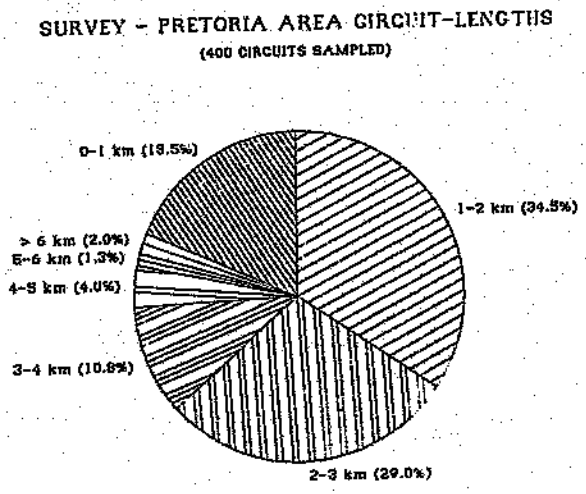


FIGURE 3.12 : SUBSCRIBER LOOP LENGTH STATISTICS

Figure 3.13 is arguably more meaningful than Figure 3.12, in that the former provides insight into the subscriber-loop attenuation statistics. From this data, in principle, a U-interface could be designed to provide a percentage of subscriber population coverage.

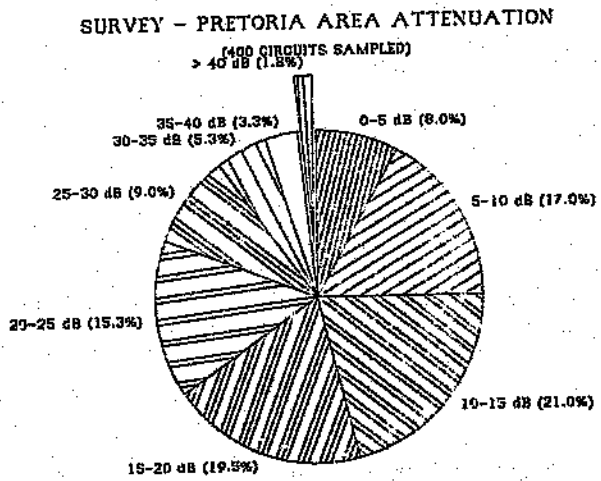


FIGURE 3.13 : SUBSCRIBER LOOP ATTENUATION STATISTICS

Figure 3.13 implies that 91% of the subscriber circuits sampled provide attenuation of 30dB or less while, 98,2% of all circuits provide no more than 40dB attenuation. Figure 3.13 must, however, be viewed within the limitations previously mentioned.

4 LINE CODES

4.1 Introduction

In digital baseband transmission systems, it is generally not acceptable to output digital signals to line in the internal binary format. This is due to the fact that the familiar binary code possesses certain inherent disadvantages, making it unsuitable for a variety of requirements essential to the operation of a transmission line system. To meet these requirements, a multitude of line codes have been devised. Of the large number of line codes which have been proposed, comparatively few have found their way into practical systems.

No one line code is ideal for every application. However, in theory at least, an ideal code should comply with all the following requirements:

The code output to line should be such that it:

a) Conveys adequate timing information.

b) Does not create a standing d.c. potential on the transmission line.

c) Does not contain low frequency signals which would affect AGC performance.

d) Reduces the symbol rate, which in turn limits the maximum line frequencies.

e) Enables error-monitoring to be performed.

4.1.1 Adequate Timing Information

The conveying of adequate timing is generally required to facilitate extraction of clocking information from the received signal. This implies that sufficient zero transitions must be present to maintain the resonant tank circuit or phase locked loop in the receiver. Binary NRZ coding lacks adequate zero-transition content during prolonged strings of ones or zeros.

It must be noted that in the case of line codes which do not possess adequate timing information, other techniques of clock extraction can be made use of, such as, for example, the superposition of a pilot tone over the transmitted symbols. This latter technique is made good use of in the DSP144 chip-set.

4.1.2 Standing D.C. Potential

Examination of the binary NRZ and RZ signals show that both have a significant d.c. component. A binary code is a two level signal in which a binary one represents current or potential to line, while a binary zero represents the absence of current or potential.

Over a short period, the average d.c. potential is given by:

$$\text{Average } d.c. = \frac{\text{Total no of binary ones}}{\text{Total no of bits}} \times \text{peak potential} \quad (4.1)$$

It follows from equation (4.1) that in a normal sequence of binary codes going to line, the average d.c. potential will vary as shown in the example of Figure 4.1.

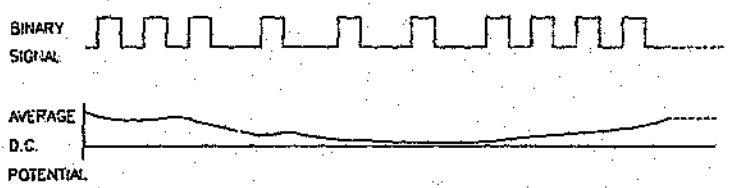


FIGURE 4.1 : AVERAGE DC POTENTIAL OF A RANDOM BINARY SEQUENCE

The undesirable effects of a varying line d.c. potential are as follows:

* Any d.c. signal component tends to disturb the differential between the pre-set threshold level and the average d.c. component of the line signal at any line signal detector in the system.

* The low frequency signal could cause the AGC circuits to operate incorrectly.

* Equalisation of low frequencies is more difficult to achieve.

4.1.3 Reduction in Symbol Rate

Probably the most important requirement of a line code in the context of the U-interface is the reduction in symbol-rate. The advantages of reducing the symbol-rate are essentially twofold. Firstly, Figure 3.8 in Chapter 3 shows that a transmission line's attenuation increases with frequency. The maximum attainable range is therefore dependent on the spectrum of the line code, which for the purposes of line attenuation should be positioned as low in the frequency domain as possible.

Another advantage of symbol-rate reduction, is that of reducing crosstalk (XTALK), ie. the unwanted transfer of energy from one or more disturbing circuits into another circuit known as the disturbed circuit. XTALK will be covered in greater detail in Section 4.6, but suffice it to say that its effects are reduced by reducing the symbol-rate.

In each of the three U-interfaces examined in this report, symbol-rate reduction is achieved through the use of block-codes such as 2B1Q , MMS43 and SU32.

4.1.4 Error Monitoring

While error-monitoring could not be considered an essential function of a digital transmission system, it certainly constitutes a useful supervisory function. By monitoring transmission errors during normal data transmission, the telecommunication administration is able to provide a faster fault-repair turnaround time than would otherwise be the case in the absence of error-monitoring. Certain line codes (eg. MMS43) have built-in error-monitoring facilities arising out of a set of rigid coding rules, which, if violated, constitutes a transmission error. The error-monitoring characteristics of MMS43 will be discussed in a later section.

It must be stated that the absence of error-monitoring capabilities in a line code does not preclude the inclusion of error-monitoring per sé in a transmission system. In fact, neither the ANSI 2B1Q, nor the BT SU32 specifications call for line codes which support error-monitoring. The latter is facilitated through the inclusion of a CRC code built into the frame-structure, which in turn increases the required symbol-rate. This topic will be covered in detail in Chapter 7.

4.2 Alternate Mark Inversion (AMI)

AMI has been rejected for use in most U-interface implementations due to its relatively high symbol-rate. It is included here, however, since it serves as a useful bench-mark against which the other line codes can be compared. Notwithstanding AMI's inferior performance, it still finds many applications due largely to its simplicity of implementation.

Most code requirements can be translated into constraints put upon the Running Digital Sum (RDS) which is defined as [14]:

$$\mathrm{RDS}(k) = \sum_{i}^{k} C_n + RDS(0) \qquad (4.2)$$

where C_n can take on any symbol value,

$RDS(0)$ is an appropriately chosen constant and

$RDS(k)$ is associated with the k'th digit of the m-ary sequency C_n.

In the case of AMI (or any ternary code), C_n can assume the values -1, 0 and +1.

Another line code parameter, the Digital Sum Variation (DSV), is defined as follows:

$$DSV = RDS_{max} - RDS_{min}$$

The DSV denotes an upper bound of the length of strings of like pulses.

AMI is classed as a 1B/1T code since one binary symbol is translated into one ternary symbol. It is not a true ternary but rather pseudo-ternary code, since it comprises 3 states but only 2 values. (A true ternary code has 3 states and 3 values).

The coding rule for the AMI code is quite simple: a "space" (binary zero) is represented by an empty time slot (ternary zero), and a "mark" (binary one) by a positive or negative pulse, the choice of which is made in such a way that successive pulses are of alternative polarity regardless of the number of spaces between them.

A compact tabular representation of a line code is the so-called coding table, which for AMI is shown in Table 4.1 [15].

	OUTPUT WORDS	
BINARY INPUT WORDS	S1	S2
0	0/1	0/2
1	+1/2	-1/1

TABLE 4.1 : Definition of AMI Line Code

S1 and S2 are the two alphabets which comprise the code. The number following the "backslash" after each output word denotes which alphabet is to be used next.

The AMI code has the following properties:

* The average power density spectrum has no d.c. component and very small low-frequency components.

* Coding and decoding circuitry are relatively simple.

* Error-monitoring can be achieved by observing AMI violations.

However, the AMI code is not transparent, which implies that a long sequence of spaces is encoded into an equally long time interval without transmitted energy, resulting in a diminished timing-recovery capability.

The Power Spectral Density (PSD) of AMI is shown in Figure 4.2. This plot (and those of the ensuing 2B1Q, MMS43, 3B2T and SU32 line codes) has been generated by a computer model as described in reference [52]. The following assumptions apply in deriving the PSDs of each code. Firstly, random equiprobable binary data is used to drive each encoder. Secondly, rectangular pulse shaping with a pulse width equal to the baud period has been used in each case. Thirdly, the line coupling network comprises a transformer with a split secondary on the twisted pair side of the line, bridged with a capacitor to allow for the provision of DC power feed. (The component values are stated in [52]). Finally, a launched power of 10mW into 140 ohms is assumed for all the line codes presented.

The baud rate required to support basic access using an AMI line code is 160kbaud.

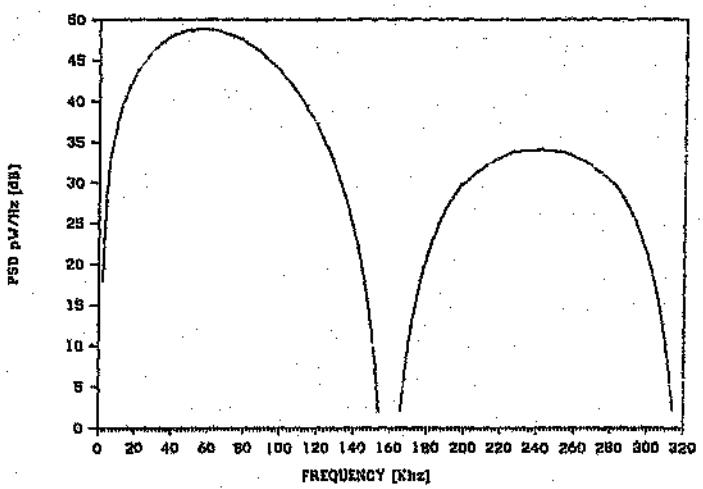


FIGURE 4.2 : POWER SPECTRAL DENSITY OF AMI

4.3 2B1Q

2B1Q (2 binary, 1 quaternary) is a 4-level PAM code comprising no redundancy. The input binary sequence is grouped into pairs of digits called dibits. Each dibit in turn is then converted to a single quaternary symbol which is termed a quat.

The conversion from dibits to quats conforms to Table 4.2 which represents a single alphabet code.

FIRST BIT (SIGN)	SECOND BIT (MAGNITUDE)	QUATERNARY SYMBOL (QUAT)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

TABLE 4.2 : 2B1Q Coding Table

The four values listed under "Quaternary Symbol" in Table 4.2 must be understood as symbol names, not numerical values.

Figure 4.3 presents the PSD of 2B1Q (80kbaud), derived using the methods of [52].

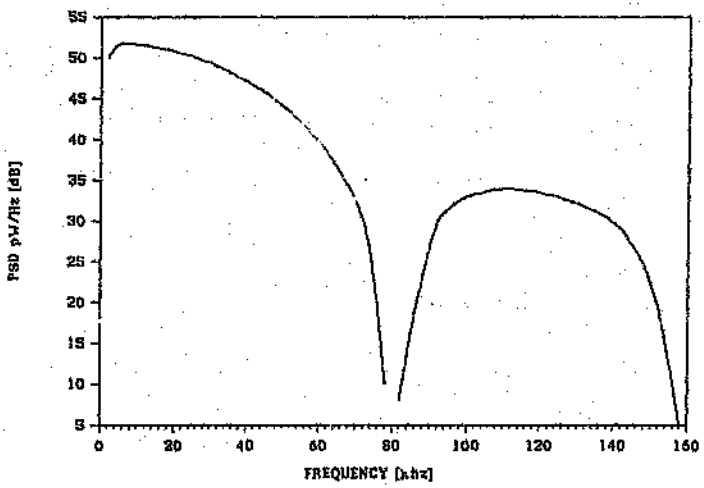


FIGURE 4.3 : POWER SPECTRAL DENSITY OF 2B1Q

4.4 MMS43

MMS43 is a variant of the line code 4B3T (4 binary, 3 ternary). The coding table for MMS43 contains four alphabets S1 to S4 as shown in Table 4.3. The relatively large number of alphabets has the effect of minimising the DSV, which in turn reduces low frequency content in the power spectrum.

	S1	S2	S3	S4
TIME -->				
0001	0-+/1	0-+/2	0-+/3	0-+/4
0111	-0+/1	-0+/2	-0+/3	-0+/4
0100	-+0/1	-+0/2	-+0/3	-+0/4
0010	+-0/1	+-0/2	+-0/3	+-0/4
1011	+0-/1	+0-/2	+0-/3	+0-/4
1110	0+-/1	0+-/2	0+-/3	0+-/4
1001	+-+/2	+-+/3	+-+/4	—/1
0011	00+/2	00+/3	00+/4	-0/2
1101	0+0/2	0+0/3	0+0/4	-0-/2
1000	+00/2	+00/3	+00/4	0-/2
0110	-++/2	-++/3	--+/2	--+/3
1010	++-/2	++-/3	+—/2	+—/3
1111	++0/3	00-/1	00-/2	00-/3
0000	+0+/3	0-0/1	0-0/2	0-0/3
0101	0++/3	-00/1	-00/2	-00/3
1100	+++/4	-+-/1	-+-/2	-+-/3

TABLE 4.3 : MMS43 Coding Table

Unlike 2B1Q, the MMS43 code does allow error-monitoring via code violations. By examining the outputs corresponding to the last 10 binary words in Table 4.3, it is seen that certain outputs are not possible under particular alphabets. For example, if the ternary triplet $++0$ were received, and the alphabet in use was S2, a code violation would be registered, since this particular triplet is invalid in the S2 alphabet. In fact, in each alphabet, $3^3 - 2^4 = 11$ ternary words are invalid and would thus constitute code violations.

Figure 4.4 is a plot of MMS43's PSD.

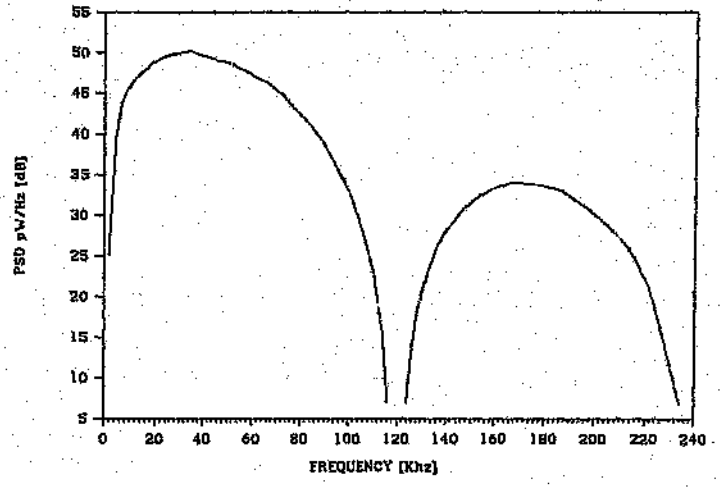


FIGURE 4.4 : POWER SPECTRAL DENSITY OF MMS43

4.5 SU32

SU32 (substitut onal 3B2T) is a variant of 3B2T (3 binary, 2 ternary). It was developed by STC (UK) and is used in this company's U-interface chip set. The code is based on the 3B2T code as shown in Table 4.4 [16]

BINARY INPUT	TERNARY OUTPUT
000	- -
001	- 0
010	- +
011	0 +
100	0 -
101	+ -
110	+ 0
111	+ +
VIOLATION	0 0

TABLE 4.4 : 3B2T Coding Table

The coding scheme comprises essentially 2 stages. The first stage splits the incoming data into groups of 3 bits (tribits), converting each tribit into a two-symbol ternary word according to Table 4.4. The output of the first encoder stage is then compared with the two previously generated symbols. If the present and previous sets of ternary symbols are identical, the present set is replaced by two zero symbols forming a violation of the normal coding rules. If the same three bit word is received again, it will be encoded normally according to

Table 4.4, and the output will continue to alternate between the code word and the violation. From the above discussion, it can be deduced that the maximum number of consecutive identical symbols in the SU32 output is four.

The description of SU32 can be converted into a coding table for processing according to [15]. The tri-alphabet SU32 code is shown in Table 4.5.

BINARY INPUT	TERNARY OUTPUT		
	S1	S2	S3
000	- -/2	0 0/1	- -/2
001	- 0/1	- 0/1	- 0/1
010	- +/1	- +/1	- +/1
011	0 +/1	0 +/1	0 +/1
100	0 -/1	0 -/1	0 -/1
101	+ -/1	+ -/1	+ -/1
110	+ 0/1	+ 0/1	+ 0/1
111	+ +/3	+ +/3	0 0/1

TABLE 4.5 : SU32 Coding Table

Figures 4.5 and 4.6 represent respectively the PSDs of 3B2T and SU32.

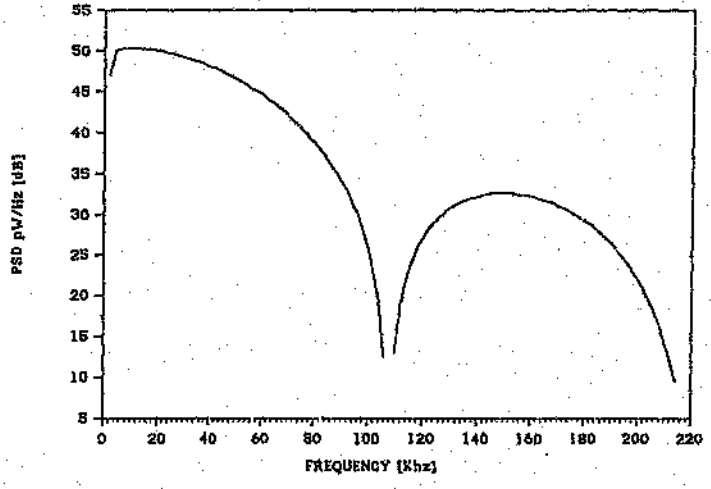


FIGURE 4.5 : POWER SPECTRAL DENSITY OF 3B2T

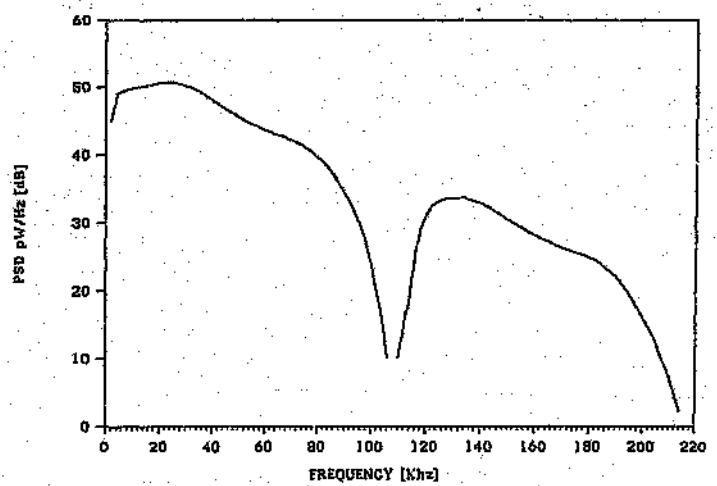


FIGURE 4.6 : POWER SPECTRAL DENSITY OF SU32

The advantage which SU32 offers over 3B2T is essentially in terms of A/D requirements. It has been observed that a small but useful saving in A/D dynamic range may be facilitated through the modification of 3B2T into SU32.

4.6 Line-Code Performance

In the digital subscriber loop, near-end crosstalk (NEXT) is considered to be the dominant source of noise. Figure 4.7 shows a schematic representation of the crosstalk mechanism.

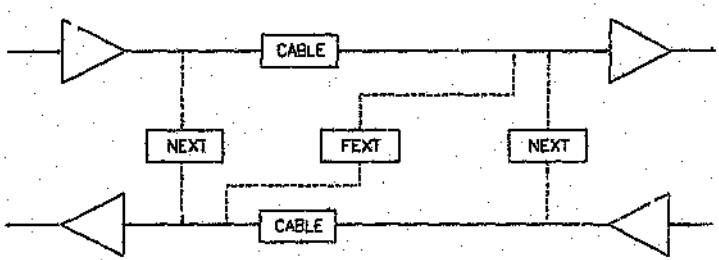


FIGURE 4.7 : CROSSTALK COUPLING MODEL

The crosstalk arises from the coupling between adjacent wire pairs in multicore cables due to cable pair imbalance. It is characterised by a power transfer function which increases with frequency and couples a proportion of the interfering signal power into the system under consideration.

The crosstalk power transfer function has the effect of favouring linecodes which reduce the required bandwidth, and hence result in lower noise power, which in turn offers a greater potential improvement in signal-to-noise ratio. Since the symbol rate of a transmission system with a fixed bit-rate can be reduced by implementing higher level line codes, it would appear that performance increases with increasing code signalling levels. Unfortunately, the number of levels cannot be increased indefinitely, as the spacing between transmitted levels will be reduced, resulting in a lower tolerance to noise at the detector. Figure 4.8 verifies this fact by presenting plots of Signal-to-Noise ratios (S/N) versus symbol error-probability for various m-ary codes (assuming gaussian noise). It can be observed that for a specified error-probability, higher S/N ratios are required for higher values of signalling levels.

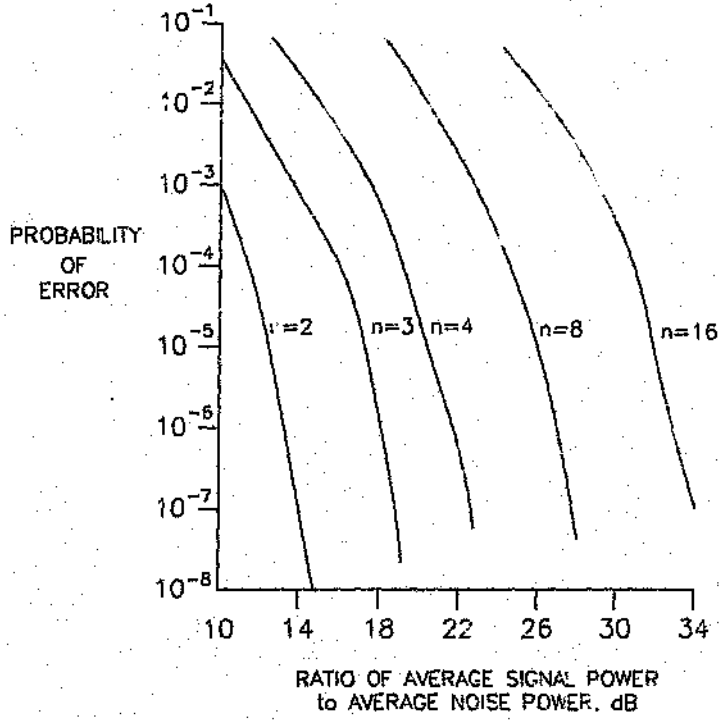


FIGURE 4.8 : SYMBOL ERROR-RATE vs S/N OF N-ARY SIGNALLING

The abovementioned two competing factors suggest that, for a given probability of error, there exists an optimum number of transmitted levels which maximises the range of the subscriber loop.

It is beyond the scope of this report to present the underlying mathematical principles of crosstalk analysis for various line codes. Excellent coverage is given in references [17], [18], [19] and [20]. The results of these investigations are presented below.

The results obtained indicate that substantial improvement in the range performance, over that obtained with 2- or 3-level line codes, is possible with 4- to 8-level signalling, and that further improvement can be obtained by using a DFE as apposed to a linear equaliser. These conclusions concur with those of the ANSI T1.D1 committee in the United states, which has set the standard for the basic access rate of the ISDN U-interface, with the current standard now incorporating a 4-level PAM code, viz; 2B1Q [43].

As far as 3-level codes are concerned, reference [18] predicts an order of increasing performance of AMI, MMS43 and SU32. For a detector signal to noise ratio of 21dB corresponding to a BER of 10^{-7}, the attainable ranges for AMI, MMS43 and SU32 are 45,0dB, 50,3dB and 54,5dB respectively, all ranges being measured at 100kHz.

5 ECHO CANCELLATION AND DFE

5.1 Introduction

There are basically four methods of bidirectional full-duplex transmission on a single pair:

* Frequency Separation.
* Time Separation.
* Dispersion Separation.
* Hybrid and Echo Canceller Separation.

The first three techniques are inferior to the hybrid separation techniques and will therefore be only briefly discussed. The vast majority of systems that achieve the required U-interface transmission range of approximately 50dB at 100kHz rely on the hybrid and echo canceller. The rest of this chapter will therefore be devoted to EC techniques.

The DFE is a structure which is very similar to that of the EC. The DFE which is essential to the operation of any viable U-interface, is therefore included in this chapter.

5.2 Non-EC Separation Techniques

5.2.1 Frequency Separation

Frequency separation or Frequency-Division Multiplexing (FDM) as it is often termed, relies on the choice of different carrier frequencies for each direction of transmission. The carrier frequencies are chosen so that the signal spectra do not overlap. At the receiving end, the far-end signal spectrum is separated out from the local spectrum by bandpass-filtering. The disadvantage of FDM is in terms of bandwidth, which has to be more than twice that of a unidirectional system to allow for practical separation filters. It is therefore not surprising that no U-interfaces employing FDM techniques have emerged.

5.2.2 Time Separation

Time separation, or Time Compression Multiplexing (TCM), known also as burst or ping-pong mode, is a technique wherein the directions of transmission are separated in time.

The input data is loaded into a buffer at the user-rate (eg. 160kbit/s) and then clocked onto the cable-pair at an increased rate (eg. 384kbit/s). The increased line-rate is to allow for data to be received in the reverse direction during periods when near-end data is not being

transmitted. The bursts are timed so that data is alternately transmitted and received, and since the user's data is at a rate less than half the line-rate, full duplex communication from the user's point of view is possible. Burst-mode is wasteful of bandwidth as both cable propagation delay and a guard-time between transmission and reception have to be accounted for.

The TCM system does, however, have one advantage over the EC technique. The transmitters of a number of co-existent systems can be synchronised such that all systems will simultaneously output data to line. This virtually eliminates degradation due to NEXT.

A number of TCM systems, mostly from Japan, have emerged as contenders for the U-interface [23], [24]. These are all considerably inferior in terms of transmission range which are of the order of 40dB at 100kHz. The TCM systems are, however, far simpler in respect of implementation.

5.2.3 Dispersion Separation

Dispersion separation relies on the use of transmitted pulses that are very short in comparison with the time available per bit. In contrast, the shapes normally used for received pulses are dispersed, occupying the whole available time. It is then necessary to gate out part of each received pulse in order to provide sufficient time for a pulse to be transmitted. With this scheme, the loss of signal-to-noise ratio in co nparison with unidirectional transmission can be quite small, even if the phase of the received pulses relative to the transmitted pulses is not known.

5.3 2/4-Wire Conversion By Hybrid Transformer

In an ordinary subscriber loop, 2/4-wire conversion is carried out by a hybrid transformer, according to the principle illustrated in Figure 5.1.

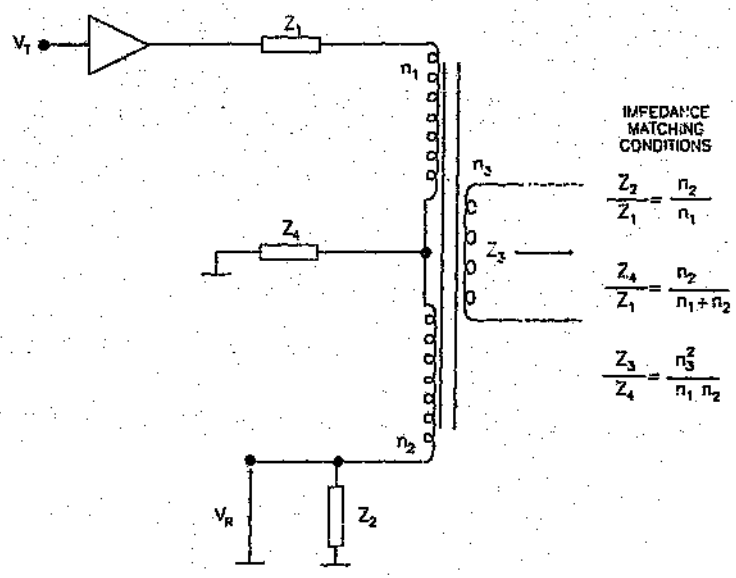


FIGURE 5.1 : HYBRID TRANSFORMER SCHEMATIC

The hybrid transformer has its limitations due to imperfect matching of the terminating impedances, as the line impedance is not perfectly known and cannot be simulated by discrete components. Because of the hybrid mismatch, the transmitted signal V_T, reaches the receive impedance Z_2, feeding a component of V_T viz; V_R to the receiver. Another part of the transmitted signal is reflected from impedance irregularities in the two-wire circuit. This reflected component also ends up in the near-end receiver. The combined effect of both imperfections can be thought of as "echoes".

Whereas in speech, the echoes are only harmful if large delays exist such as in satellite communications, in full-duplex data communications, the echo can be disastrous. The delay of the echo in this case is unimportant; only the relative level is relevant.

5.4 Echo Cancellation

Echo Cancellers can be broadly divided into 2 categories depending on the reference signal against which the cancelled signal output is compared. These are:

(A) Zero-reference Echo Cancellers (ZREC'S) [25] - [31]

(B) Nonzero-reference Echo Cancellers (NZREC's) [32] - [33]

The former scheme is based on minimising the cancelled signal (or receiver input following the Echo Canceller) when no far-end signal is present. The far-end signal can be seen as a source of additive noise which should be uncorrelated with the near-end signal. However, due to the usually present far-end signal during full-duplex transmission (ie. "double-talking"), ZREC's require a small step size thus implying large convergence times [33].

Their main advantage over the NZREC's is their independence of receiver performance as they do not require the receiver output as part of the adaptation process. This in turn simplifies the EC's implementation.

The NZREC algorithms are in theory not affected by the far-end signal, since the adaptation reference is derived from the receiver output, ie. ideally the far-end signal is subtracted from the adaptation reference signal. They therefore offer faster convergence than the ZREC algorithms at the expense of increased EC complexity.

The three U-interface implementations covered in this report are all based on the ZREC. This chapter will therefore focus attention only on zero-reference algorithms.

The ZREC algorithms differ primarily in terms of their rates of convergence and complexity of implementation. The rate of EC convergence is in general an important design criterion since it gives an indication of the efficiency of the transmission system. A large convergence time means "wasted time" in terms of data throughput, as reliable communication is not possible during EC convergence. In the ISDN basic access context, large EC convergence times imply large call set-up times.

There exist a number of algorithms for updating EC coefficients, viz; Least-Mean-Squares (LMS), Lease-Squares (LS) and Fast-Kalman.

The LMS algorithm is the most commonly used in U-interface implementations as the other two algorithms suffer from numerical instability and computational complexity. This report will therefore direct attention at the LMS algorithm alone.

5.4.1 LMS Algorithm

Consider Figure 5.2, a block diagram of the near-end full-duplex Network Terminating Unit (NTU).

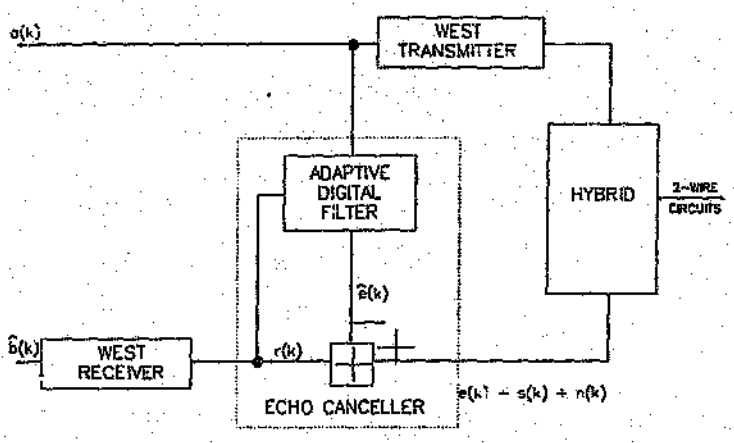


FIGURE 5.2 : NEAR-END NETWORK TERMINATING UNIT (NTU)

The echo signal is modelled as a result of "leakage" through the hybrid from transmitter to receiver. This "echo path" is essentially linear and is largely time-invariant; the small variations being due to environmental fluctuations, eg. temperature.

The echo cancellation is achieved by providing a parallel path between transmitter and receiver in which a replica $\hat{e}(k)$ of the echo $e(k)$ is formed using an adaptive filter, the former then being subtracted from the echo signal leaving only a residual echo $r(k)$ given by:

$$r(k) = s(k) + n(k) + e(k) - \hat{e}(k) \qquad (5.1)$$

where $s(k)$ is the received East signal (or far-end signal), and $n(k)$ is additive noise. The residual signal $r(k)$ forms both the input to the West receiver and the reference signal used by the adaptive filter for updating its coefficients.

An analysis is now made of the adaptive transversal filter with N taps and N coefficients in a bid to arrive at an expression yielding information about the filter's Mean-Squared-Error (MSE) as well as the rate of convergence to a steady state value.

The Transversal Filter (TF) is shown in block diagram form in Figure 5.3. It should be noted that A_i represents the adaptation unit for the i'th filter coefficient. T represents a unit delay, ie. a delay of one symbol of the input data a(k).

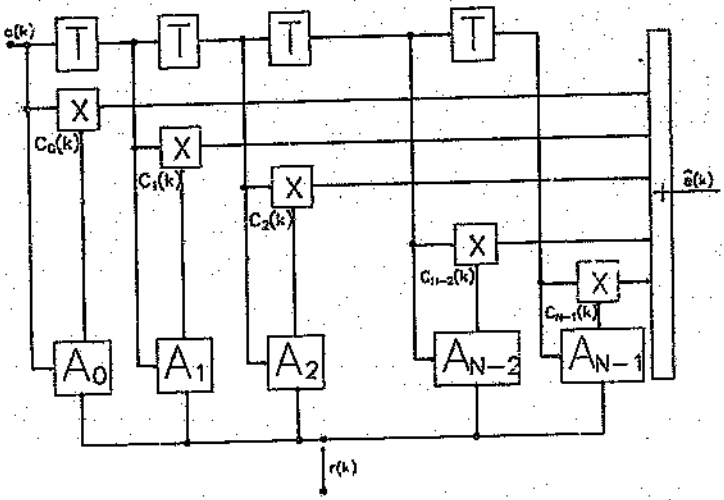


FIGURE 5.3 : ADAPTIVE TRANSVERSAL DIGITAL FILTER

It is common practice in adaptive filter analysis to work with matrices, and hence the following vectors are introduced:

* The West input vector:

$$a_k = [a(k),\ a(k-1).....a(k-N+1)]^T \tag{5.2}$$

* The echo path vector:

$$g = [g(0),\ g(1).....g(N-1)]^T \tag{5.3}$$

* The coefficient vector:

$$C_k = [C_0(k),\ C_1(k).....C_{N-1}(k)]^T \tag{5.4}$$

* The East input vector:

$$b_k = [b(k),\ b(k-1).....b(k-M+1)]^T \tag{5.5}$$

* The transmission path vector:

$$h = [h(0),\ h(1).....h(M-1)]^T \tag{5.6}$$

where ^{T} denotes matrix transposition.

Note that in the definition of the echo path vector g, the assumption is made that the impulse response g(i) is zero for $N \leq t < 0$. The order of the TF (ie. no. of taps) must therefore be chosen so as to accommodate this assumption.

L ·the concept of discrete-time convolu..on:

e(k) can be expressed as:

$$e(k) = \sum_{m=0}^{N-1} a(k-m)g(m) \tag{5.7a}$$

$$=> \quad e(k) = a(k)g(0) + a(k-1)g(1) + \ldots . a(k-N+1)g(N-1)$$

$$\text{or} \quad e(k) = a_k^T \cdot g \tag{5.7b}$$

Similarly, for the received signal

$$s(k) = b_k^T \cdot h \tag{5.8}$$

and from Figure 5.3, the echo replica

$$\hat{e}(k) = a_k^T \cdot C_k \tag{5.9}$$

Recalling (5.1) and combining the received signal s(k) with the noise signal n(k) to form a signal u(k) such that:

$$u(k) = s(k) + n(k) \tag{5.10}$$

$$\text{Hence} \quad r(k) = e(k) - \hat{e}(k) + u(k) \tag{5.11a}$$

$$=> \quad r(k) = a_k^T \cdot g - a_k^T \cdot C_k + u(k) \tag{5.11b}$$

$$\text{and} \quad r(k) = a_k^T (g - C_k) + u(k) \tag{5.11c}$$

Since it is desired to minimise the energy or mean-square value of the residual signal r(k), $\rho(k)$ is defined such that:

$$\rho(k) = E\{r(k)^2\} = E\{[a_k^T (g - C_k) + u(k)]^2\} \tag{5.12}$$

where E{} denotes mathematical expectation.

At this stage the following assumptions are made:

a) Vectors α_k and C_k are statistically independent.

b) West-end and East end input data symbols a(k) and b(k) as well as the noise component n(k) are statistically and mutually independent.

c) a(k) and b(k) can have values +1 and -1 with equal probability.

With the above assumptions in mind, (5.12) then becomes:

$$\rho(k) = E\{(g-C_k)^T \alpha_k \alpha_k^T (g-C_k)\} + E\{u^2(k)\}$$

$$\Rightarrow \quad \rho(k) = E\{(g-C_k)^T (g-C_k)\} + U \tag{5.13}$$

where $U = E\{u^2(k)\} = variance\ of\ u(k)$ (5.13a)

Note from (5.13) that p(k) or the Mean-Square (MS) value of the residual signal r(k) is a quadratic function of the filter coefficients, which has an absolute minimum U for $C_k = g$ [25].

This fact is borne out by equations (5.7b) and (5.9) where for $C_k = g$, it is noted that e(k) = $\hat{e}$(k), and equation (5.11c) where r(k) = u(k) with the same constraint, $C_k = g$.

Consider now the gradient of $\rho(k)$ with respect to C_k which is defined as:

$$\nabla\rho(k) = \left[\frac{\delta\rho(k)}{\delta C_0(k)}, \frac{\delta\rho(k)}{\delta C_1(k)}, \ldots\ldots, \frac{\delta\rho(k)}{\delta C_{N-1}(k)}\right]^T \tag{5.14}$$

From (5.13):

$$\rho(k) = (g-C_k)^T (g-C_k) + U$$

and from (5.3 and (5.4):

$$(g-C_k)^T = [g(0)-C_0(k),\ g(1)-C_1(k), \ldots\ldots, g(N-1)-C_{N-1}(k)]$$

hence:

$$\rho(k) = [g(0)-C_0(k),\ g(1)-C_1(k),\ldots\ldots,g(N-1)-C_{N-1}(k)] \begin{bmatrix} g(0)-C_0(k) \\ g(1)-C_1(k) \\ \vdots \\ \vdots \\ \vdots \\ g(N-1)-C_{N-1}(k) \end{bmatrix} + U$$

$$\Rightarrow$$

$$\rho(k)=[g^2(0)-2g(0)C_0(k)+C_0^2(k)]+[g^2(1)-2g(1)C_1(k)+C_1^2(k)]+\ldots\ldots$$

$$\ldots\ldots+[g^2(N-1)-2g(N-1)C_{N-1}(k)+C^2_{N-1}(k)] + U$$

Using (5.14) we obtain for $\nabla\rho(k)$:

$$\nabla\rho(k) = -2[g(0)-C_0(k),\ g(1)-C_1(k),\ldots\ldots,g(N-1)-C_{N-1}(k)]^T$$

or

$$\nabla\rho(k) = -2(g-C_k) \tag{5.15}$$

$\nabla\rho(k)$ can also be derived from (5.11c) and (5.12) to obtain:

$$\nabla\rho(k) = -2E\{r(k)a_k\}$$

Comparing (5.15) and (5.16), it is seen that $\nabla\rho(k)$ gives a direct measure of the difference between the actual value and the optimum value of the coefficient vector, the latter being equal to the impulse response of the echo path. The value of (5.16) can therefore be gauged by noting that an estimation of the gradient can be obtained from a knowledge of r(k) and a(k), the residual echo plus far-end signal and the input signal respectively.

We can thus adapt the coefficients of the digital TF according to the following algorithm:

$$C_{k+1} = C_k - \alpha\nabla\rho(k) \tag{5.17}$$

where α is the so-called "amplification constant".

If $\nabla\rho(k)$ can now be estimated using (5.16), the coefficient vector C_k can be interactively updated using (5.17) and a fixed value of α. Equation (5.17) characterises the "Least Mean Square Error Gradient" algorithm, or simply the LMS algorithm.

There exist three alternatives to estimating $\nabla\rho(k)$ as given by (5.16) within a finite time span, ie. within a finite number of iterations. These estimation procedures give rise to three different adaptation algorithms known as the:

* Correlation Algorithm (CA)
* Sign Algorithm (SA)
* Stochastic Interation Algorithm (SIA)

Each algorithm will be briefly considered.

5.4.1.1 Correlation Algorithm (CA)

$\nabla\rho$ can be approximated by a finite time average over K data intervals:

$$\nabla\rho(k) = -\frac{2}{K} * \sum_{l=k+1-K}^{k} r(l)\alpha l \qquad (5.18)$$

With this scheme, the updating is generally performed once every K data intervals. The block diagram of the CA is shown in Figure 5.4.

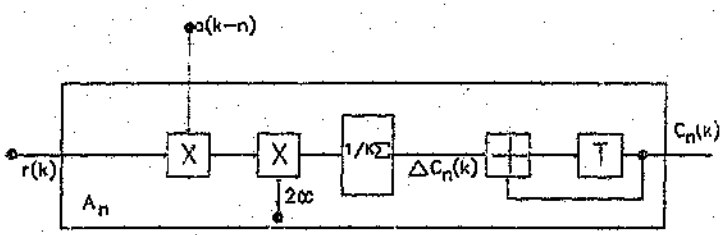


FIGURE 5.4 : BLOCK DIAGRAM OF CA ADAPTATION UNIT

5.4.1.2 Sign Algorithm (SA)

A still simpler implementation, albeit at the expense of a rougher approximation to (5.16), is based on the so-called Sign Algorithm (SA). The SA takes into account the sign of the residual echo only, as can be seen from its characteristic equation below:

$$\nabla\rho(k) = -2\ sign\ [r(k)]\alpha_k \qquad (5.19)$$

Equation (5.19) is implemented as shown diagrammatically in Figure 5.5.

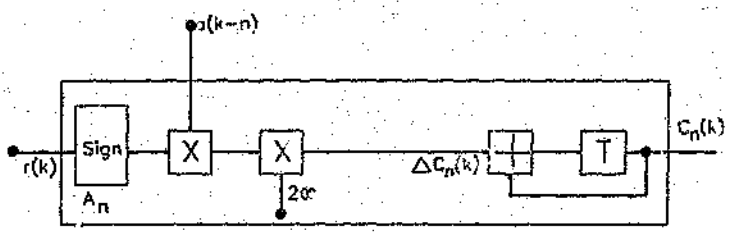


FIGURE 5.5 : BLOCK DIAGRAM OF SA ADAPTATION UNIT

5.4.1.3 Stochastic Iteration Algorithm (SIA)

This algorithm is somewhat simpler than the correlation algorithm from an implementation point of view, since the SIA dispenses with the averaging function (ie. K=1 in (5.18)) at the expense of a rougher approximation to the gradient as indicated by (5.16). The approximation to (5.16) then yields:

$$\nabla \rho(k) \approx -2r(k)a_k \qquad (5.20)$$

The block diagram describing the algorithm is shown in Figure 5.6. This algorithm will now be dealt with in greater detail.

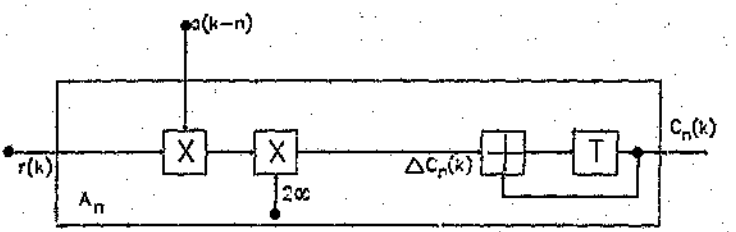


FIGURE 5.6 : BLOCK DIAGRAM OF SIA ADAPTATION UNIT

The SIA is characterised by a combination of (5.17) and (5.20):

$$C_{k+1} = C_k + 2\alpha r(k)a_k \qquad (5.21)$$

Consider now the difference between the received echo e(k) and the simulated echo $\hat{e}(k)$ as a function of time. From (5.7b) and (5.9):

$$e(k) - \hat{e}(k) = a_k{}^T(g - C_k) \qquad (5.22)$$

Denoting $\epsilon(k)$ as the MS value of (5.22), one obtains:

$$\epsilon(k) = E\{[e(k) - \hat{e}(k)]^2\} = E\left\{\left[\alpha k^T (g - C_k)\right]^2\right\} \quad (5.23)$$

Recalling the assumptions made earlier about the statistical independence of the data symbols a(k) as well as the independence of a_k from C_k, one can then simplify (5.23) to:

$$\epsilon(k) = E\{(g - C_k)^T (g - C_k)\} \quad (5.24)$$

From (5.11c) and (5.21):

$$C_{k+1} = C_k + 2\alpha a_k r(k)$$

$$= C_k + 2\alpha a_k \left[\alpha k^T (g - C_k) + u(k)\right] \quad (5.25a)$$

Replacing K in the above equation with K-1, one obtains:

$$C_k = C_{k-1} + 2\alpha a_{k-1} \left[\alpha k-1^T (g - C_{k-1}) + u(k-1)\right]$$

$$\Rightarrow \quad C_k = C_{k-1} + 2\alpha a_{k-1} \alpha k-1^T (g - C_{k-1}) + 2\alpha a_{k-1} u(k-1) \quad (5.25b)$$

Substituting (5.25b) into (5.24) and applying the previous assumptions about statistical independence, one finds:

$$\epsilon(k) = (1 - 4\alpha + 4\alpha^2 N) E\{(g - C_{k-1})^T (g - C_{k-1})\} + 4\alpha^2 N U \quad (5.26)$$

where U is defined as $E\{u^2(k)\}$.

Combining (5.24) and (5.26) one obtains:

$$\epsilon(k) = (1 - 4\alpha + 4\alpha^2 N)[\epsilon(k-1) + 4\alpha^2 N U] \quad (5.27)$$

This linear first-order difference equation can be solved to yield:

$$\frac{\epsilon(k)}{U} = (1 - 4\alpha + 4\alpha^2 N)^k \left[\frac{\epsilon(0)}{U} - \frac{\alpha N}{1 - \alpha N}\right] + \frac{\alpha N}{1 - \alpha N} \quad (5.28)$$

The dynamic behaviour of the Stochastic Interation Algorithm is fully described by (5.28), keeping in mind the assumptions made previously.

The following conclusions about equation (5.28) can now be made:

1. For $\epsilon(k)/U$ to converge as k rises without bound, it is evident that:

$$|1 - 4\alpha + 4\alpha^2 N| < 1 \tag{5.29a}$$

(5.29a) yields the following set of inequalities:

$$4\alpha - 4\alpha^2 N < 2 \tag{5.29b}$$

and

$$4\alpha - 4\alpha^2 N > 0 \tag{5.29c}$$

(5.29b) yields complex values for α (for $N \geq 1$) but (5.29c) yields the inequalities:

$$\alpha > 0$$

and

$$1 - \alpha N > 0 \quad or \quad \alpha < 1/N$$

This results in the following requirement for convergence:

$$0 < \alpha < 1/N \tag{5.29d}$$

2. After convergence, the ratio of residual echo to uncancellable signal is given by:

$$\delta = 10\log_{10}\frac{\epsilon(\infty)}{U} = 10\log_{10}\frac{\alpha N}{1-\alpha N} \quad [dB] \tag{5.30a}$$

since the first product on the RHS of (5.28) decreases as k increases under the condition of (5.29d), and vanishes in the limit, ie. after infinitely many iterations.

3. A "convergence rate number" ν_{20}V20 is introduced, representing the number of iterations required to reduce the residual echo by 20 dB, provided the linear portion of the curve represented by (5.28) is considered, ie.

$$\frac{\epsilon(k)}{U} \gg \frac{\alpha N}{1 - \alpha N}$$

With the above assumption in mind, (5.28) approximates to:

$$\frac{\epsilon(k)}{U} \approx (1 - 4\alpha + 4\alpha^2 N)^k \left(\frac{\epsilon(k)}{U} - \frac{\alpha N}{1-\alpha N}\right)$$

$$\approx (1 - 4\alpha + 4\alpha^2 N)^k \; \epsilon(k)/\epsilon$$

since $(1 - 4\alpha + 4\alpha^2 N)^k \leq 1$

$$\Rightarrow \quad \epsilon(k)/\epsilon(0) \approx (1 - 4\alpha + 4\alpha^2 N)^k$$

$$\log_{10}[\epsilon(k)/\epsilon(0)] \approx k[\log_{10}(1 - 4\alpha + 4\alpha^2 N)]$$

$$\Rightarrow \quad k \approx \frac{\log_{10}[\epsilon(k)/\epsilon(0)]}{\log_{10}(1-4\alpha+4\alpha^2 N)} \qquad (5.30b)$$

but $k = \nu_{20}$ *for* $10\log_{10}[\epsilon(k)/\epsilon(0)] = -20[dB]$

hence $\log_{10}[\epsilon(k)/\epsilon(0)] = -2 \qquad (5.30c)$

and $\nu_{20} = \frac{-2}{\log_{10}(1 - 4\alpha + 4\alpha^2 N)}$ *[iterations]* $\qquad (5.30d)$

Equation (5.30d) can be further simplified by noting that for practical applications, a very small ratio of residual echo to un :: cellable signal is required. From (5.30a) therefore, t' following requirement must be met:

$$\alpha N \ll 1 \qquad (5.31)$$

Incorporating (5.31), ν_{20} approximates to:

$$\nu_{20} \approx \frac{-2}{\log_{10}(1 - 4\alpha)} \approx \frac{-4.605}{\ln(1 - 4\alpha)} \qquad (5.32a)$$

From the Taylor Series for Logarithmic Functions:

$$\ln(x) = 2\left\{\frac{(x-1)}{(x+1)} + \frac{1}{3}\frac{(x-1)^3}{(x+1)^3} + \frac{1}{5}\frac{(x-1)^5}{(x+1)^5} + \ldots\right\} \quad (x>0)$$

hence $\ln(1 - 4\alpha) \approx 2\left\{\frac{-4\alpha}{2 - 4\alpha}\right\} \qquad (5.32b)$

since higher order terms are negligible for practical values of α.

Combining (5.32a) and (5.32b) :

$$v_{20} \approx \frac{4.605-(2-4\alpha)}{8\alpha}$$

$$\approx \frac{1,15 - 2,3\alpha}{\alpha}$$

$$v_{20} \approx \frac{1,15}{\alpha} \qquad since\ \alpha \ll 1 \qquad (5.32c)$$

Equation (5.30a) and (5.32c) show the importance of the amplification constant α. Its value determines both the rate of convergence and the minimum residual echo that can be obtained. This is graphically verified in Figures 5.7 and 5.8 where (5.28) has been plotted for different values of α and N.

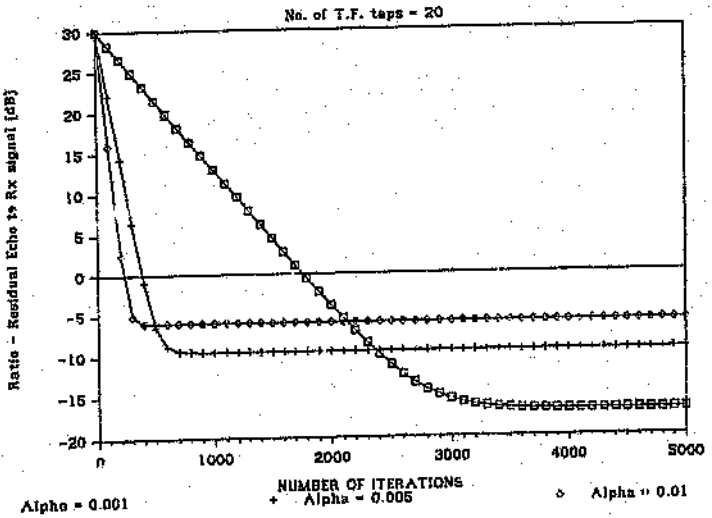


FIGURE 5.7 : CONVERGENCE OF SIA vs ALPHA

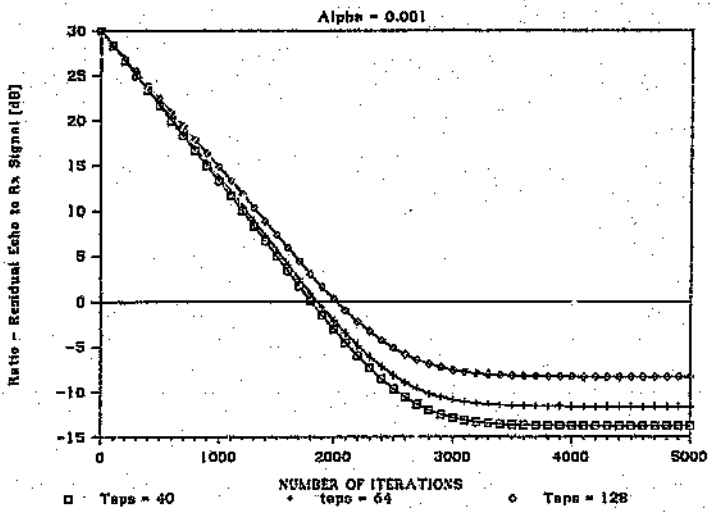


FIGURE 5.8 : CONVERGENCE OF SIA vs NO TAPS

Note what at first glance seems to be a strange outcome from varying N, the order of the TF (ie. the number of filter taps). Both the rate of convergence and the minimum residual echo improve with a reduction in N, ie. the fewer the taps, the better the performance. This apparent paradox is resolved if one considers a fundamental assumption made when defining the echo path vector g, represented by equation (5.3). For this equation to be valid, the impulse response of the echo path is required to be fully contained within the "span" of the TF ie:

$$g(i) = 0 \qquad 0 > i \geq N$$

All components of the transmitted signal occurring after a time NT where T is the input data symbol interval, will not be cancelled by the filter and will appear at the input of the receiver as an additional "uncancellable" signal. This obviously increases the overall residual echo.

One also notes that since the filter output is a weighted accumulation of all the tap outputs, the fewer the taps, the smaller the order of the input vector a_k. Now from equation (5.12), $(g-C_k)$ varies only slowly with time as convergence is approached and U(k) is assumed to be statistically stationary. The MS value of the residual signal r(k) is therefore dependent on the length (ie. order) of the input vector which is in turn governed by N, the number of filter taps (ie. $\rho(k)$ increases with an increase in N).

We summarise by stating that the fewer the taps, the better the performance of the EC, provided that there are sufficient taps to "completely" span the impulse response of the echo path.

It has been found by Verhoeckx et Al [25] that the Correlation and Stochastic Interation algorithms offer comparable performance in terms of minimum mean-square error and rates of convergence if the value of α is chosen carefully in each case. The added complexity of the former algorithm thus makes it unattractive as a solution to the echo cancellation problem. It has also been mentioned that the sign algorithm yields large convergence times if the requirement of a low minimum mean-square error is to be met.

It is for this reason that the SIA is the preferred algorithm in many present-day EC implementations.

5.5 Decision Feedback Equalisation (DFE)

It could be argued that the DFE performs a completely different functions to that of the EC, and should therefore be covered in a separate section. The fact of the matter is, however, that the structure of the DFE is so similar to that of the EC, that the former warrants a discussion in conjunction with the EC.

Furthermore, every commercially available U-interface chip-set has a DFE incorporated to counter the moderately severe Intersymbol Interference (ISI) encountered on the subscriber loop at U-interface signalling rates. A brief introduction to this topic is thus appropriate. For an indepth coverage of DFE principles and techniques, the reader is referred to the multitude of available literature [22], [34], [35] and [36].

The DFE has, as its predecessor, the linear equaliser. The latter has facilitated the design of equipment capable of successfully combating ISI in PAM data transmission systems operating over noisy linear channels in which delay distortion predominates. Since linear equalisers are required to compensate for the channel characteristics in the presence of noise, they cannot be expected to perform optionally over severely frequency-attenuating channels such as is the case with the subscriber loop.

High signalling rates over voiceband cable channels place signal energy well within the badly attenuated portion of the transmission spectrum, resulting in severe ISI correctable by linear methods only at the expense of a significant degradation in SNR.

A linear equaliser, when combined with a "bootstrap" technique, commonly referred to as "decision feedback", can yield significant performance improvement. The DFE, as this combination is known, provides for samples of the pulse tails (postcursors) interfering with

subsequent or future data symbols to be subtracted without incurring a significant noise penalty. The effect of pulse tails (precursors) which occur prior to detection and interfere with past symbols is minimised by a conventional linear equaliser.

The DFE, depicted in Figure 5.9, consists of two sections, a feedforward section and a feedback section. Both have taps spaced at the symbol interval T. The input to the feedforward section is the received signal sequence {Vk}. In this respect, the feedforward section is identical to a conventional linear TF. The feedback section has as its input the sequence of decisions on previously detected symbols $\left\{\tilde{I}_k\right\}$. Functionally, the feedback section is used to remove that part of the ISI from the present estimate caused by previously detected symbols.

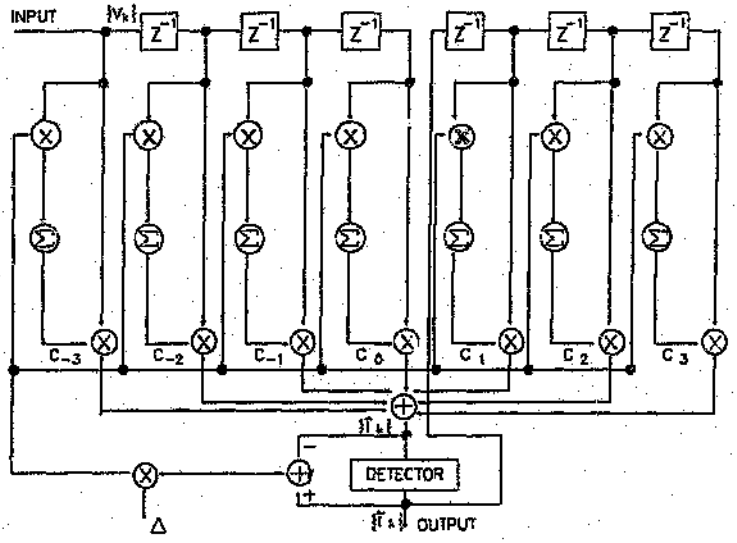


FIGURE 5.9 : BLOCK DIAGRAM OF DFE

In considering the joint behaviour of a DFE and EC, Falconer, Mueller and Weinstein [37] have indicated that convergence is critically dependent on the received signal to echo power ratio. It is for this reason that an AGC circuit often precedes a DFE so as to feed the latter with a relatively constant received signal level. The inclusion of an AGC will be verified in Chapter 8 during the discussion on current U-interface chip-sets.

6 PULSE DENSITY MODULATION

6.1 Introduction

The Pulse Density Modulator (PDM) is a device suitable for Analogue to Digital Conversion (ADC). One may justifiably believe that the ADC block in a U-interface chip-set is an implementation concern and does not warrant a chapter of its own. The reason for including a chapter on an ADC technique, and specifically on the PDM principle is simply for the following reason. For an ISDN to become a reality and not merely a technological curiosity, it has to be economically viable. The bulk of the cost of an ISDN lies in the Digital Subscriber Loop (DSL) since this cost is multiplied by the number of subscribers. One way of reducing this cost is by making use of pre-existing telephony cables for transmission; this aim has already been met by specifying an elaborate U-interface for 2-wire working. Another way of reducing DSL costs is by ensuring the lowest possible cost for the terminating transceivers at each end of the DSL. This requirement suggests VLSI implementation, and preferably a single chip. The most cost-effective technology for fabricating a system of the complexity of a U-interface on a single integrated circuit, with transistor counts approaching 100 000, is CMOS technology. Now, while CMOS is ideally suited to digital implementation, it is capable of supporting analogue functions albeit at the expense of a high chip-area overhead. It would therefore be preferable to minimise the analogue requirements in preference to digital circuits. This fact highlights the importance of the PDM ADC in U-interface chip designs, since the PDM is capable of achieving a relatively high sampling rate (100kHz) and resolution (12 bits) with minimal analogue circuitry requirements. This will be verified in the following sections.

6.2 Principle of Operation

The theory of PDM operation is well covered in the literature [38]-[41]. The complete ADC can be divided into two parts, viz; the pulse density modulator which performs the actual function of analogue to digital conversion and the Conversion Filter (CF) which provides both filtering and coding of the PDM output data stream. Since the CF forms an integral part of the ADC, it will also receive brief attention in this chapter.

The PDM embodies the Sigma-Delta Modulator ($\Sigma\Delta M$) as part of its design, and in attempting to understand and explain the PDM, it is necessary to try to unravel the workings of the $\Sigma\Delta M$.

6.2.1 Sigma Delta Modulator ($\Sigma\Delta M$)

The $\Sigma\Delta$M shown in Figure 6.1 is one of a number of devices which performs pulse density modulation. The simplicity and low cost of a PDM involving the use of a $\Sigma\Delta$M makes it very suitable for analogue to digital conversion as the front-end to a digital signal processing system.

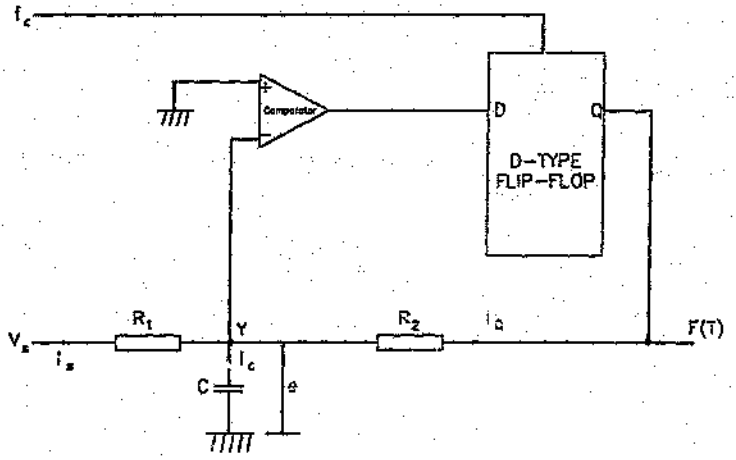


FIGURE 6.1 : SIGMA-DELTA MODULATOR

The output signal F(T), where T is the clock period ($1/F_c$), consists of a stream of pulses with mark or space density proportional to the relative amplitude of the analogue input signal, V_s. The total number of pulses available in a given time is defined by the clock frequency F_c, therefore for each additional mark there will be one less space and vice versa. In the limit, the output will consist of all-marks or all-spaces and will indicate peak positive or peak negative input signals respectively. The zero input signal will produce the idle level code of equal mark-space ratio ie. a square wave output signal.

The input signal is approximately defined by the following formula:

$$V_{sav} = \frac{M-S}{M+S} \qquad (6.1)$$

where M and S denote respectively the number of marks and spaces in a given pattern repetition period.

It can be shown that a given d.c. signal will produce a unique pulse pattern and an output which can only be accurately demodulated in digital processing by integrating the output pulses over an integral number of pattern repetition periods. A time varying input signal will obviously produce a multiplicity of output pulse patterns of different lengths and shapes and hence it would be impossible to employ a sampling period which could cater for all pattern configurations. The resulting errors will therefore introduce quantising noise due to time-sampling.

The circuit in Figure 6.1 is based on the principles of the inverting amplifier which has a transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{-R_2}{R_1} \qquad (6.2)$$

The point Y operates as a virtual earth due to the high gain amplifier. For the purpose of this discussion, R_1 and R_2 will be assumed to be equal.

The inclusion of the D-type flip-flop in the feedback path will not invalidate (6.2) provided that the loop gain is high and "D" is transparent to the input signal. The clocked flip-flop produces a pulse density modulated stream of pulses which incorporates the low frequency signal component equal and opposite in polarity to V_s. The high frequency components are highly attenuated by the RC filter. The latter also acts as an integrator for signal frequencies greater than the cutoff frequency, F_0. At these frequencies, the device behaves as a $\Sigma\Delta M$. For signal frequencies below F_0, signal integration does not occur and the device technically ceases to be a $\Sigma\Delta M$ but still performs pulse density modulation.

The action of the $\Sigma\Delta M$ can be explained as follows, with reference to Figure 6.1:

Let the input signal be V_s, assuming that the flip-flop output is normalised to ± 1 (initially $+1$), and assume V_s to be a d.c. signal such that $0 \leq V_s \leq 1$. If the charge on C is disregarded, then a current I_s, approximately equal to V_s / R_1 will flow in R_1 due to the comparator's negative input being very nearly at earth potential. This current will increase the voltage e at point Y in a positive direction as C increases its charge. However, when e has crossed the decision level of the comparator, the flip-flop will be triggered on the next rising edge of a clock pulse, outputting "-1" at Q. This will in turn draw current I_Q in R_2 which will be maintained for the duration of "p" clock pulses. Since $|T_Q| > |I_s|$ for any $|V_s| < 1$, the voltage e will fall until it recrosses the decision level, at which point the flip-flop will again change sign at the next positive transition of the clock, and the whole cycle recommences. This sequence of events is depicted in Figure 6.2.

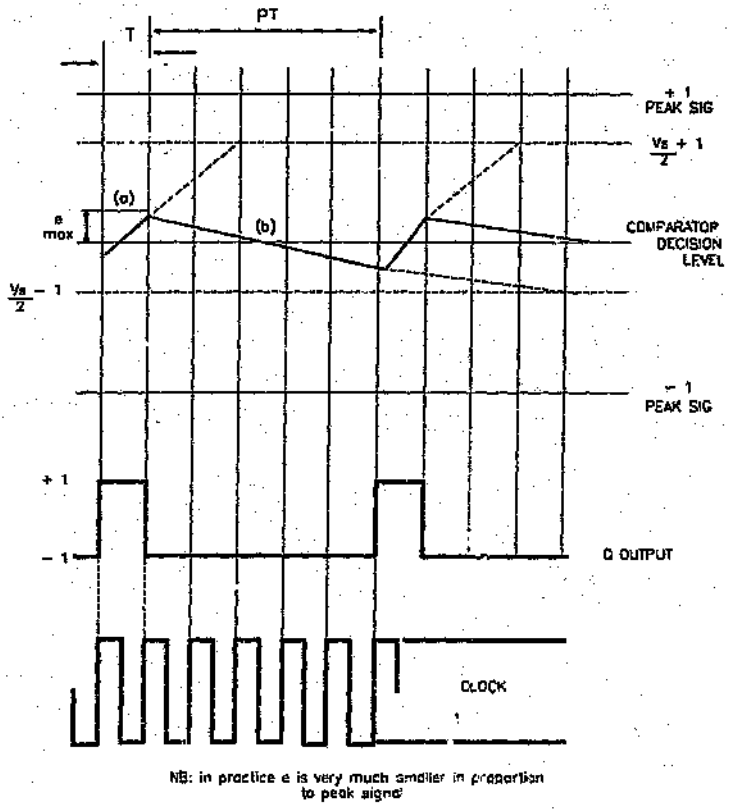


FIGURE 6.2 : SIGMA-DELTA MODULATOR WAVEFORMS

The total current I_c, flowing into C with positive flip-flop output Q is $(1+V_s)/R$, and with negative output is $-(1-V_s)/R$. Note that Q can only change sign on the positive edge of a clock pulse, and therefore the waveform at point Y is synchronised to the clock independently of the input signal. Also, the pattern of pulses is dependent on the relative slopes of segments (a) and (b) in Figure 6.2, which in turn are dependent on the instantaneous input signal amplitude. The slopes are shown as linear but in practise, are expotential.

"p" can be determined as follows:

$$e_{max} \approx \frac{I_c T}{C} \approx \frac{(1+V_s)T}{RC} \quad for \ slope \ (a) \tag{6.3}$$

$$\approx \frac{(1-V_s)pT}{RC} \quad for \ slope \ (b) \tag{6.4}$$

Equating (6.3) and (6.4) we obtain:

$$p = \frac{(1 + V_s)}{(1 - V_s)} \tag{6.5}$$

Rearranging terms, (6.5) yields:

$$V_s = \frac{(p - 1)}{(p + 1)} \tag{6.6}$$

However, from equation (6.1) the average value of the output data stream (ie. pulse density) is given by:

$$V_{av} = \frac{(p - 1)}{(p + 1)} \tag{6.7}$$

$$\text{hence} \quad V_s = V_{av} = \frac{M-S}{M+S} \tag{6.8}$$

where "M" and "S" are as previously defined.

Equation (6.8) shows that the pulse density modulation represents the signal amplitude and is independent of signal frequency over the working range of the device.

For $R_1 = R_2$ the maximum input signal must be equal to the magnitude of the flip-flop output which is assumed to be ± 1. The predominant output condition will be opposite in polarity to the input signal.

For $V_s = +1$:-

$$e^{+}_{max} = 2T/RC \tag{6.9}$$

and for $V_s = -1$:-

$$e^{-}_{max} = -2T/RC \tag{6.10}$$

Therefore:

$$V_{p-p} = 2e_{max} = 4T/RC \tag{6.11}$$

where V_{p-p} is the peak-to-peak voltage swing at the inverting input to the comparator.

6.2.2 PDM Quantisation and Noise

The encoding process of the ΣΔM differs from that of a successive approximation coder, and hence has a different noise pattern. It can be shown that the SNR of a successive approximation coder is proportional to the signal amplitude [42]. The ΣΔM, however, does not provide equal quantising steps in its transfer function. This is due to the so called threshold effect which results in zero coding changes for small increases in signal amplitude. Owing to unique output pulse patterns, threshold steps exist at certain fixed signal amplitudes. The noise structure obtained from ΣΔM is therefore more "ragged" than that of "linear" coders, and small signal amplitudes are vulnerable to distortion at certain points on the modulator transfer function.

The dynamic range of a ΣΔM may be extended by increasing the clock frequency, thereby making the steps smaller, and enlarging the integrator time constant, if the latter is not already at its practical limit.

It should be mentioned that ΣΔM does not suffer from overload distortion as does delta modulation. The reason for this is that in ΣΔM, the maximum peak-to-peak excursion of the composite integrated voltage "e" will not exceed 4T/RC which is a comparatively small quantity. The input to the comparator therefore does not track the input signal, thereby preventing overload distortion.

6.3 Conversion Filter (CF)

As stated in the introduction, the CF performs the dual function of filtering and coding the PDM data stream, and it is pertinent to know why this is required. The PDM data consists of a high frequency stream of pulses whose density is modulated by the applied analogue signal as previously described. The pulse stream is not coded, but modulated and with each pulse having equal weighting with its neighbours, the analogue signal can be recovered by means of a simple low-pass analogue filter. The process of coding implies that the data stream must be reduced to a sequence of N-bit words with binary weighting format. The word repetition rate is much lower than the original PDM data rate, and for the U-interface, ranges from 80 to 120 kwords/sec (ie. the respective baud rates). It is also imperative that the word length shall be sufficient to achieve the required performance (ie. generally ≥ 12 bits/word).

The coding circuit typically also provides filtering which is the prime consideration in the design of a PDM A/D for the following reasons. The PDM data stream not only carries the wanted analogue signal but also the inherent quantising noise from the PDM, and this noise rises in amplitude to half the clock frequency, as shown in Figure 6.3.

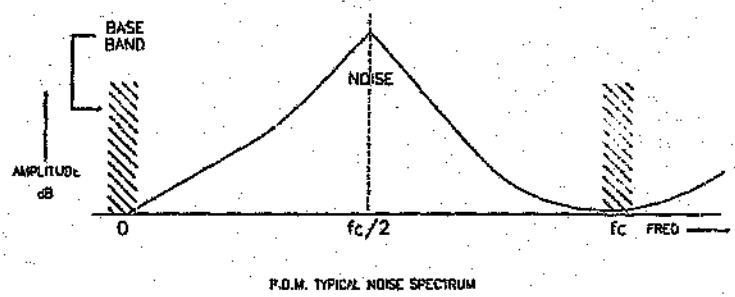


FIGURE 6.3 : SPECTRUM OF PDM DATA OUTPUT

The spectrum is typical for this type of A/D and the high frequency outband components could be effectively removed by a simple analogue low-pass filter-demodulator. However, for digital processing, the sampling action causes the outband noise to fold down into the baseband, and hence a digital filter must be interposed to minimise this noise before sampling occurs.

Digital filters operate on discrete time and amplitude samples; the former give rise to sidebands around the sampling frequency and its harmonics, and the latter to quantisation of the signal waveform. An ideal digital filter would only transmit the basebands shown in Figure 6.3, in which case residual outband noise would be zero, which is of course impossible to achieve in practice.

A typical DF for use in a U-interface is constructed with one or more equal length transversal filters in cascade. Figure 6.4 shows a sketch of attenuation vs frequency for a typical cascaded TF conversion filter.

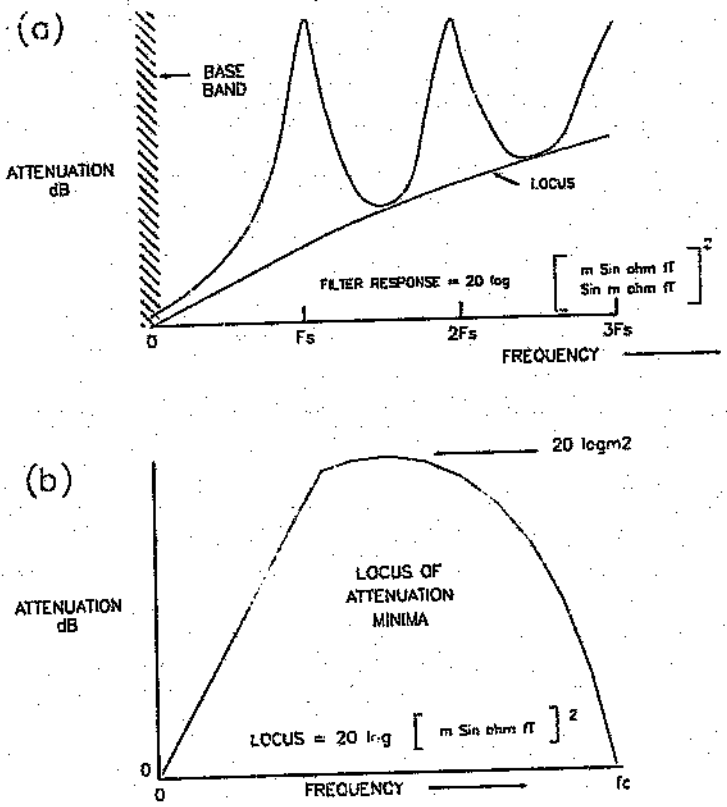


FIGURE 6.4 : ATTENUATION vs FREQUENCY FOR A TYPICAL CF

7 U-INTERFACE SPECIFICATIONS

7.1 Introduction

At the time of writing this project report, no CCITT specification for a U-interface was available. In fact it is quite probable that no such specification will appear in the future, as it is generally accepted that individual administrations will be responsible for specifying the U-interface to suit the local conditions.

The research underlying this report has concentrated on the practical validation of three U-interface specifications, viz. ANSI T1.601 [43], Deutsche Bundespost FTZ 1R220 [44] and the British Telecom specification for Digital Access to the ISDN [45].

Each specification in turn deals with the requirements of a system capable of providing full duplex data transmission at a rate of 144kbit/s (2B+D) over a single 2-wire metallic cable. The specifications do not lay down precise transmission system parameters such as EC adaptation algorithms and filter lengths, but rather concentrate on ensuring inter-working compatibility between systems conforming to the same specification. This allows manufacturers the freedom of choosing implementations and architectures which suit their technologies and product ranges.

This chapter will be structured as follows: A number of features governing the design of a U-interface transmission system will be described according to the three abovementioned specifications. In each case, an attempt will be made to highlight the fundamental differences between the requirements.

The specifications for a U-interface can be broadly divided into 3 areas, viz. transmission method, supervisory and maintenance functions, and electrical characteristics. Each area will now be dealt with in turn.

7.2 Transmission Method

The transmission system conforming to each of the three specifications is designed to operate on a 2-wire twisted metallic cable pair composed of mixed gauges. The requirements apply to a single Digital Subscriber Line (DSL) consisting of an LT, a cable pair without the inclusion of loading coils, and an NT.

All three systems have a number of aspects in common as regards the transmission method. Each system relies on echo cancellation for the separation of data directions, and operation is independent of the wiring polarity of the twisted pair. All three systems also use Pulse Amplitude Modulation (PAM) for modulating the binary digits onto the line.

An additional similarity is that of the scrambling and descrambling algorithm employed respectively in the transmitter and receiver of each transceiver. From the discussion on echo cancellation in Chapter 5, it was made clear that from a theoretical point of view, the transmitted and received symbols need to maintain both self- and mutual-independence (ie. low auto- and cross-correlation). One method of achieving symbol independence is by introducing a scrambling function into the modulation process and subsequent descrambling in the demodulator.

The scramblers and descramblers employed in all three U-interface specifications rely on the Linear Feedback Shift Register (LFSR) principle. The latter is based on a Shift Register (SR) clocked at the data rate. The scrambler/descrambler is then formed by adding (modulo 2) outputs from a number of SR taps to the incoming data stream, and feeding the composite signal back into the SR. The position of the feedback taps uniquely define the scrambling polynomial, and in the case of the U-interface, the polynomials for the two directions of transmission need to be different so as to minimise cross-correlation between transmitted and received symbols.

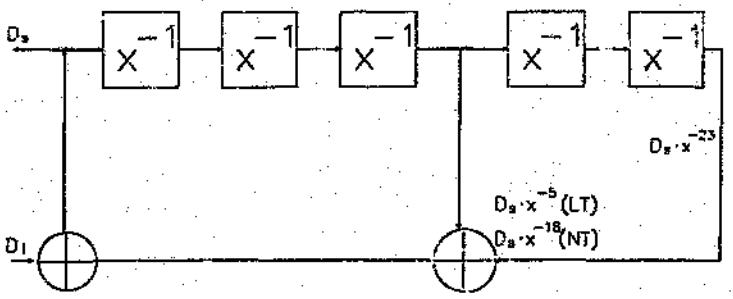
All three specifications require identical scrambling polynomials for a particular direction of transmission. These are as follows:

$$1 \oplus x^{-5} \oplus x^{-23} \qquad (LT-NT)$$

and $$1 \oplus x^{-18} \oplus x^{-23} \qquad (NT-LT)$$

where $\oplus$ implies modulo 2 addition.

The scramblers at either end are implemented as shown diagrammatically in Figure 7.1, while the descramblers are as shown in Figure 7.2.

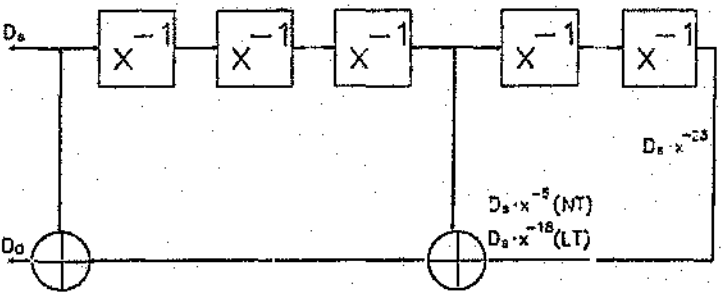


where Di denotes the input bit stream,

Ds denotes the scrambled bit-stream; and

x^{-1} denotes a delay of 1 bit period

FIGURE 7.1 : U-INTERFACE SCRAMBLER



where Do denotes the descramble output

FIGURE 7.2 : U-INTERFACE DESCRAMBLER

The final similarity between the three systems is that of timing synchronisation. All three specifications require that the DSL operate in a master-slave mode with the NT slaved to the received network signal ie. the NT transmit signal is synchronised to the receive clock. The LT on the other hand, is synchronised to the exchange master clock.

7.2.1 ANSI Transmission Method

The specified line code, 2B1Q , has already been covered in section 4.3. The user-data bitstream, comprised of two 64kbit/s B-channels and one 16kbit/s D-channel, is grouped

into pairs of digits (dibits) for conversion to quaternary symbols called quats. In each dibit, the first and second bits are called the sign and magnitude bit respectively. The relationship of the B- and D-channel bits to quats is shown in Figure 7.3.

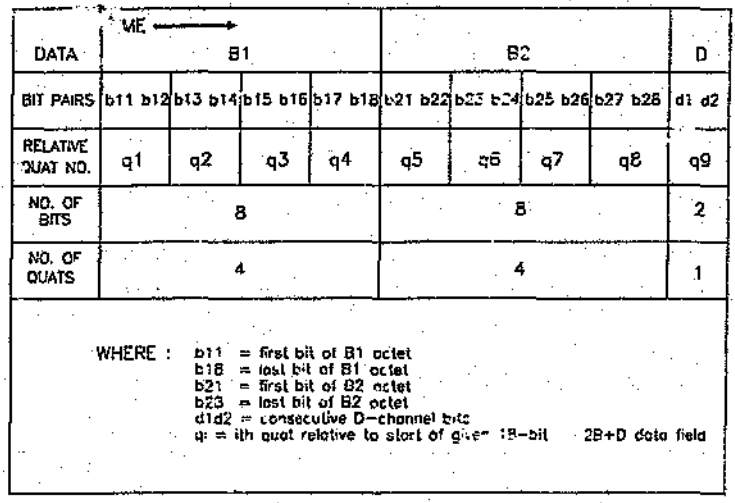


FIGURE 7.3 : ENCODING OF 2B+D BIT FIELDS

The B- and D-channel bits are scrambled, whereafter each successive dibit in the binary data-stream is converted to a quaternary symbol according to Table 4.2. After 2B1Q encoding, the quats are shaped via a transmit Low Pass Filter (LPF) before being output to line via a line driver.

At the receiver, each quat is converted to a pair of bits according to a reversed Table 4.2, descrambled and finally formed into bitstreams representing the B- and D-channels. Figure 7.3, when reversed, provides for proper placing of the B- and D-channels.

The symbol rate of the NT transmitter is required to be in the range of 80kbaud ± 5ppm, assuming a received symbol rate of 80kbaud.

7.2.1.1 ANSI Frame Structure

The ANSI frame structure is shown in Figure 7.4. It comprises 8 basic frames which constitute a superframe. A frame of 1,5ms nominal duration comprises 120 quats. The superframe therefore has a repetition period of 12msec.

		FRAMING	2B+D	OVERHEAD BITS (M1–M6)					
	QUAT POSITIONS	1–9	10–117	118s	118m	119s	119m	120s	120m
	FT POSITIONS	1–18	19–234	235	236	237	238	129	240
SUPER FRAME NO.	BASIC FRAME NO.	SYNC WORD	2B+D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B+D	eoc_{01}	eoc_{02}	eoc_{03}	act / act	1	1
	2	SW	2B+D	eoc_{04}	eoc_{11}	eoc_{12}	deact / ps1	1	febe
	3	SW	2B+D	eoc_{13}	eoc_{14}	eoc_{15}	1 / ps2	crc_1	crc_2
	4	SW	2B+D	eoc_{16}	eoc_{17}	eoc_{18}	1 / nt/m	crc_3	crc_4
	5	SW	2B+D	eoc_{01}	eoc_{02}	eoc_{03}	1 / csc	crc_5	crc_6
	6	SW	2B+D	eoc_{04}	eoc_{11}	eoc_{12}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{13}	eoc_{14}	eoc_{15}	1	crc_9	crc_{10}
	8	SW	2B+D	eoc_{16}	eoc_{17}	eoc_{18}	1	crc_{11}	crc_{12}
2,3....									

LT-to-NT DIRECTION / NT-to-LT DIRECTION

FIGURE 7.4 : ANSI FRAME STRUCTURE

The first nine symbols of each frame is a Synchronisation Word (SW), which is essentially a Barker word. The superframe m rker is a synchronisation word which is inverted relative to the Basic Frame SW, and is denoted Inverted Synchronisation Word (ISW).

The SW and ISW comprise the following nine-symbol sequence:

$$SW = +3,+3,-3,-3,-3,+3,-3,+3,+3$$

$$ISW = -3,-3,+3,+3,+3,-3,+3,-3,-3,$$

Following the SW and ISW, the next 108 quats convey the 2B+D user-data at a rate of 72kbaud or 144kbit/s. Except during startup, the 2B+D channel is transparent to user-data.

The last 3 symbols (6 bits) of each frame form a 4kbit/s M-channel for maintenance and supervisory purposes. The 3 symbols are shown in quat positions 118 to 120 inclusive (Figure 7.4), but are split into sign and magnitude components for convenience (eg. overhead bits M1 and M2 collectively form quat 118).

The M-channel is sufficiently complex to warrant separate coverage, and will therefore be discussed in section 7.3.

7.2.2 Bundespost Transmission Method

The specified line code is MMS43 (cf section 4.4). The incoming binary data-stream is encoded according to Table 4.3, with the selection of a particular alphabet being dependent on the sum of the previous 3 symbols comprising a code word.

Error recognition in the decoder is based on a violation of the RDS which is updated after every received symbol. This built-in error recognition capability of the MMS43 line code sets it apart from the 2B1Q and SU32 codes which both involve a bandwidth overhead for the inclusion of a Cyclic Redundancy Check (CRC) word.

Careful inspection of Table 4.3 will indicate that the reception of a ternary word comprising three zeros causes a problem, as no binary translation exists for this case. The MMS43 coding rules, however, require a "000" ternary word to be decoded into the binary equivalent of "0000".

The line symbol rate is specified as 120kbaud ± 1ppm, assuming a transmit and receive clock synchronised to the exchange.

7.2.2.1 Bundespost Frame Structure

The frame structure in the LT-to-NT direction as required by the Bundespost specification is shown in Figure 7.5.

1 T1	2 T1	3 T1	4 T1	5 T1	6 T1	7 T1	8 T1	9 T1	10 T1	11 T1	12 T1
13 T1	14 T1	15 T1	16 T1	17 T1	18 T1	19 T1	20 T1	21 T1	22 T1	23 T1	24 T1
25 T1	26 T1	27 T1	28 T2	29 T2	30 T2	31 T2	32 T2	33 T2	34 T2	35 T2	36 T2
37 T2	38 T2	39 T2	40 T2	41 T2	42 T2	43 T2	44 T2	45 T2	46 T2	47 T2	48 T2
49 T2	50 T2	51 T2	52 T2	53 T2	54 T2	55 T3	56 T3	57 T3	58 T3	59 T3	60 T3
61 T3	62 T3	63 T3	64 T3	65 T3	66 T3	67 T3	68 T3	69 T3	70 T3	71 T3	72 T3
73 T3	74 T3	75 T3	76 T3	77 T3	78 T3	79 T3	80 T3	81 T3	82 T4	83 T4	84 T4
85 M	86 T4	87 T4	88 T4	89 T4	90 T4	91 T4	92 T4	93 T4	94 T4	95 T4	96 T4
97 T4	98 T4	99 T4	100 T4	101 T4	102 T4	103 T4	104 T4	105 T4	106 T4	107 T4	108 T4
109 T4	110 +	111 +	112 +	113 −	114 −	115 −	116 +	117 −	118 −	119 +	120 −

FIGURE 7.5 : BUNDESPOST FRAME STRUCTURE (LT-to-NT)

The frame comprising 120 ternary symbols has a duration of 1ms. The 120 symbols are made up as follows:

* 108 symbols of 2B+D user data.
* 11 symbols comprising Barker code for both symbol and frame synchronisation.
* 1 symbol facilitating maintenance and supervisory functions.

The scrambling and descrambling operation as described in section 7.2 is only applied to the 108 user-data symbols and not the Barker code or maintenance and supervisory symbol.

The composition of the T_i symbols (i = 1.....4) as depicted in Figure 7.5, is shown in Figure 7.6. The 108 user-data symbols are split into four equally structured groups each of 27 ternary symbols (corresponding to 36 bits).

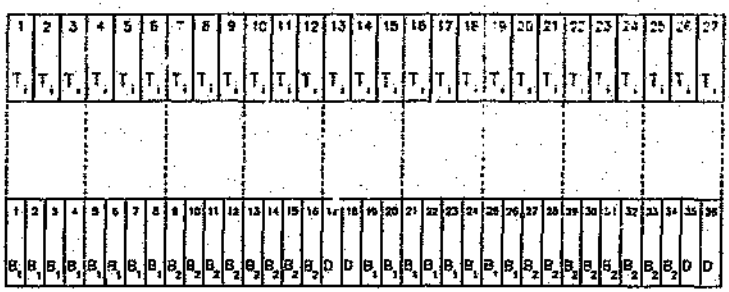


FIGURE 7.6 : POSITION OF 2B+D DATA IN A TERNARY GROUP

The 11-symbol synchronisation word differs as a function of the transmission direction, and is specified as follows:

* Downstream (ie. LT to NT) = +++—+—+-

* Upstream (ie. NT to LT) = -+--+---+++

Note that the synchronisation words are binary coded (ie. absence of "zero" symbols). This improves the performance of the timing-extraction system in the presence of noise.

In order to reduce correlation between the two directions of transmission, a 60-symbol offset is introduced between the transmitters at either end of the DSL. The transmitted Barker code in the NT to LT direction therefore occupies positions 50 to 60 in the frame.

7.2.3 British Telecom Transmission Method

The specified line code is SU32, a 3B2T variant (cf section 4.5), developed by STC Technology Ltd (STL). The encoding process follows the rules of Table 4.5.

The BT transmission method differs primarily from those of ANSI and the Bundespost in its technique of timing generation and extraction. Whereas the latter two systems rely on the technique of Barker codes for both symbol and frame synchronisation, the BT specification calls for pilot tone superposition and intentional SU32 code violation for symbol and frame synchronisation respectively.

The pilot-tone technique for extracting a received symbol clock is beyond the scope of the main body of this report, but is briefly covered in Appendix A. However, it is worth mentioning at this point that the pilot-tone technique requires no additional bandwidth as in the case of the Barker code technique, where the latter requires considerable overhead to facilitate the inclusion of the SW in the frame structure.

Frame synchronisation relies on the reception of a sequence of six consecutive ternary zeros. With reference to the coding rules of SU32 as described in section 4.5, it should be evident that under error-free conditions, a maximimum of four consecutive zeros can be output to line (eg. consider the encoding of "110" repeated twice, followed by 100). In principle therefore, the reception of six consecutive zeros would identify the start-of-frame marker with a high degree of confidence.

The line symbol-rate is 108kbaud ± 5ppm with the LT synchronised to the exchange and the NT phase-locked to the LT.

..2.3.1 British Telecom Frame Structure

The BT Ternary Data Frame Structure is shown in Figure 7.7. The frame has a duration of 750μs comprising 81 ternary symbols, and resulting in the abovementioned symbol-rate.

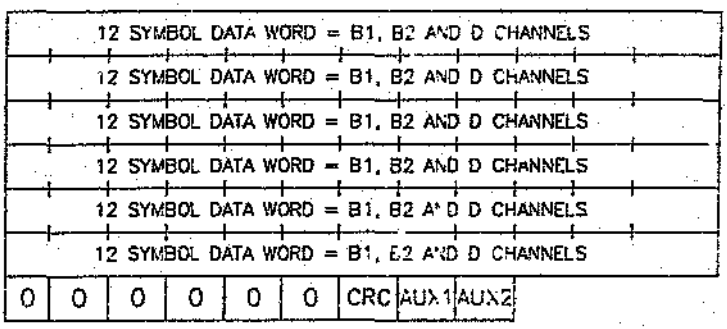


FIGURE 7.7 : BT TERNARY DATA FRAME STRUCTURE

The ternary frame comprises six 12-symbol blocks of 2B+D user-data, followed by the frame-synchronisation marker of six zeros, a CRC symbol and two auxiliary channel symbols.

The six user-data blocks are derived from the encoding of the binary data depicted in Figure 7.8. Each block of 18 bits comprises 8 B1-channel bits, followed by 8 B2-channel bits and ending with 2 D-channel bits. The six binary blocks are then transformed (after scrambling and subsequent SU32 encoding) into six 12-symbol ternary blocks.

$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2
$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2
$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2
$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2
$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2
$B1_1$	$B1_2$	$B1_3$	$B1_4$	$B1_5$	$B1_6$	$B1_7$	$B1_8$	$B2_1$	$B2_2$	$B2_3$	$B2_4$	$B2_5$	$B2_6$	$B2_7$	$B2_8$	D_1	D_2

FIGURE 7.8 : BT BINARY DATA FORMAT

The CRC and AUX symbols facilitate the supervisory and maintenance functions of the BT specification and will be dealt with in section 7.3.3

7.3 Supervisory and Maintenance (S&M) Functions

It seems significant that all three specifications call for a certain degree of supervisory and maintenance functions. It would appear that as the complexities of transmission systems increase, so too does the necessity for ensuring minimal external requirements in respect of the maintenance of such systems.

There exists a clear distinction between the two concepts of supervision and maintenance. The former refers to a facility whereby a system can be monitored in terms of its performance, <u>without</u> the need to interrupt the service. In contrast, maintenance performed on a system necessitates disruption of the service.

In specifying the supervisory and maintenance requirements, each authority has allowed prospective manufacturers the freedom to implement any additional functions, over and above the minimal requirements.

7.3.1 ANSI Supervisory and Maintenance Functions

The ANSI S&M functions are supported via the M1 to M6 overhead bits as depicted in Figure 7.4. A total of 48 bits per superframe are conveyed in either direction, facilitating a S&M channel with a capacity of 4kbit/s.

The M1-M3 bits support the so-called Embedded Operations Channel (EOC). Twenty-four bits per superframe (2kbit/s) are allocated to the EOC, which is largely responsible for maintenance functions. The actual length of an EOC frame is 12 bits, resulting in the transmission of 2 EOC frames per superframe. The composition of an EOC frame is shown in Table 7.1.

BIT	NAME	FUNCTION PROVIDED
1...3	EOC_{a1}...EOC_{a3}	Address field
4	EOC_{dm}	Data/Message indicator
5...12	EOC_{i1}...EOC_{i8}	Information field

TABLE 7.1 : EOC Frame Composition

The 3-bit Address Field is used to address up to 7 locations (0.....6), with address-7 denoting a broadcast address, and address-0 always referring to a NT. For a DSL with no regenerators in the loop, only addresses 0 and 7 have any significance.

The Data/Message Indicator is set to "1" when the Information field contains an operations message, and set to "0" when the latter contains numerical data.

The Information Field supports, in principle, 256 messages, but in reality, only 8 are defined. The messages and their associated EOC codes are listed in Table 7.2.

MESSAGE	MESSAGE CODE	ORIGIN (o) NETWORK	DEST. (d) NT
Operate 2B+D Loopback	0101 0000	o	d
Operate B_1-Channel Loopback	0101 0001	o	d
Operate B_2-Channel Loopback	0101 0010	o	d
Request Corrupted CRC	0101 0011	o	d
Notify of Corrupted CRC	0101 0100	o	d
Return to Normal	1111 1111	o	d
Hold State	0000 0000	d/o	o/d
Unable to Comply Acknowledgement	1010 1010	d	o

TABLE 7.2 : EOC Information Field Messages

The essential elements of the maintenance functions are the three loopback commands facilitating the physical looping back of individual data channels, as well as the complete 2B+D 144kbit/s channel. Note that no provision is made to loop the D-channel back independently of the B-channels, as disruption of the D-channel indirectly affects the operation of one or both B-channels during call establishment.

The Request or Notify of Corrupted CRC messages allow testing of the CRC supervisory function by intentionally forcing a corrupted CRC value to be sent down the line. The effect of this operation should be to indicate a transmission "error" in a correctly functioning system.

The EOC protocol operates in a repetitive command/response mode, ie. three identical properly-addressed consecutive messages must be received before any action is initiated. For a more detailed description of the EOC, the reader is referred to [43].

The Overhead bits, M4-M6, provide essentially two facilities, viz. transceiver activation/deactivation, and supervisory functions.

The "act" bit forms part of the start-up sequence to communicate readiness for layer-2 communication at either end of the DSL.

The "dea" bit is used by the network to communicate to the NT its intention to deactivate. In this way, an NT can deactivate in an orderly fashion (ie. freeze and store its EC and DFE coefficients).

The Power Status bits, PS1 and PS2, facilitate the communication of an NT's power supply status to the LT. PS1 and PS2 indicate the state of primary (eg. mains) and secondary (eg. battery backup) power respectively. In the event of an impending power status change at the users premises, the network would be forwarned.

The "ntm" bit indicates to the network that the NT is in a customer-initiated test mode. The NT is considered to be in a test mode when any one of the data channels is involved in a customer locally-initiated maintenance action.

The "cso" bit indicates the start-up capabilities of the NT transceiver. The ANSI specification makes provision for two types of start-up capability, viz; cold-start and warm-start. A cold-start is initiated on power-up and assumes no prior knowledge of the cable characteristics. A cold-start activation sequence therefore, has a slower conversion time than a so-called warm-start. The latter relies on knowledge of cable characteristics from a previously successful activation sequence, and as a result, allows a much-reduced activation-time.

The Far End Block Error (FEBE) bit in each direction of transmission may be monitored to determine the performance of the far-end receiver. The FEBE bit is generated for a particular superframe in the event of a CRC error being detected.

Figure 7.4 shows a number of bit positions in the superframe Overhead bits being filled with binary ones. These bits are all reserved for future standardisation and must be set to binary one to comply with the current specification.

The last allocation in the Overhead bits comprises the CRC code. Twelve bits per superframe, $CRC_1 \ldots\ldots CRC_{12}$, are allocated to the CRC function. The CRC bits are generated by dividing part of the data contained in the current superframe by the polynomial P(x), where:

$$P(x) = x^{12} \oplus x^{11} \oplus x^3 \oplus x^2 \oplus x \oplus 1$$

The superframe bits included in the CRC generation process are those comprising the D-channel, both B-channels, and the M_4 Overhead bits.

At the receiver, a CRC calculated from the same bits is compared with the CRC value received. If the two values differ, at least one error has occurred in the bits covered by the CRC.

7.3.2 Bundespost Supervisory and Maintenance Functions

The M&S capabilities of the Bundespost specification are comparatively limited, due to a mere 1kbaud M&S channel being provided. The M&S channel is facilitated via the single M-symbol once per frame as shown in symbol-position 85 of Figure 7.5.

The specified supervisory function is simply monitoring of remote code violations. A code violation is detected if the RDS of the received symbols is less than one or greater than four at the end of a ternary block. A block comprising three zeros will also generate a code violation. In the event of one or more code violations being detected in a single frame downstream, the M-symbol is coded as "+1" and sent upstream. The LT will thus be notified each time a corrupted frame is encountered at the NT.

It should be mentioned that, due to the limited error-detecting capabilities of the RDS technique, some errors will go undetected.

In terms of maintenance functions, three commands are specified. The first command, sent downstream, allows a combined loopback of the D- and B-channels to be made. The command is initiated by continuously encoding the M-symbol as "+1" for the duration of the desired loopback. On receiving a minimum of 8 consecutive "+1" M-symbols, the NT performs the loopback.

The second loopback command caters for the possible inclusion of a regenerator in the DSL. By encoding the M-symbol with alternating "+1" and "0" symbols, a loopback at the regenerator is applied after the reception of 8 consecutive frames containing alternating M-symbols.

The third and final maintenance command allows the removal of any loopback that may have been set up. On receiving 8 or more consecutive ternary zeros, an NT will disconnect the loopback and allow the transmission of transparent user-data.

7.3.3 BT Supervisory and Maintenance Functions

The BT specification calls for extensive M&S capabilities, with the emphasis on supervisory functions. The M&S capabilities are exclusively supported by the last 3 symbols depicted in Figure 7.7, viz. the CRC, AUX_1 and AUX_2 symbols. Since each frame has a duration of 750 µs, the M&S channel has a capacity of 4kbaud.

The CRC symbol establishes a 12ms superframe comprising 16 frames of 81 symbols each. The 16 CRC check symbols form a 15-bit CRC word, with a binary "1" encoded as "-1" and a binary zero encoded as "+1".

The sixteenth check symbol is a single ternary "0" which defines the start of the 12ms superframe. The CRC generating polynomial, $G(x)$, is defined as follows:

$$G(x) = x^{15} \oplus x^{8} \oplus x^{4} \oplus x^{3} \oplus x \oplus 1$$

where $\oplus$ denotes modulo 2 addition.

$G(x)$ is selected so as to ensure that a message conveyed by the two AUX symbols (3 bits), will be received erroneously not more than once per hour under the conditions of an error rate of 10^{-3}.

Within each 12ms superframe, the auxiliary channel sends 2 consecutive messages of 24 bits each (ie. 16 frames x 3 bits). Each 24-bit message comprises a:

* 3-bit Subsidiary channel
* 1-bit Ready for Data/Data Valid (R-bit)
* 5-bit Maintenance Channel (M1.....M5)
* 9-bit Supervisory Channel (S1.....S9)
* 6-bit CRC field

The 3-bit subsidiary channel gives the U-interface the capability of supporting an additional 500bit/s transparent data channel. The inclusion of the subsidiary channel is not insisted upon in the BT specification, but is in fact merely suggested as an optional feature.

The R-bit provides handshaking support for higher-level systems at either end of the DSL. It is equivalent to the ANSI "act" bit.

The 5-bit maintenance field carries maintenance commands (ie. loopbacks) from the exchange-end, and maintenance responses (ie. acknowledgements) back from the subscriber-end of the DSL. The maintenance commands are listed in Table 7.3.

MAINTENANCE					LOOPBACKS					
COMMAND WORD					REGENERATOR			NT		
M_1	M_2	M_3	M_4	M_5	B1	B2	D	B1	B2	D
1	1	1	1	1						
1	1	0	1	1	*					
1	0	1	1	1		*				
1	0	0	1	1	*	*				
0	0	1	1	1				*		
0	1	0	1	1					*	
0	1	1	1	1				*	*	

TABLE 7.3 : BT Maintenance Commands

On receiving and acting on one of these commands, the same data pattern is echoed back as the maintenance response. The NT or regenerator will return all ones (ie. null code) when not responding to a command. Note that the bandwidth provided in supporting the maintenance function, allows up to 31 commands excluding the "null" command. The capability therefore exists, to equip the system with a further 25 maintenance commands (eg. D-channel loopbacks). This option is left to the discretion of the individual manufacturer.

It should be pointed out that, unlike the ANSI specification which allows multiple maintenance commands to be acted upon simultaneously, the BT system makes provision for only a single command to be active at any one time.

The supervisory channel is used to monitor the transmission performance at the NT or regenerator. The channel consists of a 9-bit command sent from the exchange-end, and a 9-bit response returned upstream. The channel is specified as a compelled system, with a command sent by the LT until a response is received, whereafter an idle (all ones) command is sent until an idle response is received. Table 7.4 lists the supervisory commands.

REQUEST		COMMAND WORD								
DESTINATION	CLASS	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
-	Idle	1	1	1	1	1	1	1	1	1
LT	AGC Level	0	0	0	0	0	0	1	0	0
LT	Eye Noise	0	0	0	0	0	0	1	0	1
LT	Eye Height	0	0	0	0	0	0	1	1	0
LT	Error Count	0	0	0	0	0	0	1	1	1
UPSTREAM REGEN	AGC Level	0	0	0	0	0	1	0	0	1
UPSTREAM REGEN	Eye Noise	0	0	0	0	0	1	0	0	1
UPSTREAM REGEN	Eye Height	0	0	0	0	0	1	0	1	0
UPSTREAM REGEN	Error Count	0	0	0	0	0	1	0	1	1
DOWNSTREAM REGEN	AGC Level	0	0	0	0	0	1	1	0	1
DOWNSTREAM REGEN	Eye Noise	0	0	0	0	0	1	1	0	1
DOWNSTREAM REGEN	Eye Height	0	0	0	0	0	1	1	1	0
DOWNSTREAM REGEN	Error Count	0	0	0	0	0	1	1	1	1
NT	AGC Level	0	0	0	0	1	0	0	0	0
NT	Eye Noise	0	0	0	0	1	0	0	0	1
NT	Eye Height	0	0	0	0	1	0	0	1	0
NT	Error Count	0	0	0	0	1	0	0	1	1

TABLE 7.4 : BT Supervisory Commands

The power of the supervisory facilities provided by the BT specification will now be highlighted. Table 7.4 can be divided into 4 distinct groups each designated by the destination to which the command is directed. The four destinations are LT, NT, Upstream and Downstream regenerators. The reason for considering both components of what is in reality a single regenerator, is as follows: a regenerator interposed in a DSL comprises two independent transceivers, ie. an upstream transceiver which communicates with the LT, and a downstream transceiver which communicates with the NT. From a supervisory viewpoint therefore, it is desirable to be able to monitor the receivers in both regenerator components, and the BT specification makes provision for this.

The supervisory functions facilitate four measurements at each destination, viz. AGC-level, Eye-noise, Eye-height and Error-count. The response to a valid command for a particular destination is a zero (S1) followed by an 8-bit response byte transmitted with its MSB (S2) first.

The AGC parameter has a value which is set and frozen during the activation procedure. It is useful in practice since it informs the network of the approximate insertion loss (± 5dB) of the DSL. In the event of degraded performance, one can ascertain if the problem is attenuation rel: ted.

The Eye-noise and Eye-height can be lumped together to form the Eye-closure. This latter parameter provides useful insight into the SNR of the transmission system, which in turn gives a dynamic indication as to how close to the margin the system is operating, even in the absence of line errors.

The Error-count is based on the number of 15-bit CRC mismatches between received and locally synthesized CRC values. On every mismatch, the error-count is incremented by one. It is reset on detecting the Error-count command after having responded with the appropriate value.

The 15-bit superframe CRC is not to be confused with the 6-bit CRC field forming part of the Auxiliary channel. The latter CRC aims to protect the remaining 18 bits of data comprising the auxiliary channel message, by preventing corrupted messages from being executed. The auxiliary channel CRC employs a generator polynomial, G(x) of:

$$G(x) = x^6 \oplus x^5 \oplus x^3 \oplus x^2 \oplus x \oplus 1$$

7.4 Electrical Characteristics

Space precludes a detailed coverage of all the required electrical specifications characterising each of the three systems. The salient features of each system will, however, be briefly introduced, with reference to the following topics:

* Maximum attainable line lengths.
* Transmit signal characteristics.
* Jitter requirements.
* Start-up time requirements.

7.4.1 ANSI Electrical Specifications

7.4.1.1 Maximum Attainable Line Lengths

The ANSI specification defines the maximum attainable line length in terms of 16 Test Loops each of which must sustain communication with a BER of less than 10^{-7}. Furthermore, impairments (ie. power-related noise and crosstalk) may be injected onto the line, under the condition that the specified BER should not be exceeded.

Of the 16 Test Loops, one is termed a null loop (ie. zero cable length), while ten contain bridged taps. Since the latter is rarely encountered in the SAPT loop-plant, the bridged tap loops will not be considered. The makeup of the remaining 5 loops is listed in Table 7.5, along with the calculated cable-attenuation at 100kHz using a PIC model at approximately room temperature.

	CABLE MAKE-UP				
LOOP # According to [43]	SECTION 1	SECTION 2	SECTION 3	SECTION 4	INSERTION LOSS (dB)
1	5,03km (0,4mm)	0,46km (0,5mm)			58,9
4	2,29km (0,4mm)	1,37km (0,5mm)	0,61km (0,63mm)	0,91km (0,4mm)	49 0
7	4,11km (0,4mm)				45,3
12	2,29km (0,4mm)	1,37km (0,5mm)	0,46km (0,4mm)		40,7
15	3,36km (0,4mm)				40,3

TABLE 7.5 : Selected ANSI Test Loops

The attenuation figures quoted in Table 7.5 are based on attenuation values of 11,01, 7,6 and 5,43dB/km for cable gauges of 0,4mm, 0,5mm and 0,63mm respectively.

With reference to Table 7.5, it is evident that Test Loop 1 imposes the most stringent requirements in terms of overall attenuation.

The impairments alluded to earlier are introduced into the system-under-test as depicted in Figure 7.9.

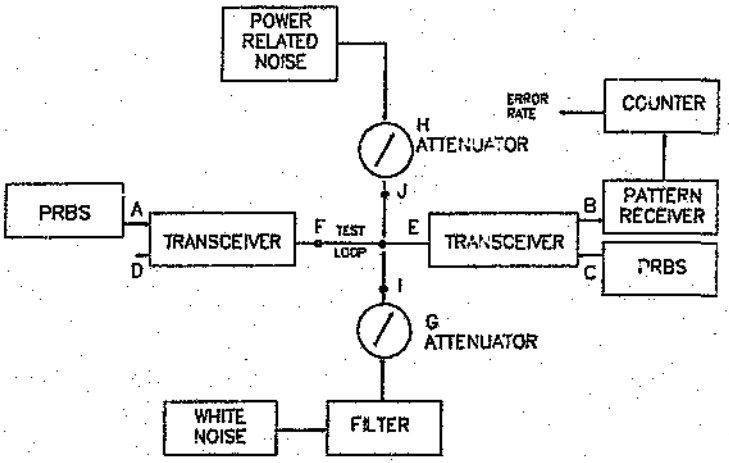


FIGURE 7.9 : LABORATORY TEST SET-UP FOR MEASURING BER

Simulated crosstalk is introduced at point E in Figure 7.9 by applying a filtered Gaussian random white noise source to the receiver input. The filter provides the frequency-shaping necessary to simulate the NEXT from 49 disturbers in a bindergroup. The derivation of the assumed Power Spectral Density (PSD) of the disturbers is covered in reference [43].

The power-related noise depicted in Figure 7.9 refers to noise simulating longitudinal power line induction with its associated harmonics. The waveform specified for power-related noise measurements is sawtooth shaped, since the latter has a harmonic content similar to power-line induction. Figure 7.10 shows the required waveform as specified by ANSI.

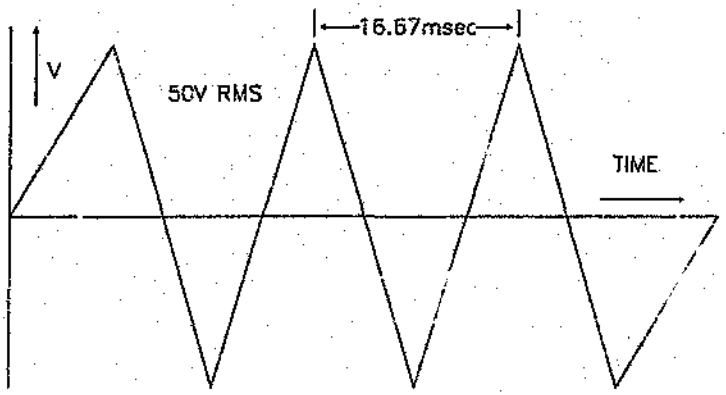


FIGURE 7.10 : ANSI SPECIFIED WAVEFORM FOR LONGITUDINAL NOISE

7.4.1.2 Transmit Signal Characteristics

The nominal peak value of a single "+3" quaternary symbol is 2,5V. The peak values for the other 3 symbols "+1", "-1" and "-3" are +0,83V, -0,83V and -2,5V respectively.

The average power of the transmit signal, comprising a framed sequence of symbols with a synchronisation word and equiprobable symbols at all other positions, is between 13 and 14dBm over a frequency range of 0 to 80kHz. The assumed termination impedance is 135ohms resistive.

The upper bound of the power spectral density of the transmitted signal is as shown in Figure 7.11.

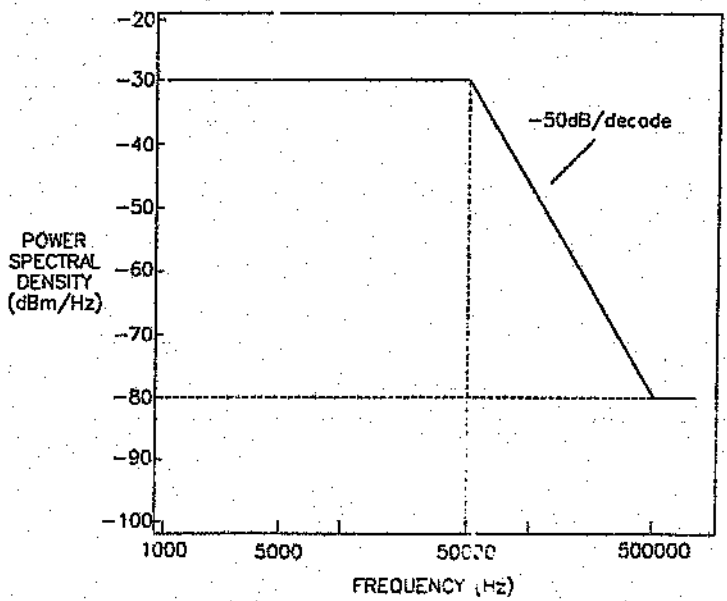


FIGURE 7.11 : UPPER-BOUND OF ANSI TRANSMIT SIGNAL PSD

7.4.1.3 Jitter Requirements

Jitter is specified in terms of Unit Intervals (UI) of the nominal 80kbaud signal, ie. 12,5 µs.

The maximum permissible output jitter at the NT is 0,04UI peak-to-peak and 0,01UIrms when measured with a High Pass Filter (HPF) having a 6dB/octave roll-off below 80Hz.

7.4.1.4 Start-Up Time Requirements

The LT and NT are required to complete the start-up process, including synchronisation and training of equalisers to the point of meeting performance criteria as specified in section 7.4.1.1, within the following lengths of time: Cold-start-only transceivers must synchronise within 15 seconds. Transceivers meeting the optional warm-start activation-tim requirements are to synchronise within 300ms.

7.4.2 Bundespost Electrical Specifications

7.4.2.1 Maximum Attainable Line Length

The Bundespost specifications are far less detailed than those of ANSI in terms of cable-makeup and impairments.

The specifications simply state that the U-interface shall enable transmission over a single cable-pair of 4,2km and 8,0km using cable-gauges of 0,4 and 0,6mm respectively.

The primary cable parameters on which the maximum ranges are based are tabulated in the specification. From the given parameters, the insertion loss (measured at 100kHz) of a single stretch of maximum length cable is 37,8 and 33,9dB for the 0,4 and 0,6mm cables respectively.

The range figures quoted above are based on an assumed noise-figure of $10\mu V/\sqrt{Hz}$ injected onto the line at the receiving-end. Longitudinal mains voltages not exceeding 65Vrms should also not degrade the transmission performance.

7.4.2.2 Transmit Signal Characteristics

The peak voltage of a single symbol transmitted to line is ± 2V when measured across a terminating impedance of 150 ohms resistive.

The upper bound of the transmit signal's spectrum is as shown in Figure 7.12. A measurement bandwidth of 9kHz is assumed.

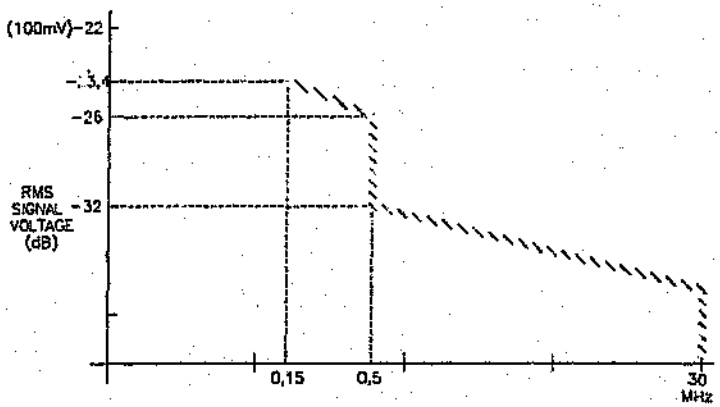


FIGURE 7.12 : UPPER-BOUND OF BUNDESPOST TRANSMIT SPECTRUM

7.4.2.3 Jitter Requirements

The maximum permissible output jitter at the NT is 0,02UI peak-to-peak measured with a first-order high pass filter centred at 30Hz.

7.4.2.4 Start-Up Time Requirements

Reference [44] does not specify a maximum start-up requirement. It is presumed that the determination of this parameter is left to the discretion of each manufacturer.

7.4.3 BT Electrical Specifications

7.4.3.1 Maximum Attainable Line Length

The BT specification calls for 3 cables with makeups and insertion losses as specified in Table 7.6.

	CABLE MAKE-UP			
LOOP # According to [45]	SECTION 1	SECTION 2	SECTION 3	INSERTION LOSS [dB]
1	4,2km (0,4mm)			46,0
2	3,0km (0,4mm)	1,5km (0,5mm)	0,5km (0,63mm)	43,0
3	3,0km (0,4mm)	1,5km (0,5mm)		43,0

TABLE 7.6 : BT Test Loops

Conformance with the maximum line length specification implies error-free (BER < 10^{-7}) transmission based on a similar setup to that of the ANSI specification as shown in Figure 7.9.

The NEXT filter of Figure 7.9 is designed to yield a crosstalk vs attenuation slope of 4,5dB/octave and power-sum crosstalk attenuation of 53dB at 100kHz.

The BT specification does not evaluate performance in the presence of power-related noise as does ANSI. Instead, impulsive noise and sine-wave interference is substituted for the power-related noise impairment as shown in Figure 7.9. The BT requirement is such that the transmission system must operate with a BER not exceeding $1 \in 10^{-7}$ when dipulses of 10mV peak are injected at the received-end at a frequency of 100Hz. A similar performance criterion is to be met with the injection of transverse and longitudinal sine-wave injection at frequencies and levels as shown in Table 7.7. The tests mentioned above are to be performed on loop#1 as shown in Table 7.6.

FREQUENCY [kHz]	TRANSVERSE INTERFERENCE [mV-pk-pk]	LONGITUDINAL INTERFERENCE [Vrms]
16	10	1,0
40	10	1,0
64	10	1,0
100	20	2,0
200	20	2,0
500	20	2,0
1000	20	2,0
1500	20	2,0

TABLE 7.7 : BT-specified Maximum Sine-Wave Injection

7.4.3.2 Transmit Signal Characteristics

The peak amplitude of a single symbol transmitted to line is specified nominally as 2,5V.

The maximum mean transmit power to line averaged in any 1 second period must not exceed 11dBm assuming a load impedance of 140 ohms resistive.

The output power-spectrum requirement is governed by the following conditions; the maximum mean transmit power averaged in any 1 second period in any 3kHz band below 108kHz, must not exceed 0dBm. At a frequency f, located above 108kHz, the power must not exceed -12-60log (f/108kHz) or -60dBm, whichever is the higher, up to a maximum frequency of 10MHz. The upper-bound of the output power-spectrum is shown in Figure 7.13.

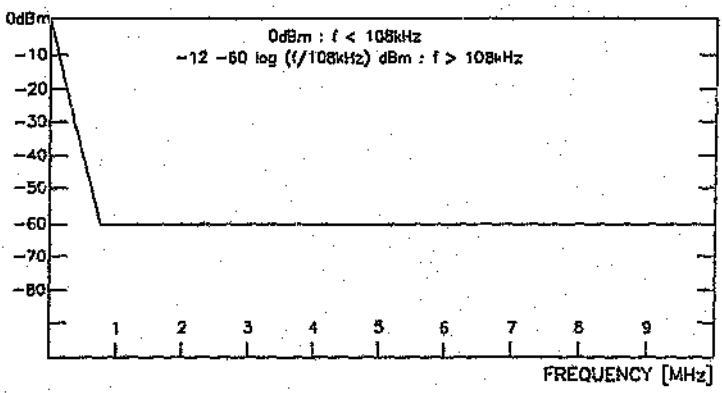


FIGURE 7.13 : UPPER-BOUND OF BT POWER SPECTRUM

7.4.3.3 Jitter Requirements

The jitter requirements are specified relative to the S-interface, ie. 192kHz. The jitter performance of the U-interface receiver should be such that the data transmitted from the S-interface contain a peak-to-peak jitter component not exceeding 5%, when measured through a first-order HPF with its -3dB point at 50Hz.

7.4.3.4 Start-Up Time Requirements

The time taken for the U-interface to achieve both bit- and frame-synchronisation at both ends of the transmission system, must be less than 200ms. This requirement is quite stringent compared with the ANSI startup-time, especially considering that no provision is made for a "warm-start", ie. the system is expected to synchronise within 200ms of a power-up condition.

8 U-INTERFACE CHIP-SETS

8.1 Introduction

Five chip-sets, as shown in Table 8.1, were initially evaluated in terms of meeting each of their respective specifications. However, only three were found to offer satisfactory performance in terms of range, and were thus selected for further evaluation. The chip-sets chosen for further evaluation are listed under the first three entries in Table 8.1.

CHIP-SETS #	MANUFACTURE	CHIP-SET	SPECIFICATION
1	INTEL/AT&T	89120	ANSI
2	SIEMENS	PEB2090	BUNDESPOST
3	STC (UK)	DSP144	BT
4	SIEMENS	PEB2091	ANSI
5	SEL/ALCATEL	UIC	BUNDESPOST

TABLE 8.1 : U-Interface Chip-Sets

The aim of this chapter is to introduce the reader very briefly to each of the three selected chip-sets without delving too deeply into specific implementation details. For a thorough coverage of each chip-set, especially for the purposes of incorporation into transmission equipment, the reader is referred to [46], [47] and [48].

8.2 Intel 89120

The 89120 comprises two 44-pin CMOS devices, viz. The 89122 Analog Front End and the 89123 Digital Loop Signal Processor. The 89122 performs the line interfacing and data conversion functions, while the 89123 performs the algorithm-specific signal processing, control, and access functions.

The 89120 block diagram is shown in Figure 8.1, with a clear partition between system functions being highlighted in the individual chips.

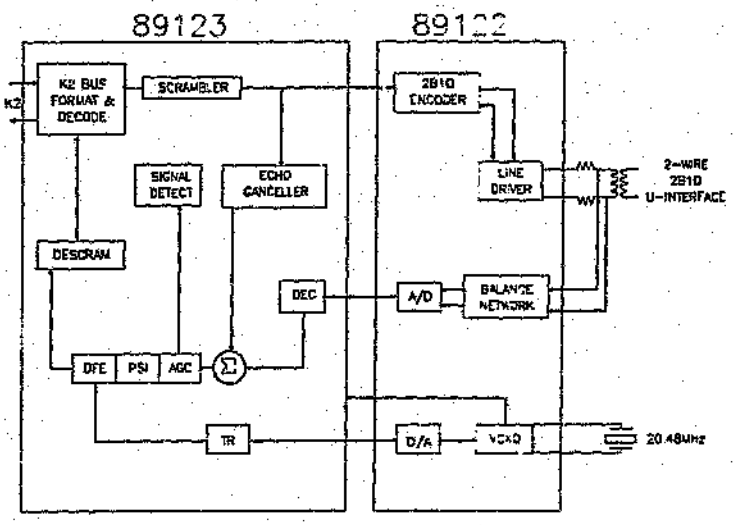


FIGURE 8.1 : 89120 CHIP-SET BLOCK DIAGRAM

The 89122 analog front-end provides the 2B1Q line coder (D/A conversion), pulse shaper, line driver, first order line balance network, VCXO clock generation and sigma-delta A/D conversion. The line driver provides pulses which allow the 2,5V template (1992 requirement) of the ANSI specification to be met when connected to the proper transformer and interface circuitry. The A/D converter is implemented using a double loop sigma-delta modulator.

A Voltage Controlled Crystal Oscillator (VCXO) provides the 20,48MHz master clock for the chip set. The on-chip phase lock loop provides the ability to synchronize the chip clock to the system clock in the LT or the line clock in the NT. Data from the 89123 to the 89122 is converted to an analog control voltage for the VCXO. Provisions are made for either an on-chip or off-chip VCXO.

The 89123 takes input at the K2 interface (described below), and formats this information for the U-interface through a scrambling algorithm, and the addition of synchronisation bits for U-interface framing. This data is then transferred to the 2B1Q encoder on the 89122 for transmission over the line. Signals coming from the line are first passed through the sigma-delta A/D converter on the 89122, and then sent to the 89123 for more extensive signal processing. The 89123 provides decimation of the sigma-delta output (DEC), linear and non-linear echo cancellation, Automatic Gain Congrol (AGC), signal detection, Phase Shift Interpolation (PSI), Decision Feedback Equalisation (DFE), Timing Recover (TR),

descrambling, line code polarity detection, and rate adaption for output onto the K2 interface. The DFE circuit provides the functionality necessary for proper operation on subscriber loops with bridged taps.

The device provides rapid cold-start and warm-start operation. From a cold start, the device will typically be operational within 3 seconds. The device supports activation/deactivation and, when properly deactivated, will store the EC coefficients such that, upon the next activation request, a faster warm-start is possible. A warm-start will typically require 200msec for the device to become operational.

The K2 interface comprises 5 lines; Data Out (DO), Data In (DI), data Clock (C), K2 Frame sync (F), and Master Timing Clock (MTC). C is a 512kHz output signal for clocking data into and out of the device at one bit per clock cycle. F is an 8kHz signal indicating the start of a K2 frame. MTC accepts an 8kHz system-clock as input, facilitating exchange-end synchronisation.

8.3 Siemens PEB2090

The PEB2090 chip-set comprises two chips, the PEB20901 and PEB20902. The former is responsible for the digital functionality, eg. encoding/decoding, echo cancellation, decision feedback equalisation and digital filtering, while the latter manages the various analogue functions, ie. A/D and D/A conversion, line buffering and clock-generation. A functional block diagram of the PEB2090 is shown in Figure 8.2.

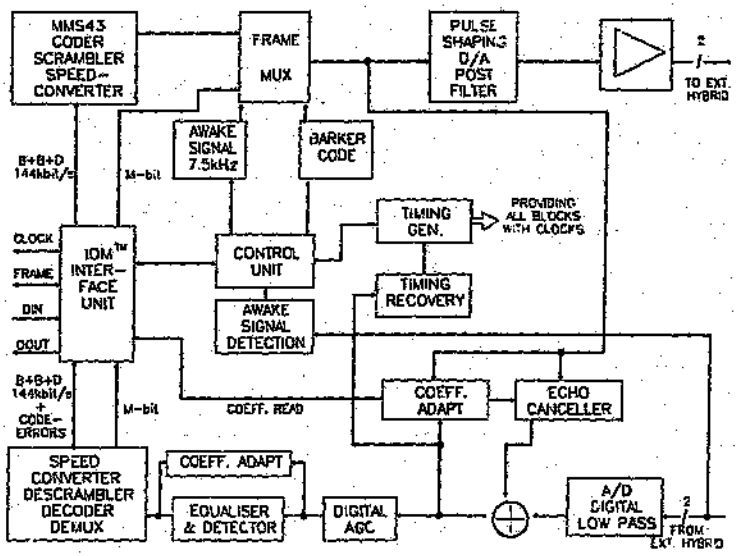


FIGURE 8.2 : PEB2090 CHIP-SET BLOCK DIAGRAM

The PEB2090 "transceiver" functions are essentially quite similar to those of the other two chip-sets being considered. Besides the obvious differences in architecture as defined by its governing specification, the PEB2090 differs notably from two aspects. Firstly, the user-interface is defined by the ISDN Oriented Modular (IOM) interface, a product of the "Group-of-Four European Telecommunications Equipment Companies", viz. Alcatel, Italtel, Plessey and Siemens [49]. Secondly, the PEB2090 allows the option of reading the EC coefficients during normal operation. This function provides a form of line fault-location, in that pre- and post-fault coefficient-vectors can serve as inputs to a fault-location algorithm in the event of a transmission malfunction.

8.4 STC DSP144

The DSP144 chip-set comprises the DSP144 and ALT144 chips. The former performs the DSP functions of filtering, echo cancellation and decision feedback equalisation, as well as data formatting, while the latter contains the A/D, D/A and line-driver circuitry. A simplified block diagram of the DSP144 system is shown in Figure 8.3.

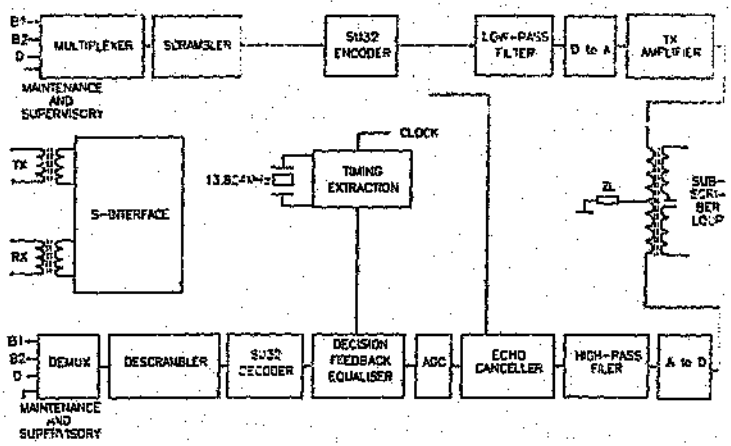


FIGURE 8.3 : DSP144 CHIP-SET BLOCK DIAGRAM

A great deal of similarity exists between the DSP144 and the previous two chip-sets, especially in terms of the basic transmission system. The DSP144 does however, differ in respect of its user-interfaces, viz; "V", "P" and "S". The V-interface is a burst-mode multiplexed interface operating at a data-rate of 2048kbit/s. It is generally used at the exchange-end of a DSL. The P-interface bears a fairly close resemblance to the K2 and IOM interfaces. It comprises four signal lines which in turn support a clock, start-of-frame, data-in and data-out signals. The S-interface requires no explanation as it conforms exactly to CCITT's I.430 specification.

For the application around which this research report centres, the V- and S-interfaces are not used, and data enters and exits the system via the P-interface.

9 EVALUATION SYSTEM

9.1 Introduction

The aim of the evaluation system is to provide the necessary platform on which the transmission performance of each of the 3 U-interface chip-sets may be assessed. Due to time constraints, it was decided to design a single system which would cater for all 3 chip-sets, with a minimum of hardware redundancy. With this philosophy in mind, the evaluation system comprises the following four sub-systems: A single "motherboard" and three "daughterboards". The motherboard performs two primary functions, viz; controlling and monitoring the activation procedure, and formatting the B-channel data for use between the chip-set and user-interface. Each daughterboard supports one of the U-interface chip-sets along with the associated analogue hybrid and clock-generation circuitry. Since attainment of maximum range is critically dependent on the PCB layout surrounding each chip-set, the daughterboard approach facilitates optimum layout due to its physical isolation from the "noisy" microprocessor circuitry on the motherboard.

In describing the evaluation hardware, an attempt has been made to steer clear of specific design details, as this only serves to confuse the issue of the transmission system. In the event of access to schematics and design-specific software being required, the latter is obtainable from STC [50].

9.2 Evaluation System Motherboard

A block diagram of the evaluation system motherboard is shown in Figure 9.1.

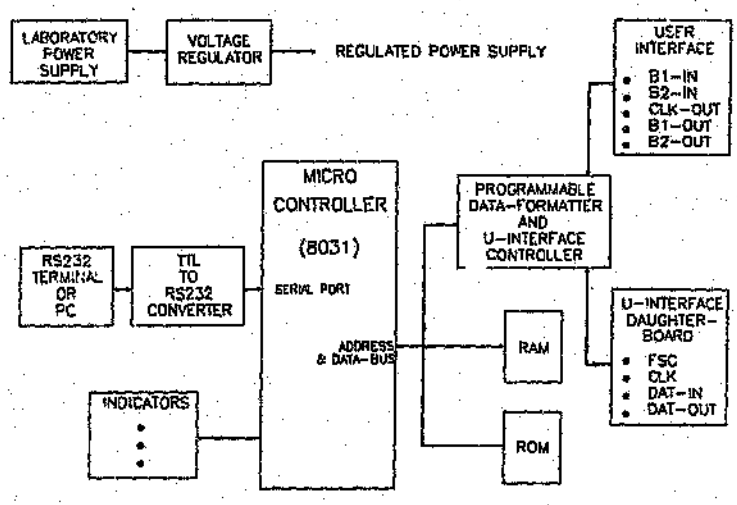


FIGURE 9.1 : BLOCK DIAGRAM OF EVALUATION SYSTEM MOTHERBOARD

The motherboard comprises essentially 9 modules, each of which will now be briefly discussed.

9.2.1 Microcontroller

The microcontroller constitutes the "intelligence on the motherboard. On receiving an activation command, it proceeds to initiate the activation sequence as required by a particular U-interface chip-set. This process also entails the monitoring of status information received from the U-interface so as to complete the sequence and achieve successful activation.

A second function of the microcontroller is that of extracting supervisory information provided by the chip-sets. Examples of supervisory information include the following; CRC or line-code violations, eye-closure, receiver noise and AGC values. Once extracted, the data is processed and sent out via the serial-port for display or recording.

9.2.2 ROM

The ROM performs a similar function to that of "program-memory" in any microcontroller based system, viz; it stores an encoded version of the software which drives the microcontroller. It is also used as a storage medium for any look-up conversion-tables, eg. AGC-to-Insertion loss table.

9.2.3 RAM

External RAM is often omitted from microcontroller-based systems, as internal RAM is usually included in the microcontroller chip. External RAM is however, deemed necessary in this design, so as to facilitate temporary storage of relatively large data arrays, eg. EC coefficients in the case of the Siemens U-interface chip-set. The external RAM also supports its traditional role of additional variable storage.

9.2.4 Programmable Data-Formatter/U-Interface Controller

This module serves two vital purposes. Firstly, it acts as the interface between the user bit-stream/s and the U-interface chip-set interface, the latter being based on one of three possible interfaces, viz; K2, IOM, or P. Secondly, it converts commands received from the microcontroller into a form suitable for the particular U-interface chip-set in use, and conversely, presents replies and acknowledgements available at the U-interface to the microcontroller on request.

Besides the features discussed above, the "programmable data-formatter and U-interface controller" is also equipped to perform local loopbacks as well as B1- and B2-channel combination if programmed to do so. The former function enables the complete transmission path to be tested, as data injected at one end of the transmission system is output at the same end, facilitating ease of error-monitoring. The B-channel combination facility allows the injection and subsequent monitoring of test-data at twice the single-channel rate of 64kbit/s, ie. 128kbit/s. By allowing both B-channels to be tested simultaneously, a specified BER measurement can be made in half the time required of a single channel measurement.

9.2.5 User-Interface

The user-interface provides a data test-set with a point of entry and exit for its digital testdata. The electrical specifications at this interface are NRZ-coded at TTL voltage levels.

The data bit-rate at the user-interface is selectable between 64kbit/s and 128kbit/s. In the case of the lower bit-rate being selected, both the B1- and B2-channel I/O ports are active at 64kbit/s, while the "CLK-OUT" port supplies a 64kHz data-clock. With the higher bit-rate selected, only the B1-channel I/O is active at 128kbit/s, while "CLK-OUT" supplies a clock of 128kHz.

9.2.6 U-Interface Daughterboard Interface

This interface provides the link between the motherboard and any one of the three "plug-in" daughterboards alluded to earlier. Fortunately, the interfaces supplied by the manufacturers of the 3 U-interface chip-sets are similar enough to allow a single hardware-level interface to suffice for all 3 systems.

The daughterboard interface comprises 4 signal lines and a power input as shown in Figure 9.1. "FSC" and "CLK" supply a "start-of-frame" and clock signal respectively to the motherboard, while "DAT-IN" is a serial input to the motherboard, conveying both data and status information in a multiplexed format. "DAT-OUT" serves as an input to the chip-set, being identical in format to the "DAT-IN" signal.

9.2.7 Indicators

This module comprises three Light-Emitting Diodes (LEDs) and associated drivers. The LEDs simply provide a visual indication of the current status of the U-interface (eg. pending activation, activated), as well as transmission error monitoring.

9.2.8 TTL-to-RS232 Converter

A means of communicating data between the evaluation system and the outside world is necessary. Since the peripheral at the end of the communications link would typically be a terminal or PC with built in "serial" card, an RS232 (V.24) specification is needed. The TTL-TO-RS232 converter module is provided to facilitate the requisite voltage level conversion.

Typical uses for the RS232 communication link include:

* Initiation of activation sequence.
* Read-out of activation sequence duration.
* Error-rate monitoring.
* Eye-closure monitoring.
* Readout of EC coefficients.

9.2.9 Power Supply Unit (PSU)

The PSU is included here merely for completeness, since its operation should be self-evident. It must be pointed out, however, that the maximum attainable transmission

range is quite dependent on the provision of a "clean" power supply, typically comprising noise not exceeding 5mV RMS. For this reason, the motherboard and each of the 3 daughterboards, have been equipped with on-board voltage-regulators.

9.3 Evaluation System Daughterboards

The schematic for each of the three daughterboards will not be shown here; however, the interested reader is referred to the relevant data sheets [46]-[48], or the STC schematics [50].

What can be shown here, however, is a block diagram (Figure 9.2) of a typical daughterboard, bearing in mind that each of the chip-sets has slightly different requirements in respect of the analogue hybrid and master-clock circuitry.

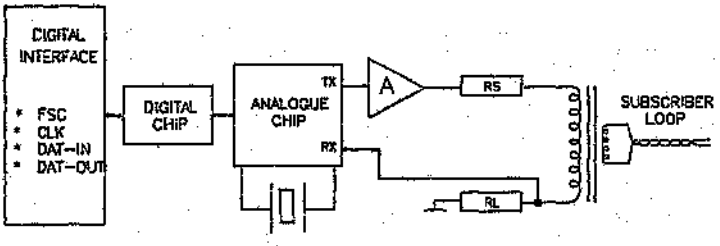


FIGURE 9.2 : BLOCK DIAGRAM OF U-INTERFACE DAUGHTERBOARD

Referring to Figure 9.2, it is seen that the daughterboard is coupled to the motherboard via a 4-wire interface as described previously.

In all three U-interface systems, implementation complexities have todate prevented merging both digital and analogue components onto a single substrate. This limitation, coupled with the typically high value of receiver input impedance, imposes fairly severe constraints on the circuit board layout in order to prevent stray sources of interference from being coupled into the system.

The master-clock is shown diagrammatically as a crystal. In reality, while a crystal suffices at the subscriber-end of a DSL, a more complex external PLL is needed at the exchange-end to achieve synchronisation of the system with the network.

The hybrid is shown in a much-simplified form. Essentially, however, the principle of operation is such that the return-loss achieved by the hybrid is a function of the match between the line-impedance and the source and load impedances presented at the circuit-side of the transformer. The design of the EC is generally such that even a 0dB return-loss will ensure the specified transmission range.

10 CHIPSET PERFORMANCE

10.1 Introduction

The purpose of this chapter is to present a coherent and succinct overview of the tests performed on each of the three chipsets described in Chapter 8. The number of possible tests applicable to a transmission system is limitless. However, emphasis has been placed on those tests which highlight a specific performance criterion, viz; BER vs transmission range. Other criteria, such as power consumption or maintenance and supervisory channel performance have not been considered.

Six independent tests form the basis for the chipset evaluations. These comprise "noise-free" range-tests, range-tests in the presence of noise, transmit power tests, power spectrum tests, receive-clock jitter, and activation-time tests. The activation-time tests do not strictly-speaking affect transmission performance, but they do play a role in the overall performance of an ISDN, as lengthy call setup times are unattractive from a subscriber's point of view.

Stremer [51] defines noise as "any unwanted signals, random or deterministic, which interfere with the faithful reproduction of a desired signal in a system". To this end, therefore, three types of interfering signal have been used in assessing transmission range performance in the presence of noise, viz; bandlimited gaussian noise, single sinusoidal tones at various frequencies, and impulsive noise.

Each test and associated results will now be discussed.

10.2 "Noise-Free" Range Tests

The quotation marks contained in the tittle are included, since it is not quite accurate to speak of a completely "noise-free" environment. Extraneous sources of noise are always present, ie. mains-induced interference, unfiltered power-supply components, crosstalk from adjacent turns on the laboratory cable-drum, and thermal noise generated by the cable itself. The term "noise-free" is therefore intended to imply that no additional sources of noise are intentionally introduced. At the same time, an attempt has been made to minimise all controllable interferences, eg. by designing well regulated and filtered power supplies.

Before describing the tests, a brief description of the cable test-bed at STC is necessary. The latter comprises eight mounted cable-drums, each of which holds a single length of 80-pair cables. These cables are in turn terminated on connectors, facilitating ease of interconnection. The characteristics of a typical cable-pair from each of the drums are listed in Table 10.1.

DRUM NO.	GAUGE (mm)	NOMINAL LENGTH (m)	ACTUAL LENGTH (m)	MEASURED ATTENUATION (dB/km)	THEORETICAL ATTENUATION (13)
1	0,4	1000	929	10,7	11,01
2	0,4	200	193	10,7	11,01
3	0,5	1000	1004	7,6	7,7
4	0,5	200	217	7,6	7,7
5	0,63	1000	1006	4,4	5,4
6	0,63	200	219	4,4	5,4
7	0,9	1000	1002	2,7	3,6
8	0,9	200	223	2,7	3,6

TABLE 10.1 : STC Cable Test-Bed Characteristics

Note the discrepancies between the measured values of attenuation and those calculated from the tables of primary parameters contained in [13]. Interestingly, these same parameters form the basis upon which the test loops in ANSI TI.601 [43] are specified. Since the cables at STC (and evidently those comprising the SAPT network) are not identical to those upon which the ANSI test-loop are based, it is futile to base the transmission range tests on cable length. Instead, in building up a particular ANSI test-loop, sections of a loop are individually measured so as to be in close accordance with the theoretical value of attenuation. The reference frequency at which all attenuation measurements and calculations are specified is 100kHz.

All specifications of maximum transmission range must be accompanied by a corresponding indication of allowable BERs. The three U-interface specifications considered in this report all require a BER not exceeding $1x10^{-7}$. To adequately test for such a BER, one needs to monitor 10^8 bits and verify that fewer than ten bits are erroneously received. To speed-up the measurement procedure, the B1 and B2 channels are multiplexed onto a single channel, thereby yielding a transmission bit-rate of 128kbit/s. The measurement period is therefore $10^8 \div 128 \times 10^3$ seconds, ie. 13 minutes.

10.2.1 Test Procedure

The test procedure is shown diagrammatically in Figure 10.1. For each test, a section of cable is inserted between points X and Y, whereafter the system is activated from the LT transceiver. A pseudo-random binary sequence of length 2^{15}-1 is then injected at 128kbit/s into the LT, while the received bit-stream is monitored for errors. Should more than 10 bit-errors be received in a single 13 minute period, the cable is shortened slightly, and the test repeated.

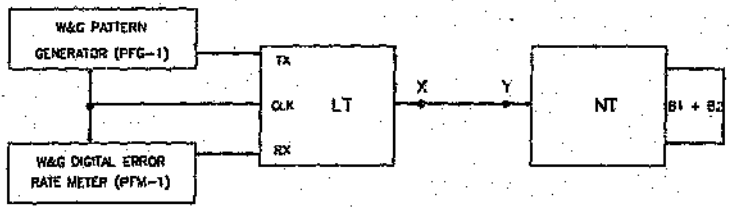


FIGURE 10.1 : NOISE-FREE TEST SET-UP

10.2.2 Test Results

Nine test loops are selected to evaluate each system's noise-free transmission range performance. The first four loops are composed exclusively from one of the available wire gauges, with the tests being performed using the maximum length of a particular gauge while still maintaining a BER not exceeding 10^{-7}. These results are summarised in Table 10.2. The last five loops are tested in a go/no-go fashion, ie. for each test, a note is made of whether a particular test-loop allows transmission with a BER not exceeding 10^{-7}. These results are summarised in Table 10.3. Note that the loops are numbered in accordance with the ANSI T1.601 [43] specification. Note also that only loops excluding bridged taps are included, since the latter are not prevalent in the SAPT networks.

	MAXIMUM TRANSMISSION RANGE FOR BER $<10^{-7}$ (km)			MAXIMUM CABLE ATTENUATION @ 300kHz FOR BER $<10^{-7}$ (dB)		
WIRE GAUGE (mm)	2B1Q	MMS43	SU32	2B1Q	MMS43	SU32
0,4	5,58	4,65	5,42	58,57	50,28	58,06
0,5	7,6	6,6	7,4	57,64	50,84	56,14
0,63	13,4	11,6	12,6	58,31	50,44	54,38
0,9	21,4	20,4	22,0	60,98	57,60	63,04

TABLE 10.2 : Noise-Free Test Results (Single-Gauge)

	BER < 10^{-7} (* INDICATES SUCCESS)		
ANSI T1.601 LOOP NO.	2B1Q	MMS43	SU32
1	*	X	*
4	*	*	*
7	*	*	*
12	*	*	*
15	*	*	*

TABLE 10.3 : Noise-Free Test Results (ANSI Loops)

Table 10.4 lists the composition of the five loops used in the noise-free tests. Each loop is composed of a number of sections, up to a maximum of four. Each section is characterised by a particular gauge and length, and corresponding attenuation. The loops are listed in terms of their ANSI requirements as well as the actual values of attenuation as measured on the STC cable test-bed. In all cases, actual attenuation of each loop section exceeded that specified by ANSI T1.601.

		TEST LOOP SECTION COMPOSITION													
		SECTION 1			SECTION 2			SECTION 3			SECTION 4			TOTAL	
ANSI T1.601 LOOP NO.		Gauge (mm)	Length (m)	Atten. (dB)	Gauge (mm)	Length (m)	Atten. (dB)	Gauge (mm)	Length (m)	Atten. (dB)	Gauge (mm)	Length (m)	Atten. (dB)	Length (m)	Atten. (dB)
1	Theoretical	0,4	5030	55,38	0,5	460	3,50	-	-	-	-	-	-	5490	58,88
1	Measured	0,4	5229	56,66	0,5	400	3,51	-	-	-	-	-	-	5629	59,95
4	Theoretical	0,4	2290	25,21	0,5	1370	10,41	0,63	610	3,31	0,4	910	10,02	5180	48,95
4	Measured	0,4	2440	26,10	0,5	1400	10,65	0,63	800	3,69	0,4	930	10,06	5393	51,06
7	Theoretical	0,4	4110	45,25	-	-	-	-	-	-	-	-	-	4110	45,25
7	Measured	0,4	4299	46,16	-	-	-	-	-	-	-	-	-	4299	46,16
12	Theoretical	0,4	2290	25,21	0,5	1370	10,41	0,4	460	5,06	-	-	-	4120	40,68
12	Measured	0,4	2440	26,28	0,5	1400	10,73	0,4	579	5,92	-	-	-	4418	43,44
15	Theoretical	0,4	3660	40,27	-	-	-	-	-	-	-	-	-	3660	40,27
15	Measured	0,4	3720	40,35	-	-	-	-	-	-	-	-	-	3720	40,35

TABLE 10.4 : Composition of ANSI T1.601 Loops

10.2.3 Analysis of Results

The noise-free range tests give a fairly clear indication of the relative performance of each system. With reference to Table 10.2, it is evident that MMS43 is the poorest performing system on all four cable gauges. 2B1Q performs the best on all the cable gauges except, surprisingly, on the 0,9mm cable, where the SU32 system offers a 2dB improvement. The SU32 system is only marginally inferior to the 2B1Q system on the two thinnest gauges.

With reference to Table 10.3, it can be seen that all five test loops are within the capabilities of the 2B1Q and SU32 systems, while all with the exception of Loop 1 are acceptable to the MMS43 system.

In the latter case a test loop based on Loop 1, but providing a reduced attenuation, was created. The shortened loop was composed of 4300m of 0,4mm gauge and 400m of 0,5mm gauge, yielding a total attenuation of 49,72dB.

In comparing Tables 10.2 and 10.4, one can arrive at a significant conclusion about all three systems. The mixing of cable gauges with its associated mismatching and corresponding reflections, appears to have little effect on the maximum transmission range. Evidently, attenuation alone seems to be the limiting factor, irrespective of the cable composition. The most likely explanation for this phenomenon is the inclusion of both an EC and DFE in each system. The former is responsible for minimising the effects of reflections due to mismatch, while the latter caters for group delay variations in cables comprising a mix of gauges.

10.3 Range Tests in a Noisy Environment

As previously stated, three noise impairments are considered in this range of tests, viz; band-limited white-noise, transversal sinusoidal-waveform single tones, and impulsive noise. The results of each test are presented in the next section.

A means of injecting the abovementioned sources of noise onto the cable-pair had to be designed. A circuit facilitating this requirement, ie. a noise-injection circuit, is depicted schematically in Figure 10.2.

The noise-injection circuit is characterised by two features. Firstly, it provides a high-impedance balanced coupling to the line. The impedance of the circuit facing the line is designed so as to have a minimal loading effect on the cable-pair. Secondly, the noise-injection circuit provides a matched impedance of 50 ohms to the noise source, thereby ensuring maximum power transfer.

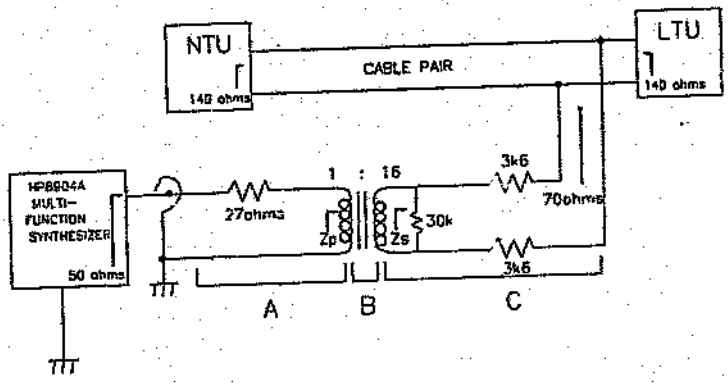


FIGURE 10.2 : NOISE-INJECTION CIRCUIT

The total insertion loss, V_L, introduced by the noise-injection circuit, can be calculated by summing the contributions due to sections A, B and C of the circuit. The necessary calculations are shown below, through equations (1) to (5).

$$Z_s = 7270//30k \approx 5852\Omega \quad (1)$$

$$Z_p = Z_s/16^2 = 22,9\Omega \quad (2)$$

$$V_{LA} = -20\log\left[\frac{22,9}{49,9}\right] = 6,8dB \quad (3)$$

$$V_{LB} = -20\log 16 = -24,1dB \text{ (assuming an ideal transformer)} \quad (4)$$

$$V_{LC} = -20\log\left[\frac{70}{7270}\right] = 40,3dB \quad (5)$$

The total loss of the noise-injection circuit is the sum of V_{LA}, V_{LB} and V_{LC}, ie. 23dB. Due to component tolerances and a non-deal transformer, the measured insertion-loss differs slightly over an extended frequency range. The amplitude response of the noise-injection circuit is shown in Figure 10.3.

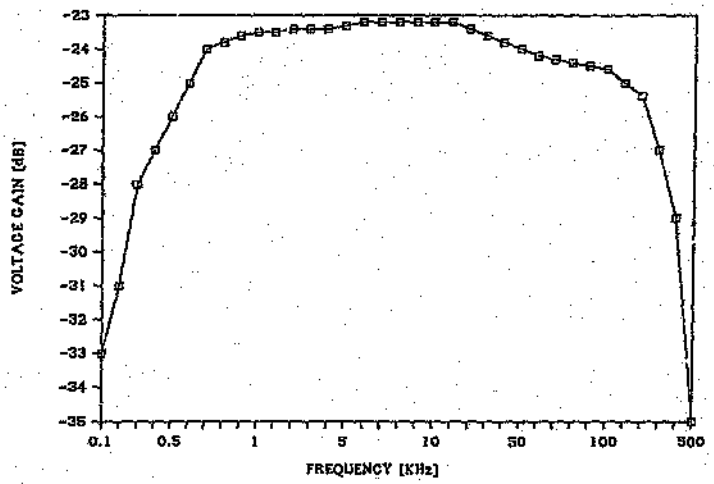


FIGURE 10.3 : NOISE-INJECTION CIRCUIT AMPLITUDE-RESPONSE

The test-procedure for the noise-tests is based on the block-diagram of Figure 10.1. Noise is coupled into the cable at point X via the noise-injection circuit. The noise amplitude is then incrementally increased until a BER of between 10^{-6} and 10^{-7}, is achieved. In practice, the noise amplitude is increased until no more than 38 bit-errors are observed in a 5 minute measuring period.

10.3.1 White-Noise Range Tests

The white-noise generator forms part of the HP8904A Multi-Function Synthesizer. The noise bandwidth (-3dB) is specified as 600kHz with a crest-factor of 4,4. Due to the rather limited frequency-response of the noise-injection circuit however, the equivalent noise-bandwidth is considerably lower than that obtained directly from the noise generator (approximately 200kHz).

The tests are repeated using various cable lengths of 0,4mm gauge. The results are listed in Table 10.5. Note that the maximum noise power available from the HP8904A, is not sufficient to cause any errors at cable lengths below 1800m.

		2B1Q			MMS43			SU32		
Length (m)	Cable Atten. (dB)	Power into 70Ω (nW)	Bit-Errors in 5 min	BER ($X10^{-7}$)	Power into 70Ω (nW)	Bit-errors in 5 min	BER ($X10^{-7}$)	Power into 70Ω (nW)	Bit-errors in 5 min	BER ($X10^{-7}$)
1860	20,31	> 6360	3	0,8	> 6360	0	0	5829	8	2,1
2790	30,54	1697	18	4,7	1837	28	7,3	1160	21	5,5
3720	40,25	359	9	2,3	344	17	4,4	225	20	5,2
4650	50,46	76	8	2,1	40	14	3,6	39	32	8,3
5580	58,79	13	4	1,0	-	-	-	0,2	35	9,1

TABLE 10.5 : White-Noise Results

10.3.2 Sine-Wave Tests

The aim of these tests is to ascertain each of the system's robustness in the presence of a single sinusoidal tone at a number of "spot" frequencies. The voltage injected onto the line is increased until a BER between 10^{-6} and 10^{-7} is achieved. The tests are carried out using a 0,4mm cable of length 4650m, with attenuation of 50,14dB, measured at 100kHz. The results are listed in Table 10.6.

	2B1Q			MMS43			SU32		
Frequency (kHz)	RMS Injected Voltage (mV)	Bit-errors in 5 min	BER ($X10^{-7}$)	RMS Injected voltage (mV)	Bit-errors in 5 min	BER ($X10^{-7}$)	RMS Injected Voltage (mV)	Bit-errors in 5 min	BER ($X10^{-7}$)
8	5,1	18	4,7	2,2	12	3,1	3,0	8	2,1
16	3,3	11	2,9	2,0	8	2,1	2,5	14	3,6
40	2,9	6	1,6	1,6	9	2,3	2,1	15	3,9
64	36,1	7	1,8	2,0	4	1,0	3,8	6	1,6
80	> 116,1	0	0	4,7	16	4,2	11,4	4	1,0
100	>90,9	0	0	24,5	10	2,6	>90,9	0	0

TABLE 10.6 : Sinusoidal-Tone Injection

Note that a ">" signifies that insufficient amplitude is available at the signal-generator output to cause errors. The voltages indicated are those measured at the output of the noise-injection circuit terminated in 70 ohms.

10.3.3 Impulse-Noise Tests

Impulse-noise is prevalent in networks in which electromagnetic switching is used. Since the use of electromagnetic switching is still fairly widespread in the SAPT network, it is essential that any prospective U-interface undergo impulse-noise testing.

The waveform used to simulate impulse-noise is the dipulse-train shown in Figure 10.4. The repetition-rate is 100Hz, while the dipulse-width is chosen as 100µS.

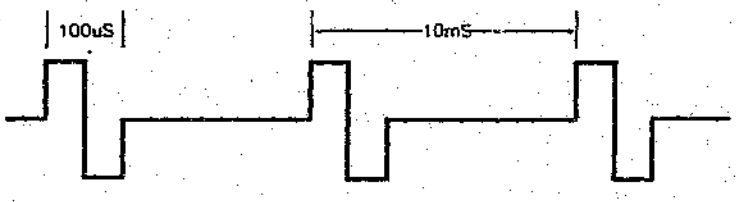


FIGURE 10.4 : DIPULSE-TRAIN SIMULATING IMPULSE-NOISE

The test procedure for impulse-noise testing is similar to the procedure used for sinusoidal-tone injection. The dipulse-train shown in Figure 10.4 is coupled into the cable via the noise injection circuit. The peak-to-peak amplitude of the waveform is steadily increased, until the number of bit-errors observed in a 5 minute period lies between 4 and 38 (ie. $10^{-7} < BER < 10^{-6}$). The cable used in this test is 0,4mm in diameter, 4650m in length, and has an attenuation of 50,14dB when measured at 100kHz.

The impulse-noise test results are summarised in Table 10.7.

SYSTEM	pk-pk INJECTED VOLTAGE (mV)	BIT-ERRORS IN 5 MIN	BER ($X10^{-7}$)
2B1Q	22,8	5	1,3
MMS43	19,0	29	7,6
SU32	16,2	15	3,9

TABLE 10.7 : Impulse-Noise Results

10.3.4 Analysis of Results

The white-noise tests yield interesting but somewhat surprising results. Since the SU32 system attains a substantially longer noise-free range than that of the MMS43 system, one would expect the SU32 system to exhibit superior noise-performance relative to the MMS43 system. The opposite is in fact true as evidenced by Table 10.5; 2B1Q performs the best, followed by MMS43 and SU32.

In terms of sinusoidal-tone injection, Table 10.6 indicates clearly that the order of performance at any disturbing frequency is 2B1Q , SU32 and MMS43. It is also interesting to note that the 2B1Q system is most sensitive to disturbing frequencies in the range of 16 to 40kHz, the SU32 system is to frequencies between 16 and 54kHz, while the MMS43 system is most sensitive to disturbing frequencies in the range of 16 to 64kHz.

The impulse-noise tests yield similar results to those of the white-noise tests, as highlighted in Table 10.7, ie. 2B1Q offers the highest performance, followed by MMS43 and SU32.

10.4 Transmit Power Tests

10.4.1 Test Procedure

In order to measure the average power appearing at one end of a U-interface, use is made of the attenuation pad shown in Figure 10.5. This device replaces the cable for the purpose of accurately measuring the power developed across one end of the pad. The resistor values shown in Figure 10.5 are chosen so to achieve an insertion loss of 33dB between terminals AB and XY, while maintaining a load impedance of 140 ohms at either end.

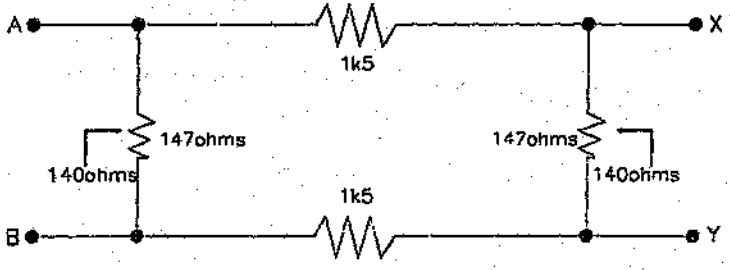


FIGURE 10.5 : ATTENUATION PAD

In order not to cause imbalance in the transmission system, the power measuring device is required to present a balanced load impedance to each of the input terminals A and B. This is achieved through a high impedance transformer coupling as shown in the Transmit Power Measurement setup of Figure 10.6.

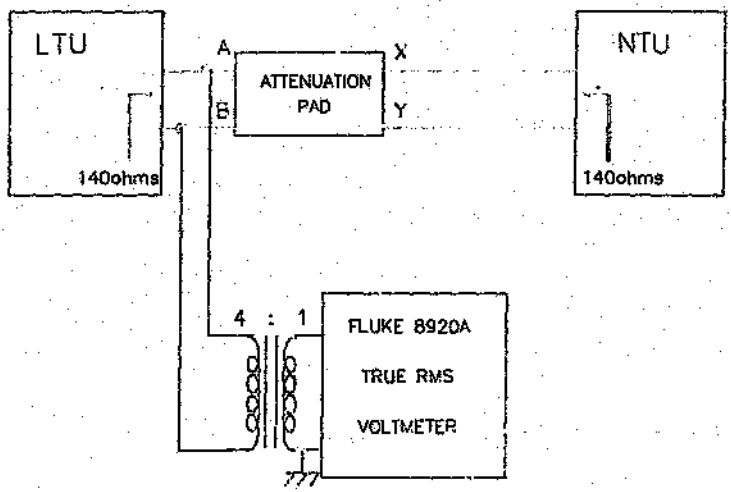


FIGURE 10.6 : TRANSMIT POWER MEASUREMENT SETUP

The procedure for measuring the transmit power is quite straightforward. Each of the three U-interface systems is activated with the attenuation pad in place. The RMS voltage reading is then recorded.

10.4.2 Test Results

In order to convert the RMS voltage readings described above, into true power values, a resistive load of 140 ohms is assumed at the input to the attenuation pad. The results are summarised in Table 10.8.

SYSTEM	RMS VOLTMETER READING (mV)	TRANSMIT VOLTAGE (mV)	TRANSMIT POWER INTO 140ohms (mW)	TRANSMIT POWER INTO 140ohms (dBm)
2B1Q	398	1592	18,1	12,6
MMS43	368	1472	15,5	11,9
SU32	310	1240	11,0	10,4

TABLE 10.8 : Transmit-Power Results

10.4.3 Analysis of Results

The results of Table 10.8 highlight an important characteristic of U-interfaces, and transmission systems in general. Increased transmit power does not necessarily imply increased transmission range. In fact, the SU32 system requires a transmit power 1,5dBm lower than that of the MMS43 (10,4 vs 11,9 dBm), yet it achieves a noise-free range of

approximately 8dB higher (58 vs 50 dB) when measured at 100kHz on 0,4mm cable. The 2B1Q system, due to its quaternary line code, needs a relatively high transmit power to achieve the required signal-to-noise ratio at its maximum range.

10.5 Transmit Power Spectra

10.5.1 Test Procedure

The test setup for measuring the output spectra is essentially the same as that shown in Figure 10.6. However, in place of the RMS voltmeter, a HP3577A Network Analyser, is substituted. The Network Analyser is set to a sweep time of 10 seconds, with start and stop frequencies of 0 Hz and 500 kHz respectively. The resolution bandwidth is set to 1kHz.

10.5.2 Test Results

The recorded power spectra of the 2B1Q , MMS43 and SU32 systems are reproduced in Figures 10.7 to 10.9 respectively.

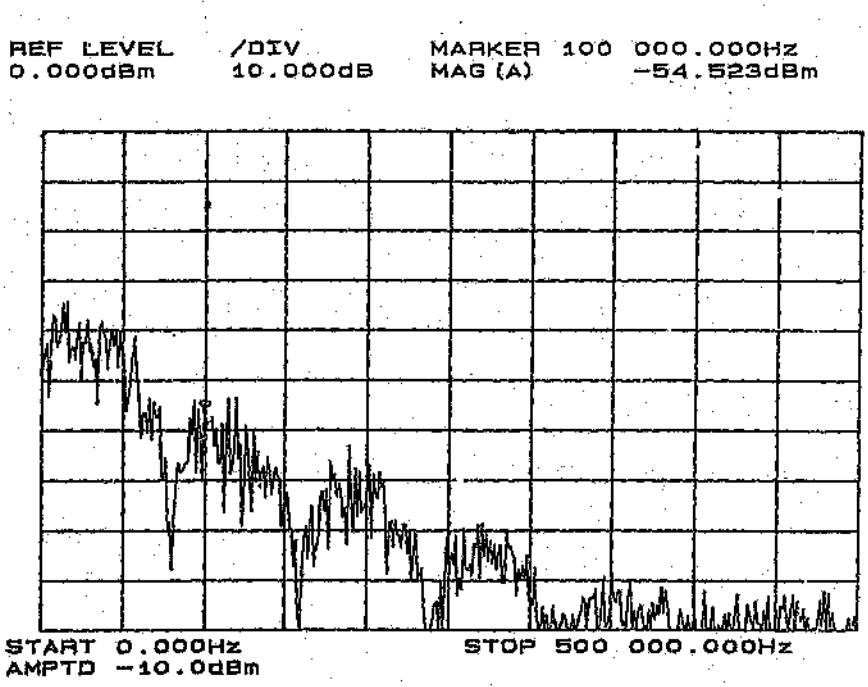


FIGURE 10.7 : 2B1Q POWER SPECTRUM

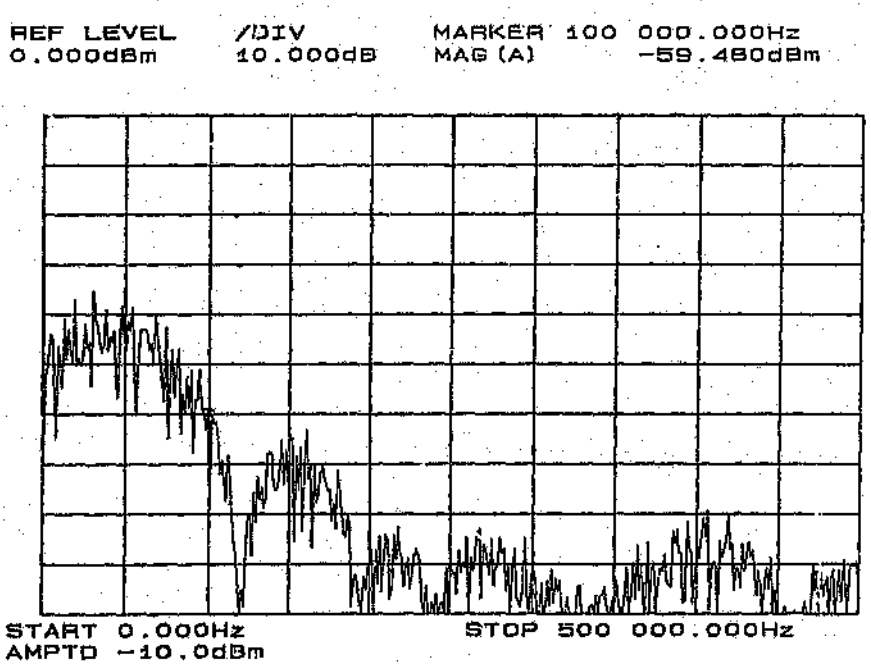


FIGURE 10.8 : MMS43 POWER SPECTRUM

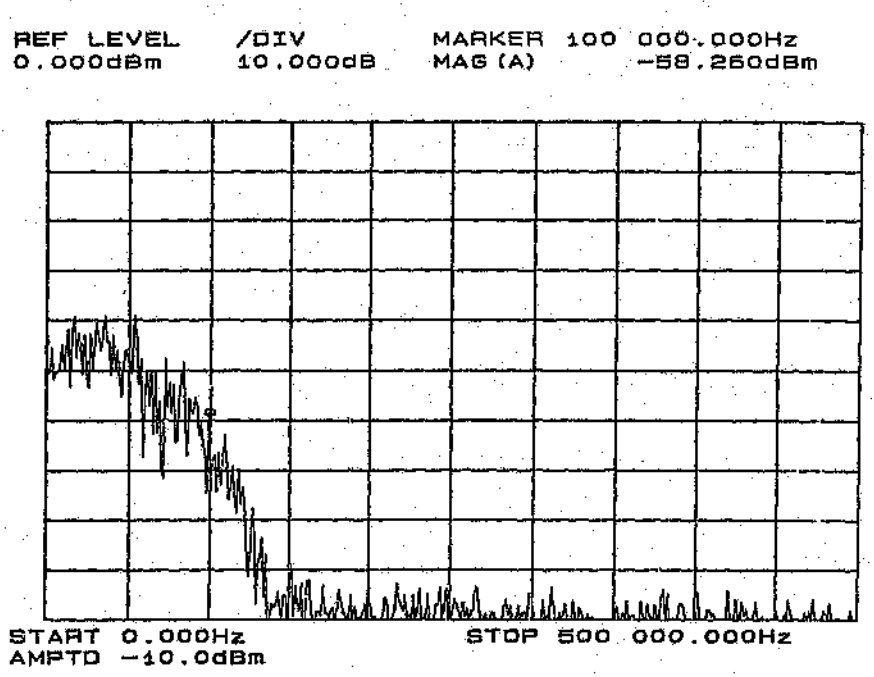


FIGURE 10.9 : SU32 POWER SPECTRUM

10.5.3 Analysis of Results

Figures 10.7 to 10.9 do not depict absolute values of power spectral density. In converting to absolute values, a correction of +10,5 dBm must be added to each point in the PSD plots, so as to account for the balancing transformer voltage gain, and impedance conversion from 140 ohms to 50 ohms. Of more importance however, is a comparison of the PSD "shapes" for each of the three systems under consideration.

In making comparisons, a useful reference figure is the frequency at which the PSD drops to -20dB of its highest value. With reference to the three PSD's, these frequencies are approximately 60kHz, 95kHz and 90kHz for the 2B1Q , MMS43 and SU32 systems

respectively. It can therefore be concluded that the 2B1Q has the lowest bandwidth requirements, followed by the SU32 and MMS43 systems. This characteristic can be largely attributed to the respective baud-rates of each system, viz; 80, 108 and 120 kbaud.

Another interesting feature of the 2B1Q and MMS43 PSDs, is the presence of transmission nulls at multiples of the baudrates, ie. 80 and 160kHz for 2B1Q , and 120 and 240kHz for MMS43. Conversely, the SU32 PSD is characterised by a low-pass-filtered spectrum, containing negligible energy above 130kHz.

10.6 Clock-Jitter Tests

Of all the tests performed on the U-interface systems, the ones involving clock-jitter proved to be the most challenging. The reason behind the difficulty lies in the fact that a commercially available jitter-meter appears to be unattainable. For this reason, and because jitter is deemed to constitute an important aspect of a transmission systems performance, a special piece of equipment was developed for the sole purpose of facilitating the measurement of clock jitter. The customised "jitter-meter" is not capable of measuring jitter unaided; hence, once captured, the jitter-bearing data is transferred to an IBM "PC", where post-processing produces a value representing the peak-to-peak jitter of the extracted clock.

10.6.1 Test Procedure

The jitter-measurement setup is shown in Figure 10.10.

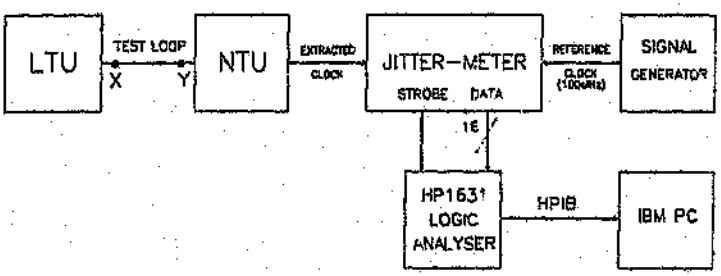


FIGURE 10.10 : JITTER-MEASUREMENT SETUP

The design of the "jitter-meter" is well documented [50], and will not be covered in this report. A brief description of the principle-of-operation, is however necessary, and follows now. The "jitter-meter" comprises essentially two functional building-blocks, viz; a free-running 16-bit counter clocked at 100MHz via the external signal generator, and a 16-bit latch, designed to capture the counter output on every occurrence of an input data

rising-edge. Since the jitter-meter is not equipped with memory, latched values are captured and stored via the logic analyser, before being transferred to the IBM "PC" for further processing.

Due to the limited storage capacity of the HP1631 Logic Analyser, it is essential to minimise the amount of redundant information captured. To clarify this point, consider the following example. The SU32 timing extraction mechanism maintains synchronisation with the received signal, by inserting or deleting a single master-clock cycle if so required, at a particular instant in each frame. Since the frame repetition rate is 1,33kHz, it makes sense to measure the jitter content of a clock designed to be as close to 1,33kHz as possible. Extracted clock frequencies higher than this frequency contain redundant information which limits the useful record length, and hence resolution. The user data-clock of 128kHz is therefore scaled down to 2kHz before being fed to the "jitter-meter" for processing.

In order to yield meaningful jitter measurements, it is necessary to vary the free-running master clocks in the LTU and NTU relative to each other. In practice, the LTU master clock is adjusted to within 2ppm of its nominal frequency, while the NTU master clock is pulled plus or minus 90ppm relative to the LTU clock.

The actual test procedure is as follows. A test loop comprising 4600m of 0,4mm gauge cable, and providing an attenuation of 49,97dB when measured at 100kHz, is inserted between points X and Y of Figure 10.10. For each system, the NTU is pulled 90ppm either way of the LTU frequency, whereafter a jitter data-record is captured. Each record is then transferred to an IBM "PC", where it is digitally processed to yield a pk-pk jitter value.

10.6.2 Test Results

Part of the digital processing performed on the IBM "PC", comprises a HPF, with corner frequency set at 50Hz. The filtering function is necessary to remove the low-frequency jitter components, otherwise known as wander. The pk-pk jitter results are presented in Table 10.9, with and without the inclusion of the HPF.

	FREQUENCY OFFSET					
	-90ppm		0ppm		+90ppm	
SYSTEM	pk-pk Jitter without HPF (UI)	pk-pk Jitter with HPF (UI)	pk-pk Jitter without HPF (UI)	pk-pk Jitter with HPF (UI)	pk-pk Jitter without HPF (UI)	pk-pk Jitter with HPF (UI)
2B1Q	0,003	0,002	0,003	0,002	0,003	0,002
MMS43	0,063	0,022	0,016	0,013	0,063	0,022
SU32	0,070	0,024	0,018	0,014	0,070	0,024

TABLE 10.9 : Clock-Jitter Results

10.6.3 Analysis of Results

The jitter results listed in Table 10.9 shows that the 2B1Q system offers the lowest jitter of all three systems. The reason for this can simply be attributed to the implementation of the receive-clock PLL. In the 2B1Q system, the PLL is implemented externally via an analogue voltage-controlled crystal oscillator. The latter is then pulled to the desired frequency and updated on a continuous basis. The SU32 and MMS43 systems, on the other hand, rely on a free-running crystal oscillator at the NTU. The technique used to maintain synchronisataion with the received signal is a periodic insertion or deletion of a master-clock cycle. Since phase-correction can only be achieved at multiples of a clock-cycle, instantaneous jitter is increased. For the same reason, the MMS43 system's pk-pk jitter is less than that of the SU32 system, due to the former's higher master-clock frequency.

10.7 Activation-Time Tests

The activation-time of a transmission system can be defined as the time taken from initiation of an activation sequence to the establishment of a full duplex transparent data-channel. As will be shown later, a substantial variation exists in the activation times of the three U-interfaces.

The 2B1Q system provides a feature not supported by the other two systems, viz; the ability to perform either a "cold-start" or a "warm-start". The former applies to a power-on activation-sequence, while the latter facilitates a faster activation due to previously stored EC and DFE coefficients. The requirements for a "warm-start" include firstly, a previously achieved orderly deactivation sequence, and secondly, an uninterrupted power supply during a state of deactivation.

10.7.1 Test Procedure

The activation-time of the U-interface chip-sets is measured quite simply by means of the HP1631 Logic Analyser. All three transmission-systems are controlled via the terminal keyboard which, on having the appropriate key pressed, initiates a microcontroller software routine. The latter issues the commands necessary to activate or deactivate the transmission system. On detection of the activation command, the Logic Analyser is triggered, thereby recording the time taken from the start-of-activation to the completion-of-activation sequence. Each chip-set's activation time is then directly read off the Logic Analyser display.

For the purposes of this test, four experiments are conducted to ascertain the activation-time characteristics of each system, viz. 2B1Q "cold-start", 2B1Q "warm-start", MMS43 and SU32. In each experiment the systems are successively activated using one of three standard cable lengths of 0,4mm guage cable, labelled "short", "medium" and "long" respectively. The lengths and attenuations of each cable section are shown in Table 10.10. This table also lists the

mean activation-time μ, for each trial, the maximum activation-time MAX, the standard deviation σ, as well as the coefficient of variation denoted σ/μ. The latter figure gives a normalised indication of the "spread" of values for each trial.

10.7.2 Test Results

The results of the tests are presented in Table 10.10.

SYSTEM	SHORT-CABLE 1860m or 19,96dB				MEDIUM-CABLE 3720m or 39,90dB				LONG-CABLE 4650m or 49,97dB			
	$\mu(ms)$	MAX (ms)	σ	σ/μ	$\mu(ms)$	MAX (ms)	σ	σ/μ	$\mu(ms)$	MAX (ms)	σ	σ/μ
2B1Q - Cold Start	2061,5	2100	20,2	0,0098	2070,1	2109	19,9	0,0096	2116,0	2232	56,5	0,027
2B1Q - Warm Start	91,3	96,9	2,8	0,031	102,3	109,8	3,8	0,037	123,1	141,8	8,8	0,071
MMS43	574,9	605,7	15,9	0,028	649,7	702,8	25,4	0,039	3059,1	3612	275,7	0,090
SU32	116,0	117,8	1,05	0,009	116,9	119	1,07	0,0091	116,0	118	1,06	0,0091

TABLE 10.10 : Activation-Time Results

10.7.3 Analysis of Results

Table 10.10 highlights the large variation in activation-times for different systems and different test-loops. The SU32 system exhibits activation-times which are largely invariant with increases in cable attenuation, as well as offering the fastest "cold-start" time of all the systems. Its "spread" of values also appears to be constant for each cable length.

The MMS43 system does not support a "warm-start" option, but offers activation-times which are quite acceptable with short and medium cable-lengths. With long cable-lengths (ie. > 4,6km), its activation-times are fairly long, being in excess of 3 seconds. Interestingly, its coefficient of variation tends to indicate a somewhat broader spread of activation-times for long cable lengths.

The 2B1Q activation-times increase slightly with increases in cable-length. The "cold-start" times are relatively long, but are quite acceptable when considering the fact that a "cold-start" is usually necessary only after a loss of power. Since this should rarely occur in practice, the duration of the "cold-start" is generally unimportant. The 2B1Q 's "warm-start" time is, however, superior to all other systems with short- and medium-length cables, and only marginally inferior to the SU32 system's activation-time when transmitting over a long-cable. Its spread of activation times is also relatively confined especially in its "cold-start" mode.

Appendix B offers a graphical representation of each trial's results in the form of Probability Distribution Functions (PDF).

11 CONCLUSION

The essential aim of this chapter is to integrate the findings of the previous chapter into a coherent form. In so doing, a framework will be provided on which a recommendation regarding a U-interface suited to the SAPT network, can be based.

Thusfar in this report, no consideration has been given to economic factors. The latter may, in fact, constitute the overriding criteria in selecting an optimal solution. Stated another way, it would indeed be inappropriate to suggest a solution offering marginal technical advantages, yet involving a cost which is totally prohibitive. It must be borne in mind that, if ISDN is to be implemented in SA, every subscriber-loop will eventually be provided with two U-interface chip-sets, ie. one at each end of the loop. The fact that two voice-channels (or even four, if for example, ADPCM is employed) are in principle available, will not increase revenue if the vast majority of subscribers still require but one telephone. In other words, for ISDN to be economically viable inasfar as the average household is concerned, the cost of an "ISDN telephone" must be no higher than that of its traditional analogue counterpart. With the above in mind, attention will also be directed at economic factors when making a final recommendation later in this chapter.

11.1 Technical Considerations

With reference to the noise-free test results listed in Table 10.2, it is evident that the MMS43 system is clearly inferior to the 2B1Q and SU32 systems in terms of transmission range. The 2B1Q system, for example, is capable of operating over a distance which exceeds that of the MMS43 system by 930m, or 20% (assuming 0,4mm cable). The difference between the SU32 and 2B1Q systems is less marked. A mere 160m, or 3% using a 0,4mm cable, separates the two system's capabilities, with 2B1Q being superior.

In respect of range performance in a noisy environment, a slightly differently picture emerges. Table 10.5 indicates that MMS43 offers improved white noise performance over SU32, particularly at lower cable-lengths. MMS43 even displays better white-noise performance over 2B1Q at cable-lengths below 3km. However, the 2B1Q system emerges the most tolerant to white-noise interference for cable-lengths in excess of 3,5km (assuming a 0,4mm cable). The impulse-noise results of Table 10.7 elicit similar conclusions about relative performance, while the sine-wave interference results depicted in Table 10.6 suggest a 2B1Q, SU32 and MMS43 order of merit.

In terms of transmit power, 2B1Q's superior performance is offset by an incurred penalty, viz; a substantially increased transmit power. The negative consequence of this is a corresponding increase in the level of crosstalk generated. However, as the plots of power spectra shown in Figures 10.7 and 10.9 prove, 2B1Q exhibits the lowest bandwidth

requirements. This factor produces the counter-effect of potentially lowering the crosstalk power. Overall therefore, the additional benefits of range and noise performance which 2B1Q offers, offsets the increased transmit power requirements. Interestingly, SU32 offers the best range vs transmit-power ratio of all three systems; yet this fact is more of academic interest than practical importance.

The jitter results are of less significance when choosing one of the three systems. The reason for this is simply the following. Jitter performance is essentially a result of the chosen implementation of a system's clock-extraction circuitry. While pilot-tone timing techniques can be shown to offer intrinsically superior jitter performance to Barker-code techniques, it is basically the design of the clock-extraction PLL which determines the jitter performance. In the case of the three systems under consideration, the 2B1Q implementation employs an external analogue PLL which offers superior performance relative to the digital PLL implementation of the MMS43 and SU32 systems. The aim of this chapter, however, is to recommend a generic system based on a specific line code, while not being restricted to a particular chip-set or manufacturer.

In terms of activation time as shown in Table 10.10, the SU32 system offers the best performance under all conditions. However, as explained in the previous chapter, the relatively long activation-time of the 2B1Q system in its "cold-start" mode, is quite acceptable considering the expected infrequency of a "cold-start". In contrast, the 2B1Q system offers the best "warm-start" activation-time for short- and medium-length cables.

From a technical point of view, therefore, it is believed that the 2B1Q system offers the best solution to the U-interface requirements for a South African ISDN.

11.2 Economic Considerations

It should be mentioned at the outset that component costs are dynamic, and subject to vast fluctuations dependent on various factors. One of the most influential factors in determining the cost of a component or system, is that of demand. This latter parameter can affect the price of a chip by orders of magnitude, since the actual cost of a piece of silicon and its encapsulation, is relatively small compared with the cost of setting up the fabrication process.

With the above in mind, consideration of economic factors implies essentially a prediction of world-market requirements. There is no way of accurately predicting market requirements, but the following facts may help to improve the probability of an accurate prediction. Firstly, the American Telecommunications Authority (ie. the ANSI T1 Committee) has opted for the 2B1Q standard. Secondly, it is believed that the Deutsche Bundespost may be considering a shift to the 2B1Q standard. Thirdly, BT, due to its interest in the semiconductor company, Mitel, may also consider adopting the 2B1Q standard, since Mitel

is at an advanced stage of producing a 2B1Q chip-set. It is therefore strongly believed, albeit with a small element of risk, that the future de facto world-standard for the U-interface will be 2B1Q. Based on this assumption, one could state with reasonable certainty that the prices of 2B1Q chip-sets will be lower than any other U-interface chip-set.

11.3 U-Interface Recommendation

From both a technical and an economic view point, it is believed that the 2B1Q system, as based on the ANSI T1.601 standard, offers the most attractive U-interface solution for an ISDN in South Africa. The results presented in this report should add credibility to this recommendation.

APPENDIX A : PILOT-TONE TIMING EXTRACTION TECHNIQUE

1 INTRODUCTION

The purpose of a timing extraction system is to enable the receivers at both ends of the system to select the most advantageous sampling phase in respect of error free detection of the data, and generate at the subscriber end, a stable low-jitter clock synchronised to the exchange clock.

The performance of the timing extraction at a U-interface receiver is dependent on the intrinsic properties of the signal transmitted over the interface. The use of a deterministic signal added to the data can substantially enhance these basic properties, and result in much improved performance of the timing extraction function, accompanied by simplification of the entire system.

In the full duplex subscriber-loop requirement, where bandwidth of the transmitted signal is at a premium, it is highly advantageous to confine the effect of such a timing signal to the specific timing function required. Other features, such as code choice and frame synchronisation method, may then be independently optimised, resulting in the most optimum interface definition.

There are several criteria by which the acceptability of a particular timing extraction method may be judged. The following criteria are suggested:

1.1 Robust Operation

The maintenance of timing under high error rates is essential. Failure of timing extraction will lead to collapse of the transmission channel. It is an important feature of a synchronous transmission channel that once frame synchronisation has been established, the maintenance of bit-timing is sufficient to ensure that frame synchronisation is correct.

1.2 Fast acquisition of bit timing at the start of the call

The fast acquisition of the correct sampling phase at the exchange- and subscriber-ends of the system aids in reducing the overall system training time.

1.3 Location of the correct timing instant for good performance

The convergence and signal-to-noise ratio of an adaptive equaliser is dependent on the correct data sampling phase. Substantial deviation from this point will reduce performance, which in the extreme case will lead to failure of the system to train or to operate properly.

1.4 Regeneration of a low jitter clock phase-locked to the exchange

The CCITT requirement for the S-interface requires < 5% pk-pk jitter measured with a 50Hz high-pass filter referred to a 192kHz clock cycle. (5% of a 912kHz clock cycle corresponds to 260nS).

1.5 Electromagnetic compatibility

The use of a deterministic signal by definition will introduce spectral lines into the signal frequency spectrum. These must neither cause interference to other systems or be sensitive to interference likely to exist.

2 SYSTEM FEATURES RESULTING FROM THE USE OF A PILOT TONE

The use of a pilot tone gives the following performance and implementation features.

* Adjustment of the timing phase is based on a single sample per baud. The phase relationship between data and pilot is arranged so that the same sample is used for data detection. The sampling rate of a front end Analogue-to-Digital converter and any signal processing prior to and including the receiver need only operate on one sample per baud.

* Timing information is to be added to the transmission code without increasing the code baud rate. The transmission code therefore needs no redundancy for the purpose of clock extraction.

* The only performance penalty incurred is the power needed for transmission of the tone which in the case of the SU32 system, is one twentieth of the power used for data transmission. The pilot does not degrade the detection process.

* During start up of the system, transmission of the pilot alone, permits very rapid acquisition of the correct timing phase before any data is transmitted. This property is used to preset the exchange-end of the system to a sampling phase which need not be changed for the duration of the connection. Under steady state conditions, the pilot need only be transmitted in the exchange to subscriber direction.

* The outgoing pilot is eliminated from the received data at the exchange-end by a single tap in the EC adaptive filter.

  The pilot is simply estimated at the subscriber receiver by a single tap in the DFE.

3 SYSTEM IMPLEMENTATION USING A PILOT TONE

In a local loop transmission system, the exchange-end acts as the master frequency reference, and the subscriber-end is slaved to the phase and frequency of the exchange-end data. The system operates in two modes; a) training, and b) steady state. Most circuitry is common to both modes.

During steady state operation, pilot tone transmission only occurs in the exchange to subscriber direction, and the exchange-end sampling phase is fixed. In the reverse direction, the pilot is only used during training, and the subscriber pilot transmission circuitry and exchange pilot recovery circuits are inoperative during steady-state transmission. The relationship between a data clock of frequency f0 = 108kHz, and example SU32 coded data, is given in Figure A1.

The pilot tone is a square-wave of frequency f0/2 = 54kHz, and the phase relationship between the data and the pilot tone is such that transitions of the pilot occur midway between transitions of the data waveform. The pilot tone itself is produced from a halving of the pilot tone clock as depicted in Figure A1.

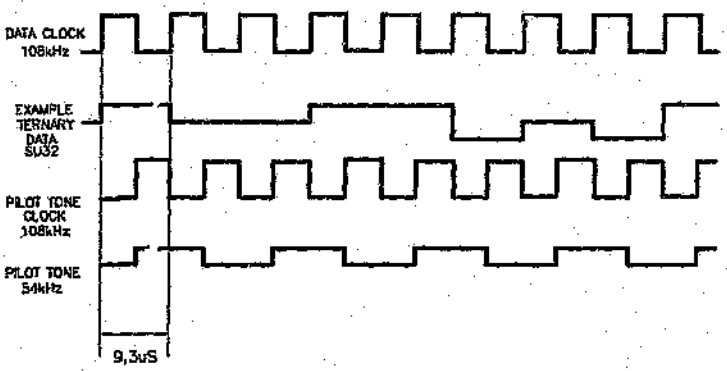


FIGURE A1 : PILOT AND TIMING DIAGRAM

Addition of the pilot tone to the PAM data-stream requires a simple summation which can be achieved digitally using, for example, two's complement number representation of the data signal and pilot amplitude.

The peak amplitude of the pilot is scaled to be one quarter of the peak amplitude of the data signal at the point of addition in the 144kbit/s subscriber loop application. This ratio is not critical, and is chosen to suit the parameters of the data receiver and data channel.

A low pass filter is placed between the pilot addition circuit and the transmission buffer amplifier for the purpose of controlling the transmitted data spectrum so as to limit interference. The composite signal is then transmitted onto the cable through the hybrid coupling network.

3.1 Cancellation of the Local Pilot Tone

The operation of an echo canceller designed to remove the local signal component from the received sampled data signal is well known. This structure may be simply modified to include an adaptive coefficient for the elimination of the locally generated pilot tone from the received signal samples as shown in Figure A2. The method of adaption and rate of adaption of this coefficient is similar to that of all other coefficients, and adjustment is proportional to the estimated gradient of the coefficient mean square error. Instead of being excited by the data sequence, the pilot excitation is the 54kHz alternating sequence +1, -1, +1, -1 etc.

The ternary data sequence is scrambled, and contains no stationary component at the half baud rate frequency; the pilot coefficient therefore converges to give an accurate estimate of the value of the sampled pilot component value, and it is therefore eliminated from the received data.

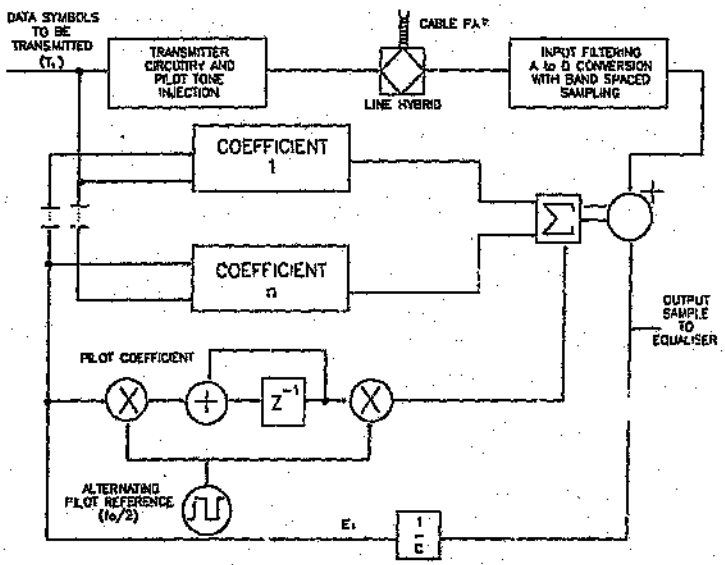


FIGURE A2 : ECHO CANCELLATION OF DATA AND PILOT

3.2 Steady-State Receiver Phase Adaption

Figure A3 shows the structure of the receiver. The purpose of the timing extraction circuit is to adjust the time at which the composite received signal is sampled by the sample and hold circuit which precedes the A to D converter.

In the steady state mode of operation, transmission and timing extraction have been established in both directions. Data plus pilot is being transmitted from the exchange to subscriber, and data only from the subscriber to the exchange. The subscriber sampling phase is determined by a digital phase locked loop which adds or subtracts cycles of a higher frequency clock from the sample and hold clock.

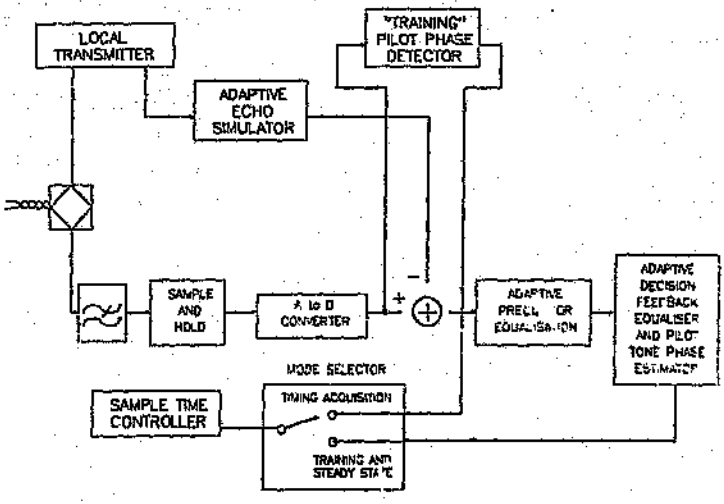


FIGURE A3 : SUBSCRIBER RECEIVER DIAGRAM

3.3 The Phase Discrimination Function

The direction of adjustment of sampling is determined by whether the pilot tone zero crossing precedes or follows the sampling point. The purpose of the timing extraction is to adjust the position at which the signal is sampled, to the point at which the pilot tone waveform crosses zero.

At the receiver sampling point, the continuous pilot tone component of received signal will resemble a sine wave due to the low pass characteristics of the transmitter, channel and receiver low pass filter. The sampling period and pilot tone will be of similar frequency, and the sample value will be alternately positive and negative with virtually the same absolute amplitude.

Since a decision feedback equaliser is employed in the receiver, it is possible to employ a very simple but accurate and low noise pilot tone phase discriminator. A single additional tap is introduced into the DFE to both estimate and eliminate the pilot tone amplitude. The direction of adjustment of the sampling time of the receiver needed to locate the zero crossing is simply determined from the sign of this coefficient.

Operation of this coefficient is similar to the pilot coefficient in the echo canceller already described. The coefficient used differs from the normal DFE coefficients, in that the decision data input is replaced by an input toggled at 54kHz. When the DFE is receiving error-free data, there is very little noise enhancement in estimation of the pilot phase, because all components of the superimposed data signal are removed by the equaliser simultaneously with the pilot component. Note that any small phase error resulting in a residual level of pilot tone superimposed on the data samples, will be eliminated by the pilot tone tap in the equaliser.

APPENDIX B : PROBABILITY DISTRIBUTION FUNCTIONS OF ACTIVATION TIMES

Figures B1 to B12 depict : Probability Distribution Functions (PDF) of activation-times for the four systems (viz. 2B1Q "cold start", 2B1Q "warm start", MMS43 and SU32) under conditions of three different cable lengths labelled "short", "medium" and "long" respectively. The cable characteristics for each of the three cables are as shown in Table B1

CABLE (0,4mm GUAGE)	LENGTH (m)	ATTENUATION (dB @ 100kHz)
Short	1860	19,96
Medium	3720	39,90
Long	4650	49,97

TABLE B1 : ACTIVATION-TIME CABLE CHARACTERISTICS

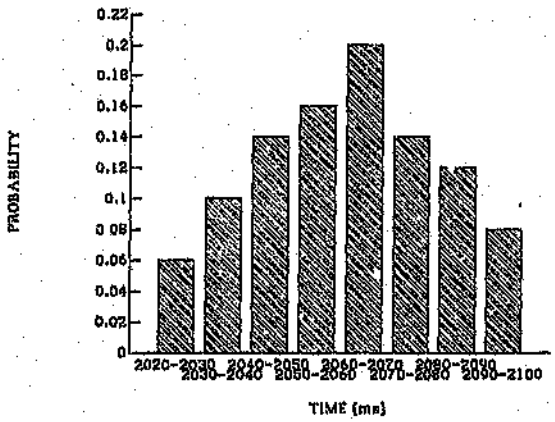


FIGURE B1 : ACTIVATION-TIME PDF-2B1Q (COLD START/SHORT CABLE)

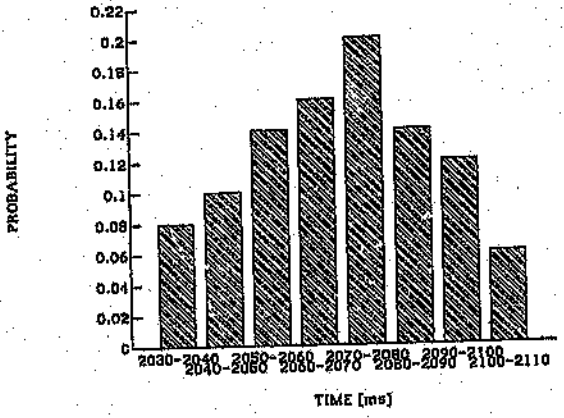


FIGURE B2 : ACTIVATION-TIME PDF-2B1Q (COLD START/MEDIUM CABLE)

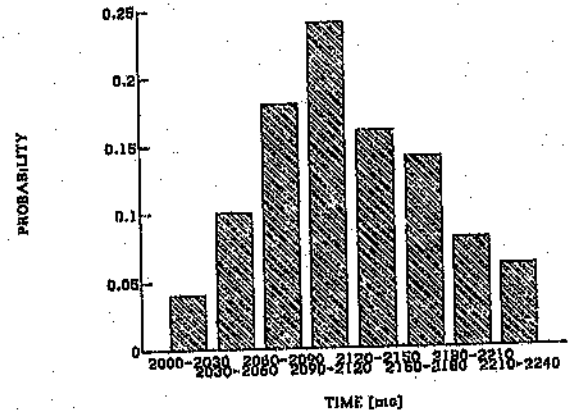


FIGURE B3 : ACTIVATION-TIME PDF-2B1Q (COLD START/LONG CABLE)

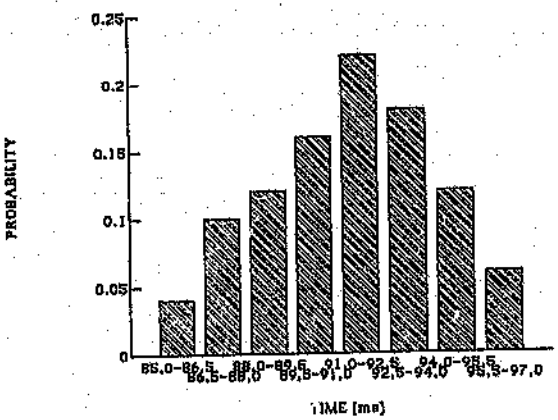


FIGURE B4 : ACTIVATION-TIME PDF-2B1Q (WARM START/SHORT CABLE)

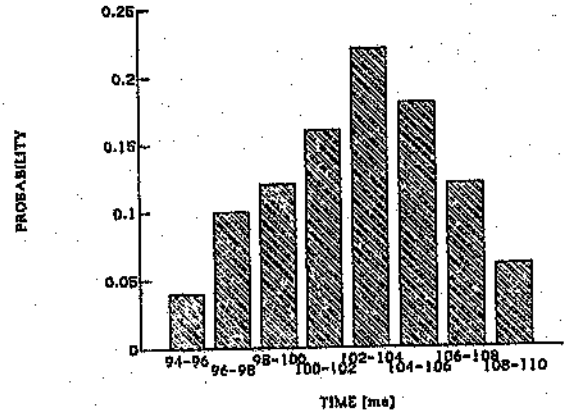


FIGURE B5 : ACTIVATION-TIME PDF-2B1Q (WARM START/MEDIUM CABLE)

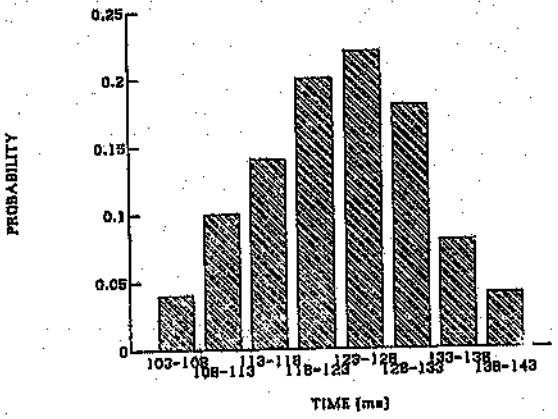


FIGURE B6 : ACTIVATION-TIME PDF-2B1Q (WARM START/LONG CABLE)

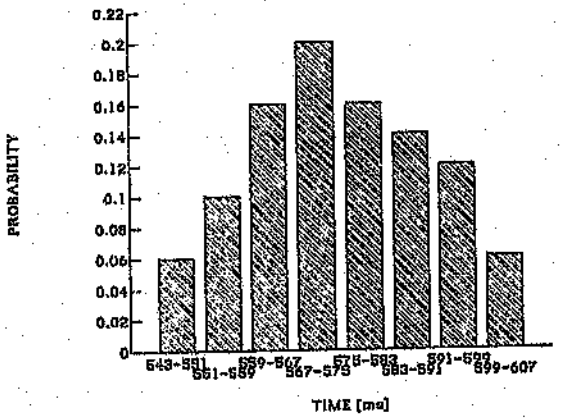


FIGURE B7 : ACTIVATION-TIME PDF-MMS43 (SHORT CABLE)

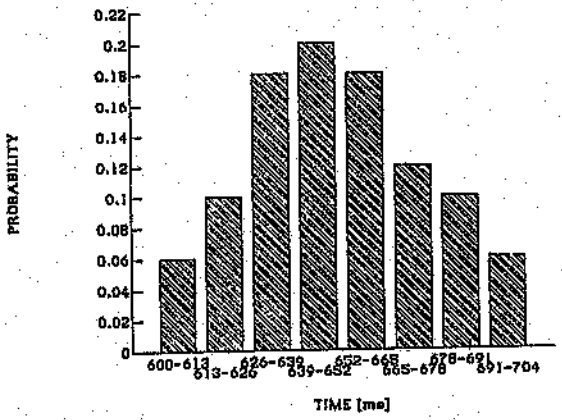


FIGURE B8 : ACTIVATION-TIME PDF-MMS43 (MEDIUM CABLE)

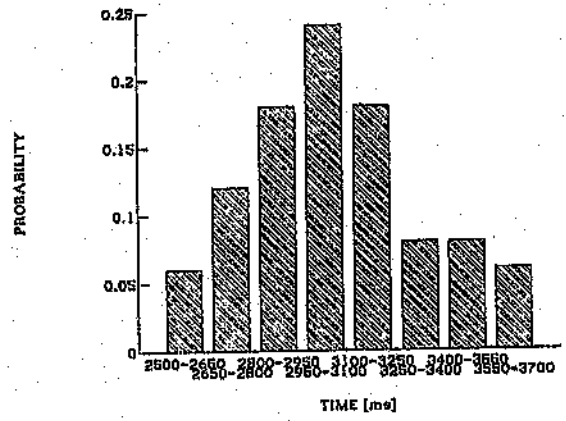


FIGURE B9 : ACTIVATION-TIME PDF-MMS43 (LONG CABLE)

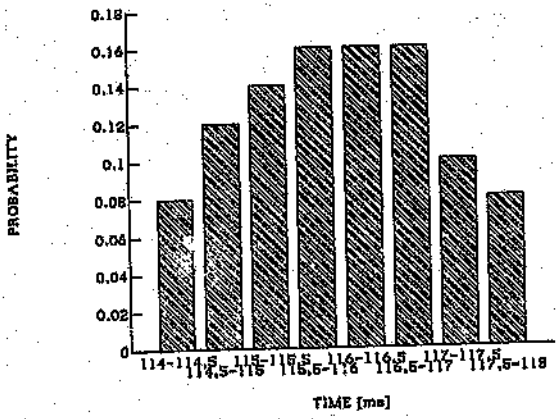


FIGURE B10 : ACTIVATION-TIME PDF-SU32 (SHORT CABLE)

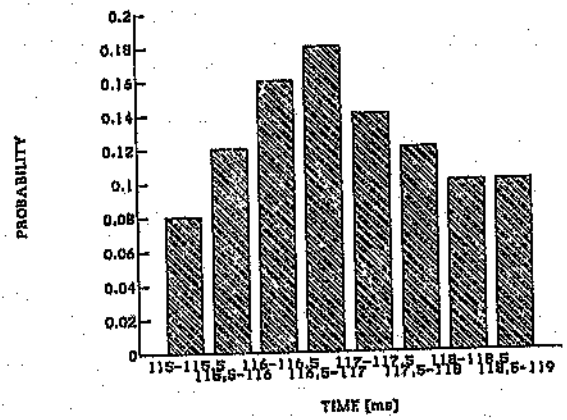


FIGURE B11 : ACTIVATION-TIME PDF-SU32 (MEDIUM CABLE)

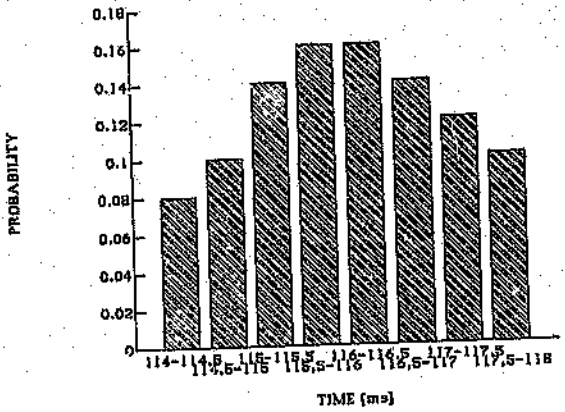


FIGURE B12 : ACTIVATION-TIME PDF-SU32 (LONG CABLE)

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