6 Analogue switch/ sample-and-hold/ analogue-to-digital conversion circuit

6.1 Design

Both positive and negative signals are handled by this board. The input signals are processed by very fast sample-and-holds and analogue-to-digital converters. Both the hardware to develop the signal control pulses and the interface between the microprocessor are contained on this board. The switching circuit used to select which peak detector channel is to be passed to the sample-and-hold is also on this board, and this circuit uses high speed, low impedance CMOS analogue switches controlled by TTL switching levels.

A 16-bit data bus is used between the microprocessor and the peripheral devices. The data concerning the multiplication factors and the output of the analogue-to-digital converters is represented as follows:

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[0][0][0][0][x][x][x] [x][x][x][x] [x][x][x][x]
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Multiplication factor   Data

This data is written into memory using the analogue-to-digital converter end of conversion pulse.
6.2 Operation

A full circuit diagram is shown in Figure A9 sheets 1, 2 and 3.

The four positive and four negative input signals come into two quad-input analogue switches, one to handle the positive signals, and the one to handle the negative signals. These input signals are the ones produced by the peak detector boards which have $x_1$, $x_{10}$, $x_{100}$ and $x_{1000}$ multiplication factors associated with them. These signals which control the switching of the analogue signals are produced on the switching board. The outputs of all the positive switches are tied together as are the outputs of the negative switch, and this is connected to the input of the positive and negative sample-and-holds respectively.

The leading edge of the pulse which is produced by a sampled signal is used to develop a 1 micro second positive going mono-stable pulse. This signal is also used to produce a 20 micro second negative going mono-stable pulse. These signals are then cross coupled so that the negative channel is blanked for 20 micro seconds when the positive channel is processing a signal and visa versa. This blanking is done using the +1 micro second pulse and negative 20 micro second pulse tied to a NAND.
gate, whose output is used to drive the sample input of the positive sample-and-hold.

Similarly the negative 1 micro second pulse is connected with the positive 20 micro second pulse to a NAND gate, the output of which is used to drive the sample input of the negative sample-and-hold. In order to produce the positive and negative start convert pulses of the analogue-to-digital converter the trailing edge of the positive or negative inverted sample pulse is used. The output of the sample-and-hold is fed to the input of the analogue-to-digital converter, which on reception of the start convert trailing edge starts its conversion cycle. Once the cycle is complete, the converter produces an end of conversion pulse which is used to drive a mono-stable the output of which is used to latch the 8-bit output of the converter into a buffer. This pulse is also used to latch the multiplication factor into a buffer. Both positive and negative channels operate identically.

The input signals are applied to the positive and negative switching circuits IC11 and IC12 and passed to the sample-and-holds IC1 and IC6. The control pulses for the sample and start convert pulses are developed by IC13, IC14, IC15 and IC16. The blanking circuit and inverter use four dual input NAND gates. From the sample-and-hold the signal is processed by the analogue-
to-digital converters IC2 and IC7. The pulse to control the updating of the 3 bits of converted data and 4 bits of multiplication factor into buffers is developed in IC4 and IC9. The output data buffers are IC5 and IC10. The output multiplication buffers are IC3 and IC8.

7 Microprocessor Interface board

7.1 Design

This is a multi-function board which provides the following features: A common data bus between the output of the analogue-to-digital converter, the multiplication buffers, the timing circuitry and the microprocessor. An interface between the instrument's data bus and the microprocessor's data bus. A clock which gives the number of mains cycles which have passed as well as the fraction of the present mains cycle that has passed. Address decoding that makes the data buffers part of the microprocessor's memory map is used.

To speed transfer of data, the 8 buffers into which data is written are addressed as memory. All these buffers are connected using a 16-bit local data bus, and the board's local data bus is tied to the 16-bit microprocessor data bus via a line driver.
There are four sets of data buffers, one for the positive peak detector's data and multiplication factor, one for the negative peak detector's data, and multiplication factor and two for the clock signal. These buffers are given the hexadecimal addresses 8000, 8002, 8004 and 8006.

The clock signals are written into the buffers at the same time as the analogue-to-digital converter data is written into the buffers, thus avoiding any timing complications which could arise.

7.2 Operation

A full circuit diagram is shown in Figure A10. This board is designed to provide the interface between the 68000 microprocessor and the digital partial discharge unit. The 68000 board uses memory locations up to 7FFF, and leaves all locations above this free. There is a memory decoder which divides the memory between 0000 and 3FFF, 4000 and 7FFF, 8000 and 11FFF and 12000 and 15FFF.

7.2.1 Addressing

When any address in the 8000 to 11FFF range is selected the appropriate decoder output is also selected. The microprocessor interface board has been memory mapped
into the address range 8000 hexadecimal to 8007 hexadecimal.

No data is ever written to the device from the microprocessor, and hence it is in read only configuration. The device is selected by a combination of the R/W signal and the select 8000 hexadecimal block signal. They are combined via an AND gate and the signal is used to enable the two 8-bit line drivers which link the instrument to the microprocessor data lines. This guarantees that the board will only be selected when an address above 8000 hexadecimal is selected. This means that partial address decoding can be used to enable each of the four buffer sets, as the internal data bus is only connected to the microprocessor data bus when addresses above or equal to 8000 hexadecimal are selected. The lower four outputs of a four input ten output 74LS42 decoder are used to select each of the four groups of buffers. The input to this decoder are derived from address lines A1, A2, A3 and A4 from the 68000 microprocessor. The combination of this and the board select signal result in the addresses 8000, 8002, 8004 and 8006 hexadecimal.

8000 is used to select the positive peak detector buffer, 8002 for the negative peak detector, and 8004 and 8006 are used to select the clock buffers. The above system means that whenever any combination of A1
and A2 are selected one of the buffers will be selected, and data will be present on the local data bus, but data will not be presented to the 68000 data bus until both the read signal and select 8000 block signal are present, thus insuring that two conflicting sets of data cannot be present on the data buses at the same time. Each address buffer can also be addressed by a set of addresses between 8000 and 11FFF, because of partial address decoding. This is not important because nothing is addressed above 8006.

7.2.2 Clock circuitry

The clock circuit is split into two sections:

1. A clock which counts the number of mains cycles that have passed.

2. A clock which counts the amount of the present cycle that has passed.

The clock is required to give the position of the impulse with respect to the mains frequency waveform. Because the signal must be compared with the mains, the mains signal is used to develop the clock signal. The mains waveform is stepped down and compared with ground. This will produce a square wave with the same zero
crossings as the AC waveform. The rising edge of this waveform is then used to produce a signal from a mono-stable. This is necessary because the waveform produced by the comparator has noise on it and the mono-stable effectively filters this noise. The signal is then used to drive the clock input of four 4-bit counters which give a maximum of a 16-bit representation of the number of mains cycles passed. The counters have a switch which resets the counter. The output of the counters is fed to a buffer.

A second set of four counters is used to detect the fraction of the mains cycle that has passed. A 40KHz timer provides the clock signal used to produce the 25 microsecond intervals in which increments the counter. This counter is reset at the start of every new mains cycle by a mono-stable controlled by the mains signal. The output of the counter is also fed to a buffer. The time of occurrence of both the positive and negative peak detected data must be determined and hence signals which update both the positive and negative analogue to digital buffers are combined using an OR gate and this signal is used to write the clock data into the clock buffers.

7.2.3 Data busses

The local 16-bit data bus connects the output of the
four buffers together and takes them to a line driver which connects the local bus to the 68000 data bus.

The address decoding for the four buffer sets is done by a 74LS42 binary to BCD decoder (IC9). The buffers are 74LS373 tri-state buffers (IC7, IC8, IC15 and IC16) and the line drivers are 74LS245s (IC17 and IC18).

An LM311 comparator (IC1) drives two 74121 mono-stables (IC2 and IC10), the one producing the clock for the one set of counters, the other producing the reset pulse for the other set of counters. A 555 timer (IC9) is used to produce the clock signal for the second set of counters. Both sets of counters are 74LS161s (IC3, IC4, IC5, IC6 and IC10, IC11, IC12, IC13).
APPENDIX B

Calibration Results

To produce a calibration graph, 5, 40, 500 and 5000pC signals were used for the positive channel and -5, -50, -500 and -5000pC signals were used for the negative channel. The negative 5pC signal result is shown in table B1, the 50pC in table B2, the 500pC in table B3 and the 5000pC in table B4. The positive 5pC signal result is shown in table B5, the 50pC in table B6, 500pC in table B7 and 5000pC in table B8. The negative calibration table is shown in Figure B1 and the positive calibration table is shown in Figure B2.

The reading at each test charge value fluctuates because of low frequency noise in the system from the earthing and hence the value used for the graph is an average of these values.