Figure A4: Comparison between the input signal and the attenuated output of the peak detector.
The peak detector pulse is used to drive a 4 stage isolating buffer. This is then combined with the peak signal via an isolator, and this signal is used to control the peak detector. The peak value is shown to be equal to the input amplitude, which means that there is enough time for the isolating buffer to match the signal.

Figure A5 Generation of the pulse used to select the analogue switch
comparator is shown in Figure A6.

In this case the trailing edge of the pulse represents the detection of a peak. As was mentioned before the initial peak decays very quickly, and the circuit is reset before the peak can be sampled by the sample-and-hold. To stretch the signal the following technique is used:

The peak detector pulse is used to fire a 4 micro second mono-stable. This is then combined with the reset pulse via an OR gate, and this signal is used to reset the peak detector. The reset pulse is therefore at least 4 micro seconds long, which means that there is enough time for the sample-and-hold to sample the signal.

The circuit is split following the buffer (IC6) between the reset circuitry and the peak detector pulse circuitry. The reset signal circuitry consists of a variable attenuator (IC8) which attenuates the signal produced by the peak detector. This signal is then compared with the input signal using a comparator (IC10). The peak detector pulse uses the identical principle of operation, with the input of the peak detector being attenuated by the variable attenuator (IC7) and then the output of this is compared with the input signal using the comparator (IC9). The output of
As the signal previously mentioned, the signal is divided up into two separate channels; one of which acts as the "old" signal, the other as the "new" one. The output of these two signals is then connected to a peak detector, which produces a peak detected pulse. This pulse is used to trigger the amplifiers for each decade of the analyzer, and the output of these amplifiers is then used to drive a cathode follower circuit. The output of this circuit is then sent to a scope, which displays the waveforms of the signal with respect to control. The signal which operates the scope is derived from the peak detected pulse and is fed back.
the comparator is then passed through inverting Schmidt triggers to allow squaring of the signal. The output of the reset comparator is passed through two inverting Schmidt triggers so that it is the correct polarity. The trailing edge of the output of the peak detector comparator is used to drive a 4 micro second mono-stable (IC32), and then this signal and the reset signal are applied to an OR gate, and the output of this is used to drive the control gate of the reset switch (IC18).

5 Switch selection circuit

5.1 Design

As has been previously explained the signal is divided up into eighth separate channels, one of which must be selected for sampling via the sample-and-hold. This board uses the input signal to select between the peak values presented at the switch. This operation is performed by again splitting the signal four ways, one amplifier for each decade, and comparing the output of these amplifiers with fixed voltage reference values. The output of these comparators are then used to drive 10 micro second mono-stables. The output of these mono-stables are fed to a logic network which selects the appropriate switch control. The signal which operates the sample control of the sample-and-hold is also generated on this board.
the comparator is then passed through inverting Schmidt triggers to allow squaring of the signal. The output of the reset comparator is passed through two inverting Schmidt triggers so that it is the correct polarity. The trailing edge of the output of the peak detector comparator is used to drive a 4 micro second mono-stable (IC32), and then this signal and the reset signal are applied to an OR gate, and the output of this is used to drive the control gate of the reset switch (IC18).

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Because of the four different amplification ranges, it is necessary to use some form of representation which applies to the data that is being processed by the analogue-to-digital converter. Due to the fact that only one of the four switches can be selected at any one time the four channels of switch selection data can also be used to represent the multiplication factor. There are a total of eight switch selection lines, four for the positive channel and four for the negative channel. Therefore one nibble represents the positive amplification factor and one the negative amplification factor.

5.2 Operation

The full circuit diagram is shown in Figure A7, sheets one and two.

This circuit is contained on a single printed circuit board which contains all the hardware for both the positive and negative channels. This printed circuit board consists of an input buffer, four channels of amplification voltage references, voltage comparators and a switch selection control network.

The signal is buffered by IC1 to stop the inverting amplifier from loading the output of the resonant circuit. After the buffer the signal is split four
ways, allowing the limits of the four decade ranges to be set. These limits are:

\[ 1 \text{mV} < x < 10 \text{mV} \]
\[ 10 \text{mV} < x < 100 \text{mV} \]
\[ 100 \text{mV} < x < 1 \text{V} \]
\[ 1 \text{V} < x < 10 \text{V} \]

To make the timing delays between the two separate sets of amplifiers as small as possible it was decided to make, with the exception of the highest gain amplifier, all the amplification channels identical. This means that all switching will be carried out in the range 1 to 10V, with the exception of the highest gain amplifier which has a lower limit of 0.25V. The four amplifiers are DC coupled, low offset voltage, low drift, two stage designs with variable DC offset. The only difference between the four amplifiers is in the resistors used to set the amplification factors. The amplification factors are: x250, x100, x10 and x1.

A x250 amplifier is used in order to try and increase stability and decrease drift, which must be done to allow the system to operate correctly.

Following the amplifiers, each channel is split between the positive and negative comparators. The reference signal for these comparators is developed in a circuit which uses a zener diode buffered by a unity gain
operational amplifier buffer. The reason for this buffering is to stop the signals developed in the switching circuit of the comparators from effecting the voltage reference signal.

The output of the voltage reference is adjustable, and is set at a value of 1V (for the positive channel) and -1V (for the negative channel) of the x100, x10 and x1 amplifiers. A value of +0.25V (for the positive channel) and -0.25V (for the negative channel) is used for the x250 amplifier. The voltage comparators are used in a feedforward format, the comparator handling the positive signals with the reference tied to the positive feedback resistor, and the voltage input tied to the inverting input. For the comparator handling the negative signals, the input connection are reversed. The output of the comparator is shown in Figure A8.

The length of time that the output pulse is produced is dependant on the value to which the signal rises above the reference, which is obviously variable between randomly varying signals. Because the peak is held after the signal has passed through zero, it is necessary to maintain the switching pulse for a longer period of time. The output of the comparator is then passed through a Schmidt trigger and a 10 micro second mono stable. Thus the behaviour of each channel of the
Figure A8: Comparator output voltage waveform
switching circuit is entirely predictable.

The Boolean representation to select each switch can be given as follows:

- \( \text{Signal} = A \) for \( >1\text{mV} \)
- \( \text{Signal} = B \) for \( >10\text{mV} \)
- \( \text{Signal} = C \) for \( >100\text{mV} \)
- \( \text{Signal} = D \) for \( >1\text{V} \)

Then:

- \( \text{switch} > 1\text{V} \) signal \( \text{ON} = \overline{A} + \overline{B} + \overline{C} + D \)
- \( \text{switch} > 100\text{mV} \) signal \( \text{ON} = \overline{A} + \overline{B} + C + \overline{D} \)
- \( \text{switch} > 10\text{mV} \) signal \( \text{ON} = \overline{A} + B + \overline{C} + \overline{D} \)
- \( \text{switch} > 1\text{mV} \) signal \( \text{ON} = A + \overline{B} + \overline{C} + \overline{D} \)

and the same for the negative channel.

The switch uses negative logic to control its operation so that the signal developed for the switch is inverted before selection. The input to the switch is used to characterise the multiplication factors as follows:

- for \( >1\text{V} \) signal = 0111
- for \( >100\text{mV} \) signal = 1011
- for \( >10\text{mV} \) signal = 1101
- for \( >1\text{mV} \) signal = 1110

The signals have the following representations:

- 0111 = x1 factor
- 1011 = x10 factor
- 1101 = x100 factor
- 1110 = x1000 factor

and the same for the negative channel.
Because any combination of the four peak detectors is capable of producing a peak detected signal. It is sufficient to know that a peak has been detected for the sampling process to begin. When the signal is greater than 1mV the greater than 1mV ten micro second monostable is activated. The peak detector signal is combined with this signal using an AND gate, which operates as a noise gate removing noise below 1mV. Thus the signal will only be sampled if there is data at the input above the value of 1mV, which means that all noise below the value of 1mV will not be processed.

The input amplifiers for the greater than 1mV channel are shown as IC2 and IC3, the comparator (IC14) compares the signal with the positive reference signal from IC10. The negative reference from IC12 is compared with the signal using IC15. These signals are then shaped by Schmidt triggers and subsequently stretched by IC22 and IC26 respectively. All four channels are identical up to this point.

The switch selection is driven by these channels and consists of a series of inverters and quad-input AND gates.